19-3732; Rev 2; 7/07

EVALUATION KIT AVAILABLE

Stereo Audio CODECs with Microphone, DirectDrive Headphones, Speaker Amplifiers, or Line Outputs

General Description

The MAX9851/MAX9853 are single-chip, stereo audio CODECs designed to provide a complete audio solution for a GSM/GPRS/EDGE cell phone. The MAX9851/MAX9853 provide stereo DirectDrive™ headphone amplifiers, a mono receiver speaker amplifier, stereo Class D speaker amplifiers (MAX9851 only), stereo differential line outputs (MAX9853 only), microphone input amplifiers, plus flexible input selection and gain control. Two serial digital audio interfaces are included, one intended to accept voiceband data and the other accepting I²S data. The voiceband interface can be reconfigured as needed to act as a secondary I²S feed input—allowing multiple audio source mixing of ringer tones or other audio at different sample rates. A transducer/vibrator signal can be derived from digital audio.

The stereo digital-to-analog converter (DAC) path includes filtering and mixing, programmable-gain amplifiers (PGA), soft muting, and optional voiceband digital filtering. The MAX9851/MAX9853 accept up to two digital audio inputs at different sample rates. All analog inputs have PGAs on the front end, allowing dynamic range optimization with a wide range of input sources.

The stereo analog-to-digital converter (ADC) converts audio signals from either internal or external microphones or stereo line inputs. The microphone amplifiers have a programmable gain from 0 to 40dB to handle both amplified microphones and electret modules. In addition to a digital highpass filter to remove DC offset voltages, the ADC also features voiceband digital filtering.

The digital audio interfaces support a variety of serial audio formats. The secondary serial audio interface has an independent supply voltage to allow integration into multiple supply systems. Control for volume levels, signal mixing, and operating modes is done through the I²C 2-wire interface.

All circuitry is optimized for high PSRR. The MAX9851/MAX9853 use a thermally efficient, space-saving 48-pin thin QFN package (7mm x 7mm x 0.8mm) with an exposed pad.

Applications

GSM/GPRS/EDGE Cell Phones

PDAs/SmartPhones

Features

- **+1.7V to +3.3V (Digital) and +2.6V to +3.3V (Analog) Operation**
- **+2.6V to +5.5V Class D Speaker Amplifier Operation (Direct from Battery)**
- **Low 26mW Quiescent Power Consumption (Playback)**
- **High 98dB Power-Supply Rejection Ratio**
- **8kHz to 48kHz Sample Rate (Replay and Record)**
- **Stereo 18-Bit ADC and DAC**
- **Low-Noise Stereo Microphone Inputs and Stereo Line Inputs**
- **Dual Source Digital Mixing (DAC)**
- **Selectable Voiceband Filter for Recording/Playback Modes**
- **Digital Filtering, Soft Mute, and Volume Control**
- **Low-Noise, High-PSRR Microphone Bias Generator**
- **Stereo DirectDrive Headphone Amplifier (2 x 50mW)**
- **Mono DirectDrive Handset Receiver Amplifier (1 x 105mW)**
- **Stereo Class D, Ultra-Low-EMI, Filterless Speaker Amplifier with Active Emissions Limiting (2 x 1.25W, 8Ω) (MAX9851)**
- **Stereo Differential Line Output Amplifiers (MAX9853)**
- **Clickless/Popless Operation**
- **Flexible Shutdown Modes for Power Saving**
- **Comprehensive Headset Detection**
- **Ultra-Low Power Wake-Up on Headset Detection**

Ordering Information

PART	PIN-PACKAGE	PKG CODE
MAX9851ETM+	48 TQFN-EP* (7mm x 7mm x 0.8mm)	T4877-6
MAX9853ETM+	48 TQFN-EP* (7mm x 7mm x 0.8mm)	T4877-6

Note: *All devices specified over the -40°C to +85°C temperature range.*

+Denotes lead-free package.

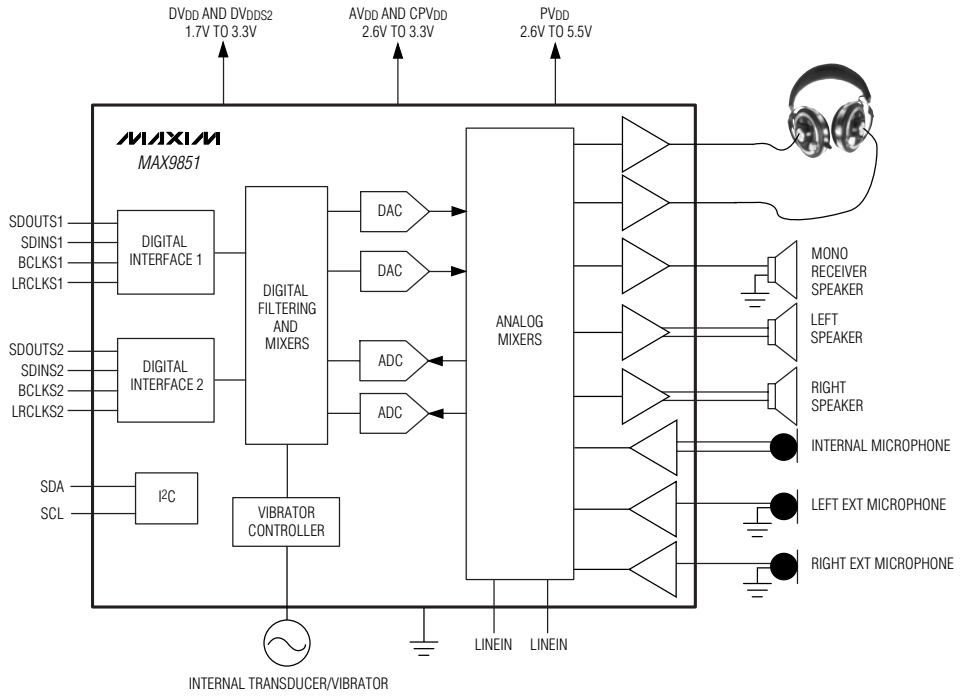
**EP = Exposed pad.*

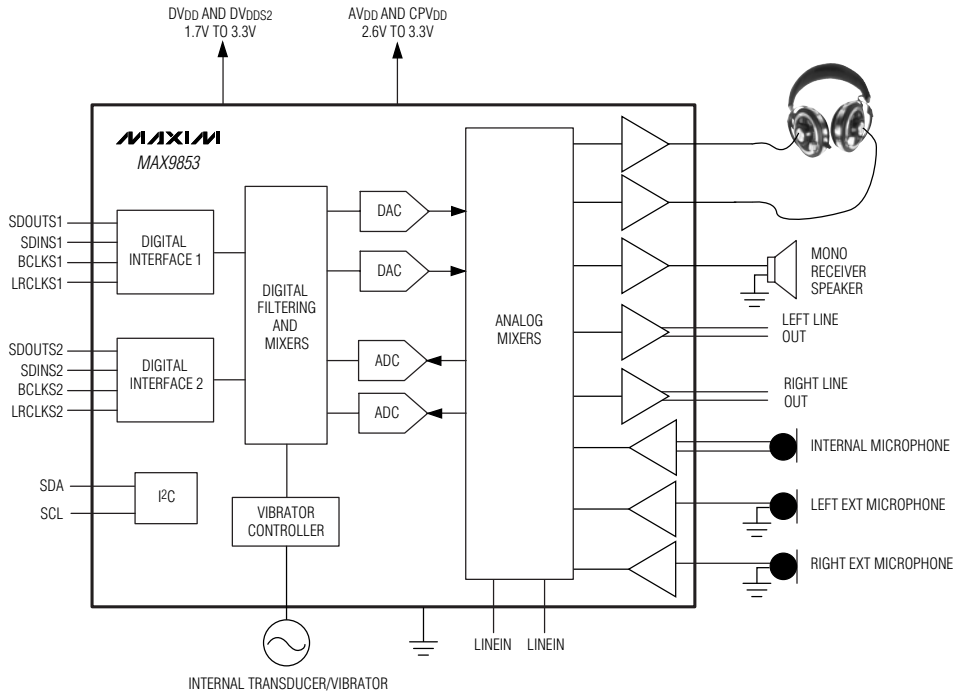
Pin Configurations and Selector Guide appear at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Stereo Audio CODECs with Microphone, DirectDrive Headphones, Speaker Amplifiers, or Line Outputs

Simplified Block Diagrams





ABSOLUTE MAXIMUM RATINGS

(Voltages with respect to AGND)
AV_{DD}, DV_{DD}, DV_{DDS2}, CPV_{DD} .....-0.3V to +4V
PV_{SS}, SV_{SS} .....-4V to +0.3V
PV_{DD}.....-0.3V to +6V
AGND, DGND, CPGND, PGND.....-0.3V to +0.3V
HPL, HPR, REC .....(SV_{SS} - 0.3V) to (AV_{DD} + 0.3V)
LSPK+, LSPK-, RSPK+, RSPK- .....-0.3V to (PV_{DD} + 0.3V)
LINEIN1, LINEIN2.....-2V to +2V
EXTMICBIASL, EXTMICBIASR.....-0.3V to (AV_{DD} + 0.3V)
INTMICP, INTMICN, EXTMICL, EXTMICR.....-2V to +2V
EXTMICGND.....-0.3V to +0.3V
C1N.....(PV_{SS} - 0.3V) to (CPGND + 0.3V)
C1P.....(CPGND - 0.3V) to (CPV_{DD} + 0.3V)
PREG, REF, MBIAS, INTMICBIAS.....-0.3V to (AV_{DD} + 0.3V)
NREG.....+0.3V to (SV_{SS} - 0.3V)
OUTL+, OUTL-, OUTR+, OUTR-,
FAULTIN.....-0.3V to (AV_{CC} + 0.3V)
MCLK, $\overline{IRQ}$, $\overline{VIBE}$, SCL, SDA.....-0.3V to +4V
SHDNOUT .....-0.3V to +6V
LRCLKS1, BCLKS1, SDOUTS1,
SDINS1.....-0.3V to DV_{DD} + 0.3V
LRCLKS2, BCLKS2, SDOUTS2,
SDINS2 .....-0.3V to DV_{DDS2} + 0.3V
Short Circuit to AGND Duration:
HPL, HPR, REC .....Continuous
LSPK+, LSPK-, RSPK+,
RSPK- .....Subject to Maximum Package Power Dissipation
INTMICBIAS, EXTMICBIASL, EXTMICBIASR.....Continuous
Short Circuit to AV_{DD} Duration
EXTMICBIASL, EXTMICBIASR .....Continuous
Current Into/Out of Any Pin (unless otherwise noted).....100mA
Continuous Power Dissipation (T_A = +70°C)
48-Pin Thin QFN (derate 40mW/°C above +70°C) 3200mW
Junction Temperature.....+150°C
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = CPV_{DD} = +3V, DV_{DD} = DV_{DDS2} = +1.8V, PV_{DD} = +3.3V, R_{HP} = 32Ω, Z_{SPK} = 8Ω + 10µH, R_{REC} = 32Ω, R_{OUTL+} to R_{OUTL-} = 10kΩ, R_{OUTR+} to R_{OUTR-} = 10kΩ, C1 = 0.22µF, C2 = C_{NREG} = C_{PREG} = $C_{INTMICBIAS}$, C_{MBIAS} = C_{REF} = 1µF, MCLK = 13MHz, all PGAs = 0dB, HP/REC volume = -20.0dB, SPK volume = -20.4dB, line output gain = -0.4dB, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (See *Functional Diagrams/Typical Operating Circuits*).

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Supply Voltage	AV_{DD}, CPV_{DD}	AV_{DD} = CPV_{DD}, no load		2.6		3.3	V
Digital Supply Voltage	DV_{DD}, DV_{DDS2}	No load		1.7		3.3	V
Speaker Supply Voltage	PV_{DD}	No load		2.6		5.5	V
Analog Supply Current	AI_{DD}	DAC playback mode, no output loads (Note 1)	Stereo headphone		7.2		mA
			Stereo speaker (MAX9851)/line output (MAX9853)		6.5	8.5	
			Mono receiver		6.4		
		Line only playback mode, no output loads	Stereo headphone		5.0		
			Stereo speaker (MAX9851)/line output (MAX9853)		4.6		
			Mono receiver		4.4		
		DAC plus line input playback mode, no output loads (Note 1)	Stereo headphone		7.2		
			Stereo speaker (MAX9851)/line output (MAX9853)		6.4		
			Mono receiver		6.3		

Stereo Audio CODECs with Microphone, DirectDrive Headphones, Speaker Amplifiers, or Line Outputs

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = CPV_{DD} = +3V, DV_{DD} = DV_{DDS2} = +1.8V, PV_{DD} = +3.3V, R_{HP} = 32Ω, Z_{SPK} = 8Ω + 10µH, R_{REC} = 32Ω, R_{OUTL+} to R_{OUTL-} = 10kΩ, R_{OUTR+} to R_{OUTR-} = 10kΩ, C1 = 0.22µF, C2 = C_{NREG} = C_{PREG} = $C_{INTMICBIAS}$, C_{MBIAS} = C_{REF} = 1µF, MCLK = 13MHz, all PGAs = 0dB, HP/REC volume = -20.0dB, SPK volume = -20.4dB, line output gain = -0.4dB, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (See *Functional Diagrams/Typical Operating Circuits*).

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Supply Current	AI_{DD}	Full-duplex voice mode, no output loads	Stereo headphone		11.9		mA
			Stereo speaker (MAX9851)/line output (MAX9853)		11.2		
			Mono receiver		11.1	14.5	
		Full-duplex voice mode plus DAC playback mode, no output loads (Notes 1, 2)	Stereo headphone		11.9		
			Stereo speaker (MAX9851)/line output (MAX9853)		11.2		
			Mono receiver		11.1		
		ADC record mode (Note 3)			12.2		
		ADC record mode plus DAC headphone playback mode (Notes 1, 3)			18.2	24.0	
Speaker Supply Current (Note 4)	PI_{DD}	Mono Class D speaker mode			5		mA
		Stereo Class D speaker mode			10	14	
		Sleep mode (MAX9851, MAX9853)			2	15	µA
Digital Supply Current	DI_{DD}	Playback operation (Note 1), no output loads			2.7	3.7	mA
		Full duplex voice operation (Note 2), no output loads, T_A = +25°C			6.2	7.8	
		Record operation (Notes 1, 3)			3.9	5.2	
Analog Shutdown Current	AI_{SHDN}	I_{AVDD} + I_{CPVDD}, T_A = +25°C			1.4	20	µA
Digital Shutdown Current	DI_{SHDN}	I_{DVDD} + I_{DVDDS2} , T_A = +25°C			0.5	10	µA
PV_{DD} Shutdown Current (Note 4)	PI_{SHDN}	I_{PVDD}, T_A = +25°C	MAX9851		1	20	µA
			MAX9853		0.1	5	
Shutdown to Full Operation	t_{ON}	ADC and DAC fully operational, master mode			70		ms
DAC PERFORMANCE (Note 5) (DAC in Master Mode)							
Gain Error					±1	±7	%
Channel Gain Matching					±1		%
Dynamic Range (Note 6)	DR	f_S = 8kHz (voice modes), headphone volume = +5.5dB			75.5		dB
		f_S = 8kHz and 48kHz (stereo audio modes), headphone volume = +5.5dB		84	87.5		

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = CPV_{DD} = +3V, DV_{DD} = DV_{DDS2} = +1.8V, PV_{DD} = +3.3V, R_{HP} = 32Ω, Z_{SPK} = 8Ω + 10µH, R_{REC} = 32Ω, R_{OUTL+} to R_{OUTL-} = 10kΩ, R_{OUTR+} to R_{OUTR-} = 10kΩ, C1 = 0.22µF, C2 = C_{NREG} = C_{PREG} = $C_{INTMICBIAS}$, C_{MBIAS} = C_{REF} = 1µF, MCLK = 13MHz, all PGAs = 0dB, HP/REC volume = -20.0dB, SPK volume = -20.4dB, line output gain = -0.4dB, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (See *Functional Diagrams/Typical Operating Circuits*).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Total Harmonic Distortion Plus Noise	THD+N	f_{IN} = 1kHz, f_S = 8kHz, 0dBFS (voice mode master mode, ADC and headphone output enabled, no load), headphone volume = +2.5dB		-71.5		dB
		f_{IN} = 1kHz, f_S = 48kHz, 0dBFS (ADC and headphone output enabled, no load), headphone volume = +2.5dB		-84.5		
Signal-to-Noise Ratio (Note 7)	SNR	f_{IN} = 1kHz, f_S = 8kHz and 16kHz (voice modes), headphone volume = +2.5dB		75.5		dB
		f_{IN} = 1kHz, f_S = 8kHz to 48kHz (stereo audio modes), headphone volume = +2.5dB		88		
Crosstalk	XTALK	Driven channel at -1dBFS, f_{IN} = 1kHz, f_S = 8kHz, headphone output (no load)		-95		dB
Power-Supply Rejection Ratio	PSRR	f = 217Hz, V_{RIPPLE} = 100mV_{P-P}		95		dB
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}		68		
DAC DIGITAL FILTERS						
Passband Cutoff	f_{PD}		0.44			f_S
Passband Ripple		f < f_{PD}			±0.2	dB
Stopband Cutoff	f_{SD}				0.58	f_S
Stopband Attenuation		f > f_{SD}	60			dB
Attenuation at f_S / 2				-6.02		dB
DAC VOICEBAND HIGHPASS FILTER (S1 Mono Voice Input Path, f_S = 8kHz, Register 0x07 bit 4 = 1)						
Passband Cutoff	f_{PH}				175	Hz
Passband -3dB Cutoff	f_{P3_H}				130	Hz
Passband Ripple		f > f_{PH}			±0.2	dB
Stopband Cutoff	f_{SH}		77			Hz
Stopband Attenuation		f < f_{SH}	28			dB
DAC VOICEBAND HIGHPASS FILTER (S1 Mono Voice Input Path, f_S = 16kHz, Register 0x07, bit 4 = 1)						
Passband Cutoff	f_{PH}				350	Hz
Passband -3dB Cutoff	f_{P3_H}				260	Hz
Passband Ripple		f > f_{PH}			±0.2	dB
Stopband Cutoff	f_{SH}		154			Hz
Stopband Attenuation		f < f_{SH}	28			dB
DAC VOICEBAND LOWPASS FILTER (S1 Mono Voice Input Path, f_S = 8kHz)						
Passband Cutoff	f_{PL}		3500			Hz
Passband Ripple		f < f_{PL}			±0.05	dB
Stopband Cutoff	f_{SL}				3900	Hz
Stopband Attenuation		f > f_{SL}	75			dB

Stereo Audio CODECs with Microphone, DirectDrive Headphones, Speaker Amplifiers, or Line Outputs

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = CPV_{DD} = +3V, DV_{DD} = DV_{DDS2} = +1.8V, PV_{DD} = +3.3V, R_{HP} = 32Ω, Z_{SPK} = 8Ω + 10µH, R_{REC} = 32Ω, R_{OUTL+} to R_{OUTL-} = 10kΩ, R_{OUTR+} to R_{OUTR-} = 10kΩ, C1 = 0.22µF, C2 = C_{NREG} = C_{PREG} = $C_{INTMICBIAS}$, C_{MBIAS} = C_{REF} = 1µF, MCLK = 13MHz, all PGAs = 0dB, HP/REC volume = -20.0dB, SPK volume = -20.4dB, line output gain = -0.4dB, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (See *Functional Diagrams/Typical Operating Circuits*).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC VOICEBAND LOWPASS FILTER (S1 Mono Voice Audio Input Path, f_S = 16kHz)						
Stopband Cutoff	f_{PL}		7000			Hz
Passband Ripple		$f < f_{PL}$			±0.05	dB
Stopband Cutoff	f_{SL}				7800	Hz
Stopband Attenuation		$f > f_{SL}$	75			dB
DAC ADJUSTABLE HIGHPASS FILTER						
DC Attenuation	DC_{ATT}	Register 0x07 bits [3:0] = 0x5, 0xA, or 0xF		90		dB
Highpass Cutoff (-3dB)	f_P	Register 0x07 [3:0] = 0x5	55		91	Hz
		Register 0x07 [3:0] = 0xA	171		279	
		Register 0x07 [3:0] = 0xF	327		533	
DAC INPUT GAIN CONTROL (Register 0x0C and 0x0D)						
Gain Control Range		For both input data interfaces	-96		0	dB
ADC DC ACCURACY						
Gain Error				±1	±7	%
Full-Scale Conversion	0dBFS	f_{IN} = 1kHz, line input, PGA = 0dB		2.05		V_{P-P}
Channel Gain Matching				±1		%
ADC DYNAMIC SPECIFICATIONS (Note 8)						
Dynamic Range (Note 6)	DR	BW = 22Hz to f_S / 2 (8kHz voice modes)	73	75		dB
		BW = 22Hz to 20kHz (48kHz stereo audio modes, A-weighted), T_A = +25°C	77	82		
		BW = 22Hz to 20kHz (48kHz stereo audio modes, A-weighted), T_A = T_{MIN} to T_{MAX}	71			
		BW = 22Hz to f_S / 2 (8kHz audio mode)		-85.5		
Total Harmonic Distortion	THD	1kHz, 0dBFS, f_S = 8kHz (voice mode)		-85.5		dB
		1kHz, 0dBFS, f_S = 48kHz (stereo audio mode)		-85.5		
Signal-to-Noise Ratio	SNR	1kHz, 0dBFS, f_S = 8kHz (voice mode)		75		dB
		1kHz, 0dBFS, f_S = 48kHz (stereo audio mode, A-weighted)		81.5		
		1kHz, 0dBFS, f_S = 8kHz (stereo audio mode, A-weighted)		87.5		
Channel Crosstalk		Driven channel at -1dBFS, f_{IN} = 1kHz, f_S = 48kHz (from MICL to ADCR or MICR to ADCL)		-75		dB
Power-Supply Rejection Ratio (Note 9)	PSRR	AV_{DD} = 2.6V to 3.3V	48	63		dB
		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}		63		
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}		50		

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = CPV_{DD} = +3V, DV_{DD} = DV_{DDS2} = +1.8V, PV_{DD} = +3.3V, R_{HP} = 32Ω, Z_{SPK} = 8Ω + 10µH, R_{REC} = 32Ω, R_{OUTL+} to R_{OUTL-} = 10kΩ, R_{OUTR+} to R_{OUTR-} = 10kΩ, C1 = 0.22µF, C2 = C_{NREG} = C_{PREG} = $C_{INTMICBIAS}$, C_{MBIAS} = C_{REF} = 1µF, MCLK = 13MHz, all PGAs = 0dB, HP/REC volume = -20.0dB, SPK volume = -20.4dB, line output gain = -0.4dB, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (See *Functional Diagrams/Typical Operating Circuits*).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC DIGITAL FILTER PATH (Stereo Audio Modes)						
Passband Cutoff	f_{PBL}		0.44			f_S
Passband Ripple		$f < f_{PBL}$			±0.5	dB
Stopband Cutoff	f_{SBL}				0.58	f_S
Stopband Attenuation		$f > f_{SBL}$	53			dB
Attenuation at $f_S/2$				-6.02		dB
ADC VOICEBAND HIGHPASS FILTER (S1 Mono Voice Input Path, f_S = 8kHz)						
Passband Cutoff	f_{PH}				175	Hz
Passband -3dB Cutoff	f_{P3_H}				130	Hz
Passband Ripple		$f > f_{PH}$			±0.2	dB
Stopband Cutoff	f_{SH}		77			Hz
Stopband Attenuation		$f < f_{SH}$	28			dB
ADC VOICEBAND HIGHPASS FILTER (S1 Mono Voice Input Path, f_S = 16kHz)						
Passband Cutoff	f_{PH}				350	Hz
Passband -3dB Cutoff	f_{P3_H}				260	Hz
Passband Ripple		$f > f_{PH}$			±0.2	dB
Stopband Cutoff	f_{SH}		154			Hz
Stopband Attenuation		$f < f_{SH}$	28			dB
ADC VOICEBAND LOWPASS FILTER (S1 Mono Voice Input Path, f_S = 8kHz)						
Passband Cutoff	f_{PL}		3500			Hz
Passband Ripple		$f < f_{PL}$			±0.05	dB
Stopband Cutoff	f_{SL}				3900	Hz
Stopband Attenuation		$f > f_{SL}$	75			dB
ADC VOICEBAND LOWPASS FILTER (S1 Mono Voice Input Path, f_S = 16kHz)						
Passband Cutoff	f_{PL}		7000			Hz
Passband Ripple		$f < f_{PL}$			±0.05	dB
Stopband Cutoff	f_{SL}				7800	Hz
Stopband Attenuation		$f > f_{SL}$	75			dB
ADC DC-BLOCKING FILTER						
DC-Blocking Filter -3dB Corner	f_C	As a fraction of output sample rate		f_S / 1608		Hz
DC Attenuation				120		dB
Maximum DC Input				0.125		V
DAC/ADC DATA RATE ACCURACY						
LRCLK Output Sample Rate Deviation From Ideal (Note 10)		f_S = 8kHz to 48kHz (master mode with DAC only enabled) (See Table 1 for details)	-0.025		+0.025	%

Stereo Audio CODECs with Microphone, DirectDrive Headphones, Speaker Amplifiers, or Line Outputs

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = CPV_{DD} = +3V, DV_{DD} = DV_{DDS2} = +1.8V, PV_{DD} = +3.3V, R_{HP} = 32Ω, Z_{SPK} = 8Ω + 10µH, R_{REC} = 32Ω, R_{OUTL+} to R_{OUTL-} = 10kΩ, R_{OUTR+} to R_{OUTR-} = 10kΩ, C1 = 0.22µF, C2 = C_{NREG} = C_{PREG} = $C_{INTMICBIAS}$, C_{MBIAS} = C_{REF} = 1µF, MCLK = 13MHz, all PGAs = 0dB, HP/REC volume = -20.0dB, SPK volume = -20.4dB, line output gain = -0.4dB, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (See *Functional Diagrams/Typical Operating Circuits*).

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DAC/ADC DATA RATE ACCURACY							
LRCLK Output Sample Rate Deviation From Ideal (Note 10)		Master mode with ADC SDOUT enabled; audio mode, unless otherwise noted	f_S = 8kHz (voice mode)		0		%
			f_S = 16kHz (voice mode)		0		
			f_S = 8kHz		0.31		
			f_S = 11.025kHz		0.27		
			f_S = 12kHz		0.31		
			f_S = 16kHz		-0.43		
			f_S = 22.05kHz		-0.41		
			f_S = 24kHz		0.31		
			f_S = 32kHz		-0.43		
			f_S = 44.1kHz		-1.74		
			f_S = 48kHz		-0.43		
LRCLK Input Sample Rate Range		Synchronous or asynchronous input (slave mode with only DAC enabled)		7.8		50	kHz
DAC TRANSDUCER/VIBE OUTPUT							
Vibe PGA Range	TGAIN	11 steps in 6dB increments		-30		+30	dB
0dBFS Output Voltage		1-bit DAC output externally filtered pullup resistor to DV_{DD} (TGAIN = 0dB)			DV_{DD} / 2		V_{P-P}
Output Offset Voltage		1-bit DAC output externally filtered, no signal, pullup resistor to DV_{DD}			DV_{DD} / 2		V
Vibe PGA Output Resolution	PGAR				10		bits
LPF Passband -3dB Cutoff	f_{PBL}	f_S = 8kHz, 16kHz, or 32kHz			483		Hz
		f_S = 11.025kHz, 22.05kHz, or 44.1kHz			665		
		f_S = 12kHz, 24kHz, or 48kHz			724		
LPF Stopband Attenuation	f_{SBL}	f > 3.5xf_{PBL}		27			dB
1-Bit DAC Digital Dynamic Range	DR_V	Ideal dynamic range (0 to 8kHz or 0 to f_S / 2 for f_S < 16kHz)			48		dB
1-Bit DAC Operating Frequency	f_V				650		kHz
OPEN-DRAIN DIGITAL OUTPUT ($\overline{VIBE}$)							
Output High Current	I_{OH}	V_{OUT} = DV_{DD}				3	µA
Output Low Voltage	V_{OL}	I_{OL} = 3mA				0.4	V

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = CPV_{DD} = +3V, DV_{DD} = DV_{DDS2} = +1.8V, PV_{DD} = +3.3V, R_{HP} = 32Ω, Z_{SPK} = 8Ω + 10µH, R_{REC} = 32Ω, R_{OUTL+} to R_{OUTL-} = 10kΩ, R_{OUTR+} to R_{OUTR-} = 10kΩ, C1 = 0.22µF, C2 = C_{NREG} = C_{PREG} = $C_{INTMICBIAS}$, C_{MBIAS} = C_{REF} = 1µF, MCLK = 13MHz, all PGAs = 0dB, HP/REC volume = -20.0dB, SPK volume = -20.4dB, line output gain = -0.4dB, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (See *Functional Diagrams/Typical Operating Circuits*).

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
HEADPHONE AMPLIFIERS							
Output Power	P_{OUT}	f = 1kHz, THD < 1%, volume +5.5dB	R_L = 16Ω		80		mW
			R_L = 32Ω	30	55		
0dBFS Output Voltage		+4.5dB volume setting, input is full-scale signal from the audio DAC		3.14	3.38	3.62	V_{P-P}
Line In to HP Out Voltage Gain		+4.5dB volume setting	Stereo/mono	1.54	1.66	1.78	V/V
			Balanced mono	3.1	3.35	3.6	
Output Offset Voltage	V_{OS}				10	40	mV
Total Harmonic Distortion Plus Noise	THD+N	R_L = 32Ω, P_{OUT} = 50mW, f = 1kHz, BW = 22Hz to 20kHz			0.03		%
		R_L = 16Ω, P_{OUT} = 60mW, f = 1kHz, BW = 22Hz to 20kHz			0.03		
Dynamic Range	DR	+5.5dB volume setting (DAC input to HP output), A-weighted		70	87.5		dB
Power-Supply Rejection Ratio (DAC Input to HP Out)	PSRR	AV_{CC} = 2.6V to 3.6V		60	95		dB
		V_{RIPPLE} = 100mV_{P-P}, f = 217Hz			95		
		V_{RIPPLE} = 100mV_{P-P}, f = 10kHz			68		
Maximum Capacitive Load	C_L	No sustained oscillations			150		pF
Crosstalk (Line Input to Headphone Output)		R_L = 32Ω, P_{OUT} = 1.6mW, f = 1kHz			-85		dB
Channel Gain Matching	AV_{MATCH}	Line input to headphone output			±1		%
Click-and-Pop Level	K_{CP}	Peak voltage, 32-samples per second, A-weighted, R_L = 32Ω (Note 11)	Into shutdown, HP disabled		-53		dBV
			Out of shutdown, HP enabled		-48		
SPEAKER AMPLIFIERS (MAX9851) (Note 12)							
Output Power	P_{OUT}	f = 1kHz, 2V_{P-P} line input, +13.1dB speaker amp volume setting	PV_{DD} = 3.3V, THD+N < 1%	R_L = 8Ω	500		mW
			PV_{DD} = 5V, THD+N < 1%	R_L = 8Ω	1150		
			PV_{DD} = 3.3V, THD+N < 10%	R_L = 8Ω	600		
			PV_{DD} = 5V, THD+N < 10%	R_L = 8Ω	1250		
0dBFS Output Voltage		+12.1dB volume setting, P_{VDD} = +5V			8.4		V_{P-P}

Stereo Audio CODECs with Microphone, DirectDrive Headphones, Speaker Amplifiers, or Line Outputs

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = CPV_{DD} = +3V, DV_{DD} = DV_{DDS2} = +1.8V, PV_{DD} = +3.3V, R_{HP} = 32Ω, Z_{SPK} = 8Ω + 10µH, R_{REC} = 32Ω, R_{OUTL+} to R_{OUTL-} = 10kΩ, R_{OUTR+} to R_{OUTR-} = 10kΩ, C1 = 0.22µF, C2 = C_{NREG} = C_{PREG} = $C_{INTMICBIAS}$, C_{MBIAS} = C_{REF} = 1µF, MCLK = 13MHz, all PGAs = 0dB, HP/REC volume = -20.0dB, SPK volume = -20.4dB, line output gain = -0.4dB, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (See *Functional Diagrams/Typical Operating Circuits*).

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Line In to Speaker Out Voltage Gain		+12.1dB volume setting, P_{VDD} = +5V		4.0	4.2	4.4	V/V
Output Offset Voltage	V_{OS}				10	100	mV
Total Harmonic Distortion Plus Noise	THD+N	R_L = 8Ω, P_{OUT} = 125mW, f = 1kHz, BW = 22Hz to 20kHz, +10.1dB volume setting			0.03		%
Dynamic Range	DR	+12.1dB volume setting, A-weighted			90		dB
Power-Supply Rejection Ratio	PSRR	PV_{DD} = 2.6V to 5.5V		50	70		dB
		V_{RIPPLE} = 100mV_{P-P}, f = 217Hz			70		
		V_{RIPPLE} = 100mV_{P-P}, f = 10kHz			55		
Crosstalk		R_L = 8Ω, P_{OUT} = 100mW, f = 1kHz			60		dB
Channel Gain Matching	AV_{MATCH}				±4		%
Class D Switching Frequency					1100		kHz
Click-and-Pop Level	K_{CP}	Peak voltage, 32-samples per second, A-weighted R_L = 8Ω (Note 11)	Into shutdown		-35		dBV
			Out of shutdown		-35		
Efficiency		P_{OUT} = 1W per channel, R_L = 8Ω			75		%
LINE OUTPUT AMPLIFIERS (MAX9853) (Note 12)							
Line Output Common-Mode Voltage				1.13	1.23	1.33	V
Line Output Differential Offset Voltage				-90		+90	mV
Maximum Differential Output Voltage				3.16	4.16	4.74	V_{P-P}
Dynamic Range	DR	1.4mV_{RMS} (-60dB) output voltage, A-weighted			88		dB
Total Harmonic Distortion Plus Noise	THD+N	f_{IN} = 1kHz, V_{OUT} = 2V_{P-P}, BW = 22Hz to 20kHz			0.004		%
Power-Supply Rejection Ratio	PSRR	AV_{DD} = 2.6V to 3.6V		57	100		dB
		V_{RIPPLE} = 100mV_{P-P}, f = 217Hz			95		
		V_{RIPPLE} = 100mV_{P-P}, f = 20kHz			55		
Line Input to Line Output Gain Accuracy				-0.4		+0.6	dB

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = CPV_{DD} = +3V, DV_{DD} = DV_{DDS2} = +1.8V, PV_{DD} = +3.3V, R_{HP} = 32Ω, Z_{SPK} = 8Ω + 10µH, R_{REC} = 32Ω, R_{OUTL+} to R_{OUTL-} = 10kΩ, R_{OUTR+} to R_{OUTR-} = 10kΩ, C1 = 0.22µF, C2 = C_{NREG} = C_{PREG} = $C_{INTMICBIAS}$, C_{MBIAS} = C_{REF} = 1µF, MCLK = 13MHz, all PGAs = 0dB, HP/REC volume = -20.0dB, SPK volume = -20.4dB, line output gain = -0.4dB, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (See *Functional Diagrams/Typical Operating Circuits*).

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RECEIVER AMPLIFIER (Note 12)							
Output Power	P_{OUT}	f = 1kHz, THD < 1%, +5.5dB volume setting	R_L = 16Ω, input signal from LINEIN1		80		mW
			R_L = 16Ω, input signal is the sum of LINEIN1+LINEIN2		105		
			R_L = 32Ω, input signal from LINEIN1	35	55		
Maximum Output Voltage		+4.5dB volume setting, 0dB PGA setting, input signal 0dBFS from DAC output, only 1 input selected		3.09	3.35	3.64	V_{P-P}
Line In to REC Out Voltage Gain		+4.5dB volume setting, 0dB PGA setting, only 1 input selected		1.54	1.68	1.82	V/V
Output Offset Voltage	V_{OS}				10	60	mV
Total Harmonic Distortion Plus Noise	THD+N	R_L = 32Ω, P_{OUT} = 40mW, f = 1kHz, BW = 22Hz to 20kHz, +3dB volume setting			0.03		%
		R_L = 16Ω, P_{OUT} = 40mW, f = 1kHz, BW = 22Hz to 20kHz, +3dB volume setting			0.04		
Dynamic Range	DR	+6dB volume setting, A-weighted			92		dB
Power-Supply Rejection Ratio	PSRR	AV_{DD} = 2.6V to 3.3V		60	100		dB
		V_{RIPPLE} = 100mV_{P-P}, f = 217Hz			98		
		V_{RIPPLE} = 100mV_{P-P}, f = 20kHz			65		
Maximum Capacitive Load	C_L	No sustained oscillations			150		pF
Click-and-Pop Level	K_{CP}	Peak voltage, 32 samples per second, A-weighted, R_L = 16Ω (Note 11)			-44.6		dBV
VOLUME CONTROL/PGAs							
Headphone/Receiver Volume Control Range				-80		+6.1	dB
Headphone/Receiver Mute Attenuation		f = 1kHz			100		dB
Speaker Volume Control Range (MAX9851)				-72.4		+13.7	dB
Speaker Mute Attenuation (MAX9851)		f = 1kHz			100		dB
Differential Line Output Gain Control Range (MAX9853)				-78.4		+7.9	dB
Differential Line Output Mute Attenuation (MAX9853)		f = 1kHz			100		dB

Stereo Audio CODECs with Microphone, DirectDrive Headphones, Speaker Amplifiers, or Line Outputs

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = CPV_{DD} = +3V, DV_{DD} = DV_{DDS2} = +1.8V, PV_{DD} = +3.3V, R_{HP} = 32Ω, Z_{SPK} = 8Ω + 10µH, R_{REC} = 32Ω, R_{OUTL+} to R_{OUTL-} = 10kΩ, R_{OUTR+} to R_{OUTR-} = 10kΩ, C1 = 0.22µF, C2 = C_{NREG} = C_{PREG} = $C_{INTMICBIAS}$, C_{MBIAS} = C_{REF} = 1µF, MCLK = 13MHz, all PGAs = 0dB, HP/REC volume = -20.0dB, SPK volume = -20.4dB, line output gain = -0.4dB, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (See *Functional Diagrams/Typical Operating Circuits*).

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Sidetone Volume Control Range				-34.0		+30.5	dB
Sidetone Mute Attenuation		f = 1kHz, sidetone deselected from input mixer			80		dB
CHARGE PUMP							
Charge-Pump Oscillator Frequency	f_{OSC}			295	650	1200	kHz
MICROPHONE AMPLIFIERS							
Preamplifier Gain	AV_{PRE}	EXTMIC_	AV_{PRE} = +20dB	+18.5		+20.5	dB
			AV_{PRE} = +20dB	-0.9		+0.4	
MIC PGA Gain	AV_{MICPGA}	PGA gain = 0dB		-0.9		+0.4	dB
		PGA gain = +20dB		+18.5		+20.5	
MIC Mute Attenuation		f = 1kHz			105		dB
Common-Mode Rejection Ratio	CMRR	EXTMIC_, V_{IN} = 100mV_{P-P} at 217Hz, AV_{PRE} = +20dB			80		dB
MIC Input Voltage Range		INTMIC_, EXTMIC_		-1		+1	V
		EXTMICGND		-0.1		+0.1	
MIC Input Resistance	R_{IN_MIC}	INTMIC_, EXTMIC_		30	50	70	kΩ
MIC GND Sense Input Resistance	R_{IN_MICS}	EXTMICGND		15	25	36	kΩ
MIC Input Resistance Matching	R_{MATCH}	INTMICP to INTMICN or EXTMICL to EXTMICR			0.3		%
MIC Input Bias Voltage	V_{CML}	Measured at INTMIC_, EXTMIC_, and EXTMICGND		-0.1	0	+0.1	V
Input Voltage Noise	E_{IN_MIC}	f = 1kHz, AV_{PRE} = +20dB, R_{SOURCE} = 0Ω			25		nV/√Hz
Total Harmonic Distortion Plus Noise	THD+N	AV_{PRE} = 0dB, AV_{MICPGA} = 0dB, V_{IN} = 2V_{P-P}, f = 1kHz, BW = 22Hz to 20kHz			0.035		%
		AV_{PRE} = +20dB, AV_{MICPGA} = 0dB, V_{IN} = 200mV_{P-P}, f = 1kHz, BW = 22Hz to 20kHz			0.035		
		AV_{PRE} = +20dB, AV_{MICPGA} = +20dB, V_{IN} = 20mV_{P-P}, f = 1kHz, BW = 22Hz to 20kHz			0.06		
MIC Power-Supply Rejection Ratio	PSRR	AV_{DD} = 2.6V to 3.3V, T_A = +25°C		48	65		dB
		V_{RIPPLE} = 100mV_{P-P} at 217Hz, output referred			65		dB
		V_{RIPPLE} = 100mV_{P-P} at 10kHz, output referred			65		dB

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = CPV_{DD} = +3V, DV_{DD} = DV_{DDS2} = +1.8V, PV_{DD} = +3.3V, R_{HP} = 32Ω, Z_{SPK} = 8Ω + 10µH, R_{REC} = 32Ω, R_{OUTL+} to R_{OUTL-} = 10kΩ, R_{OUTR+} to R_{OUTR-} = 10kΩ, C1 = 0.22µF, C2 = C_{NREG} = C_{PREG} = $C_{INTMICBIAS}$, C_{MBIAS} = C_{REF} = 1µF, MCLK = 13MHz, all PGAs = 0dB, HP/REC volume = -20.0dB, SPK volume = -20.4dB, line output gain = -0.4dB, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (See *Functional Diagrams/Typical Operating Circuits*).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MICROPHONE BIAS						
INTMICBIAS Output Voltage	$V_{MICBIAS}$		2.3	2.4	2.5	V
INTMICBIAS Load Regulation		$I_{MICBIAS}$ = 0 to 2mA		0.7	10	Ω
INTMICBIAS Minimum Capacitive Load				1		µF
INTMICBIAS Short-Circuit Current		To AGND		15		mA
INTMICBIAS Power-Supply Rejection Ratio	PSRR	AV_{DD} = 2.6V to 3.3V, T_A = +25°C		72		dB
		V_{RIPPLE} = 100mV at 217Hz		85		dB
		V_{RIPPLE} = 100mV at 10kHz		70		dB
INTMICBIAS Noise Voltage	V_{NOISE}	f = 22Hz to 20kHz		2.8		μV_{RMS}
		f = 1kHz		20		$nV/\sqrt{Hz}$
EXTMICBIAS_ Output Impedance	R_{EXTMIC}	2.2kΩ setting	2.00		2.42	kΩ
		470Ω setting	425		515	Ω
EXTMICBIAS_ Off-Impedance		$V_{EXTMICBIAS_}$ = 0 to 3.0V	1	2		MΩ
LINE INPUT (Note 13)						
Line Input Maximum Input Voltage				2		V_{P-P}
Line Input Resistance	R_{IN}		10	20		kΩ
Line Channel-to-Channel Gain Matching	AV_{MATCH}			±1		%
PGA Gain Range			-34.0		+30.5	dB
HEADSET AUTO-DETECT (Normal Operation)						
MIC Sense High Threshold	V_{TH1}	MIC bias and bias resistor enabled	0.92 x $V_{MICBIAS}$	0.95 x $V_{MICBIAS}$	0.98 x $V_{MICBIAS}$	V
MIC Sense Low Threshold	V_{TH2}	MIC bias and bias resistor enabled	0.06 x $V_{MICBIAS}$	0.1 x $V_{MICBIAS}$	0.17x $V_{MICBIAS}$	V
MIC Sense Deglitch Period	t_{GLITCH}	Pulses shorter than $t_{GLITCH1}$ are eliminated		20		ms
Headphone Sense Current	I_{SENSE}	V_{HPL} / V_{HPR} = AGND (headphones disabled)		3.4	5	µA
Headphone Sense Voltage	V_{SENSE}	HPR/HPL (headphone amplifiers disabled)		AV_{DD}		V
		Test 2 (HPTEST = 1) - HPR only		0		
Headphone Sense Threshold	V_{TH3}		0.74 x AV_{DD}	0.73 x AV_{DD}	0.82 x AV_{DD}	V
SLEEP MODE (AV_{CC} = 0V or 3V)						
MIC Sense Current	I_{MIC}	EXTMICBIASL = AGND		3	10	µA
MIC Sense Voltage	V_{MIC}			PV_{DD}		V
MIC Sense Sleep Threshold	V_{TH4}	Voltage at EXTMICBIASL	0.9	2	2.7	V

Stereo Audio CODECs with Microphone, DirectDrive Headphones, Speaker Amplifiers, or Line Outputs

TIMING CHARACTERISTICS

(AV_{DD} = CPV_{DD} = +3V, DV_{DD} = DV_{DDS2} = +1.8V, PV_{DD} = +3.3V, R_{HP} = 32Ω, Z_{SPK} = 8Ω + 10µH, R_{REC} = 32Ω, R_{OUTL+} to R_{OUTL-} = 10kΩ, R_{OUTR+} to R_{OUTR-} = 10kΩ, C1 = 0.22µF, C2 = C_{NREG} = C_{PREG} = $C_{INTMICBIAS}$, C_{MBIAS} = C_{REF} = 1µF, MCLK = 13MHz, all PGAs = 0dB, HP/REC volume = -20.0dB, SPK volume = -20.4dB, line output gain = -0.4dB, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (See *Functional Diagrams/Typical Operating Circuits*).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CLOCK CHARACTERISTICS						
MCLK Input Frequency	f_{MCLK}			13 / 26		MHz
MCLK Duty Cycle			45	50	55	%
Maximum MCLK Jitter		Maximum allowable RMS for performance limits		100		ps_{RMS}
DIGITAL INPUTS (BCLKS_, LRCLKS_, SDINS_, MCLK, SDA, SCL, FAULTIN)						
Input-Voltage High	V_{IH}		0.7 x DV_{DD}			V
Input-Voltage Low	V_{IL}				0.3 x DV_{DD}	V
Input Hysteresis				200		mV
Input Leakage Current	I_{IH}, I_{IL}		-3		+3	µA
FAULTIN Input Low Leakage Current (MAX9853)	I_{IL}	FAULTIN has internal pullup resistor			30	µA
FAULTIN Input High Leakage Current (MAX9853)	I_{IH}				3	µA
Input Capacitance				10		pF
CMOS DIGITAL OUTPUTS (BCLKS_, LRCLKS_, SDOUTS_)						
Output Low Voltage	V_{OL}	I_{OL} = 3mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = 3mA	DV_{DD} - 0.4			V
DIGITAL AUDIO INTERFACE TIMING CHARACTERISTICS (Digital Audio Interface S1 and S2)						
BCLK Cycle Time	t_{BCLKS}	Slave operation	75			ns
	t_{BCLKM}	Master operation		308		ns
BCLK High Time	t_{BCLKH}	Slave operation	30			ns
BCLK Low Time	t_{BCLKL}	Slave operation	30			ns
BCLK_ or LRCLK_ Rise and Fall Time	t_r, t_f	Master operation, C_L = 15pF		7		ns
SDIN_ or LRCLK_ to BCLK_ Rising Set-Up Time	t_{SU}	BCI = 0 (see I^2C register definition)	30			ns
SDIN_ or LRCLK_ to BCLK_ Rising Hold Time	t_{HD}	BCI = 0 (see I^2C register definition)	5			ns
SDOUTS1 Delay Time	t_{DLY}	BCI = 0 (see I^2C register definition), C_L = 30pF			35	ns
SDOUTS2 Delay Time	t_{DLY}	BCI = 0 (see I^2C register definition), C_L = 30pF			50	ns

TIMING CHARACTERISTICS (continued)

(AV_{DD} = CPV_{DD} = +3V, DV_{DD} = DV_{DDS2} = +1.8V, PV_{DD} = +3.3V, R_{HP} = 32Ω, Z_{SPK} = 8Ω + 10µH, R_{REC} = 32Ω, R_{OUTL+} to R_{OUTL-} = 10kΩ, R_{OUTR+} to R_{OUTR-} = 10kΩ, C1 = 0.22µF, C2 = C_{NREG} = C_{PREG} = $C_{INTMICBIAS}$, C_{MBIAS} = C_{REF} = 1µF, MCLK = 13MHz, all PGAs = 0dB, HP/REC volume = -20.0dB, SPK volume = -20.4dB, line output gain = -0.4dB, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (See *Functional Diagrams/Typical Operating Circuits*).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOICE MODE TIMING CHARACTERISTICS (Digital Audio Interface S1 and S2)						
BCLK_ Cycle Time	t_{BC}		75			ns
BCLK_ High Time	t_{BH}		30			ns
BCLK_ Low Time	t_{BL}		30			ns
BCLK_ or LRCLK_ Rise and Fall Time	t_r, t_f	Master mode, C_{LOAD} = 15pF		7		ns
SDIN_ or LRCLK_ to BCLK_ Rising Edge Setup Time	t_{SU}	BCI = 0 (see I^2C register definition)	30			ns
SDIN_ or LRCLK_ to BCLK_ Rising Edge Hold Time	t_{HD}	BCI = 0 (see I^2C register definition)	5			ns
SDOUTS1 Delay Time	t_{DLY}	BCI = 0 (see I^2C register definition), from BCLK rising edge			35	ns
SDOUTS2 Delay Time	t_{DLY}	BCI = 0 (see I^2C register definition), from BCLK rising edge			50	ns
OPEN-DRAIN DIGITAL OUTPUTS (SDA, $\overline{IRQ}$)						
Output High Current	I_{OH}	V_{OUT} = DV_{DD}			3	µA
Output Low Voltage	V_{OL}	I_{OL} = 3mA for DV_{DD} > 2V			0.4	V
		I_{OL} = 3mA for DV_{DD} < 2V			0.2 x DV_{DD}	
OPEN-DRAIN DIGITAL OUTPUT (SHDNOUT) (MAX9853 Only)						
Output High Current	I_{OH}	V_{OUT} = DV_{DD}			3	µA
Output Low Voltage	V_{OL}	I_{OL} = 100µA			0.4	V
I^2C TIMING CHARACTERISTICS						
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.6			µs
SCL Pulse Width Low	t_{LOW}		1.3			µs
SCL Pulse Width High	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			µs

Stereo Audio CODECs with Microphone, DirectDrive Headphones, Speaker Amplifiers, or Line Outputs

TIMING CHARACTERISTICS (continued)

(AV_{DD} = CPV_{DD} = +3V, DV_{DD} = DV_{DDS2} = +1.8V, PV_{DD} = +3.3V, R_{HP} = 32Ω, Z_{SPK} = 8Ω + 10µH, R_{REC} = 32Ω, R_{OUTL+} to R_{OUTL-} = 10kΩ, R_{OUTR+} to R_{OUTR-} = 10kΩ, C1 = 0.22µF, C2 = C_{NREG} = C_{PREG} = $C_{INTMICBIAS}$, C_{MBIAS} = C_{REF} = 1µF, MCLK = 13MHz, all PGAs = 0dB, HP/REC volume = -20.0dB, SPK volume = -20.4dB, line output gain = -0.4dB, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (See *Functional Diagrams/Typical Operating Circuits*).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Hold Time	$t_{HD,DAT}$		0		900	ns
Data Setup Time	$t_{SU,DAT}$		100			ns
SDA and SCL Receiving Rise Time	t_r	(Note 14)	$20+0.1C_b$		300	ns
SDA and SCL Receiving Fall Time	t_f	(Note 14)	$20+0.1C_b$		300	ns
SDA Transmitting Fall Time	t_f	DV_{DD} = 1.8V (Note 14)	$20+0.1C_b$		250	ns
		DV_{DD} = 3.3V (Note 14)	$20+0.05C_b$		250	
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			µs
Bus Capacitance	C_b				400	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns

Note 1: DAC playback mode is defined as clocking all zeros into the DAC which operates in stereo audio mode at the 48kHz sample rate in master mode.

Note 2: Full-duplex voice mode is defined as operating the DAC and ADC in mono 8kHz voice mode with line inputs, microphone inputs, and an analog output enabled.

Note 3: Record operation is defined as operating the stereo ADC with the stereo external microphone inputs enabled at the 48kHz sample rate in master mode.

Note 4: Speaker output available only on the MAX9851. PV_{DD} powers only the headset autodetect circuitry when in sleep mode on the MAX9853.

Note 5: DAC performance measured at headphone outputs.

Note 6: Dynamic range measured using the EIAJ method. The input is applied at -60dBFS, f_{IN} = 1kHz. The THD+N referred to 0dBFS A-weighted.

Note 7: The SNR is referred to 0dBFS A-weighted.

Note 8: ADC performance measured from line inputs (unless otherwise noted).

Note 9: Microphone amplifiers connected to ADC, mic inputs AC-grounded.

Note 10: In master-mode operation, sample clock rate is proportional to MCLK input.

Note 11: Speaker amplifier testing performed with 8Ω resistive load in series with a 68µH inductive load connected across BTL outputs. Headphone and receiver amplifier testing performed with 32Ω resistive load connected to GND. Mode transitions are controlled by toggling the amplifier on and off using the corresponding enable bit. Units expressed in dBV.

Note 12: Input signal for speaker, line output, and receiver output performance measured using line inputs.

Note 13: Line input specifications measured from line inputs to line outputs.

Note 14: C_B is in pF.

TYPICAL POWER DISSIPATION (No Output Load)

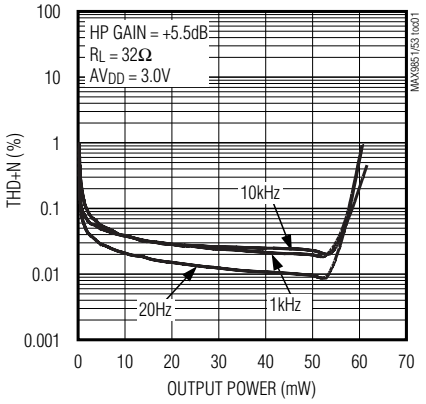
(AV_{DD} = CPV_{DD} = +3V, DV_{DD} = DV_{DDS2} = +1.8V, PV_{DD} = +2.7V.)

MODE	OUTPUT AMPLIFIER	TOTAL POWER (mW)
DAC playback mode operating at 48kHz sampling rate	Stereo headphone	27
	Stereo speaker	55
	Mono receiver	24
Line-only playback mode	Stereo headphone	16
	Stereo speaker	44
	Mono receiver	14
DAC and line input playback mode operating at 48kHz sampling rate	Stereo headphone	27
	Stereo speaker	55
	Mono receiver	25
8kHz voice mode with mono DAC, mono ADC, line inputs and a mono microphone enabled	Stereo headphone	48
	Stereo speaker	76
	Mono receiver	46
8kHz voice mode and 48kHz stereo audio mode with stereo DAC, mono ADC, line inputs and a mono microphone enabled	Stereo headphone	53
	Stereo speaker	81
	Mono receiver	51
ADC record mode with stereo microphone and line inputs enabled	—	46
ADC record and stereo playback with stereo microphone and stereo headphones	—	57

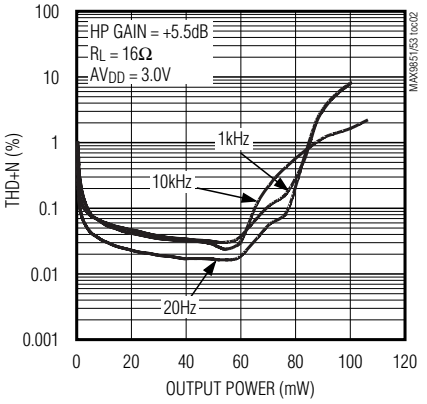
Typical Operating Characteristics

(AV_{DD} = CPV_{DD} = +3V, DV_{DD} = DV_{DDS2} = +1.8V, PV_{DD} = +3.3V, R_{HP} = 32Ω, Z_{SPK} = 8Ω + 10µH, R_{REC} = 32Ω, R_{OUTL+} to R_{OUTL-} = R_{OUTR+} to R_{OUTR-} = 10kΩ, C1 = 0.22µF, C2 = C_{VMREG} = C_{VPREG} = C_{MBIAS} = C_{REF} = 1µF, MCLK = 13MHz, all PGAs = 0dB, HP/REC volume = -20.0dB, SPK volume = -20.4dB, line output gain = -0.4dB, f_S = 48kHz for nonvoice mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

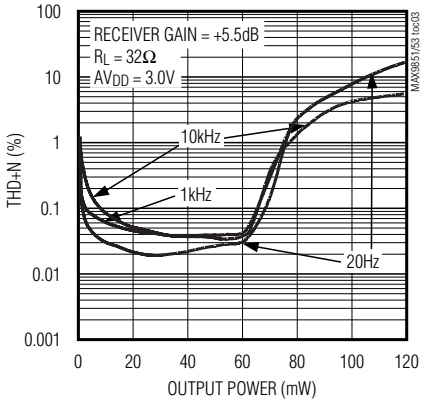
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HP)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HP)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO RECEIVER)

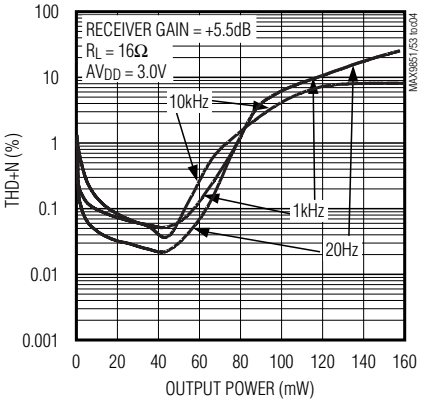


Stereo Audio CODECs with Microphone, DirectDrive Headphones, Speaker Amplifiers, or Line Outputs

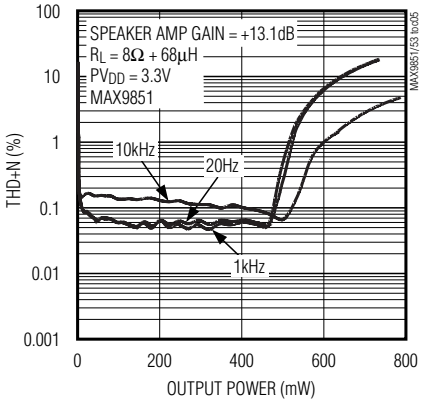
Typical Operating Characteristics (continued)

(AV_{DD} = CPV_{DD} = +3V, DV_{DD} = DV_{DDS2} = +1.8V, PV_{DD} = +3.3V, R_{HP} = 32Ω, Z_{SPK} = 8Ω + 10µH, R_{REC} = 32Ω, R_{OUTL+} to R_{OUTL-} = R_{OUTR+} to R_{OUTR-} = 10kΩ, C1 = 0.22µF, C2 = C_{VMREG} = C_{VPREG} = C_{MBIAS} = C_{REF} = 1µF, MCLK = 13MHz, all PGAs = 0dB, HP/REC volume = -20.0dB, SPK volume = -20.4dB, line output gain = -0.4dB, f_S = 48kHz for nonvoice mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

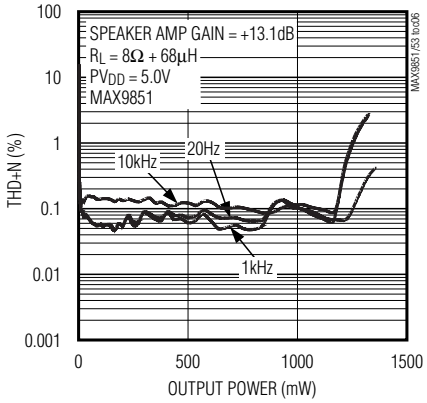
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO RECEIVER)



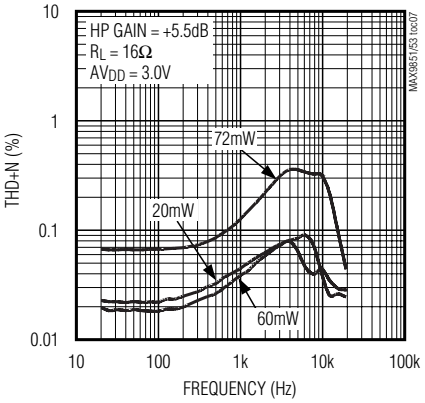
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER AMP)



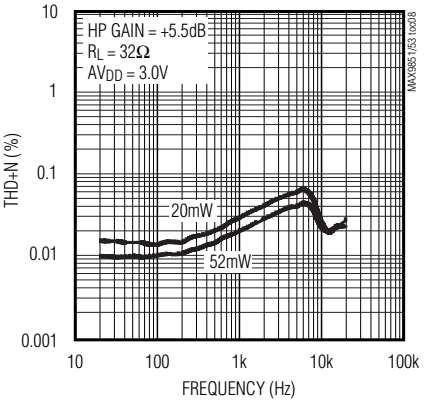
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER AMP)



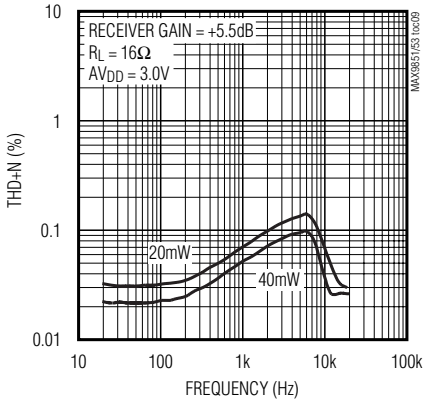
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HP)



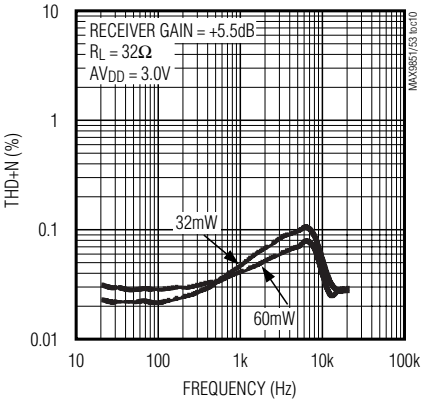
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HP)



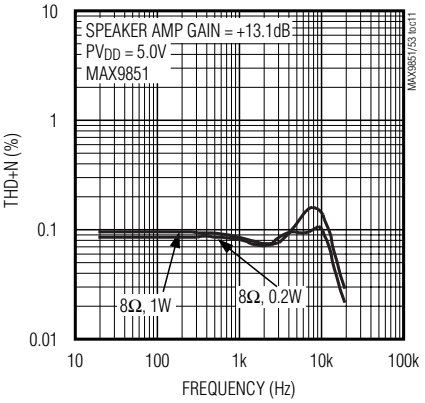
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO RECEIVER)



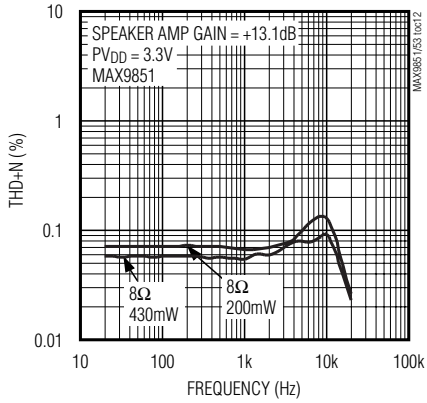
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO RECEIVER)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER AMP)



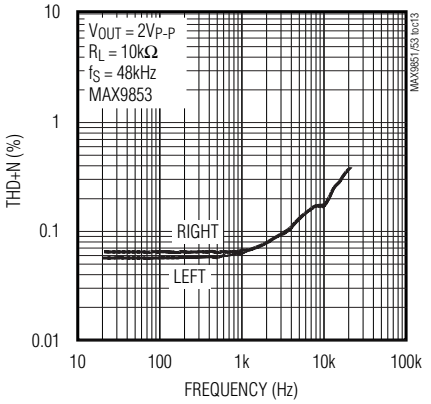
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER AMP)



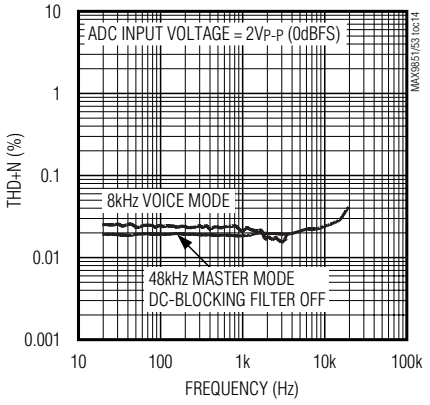
Typical Operating Characteristics (continued)

(AV_{DD} = CPV_{DD} = +3V, DV_{DD} = DV_{DDS2} = +1.8V, PV_{DD} = +3.3V, R_{HP} = 32Ω, Z_{SPK} = 8Ω + 10µH, R_{REC} = 32Ω, R_{OUTL+} to R_{OUTL-} = R_{OUTR+} to R_{OUTR-} = 10kΩ, C1 = 0.22µF, C2 = C_{VMREG} = C_{VPREG} = C_{MBIAS} = C_{REF} = 1µF, MCLK = 13MHz, all PGAs = 0dB, HP/REC volume = -20.0dB, SPK volume = -20.4dB, line output gain = -0.4dB, f_S = 48kHz for nonvoice mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

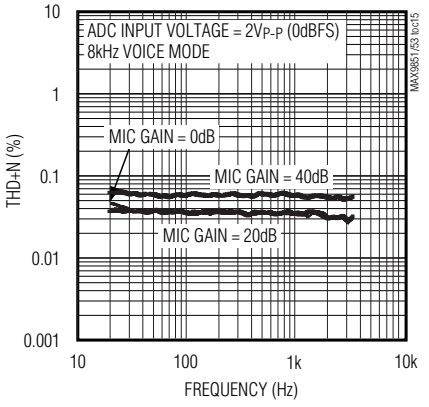
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO LINE OUT)



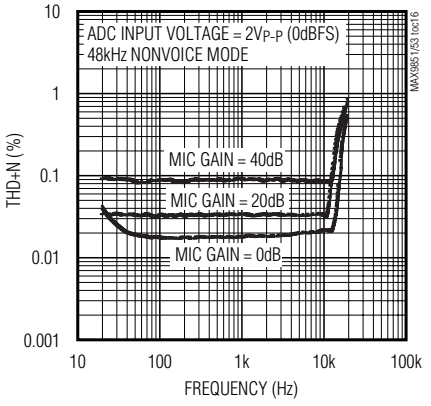
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE IN TO ADC)



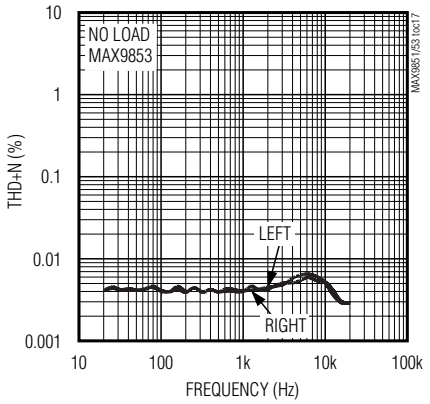
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (INTERNAL MIC TO ADC)



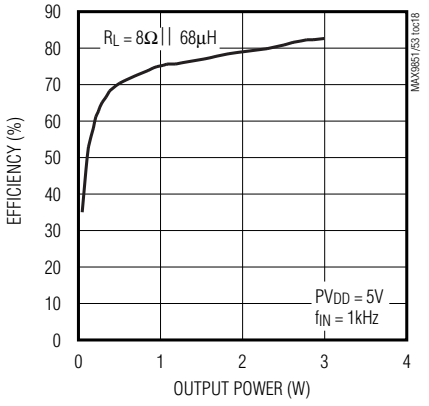
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (INTERNAL MIC TO ADC)



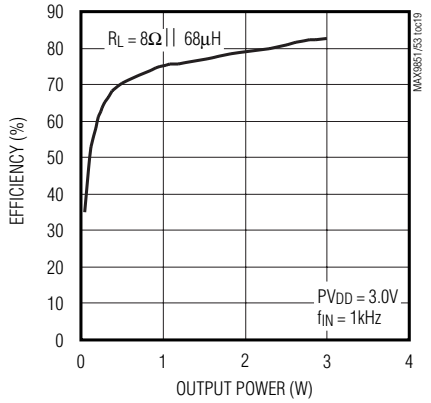
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE IN TO LINE OUT)



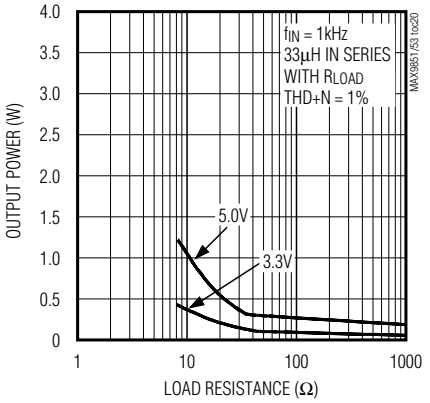
SPEAKER AMP EFFICIENCY vs. OUTPUT POWER



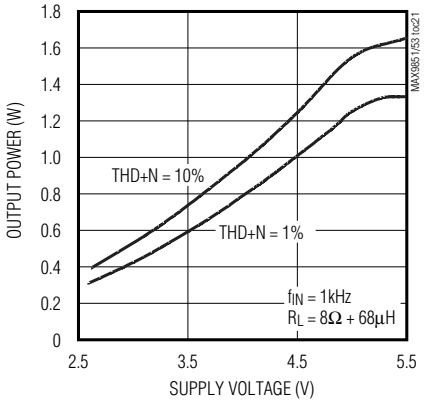
SPEAKER AMP EFFICIENCY vs. OUTPUT POWER



SPEAKER AMP OUTPUT POWER vs. LOAD RESISTANCE



SPEAKER AMP OUTPUT POWER vs. SUPPLY VOLTAGE (PV_{DD})

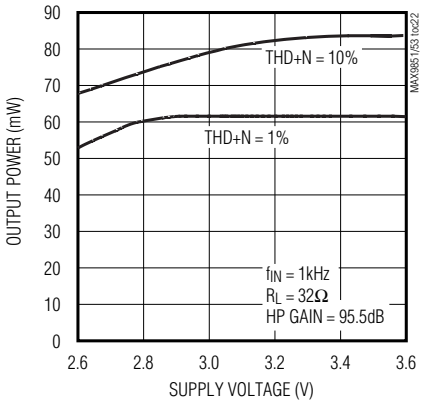


Stereo Audio CODECs with Microphone, DirectDrive Headphones, Speaker Amplifiers, or Line Outputs

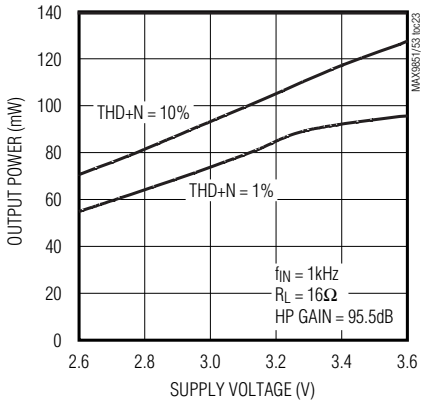
Typical Operating Characteristics (continued)

(AV_{DD} = CPV_{DD} = +3V, DV_{DD} = DV_{DDS2} = +1.8V, PV_{DD} = +3.3V, R_{HP} = 32Ω, Z_{SPK} = 8Ω + 10µH, R_{REC} = 32Ω, R_{OUTL+} to R_{OUTL-} = R_{OUTR+} to R_{OUTR-} = 10kΩ, C1 = 0.22µF, C2 = C_{VMREG} = C_{VPREG} = C_{MBIAS} = C_{REF} = 1µF, MCLK = 13MHz, all PGAs = 0dB, HP/REC volume = -20.0dB, SPK volume = -20.4dB, line output gain = -0.4dB, f_S = 48kHz for nonvoice mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

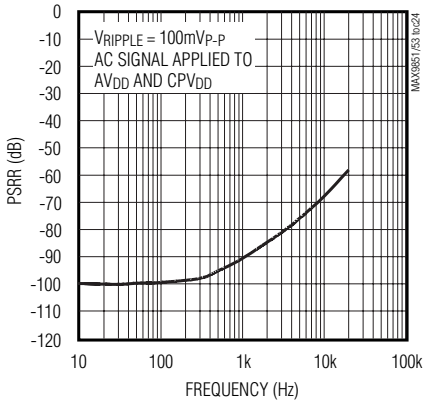
HEADPHONE AMP OUTPUT POWER vs. SUPPLY VOLTAGE (AV_{DD})



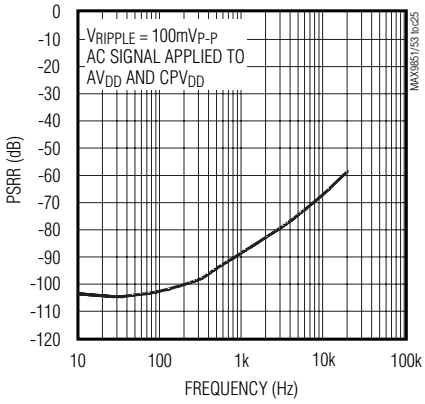
HEADPHONE AMP OUTPUT POWER vs. SUPPLY VOLTAGE (AV_{DD})



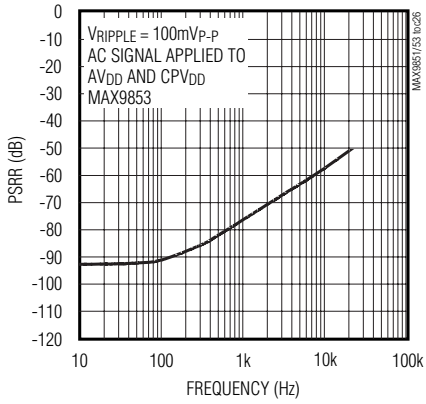
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO HP)



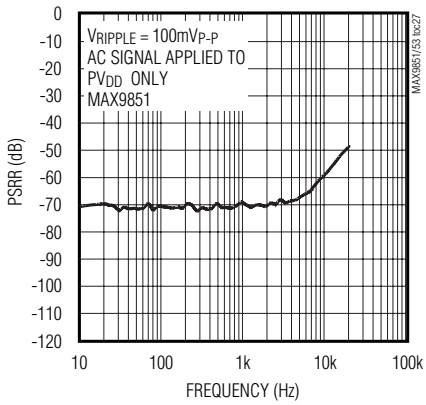
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO RECEIVER)



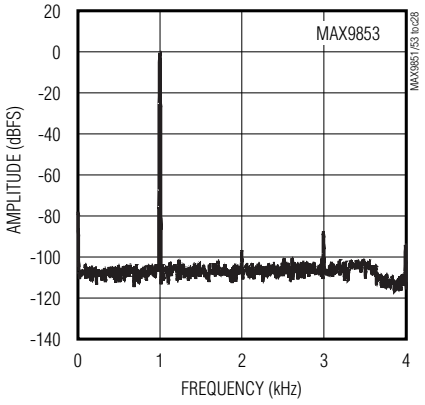
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO LINE OUT)



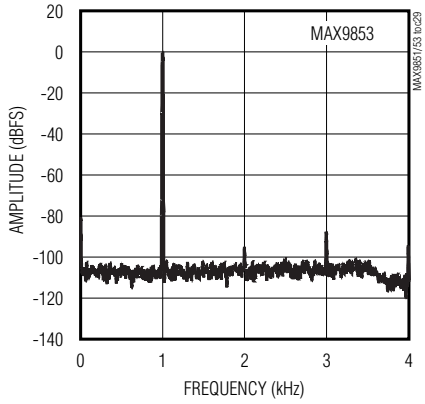
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO SPEAKER)



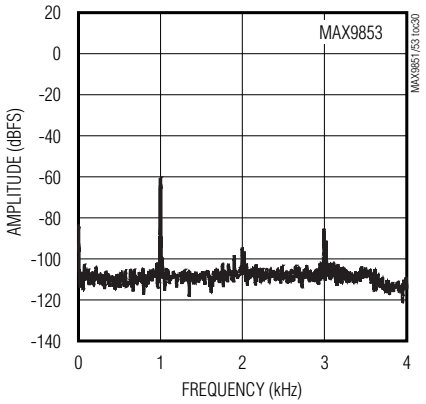
FFT, DAC TO LINE OUT 8kHz SLAVE VOICE MODE, 0dBFS



FFT, DAC TO LINE OUT 8kHz MASTER VOICE MODE, 0dBFS



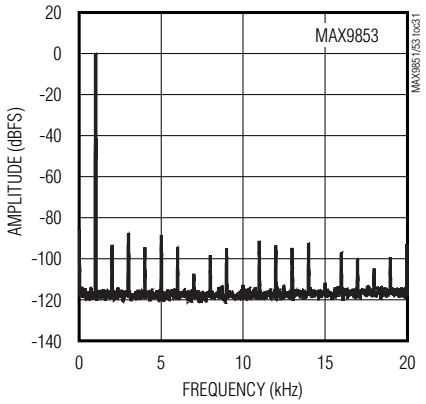
FFT, DAC TO LINE OUT 8kHz MASTER VOICE MODE, -60dBFS



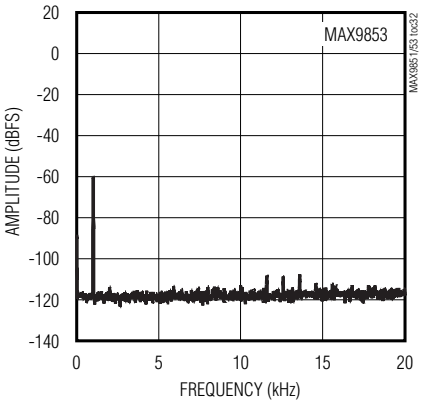
Typical Operating Characteristics (continued)

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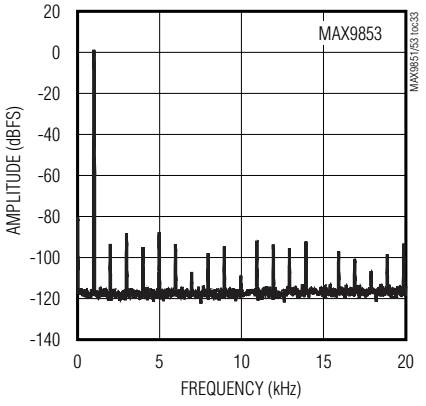
FFT, DAC TO LINE OUT
48kHz SLAVE MODE, 0dBFS



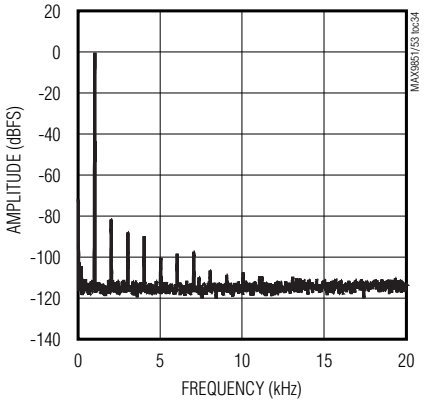
FFT, DAC TO LINE OUT
48kHz SLAVE MODE, -60dBFS



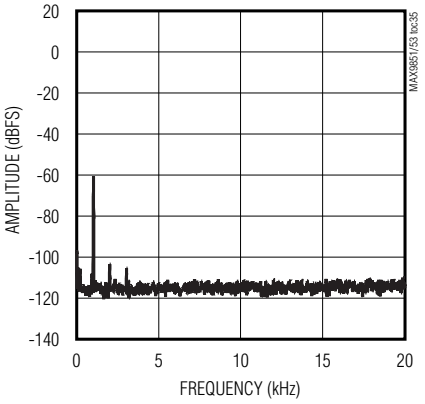
FFT, DAC TO LINE OUT
48kHz MASTER MODE, 0dBFS



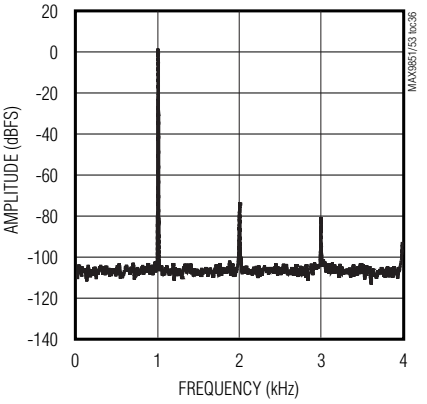
FFT, LINE IN TO ADC
48kHz MASTER MODE, 0dBFS



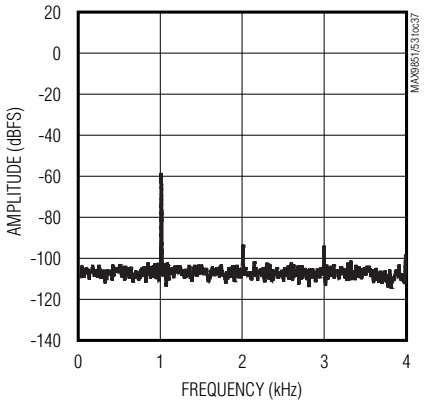
FFT, LINE IN TO ADC
48kHz MASTER MODE, -60dBFS



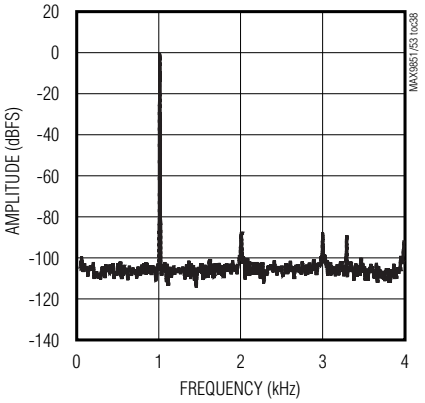
FFT, LINE IN TO ADC
8kHz MASTER VOICE MODE, 0dBFS



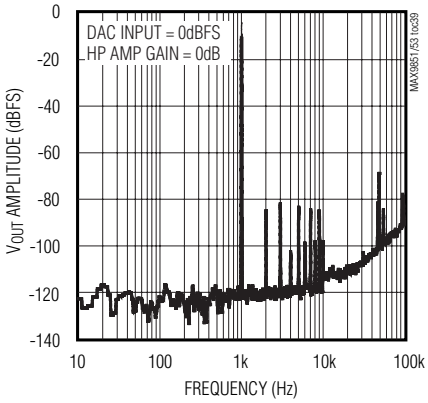
FFT, LINE IN TO ADC
8kHz MASTER VOICE MODE, -60dBFS



FFT, LINE IN TO ADC
8kHz SLAVE VOICE MODE, -60dBFS



WIDEBAND FFT
(DAC TO HP AMP)

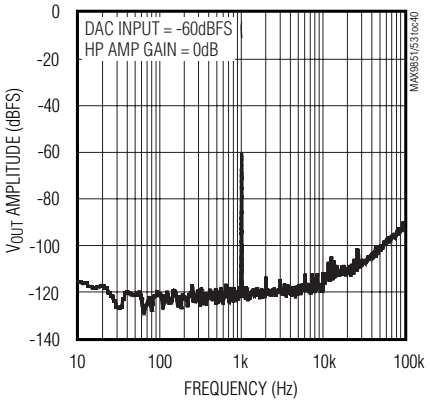


Stereo Audio CODECs with Microphone, DirectDrive Headphones, Speaker Amplifiers, or Line Outputs

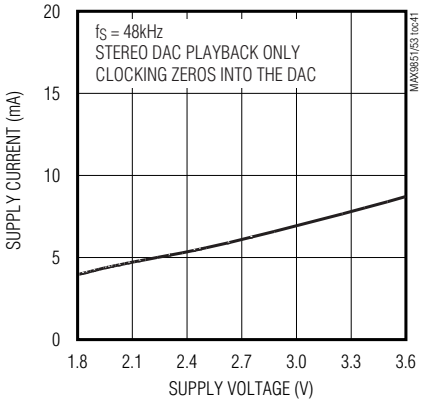
Typical Operating Characteristics (continued)

(AV_{DD} = CPV_{DD} = +3V, DV_{DD} = DV_{DDS2} = +1.8V, PV_{DD} = +3.3V, R_{HP} = 32Ω, Z_{SPK} = 8Ω + 10µH, R_{REC} = 32Ω, R_{OUTL+} to R_{OUTL-} = R_{OUTR+} to R_{OUTR-} = 10kΩ, C1 = 0.22µF, C2 = C_{VMREG} = C_{VPREG} = C_{MBIAS} = C_{REF} = 1µF, MCLK = 13MHz, all PGAs = 0dB, HP/REC volume = -20.0dB, SPK volume = -20.4dB, line output gain = -0.4dB, f_S = 48kHz for nonvoice mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

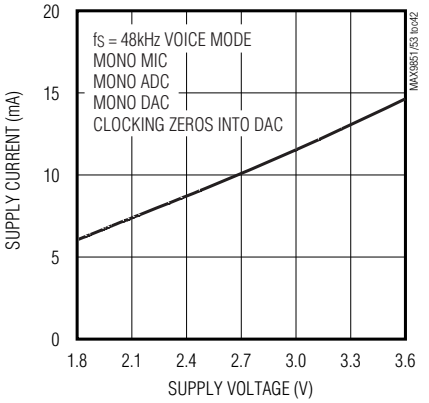
WIDEBAND FFT (DAC TO HP AMP)



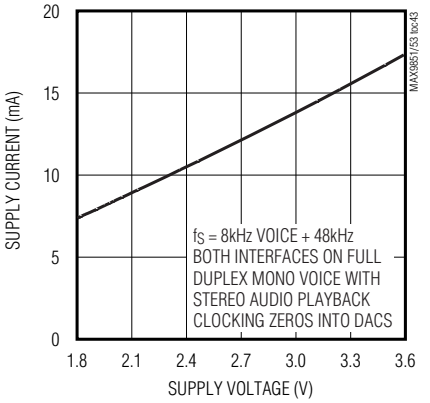
DV_{DD} AND DV_{DDS2} SUPPLY CURRENT vs. SUPPLY VOLTAGE



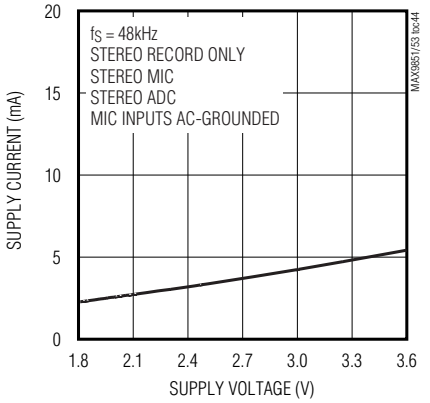
DV_{DD} AND DV_{DDS2} SUPPLY CURRENT vs. SUPPLY VOLTAGE



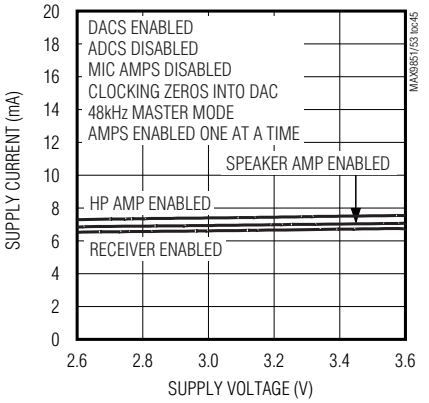
DV_{DD} AND DV_{DDS2} SUPPLY CURRENT vs. SUPPLY VOLTAGE



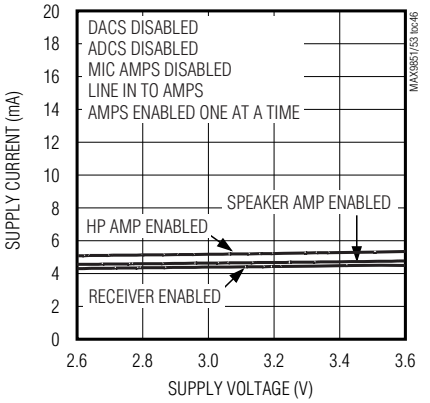
DV_{DD} AND DV_{DDS2} SUPPLY CURRENT vs. SUPPLY VOLTAGE



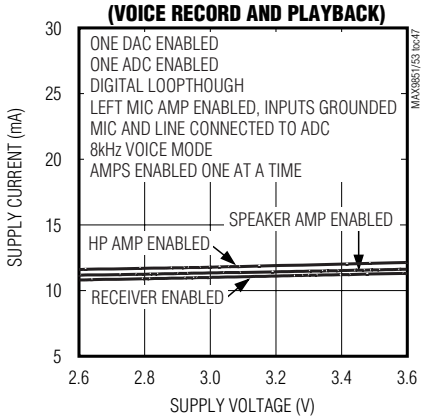
AV_{DD} SUPPLY CURRENT vs. SUPPLY VOLTAGE (STEREO PLAYBACK)



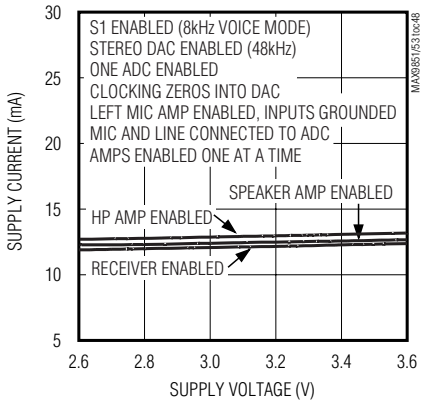
AV_{DD} SUPPLY CURRENT vs. SUPPLY VOLTAGE (ANALOG PATH)



AV_{DD} SUPPLY CURRENT vs. SUPPLY VOLTAGE (VOICE RECORD AND PLAYBACK)



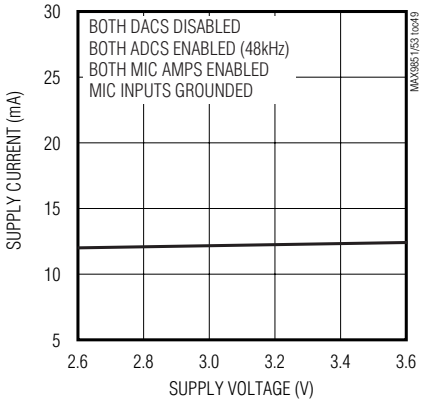
AV_{DD} SUPPLY CURRENT vs. SUPPLY VOLTAGE (DUAL DIGITAL PATH)



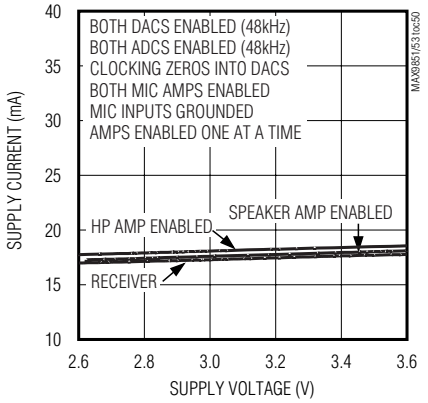
Typical Operating Characteristics (continued)

(AV_{DD} = CPV_{DD} = +3V, DV_{DD} = DV_{DDS2} = +1.8V, PV_{DD} = +3.3V, R_{HP} = 32Ω, Z_{SPK} = 8Ω + 10µH, R_{REC} = 32Ω, R_{OUTL+} to R_{OUTL-} = R_{OUTR+} to R_{OUTR-} = 10kΩ, C1 = 0.22µF, C2 = C_{VMREG} = C_{VPREG} = C_{MBIAS} = C_{REF} = 1µF, MCLK = 13MHz, all PGAs = 0dB, HP/REC volume = -20.0dB, SPK volume = -20.4dB, line output gain = -0.4dB, f_S = 48kHz for nonvoice mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

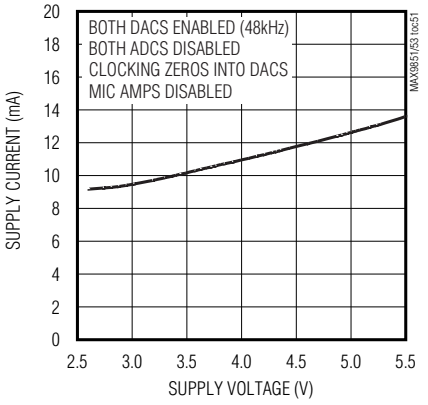
AV_{DD} SUPPLY CURRENT vs. SUPPLY VOLTAGE (STEREO RECORD)



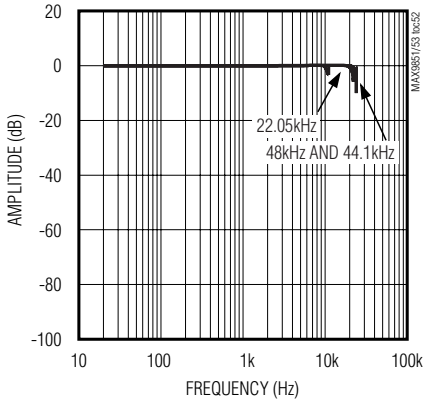
AV_{DD} SUPPLY CURRENT vs. SUPPLY VOLTAGE (STEREO RECORD AND PLAYBACK)



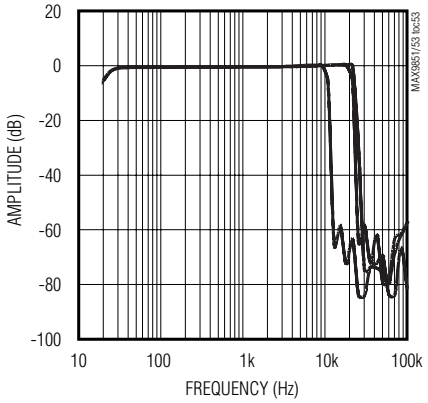
PV_{DD} SUPPLY CURRENT vs. SUPPLY VOLTAGE (DAC TO SPEAKER AMP)



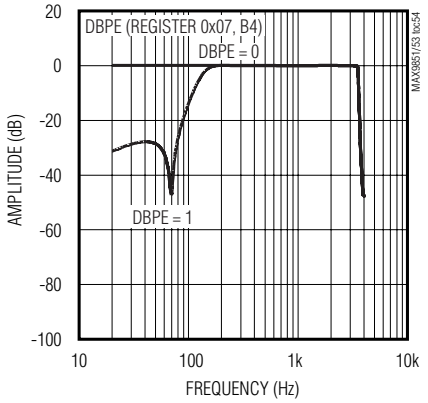
DAC FREQUENCY RESPONSE 48kHz, 44.1kHz, AND 22.05kHz



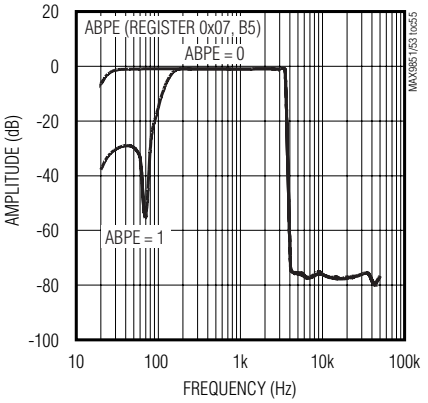
ADC FREQUENCY RESPONSE 48kHz, 44.1kHz, AND 22.05kHz



DAC FREQUENCY RESPONSE 8kHz VOICE MODE



ADC FREQUENCY RESPONSE 8kHz VOICE MODE



Pin Description

PIN		NAME	FUNCTION
MAX9851	MAX9853		
1	1	EXTMICBIASL	Left External Microphone Bias. Provides a 2.4V microphone bias for the external microphone's left channel through selectable 2.2kΩ or 470Ω output impedance resistor.
2	2	PREG	Internal Positive Regulator Output. Bypass to AGND with a 1µF capacitor.
3	—	PV_{DD}	Left Speaker Positive Power-Supply Input. Bypass to PGND with a 0.1µF capacitor.
4	—	LSPK+	Positive Left-Channel Class D Speaker Output
5	—	LSPK-	Negative Left-Channel Class D Speaker Output
6	—	PGND	Class D Speaker Amplifier Ground
7	—	RSPK-	Negative Right-Channel Class D Speaker Output
8	—	RSPK+	Positive Right-Channel Class D Speaker Output
9	—	PV_{DD}	Right Speaker Positive Power-Supply Input. Bypass to PGND with a 0.1µF capacitor.
—	3	OUTL+	Noninverted Differential Left-Channel Line-Level Output. OUTL+ is biased at 1.23V.
—	4	OUTL-	Inverted Differential Left-Channel Line-Level Output. OUTL- is biased at 1.23V.
—	5	SHDNOUT	Shutdown Output. Open-drain shutdown output used to control an external amplifier shutdown input through the MAX9851/MAX9853 I^2C interface. Connect a 10kΩ pullup resistor to DV_{DD} for full output swing.
—	6	FAULTIN	Fault Input. Logic input with internal 300kΩ pullup resistor. The state of FAULTIN is reported in status register 0x00 and can be used to trigger a hardware interrupt.
—	7	PV_{DD}	Headset Autodetect Positive Power-Supply Input. Connect to PV_{DD} battery voltage for proper headset detect operation during sleep mode (see the *Headset Detect* section). Connect to AV_{DD} if not used. Bypass to AGND with a 0.1µF capacitor.
—	8	OUTR-	Inverted Differential Right-Channel Line-Level Output. OUTR- is biased at 1.23V.
	9	OUTR+	Noninverted Differential Right-Channel Line-Level Output. OUTR+ is biased at 1.23V.
10	10	NREG	Internal Negative Regulator Output. Bypass to AGND with a 1µF capacitor.
11	11	REF	Reference Output. Bypass to AGND with a 1µF ceramic capacitor.
12	12	MBIAS	Internal Microphone Bias Regulator Output. Bypass to AGND with a 1µF capacitor.
13	13	LINEIN1	Line Input 1. AC-couple analog audio signal to LINEIN1.
14	14	LINEIN2	Line Input 2. AC-couple analog audio signal to LINEIN2.
15	15	AV_{DD}	Audio Power-Supply Input. Bypass to AGND with 0.1µF and 10µF capacitors.
16	16	HPL	Left-Channel Headphone Output (Stereo Mode)/Noninverting Headphone Output (Balanced Mono Mode). HPL is a DirectDrive output biased at AGND.
17	17	HPR	Right-Channel Headphone Output (Stereo Mode)/Noninverting Headphone Output (Balanced Mono Mode). HPR is a DirectDrive output biased at AGND.
18	18	SV_{SS}	Headphone and Receiver Amplifier Negative Supply Input. Connect to PV_{SS}.
19	19	REC	Handset Receiver Output. REC is a DirectDrive output biased at AGND.
20	20	PV_{SS}	Inverting Charge-Pump Output. Bypass to CPGND with a 1µF ceramic capacitor and connect to SV_{SS} to provide the headphone and receiver amplifiers with a negative supply.

Pin Description (continued)

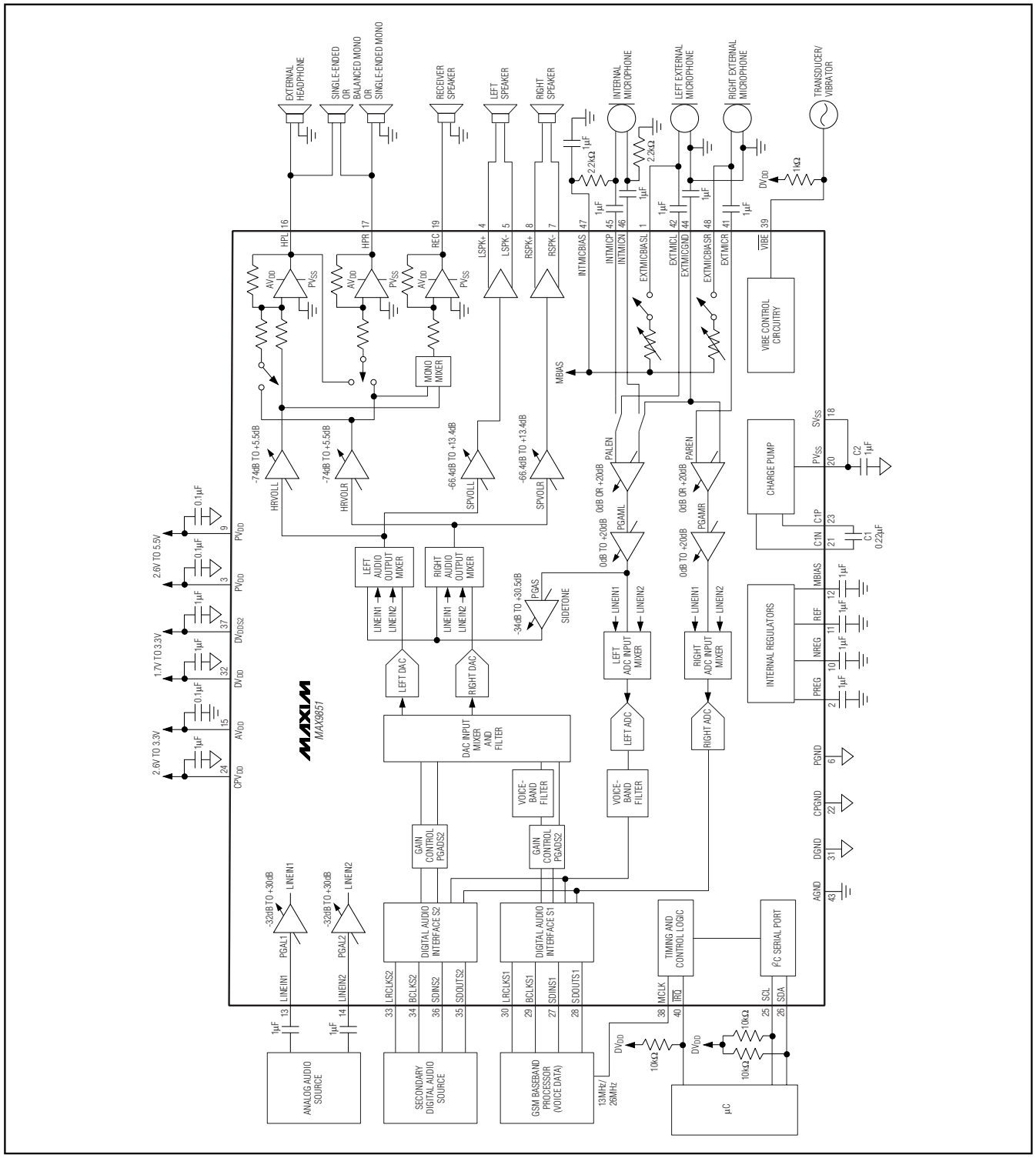
PIN		NAME	FUNCTION
MAX9851	MAX9853		
21	21	C1N	Charge-Pump Flying Capacitor Negative Terminal. Connect a 0.22µF ceramic capacitor between C1N and C1P.
22	22	CPGND	Charge-Pump Ground
23	23	C1P	Charge-Pump Flying Capacitor Positive Terminal. Connect a 0.22µF ceramic capacitor between C1N and C1P.
24	24	CPV_{DD}	Charge-Pump Positive Power-Supply Input. Bypass to CPGND with a 1µF capacitor.
25	25	SCL	I^2C-Compatible Serial Clock Input. Connect a 10kΩ pullup resistor to DV_{DD} for full output swing.
26	26	SDA	I^2C-Compatible Serial Data Input/Output. Connect a 10kΩ pullup resistor to DV_{DD} for full output swing.
27	27	SDINS1	Primary Interface Digital Audio Serial Data DAC Input. Voiceband filtering available on this input.
28	28	SDOUTS1	Primary Interface Digital Audio Serial Data ADC Output. Voiceband filtering available on this output.
29	29	BCLKS1	Primary Interface Digital Audio Bit Clock Input/Output. BCLKS1 is an input when the MAX9851/MAX9853 is in slave mode and an output when in master mode.
30	30	LRCLKS1	Primary Interface Digital Audio Left-Right Clock Input/Output. LRCLKS1 is the audio sample rate clock and determines whether the audio data on SDINS1 is routed to the left or right channel. LRCLKS1 is an input when the MAX9851/MAX9853 is in slave mode and an output when in master mode.
31	31	DGND	Digital Ground
32	32	DV_{DD}	Digital Power-Supply Input. DV_{DD} provides power to the digital core, the I^2C interface and the primary digital audio interface. Bypass to DGND with a 1µF capacitor.
33	33	LRCLKS2	Secondary Interface Digital Audio Left-Right Clock Input/Output. LRCLKS2 is the audio sample rate clock and determines whether the audio data on SDINS2 is routed to the left or right channel. LRCLKS2 is an input when the MAX9851/MAX9853 is in slave mode and an output when in master mode.
34	34	BCLKS2	Secondary Interface Digital Audio Bit Clock Input/Output. BCLKS2 is an input when the MAX9851/MAX9853 is in slave mode and an output when in master mode.
35	35	SDOUTS2	Secondary Interface Digital Audio Serial Data ADC Output
36	36	SDINS2	Secondary Interface Digital Audio Serial Data DAC Input

Stereo Audio CODECs with Microphone, DirectDrive Headphones, Speaker Amplifiers, or Line Outputs

Pin Description (continued)

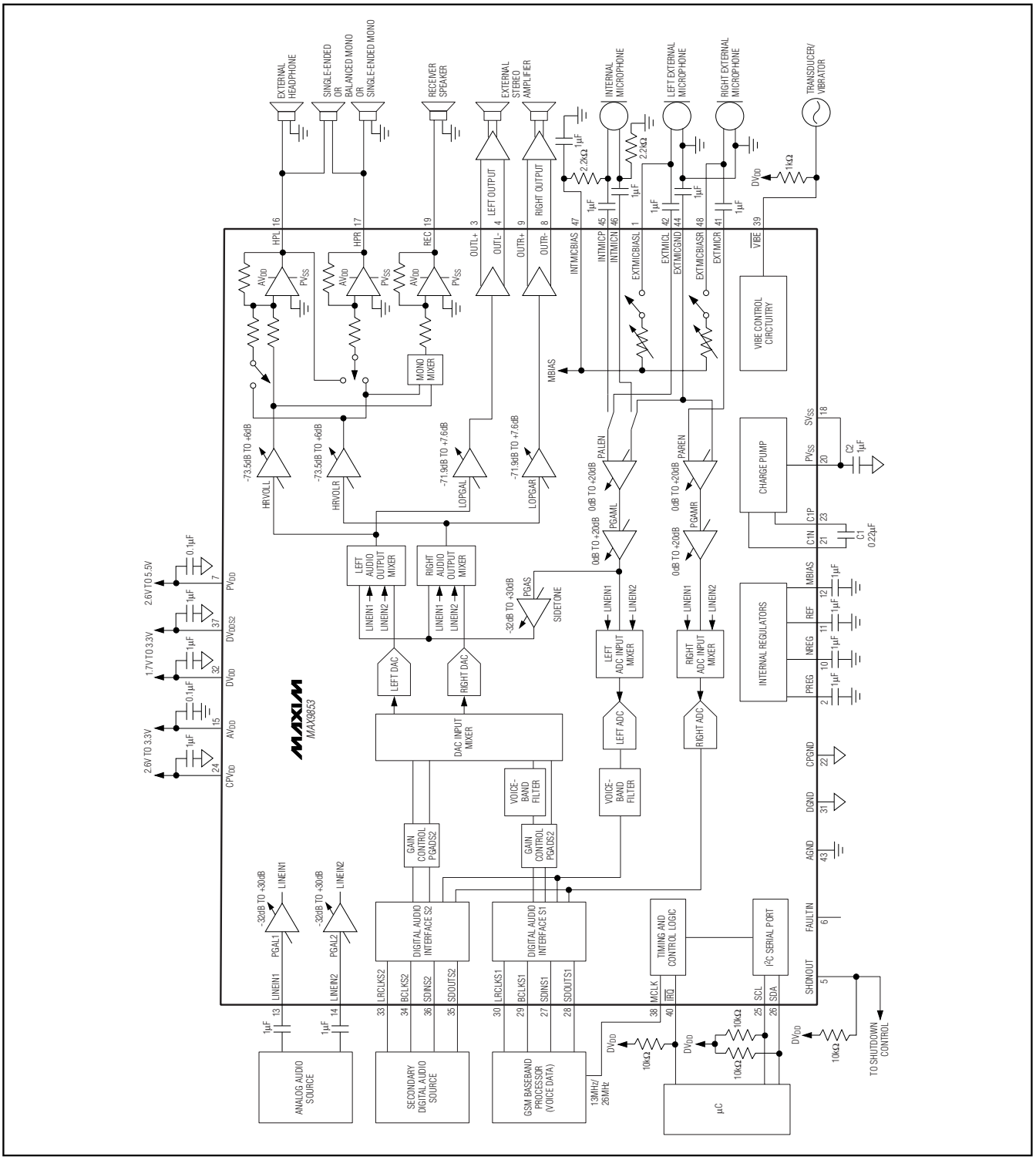
PIN		NAME	FUNCTION
MAX9851	MAX9853		
37	37	DV_{DDS2}	Secondary Digital Audio Interface Power-Supply Input. Bypass to DGND with a 1µF capacitor.
38	38	MCLK	13MHz/26MHz Master Clock Input
39	39	$\overline{VIBE}$	Transducer/Vibrator Output. Open-drain output programmable to control a vibrator motor or a transducer. Connect a 1kΩ pullup resistor to DV_{DD} for full output swing.
40	40	$\overline{IRQ}$	Hardware Interrupt Output. $\overline{IRQ}$ can be programmed to pull low when bits in the status register 0x00 change state. Read status register 0x00 to clear $\overline{IRQ}$ once set. Repeat faults will have no effect on $\overline{IRQ}$ until it is cleared by reading the I^2C status register 0x00. Connect a 10kΩ pullup resistor to DV_{DD} for full output swing.
41	41	EXTMICR	External Microphone Right-Channel Single-Ended Input. Connect a compatible high-impedance or low-impedance (with built-in pre-amplifiers) microphone between EXTMICR and EXTMICGND. AC-couple a microphone to EXTMICR with a series 1µF capacitor.
42	42	EXTMICL	External Microphone Left-Channel Single-Ended Input. Connect a compatible high-impedance or low-impedance (with built-in pre-amplifiers) microphone between EXTMICL and EXTMICGND. AC-couple a microphone to EXTMICL with a series 1µF capacitor.
43	43	AGND	Analog Ground
44	44	EXTMICGND	External Microphone Ground Sense Return. AC-couple EXTMICGND to the external jack ground with a series 1µF capacitor to reduce noise.
45	45	INTMICP	Internal Positive Differential Microphone Input. AC-couple a microphone to INTMICP with a series 1µF capacitor.
46	46	INTMICN	Internal Negative Differential Microphone Input. AC-couple a microphone to INTMICN with a series 1µF capacitor.
47	47	INTMICBIAS	Internal Microphone Bias. Bypass INTMICBIAS to AGND with a 1µF capacitor. Provides 2.4V microphone bias for the internal differential microphone through an external 2.2kΩ resistor.
48	48	EXTMICBIASR	Right External Microphone Bias. Provides a 2.4V microphone bias for a right-channel external microphone through an internal selectable 2.2kΩ or 470Ω output resistor.
—	—	EP	Exposed Thermal Pad. Connect to AGND.

MAX9851 Functional Diagram/Typical Operating Circuit



Stereo Audio CODECs with Microphone, DirectDrive Headphones, Speaker Amplifiers, or Line Outputs

MAX9853 Functional Diagram/Typical Operating Circuit



Detailed Description

The MAX9851 CODEC, with a stereo DirectDrive headphone amplifier and a stereo Class D speaker amplifier, is a complete digital audio solution for GSM/GPRS/EDGE cell phones and PDA phones. The MAX9853 audio CODEC shares all the functionality of the MAX9851 without the Class D speaker amplifier, substituting it with stereo differential line outputs to facilitate external amplifiers and other analog audio devices. The MAX9851/MAX9853 additionally feature stereo and mono microphone inputs, and a mono DirectDrive handset receiver amplifier combined with sigma-delta stereo DACs and stereo ADCs.

The sigma-delta DAC has 88dB of dynamic range and accepts stereo audio data from two independent digital audio interfaces at sampling frequencies ranging from 8kHz to 48kHz. The interfaces can accept I²S-compatible data in addition to voiceband data and allows the mixing of multiple audio sources at different unrelated sample rates. The primary digital audio input integrates bandpass filtering that can be used when operating in voice mode. Digital audio from the ADC can output on both interfaces allowing maximum flexibility.

Analog and digital volume levels, muting, and device configuration are programmed through the I²C-compatible interface. Audio data is sent to and from the MAX9851/MAX9853 through either of two 4-wire digital audio data buses that support numerous formats. LRCLK and BCLK signals are generated by the MAX9851/MAX9853 when configured in master mode. The MAX9851/MAX9853 can also be configured as a slave DAC stereo audio playback device or a full duplex slave voice CODEC, accepting LRCLK and BCLK signals from an external digital audio master.

Maxim's DirectDrive architecture employs an internal charge pump to create a negative voltage supply powering the headphone and receiver amplifier outputs. The internal negative supply allows the analog output signals to be biased at ground, eliminating the need for an output-coupling capacitor, reducing system cost and size. The MAX9851/MAX9853's stereo line inputs allow mixing of analog audio with digital audio. Numerous signal routing options and programmable gain allow any combination of analog and digital input signals at varying signal levels to be routed to any output. Sophisticated headset sensing circuitry allows the MAX9851/MAX9853 to detect a wide variety of headset configurations and trigger a hardware interrupt on jack insertion (even when powered down). The external stereo microphone inputs provide configurable internal bias resistors and a gain range of 40dB to accommodate a wide variety of microphones. The internal mono microphone input provides a differential input and a gain range of 40dB. The $\overline{VIBE}$ digital output can be used to control a vibrator, transducer, or can be used as a general-purpose digital output.

Serial Digital Audio Interface

The MAX9851/MAX9853 have two independent digital audio interfaces, S1 and S2, each capable of operating independently in the full-duplex master and slave timing modes shown in Figures 1 and 2. The second digital audio interface operates from a secondary supply voltage (DV_{DDS2}) to allow simple integration into multiple supply systems.

Set S1SDO or S2SDO to 1 (register 0x03 or 0x05, bit B7) to enable the output of ADC data to the corresponding SDOUT pin. Enabling both SDOUTS1 and SDOUTS2 will output the same digital audio signal on both interfaces and the primary S1 interface will specify the sample rate of the ADC.

Set S1SDI or S2SDI to 1 (register 0x03 or 0x05, bit B6) to enable DAC input and begin an internal soft-start sequence for the corresponding SDIN pin. Clearing a particular SDI bit begins an internal soft-stop sequence prior to disabling the input. The SLD slew detect status bit (register 0x00, bit B6) indicates when a soft-start/stop sequence has completed. This allows interface mode changes without interrupting the other interface's signal flow. Clear both S1SDI and S2SDI before enabling the left and right DAC with DACLEN and DACREN (register 0x1B, bits B7 and B6).

To achieve the most exact sample clocks, operate the MAX9851/MAX9853 in slave mode with the exact LRCLK provided externally (in DAC-only mode) or in master mode with the ADCs disabled. The ADC requires an exact integer LRCLK frequency resulting in less accurate sample clocks than when only operating the DAC. Slave mode is only available for the DACs when the ADCs are inactive, or for fully synchronous 8kHz and 16kHz voice modes.

Table 1 lists the MAX9851/MAX9853 available interface modes for each sampling frequency.

Stereo Audio CODECs with Microphone, DirectDrive Headphones, Speaker Amplifiers, or Line Outputs

Table 1. Digital Audio Interface Modes

MODE		f_S (ADC ON) (kHz)	f_S (ADC OFF) (kHz)
48	Master (stereo audio mode)	47.794	48.0011
44.1	Master (stereo audio mode)	43.333	44.0989
32	Master (stereo audio mode)	31.863	31.9986
24	Master (stereo audio mode)	24.074	23.9990
22.05	Master (stereo audio mode)	21.959	22.0494
16	Master (stereo audio mode)	15.931	15.9993
12	Master (stereo audio mode)	12.037	12.0010
11.025	Master (stereo audio mode)	11.054	11.0247
8	Master (stereo audio mode)	8.025	7.9997
8	Master (voice mode)	8.000	8.000
16	Master (voice mode)	16.000*	16.000*
8 to 48	Slave (stereo audio mode)	—	8 to 48
16	Slave (voice mode)	16.000*	16.000*
8	Slave (voice mode)	8.000	8.000

**26MHz clock required for synchronous 16kHz sample rate.*

Stereo Audio Modes

Set S1MAS or S2MAS to 1 (register 0x04 or 0x06, bit B7) to operate the respective interface in master mode. The MAX9851/MAX9853 generate the LRCLK and BCLK signals, which can be used to send and receive digital audio samples. In stereo audio mode, the BCLK signal is a pulse with a period of 310ns. BCLK is inactive when there are no bits transmitted on SDIN or SDOUT. The number of clock cycles per frame is equal to the configured bit depth. Set S1MAS or S2MAS to 0 to operate the respective interface in slave mode, and disable the ADC in stereo audio modes (slave mode not available). The interface accepts slave mode noninteger sample clocks ranging from 8kHz to 48kHz and the appropriate bit clocks in these DAC-only stereo audio modes. See Figure 4 for the digital audio interface timing diagrams.

Voice Modes

In master voice mode, the S1 digital audio interface operates as shown in Figure 3. The BCLK signal is a continuous 13MHz clock. The LRCLK consists of a single-pulse frame sync signal rather than the left-/right-frame sync clock method used in I²S. Although the 8kHz voice mode can be run from either the 13MHz or 26MHz MCLK frequency, 16kHz voice mode requires a 26MHz MCLK. Although both S1 and S2 interfaces are capable of operating in voice mode, only the primary S1 interface can be configured with a bandpass voice filter.

In slave voice mode, an external device must provide at least 16 BCLK cycles following an LRCLK pulse, which will allow operation using any BCLK rate or operation with BCLK shut off between word transfers.

In voice mode, the first 16 bits of each sample treated as left-channel audio data. The MAX9851/MAX9853 are capable of receiving up to 16 additional bits per sample word, treated as right-channel data. These additional bits are routed to the Vibe circuitry when operating in voice mode on the S1 interface. When operating on the S2 interface, these additional bits are interpreted as right-channel data, optionally routed to the right DAC and the Vibe circuitry.

Additional Features

Included in each digital audio interface is a timing control module allowing the MAX9851/MAX9853 to generate the clock signals for master mode.

The two digital audio interfaces include full functionality for I²S modes of operation, including true I²S data, left-justified data, and either inverted LRCLK or inverted BCLK. Set S1MODE or S2MODE to 0xA or 0xB (register 0x03 or 0x05, bits B3–B0) to configure the interface for 8kHz or 16kHz voice mode, respectively.

Set S1MNO or S2MNO to 1 (register 0x03 or 0x05, bit B5) to mix the right- and left-channel input data to create a mono serial data signal from the left and right input data. The result is then input to the left digital filter path, leaving the right path unused. The output of the left filter path can still be sent to either or both the left

and right DACs (see the *Signal Routing* section). The right- and left-channel input data is summed without attenuation and may overdrive the input filter, causing distortion, when the input signals are large. The sum of the stereo input signal should not exceed the dynamic range of the filter, typically 0dBFS digital full scale.

When operating in a voice mode with the primary S1 interface, the digital signal data is input to the left channel without summing since the incoming data is assumed to be mono. Adjust PGADS1 and PGADS2 (register 0x0C and 0x0D) to program the gain for the primary and secondary digital audio interfaces. Independent gain adjustment for each interface allows level-matching of different digital signal sources or fade adjustment between two signal sources.

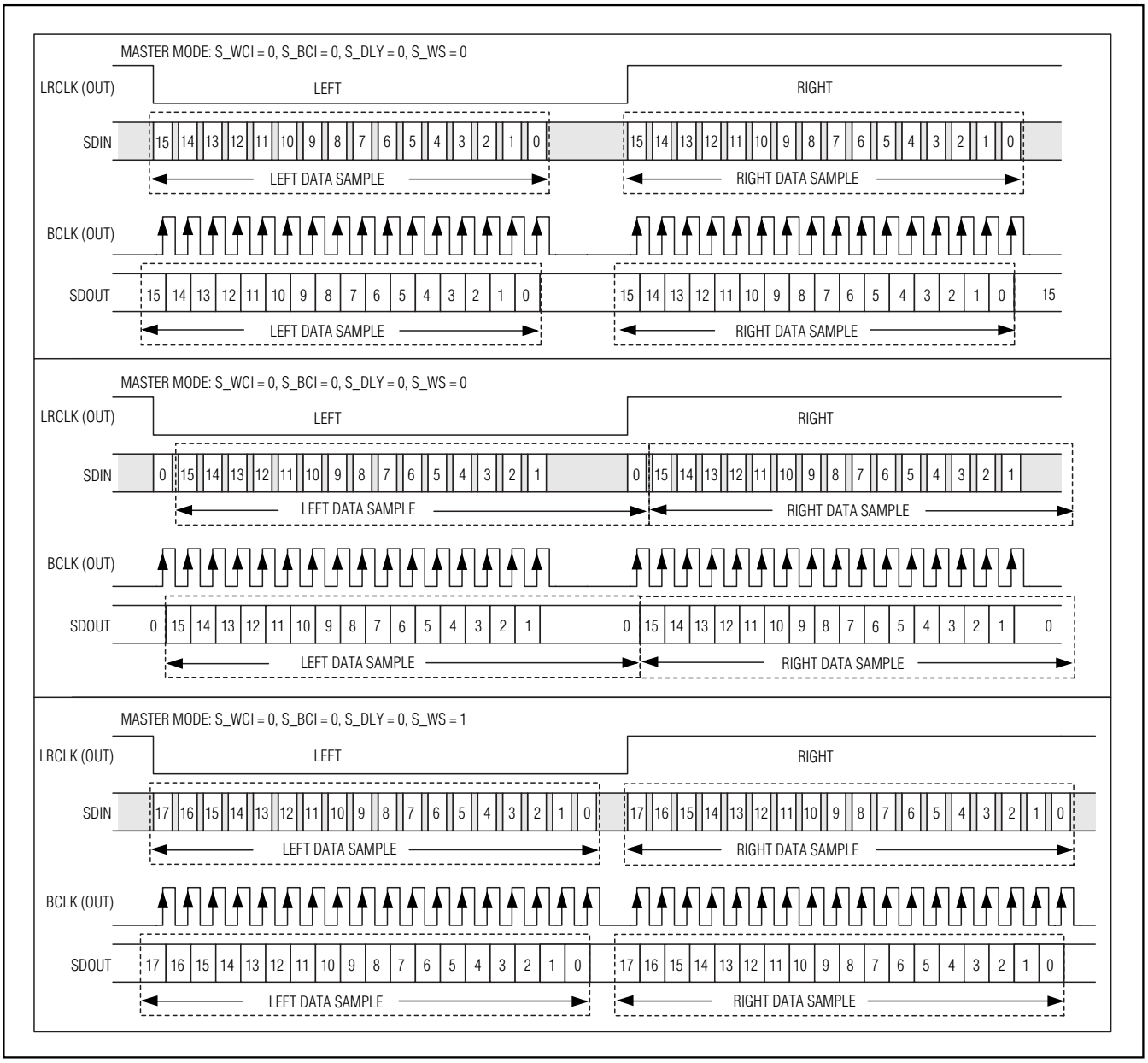


Figure 1. Digital Audio Interface Timing—I²S Master Modes

Stereo Audio CODECs with Microphone, DirectDrive Headphones, Speaker Amplifiers, or Line Outputs

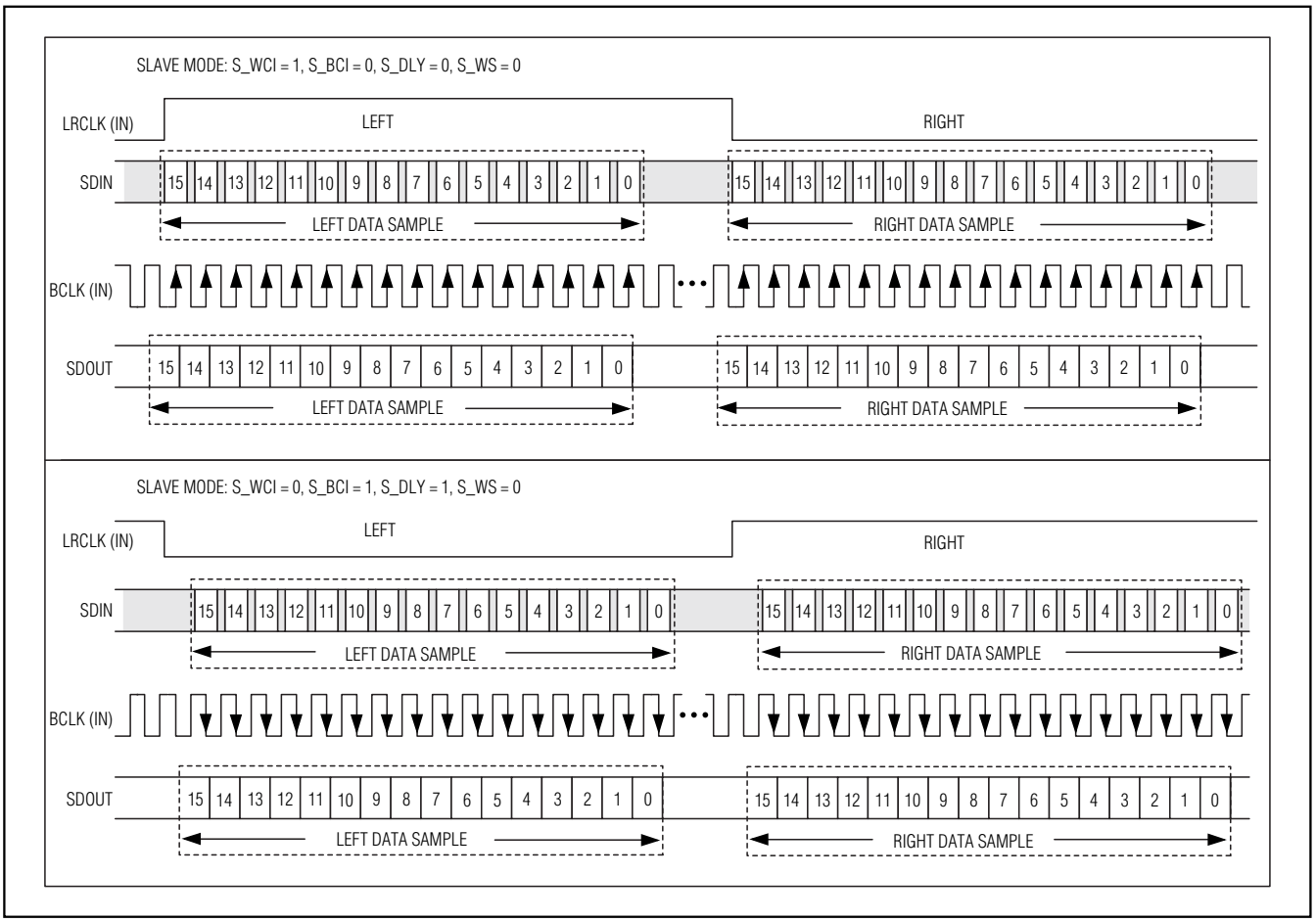


Figure 2. Digital Audio Interface Timing—I²S Slave Modes

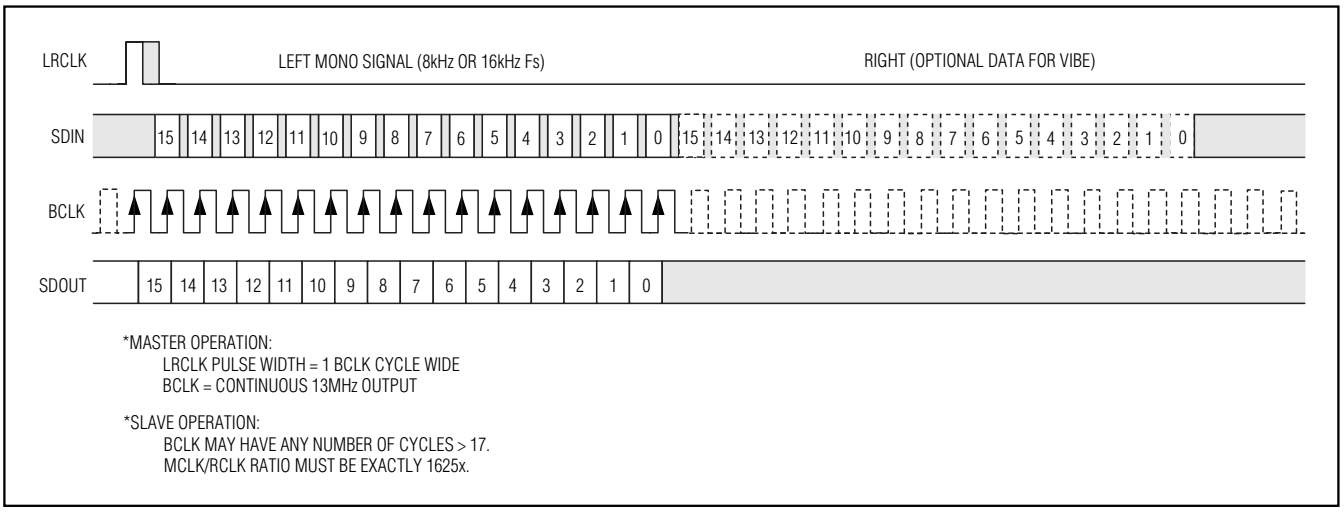


Figure 3. Digital Audio Interface Timing—Voice Modes with Optional Vibe Data

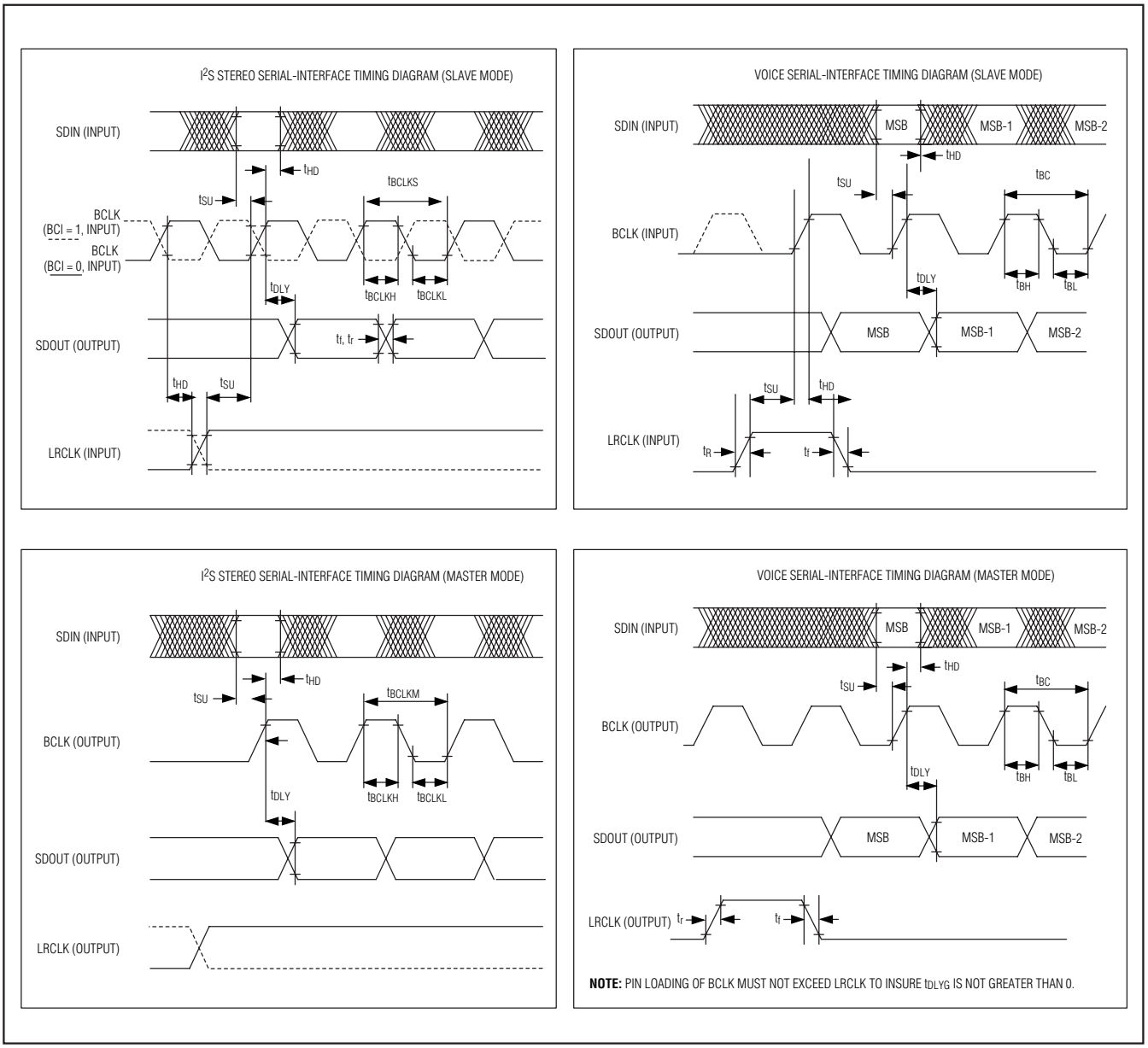


Figure 4. Digital Audio Interface Timing Diagrams

Stereo Audio CODECs with Microphone, DirectDrive Headphones, Speaker Amplifiers, or Line Outputs

Changing Serial Audio Interface Modes

Set S1SD0 = S1SDI = 0 (register 0x03 and 0x05, bit B6) before making any mode changes to serial audio interface S1 to ensure proper operation. Similarly, set S2SD0 = S2SDI = 0 before making any mode changes to serial audio interface S2. This will disable the serial interface and ensure that sampling rate and filtering changes are made properly. Once the desired mode has been selected through I²C, the interface can be re-enabled. **Failure to observe this procedure can result in the MAX9851/MAX9853 being placed in an invalid operational mode, leading to unexpected results.**

Powering On/Off the MAX9851/MAX9853

The MAX9851/MAX9853 power on in low-power shutdown mode with all signal paths disabled. It is good practice to configure all I²C registers except S1SDI and S2SDI (register 0x03 and 0x05, bit B6) before taking the MAX9851/MAX9853 out of shutdown. This may include setting initial volume levels, DAC and ADC modes of operation, stereo or mono operation, and audio interface settings. The analog section of the MAX9851/MAX9853 must be fully operational before the digital circuitry will function. Enable the charge pump by setting CPEN = 1 (register 0x1A, bit B4). Once the MAX9851/MAX9853 have been properly configured, set the global shutdown bit, $\overline{SHDN}$, to 1 (register 0x1A, bit B7). The MAX9851/MAX9853 are fully operational 70ms after $\overline{SHDN}$ is set. Finally, if the DACs are to be used, program S1SDI and S2SDI as desired to enable DAC soft-start.

Disable the audio outputs before powering down the MAX9851/MAX9853 by setting HRMODE and SPMODE (LOMODE) bits (Register 0x18). Ramping the volume to maximum attenuation is recommended before disabling the output amplifiers. Disable the headphone and speaker (or line outputs) once the audio is fully attenuated. The headphone and speaker (or line outputs) can be disabled within 50µs of attenuation without any audible clicks or pops. Place the MAX9851/MAX9853 in shutdown after the outputs are disabled.

Sigma-Delta DAC

Set DACLEN and DACREN to 1 (register 0x1B, bit B7 and B6) to enable the left and right DACs while the S1SDI and S2SDI bits are cleared and the SLD status bit is low to ensure click/pop suppression, then enable S1SDI and S2SDI as desired. The stereo DACs can mix any combination of the four channels of data from the S1 left/right and S2 left/right signal sources using the MIXDAL/R bits (register 0x08). Digital signals from the two interfaces in the 8kHz to 48kHz sample rate range are combined regardless of S1 and S2 interfaces modes, even if asynchronous with respect to each other or MCLK (in DAC-only mode).

When operating in standard stereo audio mode, the input data stream from each interface is passed through separate 8x FIR interpolating filters. When operating in voice mode, the primary interface makes use of an interpolating IIR voiceband filter with an optional highpass component. When operating in mono mode, or when serial input data is disabled for a digital audio interface, the unused digital-signal processing filter paths are disabled to minimize supply-current consumption.

The stereo signals at the left and right DAC may be additionally filtered in any mode with a programmable highpass filter to band limit the audio output and block DC. Set DHPL and DHPR (register 0x07, bits B3–B0) to 01, 10, or 11 to select one of the three highpass filter cutoff frequencies as shown in Table 2.

Table 2. DAC Highpass Filter Modes

DHPL/DHPR BIT SETTINGS	FILTER MODE
00	No filtering
01	55Hz to 91Hz cutoff frequency
10	171Hz to 279Hz cutoff frequency
11	327Hz to 533Hz cutoff frequency

Sigma-Delta ADC

Set ADCLEN and ADCREN to 1 (register 0x1B, bit B5 and B4) to enable the MAX9851/MAX9853's stereo ADCs. The ADCs accept analog signals from the line inputs and the microphone inputs which can be mixed as described in the *Signal Routing* section prior to conversion. For ADC operation, program the enabled digital audio interface(s) to operate in master mode so that the sampling clock is generated within the MAX9851/MAX9853.

The maximum signal that will not clip the ADC input is $2V_{P-P}$. If clipping does occur, reduce the microphone or line input gain as appropriate. Clipping in the digital circuitry is indicated by CLD (register 0x00, bit B7).

Internal Timing

The MAX9851/MAX9853 operate from either a 13MHz or 26MHz master input clock (MCLK). 16kHz voice mode requires a 26MHz clock. The quality of the clock signal has a direct relationship with the dynamic range performance of the data converters. Clock jitter below $100ps_{RMS}$ is necessary to maintain maximum performance figures.

The MAX9851/MAX9853 make extensive use of MCLK for all chip functions. The digital circuitry and Class D amplifiers require a master clock to operate.

Once the MAX9851/MAX9853 are initialized, MCLK is not required during modes where the ADC and DAC are disabled (for instance, playing line inputs through the headphone outputs). **However, MCLK needs to be applied for a short period of time (> 1ms) after power-on to initialize volume control circuitry—this is only once per power-on.**

Voiceband Filters

The MAX9851/MAX9853 provide mono voiceband filtering for both output and input digital audio signals on the primary interface. Set ABPE to 1 (register 0x07, bit B5) to enable the highpass component of the voiceband filtering on the output of the ADC. Similarly, set DBPE to 1 (register 0x07, bit B4) to enable the highpass component of the voiceband filtering for incoming data on the primary digital audio interface. Voiceband filtering is available on either interface for outgoing digital audio from the ADC, and incoming data only on the primary S1 digital audio interface. The voiceband filters only operate when the MAX9851/MAX9853 are configured in voice mode. The DAC and ADC voiceband filters are identical, with sample-rate-specific corner frequencies. Operating in 8kHz voice mode, the filter passband extends from 130Hz to 3.5kHz. In 16kHz voice mode, the filter passband extends from 260Hz to 7kHz. Stopband attenuation is greater than 28dB for low frequency and 75dB for high frequencies and the lowpass cutoff frequency is below f_S / 2. See the *Typical Operating Characteristics* for filter characteristics.

Line Inputs

The MAX9851/MAX9853 provide two single-ended audio line inputs for mixing with analog audio from either the ADC record path or to the DAC playback path. Each line input amplifier has a programmable-gain function controlled by PGAL1 and PGAL2 (registers 0x0E and 0x0F). The gain is adjustable over the +30dB to -32dB range in 2dB increments.

DirectDrive Headphone and Receiver Amplifiers

The MAX9851/MAX9853 headphone and receiver amplifiers make use of Maxim's DirectDrive architecture to create ground-biased outputs as shown in Figure 5. Traditional single-supply headphone amplifiers have their outputs biased about a nominal DC voltage, typically half the supply. Large coupling capacitors are typically needed to block this DC bias from the headphone. Without these capacitors, a significant amount of DC current flows to the headphone, resulting in unnecessary power dissipation and possible damage to both headphone and headphone amplifier. The DirectDrive architecture uses a charge pump to create an internal negative supply voltage. This allows the MAX9851/MAX9853 headphone and receiver outputs to be biased about ground, almost doubling the dynamic range while operating from a single supply. With no DC component, there is no need for the large DC-blocking capacitors. Instead of two large (33µF to 330µF) capacitors, the MAX9851/MAX9853 charge pump requires only two small ceramic capacitors (0.22µF and 1µF), conserving board space, reducing cost, improving the frequency response, and THD of the headphone amplifier. In addition to the cost and size disadvantages, the DC-blocking capacitors required by conventional headphone amplifiers limit low-frequency response and decrease PSRR performance. Some dielectrics can significantly distort the audio signal.

Stereo Audio CODECs with Microphone, DirectDrive Headphones, Speaker Amplifiers, or Line Outputs

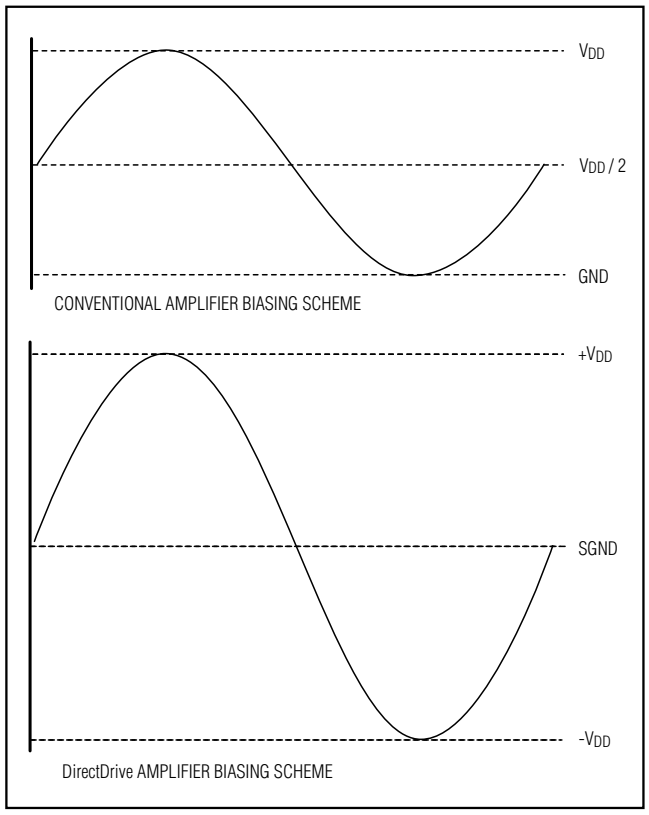


Figure 5. Traditional Amplifier Output vs. MAX9851/MAX9853 DirectDrive Output

Set HRMODE to 100 (register 0x18, bits B2–B0) to enable standard stereo headphone mode. Set HRMODE to 110 to configure balanced mono operation and 101 for single-ended mono operation. When operating in balanced mode, the right headphone amplifier is reconfigured as a slave amplifier to create a bridge-tied load output. In single-ended mono mode, only the left headphone amplifier is used. Both mono modes output the sum of the left- and right-channel audio.

Set HRMODE to 111 to disable the headphone amplifier and enable the mono receiver amplifier. The receiver amplifier outputs a sum of the left and right headphone signals to provide 100mW to a telephone earpiece speaker.

The headphone/receiver amplifiers have programmable gain controlled by HRVOLL and HRVOLR (registers 0x14 and 0x15). The independent gain control offers a range of +5.5dB to -74dB.

Class D Speaker Amplifiers (MAX9851 Only)

Set SPMODE to 11 (register 0x18, bits B4 and B3) to enable the stereo speaker amplifier of the MAX9851. SPMODE can be optionally set to enable just the left or the right speaker. **CPCLK (register 0x1A, bit B0) must be set to 1 to ensure proper Class D amplifier operation.** The Class D amplifier oscillator is derived from MCLK. MCLK must be enabled for proper Class D amplifier operation.

The on-board filterless, low-EMI, Class D audio power amplifier offers Class AB performance with Class D efficiency. The amplifiers are powered directly from the battery (PV_{DD}) for maximum efficiency and power output. A typical output power of up to 2W per channel allows powering of internal speakers without the need for a separate power amplifier IC. The Class D amplifier has been optimized for efficiency and greatly reduced EMI. The output gain is adjustable between +13.1dB and -66.4dB. The gain of the speaker amplifier is controlled with SPVOLL and SPVOLR (registers 0x16 and 0x17, bits B0–B5).

Efficiency

Rather than using a traditional Class AB speaker amplifier, the MAX9851 uses a high-efficiency Class D audio amplifier to provide speaker outputs. The MAX9851 uses Maxim's unique modulation scheme that eliminates the LC filter required by standard Class D amplifiers, improving efficiency, reducing component count, and conserving board space and system cost. Conventional Class D amplifiers output a 50% duty-cycle square wave when no signal is present. With no filter, the square wave appears across the load as a DC voltage, resulting in finite load current, increasing power consumption. When no signal is present at the input of the MAX9851, the outputs switch in-phase at a low duty cycle. Because the MAX9851 drives the speaker differentially, the two outputs cancel, resulting in no net voltage across the speaker, minimizing power consumption.

Filterless Operation

Proprietary active emissions limiting (AEL) output stage circuitry allows the amplifier to operate at switching frequencies above 1MHz while still providing at least 20dB margin below FCC-radiated emissions limits. Set CPCLK = 1 (register 0x1A, bit B0) to configure the Class D amplifier to operate with a 1.1MHz MCLK derived switching frequency. The MAX9851 does not require an output filter, instead relying on the inherent

inductance of the speaker coil to filter the high-frequency PWM components, and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output. Eliminating the output filter results in a smaller, less costly, and more efficient solution. Because the switching frequency of the MAX9851 output is well beyond the bandwidth of cell-phone speakers, voice coil movement due to the square-wave frequency is negligible.

Differential Line Outputs (MAX9853 Only)

The MAX9853 features a pair of differential line outputs instead of the Class D speaker amplifiers of the MAX9851. Set LOMODE to 11 (register 0x18, bits B4 and B3) to enable the stereo line outputs of the MAX9853. The line outputs can be used simultaneously with the headphone or receiver amplifier for maximum flexibility in driving an external audio amplifier or other analog audio IC. The line outputs feature gain adjustable between +7.1dB and -72.4dB. Program the gain of the line outputs with LOPGAL and LOPGAR (registers 0x16 and 0x17, bits B5 to B0).

Shutdown Output and Fault Input

Shutdown output and fault input pins are available for interfacing with an external speaker amplifier IC. The open-drain shutdown output can be used to control an external amplifier through the MAX9853 I²C interface. The fault logic input has an internal 300kΩ pullup resistor which can be reported in the I²C status register and trigger the interrupt output.

Volume Control

The MAX9851/MAX9853 feature volume control amplifiers on the headphone, receiver, speaker (MAX9851 only), and line (MAX9853 only) outputs that can be controlled through the I²C interface. Each output has separate volume control amplifiers for left and right in addition to a mute feature. Set VSEN to 1 (register 0x18, bit B6) to enable volume change smoothing. Enabling this feature gives a smooth-sounding gain change by stepping through all intermediate settings at a 2ms rate per step when a volume or mute change occurs.

Set ZDEN to 1 (register 0x18, bit B5) to enable the zero-crossing detection feature. This causes volume and mute changes to occur only at zero-crossings of the audio waveform and reduces objectionable clicks or "zipper noise" that can occur while making volume changes.

Once the part is initialized, the MCLK is not required during modes where the ADC and DAC are disabled (for instance, playing line inputs through the headphone outputs). However, the part needs MCLK to be applied for a short period of time (> 1ms) after power-on to initialize volume control circuitry—this is only once per power-on.

Microphone Amplifiers

Two microphone interfaces allow the MAX9851/MAX9853 to accommodate inputs from both an internal handset microphone and external headset microphones. Both inputs feature 0 to +20dB of gain selectable in 1dB increments with an additional 20dB of gain selectable to increase the range from 0 to +40dB, accommodating a wide range of microphones.

Set MEXT to 0 (register 0x12, bit B2) to select the internal microphone input, featuring a differential input to minimize noise pickup. A low-noise bias voltage (INTMICBIAS) is available to bias the microphone from a clean supply. The mono input signal is treated as a left microphone signal by MAX9851/MAX9853 internal circuitry. Bypass INTMICBIAS to GND with a 1µF capacitor.

Set MEXT to 1 to select the external microphone input featuring stereo single-ended inputs with a separate ground to reduce noise pickup. Connect the external microphones to EXTMICBIASL and EXTMICBIASR to provide a bias voltage for the microphones. Set RBIAS to 0 (register 0x12, bit B0) to select an output impedance of 2.2kΩ for the independent low-noise bias pins. Alternatively, set RBIAS to 1 to select an output impedance of 470Ω. A microphone bias voltage of +2.4V, generated from INTMICBIAS, is used for both resistor settings. The selectable bias resistors allow extra flexibility in selecting microphones without requiring external resistors to bias the microphones. The 470Ω impedance can be chosen when using an external RC filter near the headset jack. The external biases are high impedance when disabled, even in the presence of an applied voltage up to AV_{DD}.

Sidetone

An internally routed sidetone signal is available to allow analog routing of the left microphone signal. The sidetone input is the output of the left microphone gain amplifier. This sidetone signal has an independent gain adjustment from -32dB to +30dB. The sidetone signal is available as an input to both the left and right analog output mixer (see the *Signal Routing* section).

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$\overline{\text{VIBE}}$ Output

The MAX9851/MAX9853 include a $\overline{\text{VIBE}}$ digital output that may be used to control an external vibrator/transducer, or may be used as a general-purpose output. The Vibe circuitry module has its own multiplexer to allow it to operate from either the S1 or S2 digital audio interface. Set TSEL to 0 (register 0x09, bit B5) to derive the $\overline{\text{VIBE}}$ output from the primary digital audio interface right channel. Set TSEL to 1 to derive the $\overline{\text{VIBE}}$ output from the secondary digital audio interface left or mono-mixed left and right channels.

When using signal data to drive $\overline{\text{VIBE}}$, programmable gain set by TGAIN (register 0x19, bits B7–B4) is used to make adjustments with 10-bit output resolution. A digital lowpass filter is used to condition the signal for use at the $\overline{\text{VIBE}}$ output.

The $\overline{\text{VIBE}}$ output signal may be generated using either a threshold comparison of a rectified signal or by an oversampled 1-bit DAC conversion of a nonrectified signal. Set TMUX to 11 (register 0x09, bits B7–B6) to use the output of the internal sigma-delta converter for driving the transducer output. Set TMUX to 10 to compare the digital audio signal to a programmable squelch threshold level and generate an output signal as shown in Figure 6. When driving an external transducer use an external lowpass filter as shown in Figure 7. The $\overline{\text{VIBE}}$ signal can be amplified if needed by an external amplifier. Set TMUX to 00 or 01 to force the output to a fixed 1 or 0, respectively, when using $\overline{\text{VIBE}}$ as a general-purpose output. Use a 1kΩ pullup resistor to DV_{DD} to achieve a full-scale signal from the open-drain output.

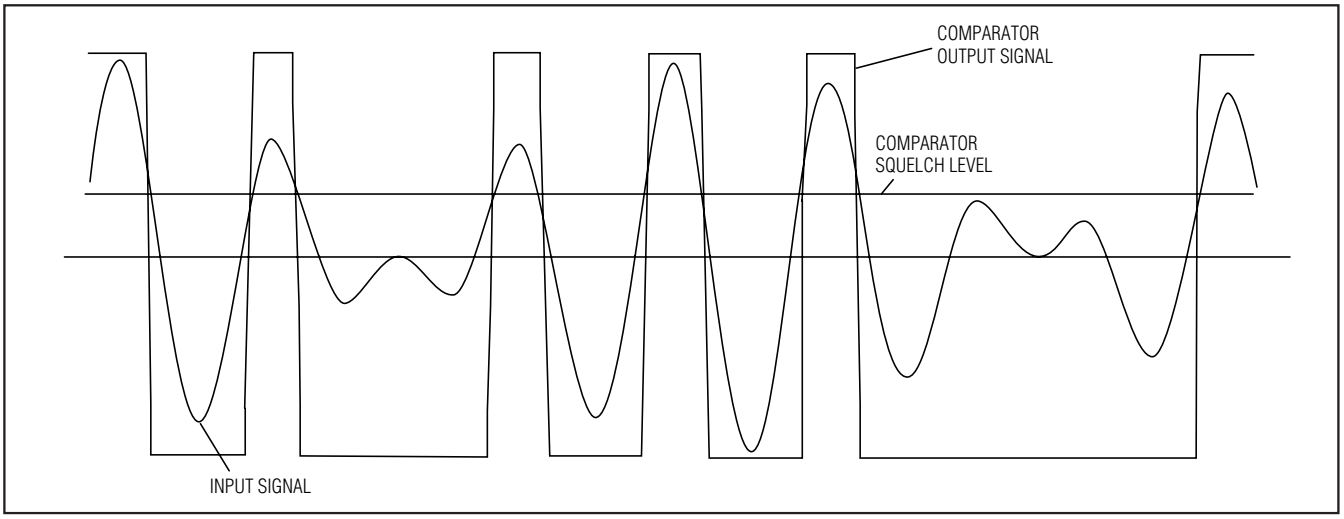


Figure 6. $\overline{\text{VIBE}}$ Output Using Comparator

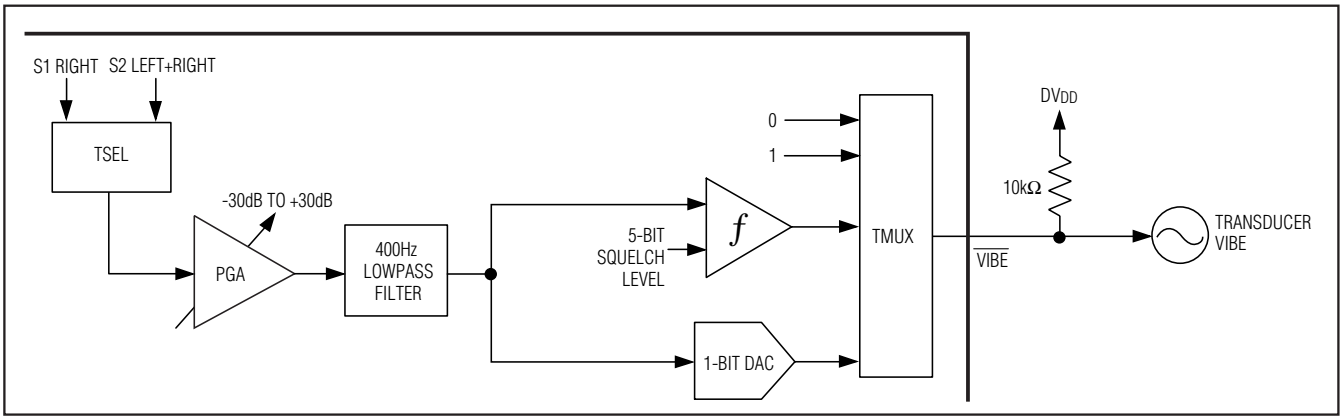


Figure 7. Transducer/Vibe Functional Diagram

Signal Routing

The MAX9851/MAX9853 feature extensive signal-path mixing, allowing nearly any combination of inputs and outputs.

DAC Inputs

Use MIXDAL and MIXDAR (register 0x08–see the *I²C Registers and Bit Descriptions* section for detailed register definitions) to configure the digital mixer at the input of each DAC. The mixer allows signals from each digital audio interface to be mixed prior to conversion, regardless of sampling rate and synchronization. Each left and right data stream can be routed independently to either the left or right DAC to allow for swapping of the left and right channels and any possible combination of digital signals.

Audio Outputs

Configure MXOUTL and MXOUTR (register 0x0B–see the *I²C Registers and Bit Descriptions* section for detailed register definitions) to adjust the analog output mixer. This mixer combines signals prior to the analog output stages: consisting of the headphone amplifier, receiver amplifier, and speaker or line amplifiers. Each line input, in addition to the analog sidetone, can be mixed with the left or right DAC output prior to amplification.

ADC Inputs

Use MXINL and MXINR (register 0x0A–see the *I²C Registers and Bit Descriptions* section for detailed register definitions) to configure the ADC mixer. Each ADC has the option of converting the left microphone signal, the right microphone signal, and each of the line inputs. This allows for maximum flexibility when recording input signals.

Charge Pump

The DirectDrive headphone and receiver outputs of the MAX9851/MAX9853 require a charge pump to create an internal negative power supply. Set CPEN = 1 (register 0x1A, bit B4) to turn on the charge pump. The negative charge-pump voltage is established and the audio outputs are ready for use approximately 70ms after CPEN is set to 1. The state of CPCLK (register 0x1A, bit B0) determines whether the charge-pump oscillator is derived from the internal 650kHz oscillator or from the MCLK. Set LFEN = 1, CPEN = 1 and set CPCLK = 0 (register 0x1A, Bits B5, B4 and B0) to enable the charge pump using the internal oscillator. The charge pump runs independent from MCLK when the internal oscillator is enabled allowing the charge pump to operate when the DAC is disabled or when only the line inputs are used. Set CPCLK = 1 to synchronize the charge pump with the MCLK. The switching frequency of the charge pump is well beyond the audio range and does not interfere with audio signals. The switch drivers utilize techniques that minimize noise generated by turn-on and turn-off transients. Although not typically required, additional high-frequency noise attenuation can be achieved by increasing the size of C2 and the CPV_{DD} bypass capacitor (see the *Functional Diagrams/Typical Operating Circuits*).

Headset Detect

The MAX9851/MAX9853 feature comprehensive headset detection to accommodate a wide variety of headsets. Two operating modes are provided: one for wake-up upon headset insertion and one for detecting the configuration of the headset in use. While in sleep mode, the detection circuitry can be used to detect the insertion of a headset and trigger a hardware interrupt. In this mode, the circuitry can be powered directly from the battery using minimal power. When a headset is inserted, the microcontroller (µC) can detect the hardware interrupt and bring the system out of low-power standby. The µC can then determine the configuration of the inserted headset and appropriately configure the MAX9851/MAX9853. Figure 8 shows the headset detection circuitry.

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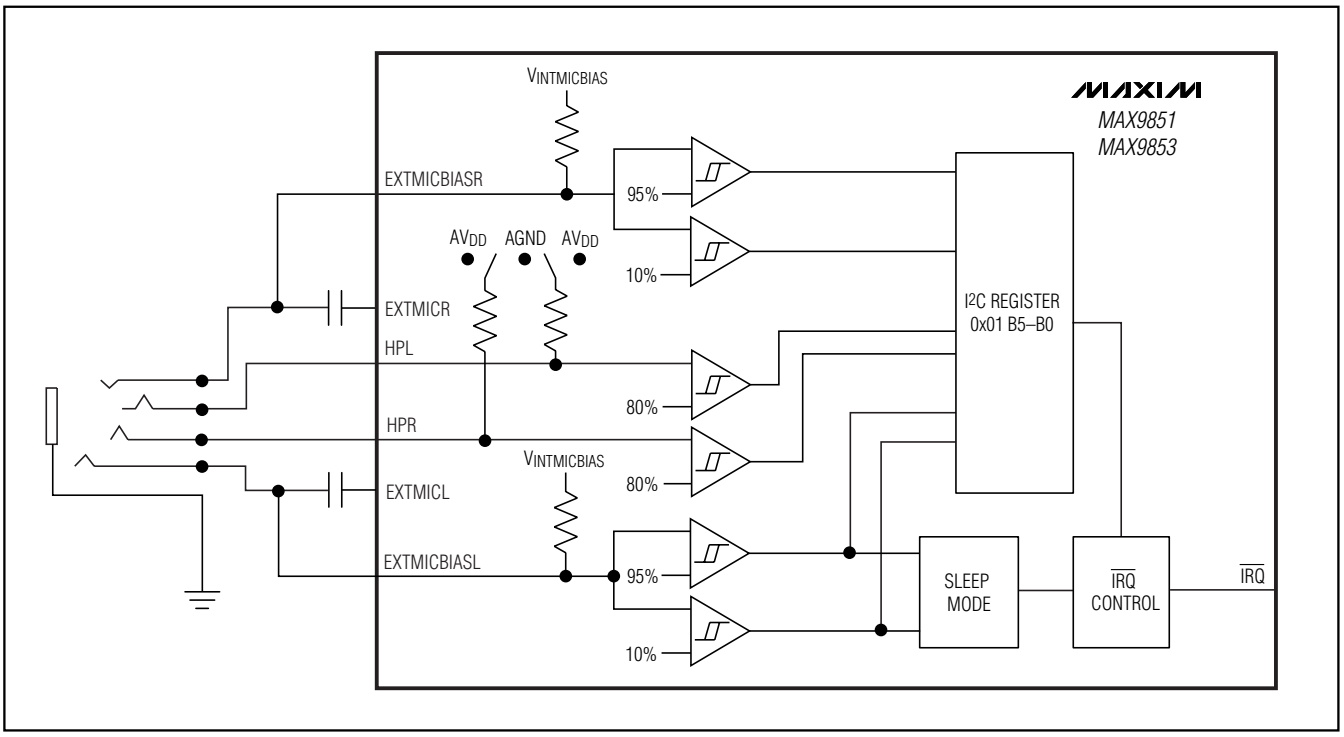


Figure 8. Headset-Detection Circuitry

Power-Off/Sleep Mode

When the analog or digital supplies are removed from the MAX9851/MAX9853, the headset detect circuit enters sleep mode (PV_{DD} must remain powered, typically through a direct connection to the battery). Alternatively, set SLEEP = 1 (register 0x19, bit B2) to allow sleep mode to monitor headset insertion and removal while the MAX9851/MAX9853 are in low-power shutdown. In this mode, the external headset jack is monitored for activity, but no attempt is made to detect the headset configuration. For proper operation, the battery voltage must be available, through PV_{DD}. A low-current bias is supplied to EXTMICBIASL to allow detection of activity. If this pin is pulled low at any time, a hardware interrupt is triggered and $\overline{IRQ}$ is set. $\overline{IRQ}$ remains asserted until sleep mode is exited or the headset jack is removed. Any pullup resistor on the open-drain $\overline{IRQ}$ output will cause a small current to be drawn until the µC can initiate a power-up sequence. Once power is applied to the MAX9851/MAX9853, or SLEEP is set to 0, the sleep mode is disabled and normal headset detect functions can be used.

In sleep mode it is important that the microphone bias be disabled by setting RBEN to 0, and that no parasitic diodes load the EXTMICBIASL/R pins. Also note that the autodetect circuitry will trigger $\overline{IRQ}$ for approximately 50ms when PV_{DD} is initially applied or when sleep mode is first enabled. This is a consequence of the weak pullup current used to sense EXTMICBIASL and the attached AC-coupling capacitor that must be charged.

Normal Operation

Set ENA to 1 (register 0x19, bit B3) and HSTEST to 01 (register 0x19, bits B1–B0) to enable normal operation. In this mode EXTMICBIASL, EXTMICBIASR, HPL, and HPR are probed to determine the loading of each pin. The detected loading is then reported in the HSDET bits (status register 0x01 B5–B0). The loading of each pin is shown in Table 3 along with the reported HSDET code. The headset configuration that corresponds to some possible loading states is shown in Table 4.

Headphone detection is done in a two-step process. Test 1 (HSTEST = 01) is used to determine if stereo headphones are connected. If a balanced mono headphone is connected, this test will be inconclusive. Test 2 (HSTEST = 10) must then be performed to determine the configuration. See Figure 9 for the typical headphone test procedure.

Table 3. HSDET Bit Decode

HSDET	HPR	HPL	EXTMICBIASL	EXTMICBIASR
[11XXXX]	x	x	Low	x
[01XXXX]	x	x	Mid	x
[00XXXX]	x	x	High	x
[XX1XXX]	Low	x	x	x
[XX0XXX]	High	x	x	x
[XXX1XX]	x	Low	x	x
[XXX0XX]	x	High	x	x
[XXXX11]	x	x	x	Low
[XXXX01]	x	x	x	Mid
[XXXX00]	x	x	x	High

Table 4. Example Headset Configurations

HEADSET CONFIGURATION	HPR	HPL	EXTMICBIASL	EXTMICBIASR
No External Connector	High	High	High	High
3-Pole Connector				
Mono HP, Mono Microphone	Low	High	Mid	High
4-Pole Connector				
Stereo HP, Mono Microphone	Low	Low	Mid	High
Mono HP, Stereo Microphone	Low	High	Mid	Mid
5-Pole Connector				
Stereo HP, Stereo Microphone	Low	Low	Mid	Mid
Test 2 Only*				
No HP	Low	High	X	X
Mono Balanced HP	Low	Low	X	X
Mono Balanced HP, Mono Microphone	Low	Low	Mid	High
Mono Balanced HP, Stereo Microphone	Low	Low	Mid	Mid

**Test 2 is to be performed after Test 1 finds HPR and HPL High. Test 2 is needed only to determine if a balanced mono speaker is connected to HPR and HPL.*

Microphone detection is provided by the microphone bias circuitry. Set RBEN, MICLEN, and MICREN to 1 (register 0x12, bit B1 and register 0x1B, bits B1 and B0) to enable the microphone bias circuitry. The microphone bias voltage is compared with two thresholds, 95% and 10% of $V_{INTMICBIAS}$. The thresholds define three output-impedance states: high, medium, and low. The high-impedance state occurs when there is no load on the EXTMICBIAS pins. The medium state occurs when the load is an electret module or an amplified microphone biased at midsupply. The low state occurs when the microphone pin is shorted to AGND by a hook switch or an accessory logic/identification pin. Alternatively, hook switches that disconnect the microphone can be detected by looking for the high state.

Headphone detection is accomplished by placing a small pullup current on HPL and HPR. For proper headphone detection, make sure that the headphone amplifiers are disabled. Set HSTEST to 01 (register 0x19, bit B1 and B0) to enable headphone Test 1 (see Table 5). The sense bias for the headphone pins attempts to pull both HPL and HPR up to AV_{DD} with a low current to avoid creating an audible disturbance on the headphones. When a stereo headphone is connected, both HPR and HPL are pulled low. When no headphone is connected, or a balanced mono speaker has been

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connected, HPR and HPL are pulled high by the internal sense bias. To detect the balanced mono configuration, set HSTEST to 10 to enable Test 2. Test 2 connects a small pulldown current to HPR and a pullup to HPL. A balanced mono speaker will result in HPL pulled low whereas an open circuit would still allow HPL to be pulled high by AV_{DD}. Attempting to detect the headphone configuration while the amplifiers are active will lead to erroneous results as the outputs of the active headphone amplifiers are biased at 0V.

In normal headset detect mode, the removal or insertion of a jack, as monitored by EXTMICBIASL, triggers an interrupt on the $\overline{IRQ}$ pin. The state changes that trigger an interrupt are shown in Table 6. Alternatively, set IHSD = 1 (register 0x02, bit B1) to cause all changes in the HSDET bits to trigger an interrupt. Changes to HSDET are digitally debounced with a 20ms filter.

Interrupt Output

Hardware interrupts are reported on the MAX9851/MAX9853 open-drain $\overline{IRQ}$ pin. The interrupt pin can be triggered by the sources shown in Table 7. When an interrupt occurs, $\overline{IRQ}$ remains low until the interrupt is serviced by reading the status register 0x00. If an interrupt occurs, it will be reported only if the corresponding interrupt enable is set in register 0x02 (see the *I²C Registers and Bit Descriptions* section for detailed register definitions).

Table 5. Headphone Detect Test Modes

HSTEST(1:0)	CONFIGURATION
00	Headphone sense bias disconnected
01	Headphone sense test 1 (standard headphone detection)
10	Headphone sense test 2 (balanced mono headphone detection)
11	Reserved

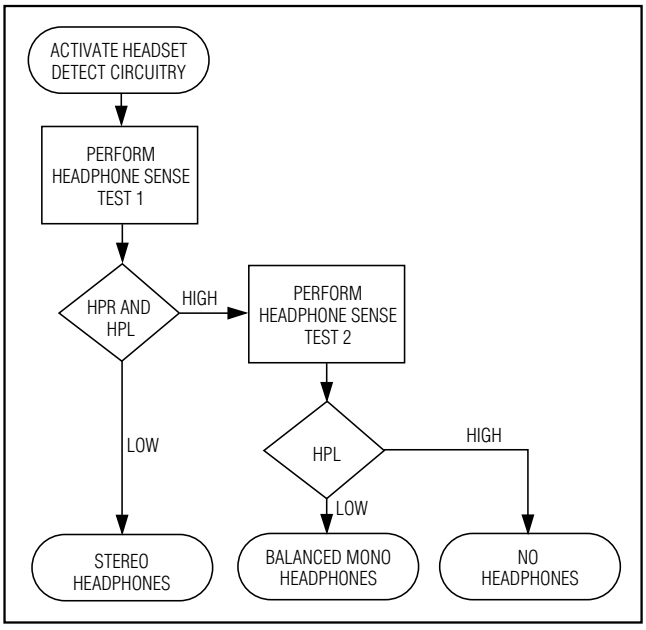


Figure 9. Headphone Detection Procedure

Table 6. Headset Pin Changes Causing Hardware Interrupts

PIN-STATE CHANGE	DESCRIPTION
EXTMICBIASL: high → low or mid	Headset inserted
EXTMICBIASL: mid → low	Hook switch pressed
EXTMICBIASL: low → mid	Hook switch released
EXTMICBIASL: low → high	Headset removed

Table 7. Sources of Hardware Interrupts

INTERRUPT SOURCES	MASKABLE IN REGISTER (0x02)
Clip Detect	Yes
Slew Level Detect	Yes
Digital PLL UnLock	Yes
Headset Configuration Change	Yes
Headset Removal and Insertion	No
Speaker/External Fault	Yes

I²C Registers and Bit Descriptions

Twenty-eight internal registers program and report the status of the MAX9851/MAX9853. Table 8 lists all of the registers, their addresses, and power-on-reset states. Registers 0x00 and 0x01 are read-only while all of the other registers are read/write. Registers 0x1C–0x1F are reserved for factory testing. Write zeros to all unused bits in the register table when updating the register, unless otherwise noted.

Slave Address

The MAX9851/MAX9853 are preprogrammed with a slave address of 0x20 or 0010000. The address is defined as the 7 most significant bits (MSBs) followed by the read/write bit. Set the read/write bit to 1 to configure the MAX9851/MAX9853 to read mode. Set the read/write bit to 0 to configure the MAX9851/MAX9853 to write mode. The address is the first byte of information sent to the MAX9851/MAX9853 after the START condition.

Table 8. Register Map

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS	POWER-ON RESET STATE
STATUS										
Status 0	CLD	SLD	ULK	0	0	0	HSD	FAULT	0x00	—
Status 1	AOK	1	HSDET						0x01	—
Interrupt Enable	ICLD	ISLD	IULK	0	0	0	IHSD	IFAULT	0x02	0x00
DIGITAL AUDIO S1										
Interface Mode	S1SDO	S1SDI	S1MNO	0	S1MODE				0x03	0x00
Interface Mode	S1MAS	S1WCI	S1BCI	0	S1DLY	0	0	S1WS	0x04	0x00
DIGITAL AUDIO S2										
Interface Mode	S2SDO	S2SDI	S2MNO	0	S2MODE				0x05	0x00
Interface Mode	S2MAS	S2WCI	S2BCI	0	S2DLY	0	0	S2WS	0x06	0x00
DIGITAL FILTERS										
Filter Modes	MHZ	ADCDC	ABPE	DBPE	DHPL		DHPR		0x07	0x70
DIGITAL MIXERS										
DAC-L/R Mixer	MIXDAL				MIXDAR				0x08	0x20
TRANSDUCER/VIBE										
T-DAC MUX/ Squelch	TMUX		TSEL	VTH					0x09	0x00
ANALOG MIXERS										
ADC Input Mixers	MXINL				MXINR				0x0A	0x00
Audio Output Mixers	MXOUTL				MXOUTR				0x0B	0x00
AUDIO GAIN										
Audio Interface S1 Gain	PGADS1								0x0C	0x00
Audio Interface S2 Gain	PGADS2								0x0D	0x00
Line1 Input Gain	0	0	0	PGAL1					0x0E	0x00
Line2 Input Gain	0	0	0	PGAL2					0x0F	0x00

Table 8. Register Map (continued)

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS	POWER-ON RESET STATE
Microphone L Input Gain	0	0	PALEN	PGAML					0x10	0x00
Microphone R Input Gain	0	0	PAREN	PGAMR					0x11	0x00
MICROPHONE										
Microphone Mode	0	0	0	0	MMIC	MEXT	RBEN	RBIAS	0x12	0x00
AUDIO VOLUME										
Sidetone Volume	0	0	0	PGAS					0x13	0x00
Headphone/ Receiver Volume Left	0	HRMUT	HRVOLL						0x14	0x00
Headphone/ Receiver Volume Right	0	0	HRVOLR						0x15	0x00
Left Speaker Volume[1] or Line Output Gain[2]	0	SPMUT[1] or LOMUT[2]	SPVOLL[1] or LOPGAL[2]						0x16	0x00
Right Speaker Volume[1] or Line Output Gain[2]	0	0	SPVOLR[1] or LOPGAR[2]						0x17	0x00
AUDIO OUTPUT										
Audio Output Mode	0	VSEN	ZDEN	SPMODE[1] or LOMODE[2]		HRMODE			0x18	0x00
VIBE/HEADSET DETECT										
T-DAC PGA/HSET Detect	TGAIN				ENA	SLEEP	HSTEST		0x19	0x00
SYSTEM										
System	$\overline{\text{SHDN}}$	HFEN	LFEN	CPEN	0	1	0	CPCLK	0x1A	0x00
SHUTDOWN										
Audio Shutdown	DACLEN	DACREN	ADCLEN	ADCREN	DATEN	0	MICLEN	MICREN	0x1B	0x00

[1] *MAX9851*

[2] *MAX9853*

Status Registers (0x00, 0x01)

Table 9. Status Register 0

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x00	CLD	SLD	ULK	0	0	0	HSD	FAULT

Bits in status registers 0x00 and 0x01 are set when an alert condition exists. The status bits are only updated if the corresponding interrupt enable is set in register 0x02. All bits in status register 0x00 are automatically cleared upon a read operation of the register and will be set again if the condition remains or occurs following the read of this register.

Clip Detect Flag (CLD)

1 = DAC or ADC clipping has occurred.

0 = No clipping has occurred.

CLD reports that the DAC input data or ADC output data is clipping due to an excessive signal amplitude in the digital signal path at any one of seven locations: DAC mono mixer (left or right), DAC modulator (left or right), ADC path highpass filter (left or right), or the $\overline{VIBE}$ path modulator. To resolve a clip condition in the signal path, the DAC gain settings and analog input gain settings should be lowered. As the CLD bit does not indicate where the overload has occurred, identify the source by lowering gains individually.

Slew Level Detect Flag (SLD)

1 = Volume slewing complete.

0 = No volume slewing sequences have completed since the status register was last read.

SLD reports that any one of the programmable-gain arrays or volume controllers has completed slews from a previous setting to a new programmed setting. If multiple gain arrays or volume controllers are changed at the same time, in either the analog or digital domain, SLD flag will be set after the last slew adjusting in each domain. SLD also reports when the serial interface soft-start or soft-stop process has completed.

Digital PLL Unlock Flag (ULK)

1 = Either the S1 or S2 internal DAC PLL is not locked.

0 = Both the S1 and S2 internal PLLs are locked if enabled and operating properly.

ULK reports that the digital audio phase-locked loop for either DAC became unlocked and input digital signal data is unreliable.

Headset Configuration Change Flag (HSD)

1 = Headset configuration has changed.

0 = No change in headset configuration.

HSD reports changes in HSDET (register 0x01, bits B5–B0). Regardless of the state of IHSD, any removal or insertion of a jack (detected by monitoring EXTMICBIASL) triggers an interrupt on the $\overline{IRQ}$ line. See the *Headset Detect* section. Changes on HSDET are digitally debounced with an approximate 20ms filter before setting HSD. Valid changes on HSDET are delayed by this amount. MCLK needs to be applied for a short period of time (> 1ms) after power-on to initialize this flag.

MAX9851: Speaker Fault Flag (FAULT)

1 = Current overload has occurred on the speaker amplifiers.

0 = Current consumption is normal.

For the MAX9851, FAULT indicates that the Class D output amplifiers have entered a current overload state.

MAX9853: External Fault Flag (FAULT)

1 = The FAULTIN pin has been pulled low.

0 = FAULTIN pin high.

For the MAX9853, FAULT indicates that the FAULTIN pin has been pulled low.

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Table 10. Status Register 1

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x01	AOK	1	HSDET					

Analog Section OK (AOK)

1 = Analog circuitry operating properly.

0 = Analog startup not complete or the MAX9851/MAX9853 are in shutdown.

AOK reports that the analog section of the MAX9851/MAX9853 is properly operating. When power is applied to MAX9851/MAX9853, the AOK bit is set to 0. The MAX9851/MAX9853 must be taken out of shutdown and the charge pump must be operating for this bit to be set to 1. The digital signal processing sections of the MAX9851/MAX9853 do not operate unless this bit is 1.

Headset Jack Mode Indicator (HSDET)

HSDET reports the load impedance of the four headset test pins, EXTMICBIASL, EXTMICBIASR, HPL, and HPR, for use in determining the connected headset configuration. See Table 3 in the *Headset Detect* section for decoding the value of these bits.

Interrupt Enable Register (0x02)

Table 11. Interrupt Enables

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x02	ICLD	ISLD	IULK	0	0	0	IHSD	IFAULT

Clip Detect Interrupt Enable (ICLD)

1 = Detection of clipping triggers a hardware interrupt and sets CLD (register 0x00, B7).

0 = Clipping not reported.

Slew Detect Interrupt Enable (ISLD)

1 = Completion of a slewed volume change triggers a hardware interrupt and sets SLD (register 0x00, B6).

0 = Completion of slewing not reported.

Digital PLL Unlock Interrupt Enable (IULK)

1 = An unlock condition in the internal PLLs trigger a hardware interrupt and sets ULK (register 0x00, B5).

0 = Unlock conditions not reported.

Headset Detect Interrupt Enable (IHSD)

1 = All changes in headset configuration trigger a hardware interrupt and set HSD (register 0x00, B1).

0 = Only jack insertions and removals are reported.

If IHSD = 0 any removal or insertion of a jack (detected by monitoring EXTMICBIASL) will still trigger an interrupt on the $\overline{IRQ}$ line, but other HSDET bit changes will not.

MAX9851: Speaker Fault Interrupt Enable (IFAULT)

1 = Current overload at the Class D speaker amplifier triggers a hardware interrupt and sets FAULT (register 0x00, B0).

0 = Current overload not reported.

MAX9853: External Fault Interrupt Enable (IFAULT)

1 = Inputs on FAULTIN trigger a hardware interrupt and set FAULT (register 0x00, B0).

0 = Fault inputs not reported.

Audio Interface Registers (0x03, 0x04, 0x05, 0x06)

Table 12. Audio Interface S1

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x03	S1SDO	S1SDI	S1MNO	0	S1MODE			
0x04	S1MAS	S1WCI	S1BCI	0	S1DLY	0	0	S1WS
0x05	S2SDO	S2SDI	S2MNO	0	S2MODE			
0x06	S2MAS	S2WCI	S2BCI	0	S2DLY	0	0	S2WS

Serial Data Output Enable (S1SDO/S2SDO)

1 = Digital audio output enabled.

0 = Digital audio output disabled.

S1SDO/S2SDO = 1 configures the MAX9851/MAX9853 to route ADC output data to the respective audio interface output pin. S1SDO/S2SDO = 0 forces SDOUTS1/SDOUTS2 low.

When both S1SDO and S2SDO are enabled, the S1 and S2 interfaces output the same data. If both outputs are enabled, the individual interfaces may be configured into different format modes as long as the programmed sample rates are identical.

Serial Data Input Enable (S1SDI/S2SDI)

1 = Digital audio input enabled.

0 = Digital audio input disabled.

S1SDI/S2SDI = 1 configures the MAX9851/MAX9853 to perform a soft-start sequence and transfer incoming audio data from the respective SDIN pin to the digital filters for that interface. S1SDI/S2SDI = 0 configures the MAX9851/MAX9853 to begin a soft-stop sequence and then disregard incoming audio data and disable the digital input filter path of that interface.

The SLD (register 0x00, B6) flag is set when the soft-start or soft-stop sequence completes. The S1SDI and S2SDI bits should be used to cleanly soft-stop signal data prior to changing the S1MODE or S2MODE bits. Soft-stop sequences take approximately 10ms to completely slew the volume from full scale to mute. Set the S1SDI/S2SDI bits to enable the DACs after DACLEN and DACREN (register 0x1B, bits B7 and B6) are set for clean startup transitions. Likewise, clear S1SDI/S2SDI before clearing DACLEN and DACREN.

Serial Input Mono Mix Enable (S1MNO/S2MNO)

1 = Left and right digital input signals mixed to mono and output to the left channel.

0 = Stereo left and right digital signals maintained.

The mono signal is digitally filtered and interpolated through the left-channel digital filter while the right-channel digital filter is shut down. The output of the left-channel filter can be routed to either or both the left and right DACs. The stereo inputs are not attenuated before mixing to mono. Clipping can occur with large input signals.

Interface S1/S2 Mode (S1MODE/S2MODE)

S1MODE/S2MODE configures the MAX9851/MAX9853 for a specific audio sampling rate on the respective digital audio interface. Set S1MODE/S2MODE to 0x1 through 0x9 to configure the interface for stereo audio operation at the specified sample rate. Set S1MODE/S2MODE to 0xA or 0xB to configure the interface to operate in voice mode. The secondary digital audio interface is intended to be used primarily in modes 0x1 through 0x9 as voiceband filtering is available only on the primary serial interface. MCLK must be 26MHz when operating in 16kHz voice mode.

Table 13. Serial Interface Modes of Operation

S1 MODE/ S2 MODE	RATE (kHz)	MODE
0x0	—	Interface off
0x1	8	Stereo audio
0x2	11.025	Stereo audio
0x3	12	Stereo audio
0x4	16	Stereo audio
0x5	22.05	Stereo audio
0x6	24	Stereo audio
0x7	32	Stereo audio
0x8	44.1	Stereo audio
0x9	48	Stereo audio
0xA	8	Mono voice mode
0xB	16	Mono voice mode (MCLK must be 26MHz)
0xC, 0xD, 0xE, 0xF	—	Reserved

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Master Mode (S1MAS/S2MAS)

1 = Master mode (LRCLK and BCLK timing signals generated internally; LRCLK and BCLK configured as outputs).

0 = Slave mode (LRCLK and BCLK accepted from external source; LRCLK and BCLK configured as inputs).

Slave mode timing signals may operate asynchronous to either the MCLK or the other audio interface source in DAC-only stereo audio modes. An interface with the ADC output enabled must operate in master mode, unless operating synchronously in voice mode.

LRCLK Invert (S1WCI/S2WCI)

1 = Right-channel data is transmitted while LRCLK is low.

0 = Left-channel data is transmitted while LRCLK is low.

Set S1WCI/S2WCI = 0 to conform to the I²S standard. S1WCI/S2WCI have no effect in voice mode.

BCLK Invert (S1BCI/S2BCI)

1 = Digital audio bits are transferred on the falling edge of BCLK.

0 = Digital audio bits are transferred on the rising edge of BCLK.

Set S1BCI/S2BCI = 0 to conform to the I²S standard.

Data Delay (S1DLY/S2DLY)

1 = Digital audio MSB on SDIN and SDOUT is transferred on the 2nd BCLK edge following an LRCLK edge.

0 = Digital audio MSB on SDIN and SDOUT is transferred on the 1st BCLK edge following an LRCLK edge.

Set S1DLY/S2DLY = 1 to conform to the I²S standard. S1DLY/S2DLY have no effect in voice mode.

Word Size (S1WS/S2WS)

1 = 18-bit digital audio data.

0 = 16-bit digital audio data.

When operating in master mode, the number of BLCK cycles per sample corresponds to the word size selected by S1WS/S2WS. S1WS/S2WS have no effect in voice mode.

Digital Filter Register (0x07)

Table 14. Digital Filter

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x07	MHZ	ADCDC	ABPE	DBPE	DHPL		DHPR	

MCLK Frequency Mode (MHz)

1 = 26MHz MCLK.

0 = 13MHz MCLK.

A 26MHz clock allows for synchronous 16kHz voice mode. All other modes of operation can operate from either MCLK frequency.

ADC DC-Blocking Filter Enable (ADCDC)

1 = ADC DC block enabled.

0 = ADC DC block disabled.

DC-blocking consists of a highpass filter with a cutoff frequency of f_S / 1608. This filter is available in all modes of operation including voice modes. The ADC DC-blocking filter can be overloaded with low-frequency signals with DC offset greater than ±0.125V (one-eighth full scale).

ADC Bandpass Filter Enable (ABPE)

1 = ADC bandpass filter enabled.

0 = ADC bandpass filter disabled.

ABPE = 1 enables the ADC highpass filter in combination with the ADC lowpass filter to create a bandpass filter. The ADC voiceband filters only operate on the left output channel data of voiceband, the ADC, and when operating in voice mode.

DAC Bandpass Filter Enable (DBPE)

1 = DAC bandpass filter enabled.

0 = DAC bandpass filter disabled.

DBPE = 1 enables the DAC highpass filter in combination with the DAC lowpass filter to create a bandpass filter. The DAC filters only operate on the S1 left input or mono S1 L+R input signal data.

Left and Right DAC Highpass Filter Mode (DHPL/DHPR)

00 = No filtering.

01 = 55Hz to 91Hz cutoff frequency.

10 = 171Hz to 279Hz cutoff frequency.

11 = 327Hz to 533Hz cutoff frequency.

When both the ADC and DAC are enabled, the exact cutoff frequency of each setting depends on the sample rate in use. In DAC-only mode, the exact cutoff frequency will be the high end of the range above.

Digital Mixer Register (0x08)

Table 15. DAC Input Mixer

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x08	MIXDAL				MIXDAR			

Left and Right DAC Input Mixer (MIXDAL/MIXDAR)

Table 16 shows the possible mixing configurations of the incoming digital audio streams. Each of the four digital audio streams can be mixed in any combination and routed to the left or right DAC independently.

Table 16. DAC Input Mixer

INPUT SOURCE	MIXDAL LEFT DAC (REGISTER 0x08, BITS B7–B4)	MIXDAR RIGHT DAC (REGISTER 0x08, BITS B3–B0)	DESCRIPTION
S1 Left	XX1X	XX1X	Mix the primary digital audio interface left channel
S1 Right	XXX1	XXX1	Mix the primary digital audio interface right channel
S2 Left	1XXX	1XXX	Mix the secondary digital audio interface left channel
S2 Right	X1XX	X1XX	Mix the secondary digital audio interface right channel

X = Don't care.

Transducer/Vibe Register (0x09)

Table 17. Transducer/Vibe Bit Descriptions

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x09	TMUX		TSEL	VTH				

Transducer/Vibe DAC Output Select (TMUX)

00 = $\overline{VIBE}$ is high.

01 = $\overline{VIBE}$ is low.

10 = Inverted threshold comparator output connected to $\overline{VIBE}$.

11 = Inverted 1-bit DAC nonfiltered output connected to $\overline{VIBE}$.

See the *$\overline{VIBE}$ Output* section. TMUX selects the signal path of the $\overline{VIBE}$ output. Set TSEL (register 0x07, B5).

Transducer/Vibe DAC Path Enable (TSEL)

1 = Secondary (S2) left or left + right digital audio signal.

0 = Primary (S1) right digital audio signal.

TSEL = 0 configures the MAX9851/MAX9853 to use the right channel of the primary digital audio interface for transducer/vibe signal conditioning. TSEL = 1 configures the MAX9851/MAX9853 to use the left channel (or left + right if S2 mono mix is enabled) of the secondary digital audio interface for transducer/vibe signal conditioning.

Transducer/Vibe Squelch Comparator Threshold (VTH)

When using the comparator for $\overline{VIBE}$ output, program VTH to set the level that positive digital audio data will be compared against. If the input data is less than VTH, then $\overline{VIBE}$ = 1. If the input data is greater than VTH, then $\overline{VIBE}$ = 0. If VTH = 0x00, all negative signal values will force $\overline{VIBE}$ high and all positive values will force $\overline{VIBE}$ low (see Figure 6 for operation).

Table 18. Vibe Threshold

VTH	THRESHOLD VALUE
0x1F	31/32 x FS
0x1E	30/32 x FS
0x1D	29/32 x FS
0x1C	28/32 x FS
0x1B	27/32 x FS
0x1A	26/32 x FS
0x19	25/32 x FS
0x18	24/32 x FS
0x17	23/32 x FS
0x16	22/32 x FS
0x15	21/32 x FS
0x14	20/32 x FS
0x13	19/32 x FS
0x12	18/32 x FS
0x11	17/32 x FS
0x10	16/32 x FS
0x0F	15/32 x FS
0x0E	14/32 x FS
0x0D	13/32 x FS
0x0C	12/32 x FS
0x0B	11/32 x FS
0x0A	10/32 x FS
0x09	9/32 x FS
0x08	8/32 x FS
0x07	7/32 x FS
0x06	6/32 x FS
0x05	5/32 x FS
0x04	4/32 x FS
0x03	3/32 x FS
0x02	2/32 x FS
0x01	1/32 x FS
0x00	0

Analog Mixer Registers (0x0A, 0x0B)

Table 19. Audio Mixer Bit Descriptions

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x0A	MXINL				MXINR			
0x0B	MXOUTL				MXOUTR			

Left and Right ADC Input Mixer (MXINL/MXINR)

Table 20. ADC Input Mixer

INPUT SOURCE	MIXINL LEFT ADC (REGISTER 0x0A, Bits B7–B4)	MIXINR RIGHT ADC (REGISTER 0x0A, Bits B3–B0)	DESCRIPTION
Line 1	1XXX	1XXX	Mix line input 1
Line 2	X1XX	X1XX	Mix line input 2
Left Microphone	XX1X	XX1X	Mix the left microphone input
Right Microphone	XXX1	XXX1	Mix the right microphone input

X = Don't care.

Table 20 shows the possible mixing configurations of the analog input signals at the ADC. Each of the four input signals can be routed to either the left or right ADC independently in any combination. The ADC will provide erroneous results if the microphones are selected as a mixer input while the microphone circuit is not enabled.

Left and Right Audio Output Mixer (MXOUTL/MXOUTR)

Table 21. Analog Output Mixer

INPUT SOURCE	MXOUTL LEFT AUDIO OUTPUT (REGISTER 0x0B, BITS B7–B4)	MXOUTR RIGHT AUDIO OUTPUT (REGISTER 0x0B, BITS B3–B0)	DESCRIPTION
Sidetone	1XXX	1XXX	Mix the sidetone
Line 1	X1XX	X1XX	Mix line input 1
Line 2	XX1X	XX1X	Mix line input 1
Left DAC Output	XXX1	XXXX	Mix the left DAC output to the left analog output
Right DAC Output	XXXX	XXX1	Mix the right DAC output to the right analog output

X = Don't care.

Table 21 shows the possible mixing configurations of the analog audio output mixer. The sidetone, line 1, and line 2 signals can be routed to either the left or right audio output in the combinations shown in Table 21. The left DAC output is only available on the left audio output and similarly for the right DAC output.

Audio Gain Control Registers (0x0C, 0x0D, 0x0E, 0x0F, 0x10, 0x11)

Table 22. Digital Audio Input Gain Bit Descriptions

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x0C	PGADS1							
0x0D	PGADS2							

Programmable-Gain Adjustment for Digital Audio Inputs (PGADS1/PGADS2)

PGADS1/PGADS2 configures the gain adjustment for the digital audio interface inputs. Code 0x00 is full signal while 0xFF is full attenuation. This programmable-gain adjustment follows the mono mixers. Table 23 shows simplified gain control settings for digital signal inputs.

Table 23. Digital Audio Input Gain Settings

PGADS1/ PGADS2	SETTING (dB)
0x00	0
0x0E	-1
0x1C	-2
0x29	-3
0x35	-4
0x40	-5
0x4A	-6
0x55	-7
0x5E	-8
0x67	-9
0x70	-10
0x78	-11
0x7F	-12
0x86	-13

PGADS1/ PGADS2	SETTING (dB)
0x8D	-14
0x93	-15
0x99	-16
0x9F	-17
0xA5	-18
0xAA	-19
0xAE	-20
0xB3	-21
0xB7	-22
0xBB	-23
0xBF	-24
0xC2	-25
0xC6	-26
0xC9	-27

PGADS1/ PGADS2	SETTING (dB)
0xCC	-28
0xCF	-29
0xD2	-30
0xD4	-31
0xD6	-32
0xD9	-33
0xDB	-34
0xDD	-35
0xDF	-36
0xE1	-37
0xE2	-38
0xE4	-39
0xE5	-40
0xFF	Mute

Table 24. Line Input Gain Bit Descriptions

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x0E	0	0	0	PGAL1				
0x0F	0	0	0	PGAL2				

Programmable-Gain Adjustment for Line Inputs (PGAL1/PGAL2)

PGAL1/PGAL2 configures the programmable-gain adjustment setting for line input 1/line input 2. Code 0x00 is maximum gain while 0x1F is maximum attenuation. Table 25 lists the gain setting for each code.

Table 25. Line Input Gain Control Settings

PGAL1/PGAL2	SETTING (dB)
0x00	+30
0x01	+28
0x02	+26
0x03	+24
0x04	+22
0x05	+20
0x06	+18
0x07	+16
0x08	+14
0x09	+12
0x0A	+10
0x0B	+8
0x0C	+6
0x0D	+4
0x0E	+2
0x0F	0
0x10	-2

PGAL1/PGAL2	SETTING (dB)
0x11	-4
0x12	-6
0x13	-8
0x14	-10
0x15	-12
0x16	-14
0x17	-16
0x18	-18
0x19	-20
0x1A	-22
0x1B	-24
0x1C	-26
0x1D	-28
0x1E	-30
0x1F	-32
—	—

Table 26. Microphone Input Gain Bit Descriptions

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x10	0	0	PALEN	PGAML				
0x11	0	0	PAREN	PGAMR				

Programmable-Gain Adjustment for Microphone Sources (PGAML/PGAMR)

PGAML/PGAMR configures the programmable-gain adjustment setting for the microphone left/microphone right input. Code 0x00 is maximum gain while 0x1F is maximum attenuation. Table 27 lists the gain setting for each code.

Microphone Preamplifier Enable (PALEN/PAREN)

1 = Additional +20dB of gain applied to microphone inputs by the preamplifier

0 = 0dB of gain applied by the microphone preamplifier

Preamplifier gain adds to the gain set by PGAML/PGAMR. See the *Microphone Amplifiers* section.

Table 27. Microphone Input Gain Control Settings

PGAML/PGAMR	SETTING (dB)
0x00	+20
0x01	+19
0x02	+18
0x03	+17
0x04	+16
0x05	+15
0x06	+14
0x07	+13
0x08	+12
0x09	+11
0x0A	+10
0x0B	+9
0x0C	+8
0x0D	+7
0x0E	+6
0x0F	+5
0x10	+4
0x11	+3
0x12	+2
0x13	+1
0x14–0x1F	+0

Microphone Control Register (0x12)

Table 28. Microphone Control Bit Settings

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x12	0	0	0	0	MMIC	MEXT	RBEN	RBIAS

Microphone Mute (MMIC)

1 = Mute all microphone inputs.

0 = Mute disabled.

External Microphone Mode (MEXT)

1 = External microphone inputs.

0 = Internal microphone inputs.

Resistor Bias Enable (RBEN)

1 = Internal bias resistors for EXTMICBIASL and EXTMICBIASR connected.

0 = Internal bias resistors disconnected.

Microphone Bias Output Impedance Select (RBIAS)

1 = 470Ω.

0 = 2.2kΩ.

Select 2.2kΩ when using electret or amplified microphones. Select 470Ω when using an external RC filter near the headset jack.

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Table 29. Sidetone Gain Bit Descriptions

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x13	0	0	0	PGAS				

Sidetone Volume Control (PGAS)

PGAS configures the volume of the sidetone signal that feeds into the audio output mixer. As the sidetone signal is routed from the left microphone input, this volume control is in addition to the gain setting of the left microphone input. Code 0x00 is maximum gain while 0x1F is maximum attenuation. Table 30 lists the gain setting for each code.

Table 30. Sidetone Volume Control Settings

PGAS	SETTING (dB)
0x00	+30
0x01	+28
0x02	+26
0x03	+24
0x04	+22
0x05	+20
0x06	+18
0x07	+16
0x08	+14
0x09	+12
0x0A	+10
0x0B	+8
0x0C	+6
0x0D	+4
0x0E	+2
0x0F	0

PGAS	SETTING (dB)
0x10	-2
0x11	-4
0x12	-6
0x13	-8
0x14	-10
0x15	-12
0x16	-14
0x17	-16
0x18	-18
0x19	-20
0x1A	-22
0x1B	-24
0x1C	-26
0x1D	-28
0x1E	-30
0x1F	-32

Table 31. Headphone/Receiver Gain Bit Descriptions

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x14	0	HRMUT	HRVOLL					
0x15	0	0	HRVOLR					

Left and Right Headphone/Receiver Volume Control (HRVOLL/HRVOLR)

HRVOLL/HRVOLR configure the volume of the left/right headphone output. HRVOLL and HRVOLR also control the volume of the receiver output as the receiver signal is a mono mix of both the left and the right headphone signals. Code 0x00 is maximum gain while 0x3F is full attenuation. Table 32 lists the gain setting for each code.

Table 32. Headphone/Receiver Volume Control Settings

HRVOLL/HRVOLR	SETTING (dB)
0x00	+5.5
0x01	+5.0
0x02	+4.5
0x03	+4.0
0x04	+3.5
0x05	+3.0
0x06	+2.5
0x07	+2.0
0x08	+1.0
0x09	0
0x0A	-1.0
0x0B	-2.0
0x0C	-4.0
0x0D	-6.0
0x0E	-8.0
0x0F	-10.0
0x10	-12.0
0x11	-14.0
0x12	-16.0
0x13	-18.0
0x14	-20.0
0x15	-22.0
0x16	-24.0
0x17	-26.0
0x18	-28.0
0x19	-30.0
0x1A	-32.0
0x1B	-34.0
0x1C	-36.0
0x1D	-38.0
0x1E	-40.0
0x1F	-42.0
0x20	-46.0
0x21	-50.0
0x22	-54.0
0x23	-58.0
0x24	-62.0
0x25	-66.0
0x26	-70.0
0x27	-74.0
0x28 to 0x3F	Mute
—	—

Headphone Mute (HRMUT)

1 = Headphone/receiver output muted.

0 = Headphone/receiver output level set by the volume control bits.

Table 33. Speaker/Line Out Gain Bit Descriptions

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x16	0	SPMUT[1] LOMUT[2]	SPVOLL[1] LOPGAL[2]					
0x17	0	0	SPVOLR[1] LOPGAR[2]					

[1]MAX9851. [2]MAX9853

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MAX9851: Left and Right Class D Volume Control (SPVOLL/SPVOLR)

SPVOLL/SPVOLR configure the output volume of the MAX9851 left/right Class D speaker amplifier. Code 0x00 is maximum gain while 0x3F is full attenuation. Table 34 lists the gain setting for each code.

Table 34. Speaker Volume Control Settings

SPVOLL/SPVOLR	SETTING (dB)
0x00	+13.1
0x01	+12.6
0x02	+12.1
0x03	+11.6
0x04	+11.1
0x05	+10.6
0x06	+10.1
0x07	+9.6
0x08	+8.6
0x09	+7.6
0x0A	+6.6
0x0B	+5.6
0x0C	+3.6
0x0D	+1.6
0x0E	-0.4
0x0F	-2.4
0x10	-4.4
0x11	-6.4
0x12	-8.4
0x13	-10.4
0x14	-12.4
0x15	-14.4
0x16	-16.4
0x17	-18.4
0x18	-20.4
0x19	-22.4
0x1A	-24.4
0x1B	-26.4
0x1C	-28.4
0x1D	-30.4
0x1E	-32.4
0x1F	-34.4
0x20	-38.4
0x21	-42.4
0x22	-46.4
0x23	-50.4
0x24	-54.4
0x25	-58.4
0x26	-62.4
0x27	-66.4
0x28 to 0x3F	Mute
—	—

MAX9853: Left and Right Line Output Volume Control (LOPGAL/LOPGAR)

LOPGAL/LOPGAR configures the output volume of the MAX9853 left/right differential line outputs. Code 0x00 is maximum gain while 0x3F is full attenuation. Table 35 lists the gain setting for each code.

MAX9851: Speaker Output Mute (SPMUT)

1 = Speaker output muted.

0 = Speaker set by the volume control bits.

MAX9853: Line Output Mute (LOMUT)

1 = Line output muted.

0 = Line output set by the volume control bits.

Table 35. Line Output Volume Control Settings

LOPGAL/LOPGAR	SETTING (dB)
0x00	+7.1
0x01	+6.6
0x02	+6.1
0x03	+5.6
0x04	+5.1
0x05	+4.6
0x06	+4.1
0x07	+3.6
0x08	+2.6
0x09	+1.6
0x0A	+0.6
0x0B	-0.4
0x0C	-2.4
0x0D	-4.4
0x0E	-6.4
0x0F	-8.4
0x10	-10.4
0x11	-12.4
0x12	-14.4
0x13	-16.4
0x14	-18.4

LOPGAL/LOPGAR	SETTING (dB)
0x15	-20.4
0x16	-22.4
0x17	-24.4
0x18	-26.4
0x19	-28.4
0x1A	-30.4
0x1B	-32.4
0x1C	-34.4
0x1D	-36.4
0x1E	-38.4
0x1F	-40.4
0x20	-44.4
0x21	-48.4
0x22	-52.4
0x23	-56.4
0x24	-60.4
0x25	-64.4
0x26	-68.4
0x27	-72.4
0x28 to 0x3F	Mute
—	—

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Audio Output Control Register (0x18)

Table 36. Audio Output Bit Descriptions

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x18	0	VSEN	ZDEN	SPMODE[1] LOMODE[2]		HRMODE		

[1]*MAX9851*, [2]*MAX9853*

Volume Adjustment Smoothing (VSEN)

1 = Volume changes smoothed by stepping through intermediate values.

0 = Volume changes made by bypassing intermediate settings.

Zero-Crossing Detection (ZDEN)

1 = Volume changes made only at zero crossings in the audio waveform or after approximately 100ms.
0 = Volume changes made immediately upon request.

MAX9851: Speaker Output Mode (SPMODE)

00 = Speaker amplifiers shutdown.

01 = Right channel enabled only.

10 = Left channel enabled only.

11 = Stereo speaker output enabled.

MAX9853: Line Output Mode (LOMODE)

00 = Line outputs disabled and SHDNOUT high.

11 = Line outputs enabled and SHDNOUT low.

Headphone and Receiver Output Mode (HRMODE)

000 = Headphone and receiver amplifiers shutdown.

001 to 011 = Reserved.

100 = Stereo headphone mode.

101 = Single-ended mono headphone mode (L+R).

110 = Balanced mono headphone mode (bridge-tied load output L+R).

111 = Receiver amplifier enabled (L+R).

HRMODE selects between headphone amplifier and receiver amplifier modes. The headphone amplifier and receiver amplifier cannot be enabled at the same time. To minimize click/pop, HRMODE should be programmed after power-on sequence and AOK = 1 (register 0x01, bit B7).

Vibe Gain and Headset Autodetect Register (0x19)

Table 37. Vibe and Headset Autodetect Bit Descriptions

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x19	TGAIN				ENA	SLEEP	HSTEST	

Transducer/Vibe Gain (TGAIN)

TGAIN selects the programmable-gain setting of the $\overline{VIBE}$ signal data when signal conditioning is enabled. Table 38 lists the gain setting for each code.

Table 38. Transducer DAC Gain Settings

TGAIN	T-DAC $\overline{VIBE}$ SIGNAL INPUT PGA
0x0	Disabled, PGA output = 0
0x1	Reserved
0x2	Reserved
0x3	-30dB
0x4	-24dB
0x5	-18dB
0x6	-12dB
0x7	-6dB
0x8	0dB
0x9	+6dB
0xA	+12dB
0xB	+18dB
0xC	+24dB
0xD	+30dB
0xE	Reserved
0xF	Reserved

Headset Detect Enable (ENA)

1 = Enabled.

0 = Disabled.

ENA = 1 enables the headphone sense biases and powers on the threshold comparator circuitry. Headphone amplifiers must be disabled and microphone amplifiers and bias resistors must be enabled for proper headset detection. ENA = 0 powers down the circuitry and sets HSDET (register 0x01, bits B5–B0) to 0x00.

Headset Detect Low-Power Mode (SLEEP)

1 = Enabled.

0 = Disabled.

SLEEP = 1 places the detection circuitry in low-power mode and disables normal detect mode. This feature is most useful when operating the MAX9851/MAX9853 in low-power shutdown mode. EXTMICBIASL is monitored and a hardware interrupt is triggered when a load is detected. Exit sleep mode to clear the hardware interrupt.

Sleep mode is automatically entered when AV_{DD} is removed and the battery voltage (PV_{DD}) is still present. See the *Headset Detect* section.

Headset Detect Configuration (HSTEST)

00 = Headphone sense bias disconnected.

01 = Headphone sense test 1 (standard headphone detection).

10 = Headphone sense test 2 (balanced mono headphone detection).

11 = Reserved.

Set HRMODE = 000 prior to headset detection to disable the headphone amplifiers.

System Control Register (0x1A)

Table 39. System Bit Descriptions

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x1A	$\overline{SHDN}$	HFEN	LFEN	CPEN	0	1	0	CPCLK

Shutdown ($\overline{SHDN}$)

1 = MAX9851/MAX9853 operational.

0 = Complete shutdown.

$\overline{SDALL}$ is an active-low shutdown bit that overrides all settings and places the entire MAX9851/MAX9853 in low-power shutdown.

Clock Input Enable (HFEN)

1 = Enable.

0 = Disable.

HFEN = 1 enables the MCLK input and allows all clock dependent circuitry to operate.

Analog Low-Frequency Oscillator Enable (LFEN)

1 = Enable.

0 = Disable.

LFEN = 1 enables the analog internal low-frequency oscillator that is used by the charge pump when MCLK is disabled.

Charge-Pump Enable (CPEN)

1 = Enable.

0 = Disable.

Always program to 1 for proper operation.

Charge-Pump Oscillator Select (CPCLK)

1 = Charge-pump oscillator derived from MCLK.

0 = Charge-pump oscillator derived from internal oscillator.

CPCLK = 1 configures the charge pump to use MCLK as a clock source. CPCLK = 0 configures the internal oscillator to be used instead of the MCLK. **CPCLK must bet set to 1 when the Class D amplifier is being used (MAX9851 only).**

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Table 40. Shutdown Bit Descriptions (0x1B)

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x1B	DACLEN	DACREN	ADCLEN	ADCREN	DATEN	0	MICLEN	MICREN

Left and Right DAC Enable (DACLEN/DACREN)

1 = Enable.

0 = Disable.

Enable and disable the DACs only when S1SDI and S2SDI (register 0x03 and 0x05, bit B6) are cleared and all soft-stop sequences have completed (indicated by the SLD bit in resister 0x00) to insure proper click-and-pop suppression. Disable DACLEN/DACREN before making interface mode changes.

Left and Right ADC Enable (ADCLEN/ADCREN)

1 = Enable.

0 = Disable.

Disable ADCLEN/ADCREN before making interface mode changes.

Transducer/Vibe DAC Enable (DATEN)

1 = Enable.

0 = Disable.

$\overline{VIBE}$ goes to high impedance when the DATEN is disabled.

Left and Right Microphone Enable (MICLEN/MICREN)

1 = Enable.

0 = Disable.

I²C Serial Interface

The MAX9851/MAX9853 feature an I²C/SMBus™-compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the MAX9851/MAX9853 and the master at clock rates up to 400kHz. Figure 10 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. A master device writes data to the MAX9851/MAX9853 by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX9851/MAX9853 is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX9851/MAX9853 transmits the proper slave address followed by a series of nine SCL pulses. The MAX9851/MAX9853 transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or REPEATED START condition, a not acknowledge, and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on the SDA bus. SCL operates as only an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX9851/MAX9853 from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

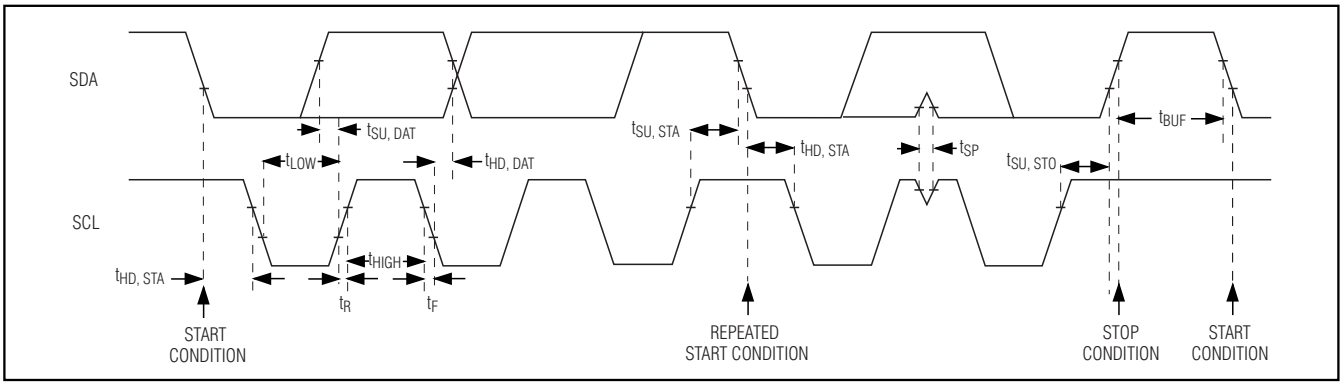


Figure 10. 2-Wire Interface Timing Diagram

SMBus is a trademark of Intel Corp.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section). SDA and SCL idle high when the I²C bus is not busy.

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 11). A START condition from the master signals the beginning of a transmission to the MAX9851/MAX9853. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

Early STOP Conditions

The MAX9851/MAX9853 recognize a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

The MAX9851/MAX9853 are preprogrammed with a slave address of 0x20 or 0010000. The address is defined as the 7 most significant bits (MSBs) followed by the read/write bit. Set the read/write bit to 1 to configure the MAX9851/MAX9853 to read mode. Set the read/write bit to 0 to configure the MAX9851/MAX9853 to write mode. The address is the first byte of information sent to the MAX9851/MAX9853 after the START condition.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX9851/MAX9853 use to handshake receipt each byte of data when in write mode (see Figure 12). The MAX9851/MAX9853 pull down SDA during the entire master-generated ninth clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master may retry communication.

The master pulls down SDA during the ninth clock cycle to acknowledge receipt of data when the MAX9851/MAX9853 are in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not acknowledge is sent when the master reads the final byte of data from the MAX9851/MAX9853, followed by a STOP condition.

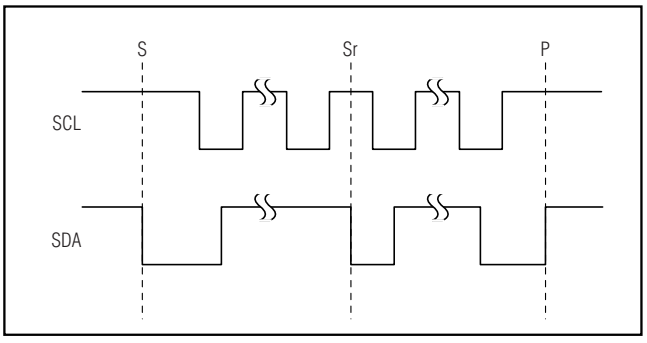


Figure 11. START, STOP, and REPEATED START Conditions

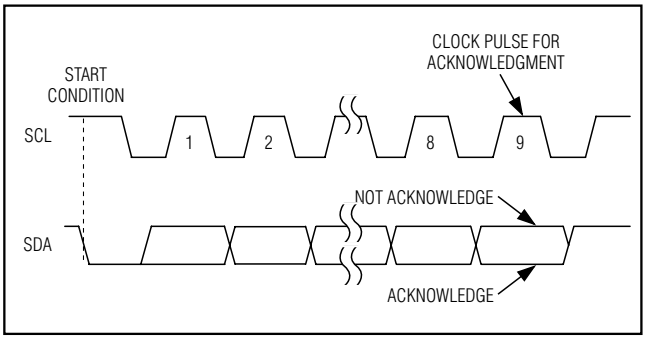


Figure 12. Acknowledge

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Write Data Format

A write to the MAX9851/MAX9853 includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0, one byte of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition. Figure 13 illustrates the proper frame format for writing one byte of data to the MAX9851/MAX9853. Figure 14 illustrates the frame format for writing n-bytes of data to the MAX9851/MAX9853.

The slave address with the R/$\overline{W}$ bit set to 0 indicates that the master intends to write data to the MAX9851/MAX9853. The MAX9851/MAX9853 acknowledge receipt of the address byte during the master-generated ninth SCL pulse.

The second byte transmitted from the master configures the MAX9851/MAX9853's internal register address pointer. The pointer tells the MAX9851/MAX9853 where to write the next byte of data. An acknowledge pulse is sent by the MAX9851/MAX9853 upon receipt of the address pointer data.

The third byte sent to the MAX9851/MAX9853 contains the data that will be written to the chosen register. An acknowledge pulse from the MAX9851/MAX9853 signals receipt of the data byte. The address pointer auto increments to the next register address after each received data byte. This autoincrement feature allows a master to write to sequential registers within one continuous frame. Figure 14 illustrates how to write to multiple registers with one frame. The master signals the end of transmission by issuing a STOP condition.

Register addresses greater than 0x1B are reserved. Do not write to these addresses.

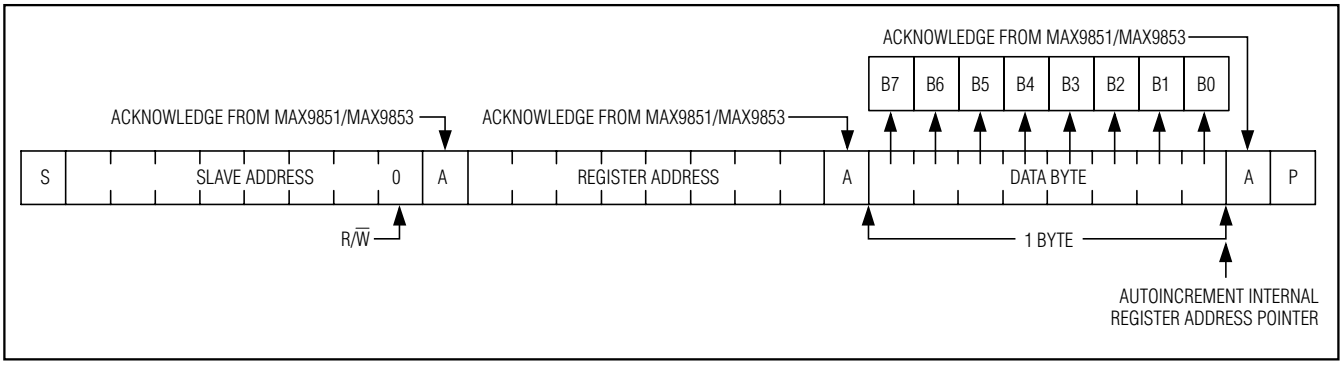


Figure 13. Writing 1 Byte of Data to the MAX9851/MAX9853

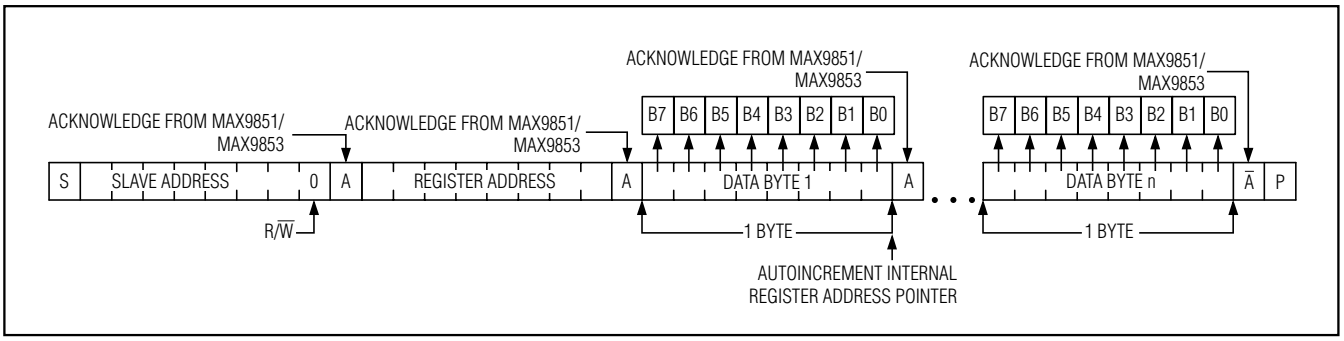


Figure 14. Writing n-Bytes of Data to the MAX9851/MAX9853

Read Data Format

Send the slave address with the R/$\overline{W}$ bit set to 1 to initiate a read operation. The MAX9851/MAX9853 acknowledge receipt of its slave address by pulling SDA low during the ninth SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00. The first byte transmitted from the MAX9851/MAX9853 will be the contents of register 0x00. Transmitted data is valid on the rising edge of the master-generated serial clock (SCL). The address pointer autoincrements after each read data byte. This autoincrement feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read will be from register 0x00 and subsequent reads will autoincrement the address pointer until the next STOP condition. The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the MAX9851/MAX9853's slave address with the R/$\overline{W}$ bit set to 0 followed by the register address. A REPEATED START condition is then sent followed by the slave address with the R/$\overline{W}$ bit set to 1. The MAX9851/MAX9853 transmit the contents of the specified register. The address pointer auto-increments after transmitting the first byte. Attempting to read from register addresses higher than 0x1F results in repeated reads of 0x1F. Note that 0x1C to 0x1F are reserved registers. The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figure 15 illustrates the frame format for reading one byte from the MAX9851/MAX9853. Figure 16 illustrates the frame format for reading multiple bytes from the MAX9851/MAX9853.

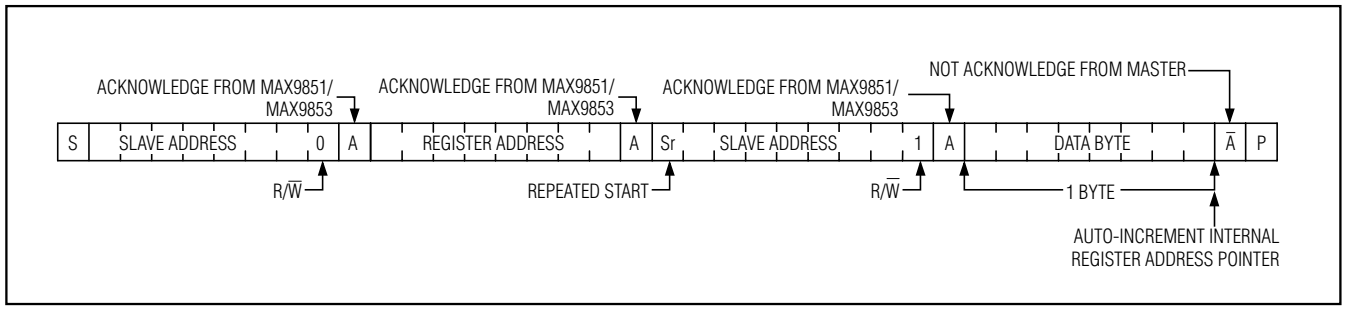


Figure 15. Reading One Indexed Byte of Data from the MAX9851/MAX9853

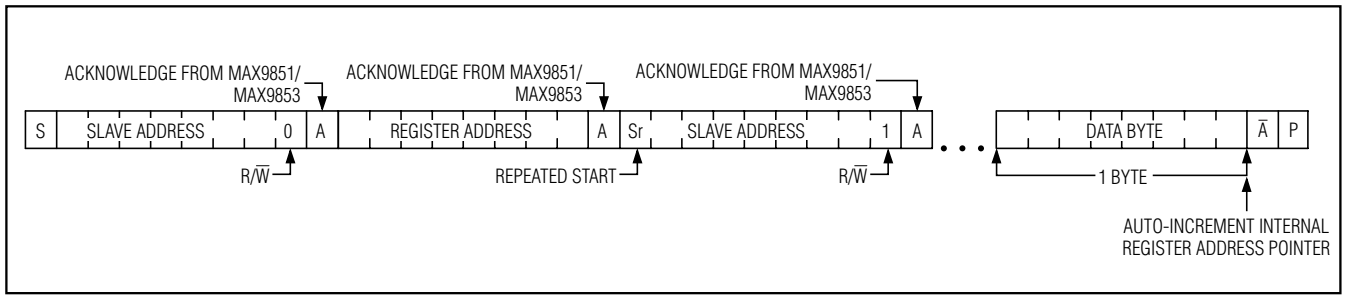


Figure 16. Reading n-Bytes of Indexed Data from the MAX9851/MAX9853

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Applications Information

Typical Operating Modes

The MAX9851/MAX9853 are capable of a wide variety of operating modes. To ease the process of determining the appropriate settings for a particular operating mode, several typical modes of operation are detailed below.

Voiceband Playback and Voiceband Record

Typical cellular phone operation requires both playback and record functions, and audio data to be sent and received with the cell-phone communications chipset. Table 41 lists an example of this configuration and Table 42 lists the corresponding register settings in the proper programming sequence.

Table 41. Example Voiceband Playback and Voiceband Record Configuration

- 13MHz MCLK
- 8kHz voice mode for incoming and outgoing data
- DAC and ADC enabled for mono data
- Digital audio input and output on the primary digital audio interface operating in slave mode
- Voice filter activated for both DAC and ADC
- Audio output on receiver amplifier
- Audio input on internal microphone input

Table 42. I²C Register Settings for Voiceband Playback and Record Voiceband Mode

REGISTER (hex)	VALUE (hex)	DESCRIPTION
0x00	N/A	Read-only status register
0x01	N/A	Read-only status register
0x02	0x00	No interrupts are enabled
Program 0x03 last for proper soft-start		
0x04	0x00	Configure for slave mode
0x05	0x00	Disable secondary digital audio interface
0x06	0x00	No configuration necessary
0x07	0x30	Configure for a 13MHz MCLK and voiceband filtering on both the ADC and DAC
0x08	0x20	Route digital audio from the primary interface to the left DAC
0x09	0x00	No configuration necessary
0x0A	0x20	Route the left microphone signal to the ADC
0x0B	0x90	Route the left DAC output to the receiver amplifier and enabled sidetone
0x0C	0x00	No configuration necessary
0x0D	0x00	No configuration necessary
0x0E	0x00	No configuration necessary
0x0F	0x00	No configuration necessary
0x10	0x00	Configure the left microphone input for +20dB of gain, adjust as appropriate
0x11	0x00	No configuration necessary
0x12	0x00	Select the internal microphone interface and disable external microphone bias circuitry
0x13	0x00	Sidetone PGA, adjust as necessary
0x14	0x14	Configure left output gain to -20dB, adjust as necessary

Table 42. I²C Register Settings for Voiceband Playback and Record Voiceband Mode (continued)

REGISTER (hex)	VALUE (hex)	DESCRIPTION
0x15	0x00	No configuration necessary
0x16	0x00	No configuration necessary
0x17	0x00	No configuration necessary
0x18	0x67	Enable volume smoothing and zero-crossing detection and select the receiver amplifier for output
0x19	0x00	No configuration necessary
0x1A	0xD5	Enable the MAX9851/MAX9853 and configure the charge-pump circuitry to run from MCLK
0x1B	0xA2	Enable the left DAC, left ADC, and microphone interface
0x03	0xCA	Enable primary digital audio interface and configure for full-duplex operation at 8kHz voice mode

Stereo Audio Playback with the MAX9851 Speaker Amplifier

Typical operation often requires audio playback of a digital source. Table 43 lists an example of this configuration and Table 44 lists the corresponding register settings in the proper programming sequence.

An example configuration is to supply I²S stereo digital audio sampled at 48kHz to the secondary digital audio interface (S2). The audio is converted to analog and amplified by the speaker amplifiers of the MAX9851. This configuration will be set to run from a 13MHz MCLK and operate the MAX9851 as the digital audio master.

Table 43. Example Stereo Audio Playback Configuration

- 13MHz MCLK
- 48kHz sample rate for incoming data
- DAC enabled for stereo data
- Digital audio input on the secondary digital audio interface operating in master mode
- Audio output on the speaker amplifier

Table 44. I²C Register Settings for Stereo Audio Playback Mode

REGISTER (hex)	VALUE (hex)	DESCRIPTION
0x00	—	Read-only status register
0x01	—	Read-only status register
0x02	0x00	No interrupts are enabled
0x03	0x00	Disable primary digital audio interface
0x04	0x00	No configuration necessary
Program 0x05 last for proper soft-start		
0x06	0x88	Configure for master mode and I²S data format
0x07	0x00	Configure for a 13MHz MCLK
0x08	0x84	Route digital audio from the secondary interface to the DAC
0x09	0x00	No configuration necessary
0x0A	0x00	No configuration necessary
0x0B	0x11	Route the DAC output to the speaker amplifier
0x0C	0x00	No configuration necessary
0x0D	0x00	No configuration necessary
0x0E	0x00	No configuration necessary
0x0F	0x00	No configuration necessary
0x10	0x00	No configuration necessary
0x11	0x00	No configuration necessary
0x12	0x00	No configuration necessary
0x13	0x00	No configuration necessary
0x14	0x00	No configuration necessary
0x15	0x00	No configuration necessary
0x16	0x0E	Configure left-speaker output for -0.4dB of gain, adjust as necessary
0x17	0x0E	Configure right-speaker output for -0.4dB of gain, adjust as necessary
0x18	0x78	Enable volume smoothing and zero-crossing detection and select the speaker amplifier for stereo operation
0x19	0x00	No configuration necessary
0x1A	0xD5	Enable the MAX9851/MAX9853, configure the charge-pump circuitry to run from MCLK
0x1B	0xC0	Enable the left and right DAC
0x05	0x49	Enable secondary interface to input data at 48kHz

Stereo Audio Record

To record audio samples, only the ADC and microphone interface are required. Table 45 lists an example of this configuration and Table 46 lists the corresponding register settings in the proper programming sequence.

Table 45. Example Stereo Audio Record Configuration

- 13MHz MCLK
- 48kHz sample rate for recorded data
- Output data routed through the secondary digital audio interface operating in master mode
- ADC enabled for stereo record
- Audio input on external microphone input using internal bias

Table 46. I²C Register Settings for Stereo Audio Record Mode

REGISTER (hex)	VALUE (hex)	DESCRIPTION
0x00	—	Read-only status register
0x01	—	Read-only status register
0x02	0x00	No interrupt enables are set
0x03	0x00	No configuration necessary
0x04	0x00	No configuration necessary
Program 0x05 last for proper soft-start		
0x06	0x80	Configure for master mode
0x07	0x00	Configure for a 13MHz MCLK
0x08	0x00	No configuration necessary
0x09	0x00	No configuration necessary
0x0A	0x21	Route the left and right microphone signals to the ADC
0x0B	0x00	No configuration necessary
0x0C	0x00	No configuration necessary
0x0D	0x00	No configuration necessary
0x0E	0x00	No configuration necessary
0x0F	0x00	No configuration necessary
0x10	0x00	Configure the left microphone input for +20dB of gain, adjust as appropriate
0x11	0x00	Configure the left microphone input for +20dB of gain, adjust as appropriate

Table 46. I²C Register Settings for Stereo Audio Record Mode (continued)

REGISTER (hex)	VALUE (hex)	DESCRIPTION
0x12	0x06	Select the external microphone interface and enable the external microphone bias circuitry using 2.2kΩ bias resistors.
0x13	0x00	No configuration necessary
0x14	0x00	No configuration necessary
0x15	0x00	No configuration necessary
0x16	0x00	No configuration necessary
0x17	0x00	No configuration necessary
0x18	0x00	No configuration necessary
0x19	0x00	No configuration necessary
0x1A	0xD5	Enable the MAX9851/MAX9853 and configure the charge-pump circuitry to run from MCLK (charge pump required to set AOK = 1 and allow digital circuitry to operate)
0x1B	0x33	Enable the ADC and microphone interface
0x05	0x89	Enable secondary digital audio interface and configure for output operation at 48kHz stereo audio mode

PC Board Layout and Bypassing

Proper layout and grounding are essential for optimum performance. Use large traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance. Large traces also aid in moving heat away from the package. Proper grounding improves audio performance, minimizes crosstalk between channels, and prevents any switching noise from coupling into the audio signal. Connect AGND, DGND, CPGND, and PGND (MAX9851 only) together at a single point on the PC board using the star grounding technique. Route DGND, CPGND, and all traces that carry switching transients or digital signals separately from AGND and analog audio signal paths. Ground all components associated with the charge pump to CPGND (CPV_{SS} bypassing and CPV_{DD} bypassing). Connect all digital I/O termination to DGND including DV_{DD} and DV_{DDS2} bypassing. Bypass both PV_{DD} pins on the MAX9851 (Class D power supplies) to PGND. Bypass V_{REF}, MBIAS, INTMICBIAS to a quiet analog ground (AGND).

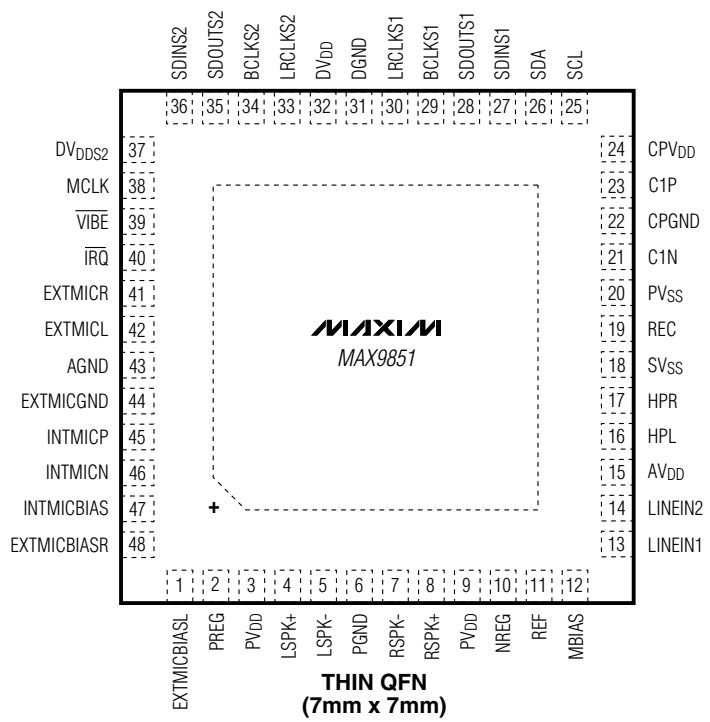
Connect PV_{SS} and SV_{SS} together at the device and place the charge-pump capacitors as close to SV_{SS} as possible. Ensure C2 is connected to CPGND and bypass CPV_{DD} with 1µF to CPGND. Place the bypass capacitors as close to the device as possible.

The MAX9851/MAX9853 thin QFN package features an exposed thermal pad on its underside. This pad lowers the package's thermal resistance by providing a direct-heat conduction path from the die to the PC board. If possible, connect the exposed thermal pad to an electrically isolated, large pad of copper. If it cannot be left floating, connect it to AGND.

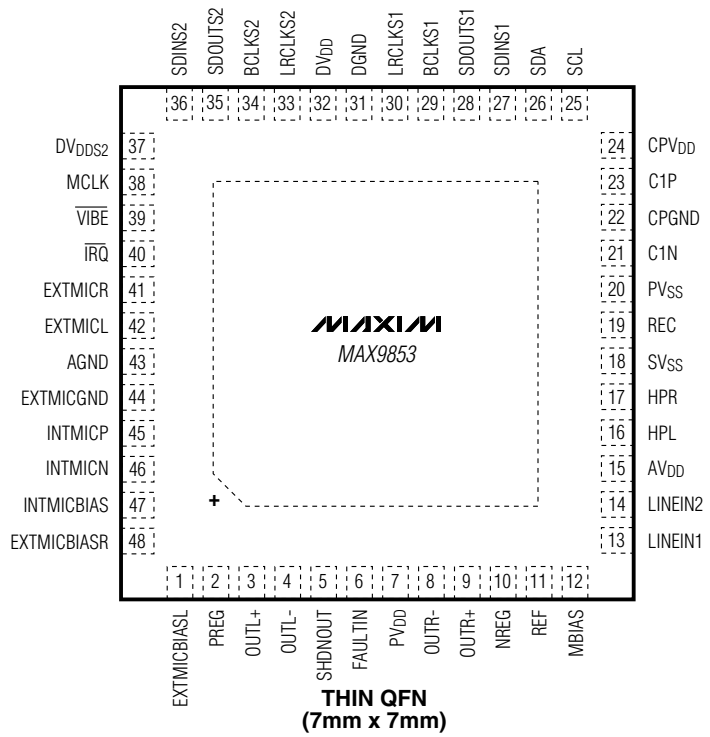
An evaluation kit (EV kit) is available to provide example layouts for the MAX9851 and MAX9853. The EV kit allows quick setup of the MAX9851/MAX9853 and includes easy-to-use software allowing all internal registers to be controlled.

Pin Configurations

TOP VIEW



THIN QFN (7mm x 7mm)



THIN QFN (7mm x 7mm)

Stereo Audio CODECs with Microphone, DirectDrive Headphones, Speaker Amplifiers, or Line Outputs

Selector Guide

PART	SPEAKER AMPLIFIERS	LINE OUTPUTS	I²C SLAVE ADDRESS
MAX9851ETM	√	—	0x20
MAX9853ETM	—	√	0x20

Chip Information

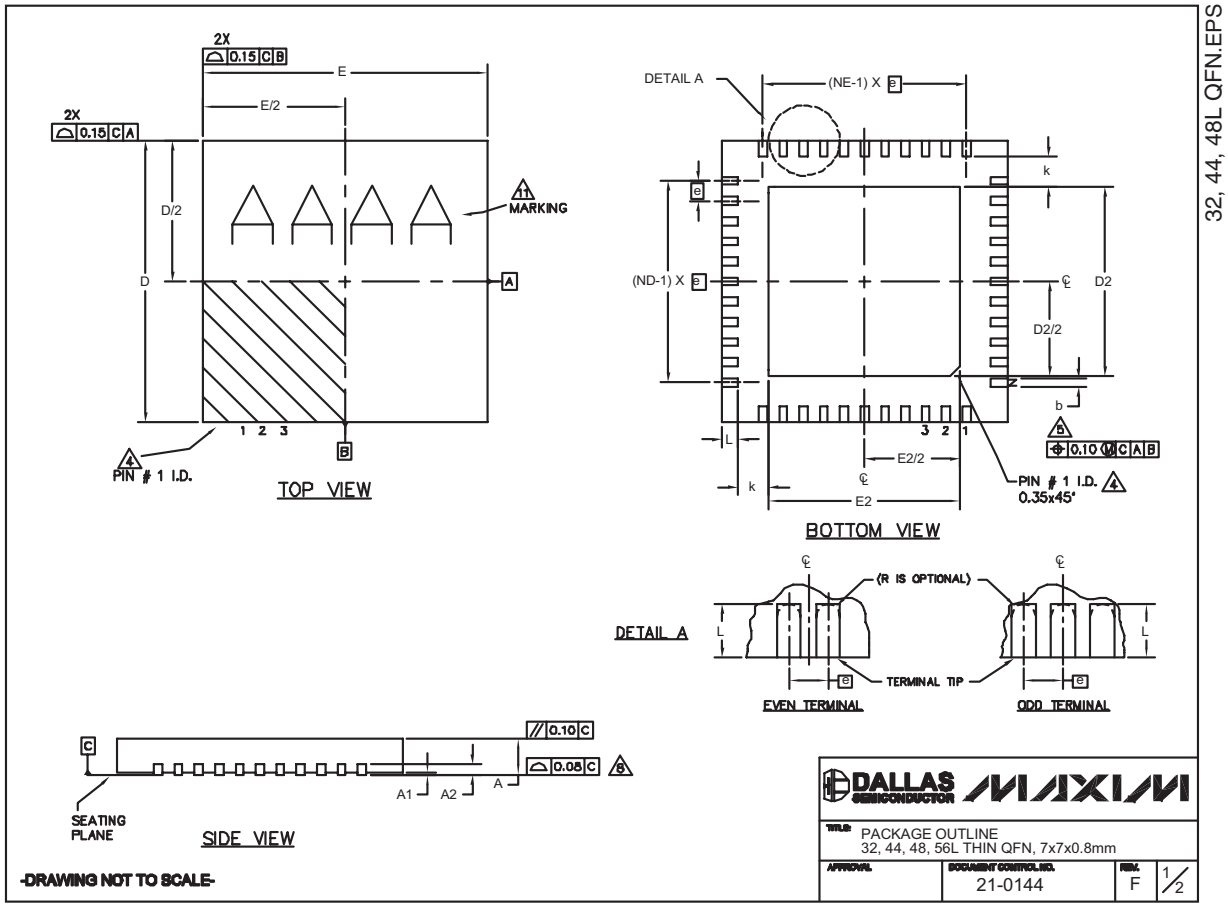
MAX9851 TRANSISTOR COUNT: 348,122

MAX9853 TRANSISTOR COUNT: 345,688

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Stereo Audio CODECs with Microphone, DirectDrive Headphones, Speaker Amplifiers, or Line Outputs

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7			56L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65	0.30	0.40	0.50
N	32			44			48			44			56		
ND	8			11			12			10			14		
NE	8			11			12			12			14		

EXPOSED PAD VARIATIONS

PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3277-2	–	4.55	4.70	4.85	4.55	4.70	4.85	–
T3277-3	–	4.55	4.70	4.85	4.55	4.70	4.85	–
T4477-2	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4477-3	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4877-1**	13,24,37,48	4.20	4.30	4.40	4.20	4.30	4.40	–
T4877-3	–	4.95	5.10	5.25	4.95	5.10	5.25	–
T4877-4	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877-5	–	2.40	2.50	2.60	2.40	2.50	2.60	–
T4877-6	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877-7	–	4.95	5.10	5.25	4.95	5.10	5.25	–
T4877M-1	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877M-6	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877MN-8	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T5677-1	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T5677-2	–	5.40	5.50	5.60	5.40	5.50	5.60	–

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED. TOTAL NUMBER OF LEADS ARE 44.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 EXCEPT THE EXPOSED PAD DIMENSIONS OF T4877-1/-3/-4/-5/-6 & T5677-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE 32, 44, 48, 56L THIN QFN, 7x7x0.8mm

APPROVAL | DOCUMENT CONTROL NO. 21-0144 | REV. F | 2/2

MAX9851/MAX9853 Package Code: T4877-3

Revision History

Pages changed at Rev 1: 1, 2, 3–25, 30, 68, 71

Pages changed at Rev 2: 1, 60, 63, 69, 71

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