19-2084; Rev 0; 7/01

MAXIM

Tracking/Sequencing Triple/Quintuple Power-Supply Controllers

General Description

The MAX1964/MAX1965 power-supply controllers are designed to address cost-sensitive applications demanding voltage sequencing/tracking, such as cable modem consumer premise equipment (CPE), xDSL CPE, and set-top boxes. Operating off a low-cost, unregulated DC supply (such as a wall adapter output), the MAX1964 generates three positive outputs and the MAX1965 generates four positive outputs and one negative output to provide an inexpensive system power supply.

The MAX1964 includes a current-mode synchronous step-down controller and two positive regulator gain blocks. The MAX1965 has one additional positive gain block and one negative regulator gain block. The main synchronous step-down controller generates a high-current output that is preset to 3.3V or adjustable from 1.236V to 0.75 × V_{IN} with an external resistive-divider. The 200kHz operating frequency allows the use of low-cost aluminum-electrolytic capacitors and low-cost power magnetics. Additionally, the MAX1964/MAX1965 step-down controllers sense the voltage across the low-side MOSFET's on-resistance to efficiently provide the current-limit signal, eliminating the need for costly current-sense resistors.

The MAX1964/MAX1965 generate additional supply rails at low cost. The positive regulator gain blocks use an external PNP pass transistor to generate low voltage rails directly from the main step-down converter (such as 2.5V or 1.8V from the main 3.3V output) or higher voltages using coupled windings from the step-down converter (such as 5V, 12V, or 15V). The MAX1965's negative gain block uses an external NPN pass transistor in conjunction with a coupled winding to generate -5V, -12V, or -15V.

All output voltages are externally adjustable, providing maximum flexibility. During startup, the MAX1964 features voltage sequencing and the MAX1965 features voltage tracking. Both controllers provide a power-good output that monitors all of the output voltages.

Applications

xDSL, Cable, and ISDN Modems

Set-Top Boxes

Wireless Local Loop

Typical Operating Circuit appears at end of data sheet.

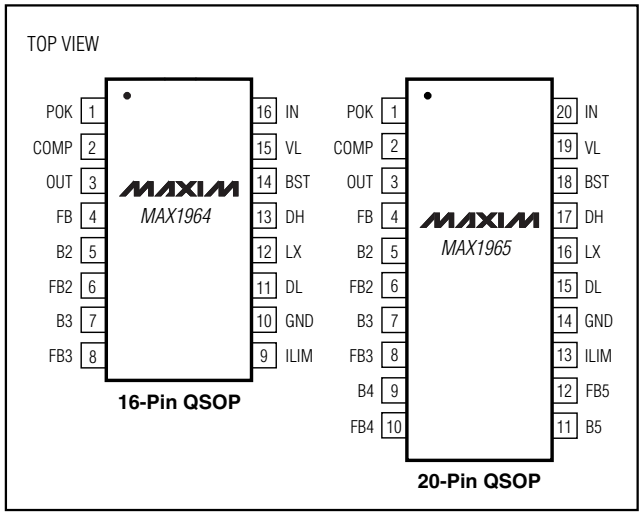
Features

- **4.5V to 28V Input Voltage Range**
- **Master DC-DC Step-Down Converter:**
  - **Preset 3.3V or Adjustable (1.236V to 0.75 x V_{IN}) Output Voltage**
  - **Fixed Frequency (200kHz) PWM Controller**
  - **No Current-Sense Resistor**
  - **Adjustable Current Limit**
  - **95% Efficient**
  - **Soft-Start**
- **Two (MAX1964)/Four (MAX1965) Analog Gain Blocks:**
  - **Positive Analog Blocks Drive Low-Cost PNP Pass Transistors to Build Positive Linear Regulators**
  - **Negative Analog Block (MAX1965) Drives a Low-Cost NPN Pass Transistor to Build a Negative Linear Regulator**
- **Power-Good Indicator**
- **Voltage Sequencing (MAX1964) or Tracking (MAX1965)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	f_{OSC} (kHz)
MAX1964TEEE	-40°C to +85°C	16 QSOP	200
MAX1965TEEP	-40°C to +85°C	20 QSOP	200

Pin Configurations



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Tracking/Sequencing Triple/Quintuple Power-Supply Controllers

ABSOLUTE MAXIMUM RATINGS

IN, B2, B3, B4 to GND .....-0.3V to +30V
B5 to OUT .....-20V to +0.3V
VL, POK, FB, FB2, FB3, FB4, FB5 to GND .....-0.3V to +6V
LX to BST .....-6V to +0.3V
BST to GND .....-0.3V to +36V
DH to LX .....-0.3V to (V_{BST} + 0.3V)
DL, OUT, COMP, ILIM to GND .....-0.3V to (V_L + 0.3V)
VL Output Current 50mA
VL Short Circuit to GND .....≤ 100ms

Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C) 666mW
20-Pin QSOP (derate 9.1mW/°C above +70°C) 727mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, ILIM = FB = GND, V_{BST} - V_{LX} = 5V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL							
Operating Input Voltage Range (Note 1)	V_{IN}			4.5		28	V
Quiescent Supply Current	I_{IN}	V_{FB} = 0, V_{OUT} = 4V, V_{FB2} = V_{FB3} = V_{FB4} = 1.5V, V_{FB5} = -0.1V	MAX1964		1.25	2.5	mA
			MAX1965		1.5	3.0	
VL REGULATOR							
Output Voltage	VL	6V < V_{IN} < 28V, 0.1mA < I_{LOAD} <20mA		4.75	5.00	5.25	V
Line Regulation		V_{IN} = 6V to 28V				3.0	%
Undervoltage Lockout Trip Level	V_{UVLO}	VL rising, 3% hysteresis (typ)		3.2	3.5	3.8	V
Minimum Bypass Capacitance	$C_{BYP(MIN)}$	10mΩ < ESR < 500mΩ			1		µF
DC-DC CONTROLLER							
Output Voltage (Preset Mode)	V_{OUT}	FB = GND		3.272	3.34	3.355	V
Typical Output Voltage Range (Adjustable Mode) (Note 2)	V_{OUT}			V_{SET}		0.75 × V_{IN}	V
FB Set Voltage (Adjustable Mode)	V_{SET}	FB = COMP		1.221	1.236	1.252	V
FB Dual-Mode™ Threshold				50	100	150	mV
FB Input Leakage Current	I_{FB}	V_{FB} = 1.5V			0.01	100	nA
FB to COMP Transconductance	g_m	FB = COMP, I_{COMP} = ±5µA		70	100	140	µS
Current-Sense Amplifier Voltage Gain	A_{LIM}	V_{IN} - V_{LX} = 250mV		4.46	4.9	5.44	V/V
Current-Limit Threshold (Internal Mode)	V_{VALLEY}	V_{ILIM} = 5.0V		190	250	310	mV
Current-Limit Threshold (External Mode)	V_{VALLEY}	V_{ILIM} = 2.5V		440	530	620	mV
Switching Frequency	f_{OSC}			160	200	240	kHz

Dual Mode is a trademark of Maxim Integrated Products, Inc.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, ILIM = FB = GND, V_{BST} - V_{LX} = 5V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Duty Cycle	D_{MAX}		77	82	90	%
Soft-Start Period	t_{SOFT}			1024		$1/f_{OSC}$
Soft-Start Step Size				$V_{REF}/64$		V
FB Power-Up Sequence Threshold		MAX1964, FB rising, B2 turns on		1.145		V
DH Output Low Voltage		I_{SINK} = 10mA, measured from DH to LX			40	mV
DH Output High Voltage		I_{SOURCE} = 10mA, measured from BST to DH	40			mV
DL Output Low Voltage		I_{SINK} = 10mA, measured from DL to GND			20	mV
DL Output High Voltage		I_{SOURCE} = 10mA, measured from DL to GND	VL - 0.1			V
DH On-Resistance		High (DH to BST) and low (DH to LX)		1.5	4	Ω
DL On-Resistance		High (DL to VL)		4.3	10	Ω
		Low (DL to GND)		0.7	2	
Output Drive Current		Sourcing or sinking, V_{DH} or V_{DL} = VL/2		0.5		A
LX, BST Leakage Current		V_{BST} = V_{LX} = V_{IN} = 28V, V_{FB} = 1.5V		0.04	10	µA
POSITIVE ANALOG GAIN BLOCKS						
FB2, FB3, FB4 Regulation Voltage		V_{B2} = V_{B3} = V_{B4} = 5V, I_{B2} = I_{B3} = I_{B4} = 1mA (sink)	1.226	1.24	1.257	V
FB2 Power-Up Sequence Threshold		MAX1964, FB2 rising, B3 turns on		1.145		V
FB2, FB3, FB4 to B_ Transconductance Error	$\Delta V_{FB_}$	V_{B2} = V_{B3} = V_{B4} = 5V, I_{B2} = I_{B3} = I_{B4} = 0.5mA to 5mA (sink)		13	22	mV
Feedback Input Leakage Current	$I_{FB_}$	V_{FB2} = V_{FB3} = V_{FB4} = 1.5V		0.01	100	nA
Driver Sink Current	$I_{B_}$	V_{FB2} = V_{FB3} = V_{FB4} = 1.188V; V_{B2} = V_{B3} = V_{B4} = 2.5V	10	21		mA
		V_{FB2} = V_{FB3} = V_{FB4} = 1.188V; V_{B2} = V_{B3} = V_{B4} = 4.0V		24		
NEGATIVE ANALOG GAIN BLOCK						
FB5 Regulation Voltage		V_{B5} = V_{OUT} - 2V, V_{OUT} = 3.5V, I_{B5} = 1mA (source)	-20	-5	+10	mV
FB5 to B5 Transconductance Error	ΔV_{FB5}	V_{B5} = 0, I_{B5} = 0.5mA to 5mA (source)		-13	-20	mV
Feedback Input Leakage Current	I_{FB5}	V_{FB5} = -100mV		0.01	100	nA
Driver Source Current	I_{B5}	V_{FB5} = 200mV, V_{B5} = V_{OUT} - 2.0V, V_{OUT} = 3.5V	10	25		mA
POWER GOOD (POK)						
OUT Trip Level (Preset Mode)		FB = GND, falling edge, 3% hysteresis (typ)	2.88	3.0	3.12	V
FB Trip Level (Adjustable Mode)		Falling edge, 3% hysteresis (typ)	1.070	1.114	1.159	V
FB2, FB3, FB4 Trip Level		Falling edge, 3% hysteresis (typ)	1.070	1.114	1.159	V
FB5 Trip Level		Rising edge, 35mV hysteresis (typ)	368	530	632	mV
POK Output Low Level		I_{SINK} = 1mA			0.4	V
POK Output High Leakage		V_{POK} = 5V			1	µA

Tracking/Sequencing Triple/Quintuple Power-Supply Controllers

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, ILIM = FB = GND, V_{BST} - V_{LX} = 5V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THERMAL PROTECTION (NOTE 3)						
Thermal Shutdown		Rising temperature		160		°C
Thermal Shutdown Hysteresis				15		°C

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, ILIM = FB = GND, V_{BST} - V_{LX} = 5V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL							
Operating Input Voltage Range (Note 1)	V_{IN}			4.5		28	V
Quiescent Supply Current	I_{IN}	V_{FB} = 0, V_{OUT} = 4V, V_{FB2} = V_{FB3} = V_{FB4} = 1.5V, V_{FB5} = -0.1V	MAX1964			2.5	mA
			MAX1965			3.0	
VL REGULATOR							
Output Voltage	VL	6V < V_{IN} < 28V, 0.1mA < I_{LOAD} <20mA		4.75		5.25	V
Line Regulation		V_{IN} = 6V to 28V				3.0	%
Undervoltage Lockout Trip Level	V_{UVLO}	VL rising, 3% hysteresis (typ)		3.0		4.0	V
DC-DC CONTROLLER							
Output Voltage (Preset Mode)	V_{OUT}	FB = GND		3.247		3.38	V
Feedback Set Voltage (Adjustable Mode)	V_{SET}	FB = COMP		1.211		1.261	V
Current-Sense Amplifier Voltage Gain	A_{LIM}	V_{IN} - V_{LX} = 250mV		4.12		5.68	V/V
Current-Limit Threshold (Internal Mode)	V_{VALLEY}	V_{ILIM} = 5.0V		150		350	mV
Current-Limit Threshold (External Mode)	V_{VALLEY}	V_{ILIM} = 2.5V		400		660	mV
Switching Frequency	f_{OSC}			160		240	kHz
Maximum Duty Cycle	D_{MAX}			74		90	%
POSITIVE ANALOG GAIN BLOCKS							
FB2, FB3, FB4 Regulation Voltage		V_{B2} = V_{B3} = V_{B4} = 5V, I_{B2} = I_{B3} = I_{B4} = 1mA (sink)		1.215		1.265	V
FB2, FB3, FB4 to B_ Transconductance Error	$\Delta V_{FB_}$	V_{B2} = V_{B3} = V_{B4} = 5V, I_{B2} = I_{B3} = I_{B4} = 0.5mA to 5mA (sink)				28	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, ILIM = FB = GND, V_{BST} - V_{LX} = 5V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

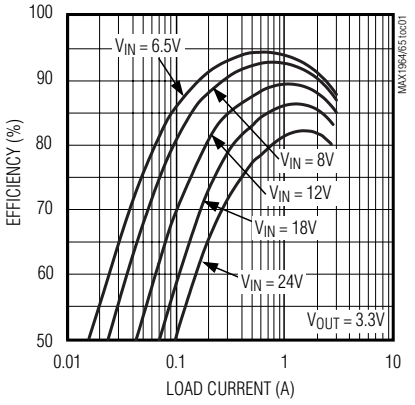
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
NEGATIVE ANALOG GAIN BLOCK						
FB5 Regulation Voltage		V_{B5} = V_{OUT} - 2V, V_{OUT} = 3.5V, I_{B5} = 1mA (source)	-25		+10	mV
FB5 to B5 Transconductance Error	ΔV_{FB5}	V_{B5} = 0, I_{B5} = 0.5mA to 5mA (source)			-30	mV
POWER GOOD (POK)						
OUT Trip Level (Preset Mode)		FB = GND, falling edge, 3% hysteresis (typ)	2.85		3.15	V
FB Trip Level (Adjustable Mode)		Falling edge, 3% hysteresis (typ)	1.058		1.17	V
FB2, FB3, FB4 Trip Level		Falling edge, 3% hysteresis (typ)	1.058		1.17	V
FB5 Trip Level		Rising edge, 35mV hysteresis (typ)	325		675	mV

Note 1: Connect VL to IN for operation with V_{IN} < 5V.
Note 2: See *Output Voltage Selection* section.
Note 3: The internal 5V linear regulator (VL) powers the thermal shutdown block. Shorting VL to GND disables thermal shutdown.
Note 4: Specifications to -40°C are guaranteed by design, not production tested.

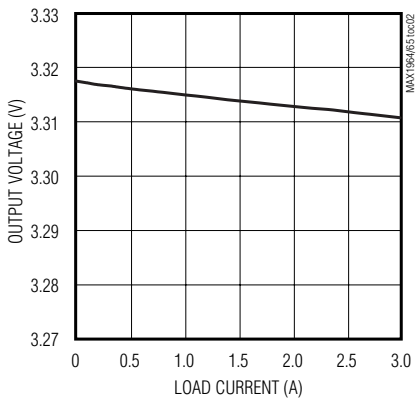
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 12V, V_{OUT} = 3.3V, T_A = +25°C, unless otherwise noted.)

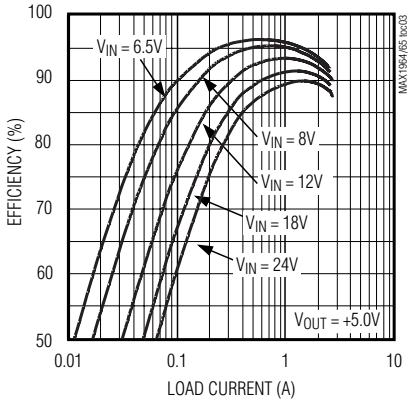
EFFICIENCY vs. LOAD CURRENT (PRESET MODE)



OUTPUT VOLTAGE vs. LOAD CURRENT (PRESET MODE)



EFFICIENCY vs. LOAD CURRENT (ADJUSTABLE MODE)

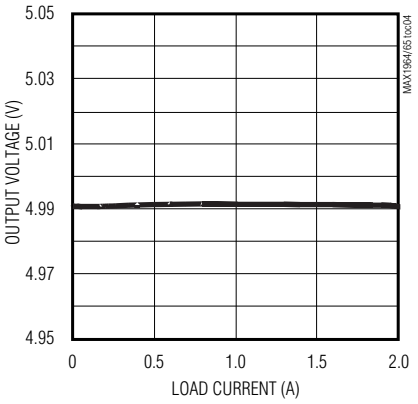


Tracking/Sequencing Triple/Quintuple Power-Supply Controllers

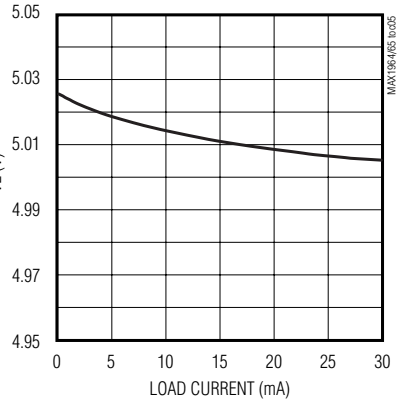
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{OUT} = 3.3V, T_A = +25°C, unless otherwise noted.)

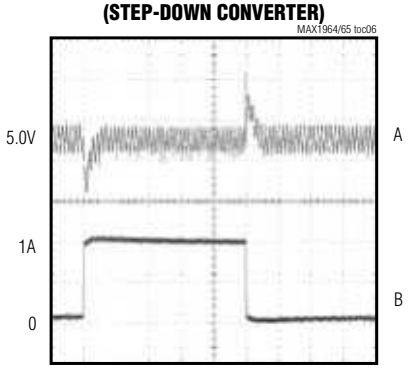
OUPUT VOLTAGE vs. LOAD CURRENT (ADJUSTABLE MODE)



INTERNAL 5V LINEAR REGULATOR vs. LOAD CURRENT



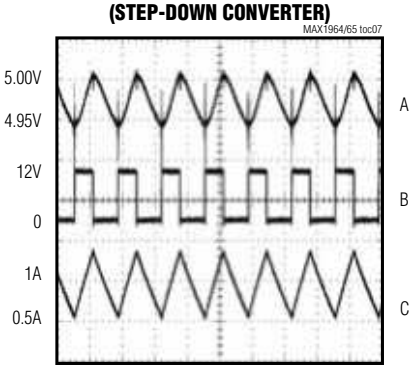
LOAD TRANSIENT (STEP-DOWN CONVERTER)



40µs/div

A. V_{OUT} = 5V, 100mV/div
B. I_{OUT} = 10mA TO 1A, 500mA/div
V_{IN} = 12V

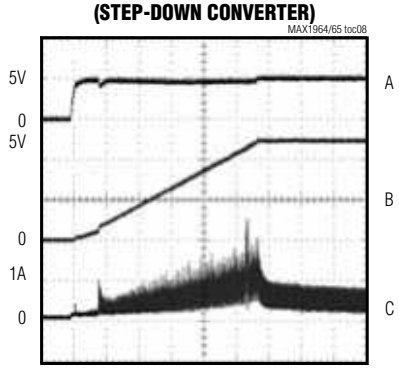
SWITCHING WAVEFORMS (STEP-DOWN CONVERTER)



40µs/div

A. V_{OUT} = 5.0V, 50mV/div
B. V_{LX},10V/div
C. INDUCTOR CURRENT, 500mA/div
V_{IN} = 12V, R_{OUT1} = 5V

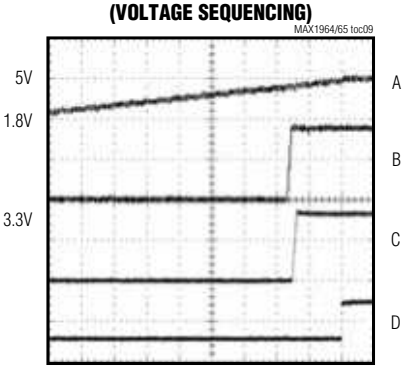
SOFT-START (STEP-DOWN CONVERTER)



1ms/div

A. V_L = 5V, 5V/div
B. V_{OUT1} = 5V (ADJ),2V/div
C. INDUCTOR CURRENT, 1A/div
V_{IN} = STEPPED FROM 0 TO 12V, R_{OUT1} = 10Ω

MAX1964 STARTUP WAVEFORM (VOLTAGE SEQUENCING)



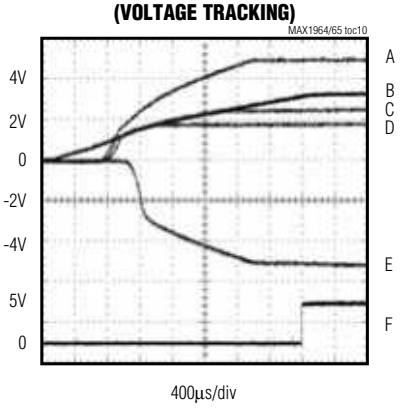
200µs/div

A. V_{OUT1} = 5V (ADJ), 2V/div
B. V_{OUT2} = 1.8V, 1V/div
C. V_{OUT3} = 3.3V, 2V/div
D. V_{POK}, 5V/div
V_{IN} = STEPPED FROM 0 TO 12V, R_{OUT1} = 5Ω

Typical Operating Characteristics (continued)

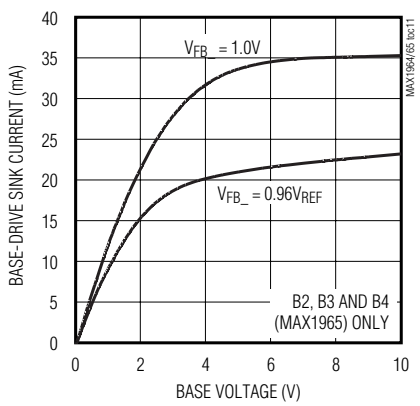
(Circuit of Figure 1, V_{IN} = 12V, V_{OUT} = 3.3V, T_A = +25°C, unless otherwise noted.)

MAX1965 STARTUP WAVEFORM (VOLTAGE TRACKING)

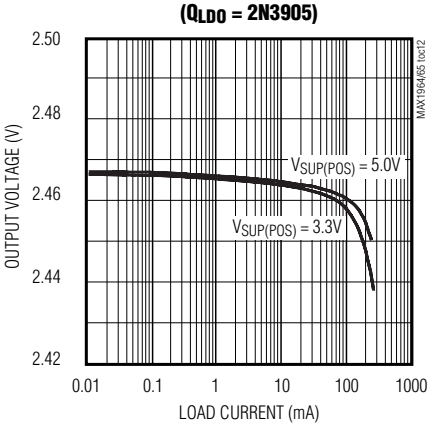


A. V_{OUT4} = 5.0V, 2V/div
B. V_{OUT1} = 3.3V, 2V/div
C. V_{OUT2} = 2.5V, 2V/div
D. V_{OUT3} = 1.8V/div
E. V_{OUT5} = -5.0V, 2V/div
F. V_{POK}, 5V/div
V_{IN} = STEPPED FROM 0 TO 12V,
R_{OUT1} = 6.6Ω
CIRCUIT OF FIGURE 6

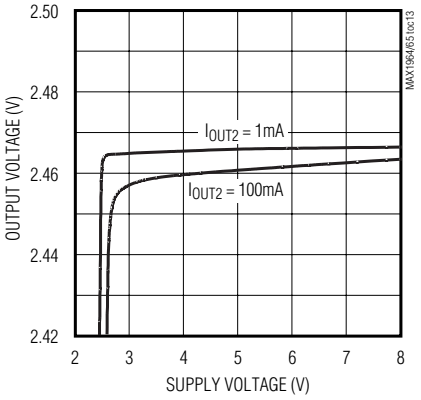
POSITIVE LINEAR REGULATOR BASE-DRIVE CURRENT vs. BASE-DRIVE VOLTAGE



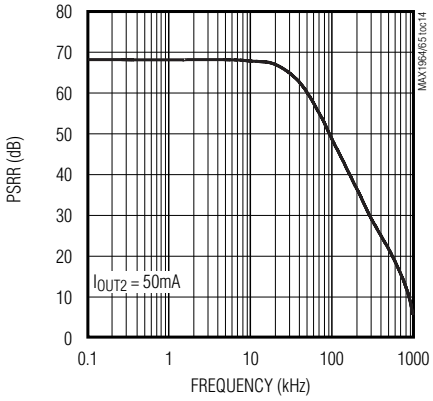
POSITIVE LINEAR REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT (Q_{LDO} = 2N3905)



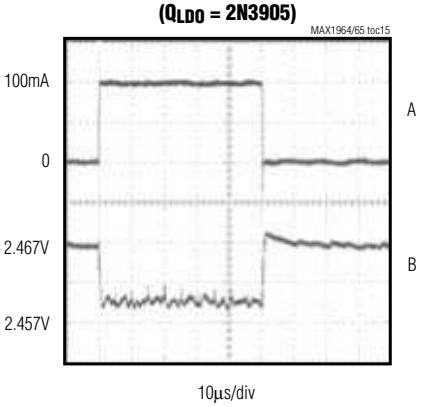
POSITIVE LINEAR REGULATOR OUTPUT VOLTAGE vs. SUPPLY VOLTAGE (Q_{LDO} = 2N3905)



POSITIVE LINEAR REGULATOR POWER-SUPPLY REJECTION RATIO (Q_{LDO} = 2N3905)



POSITIVE LINEAR REGULATOR LOAD TRANSIENT (Q_{LDO} = 2N3905)



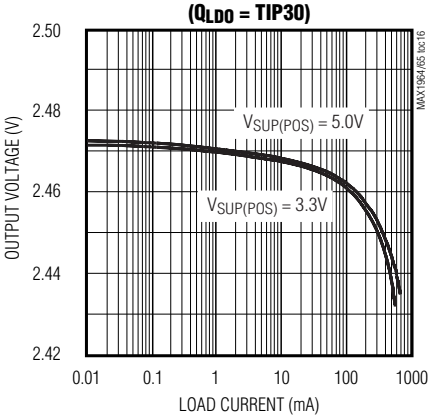
A. I_{OUTZ} = 1mA TO 100mA, 50mA/div
B. V_{OUTZ} = 2.5V, 5mV/div
$C_{LDO(POS)}$ = 10µF CERAMIC, $V_{SUP(POS)}$ = 3.3V
CIRCUIT OF FIGURE 1

Tracking/Sequencing Triple/Quintuple Power-Supply Controllers

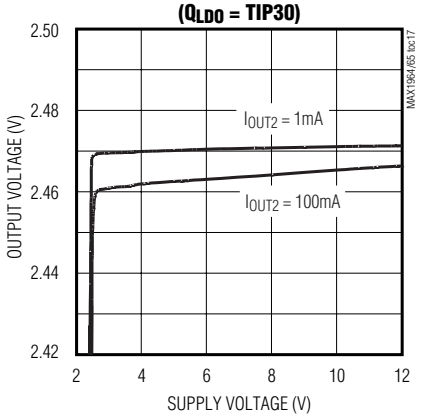
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{OUT} = 3.3V, T_A = +25°C, unless otherwise noted.)

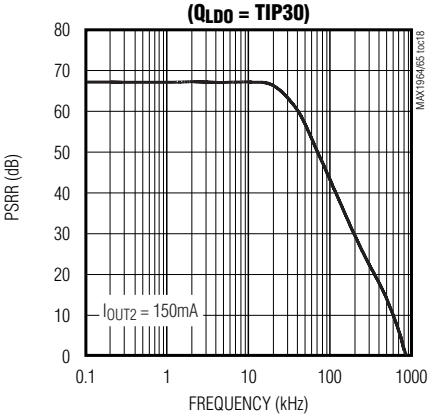
POSITIVE LINEAR REGUALTOR OUTPUT VOLTAGE vs. LOAD CURRENT (Q_{LDO} = TIP30)



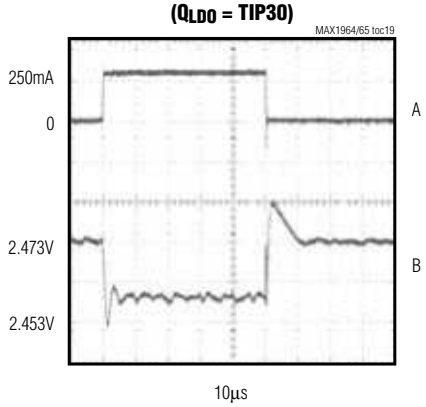
POSITIVE LINEAR REGULATOR OUTPUT VOLTAGE vs. SUPPLY VOLTAGE (Q_{LDO} = TIP30)



POSITIVE LINEAR REGULATOR POWER-SUPPLY REJECTION RATIO (Q_{LDO} = TIP30)

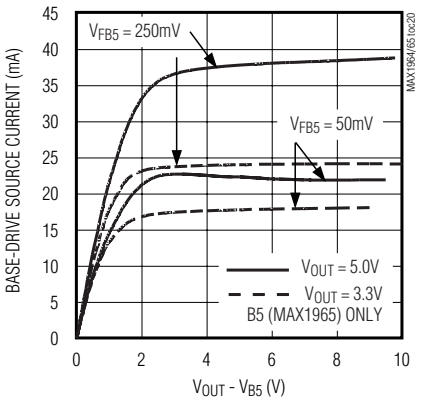


POSITIVE LINEAR REGULATOR LOAD TRANSIENT (Q_{LDO} = TIP30)

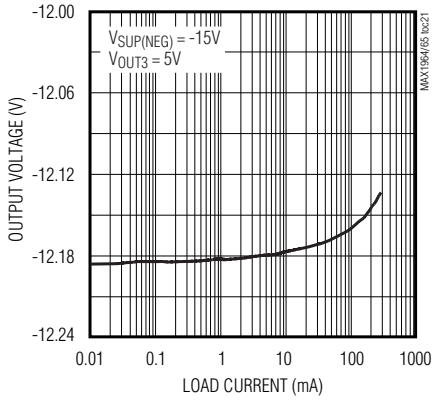


A. I_{OUT2} = 10mA TO 250mA, 200mA/div
B. V_{OUT2} = 2.5V, 10mV/div
$C_{LDO(POS)}$ = 10µF CERAMIC, $V_{SUP(POS)}$ = 3.3V
CIRCUIT OF FIGURE 1

NEGATIVE LINEAR REGULATOR BASE-DRIVE CURRENT vs. BASE-DRIVE VOLTAGE

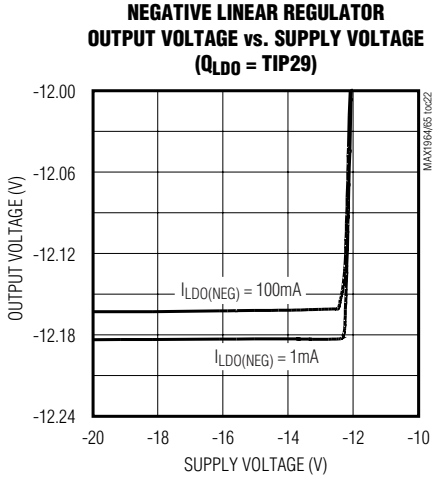


NEGATIVE LINEAR REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT (Q_{LDO} = TIP29)



Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{OUT} - 3.3V, T_A = +25°C, unless otherwise noted.)



Pin Description

PIN		NAME	FUNCTION
MAX1964	MAX1965		
1	1	POK	Open-Drain Power-Good Output. POK is low when any output voltage is more than 10% below its regulation point. POK is high impedance when all the outputs are in regulation. Connect a resistor between POK and VL for logic-level voltages.
2	2	COMP	Compensation Pin. Connect the compensation network to GND to compensate the control loop.
3	3	OUT	Regulated Output Voltage High-Impedance Sense Input. Internally connected to a resistive-divider and negative gain block (MAX1965).
4	4	FB	Dual-Mode Switching-Regulator Feedback Input. Connect to GND for the preset 3.3V output. Connect to a resistive-divider from the output to FB to GND to adjust the output voltage between 1.236V and 0.75 × V_{IN}. The feedback set point is 1.236V.
5	5	B2	Open-Drain Output PNP Transistor Driver (Regulator 2). Internally connected to the drain of a DMOS. B2 connects to the base of an external PNP pass transistor to form a positive linear regulator.
6	6	FB2	Analog Gain Block Feedback Input (Regulator 2). Connect to a resistive-divider between the positive linear regulator's output and GND to adjust the output voltage. The feedback set point is 1.24V.

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Pin Description (continued)

PIN		NAME	FUNCTION
MAX1964	MAX1965		
7	7	B3	Open-Drain Output PNP Transistor Driver (Regulator 3). Internally connected to the drain of a DMOS. B3 connects to the base of an external PNP pass transistor to form a positive linear regulator.
8	8	FB3	Analog Gain Block Feedback Input (Regulator 3). Connect to a resistive-divider between the positive linear regulator's output and GND to adjust the output voltage. The feedback set point is 1.24V.
—	9	B4	Open-Drain Output PNP Transistor Driver (Regulator 4). Internally connected to the drain of a DMOS. B4 connects to the base of an external PNP pass transistor to form a positive linear regulator.
—	10	FB4	Analog Gain Block Feedback Input (Regulator 4). Connect to a resistive-divider between the positive linear regulator's output and GND to adjust the output voltage. The feedback set point is 1.24V.
—	11	B5	Open-Drain Output NPN Transistor Driver (Regulator 5). Internally connected to the drain of a P-channel MOSFET. B5 connects to the base of an external NPN pass transistor to form a negative linear regulator.
—	12	FB5	Analog Gain Block Feedback Input (Regulator 5). Connect to a resistive-divider between the negative linear regulator's output and a positive reference voltage, typically one of the positive linear regulator outputs, to adjust the output voltage. The feedback set point is at GND.
9	13	ILIM	Dual-Mode Current-Limit Adjustment Input. Connect to VL for the default 250mV current-limit threshold. In adjustable mode, the current-limit threshold voltage is 1/5 th the voltage present at ILIM. Connect to a resistive-divider between VL and GND to adjust V_{ILIM} between 500mV and 2.5V. The logic threshold for switchover to the 250mV default value is approximately VL - 1V.
10	14	GND	Ground
11	15	DL	Low-Side Gate-Driver Output. DL swings between GND and VL.
12	16	LX	Inductor Connection. Used for current-sense between IN and LX, and used for current-limit between LX and GND.
13	17	DH	High-Side Gate-Driver Output. DH swings between LX and BST.
14	18	BST	Boost Flying Capacitor Connection. Connect BST to the external boost diode and capacitor as shown in the *Standard Application Circuit*.
15	19	VL	Internal 5V Linear Regulator Output. Supplies the IC and powers the DL low-side gate driver and external boost diode and capacitor. Bypass with a 1µF or greater ceramic capacitor to GND.
16	20	IN	Input Supply Voltage. 4.5V to 28V. Bypass to GND with a 1µF or greater ceramic capacitor close to the IC.

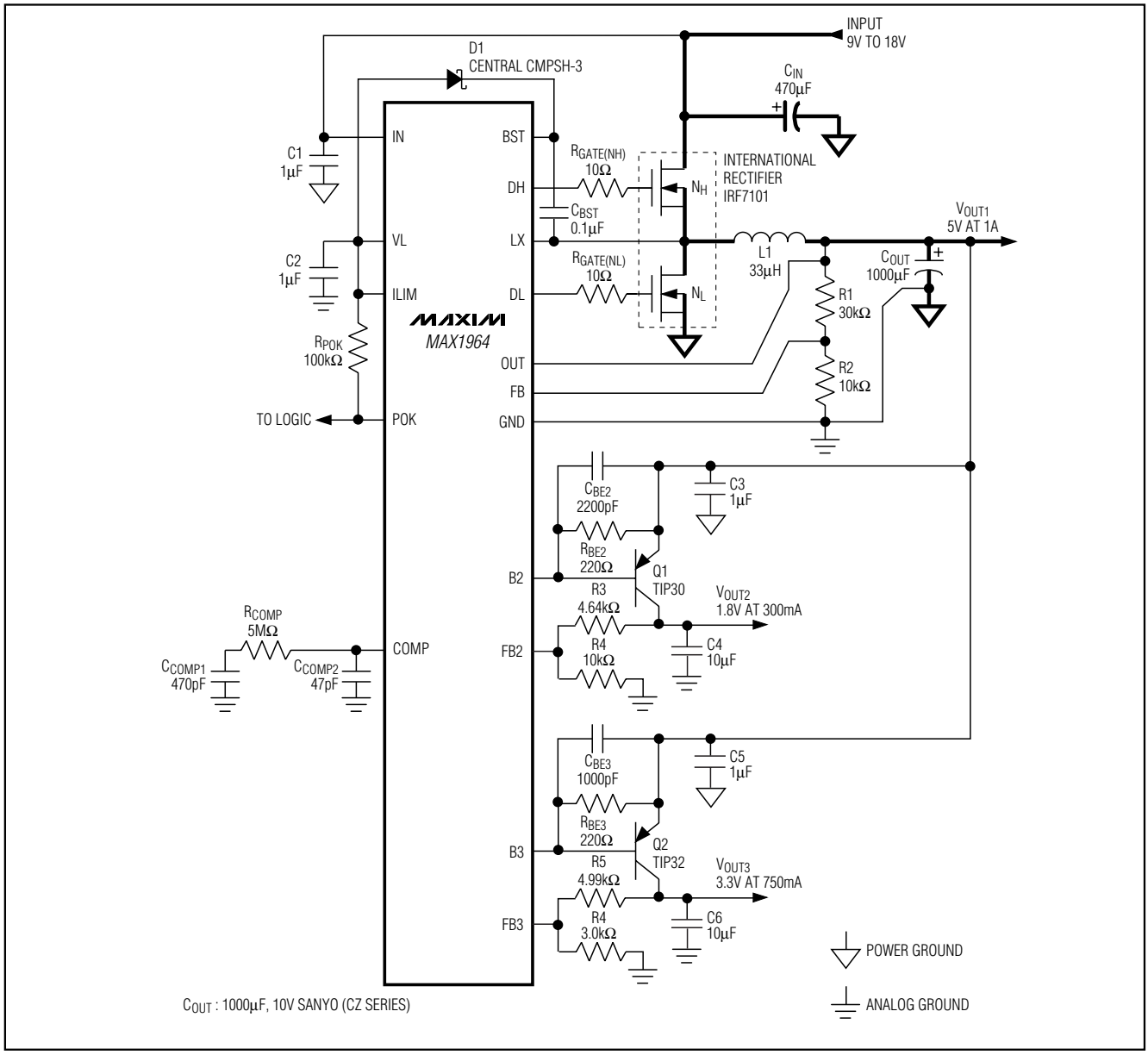


Figure 1. MAX1964 Standard Application Circuit

Detailed Description

The MAX1964/MAX1965 power-supply controllers provide system power for cable and xDSL modems. The main step-down DC-DC controller operates in a current-mode pulse-width-modulation (PWM) control scheme to ease compensation requirements and provide excellent load and line transient response.

The MAX1964 includes two analog gain blocks to regulate two additional positive auxiliary output voltages, and the MAX1965 includes four analog gain blocks to regulate three additional positive and one negative auxiliary output voltages. The positive regulator gain blocks can be used to generate low voltage rails directly from the main step-down converter or higher voltages using coupled windings from the step-down converter. The

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negative gain block can be used in conjunction with a coupled winding to generate -5V, -12V, or -15V.

DC-DC Controller

The MAX1964/MAX1965 step-down converters use a pulse-width-modulated (PWM) current-mode control scheme (Figure 2). An internal transconductance amplifier establishes an integrated error voltage at the COMP pin. The heart of the current-mode PWM controller is an open-loop comparator that compares the integrated voltage-feedback signal against the amplified current-sense signal plus the slope compensation ramp. At each rising edge of the internal clock, the high-side MOSFET turns on until the PWM comparator trips or the maximum duty cycle is reached. During this on-time, current ramps up through the inductor, sourcing current to the output and storing energy in a magnetic field. The current-mode feedback system regulates the peak inductor current as a function of the output voltage error signal. Since the average inductor current is nearly the same as the peak inductor current (assuming that the inductor value is relatively high to minimize ripple current), the circuit acts as a switch-mode transconductance amplifier. It pushes the output LC filter pole, normally found in a voltage-mode PWM, to a higher frequency. To preserve inner-loop stability and eliminate inductor stair casing, a slope-compensation ramp is summed into the main PWM comparator.

During the second-half of the cycle, the high-side MOSFET turns off and the low-side N-Channel MOSFET turns on. Now the inductor releases the stored energy as its current ramps down, providing current to the output. Therefore, the output capacitor stores charge when the inductor current exceeds the load current, and discharges when the inductor current is lower, smoothing the voltage across the load. Under overload conditions when the inductor current exceeds the selected current-limit (see the *Current Limit* section), the high-side MOSFET is not turned on at the rising edge of the clock and the low-side MOSFET remains on to let the inductor current ramp down.

The MAX1964/MAX1965 operate in a forced-PWM mode, so even under light loads, the controller maintains a constant switching frequency to minimize cross-regulation errors in applications that use a transformer. So the low-side gate-drive waveform is the complement of the high-side gate-drive waveform, which causes the inductor current to reverse under light loads.

Current-Sense Amplifier

The one MAX1964/MAX1965's one current-sense circuit amplifies (A_V = 4.9) the current-sense voltage generated by the high-side MOSFET's on resistance ($R_{DS(ON)} \times I_{INDUCTOR}$). This amplified current-sense signal and the internal slope compensation signal are summed together (V_{SUM}) and fed into the PWM comparator's inverting input. The PWM comparator turns off the high-side MOSFET when the V_{SUM} exceeds the integrated feedback voltage (V_{COMP}). Place the high-side MOSFET no further than 5mm from the controller and connect IN and LX to the MOSFET using Kelvin sense connections to guarantee current-sense accuracy and improve stability.

Current-Limit Circuit

The current-limit circuit employs a unique "valley" current-limiting algorithm that uses the low-side MOSFET's on-resistance as a sensing element (Figure 3). If the voltage across the low-side MOSFET ($R_{DS(ON)} \times I_{INDUCTOR}$) exceeds the current-limit threshold at the beginning of a new oscillator cycle, the MAX1964/MAX1965 will not turn on the high-side MOSFET. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the low-side MOSFET on-resistance, inductor value, input voltage, and output voltage. The reward for this uncertainty is robust, lossless overcurrent limiting.

In adjustable mode, the current-limit threshold voltage is approximately one-fifth the voltage seen at ILIM ($I_{VALLEY} = 0.2 \times V_{ILIM}$). Adjust the current-limit threshold by connecting a resistive-divider from VL to ILIM to GND. The current-limit threshold can be set from 106mV to 530mV, which corresponds to ILIM input voltages of 500mV to 2.5V. This adjustable current limit accommodates MOSFETs with a wide range of on-resistance characteristics (see the *Design Procedure* section). The current-limit threshold defaults to 250mV when ILIM is connected to VL. The logic threshold for switchover to the 250mV default value is approximately VL - 1V.

Carefully observe the PC board layout guidelines to ensure that noise and DC errors don't corrupt the current-sense signals seen by LX and GND. The IC must be mounted close to the low-side MOSFET with short (less than 5mm), direct traces making a Kelvin sense connection.

Synchronous Rectifier Driver (DL)

Synchronous rectification reduces conduction losses in the rectifier by replacing the normal Schottky catch diode with a low-resistance MOSFET switch. The MAX1964/MAX1965 also use the synchronous rectifier to ensure proper startup of the boost gate-driver circuit and to provide the current-limit signal.

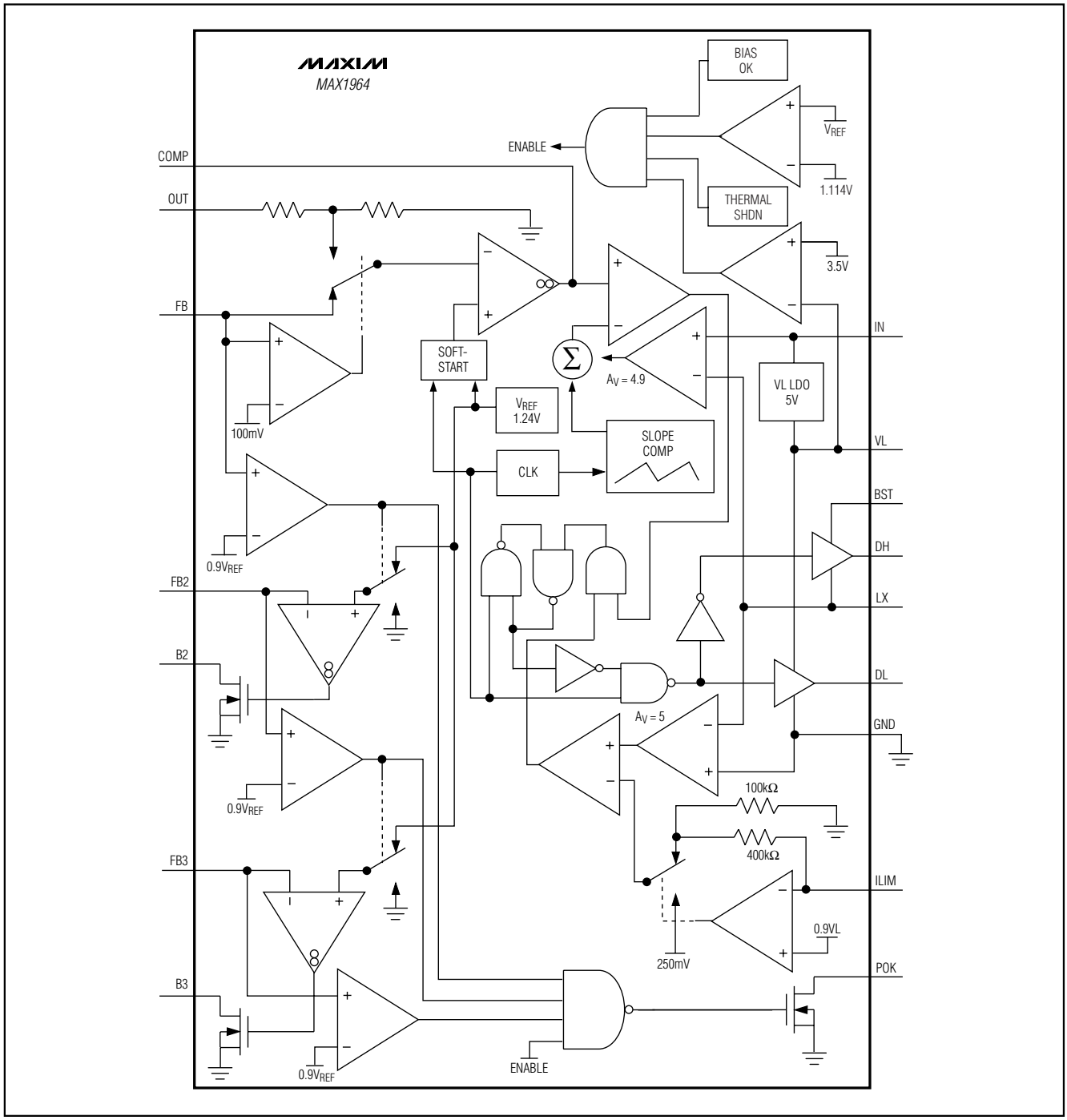


Figure 2a. MAX1964 Functional Diagram

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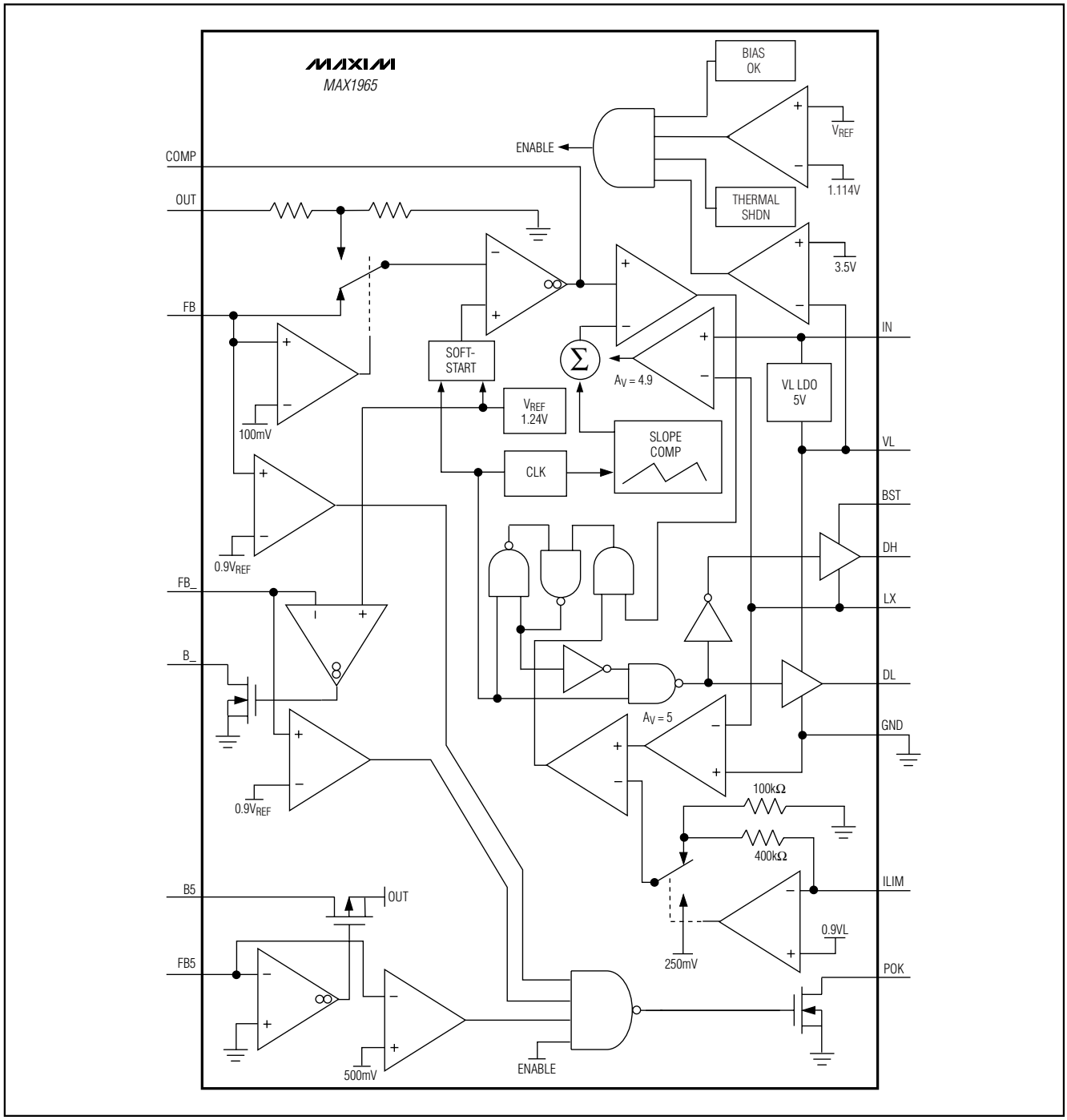


Figure 2b. MAX1965 Functional Diagram

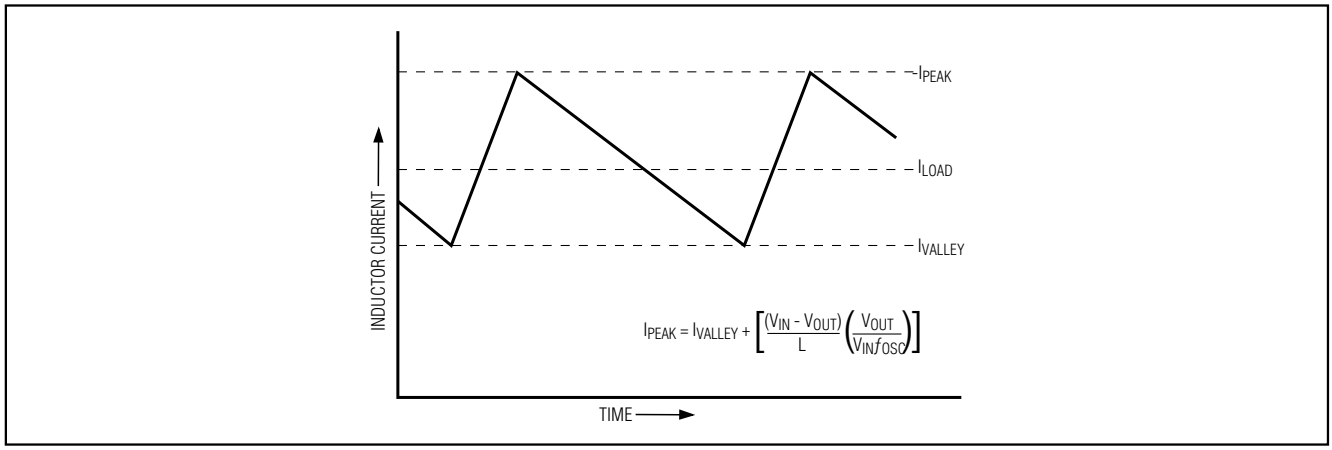


Figure 3. "Valley" Current-Limit Threshold Point

The DL low-side drive waveform is always the complement of the DH high-side drive waveform (with controlled dead time to prevent cross-conduction or "shoot-through"). A dead-time circuit monitors the DL output and prevents the high-side FET from turning on until DL is fully off. In order for the dead-time circuit to work properly, there must be a low-resistance, low-inductance path from the DL driver to the MOSFET gate. Otherwise, the sense circuitry in the MAX1964/MAX1965 will interpret the MOSFET gate as "off" when gate charge actually remains. Use very short, wide traces (50mils to 100mils wide if the MOSFET is 1 inch from the device). The dead time at the other edge (DH turning off) is determined by a fixed internal delay.

High-Side Gate-Drive Supply (BST)

Gate-drive voltage for the high-side N-channel switch is generated by a flying-capacitor boost circuit (Figure 1). The capacitor between BST and LX is alternately charged from the VL supply and placed parallel to the high-side MOSFET's gate and source terminals.

On startup, the synchronous rectifier (low-side MOSFET) forces LX to ground and charges the boost capacitor to 5V. On the second half-cycle, the switch-mode power supply turns on the high-side MOSFET by closing an internal switch between BST and DH. This provides the necessary gate-to-source voltage to turn on the high-side switch, an action that boosts the 5V gate-drive signal above the input voltage.

Internal 5V Linear Regulator (VL)

All MAX1964/MAX1965 functions, except the current-sense amplifier, are internally powered from the on-chip, low-dropout 5V regulator. The maximum regulator input voltage (V_{IN}) is 28V. Bypass the regulator's output (VL) with a ceramic capacitor of at least 1µF to GND. The V_{IN}-to-VL dropout voltage is typically 200mV, so when V_{IN} is less than 5.2V, VL is typically V_{IN} - 200mV.

The internal linear regulator can source up to 20mA to supply the IC, power the low-side gate driver, charge the external boost capacitor, and supply small external loads. When driving particularly large FETs, little or no regulator current may be available for external loads. For example, when switched at 200kHz, a large FET with 40nC total gate charge requires 40nC x 200kHz, or 8mA.

Undervoltage Lockout

If VL drops below 3.5V, the MAX1964/MAX1965 assumes that the supply voltage is too low to make valid decisions, so the undervoltage lockout (UVLO) circuitry inhibits switching, forces POK low, and forces the DL and DH gate drivers low. After VL rises above 3.5V, the controller powers up the outputs (see *Startup* section).

Startup

Externally, the MAX1964/MAX1965 start switching when VL rises above the 3.5V undervoltage lockout threshold. However, the controller is not enabled unless *all four* conditions are met: 1) VL exceeds the 3.5V undervoltage lockout threshold, 2) the internal reference exceeds 92% of its nominal value (V_{REF} > 1.145V), 3) the internal bias circuitry powers up, and 4) the thermal limit is not exceeded. Once the MAX1964/MAX1965 assert the internal enable signal, the step-down controller starts switching and enables soft-start.

The soft-start circuitry gradually ramps up to the reference voltage in order to control the rate of rise of the step-down controller and reduce input surge currents

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during startup. The soft-start period is 1024 clock cycles (1024/f_{OSC}), and the internal soft-start DAC ramps up the voltage in 64 steps. The output reaches regulation when soft-start is completed, regardless of output capacitance and load.

Output Voltage Sequencing (MAX1964)

After the reference powers up, the controller begins a startup sequence. First, the main DC-DC step-down converter powers up with soft-start enabled. Once the step-down converter reaches 92% of its nominal value (V_{FB} > 1.145V) and soft-start is completed, the controller powers up the first positive linear regulator. Once the first linear regulator reaches 92% of its nominal value (V_{FB2} > 1.145V), the second linear regulator powers up. Once all three output voltages exceed 92% of their nominal values, the active-high ready signal (POK) goes high (see *Power-Good Output* section).

Output Voltage Tracking (MAX1965)

After the reference powers up, the controller simultaneously powers up all five output voltages. The main DC-DC step-down converter powers up with soft-start enabled while the linear regulators are fully activated. However, the linear regulators' inputs are typically connected to or derived from the step-down converter output voltage. Since the linear regulators are fully active, the pass transistors immediately saturate, allowing these output voltages to track the step-down converter's slow rising output voltage (see *Typical Operating Characteristics*). Once all five output voltages exceed 92% of their nominal values, the active-high ready signal (POK) goes high (see *Power-Good Output* section).

Power-Good Output (POK)

POK is an open-drain output. The MOSFET turns on and pulls POK low when any output falls below 90% of its nominal regulation voltage. Once all of the outputs exceed 92% of their nominal regulation voltages and soft-start is completed, POK goes high impedance. To obtain a logic voltage output, connect a pullup resistor from POK to VL. A 100kΩ resistor works well for most applications. If unused, leave POK grounded or unconnected.

Thermal overload Protection

Thermal overload protection limits total power dissipation in the MAX1964/MAX1965. When the junction temperature exceeds T_J = +160°C, a thermal sensor shuts down the device, forcing DL and DH low, allowing the IC to cool. The thermal sensor turns the part on again after the junction temperature cools by 15°C, resulting in a pulsed output during continuous thermal overload conditions. If the VL output is short-circuited, thermal overload protection is disabled.

During a thermal event, the main step-down converter and the linear regulators are turned off, POK goes low, and soft-start is reset.

Design Procedure

DC-DC Step-Down Converter

Output Voltage Selection

The step-down controller's feedback input features dual mode operation. Connect the output to OUT and connect FB to GND for the preset 3.3V output voltage. Alternatively, the MAX1964/MAX1965 output voltage may be adjusted by connecting a voltage-divider from the output to FB to GND (Figure 4). Select R2 in the 5kΩ to 50kΩ range. Calculate R1 with the following equation:

$$R1 = R2\left[\left(\frac{V_{OUT}}{V_{SET}}\right) - 1\right]$$

where V_{SET} = 1.236V and V_{OUT} may range from 1.236V to approximately 0.75 × V_{IN} (up to 20V). If V_{OUT} > 5.5V, connect OUT to GND (MAX1964) or to one of the positive linear regulators (MAX1965) with an output voltage between 2V and 5V.

Inductor Value

Three key inductor parameters must be specified: inductance value (L), peak current (I_{PEAK}), and DC resistance (R_{DC}). The following equation includes a constant LIR, which is the ratio of inductor peak-to-peak AC current to DC load current. A higher LIR value allows smaller inductance, but results in higher losses and higher output ripple. A good compromise between size and losses is a 30% ripple-current to load-current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, selected LIR determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} f_{SW} I_{LOAD(MAX)} LIR}$$

where f_{SW} is 200kHz. The exact inductor value is not critical and can be adjusted in order to make trade-offs among size, cost, and efficiency. Lower inductor values minimize size and cost, but they also increase the output ripple and reduce the efficiency due to higher peak currents. On the other hand, higher inductor values increase efficiency, but at some point resistive losses due to extra turns of wire will exceed the benefit gained from lower AC current levels.

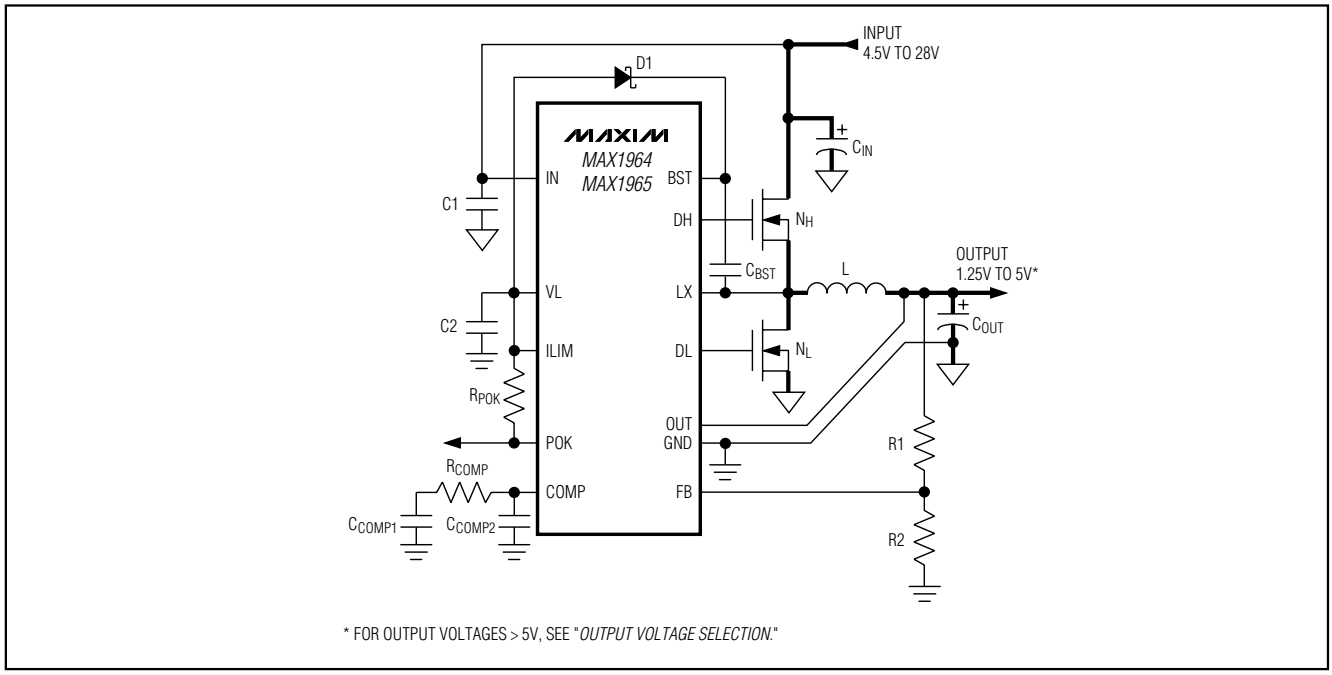


Figure 4. Adjustable Output Voltage

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The chosen inductor's saturation rating must exceed the peak inductor current:

$$I_{PEAK} = I_{LOAD(MAX)} + \left(\frac{LIR}{2}\right) I_{LOAD(MAX)}$$

Setting the Current Limit

The minimum current-limit threshold must be high enough to support the maximum load current at the minimum tolerance level of the current-limit circuit. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half of the ripple current:

$$\frac{V_{VALLEY(LOW)}}{R_{DS(ON)}} > I_{LOAD(MAX)} - \left(\frac{LIR}{2}\right) I_{LOAD(MAX)}$$

where $R_{DS(ON)}$ is the on-resistance of the low-side MOSFET (N_L). For the MAX1964/MAX1965, the minimum current-limit threshold is 190mV (for the typical 250mV default setting). Use the worst-case maximum value for $R_{DS(ON)}$ from the MOSFET N_L data sheet, and add some margin for the rise in $R_{DS(ON)}$ over temperature. A good general rule is to allow 0.5% additional resistance for each °C of the MOSFET junction temperature rise.

Connect ILIM to VL for the default 250mV (typ) current-limit threshold. For an adjustable threshold, connect a resistive-divider from VL to ILIM to GND. The external adjustment range of 500mV to 2.5V corresponds to a current-limit threshold of 106mV to 530mV. When adjusting the current limit, use 1% tolerance resistors and a 10µA divider current to prevent a significant increase in the current-limit tolerance.

MOSFET Selection

The MAX1964/MAX1965's step-down controller drives two external logic-level N-channel MOSFETs as the circuit switch elements. The key selection parameters are:

1. On-resistance ($R_{DS(ON)}$)
2. Maximum drain-to-source voltage ($V_{DS(MAX)}$)
3. Minimum threshold voltage ($V_{TH(MIN)}$)
4. Total gate charge (Q_G)
5. Reverse transfer capacitance (C_{RSS})

The high-side N-channel MOSFET must be a logic-level type with guaranteed on-resistance specifications at $V_{GS} \le 4.5V$. Select the high-side MOSFET's on-resistance ($R_{DS(ON)}$) so $I_{PEAK} \times R_{DS(ON)} \le 225mV$ for the

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current-sense range. For a good compromise between efficiency and cost, choose a high-side MOSFET (N_H) that has conduction losses equal to the switching losses at the optimum input voltage. Check to ensure that the conduction losses at minimum input voltage don't exceed the package thermal limits or violate the overall thermal budget. Check to ensure that the conduction losses plus switching losses at the maximum input voltage don't exceed package ratings or violate the overall thermal budget.

The low-side MOSFET (N_L) provides the current-limit signal, so choose a MOSFET with an $R_{DS(ON)}$ large enough to provide adequate circuit protection (see the *Setting the Current-Limit* section):

$$R_{DS(ON)} = \frac{V_{VALLEY}}{I_{VALLEY}}$$

Use the worst-case maximum value for $R_{DS(ON)}$ from the MOSFET NL data sheet, and add some margin for the rise in $R_{DS(ON)}$ over temperature. A good general rule is to allow 0.5% additional resistance for each °C of the MOSFET junction temperature rise. Ensure that the MAX1964/MAX1965 DL gate drivers can drive N_L; in other words, check that the dv/dt caused by N_H turning on does not pull up the N_L gate due to drain-to-gate capacitance, causing cross-conduction problems.

MOSFET package power dissipation often becomes a dominant design factor. I^2R power losses are the greatest heat contributor for both high-side and low-side MOSFETs. I^2R losses are distributed between N_H and N_L according to duty factor as shown in the equations below. Generally, switching losses affect only the high-side MOSFET, since the low-side MOSFET is a zero-voltage switched device when used in the buck topology.

Gate-charge losses are dissipated by the driver and do not heat the MOSFET. Calculate the temperature rise according to package thermal-resistance specifications to ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature. The worst-case dissipation for the high-side MOSFET (P_{NH}) occurs at both extremes of input voltage, and the worst-case dissipation for the low-side MOSFET (P_{NL}) occurs at maximum input voltage.

$$P_{NH(SWITCHING)} = V_{IN} I_{LOAD} f_{OSC} \left(\frac{Q_{GS} + Q_{GD}}{I_{GATE}} \right)$$

I_{GATE} is the average DH driver output current capability determined by:

$$I_{GATE} = \frac{VL}{2\left(R_{DS(ON)DH} + R_{GATE}\right)}$$

where $R_{DS(ON)DH}$ is the high-side MOSFET driver's on-resistance (4Ω max), and R_{GATE} is any resistance placed between DH and the high-side MOSFET's gate (Figure 5).

$$P_{NH(CONDUCTION)} = I_{LOAD}{}^2 R_{DS(ON)NH} \left(\frac{V_{OUT}}{V_{IN}} \right)$$

$$P_{NH(TOTAL)} = P_{NH(SWITCHING)} + P_{NH(CONDUCTION)}$$

$$P_{NL} = I_{LOAD}{}^2 R_{DS(ON)NL} \left(1 - \left(\frac{V_{OUT}}{V_{IN}} \right) \right)$$

To reduce EMI caused by switching noise, add a 0.1µF ceramic capacitor from the high-side switch drain to the low-side switch source or add resistors (max 47Ω) in series with DL and DH to increase the switches' turn-on and turn-off times (Figure 5).

The minimum load current should exceed the high-side MOSFET's maximum leakage current over temperature if fault conditions are expected.

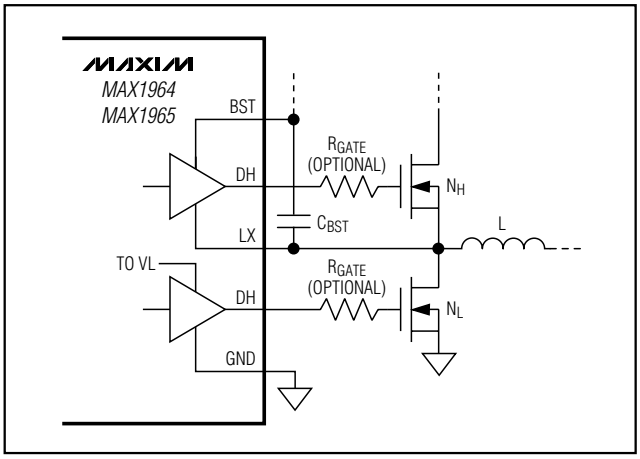


Figure 5. Reducing the Switching EMI

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents defined by the following equation:

$$I_{RMS} = I_{LOAD} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = $2V_{OUT}$), so $I_{RMS(MAX)}$ = $I_{LOAD}/2$. For most applications, nontantalum capacitors (ceramic, aluminum, polymer, or OSCON) are preferred due to their robustness with high inrush currents typical of systems with low impedance inputs. Additionally, two (or more) smaller value low-ESR capacitors can be connected in parallel for lower cost. Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal circuit long-term reliability.

Output Capacitor

The key selection parameters for the output capacitor are the actual capacitance value, the equivalent series resistance (ESR), and voltage-rating requirements which affect the overall stability, output ripple voltage, and transient response.

The output ripple has two components: variations in the charge stored in the output capacitor, and the voltage drop across the capacitor's equivalent series resistance (ESR) caused by the current into and out of the capacitor.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

The output voltage ripple as a consequence of the ESR and output capacitance is:

$$V_{RIPPLE(ESR)} = I_{P-P}ESR$$

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8C_{OUT}f_{SW}}$$

$$I_{P-P} = \left(\frac{V_{IN} - V_{OUT}}{f_{SW}L}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)$$

where I_{p-p} is the peak-to-peak inductor current (see *Inductor Selection* section). These equations are suitable for initial capacitor selection, but final values should be set by testing a prototype or evaluation circuit. As a general rule, a smaller ripple current results in less output ripple. Since the inductor ripple current is a factor of the inductor value and input voltage, the output voltage ripple decreases with larger inductance, but increases with lower input voltages.

With low-cost aluminum electrolytic capacitors, the ESR-induced ripple can be larger than that caused by the charge into and out of the capacitor. Consequently, high quality low-ESR aluminum-electrolytic, tantalum, polymer, or ceramic filter capacitors are required to minimize output ripple. Best results at reasonable cost are typically achieved with an aluminum-electrolytic capacitor in the 470µF range, in parallel with a 0.1µF ceramic capacitor.

Since the MAX1964/MAX1965 use a current-mode control scheme, the output capacitor forms a pole that affects circuit stability (see *Compensation Design*). Furthermore, the output capacitor's ESR also forms a zero.

The MAX1964/MAX1965's response to a load transient depends on the selected output capacitor. After a load transient, the output instantly changes by ESR x ΔI_{LOAD}. Before the controller can respond, the output will sag further depending on the inductor and output capacitor values. After a short period of time (see *Typical Operating Characteristics*), the controller responds by regulating the output voltage back to its nominal state. For applications that have strict transient requirements, low-ESR high-capacitance electrolytic capacitors are recommended to minimize the transient voltage swing.

Do not exceed the capacitor's voltage or ripple-current ratings.

Compensation Design

The MAX1964/MAX1965 controllers use an internal transconductance error amplifier whose output allows compensation of the control loop. Connect a series resistor and capacitor between COMP and GND to form a pole-zero pair, and connect a second parallel capacitor between COMP and GND to form another pole. The external inductor, high-side MOSFET, output capacitor, compensation resistor, and compensation capacitors determine the loop stability. The inductor and output capacitor are chosen based on performance, size, and cost, while the compensation resistor and capacitors are selected to optimize control-loop stability. The component values shown in the *Standard Application Circuit* (Figures 1 and 6) yield stable operation over a broad range of input-to-output voltages.

The controller uses a current-mode control scheme that regulates the output voltage by forcing the required current through the external inductor, so the MAX1964/MAX1965 use the voltage across the high-side MOSFET's on-resistance ($R_{DS(ON)}$) to sense the inductor current. Using the current-sense amplifier's output signal and the amplified feedback voltage, the control loop determines the peak inductor current by:

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$$I_{PEAK} = \frac{V_{OUT}V_{REF}A_{VEA}}{V_{OUT(NOMINAL)}R_{DS(ON)}A_{VCS}}$$

where V_{REF} = 1.24V, A_{VCS} is the current-sense amplifier's gain (4.9 typ), A_{VEA} is the DC gain of the transconductance error amplifier (2000 typ) set by its DC output resistance, and $V_{OUT(NOMINAL)}$ is the output voltage set by the feedback resistive-divider (internal or external). Since the output voltage is a function of the load current and load resistance, the total DC loop gain ($A_{V(DC)}$) is approximately:

$$A_{V(DC)} \approx \frac{I_{PEAK}}{I_{LOAD}} \approx \frac{V_{REF}R_{LOAD}A_{VEA}}{V_{OUT(NOMINAL)}R_{DS(ON)}A_{VCS}}$$
$$\approx \frac{400 \times V_{REF}R_{LOAD}}{V_{OUT(NOMINAL)}R_{DS(ON)}}$$

The first compensation capacitor (C_{COMP1}) creates the dominant pole. Due to the current-mode control scheme, the output capacitor also creates a pole in the system which is a function of the load resistance. As the load resistance increases, the frequency of the output capacitor's pole decreases. However, the DC loop gain increases with larger load resistance, so the unity-gain bandwidth remains fixed. Additionally, the compensation resistor and the output capacitor's ESR both generate zeros which must be canceled out by corresponding poles. Therefore, in order to achieve stable operation, use the following procedure to properly compensate the system:

1) The crossover frequency (the frequency at which unity gain occurs) must be less than 1/5th the switching frequency:

$$f_C \le \frac{f_{SW}}{5}$$

2) Determine the series compensation capacitor (C_{COMP1}) required to set the desired crossover frequency:

$$C_{COMP1} \ge \frac{1}{2\pi}\left(\frac{g_m A_{V(DC)}}{2000 f_C}\right)$$

where the error amplifier's transconductance (g_m) is 100µS (see *Electrical Characteristics*) and $A_{V(DC)}$ is the total DC loop gain defined above.

3) Before crossover occurs, the output capacitor and the load resistor generate a second pole:

$$f_{POLE(OUT)} = \frac{1}{2\pi C_{OUT}R_{LOAD}} = \frac{I_{LOAD(MAX)}}{2\pi C_{OUT}V_{OUT}}$$

4) The series compensation resistor and capacitor provide a zero which can be used to cancel the second pole in order to ensure stability:

$$R_{COMP} \ge \frac{1}{2\pi C_{COMP1}f_{POLE(OUT)}}$$

5) For most applications using electrolytic capacitors, the output capacitor's ESR forms a second zero that occurs before crossover. Applications using low-ESR capacitors (e.g., polymer, OS-CON) may have ESR zeros that occur after crossover. Therefore, verify the frequency of the output capacitor's ESR zero:

$$f_{ZERO(ESR)} \approx \frac{1}{2\pi C_{OUT}R_{ESR}}$$

6) Finally, if the output capacitor's ESR zero occurs before crossover, add the parallel compensation capacitor (C_{COMP2}) to form a third pole to cancel this second zero:

$$C_{COMP2} \approx \frac{C_{COMP1}}{\left(2\pi R_{COMP}C_{COMP1}f_{ZERO(ESR)} - 1\right)}$$
$$\approx \frac{C_{COMP1}f_{POLE(OUT)}}{\left(f_{ZERO(ESR)} - f_{POLE(OUT)}\right)}$$

For example, the MAX1964 *Standard Application Circuit* shown in Figure 1 requires a 5V output that supports up to 2A. Using the above compensation guidelines, we can determine the proper component values:

- First, select the crossover frequency to be 1/5th the 200kHz switching frequency.
- Next, determine the total DC loop gain ($A_{V(DC)}$) so you can calculate the series compensation capacitance (C_{COMP1}). Since the applications circuit uses the International Rectifier IRF7101 with an $R_{DS(ON)}$ of 100mΩ, the DC loop gain approximately equals 2480 and C_{COMP1} must be approximately 490pF. Select the closest standard capacitor value of 470pF.
- Determine the location of the output pole ($f_{POLE(OUT)}$). With a 5V output supplying 2A and a 1000µF electrolytic capacitor, the output pole occurs at 64Hz.

- With the output pole's frequency and series compensation capacitor values, the required series resistance can be determined. Based on the above equation, select R_{COMP} = 5.1MΩ.
- Now we must determine if the selected output capacitor's ESR generates a second zero before crossover—the circuit shown in Figure 1 uses a 1000µF 10V Sanyo CZ-series electrolytic capacitor with an ESR rating of 0.2Ω, so the zero occurs at 800Hz. Since crossover occurs at 40kHz, add the second parallel compensation capacitor.
- Finally, the second compensation capacitor value must be approximately 43pF. Select the closest standard capacitor value of 47pF.

Boost-Supply Diode

A signal diode, such as the 1N4148, works well in most applications. If the input voltage goes below 6V, use a small 20mA Schottky diode for slightly improved efficiency and dropout characteristics. Do not use large power diodes, such as the 1N5817 or 1N4001, since high junction capacitance can charge up VL to excessive voltages.

Linear Regulator Controllers

Positive Output Voltage Selection

The MAX1964/MAX1965's positive linear regulator output voltages are set by connecting a voltage divider from the output to FB_ to GND (Figure 6). Select R4 in the 1kΩ to 50kΩ range. Calculate R3 with the following equation:

$$R3 = R4\left[\left(\frac{V_{OUT}}{V_{FB}}\right) - 1\right]$$

where V_{FB} = 1.24V and V_{OUT} may range from 1.24V to 30V.

Negative Output Voltage Selection (MAX1965)

The MAX1965's negative output voltage is set by connecting a voltage divider from the output to FB5 to a positive voltage reference (Figure 6). Select R6 in the 1kΩ to 50kΩ range. Calculate R5 with the following equation:

$$R5 = R6\left(\frac{V_{OUT}}{V_{REF}}\right)$$

where V_{REF} is the positive reference voltage used and V_{OUT} may be set between 0 and -20V.

If the negative regulator is used, the OUT pin must be connected to a voltage supply between 2V and 5V that can source at least 25mA. Typically, the OUT pin is connected to the step-down converter's output. However, if the step-down converter's output voltage is set higher than 5V, OUT must be connected to one of the positive linear regulators with an output voltage between 2V and 5V.

Transistor Selection

The pass transistors must meet specifications for current gain (h_{FE}), input capacitance, collector-emitter saturation voltage, and power dissipation. The transistor's current gain limits the guaranteed maximum output current to:

$$I_{LOAD(MAX)} = \left[I_{DRV} - \left(\frac{V_{BE}}{R_{BE}}\right)\right] h_{FE(MIN)}$$

where I_{DRV} is the minimum 10mA base drive current and R_{BE} (220Ω) is the pullup resistor connected between the transistor's base and emitter. Furthermore, the transistor's current gain increases the linear regulator's DC loop gain (see *Stability Requirements*), so excessive gain will destabilize the output. Therefore, transistors with current gain over 100 at the maximum output current, such as Darlington transistors, are not recommended. The transistor's input capacitance and input resistance also create a second pole, which could be low enough to destabilize the output when heavily loaded.

The transistor's saturation voltage at the maximum output current determines the minimum input-to-output voltage differential that the linear regulator will support. Alternatively, the package's power dissipation could limit the useable maximum input-to-output voltage differential. The maximum power dissipation capability of the transistor's package and mounting must exceed the actual power dissipation in the device. The power dissipated equals the maximum load current times the maximum input-to-output voltage differential:

$$P = I_{LOAD(MAX)}(V_{LDOIN} - V_{OUT}) = I_{LOAD(MAX)}\, V_{CE}$$

Stability Requirements

The MAX1964/MAX1965 linear regulators use an internal transconductance amplifier to drive an external pass transistor. The transconductance amplifier, pass transistor's specifications, the base-emitter resistor, and the output capacitor determine the loop stability. If the output capacitor and pass transistor are not properly selected, the linear regulator will be unstable.

The transconductance amplifier regulates the output voltage by controlling the pass transistor's base current. Since the output voltage is a function of the load

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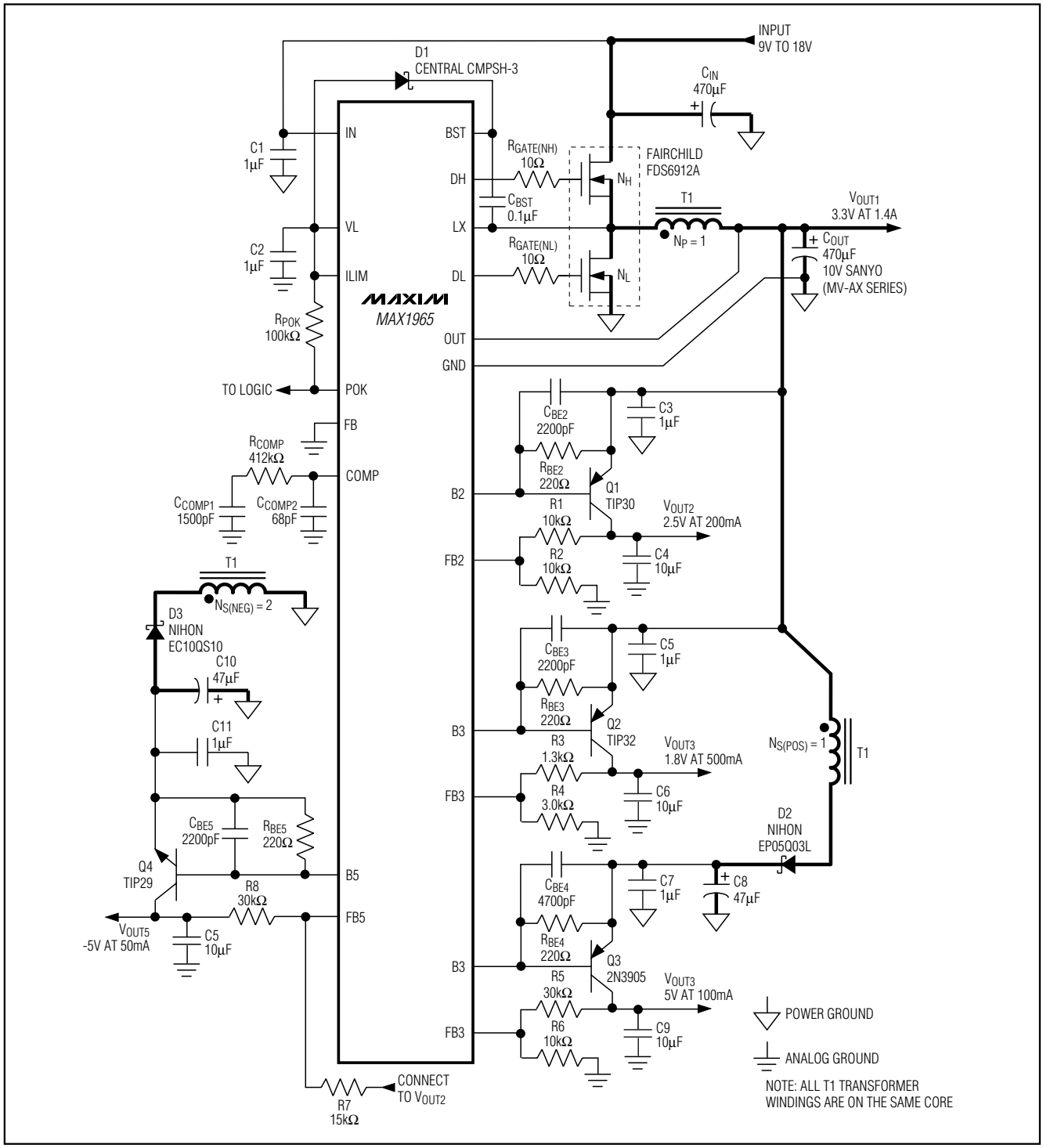


Figure 6. MAX1965 Application Circuit

current and load resistance, the total DC loop gain ($A_{V(LDO)}$) is approximately:

$$A_{V(LDO)} \approx \left(\frac{5.5}{V_T}\right)\left[1+\left(\frac{I_{BIAS}h_{FE}}{I_{LOAD}}\right)\right]V_{REF}$$

where V_T is 26mV, and I_{BIAS} is the current through the base-to-emitter resistor (R_{BE}). This bias resistor is typically 220Ω, providing approximately 3.2mA of bias current.

The output capacitor creates the dominant pole. However, the pass transistor's input capacitance creates a second pole in the system. Additionally, the output capacitor's ESR generate a zero, which may be used to cancel the second pole if necessary. Therefore, in order to achieve stable operation, use the following equations to verify that the linear regulator is properly compensated:

1) First, determine the dominant pole set by the linear regulator's output capacitor and the load resistor:

$$f_{POLE(CLDO)} = \frac{1}{2\pi C_{LDO}R_{LOAD}} = \frac{I_{LOAD(MAX)}}{2\pi C_{LDO}V_{LDO}}$$

unity-gain crossover = $A_{V(LDO)}\, f_{POLE(CLDO)}$

2) Next, determine the second pole set by the base-to-emitter capacitance (including the transistor's input capacitance), the transistor's input resistance, and the base-to-emitter pullup resistor:

$$f_{POLE(CBE)} = \frac{1}{2\pi C_{BE}\left(R_{BE}\left\|R_{IN(BJT)}\right.\right)} = \frac{R_{BE}I_{LOAD} + V_T h_{FE}}{2\pi C_{BE}R_{BE}V_T h_{FE}}$$

3) A third pole is set by the linear regulator's feedback resistance and the capacitance between FB_ and GND (including 20pF stray capacitance).

$$f_{POLE(FB)} = \frac{1}{2\pi C_{FB}\left(R1\left\|R2\right.\right)}$$

4) If the second and third pole occur well after unity-gain crossover, the linear regulator will remain stable:

$$f_{POLE(FB)} \text{ and } f_{POLE(CBE)} > 2f_{POLE(CLDO)}\, A_{V(LDO)}$$

However, if the ESR zero occurs before unity-gain crossover, cancel the zero with $f_{POLE(FB)}$ by changing circuit components such that:

$$f_{POLE(FB)} \approx \frac{1}{\pi C_{OUT}R_{ESR}}$$

Do not use output capacitors with more than 200mΩ of ESR. Typically, more output capacitance provides the best solution, since this also reduces the output voltage drop immediately after a load transient.

Linear Regulator Output Capacitors

Connect at least 1µF capacitor between the linear regulator's output and ground, as close to the MAX1964/MAX1965 and external pass transistors as possible. Depending on the selected pass transistor, larger capacitor values may be required for stability (see *Stability Requirements*). Furthermore, the output capacitor's equivalent series resistance (ESR) affects stability, providing a zero that may be necessary to cancel the second pole. Use output capacitors with an ESR less than 200mΩ to ensure stability and optimum transient response.

Once the minimum capacitor value for stability is determined, verify that the linear regulator's output does not contain excessive noise. Although adequate for stability, small capacitor values may provide too much bandwidth, making the linear regulator sensitive to noise. Larger capacitor values reduce the bandwidth, thereby reducing the regulator's noise sensitivity.

For the negative linear regulator, if noise on the ground reference causes the design to be marginally stable, bypass the negative output back to its reference voltage (V_{REF}, Figure 7). This technique reduces the differential noise on the output.

Base-Drive Noise Reduction

The high-impedance base driver is susceptible to system noise, especially when the linear regulator is lightly loaded. Capacitively coupled switching noise or inductively coupled EMI onto the base drive causes fluctuations in the base current, which appear as noise on the linear regulator's output. Keep the base-drive traces away from the step-down converter and as short as possible to minimize noise coupling. Resistors in series with the gate drivers (DH and DL) reduce the LX switching noise generated by the step-down converter (Figure 5). Additionally, a bypass capacitor may be placed across the base-to-emitter resistor (Figure 7). This bypass capacitor, in addition to the transistor's input capacitance, could bring in a second pole that will destabilize the linear regulator (see *Stability Requirements*). Therefore, the stability requirements determine the maximum base-to-emitter capacitance:

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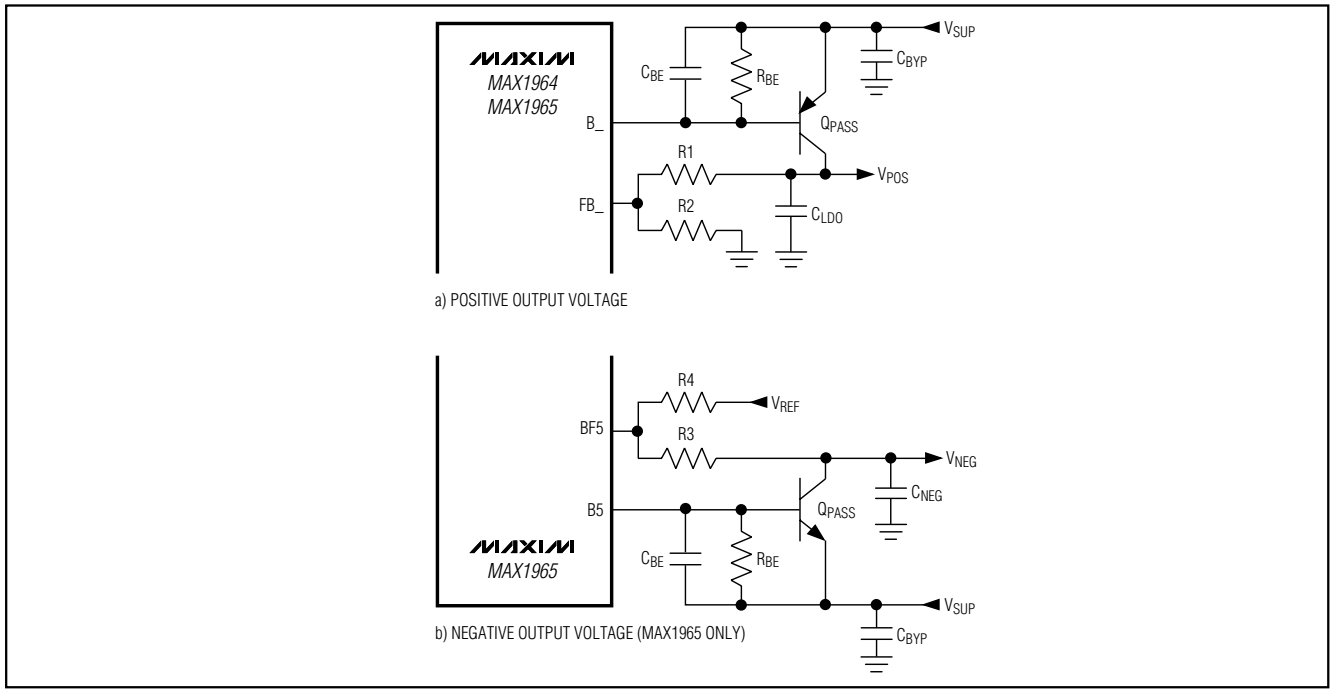


Figure 7. Base-Drive Noise Reduction

$$C_{BE} \le \frac{1}{2\pi f_{POLE(CBE)}} \left(\frac{R_{BE} I_{LOAD} + V_T h_{FE}}{R_{BE} V_T h_{FE}} \right) - C_{IN(Q)}$$

where $C_{IN(Q)}$ is the transistor's input capacitance, and $f_{POLE(CBE)}$ is the second pole required for stability.

Transformer Selection

In systems where the step-down controller's output is not the highest voltage, a transformer may be used to provide additional post-regulated, high-voltage outputs. The transformer generates unregulated, high-voltage supplies which power the positive and negative linear regulators. These unregulated supply voltages are dependent on the transformer's turns ratio – number of secondary turns (N_S) divided by the number of primary turns (N_P). So the transformer must be selected to provide supply voltages high enough to keep the pass transistors from saturating. For positive output voltages, connect the transformer as shown in Figure 6 where the minimum turns ratio ($N_{POS} = N_{S(POS)}/N_P$) is determined by:

$$N_{POS} \ge \left(\frac{V_{LDO(POS)} + V_{SAT} + V_{DIODE}}{V_{OUT}} - 1 \right)$$

where V_{SAT} is the pass transistor's saturation voltage under full load. For negative output voltages (MAX1965 only), connect the transformer as shown in Figure 6 where the minimum turns ratio ($N_{NEG} = N_{S(NEG)}/N_P$) is determined by:

$$N_{NEG} \ge \left(\frac{\left|V_{LDO(NEG)}\right| + V_{SAT} + V_{DIODE}}{V_{OUT}} \right)$$

Since power transfer occurs when the low-side MOSFET is on (DL = high), the transformer cannot support heavy loads with high duty cycles.

Snubber Design

The MAX1964/MAX1965 use current-mode control schemes that sense the current across the high-side MOSFET (N_H). Immediately after the high-side MOSFET turns on, the MAX1964/MAX1965 use a 60ns current-sense blanking period to minimize noise sensitivity. However, when the MOSFET turns on, the transformer's secondary inductance and the diode's parasitic capacitance form a resonant circuit that causes ringing. Reflected back through the transformer to the primary side, these oscillations appear across the high-side MOSFET may last longer than the blanking period. As

shown in Figure 8, a series RC snubber circuit at the diode increases the damping factor, allowing the ringing to settle quickly. Applications with multiple transformer windings require only one snubber circuit on the highest output voltage.

The diode's parasitic capacitance can be estimated using the diode's reverse voltage rating (V_{RRM}), current capability (I_O), and recovery time (t_{RR}). A rough approximation is:

$$C_{DIODE} = \frac{I_0 \times t_{RR}}{V_{RRM}}$$

For the EC10QS10 Nihon diode used in Figure 8, the capacitance is roughly 15pF. The output snubber only needs to dampen the ringing, so the initial turn-on spike that occurs during the blanking period is still present. A 100pF capacitor works well in most applications. Larger capacitance values require more charge, thereby increasing the power dissipation.

The snubber's time constant (t_{SNUB}) must be smaller than the 60ns blanking time. A typical RC time constant of approximately 30ns was chosen for Figure 8:

$$R_{SNUB} = \frac{t_{SNUB}}{C_{SNUB}} = \frac{30ns}{C_{SNUB}}$$

Minimum Load Requirements (Linear Regulators)

Under no-load conditions, leakage currents from the pass transistors supply the output capacitor, even when the transistor is off. Generally, this is not a problem since the feedback resistors' current drain the excess charge. However, charge may build up on the output capacitor over temperature, making V_{LDO} rise above its set point. Care must be taken to ensure that the feedback resistors' current exceeds the pass transistor's leakage current over the entire temperature range.

Applications Information

PC Board Layout Guidelines

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. Follow these guidelines for good PC board layout:

1) Place the power components first, with ground terminals adjacent (NL source, C_{IN}, C_{OUT}). If possible, make all these connections on the top layer with wide, copper-filled areas. Keep these high-current paths short, especially at ground terminals.
2) Mount the MAX1964/MAX1965 adjacent to the switching MOSFETs in order to keep IN-LX current-sense lines, LX-GND current-limit sense lines, and the driver lines (DL and DH) short and wide. The current-sense amplifier inputs are connected between IN and LX, so these pins must be connected as close as possible to the high-side MOSFET. The current-limit comparator inputs are connected between LX and GND, but accuracy is not as important, so give priority to the high-side MOSFET connections. The IN, LX, and GND connections to the MOSFETs must be made using Kelvin sense connections to guarantee current-sense and current-limit accuracy.
3) Group the gate-drive components (BST diode and capacitor, IN bypass capacitor) together near the MAX1964/MAX1965.
4) All analog grounding must be done to a separate solid copper ground plane, which connects to the MAX1964/MAX1965 at the GND pin. This includes the VL bypass capacitor, feedback resistors, compensation components (R_{COMP}, C_{COMP}), and adjustable current-limit threshold resistors connected to ILIM.
5) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the MAX1964/MAX1965 as possible.
6) When trade-offs in trace lengths must be made, it's preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and low-side MOSFET.
7) Route high-speed switching nodes away from sensitive analog areas (B_, FB_, COMP, ILIM).

Regulating High Voltage

The linear regulator controllers can be configured to regulate high output voltages by adding a cascode transistor to buffer the base-drive output. For example, to generate an output voltage between 30V and 60V, add a 2N5550 high-voltage NPN transistor as shown in Figure 9A where VBIAS is a DC voltage between 3V and 20V that can source at least 1mA. R_{DROP} protects the cascode transistor by decreasing the voltage across the transistor when the pass transistor saturates. Similarly, to regulate a negative output voltage between -20V and -120V, add a 2N5401 high-voltage PNP transistor as shown in Figure 9B.

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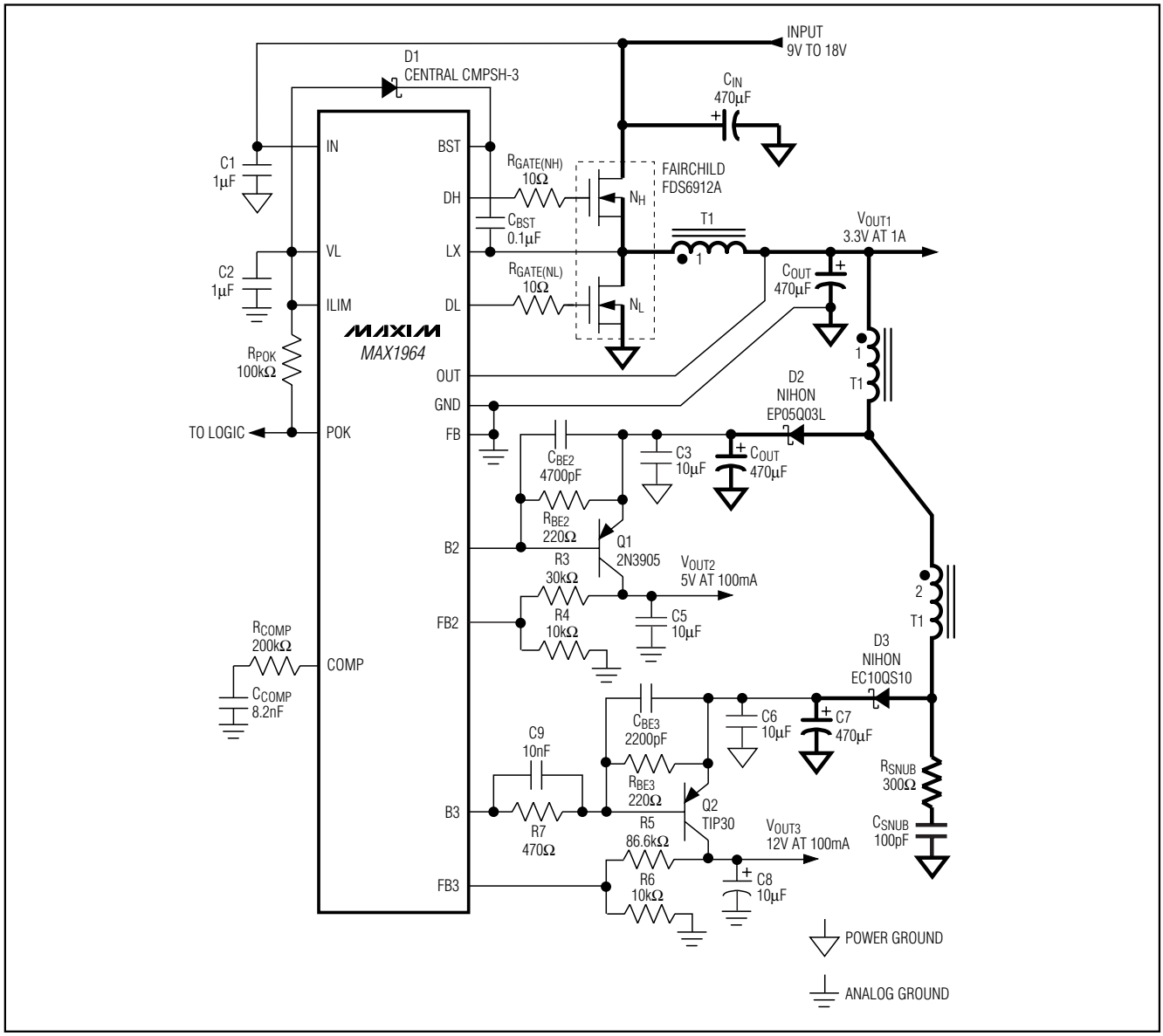


Figure 8. MAX1964 High-Voltage Application Requires Snubber Circuit

Output Filtering for Analog Circuits

Some applications need to generate analog and power outputs at the same voltage. By adding an LC filter to filter the noise present on an analog output (Figure 10), one output voltage can provide both analog and power outputs. The LC filter provides approximately 40dB/decade of attenuation. Select the LC corner frequency ($1/2\ \pi\ \sqrt{LC}$) to provide desired attenuation. For stable operation, the filter inductor (L_{FILTER}) and output filter capacitor (C_{FILTER}) used to generate the filter must be selected to provide an overdamped response to output transients:

$$\frac{(R_{DCR} + R_{ESR})^2 C_{FILTER}}{4L_{FILTER}} \geq 1$$

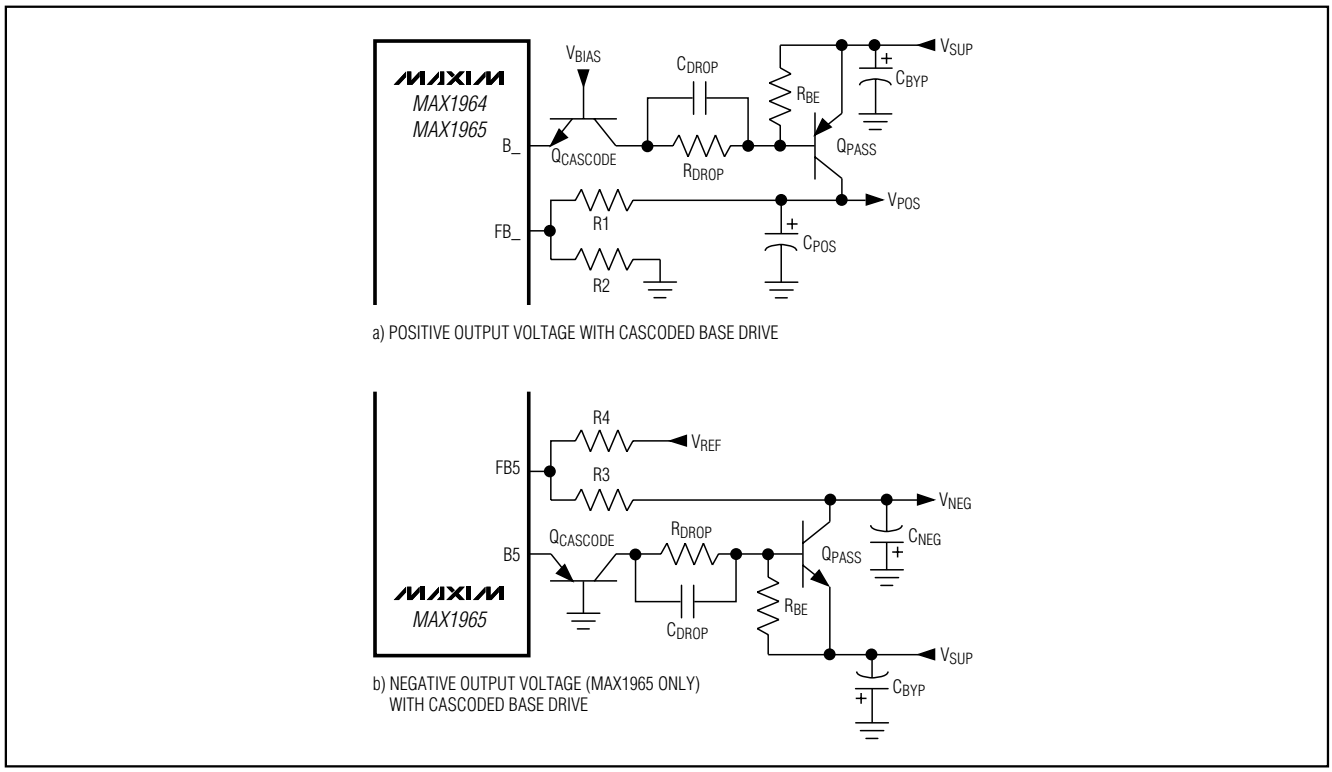


Figure 9. High-Voltage Linear Regulation

where the R_{DCR} is the inductor's DC resistance and R_{ESR} is the output filter capacitor's effective series resistance (ESR). Inductors with high DC resistance will provide poor load regulation but allow the use of smaller filter capacitors:

$$V_{OUT(FILTER)} = V_{OUT(NOMINAL)} - R_{DCR}I_{OUT}$$

Therefore, power chokes are ideal for these applications due to their high inductance values, high saturation current ratings, and low resistance.

Chip Information

TRANSISTOR COUNT: 1617

PROCESS: BiCMOS

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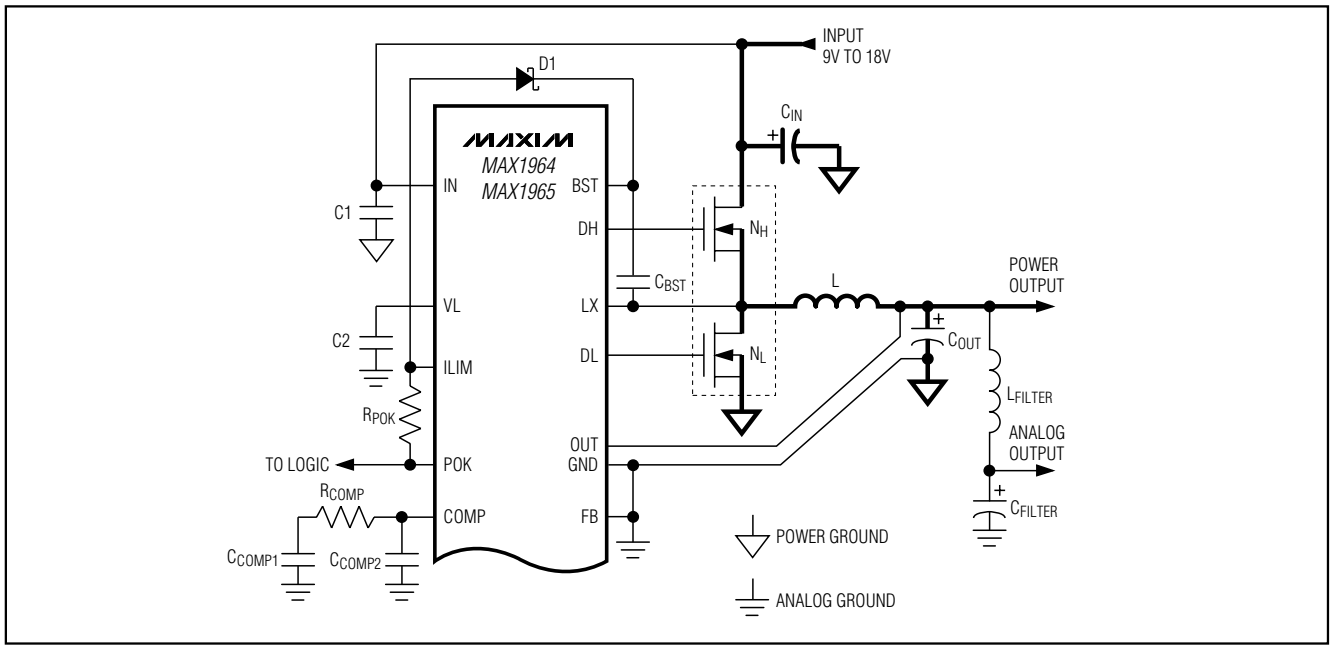
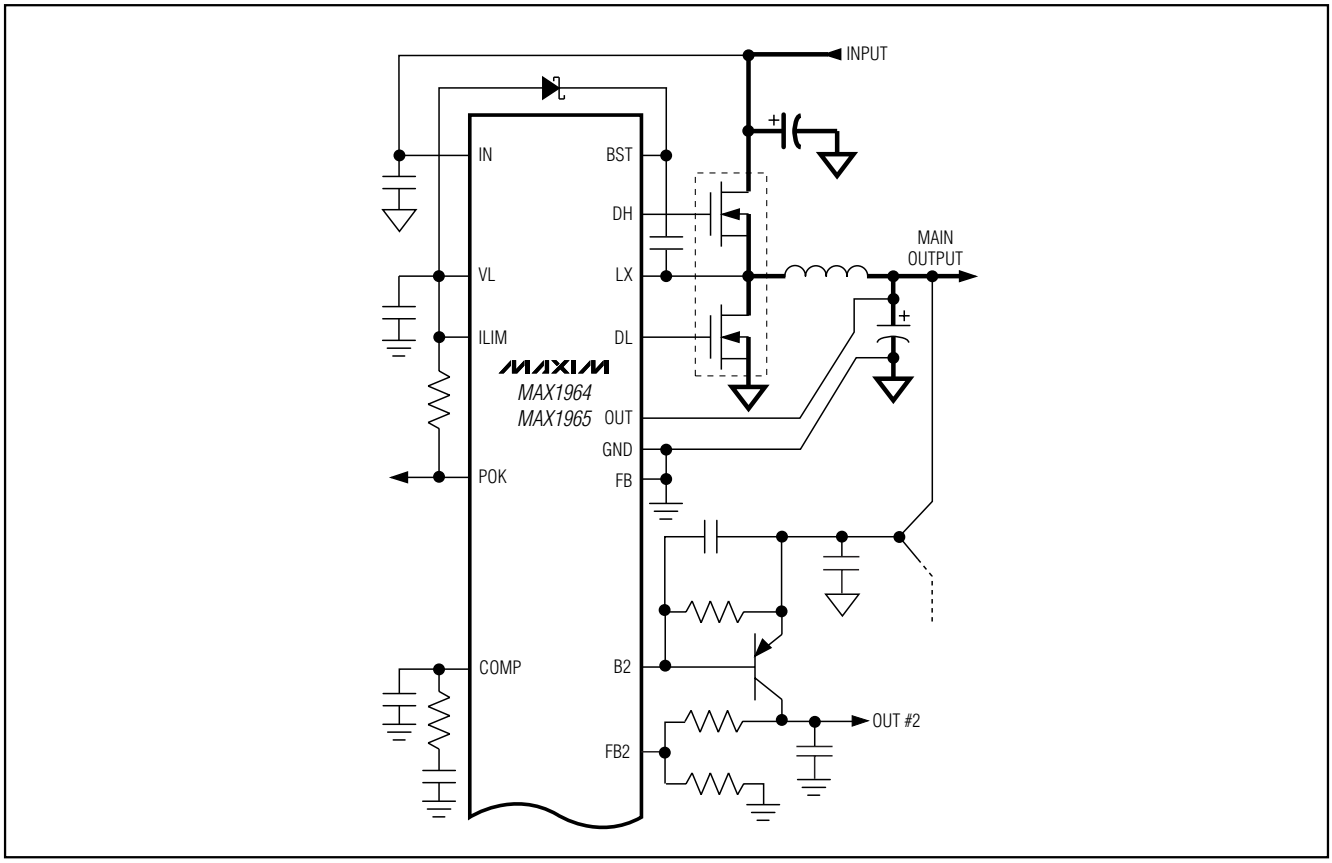


Figure 10. Filtered Output for Analog Circuits

Table 1. Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
INDUCTORS & TRANSFORMERS			
Coilcraft	847-639-6400	847-639-1469	www.coilcraft.com
Coiltronics	561-241-7876	561-241-9339	www.coiltronics.com
ICE Components	800-729-2099	800-729-2099	www.icecomponents.com
Sumida USA	847-956-0666	847-956-0702	www.sumida.com
Toko	847-297-0070	847-699-1194	www.tokoam.com
CAPACITORS			
AVX	803-946-0690	803-626-3123	www.avxcorp.com
Kemet	408-986-0424	408-986-1442	www.kemet.com
Panasonic	847-468-5624	847-468-5815	www.panasonic.com
Sanyo	619-661-6835	619-661-1055	www.secc.co.jp
Taiyo Yuden	408-573-4150	408-573-4159	www.t-yuden.com
DIODES			
Central Semiconductor	516-435-1110	516-435-1824	www.centralsemi.com
International Rectifier	310-322-3331	310-322-3332	www.irf.com
Nihon	847-843-7500	847-843-2798	www.niec.co.jp
On Semiconductor	602-303-5454	602-994-6430	www.onsemi.com
Zetex	516-543-7100	516-864-7630	www.zetex.com

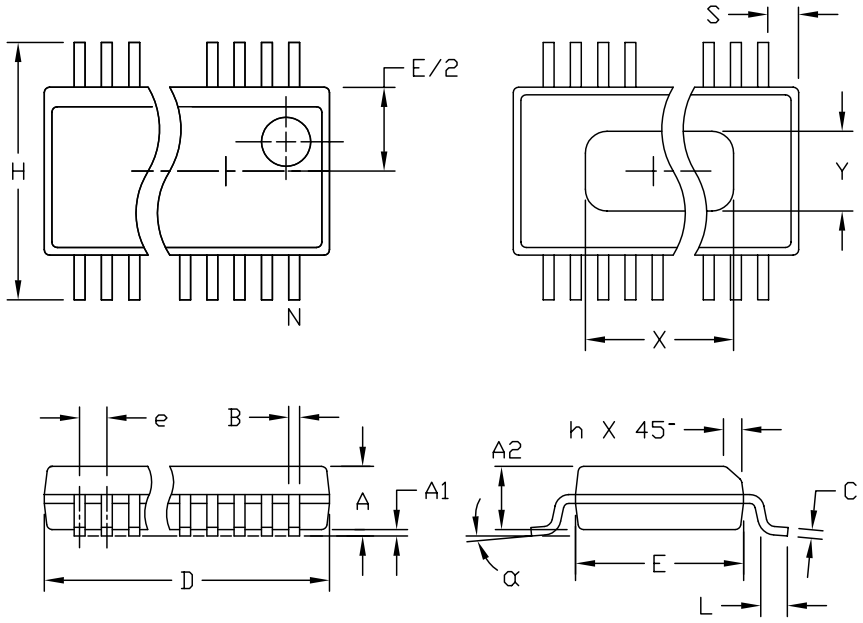
Typical Operating Circuit



Tracking/Sequencing Triple/Quintuple Power-Supply Controllers

Package Information

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.
5. MEETS JEDEC MO137.

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	C	1/1

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