MAXIM

Triplexed LCD Decoder/Drivers

General Description

The MAX7231/32/33/34 family of integrated circuits is a complete line of triplexed liquid crystal display (LCD) drivers. These devices interface microprocessors (or digital systems) to multiplexed numeric and alphanumeric displays. The MAX7231 drives 8 digits and accepts data in a parallel format. The MAX7232 drives 10 digits and accepts data in a serial format. Both devices feature two independent annunciators per digit. The MAX7233 drives 4 alphanumeric 18 segment characters. The MAX7234 drives 5 alphanumeric 18 segment characters.

Each device includes an input buffer, digit address decoding circuitry and mask-programmed ROM allowing six bits of input data to be decoded into 64 independent combinations of the output segments of each digit. This offloads the microprocessor system, reducing the ROM space and CPU time needed to service a display.

Applications

These low-power LCD drivers are ideal for microprocessor-based portable applications where power consumption is a primary concern. Many applications also take advantage of the annunciator drive capability, which allows unlimited variations of display layout.

Portable instrumentation
Industrial equipment
Telecommunications
Medical equipment
Panel Meters
Machine control

Features

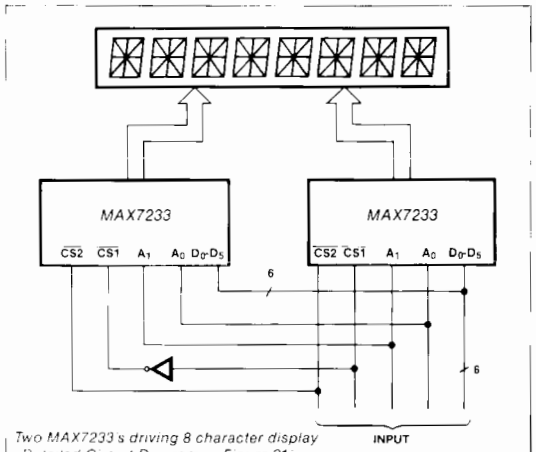
- **MAX7231 drives 8 digits/7 segments; parallel input format; 2 annunciators per digit**
- **MAX7232 drives 10 digits/7 segments; serial input format; 2 annunciators per digit**
- **MAX7233 drives 4 alphanumeric characters/ 18 segments; parallel input format**
- **MAX7234 drives 5 alphanumeric characters/ 18 segments; serial input format**
- **On-chip oscillator**
- **Direct interface to microprocessors**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX7231AFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7231BFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7231CFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7232AFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7232BFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7232CFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7233AFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7233BFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7234AFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7234BFIPL	-20°C to +85°C	40 Lead Plastic DIP

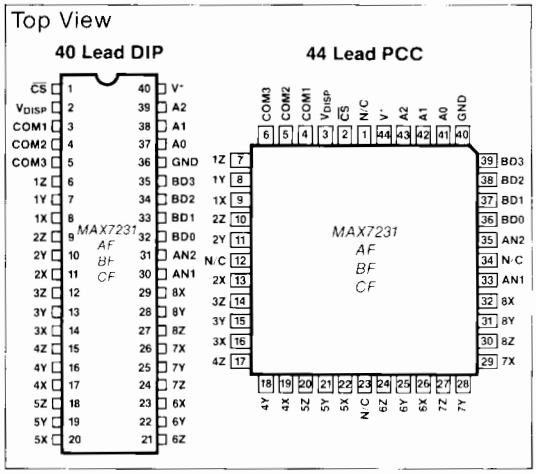
Ordering information continued on next page

Typical Operating Circuit



Two MAX7233's driving 8 character display (Detailed Circuit Diagram — Figure 21)

Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

Triplexed LCD Decoder/Drivers

OPTION TABLE

DEVICE	OUTPUT CODE	ANNUNCIATOR LOCATIONS	INPUT	OUTPUT
MAX7231AF MAX7231BF MAX7231CF	Hexdecimal Code B Code B	Both Annunicators on COM3 1 Annunciator COM1 1 Annunciator COM3	Parallel Entry 4 bit Data 2 bit Annunciators 3 bit Address	8 Digits plus 16 Annunciators
MAX7232AF MAX7232BF MAX7232CF	Hexadecimal Code B Code B	Both Annunciators on COM3 1 Annunciator COM1 1 Annunciator COM3	Serial Entry 4 bit Data 2 Bit Annunciators 4 bit Address	10 Digits plus 20 Annunciators
MAX7233AF	64 Character (ASCII) 18 Segment (Half width numbers)	No independent Annunciators	Parallel Entry 6 bit (ASCII) Data 2 bit Address	Four Characters
MAX7233BF	64 Character (ASCII) 18 Segment (Full width numbers)	No Independent Annunciators	Parallel Entry 6 bit (ASCII) Data 2 bit Address	Four Characters
MAX7234AF	64 Character (ASCII) 18 Segment (Half width numbers)	No Independent Annunciators	Serial Entry 6 bit (ASCII) Data 3 bit Address	Five Characters
MAX7234BF	64 Character (ASCII) 18 Segment (Full width numbers)	No Independent Annunciators	Serial Entry 6 bit (ASCII) Data 3 bit Address	Five Characters

Ordering Information

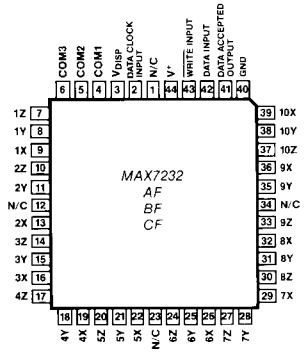
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PART	TEMP. RANGE	PACKAGE
MAX7231AFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7231BFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7231CFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7232AFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7232BFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7232CFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7233AFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7233BFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7234AFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7234BFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier

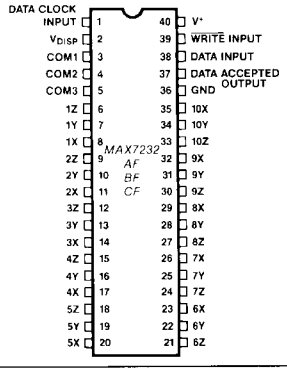
Pin Configuration

Top View

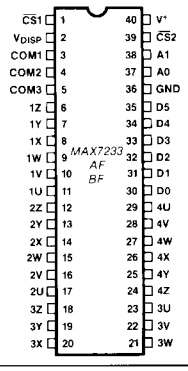
44 Lead PCC



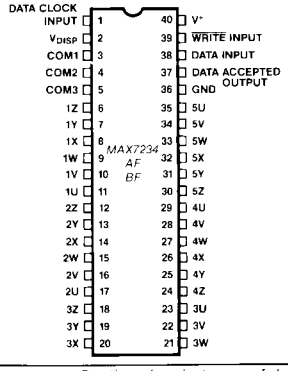
40 Lead DIP



40 Lead DIP



40 Lead DIP



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ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5 W @ 85°C
Supply Voltage (V^+) 6.5V
Input Voltage (Note 2) ..... $-0.3V \le V_{IN} \le 6.5V$
Display Voltage (Note 2) ..... $-0.3V$ to $V^+ + 0.3V$
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Soldering Temperature (10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not limited. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($V^+ = +5V \pm 10\%$, $T_A = -20°C$ to $+85°C$ unless noted)

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION		MIN	TYP	MAX	UNITS
Power Supply Voltage	V^+			4.5		5.5	V
Data Retention Supply Voltage	V^+	Guaranteed Retention at 2V		2	1.6		V
Logic Supply Current	I^+	Current from V^+ to Ground excluding Display, $V_{DISP} = 2V$			30	100	µA
Shutdown Total Current	I_S	V_{DISP} Pin 2 Open, $T_A = +25°C$			1	10	µA
Display Voltage Range	V_{DISP}	Ground $\le V_{DISP} \le V^+$		0		V^+	V
Display Voltage Setup Current	I_{DISP}	$V_{DISP} = (V^+ - 3V)$, Current from V^+ to V_{DISP} On-Chip (Note 3), $T_A = +25°C$			15	25	µA
Display Voltage Setup Resistor Value	R_{DISP}	One of Three Identical Resistors in String (Note 3), $T_A = +25°C$		40	75		kΩ
DC Component of Display Signals		Sample Test only, $V_{DISP} = 0V$			1/4	1	% (V^+-V_{DISP})
Display Frame Rate	f_{DISP}	See Figure 2, $T_A = +25°C$		60	90	120	Hz
Input Low Level (Note 3)	V_{IL}	MAX7231, MAX7233	MAX7232, MAX7234			0.8	V
Input High Level (Note 3)	V_{IH}	Pins 1, 30-35, 37-39	Pins 1, 38, 39	2.0			V
Input Leakage	I_{ILK}	MAX7231, MAX7233	MAX7232, MAX7234		0.1	1	µA
Input Capacitance	C_{IN}	Pins 1, 30-35, 37-39	Pins 1, 38, 39		5		pF
Output Low Level	V_{OL}	Pin 37, MAX7232, MAX7234, $I_{OL} = 1mA$,				0.4	V
Output High Level	V_{OH}	$V^+ = 4.5V$, $I_{OH} = -500µA$		4.1			V

AC CHARACTERISTICS ($V^+ = 5V$, $T_A = 25°C$, 0-3V INPUT SWINGS) PARALLEL INPUT (MAX7231, MAX7233) See Figure 5

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN	TYP	MAX	UNITS
Chip Select Pulse Width	t_{cs}		500	350		ns
Address/Data Setup Time	t_{ds}		350			ns
Address/Data Hold Time	t_{dh}		0	-20		ns
Inter-Chip Select Time	t_{ics}		3.5			µs

AC CHARACTERISTICS 0-3V INPUT SWINGS SERIAL INPUT (MAX7232, MAX7234) See Figures 6, 7, 8

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN	TYP	MAX	UNITS
Data Clock Low Time	t_{cl}		350			ns
Data Clock Period	t_{cl}		1			µs
Data Setup Time	t_{ds}		350			ns
Data Hold Time	t_{dh}		0	-20		ns
Write Pulse Width	t_{wp}		500	350		ns
Write Pulse to Clock at Initialization	t_{wll}		4.0			µs
Data Accepted Low Output Delay	t_{odl}				1	µs
Data Accepted High Output Delay	t_{odh}			1.5	3	µs
Write Delay After Last Clock	t_{cws}		350			ns

Note 1: This limit refers to that of the package and will not be obtained during normal operation.
Note 2: Due to the SCR structure inherent in these devices, connecting any display terminal or the display voltage terminal to a voltage outside the power supply to the chip may cause destructive device latchup. The digital inputs should never be connected to a voltage less than -0.3 volts below ground, but may be connected to voltages above V^+ but not more than 6.5 volts above GND.
Note 3: $V^+ = 5V$, $T_A = +25°C$.

Triplexed LCD Decoder/Drivers

TERMINAL DEFINITIONS

MAX7231 PARALLEL INPUT NUMERIC DISPLAY

TERMINAL	PIN NO.	DESCRIPTION		FUNCTION	
AN1 AN2	30 31	Annunciator 1 Control Bit Annunciator 2 Control Bit		High = ON Low = OFF	See Table 1
BD0 BD1 BD2 BD3	32 33 34 35	Least Significant Most Significant	4 Bit Binary Data Inputs	Input Data (See Table 2)	HIGH = Logical One (1) LOW = Logical Zero (0)
A0 A1 A2	37 38 39	Least Significant Most Significant	3 Bit Digit Address Inputs	Input Address (See Table 4)	
$\overline{CS}$	1	Data Input Strobe/Chip Select (Note 3)		Trailing (Positive going) edge latches data, causes data input to be decoded and sent out to addressed digit	

Note 3: CS has a special "mid-level" sense circuit that establishes a test mode if it is held near 3V for several msec. Inadvertent triggering of this mode can be avoided by pulling it high when inactive, and driving it with fast rise and fall times.

MAX7233 PARALLEL INPUT ALPHA DISPLAY

TERMINAL	PIN NO.	DESCRIPTION		FUNCTION	
D0 D1 D2 D3 D4 D5	30 31 32 33 34 35	Least Significant Most Significant	6 Bit (ASCII) Data Inputs	Input Data (See Table 3)	HIGH = Logical One (1) LOW = Logical Zero (0)
A0 A1	37 3	Least Significant Most Significant	Address Inputs	Input Add. (See Table 5)	
$\overline{CS}1$ $\overline{CS}2$	39 1	Chip Select Inputs (Note 3)		Both Inputs LOW, load data into input latches. Rising edge of either input causes data to be latched, decoded and sent out to addressed character.	

MAX7232 and MAX7234 SERIAL DATA AND ADDRESS INPUT

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION
Data Input	38	Data + Address Shift Register Input	HIGH = Logical One (1) LOW = Logical Zero (0)
$\overline{WRITE}$ Input	39	Decode, Output, and Reset Strobe	When DATA ACCEPTED Output is LOW, positive going edge of WRITE causes data in shift register to be decoded and sent to addressed digit, then shift register and control logic is reset. When DATA ACCEPTED Output is HIGH, positive going edge of WRITE triggers reset only.
Data Clock Input	1	Data Shift Register and Control Logic Clock	Positive going edge advances data in shift register. MAX7232: Eleventh edge resets shift register and control logic. MAX7234: Tenth edge resets shift register and control logic.
DATA ACCEPTED Output	37	Handshake Output	Output LOW when correct number of bits entered into shift register; MAX7232: 8, 9 or 10 bits. MAX7234: 9 bits.

ALL DEVICES

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION
Display Voltage V_{DISP}	2	Negative end of on-chip resistor string used to generate intermediate voltage levels for display. Shutdown Input.	Display voltage control. When open (or less than 1V from V^+) chip is shutdown; oscillator stops, all display pins to V^+.
Common Line Driver Outputs	3,4,5		Drive display commons, or rows.
Segment Line Driver Outputs	6-29 6-35	(On MAX7231/33) (On MAX7232/34)	Drive display segments, or columns.
V^+	40	Positive Supply	
GND	36	Ground	

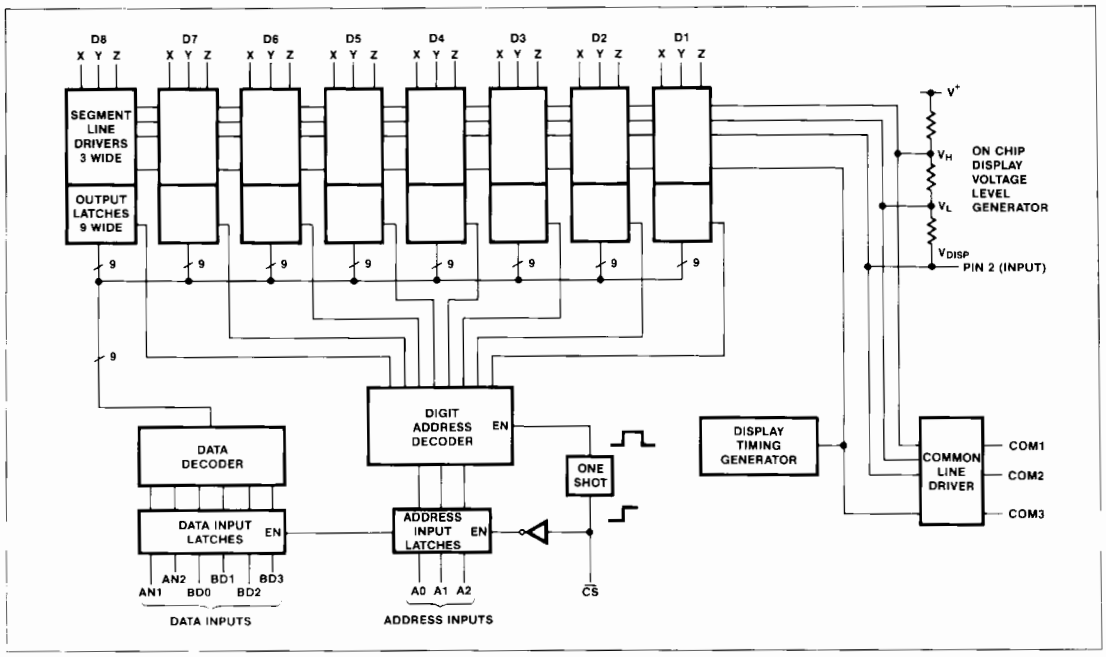


Figure 1. Block Diagram of MAX7231.

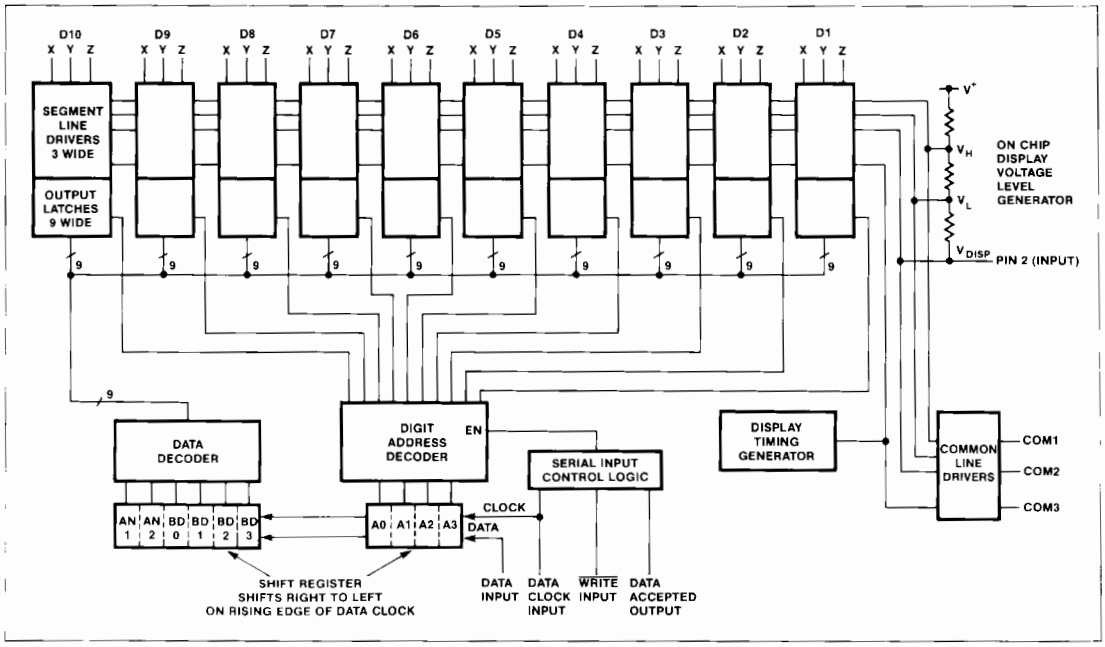


Figure 2. Block Diagram of MAX7232

Triplexed LCD Decoder/Drivers

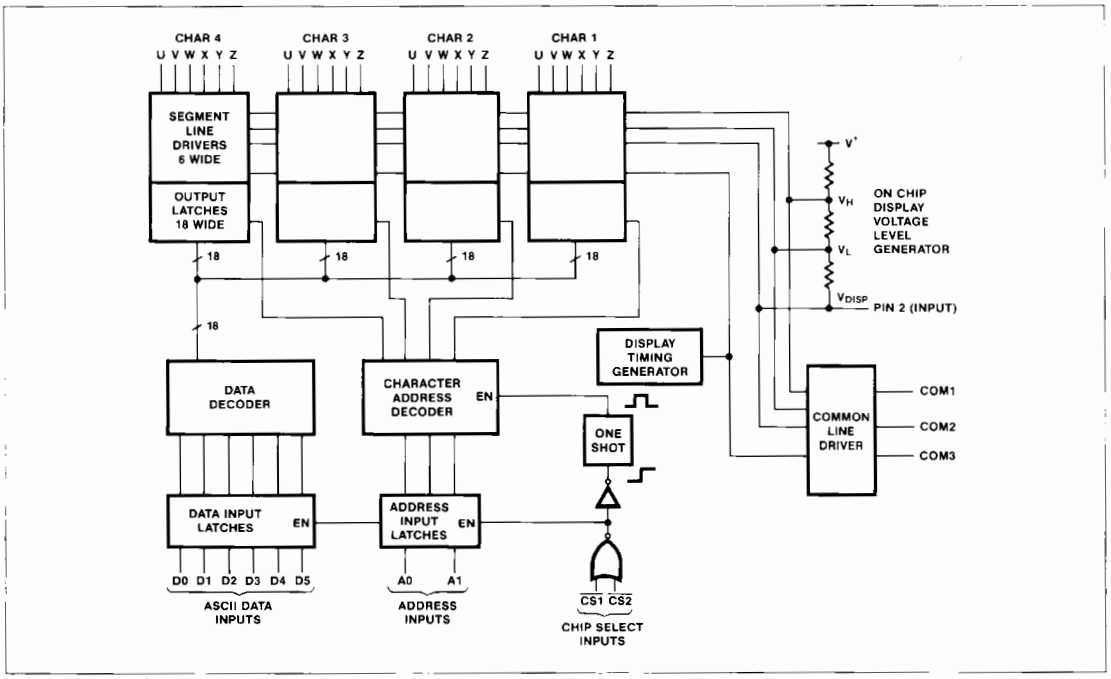


Figure 3. Block Diagram of MAX7233

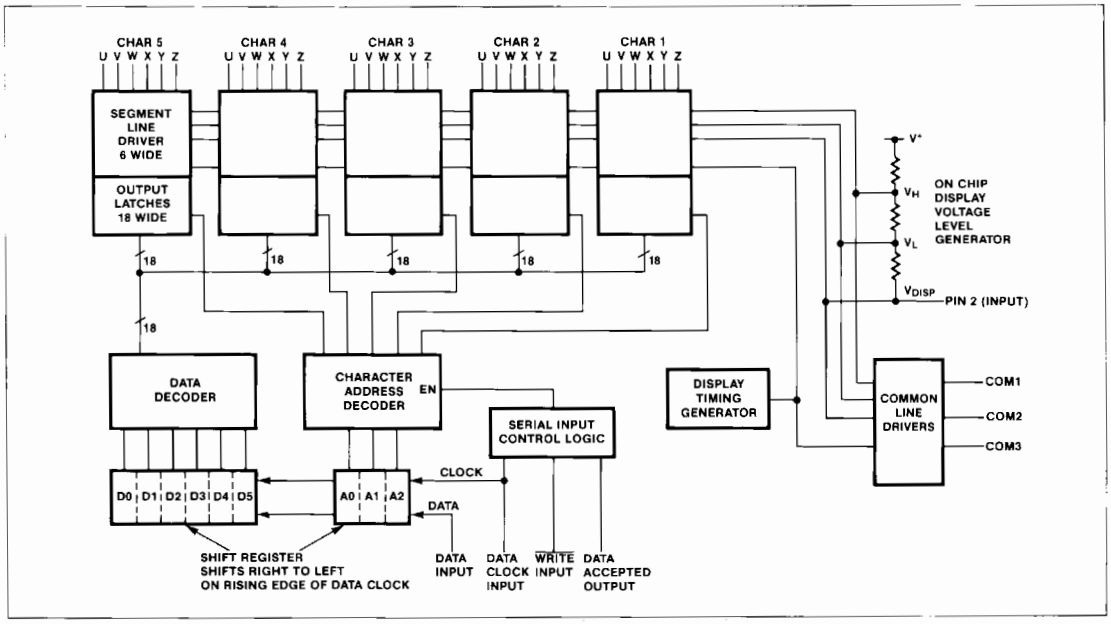


Figure 4. Block Diagram of MAX7234

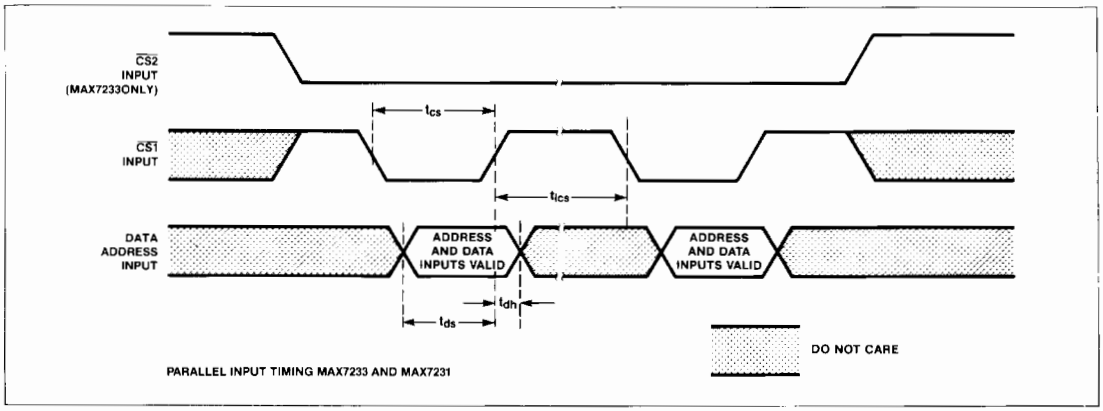


Figure 5. Parallel Input Timing

Detailed Description

Parallel Input Interface

The MAX7231 and MAX7233 have a parallel interface allowing direct parallel connection to microprocessors. The address and data bits are latched on the positive going edge of the Chip Select. The positive going edge of Chip Select also triggers an internal monostable that enables the address decoder and latches the decoded data into the digit/character output latches.

Figure 5 shows the timing requirements for the parallel input devices (7231 and 7233). To ensure that the new data does not appear at the decoder inputs before the previous decoded data is written to the outputs, there is a minimum time required between CHIP SELECT pulses.

Serial Input Interface

A $\overline{\text{WRITE}}$ pulse while Data Accepted Output is high will reset the serial input control logic, but will not latch any data. A $\overline{\text{WRITE}}$ pulse while Data Accepted Output is low will cause the MAX7232 and MAX7234 to decode the data, latch the data into the output latches and then reset the serial input control logic.

This assures that each data bit will be entered into the correct position in the shift register, depending on the subsequent data clock inputs. The MAX7232's Data Accepted Output goes low after 8 Data Clock pulses, whereas the MAX7234's Data Accepted Output goes low after 9 Data Clock Inpulses. Further Data Clock pulses occuring before a $\overline{\text{WRITE}}$ pulse will cause the Data Accepted Output to go high after 11 Data Clock pulses in the MAX7232 and the 10 Data Clock pulses in the MAX7234. In both cases, the serial input control logic is also reset when Data Accepted goes high.

The serial input timing diagram shown in Figure 6 illustrates the recommended procedure for entering data.

Note that the eleventh clock resets the shift register and control logic for the MAX7232, but the Data Accepted Output goes low after the eighth clock. As Figure 7 illustrates, this allows the user to reduce the data to eight bits. The MAX7232 then writes to the 7 segment display, but leaves the annunciators off. Nine Bits are clocked in if only AN2 is turned on.

The control logic of the MAX7234 is similar to the MAX7232, but nine bits are always required. As illustrated in Figure 8, the data bits are only latched if the $\overline{\text{WRITE}}$ input occurs after the ninth data bit has been entered and Data Accepted Output is low.

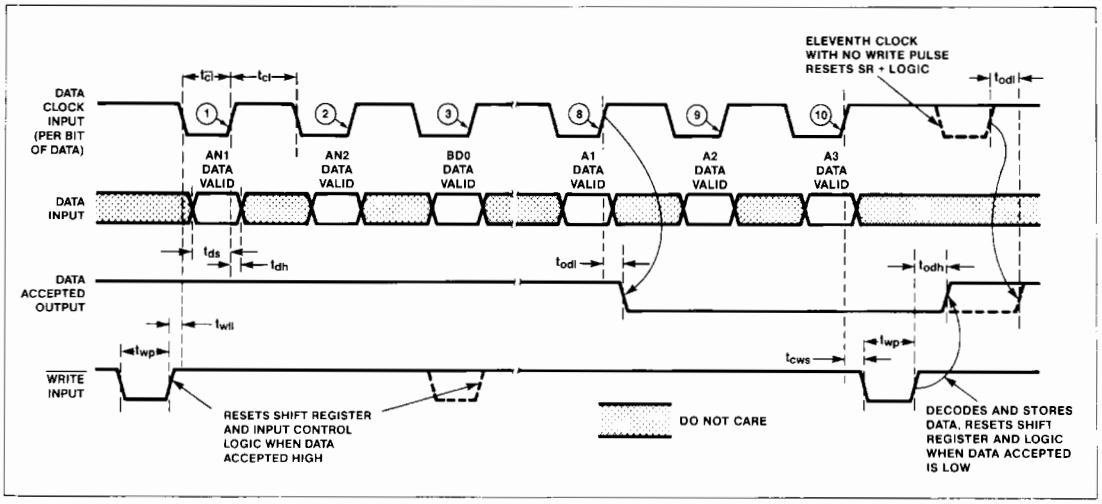


Figure 6. One Digit Timing Diagram for the MAX7232, Writing Both Annunciators.

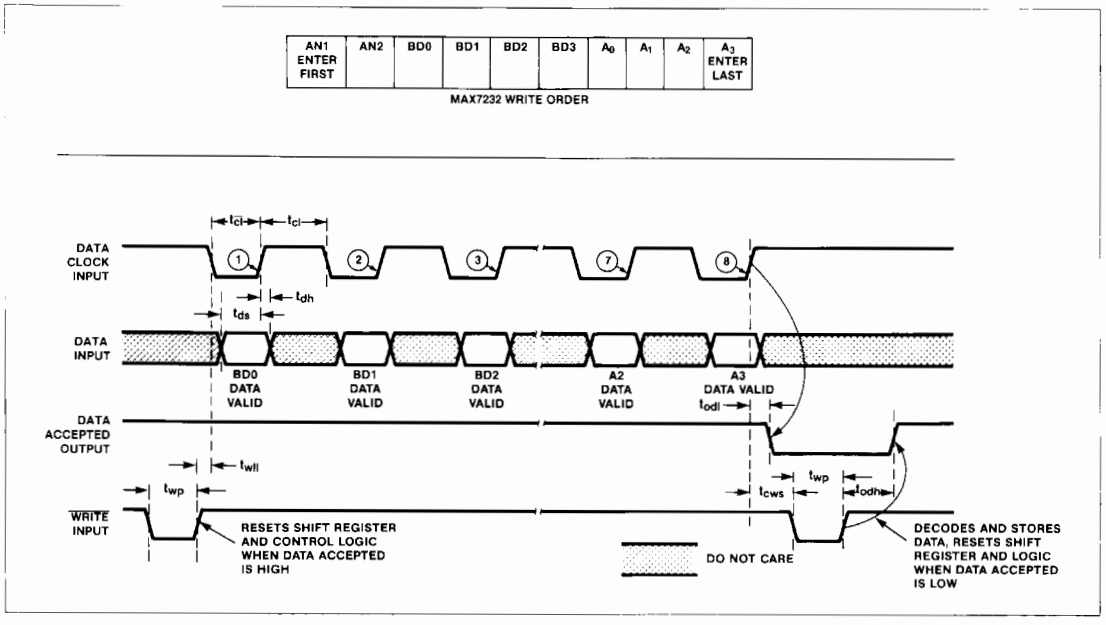


Figure 7. Input Timing Diagram of the MAX7232. Both Annunciators OFF.

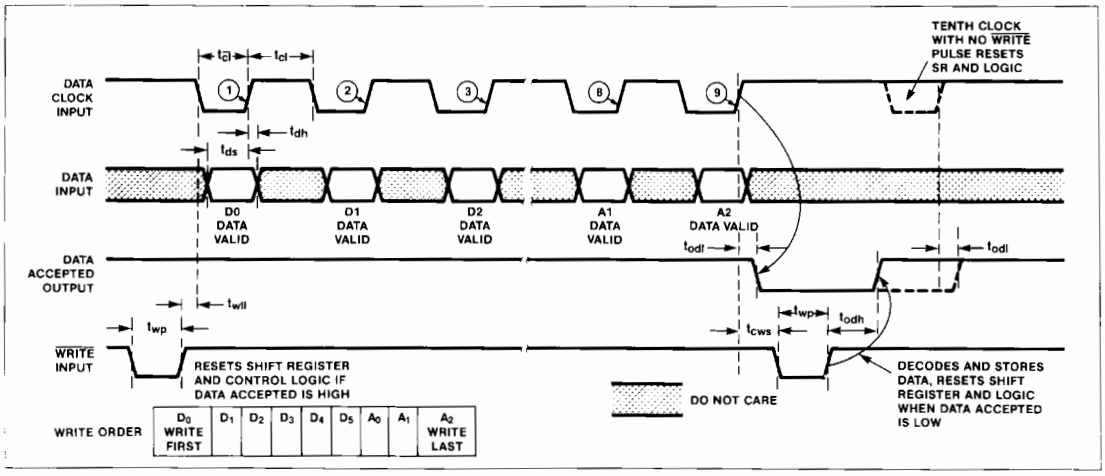


Figure 8. One Character Input Timing Diagram of the MAX7234.

Temperature Compensation

Temperature Effects

Temperature affects the performance of liquid crystal displays (LCD's) in two ways. As the display temperature drops, the response time of the display becomes longer. At very low temperatures, some displays may take several seconds to change to a new character. However, high-speed liquid crystal materials are available for low temperature environments.

Temperature has a significant effect on the variation of liquid crystal threshold voltage. The peak voltage (V_P) required to turn on the display has a temperature coefficient of -7 to -14 mV/°C for typical liquid crystal materials used in multiplexed LCD's. This means that as the temperature increases, the threshold voltage decreases. Figure 9 illustrates the dependence of peak voltage (V_P) on temperature for the same liquid crystal material described in Figure 10. Assuming a fixed value for V_P, OFF segments begin to be visible when the threshold voltage drops below $V_P/3$. To avoid this problem at high temperature, V_P may be set at a fixed voltage chosen to make the RMS OFF voltage, $V_P/3$, just below the threshold voltage at the highest temperature expected. This is appropriate where display temperatures do not vary widely.

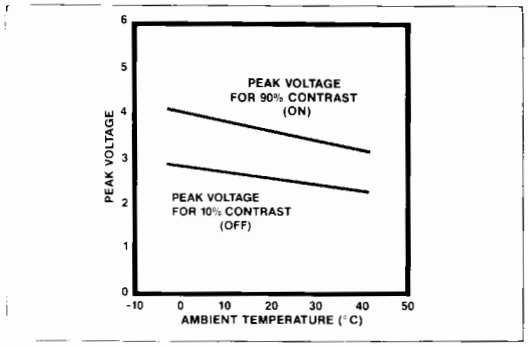


Figure 9. Temperature Dependence of Liquid Crystal Threshold.

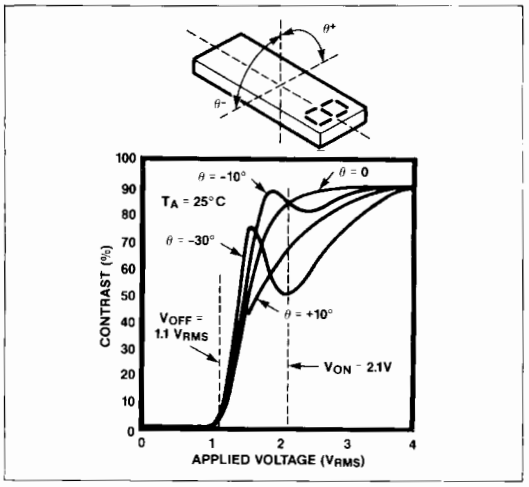


Figure 10. Applied RMS Voltage vs. Contrast.

Triplexed LCD Decoder/Drivers

Display Voltage

An internal resistor string of three equal value resistors is used to generate the display drive voltages. One end of the string is available at Pin 2 (V_{DISP}) and the other end is connected to V^+ on the chip. Pin 2, the user's input, allows the display voltage to be optimized for a particular liquid crystal material. Note that V_P should be three times the threshold voltage for the liquid crystal material used ($V_P = V^+ - V_{DISP}$). To avoid device latchup and possible destruction of the chip, never drive Pin 2 below Ground or above V^+.

Figure 11 illustrates a simple method of generating a display voltage suitable for a particular display. A potentiometer with a maximum value of 200kΩ connected from Pin 2 to Ground gives sufficient range adjustment to suit most displays. Due to the positive temperature coefficient of the resistors on-chip, this method for generating display voltage should be used only in applications where the temperature variation of the chip and display will not vary more than ±5°C (15°F). The power supply voltage also effects the display voltage.

The chip may be operated at the display voltage with V_{DISP} connected to Ground in battery powered applications where the display voltage is the same as the battery voltage (typically 3 to 4.5 volts). The inputs of the chip are designed such that they may be driven above V^+ without damage. This allows the chip and display to operate at a regulated 3V while its inputs are driven by a microprocessor that is operating at a less well controlled 5V supply. Under no circumstances should the inputs be driven more than 6.5V above Ground. Independent adjustment of both voltage and temperature compensation is illustrated in Figure 12. Temperature compensation is performed by the ICL7663.

Another method of setting up a display voltage is illustrated in Figure 13. The five diodes (1N914 or equivalent), each have a forward drop of approximately 0.65V, with 20 (μA) at room temperature. This configuration is suitable for the 3V display using the material properties as shown in Figures 9 and 10. More diodes may be added for higher voltage displays. Each diode has a negative temperature coefficient of -2mV/°C (5 in series gives -10mV/°C). Consequently, this circuit will provide reasonable temperature compensation.

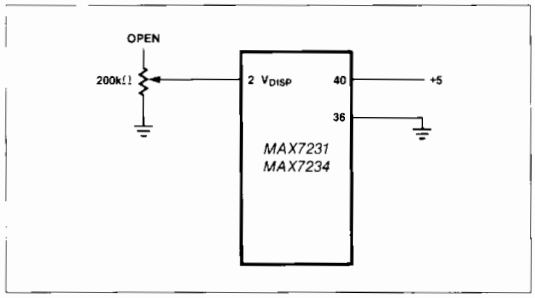


Figure 11. Simple Display Voltage Adjustment.

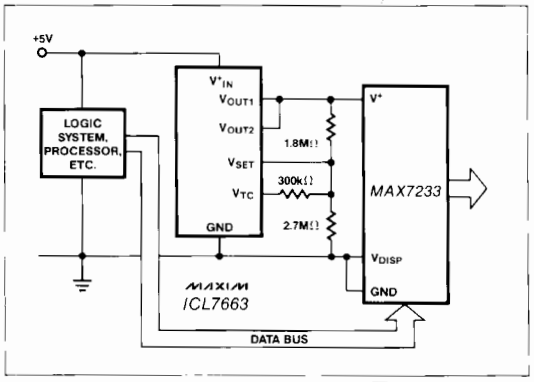


Figure 12. Flexible Temperature Compensation.

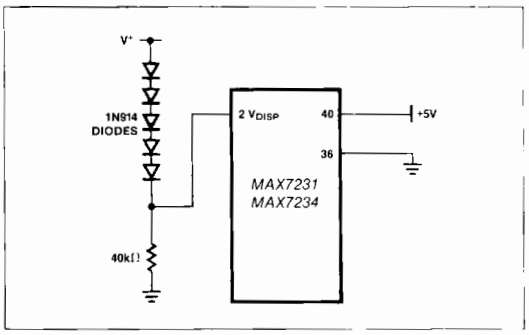


Figure 13. Diode String VDISP Generator.

Triplexing

The connection diagram for a typical 7-segment display font with 2 annunciators is illustrated in Figure 15. The MAX7231 and MAX7232 (A and B suffix versions) numeric display drivers use this configuration. The voltage waveforms of the common lines and one segment line are illustrated in Figure 14. The "Y" segment line has been chosen as an example. This line intersects with COM1 to form the "A" segment, COM2 to form the "G" segment, and COM3 to form the "D" segment. Four different ON/OFF combinations of the "A", "G" and "D" segments and their corresponding waveforms of the "Y" segment line are illustrated in Figure 14. The schematic diagram in Figure 16 shows that each intersection acts as a capacitance from segment line to common line. Figure 17 illustrates the voltage across the "G" segment for the same four combinations of ON/OFF segments shown in Figure 14.

The RMS voltage across the segment determines the degree of polarization for the liquid crystal material and thus the contrast of the segment. The

RMS OFF voltage is always VP/3, whereas the RMS ON voltage is always 1.92 VP/3. This is illustrated in Figure 17. The ratio of RMS ON to OFF voltage is fixed at 1.92 for a triplexed liquid crystal display.

Contrast vs. applied RMS voltage is shown in Figure 10. With a VP of 3.1V, the RMS ON voltage is 2.1V and the RMS OFF voltage is 1.1V. The OFF segment will have a contrast of less than 5%, while the ON segments will have greater than 85% contrast.

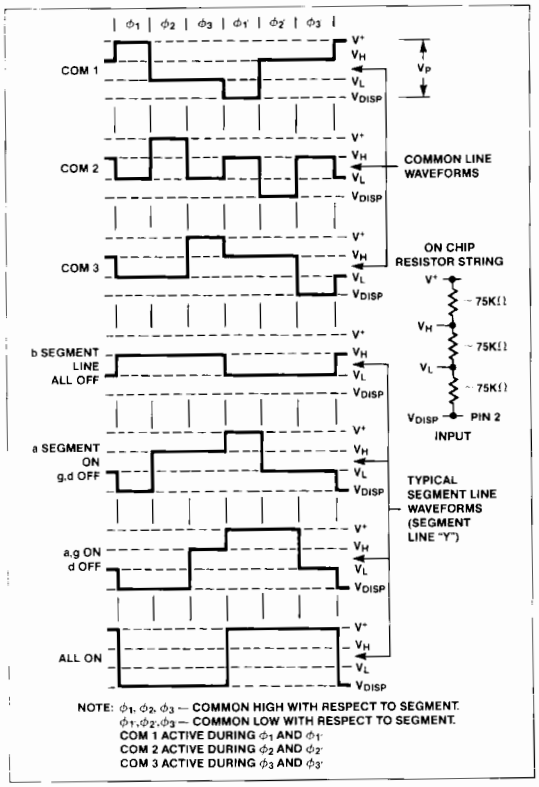


Figure 14. Display Voltage Waveforms.

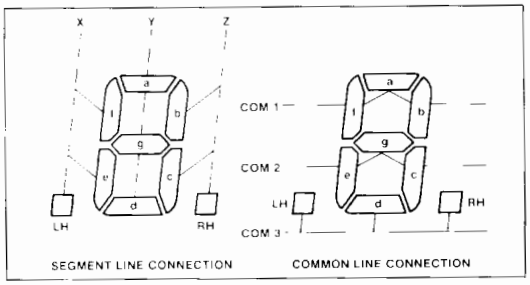


Figure 15. Connection Diagrams for Typical 7-Segment Displays.

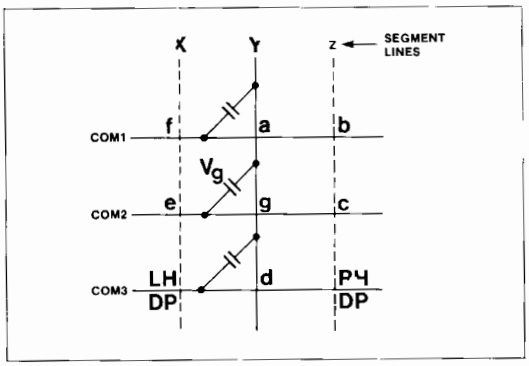


Figure 16. Schematic of Display.

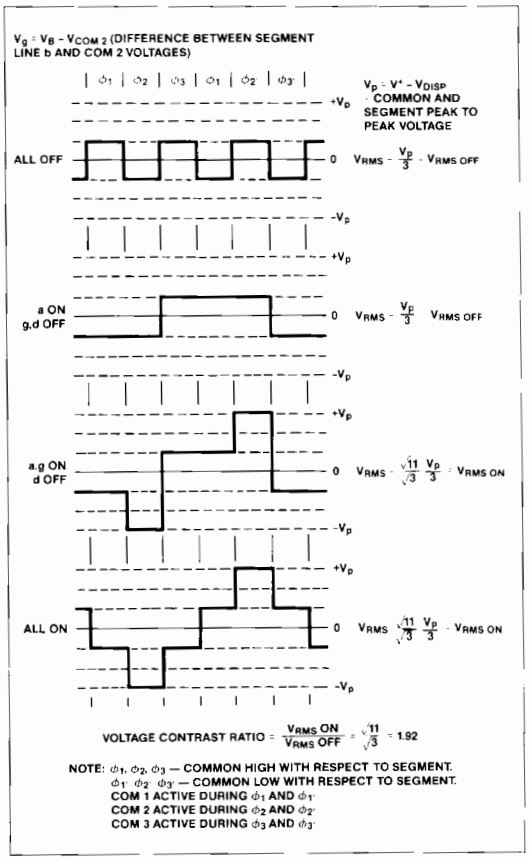


Figure 17. Voltage Waveforms on Segment g (Vg).

Triplexed LCD Decoder/Drivers

Output Codes and Display Fonts

The MAX7231 and MAX7232 numeric display drivers are programmed to drive 7-segment displays plus 2 annunciators per digit. Refer to Table 1 for annunciator input controls. The display connections for one digit are shown in Figure 18. Both annunciators are placed on COM3 on the "A" and "B" suffix devices. The "A" devices offer a "hexadecimal" 7-segment output, while the "B" devices offer "Code B" outputs. This is illustrated in Table 2. Figure 19 illustrates the "C" device configuration. The Left hand annunciator is placed on COM1 (AN2) and the right hand annunciator (usually a decimal point) is placed on COM3 (AN1). Only a "Code B" output is offered for the "C" devices.

Both the MAX7233 and MAX7234 are supplied in "A" and "B" versions, decoding an ASCII 6-bit subset to an 18-segment display, with 16 "flag" segments and 2 "dots". Figure 20 illustrates the layout for a single character. The "A" devices have numbers which are half-width and the "B" devices have full-width numbers. Refer to Table 3 for output decoding.

Table 1: Annunciator Decoding

CODE INPUT		DISPLAY OUTPUT	
AN 2	AN 1	MAX7231 A/B MAX7232 A/B BOTH ANNUNCIATORS ON COM 3	MAX7231C MAX7232C LH ANNUNCIATOR COM 1 RH ANNUNCIATOR COM 3
0	0	8	8
0	1	.8	8.
1	0	8.	8
1	1	.8.	8.

Table 2: Binary Data Decoding (MAX7231/MAX7232)

CODE INPUT				DISPLAY OUTPUT	
BD 3	BD 2	BD 1	BD 0	HEX	CODE B
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	BLANK

Table 3: Data Decoding — 18 Segment (MAX7233/MAX7234)

CODE INPUT				DISPLAY OUTPUT				
				D5	D4		A VERSION	B VERSION
D3	D2	D1	D0	0,0	0,1	1,0	1,1	
0	0	0	0		P		0	0
0	0	0	1	A	Q	!	1	1
0	0	1	0	B	R	"	2	2
0	0	1	1	C	S	#	3	3
0	1	0	0	D	T	$	4	4
0	1	0	1	E	U	%	5	5
0	1	1	0	F	V	&	6	6
0	1	1	1	G	W	'	7	7
1	0	0	0	H	X	(	8	8
1	0	0	1	I	Y	)	9	9
1	0	1	0	J	Z	*	:	
1	0	1	1	K	[	+	;	
1	1	0	0	L	\	/	<	
1	1	0	1	M	]	—	=	
1	1	1	0	N	↑	.	>	
1	1	1	1	O	←	/	?	

Table 4: Address Decoding (MAX7231/7232)

CODE INPUT				DISPLAY OUTPUT
MAX 7232 ONLY A3	A2	A1	A0	DIGIT SELECTED
0	0	0	0	D1
0	0	0	1	D2
0	0	1	0	D3
0	0	1	1	D4
0	1	0	0	D5
0	1	0	1	D6
0	1	1	0	D7
0	1	1	1	D8
1	0	0	0	D9
1	0	0	1	D10
1	0	1	0	NONE
1	0	1	1	NONE
1	1	0	0	NONE
1	1	0	1	NONE
1	1	1	0	NONE
1	1	1	1	NONE

Table 5: Address Decoding (MAX7233/7234)

CODE INPUT			DIGIT SELECTED
MAX 7234 ONLY A2	A1	A0	
0	0	0	D1
0	0	1	D2
0	1	0	D3
0	1	1	D4
1	0	0	D5
1	0	1	NONE
1	1	0	NONE
1	1	1	NONE

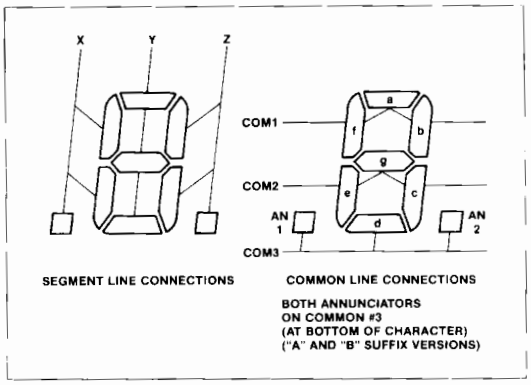


Figure 18. Display Fonts for MAX7231 and 7232. (Suffix Versions "A" and "B").

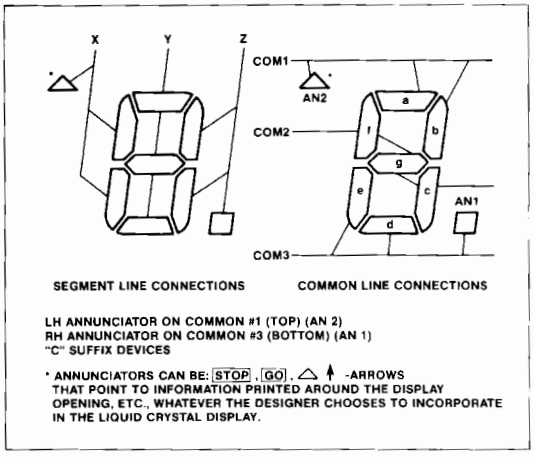


Figure 19. Display Fonts for MAX7231 and 7232. (Suffix Version "C").

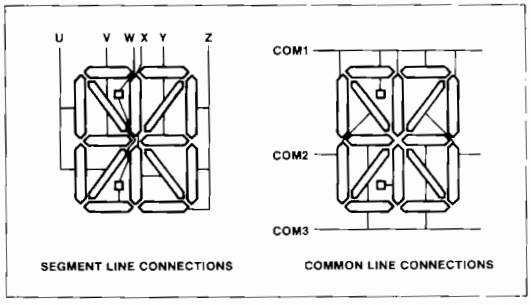


Figure 20. Display Fonts for MAX7233 and 7234. (18-Segment Alphanumeric).

Triplexed LCD Decoder/Drivers

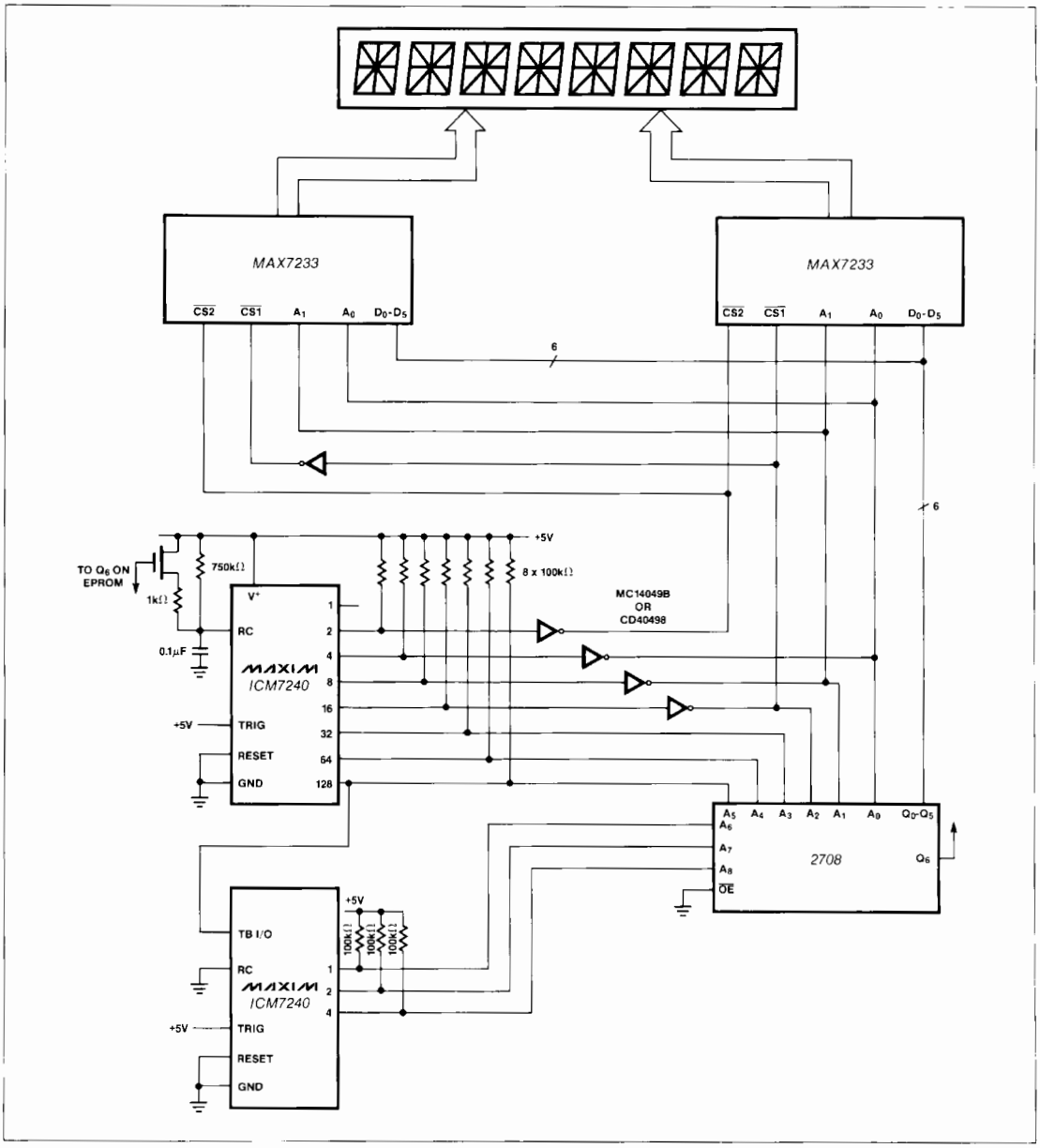


Figure 21. EPROM-Coded Message System. This circuit cycles through a message coded in the EPROM, pausing at the end of each line, or whenever coded on Q_6.

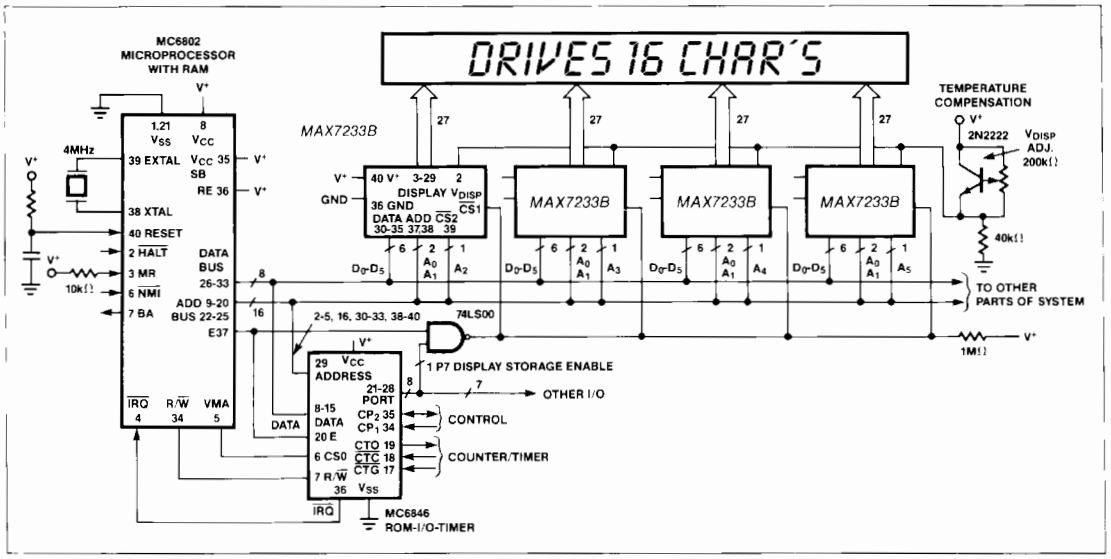
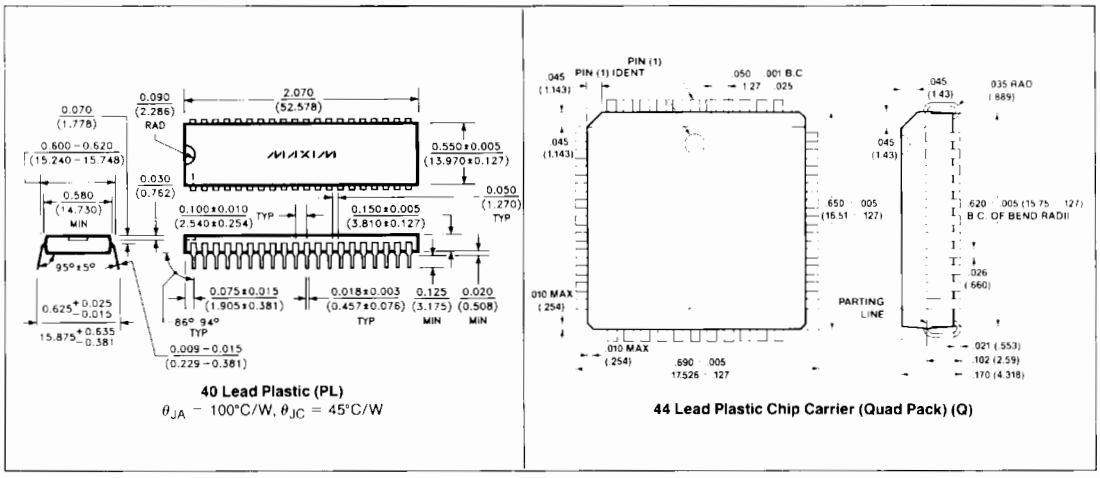


Figure 22. MC6802 Microprocessor with 16 Character 16 Segment ASCII Liquid Crystal Display.

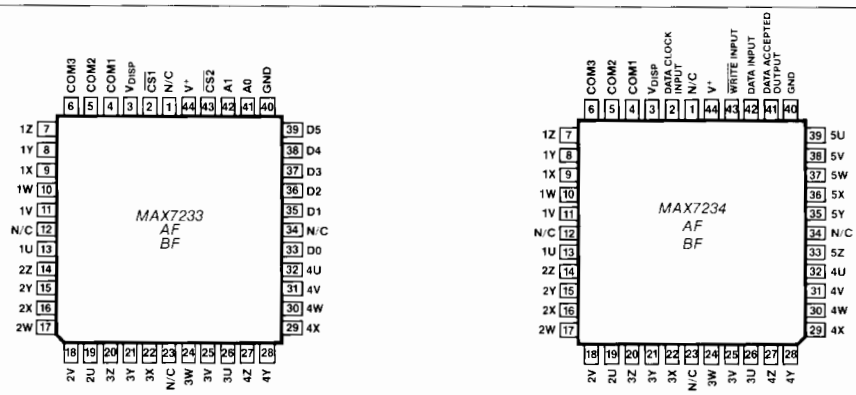
Package Information



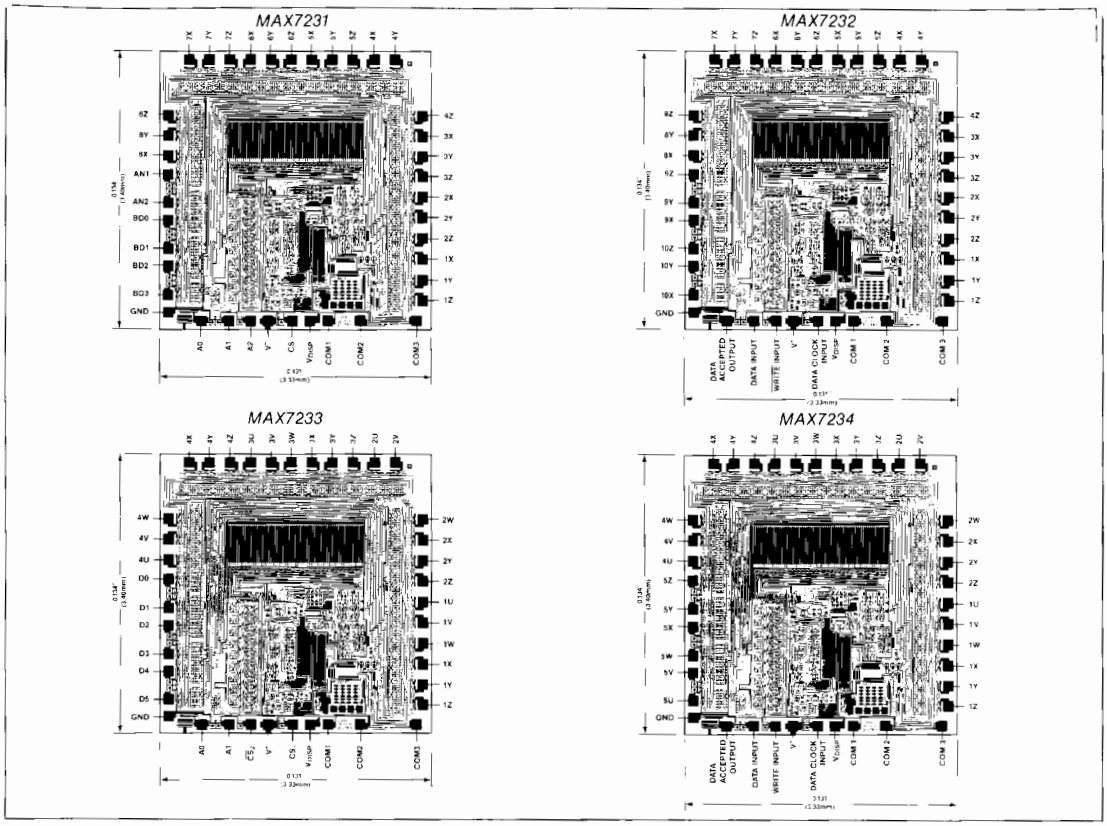
Triplexed LCD Decoder/Drivers

Pin Configuration

Top View



Chip Topography



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