19-2711; Rev 1; 8/05

EVALUATION KIT AVAILABLE

Dual Low-Dropout Linear Regulators with RESET or Low-Noise Output in UCSP or QFN

General Description

The MAX8530/MAX8531 offer the benefits of low-dropout voltage and ultra-low power regulation in subminiaturized UCSP and QFN packages with an integrated microprocessor reset circuit (MAX8530 only). The devices operate from a 2.5V to 6.5V input and deliver up to 200mA and 150mA outputs with low dropout of 100mV (typ) at 100mA. Designed with an internal P-channel MOSFET pass transistor, the supply current is kept at a low 130µA (with both LDOs on), independent of the load current and dropout voltage. Other features include short-circuit protection and thermal-shutdown protection.

The MAX8530 provides microprocessor open-drain, active-low reset output to monitor OUT1, eliminating external components and adjustments. The MAX8530 asserts a 100ms (min) $\overline{\text{RESET}}$ signal when OUT1 drops below 87% of the nominal output voltage. The MAX8531 includes a reference bypass pin for low output noise ($40\mu V_{RMS}$).

Both devices include a logic-controlled shutdown input and are available in 6-bump UCSP and 6-pin thin QFN exposed pad packages.

Applications

Cellular and Cordless Phones

PDAs and Palmtop Computers

Notebook Computers

Digital Cameras

PCMCIA Cards

Wireless LAN Cards

Hand-Held Instruments

Features

- **Guaranteed 200mA Output Current for OUT1**
- **Guaranteed 150mA Output Current for OUT2**
- **Low 100mV (typ) Dropout at 100mA Load for both LDOs**
- **Open-Drain, Active-Low 100ms (min) Reset Timer (MAX8530)**
- **Low $40\mu V_{RMS}$ Output Noise (MAX8531)**
- **Low 130µA Operating Supply Current**
- **<1µA Shutdown Current**
- **Thermal-Overload and Short-Circuit Protection**
- **Output Current Limit**
- **Tiny Packages Available**
  1.16 x 1.57 x 0.6mm UCSP (3 x 2 Grid)
  3mm x 3mm Thin QFN

Ordering Information

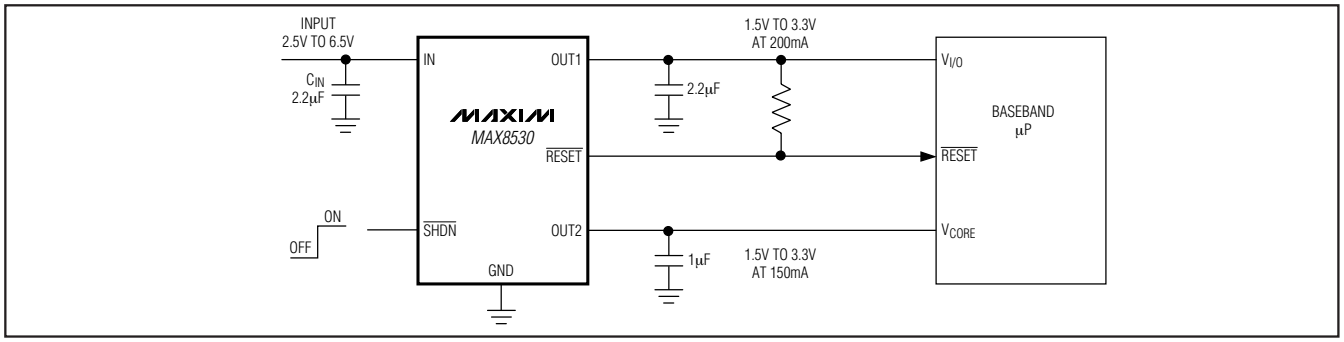
PART	TEMP RANGE	OUT_ VOLTAGE	PIN-PACKAGE
MAX8530EBTxy*-T	-40°C to +85°C	1.5V to 3.3V	6 UCSP
MAX8530EBTxy*+T	-40°C to +85°C	1.5V to 3.3V	6 UCSP
MAX8530ETTxy*-T	-40°C to +85°C	1.5V to 3.3V	6 Thin QFN-EP**
MAX8530ETTxy*+T	-40°C to +85°C	1.5V to 3.3V	6 Thin QFN-EP**
MAX8531EBTxy*-T	-40°C to +85°C	1.5V to 3.3V	6 UCSP
MAX8531EBTxy*+T	-40°C to +85°C	1.5V to 3.3V	6 UCSP
MAX8531ETTxy*-T	-40°C to +85°C	1.5V to 3.3V	6 Thin QFN-EP
MAX8531ETTxy*+T	-40°C to +85°C	1.5V to 3.3V	6 Thin QFN-EP

*xy = Output voltage code (see the Output Voltage Selector Guide).
**EP = Exposed pad.
+Denotes lead-free package.

Pin Configurations appear at end of data sheet.

Output Voltage Selector Guide appears at end of data sheet.

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Dual Low-Dropout Linear Regulators with RESET or Low-Noise Output in UCSP or QFN

ABSOLUTE MAXIMUM RATINGS

IN, $\overline{SHDN}$, $\overline{RESET}$, BP to GND .....-0.3V to +7V
OUT1, OUT2 to GND.....-0.3V to (V_{IN} + 0.3V)
Output Short-Circuit Duration .....Indefinite
Continuous Power Dissipation (T_A = +70°C)
6-Bump UCSP (derate 3.9mW/°C above +70°C) 308mW
6-Lead QFN (derate 24.4mW/°C above +70°C) 1951mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
6-Bump+ UCSP Solder Profile .....(Note 1)
6-Lead QFN Lead Temperature (10s) .....+300°C

Note 1: For UCSP solder profile information, visit www.maxim-ic.com/1st_pages/UCSP.html.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(IN = 3.8V, $\overline{SHDN}$ = IN, C_{BP} = 10nF (MAX8531), T_A = **-40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}			2.5		6.5	V
Undervoltage Lockout Threshold	V_{UVLO}	IN rising, hysteresis is 40mV (typ)		2.15	2.25	2.42	V
Output Voltage Accuracy		T_A = +25°C, I_{OUT1} = I_{OUT2} = 1mA		-1		+1	%
		T_A = -40°C to +85°C, I_{OUT1} = I_{OUT2} = 1mA		-2		+2	
		T_A = -40°C to +85°C, I_{OUT1} = 0.1mA to 200mA, I_{OUT2} = 0.1mA to 150mA		-3		+3	
Maximum Output Current	$I_{OUT_}$	OUT1		200			mA
		OUT2		150			
Current Limit	I_{LIM}	OUT1		210	330	550	mA
		OUT2		165	280	500	
Ground Current	I_Q	No load			130	220	µA
		I_{OUT1} = I_{OUT2} = 100mA			150		
Dropout Voltage	$V_{OUT_}$ - V_{IN}	$I_{OUT_}$ = 100mA (Note 3)			100	200	mV
Line Regulation	ΔV_{LNR}	IN = (OUT_ + 0.1V) to 3.8V		-0.2		+0.2	%/V
Output Voltage Noise		10Hz to 100kHz, C_{OUT} = 10µF, I_{OUT} = 10mA	MAX8530		320		$µV_{RMS}$
			MAX8531		40		
Ripple Rejection	PSRR	100Hz, I_{OUT} = 30mA	MAX8530		60		dB
			MAX8531		62		
SHUTDOWN							
$\overline{SHDN}$ Supply Current	I_{OFF}	$\overline{SHDN}$ = 0, T_A = +25°C			0.01	1	µA
		$\overline{SHDN}$ = 0, T_A = +85°C			0.1		
$\overline{SHDN}$ Input Threshold	V_{IH}	Input high voltage		1.6			V
	V_{IL}	Input low voltage				0.4	
$\overline{SHDN}$ Input Bias Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = IN or GND	T_A = +25°C		0.7	100	nA
			T_A = +85°C		0.8		
THERMAL PROTECTION							
Thermal-Shutdown Temperature	T_{SHDN}	T_J rising			160		°C
Thermal-Shutdown Hysteresis	ΔT_{SHDN}				10		°C

ELECTRICAL CHARACTERISTICS (continued)

(IN = 3.8V, $\overline{SHDN}$ = IN, C_{BP} = 10nF (MAX8531), T_A = **-40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

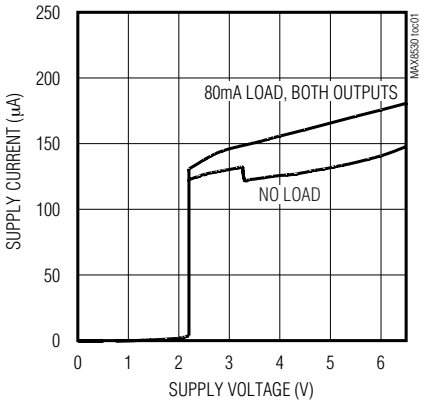
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RESET OUTPUT (MAX8530 ONLY)							
$\overline{RESET}$ Threshold	V_{TH}	Percentage of nominal output, OUT1 falling, when $\overline{RESET}$ falls.		84	87	89	%
$\overline{RESET}$ Threshold Hysteresis					0.5		%
$\overline{RESET}$ Output Voltage Low (Open-Drain, Active Low)	V_{OL}	$I_{\overline{RESET}}$ = 500µA, IN = 3.8V			10	20	mV
		$I_{\overline{RESET}}$ = 100µA, IN = 1.2V			10	40	
$\overline{RESET}$ Open-Drain Output Leakage Current		$V_{\overline{RESET}}$ = 6.5V	T_A = +25°C		0.001	1	µA
			T_A = +85°C		0.01		
$\overline{RESET}$ Active Timeout Delay		From OUT1 rising to $\overline{RESET}$ rising.		100	200	360	ms

Note 2: All units are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
Note 3: The dropout voltage is defined as V_{IN} - V_{OUT}, when V_{OUT} is 100mV below the value of V_{OUT} for V_{IN} = V_{OUT} + 0.5V. Specification applies only when $V_{OUT} \geq$ 2.5V.

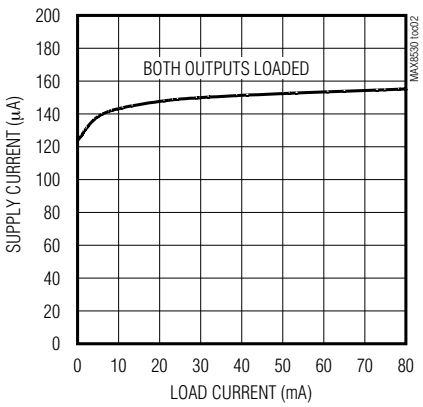
Typical Operating Characteristics

V_{OUT1} = 3.3V, V_{OUT2} = 1.5V, load = 80mA (both output voltages), V_{IN} = 3.8V, $C_{OUT_}$ = 2.2µF, C_{BP} = 0.01µF, C_{IN} = 2.2µF, and T_A = +25°C, unless otherwise noted.

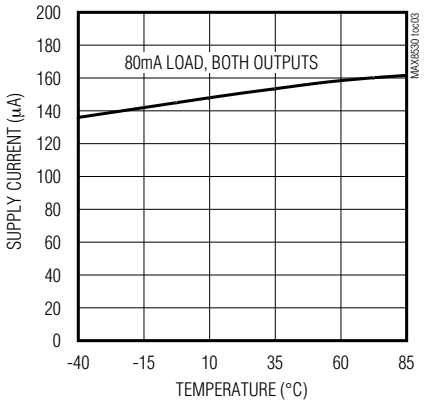
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. LOAD CURRENT



SUPPLY CURRENT vs. TEMPERATURE

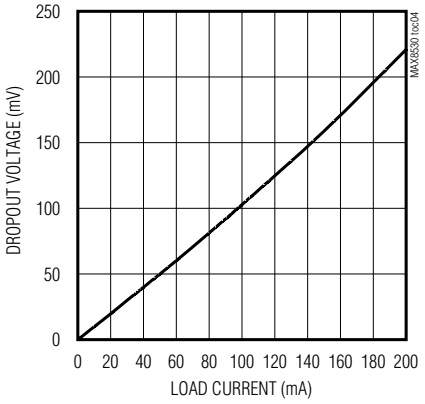


Dual Low-Dropout Linear Regulators with RESET or Low-Noise Output in UCSP or QFN

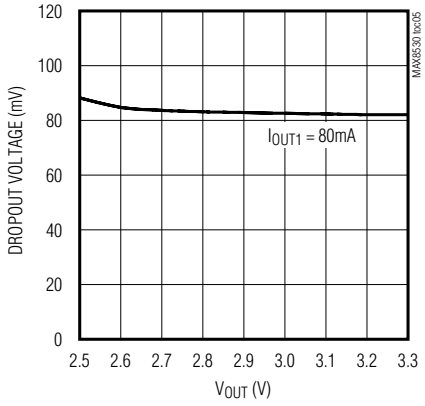
Typical Operating Characteristics (continued)

V_{OUT1} = 3.3V, V_{OUT2} = 1.5V, load = 80mA (both output voltages), V_{IN} = 3.8V, $C_{OUT_}$ = 2.2µF, C_{BP} = 0.01µF, C_{IN} = 2.2µF, and T_A = +25°C, unless otherwise noted.

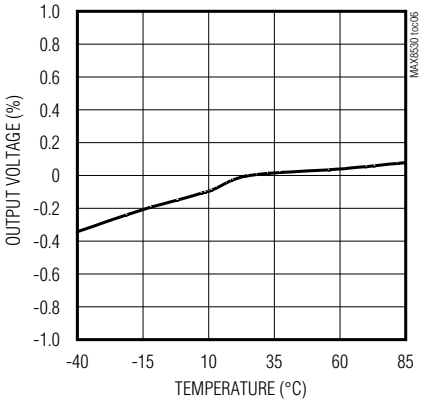
DROPOUT VOLTAGE vs. LOAD CURRENT



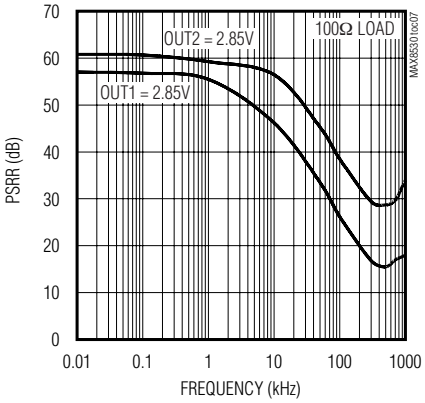
LDO DROPOUT VOLTAGE vs. V_{OUT}



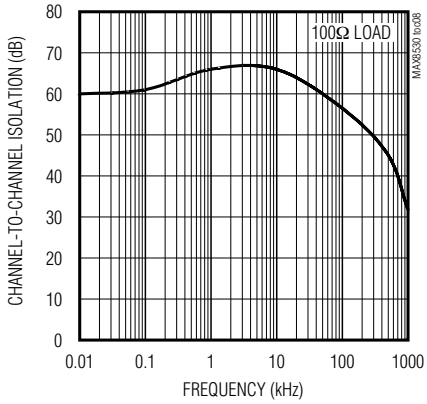
OUTPUT VOLTAGE ACCURACY vs. TEMPERATURE



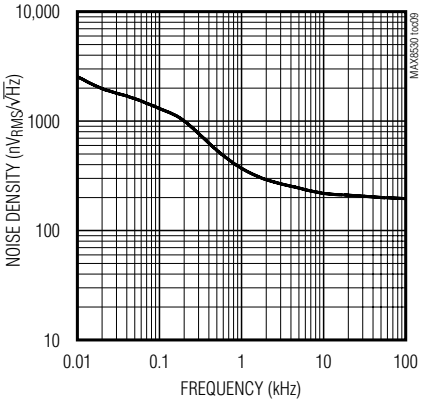
PSRR vs. FREQUENCY



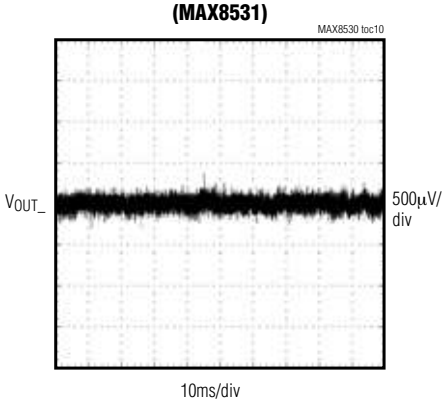
CHANNEL-TO-CHANNEL ISOLATION vs. FREQUENCY (MAX8531)



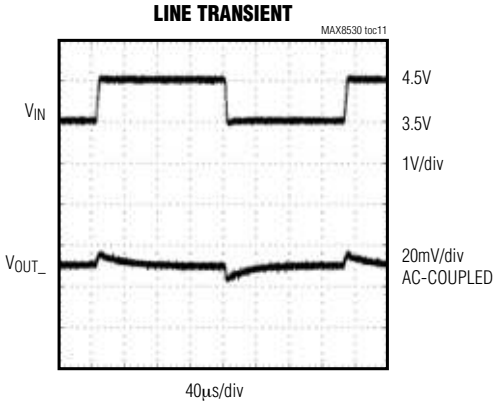
OUTPUT NOISE SPECTRAL DENSITY vs. FREQUENCY (MAX8531)



OUTPUT NOISE (10Hz TO 100kHz) (MAX8531)



LINE TRANSIENT

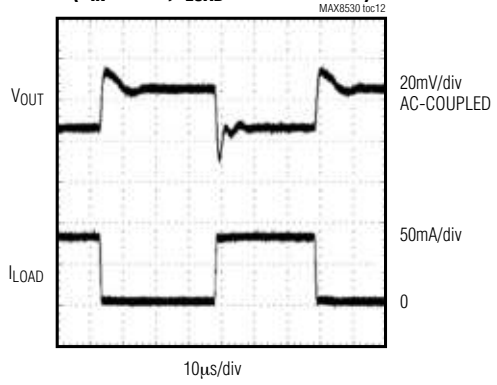


Dual Low-Dropout Linear Regulators with RESET or Low-Noise Output in UCSP or QFN

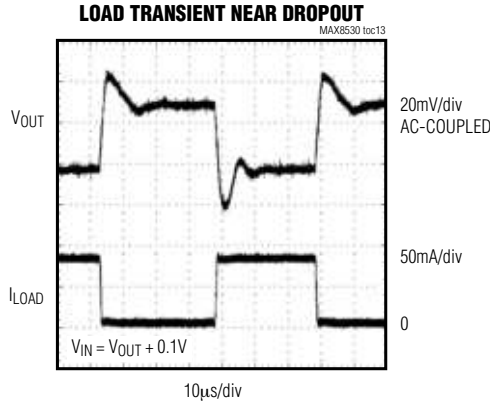
Typical Operating Characteristics (continued)

V_{OUT1} = 3.3V, V_{OUT2} = 1.5V, load = 80mA (both output voltages), V_{IN} = 3.8V, $C_{OUT_}$ = 2.2µF, C_{BP} = 0.01µF, C_{IN} = 2.2µF, and T_A = +25°C, unless otherwise noted.

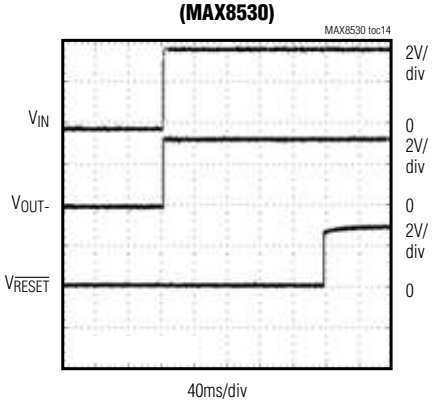
LOAD TRANSIENT
(V_{IN} = 3.8V, I_{LOAD} = 1mA TO 80mA)



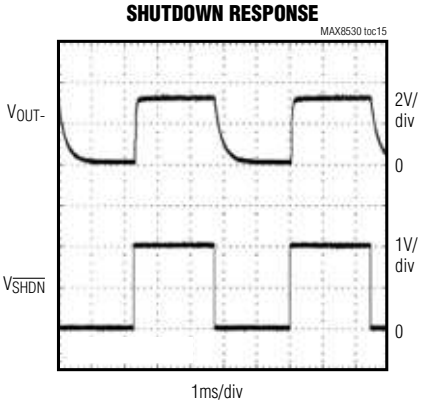
LOAD TRANSIENT NEAR DROPOUT



$\overline{RESET}$ RESPONSE (MAX8530)



SHUTDOWN RESPONSE

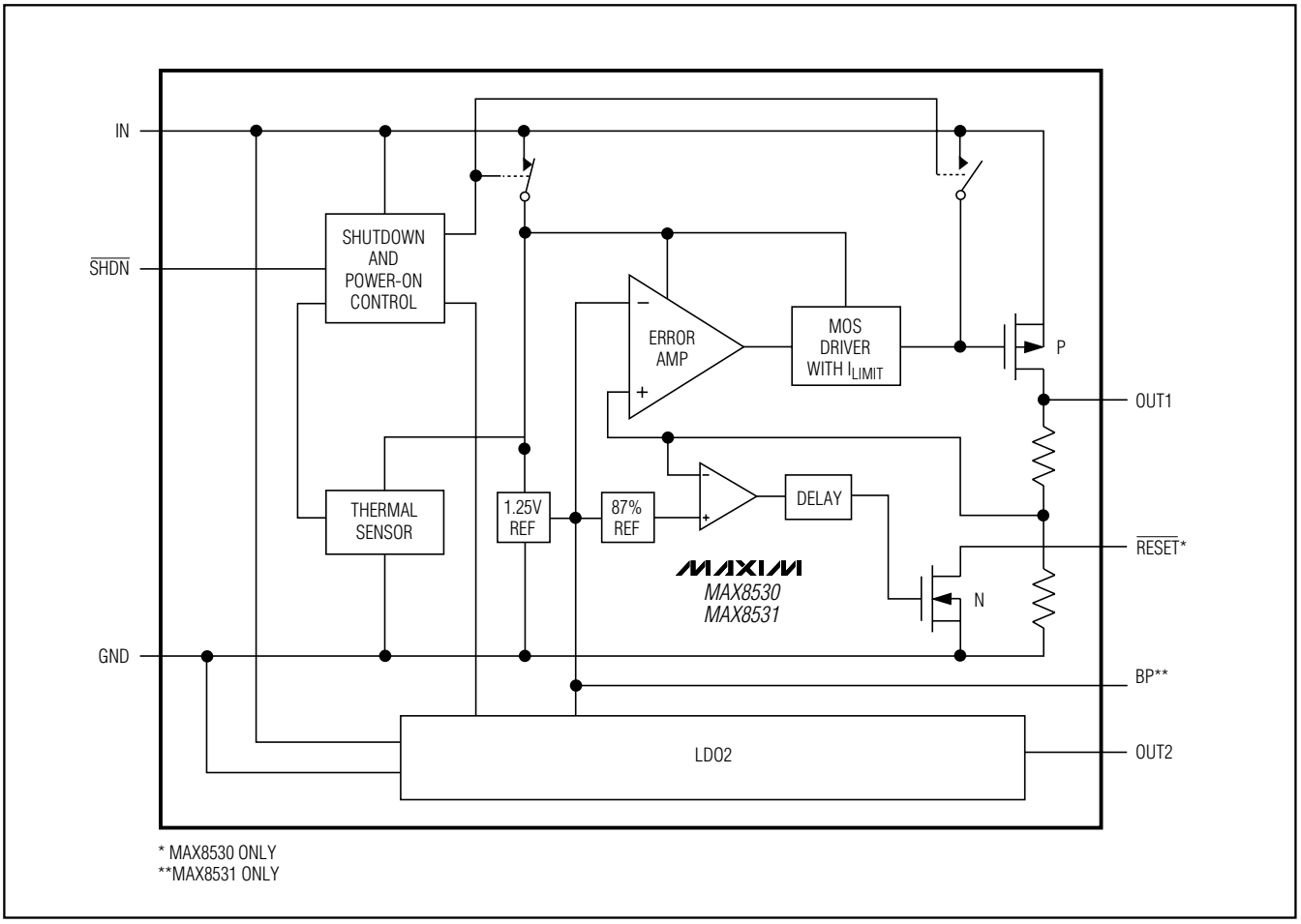


Pin Description

PIN				NAME	FUNCTION
MAX8530 (QFN)	MAX8531 (QFN)	MAX8530 (UCSP)	MAX8531 (UCSP)		
1	1	B3	B3	OUT2	Regulator 2 Output. Guaranteed 150mA output current.
2	2	B2	B2	IN	Regulator Input
3	3	B1	B1	OUT1	Regulator 1 Output. Guaranteed 200mA output current.
4	4	A1	A1	GND	Ground. Also functions as a heatsink for the 6-pin QFN. Solder to a large pad or the circuit board ground plane to maximize thermal dissipation.
5	5	A2	A2	$\overline{SHDN}$	Shutdown Input. A logic low shuts down both regulators. Connect to IN for normal operation.
6	—	A3	—	$\overline{RESET}$	Reset Active-Low Open-Drain Output. Minimum timeout of 100ms. $\overline{RESET}$ is low in shutdown.
—	6	—	A3	BP	Reference Noise Bypass. Connect to a 0.01µF ceramic capacitor for reduced noise at both outputs.

Dual Low-Dropout Linear Regulators with RESET or Low-Noise Output in UCSP or QFN

Functional Diagram



Detailed Description

The MAX8530/MAX8531 are low-power, low-dropout, low-quiescent current linear regulators with reset designed primarily for battery-powered applications. For preset output voltages, refer to the *Output Voltage Selector Guide*. Other combinations between 1.5V and 3.3V are available in 50mV increments. This device supplies loads up to 200mA for OUT1 and 150mA for OUT2. The MAX8530/MAX8531 consist of a 1.25V reference, error amplifiers, P-channel pass transistors, reset block, and internal feedback voltage-dividers.

The 1.25V bandgap reference is connected to the error amplifier's inverting input. The error amplifier compares this reference with the feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the pass-transistor gate is pulled lower, allowing more current to pass to the output and increasing the output voltage. If the feedback voltage is too high, the pass-transistor gate is pulled up, allowing less current to pass to the output. The output voltage is fed back through an internal resistor voltage-divider connected to the OUT_ pin.

RESET

The reset circuit is active at power-up and power-down. RESET is held low at power-up. The reset timing starts once the OUT1 voltage reaches 87% (typ) of its regulation voltage. The RESET signal goes high 200ms (typ) after the OUT1 voltage reaches 87% (typ) of its regulation voltage. At power-off, RESET goes low when the OUT1 voltage is below 87% (typ) of its regulation voltage.

Dual Low-Dropout Linear Regulators with RESET or Low-Noise Output in UCSP or QFN

Shutdown

The MAX8530/MAX8531 have a single shutdown control input ($\overline{SHDN}$). Drive $\overline{SHDN}$ low to shut down both outputs, reducing supply current to 10nA. Connect $\overline{SHDN}$ to a logic high, or IN, for normal operation.

Internal P-Channel Pass Transistor

The MAX8530/MAX8531 feature two 1Ω P-channel MOSFET pass transistors. A P-channel MOSFET provides several advantages over similar designs using PNP pass transistors, including longer battery life. It requires no base drive, substantially reducing quiescent current. PNP-based regulators waste considerable current in dropout when the pass transistor saturates and also use high base-drive currents under heavy loads. The MAX8530/MAX8531 do not suffer these problems and consume only 150µA of quiescent current whether in dropout, light-load, or heavy-load applications (see the *Typical Operating Characteristics*). Whereas a PNP-based regulator has dropout voltage that is independent of the load, a P-channel MOSFET's dropout voltage is proportional to load current, providing for low dropout voltage at heavy loads and extremely low dropout voltage at lighter loads.

Current Limit

The MAX8530/MAX8531 contain two independent current limiters, one for each regulator, which monitor and control the pass transistor's gate voltage and limit the output currents to 210mA and 165mA minimum. The output can be shorted to ground for an indefinite time without damaging the part.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX8530/MAX8531. When the junction temperature exceeds T_J = +160°C, the thermal sensor signals the shutdown logic, turning off the pass transistor and allowing the IC to cool. The thermal sensor turns the pass transistor on again after the IC's junction temperature cools by 10°C, resulting in a pulsed output during continuous thermal-overload conditions.

Thermal-overload protection is designed to protect the MAX8530/MAX8531 in the event of fault conditions. For continual operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

Operating Region and Power Dissipation

The MAX8530/MAX8531s' maximum power dissipation depends on the thermal resistance of the case and circuit board, the temperature difference between the die junction and ambient air, and the rate of airflow. The power dissipation across the device is $P = I_{OUT} (V_{IN} - V_{OUT})$. Maximum power dissipation:

$$P_{MAX} = (T_J - T_A)/(\theta_{JB} + \theta_{BA})$$

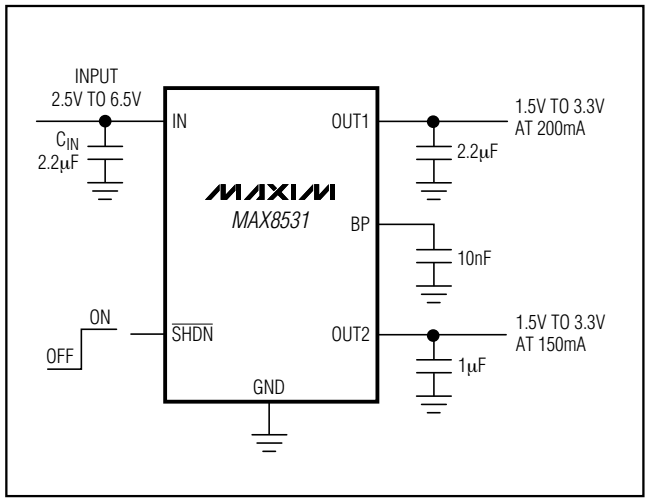
where $T_J - T_A$ is the temperature difference between the MAX8530/MAX8531 die junction and the surrounding air, θ_{JB} (or θ_{JC}) is the thermal resistance of the package, and θ_{BA} is the thermal resistance through the printed circuit board, copper traces, and other materials to the surrounding air.

The GND pin of the MAX853_ETT__ (6-lead QFN) performs the dual functions of providing an electrical connection to the ground and channeling heat away. Connect the GND pin and exposed pad to ground using a large pad or ground plane.

Low-Noise Operation (MAX8531)

An external 0.01µF bypass capacitor at BP, in conjunction with an internal resistor, creates a lowpass filter (see the *Typical Application Circuit*). The MAX8531 exhibits 40μV_{RMS} output voltage noise with C_{BP} = 0.01µF and C_{OUT} = 2.2µF (see the Output Noise Spectral Density vs. Frequency graph in the *Typical Operating Characteristics*).

MAX8531 Typical Appication Circuit



Dual Low-Dropout Linear Regulators with RESET or Low-Noise Output in UCSP or QFN

Applications Information

Capacitor Selection and Regulator Stability

Use a 2.2µF capacitor on the MAX8530/MAX8531s' inputs. Larger input capacitor values with lower ESRs provide better supply-noise rejection and line-transient response. To reduce noise and improve load transients, use large-output capacitors, up to 10µF. For stable operation over the full temperature range and with rated maximum load currents, use a minimum of 2.2µF (or 1µF for <150mA loading for OUT1) and 1µF for OUT2.

Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature. With dielectrics such as Z5U and Y5V, it is necessary to use 4.7µF or more to ensure stability at temperatures below -10°C. With X7R or X5R dielectrics, 2.2µF is sufficient at all operating temperatures. These regulators are optimized for ceramic capacitors. Tantalum capacitors are not recommended.

PSRR and Operation from Sources Other than Batteries

The MAX8530/MAX8531 is designed to deliver low dropout voltages and low quiescent currents in battery-powered systems. Power-supply rejection is 60dB at low frequencies (see the Power-Supply Rejection Ratio vs. Frequency graph in the *Typical Operating Characteristics*).

When operating from sources other than batteries, improve supply-noise rejection and transient response by increasing the values of the input and output bypass capacitors and through passive filtering techniques.

Load-Transient Considerations

The MAX8530/MAX8531 load-transient response graphs (see the *Typical Operating Characteristics*) show two components of the output response: a DC shift in the output voltage because of the different load currents, and the transient response. Increase the output capacitor's value and decrease its ESR to attenuate transient spikes.

Input/Output (Dropout Voltage)

A regulator's minimum input/output voltage differential (or dropout voltage) determines the lowest usable supply voltage. In battery-powered systems, this determines the useful end-of-life battery voltage. Because the MAX8530/MAX8531 use a P-channel MOSFET pass transistor, their dropout voltage is a function of drain-to-source on-resistance ($R_{DS(ON)}$) multiplied by the load current (see the *Typical Operating Characteristics*).

Calculating the Maximum Output Power in UCSP

The maximum output power of the MAX8530/MAX8531 can be limited by the maximum power dissipation of the package. Obtain the maximum power dissipation by calculating the power dissipation of the package as a function of the input voltage, output voltage, and output currents. The maximum power dissipation should not exceed the package's maximum power rating:

$$P = (V_{IN(MAX)} - V_{OUT1}) \times I_{OUT1} + (V_{IN(MAX)} - V_{OUT2}) \times I_{OUT2}$$

where:

$V_{IN(MAX)}$ = Maximum input voltage

P_{MAX} = Maximum power dissipation of the package (308mW for UCSP and 1951mW for the QFN package)

V_{OUT1} = Output voltage of OUT1

V_{OUT2} = Output voltage of OUT2

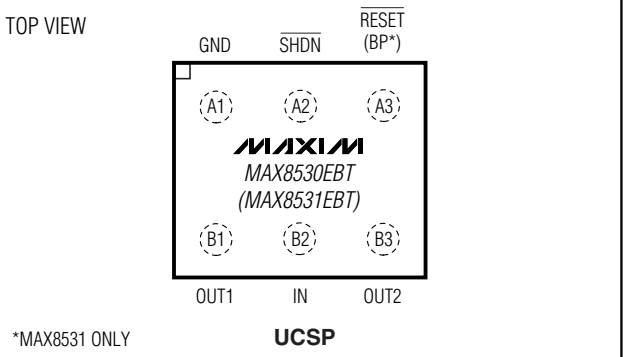
I_{OUT1} = Maximum output current of OUT1

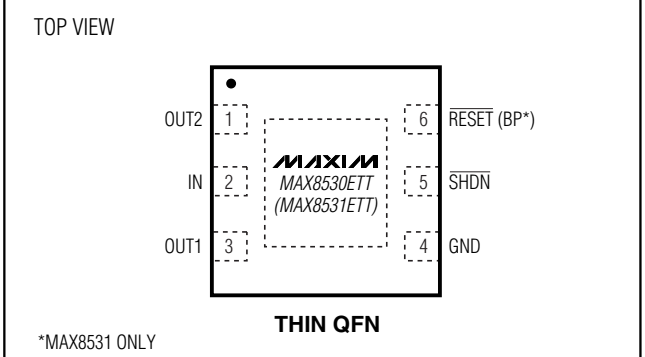
I_{OUT2} = Maximum output current of OUT2

P should be less than P_{MAX}. If P is greater than P_{MAX}, consider using the QFN package.

Dual Low-Dropout Linear Regulators with RESET or Low-Noise Output in UCSP or QFN

Pin Configurations





Output Voltage Selector Guide

PART	V_{OUT1}	V_{OUT2}	TOP MARK
MAX8530EBTJ2	2.85	1.8	ACR
MAX8530EBTJO	2.85	2.6	ACA
MAX8530EBTKG	2.8	3.0	ACT
MAX8530ETTP2	2.5	1.8	AET
MAX8530ETTO2	2.6	1.8	AES
MAX8530ETTK2	2.8	1.8	AER
MAX8530ETTKO	2.8	2.6	AEQ
MAX8531EBTJJ	2.85	2.85	ACG
MAX8531EBTGG	3.0	3.0	ACI
MAX8531ETTGG	3.0	3.0	AEF

***Note**: Contact the factory for other output voltages between 1.5V and 3.3V. The minimum order quantity is 25,000 units.*

Chip Information

TRANSISTOR COUNT: 1720

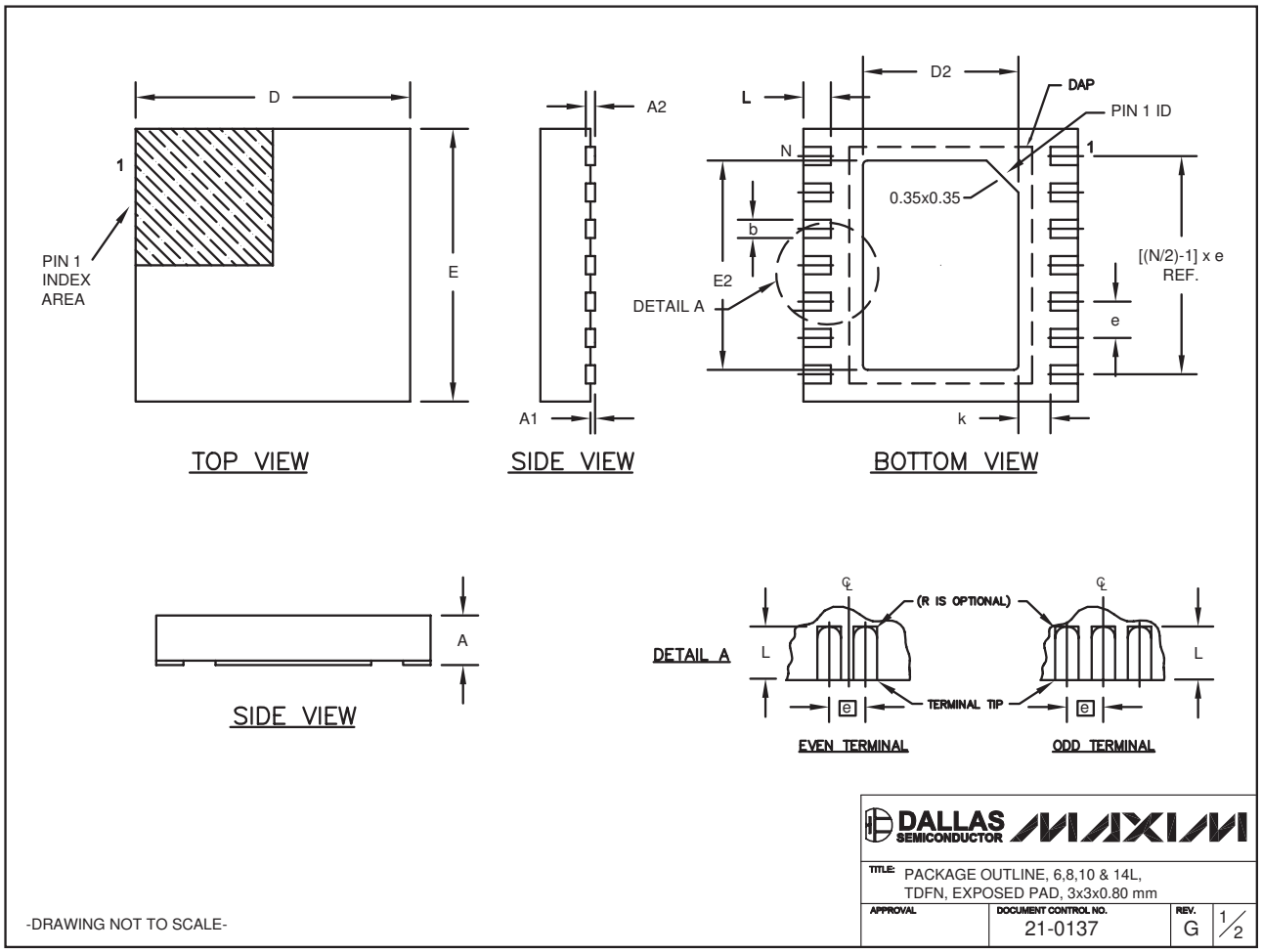
PROCESS: BiCMOS

Dual Low-Dropout Linear Regulators with RESET or Low-Noise Output in UCSP or QFN

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

6, 8, &10L, DFN THIN.EPS



Dual Low-Dropout Linear Regulators with RESET or Low-Noise Output in UCSP or QFN

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS								
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e	DOWNBONDS ALLOWED
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	YES
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF	NO
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF	YES
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF	NO

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

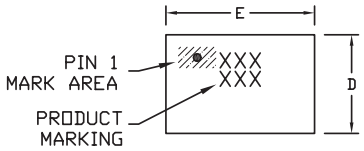
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	G	2/2

Dual Low-Dropout Linear Regulators with RESET or Low-Noise Output in UCSP or QFN

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

6L, UCSP.EPS

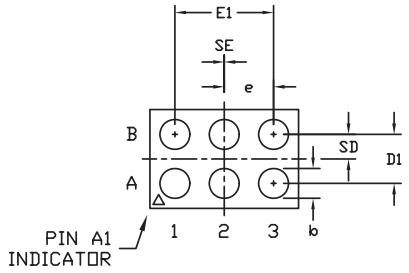


TOP VIEW

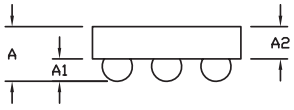
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	0.50 BASIC
E1	1.00 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B6-1	1.00±0.05	1.52±0.05	NONE
B6-2	1.00±0.05	1.52±0.05	B2
B6-3	1.05±0.05	1.57±0.05	NONE
B6-4	1.05±0.05	1.57±0.05	B2
B6-5	0.97±0.05	1.46±0.05	NONE
B6-6	1.16±0.05	1.57±0.05	NONE

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



BOTTOM VIEW



SIDE VIEW

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 3x2 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0097	G	1/1

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