# MC10E451, MC100E451

# 5 V ECL 6-Bit D Register Differential Data and Clock

### Description

The MC10E/100E451 contains six D-type flip-flops with single-ended outputs and differential data inputs. The common clock input is also differential. The registers are triggered by a positive transition of the positive clock (CLK) input.

A HIGH on the Master Reset (MR) input resets all Q outputs to LOW.

The differential input structures are clamped so that the inputs of unused registers can be left open without upsetting the bias network of the device. The clamping action will assert the $\overline{D}$ and the $\overline{CLK}$ sides of the inputs. Because of the edge triggered flip-flop nature of the device simultaneously opening both the clock and data inputs will result in an output which reaches an unidentified but valid state. Note that the input clamps only operate when both inputs fall to 2.5 V below $V_{CC}$.

The $V_{BB}$ pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to $V_{BB}$ as a switching reference voltage. $V_{BB}$ may also rebias AC coupled inputs. When used, decouple $V_{BB}$ and $V_{CC}$ via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, $V_{BB}$ should be left open.

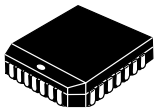
The 100 Series contains temperature compensation.

### Features

- Differential Inputs: Data and Clock
- $V_{BB}$ Output
- 1100 MHz Min. Toggle Frequency
- Asynchronous Master Reset
- PECL Mode Operating Range:
  $V_{CC}$ = 4.2 V to 5.7 V with $V_{EE}$ = 0 V
- NECL Mode Operating Range:
  $V_{CC}$ = 0 V with $V_{EE}$ = −4.2 V to −5.7 V
- Internal Input 50 kΩ Pulldown Resistors
- ESD Protection:
  - > 2 kV Human Body Model
  - > 200 V Machine Model
- Transistor Count = 348 Devices
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Flammability Rating: UL 94 V−0 @ 0.125 in,
  Oxygen Index: 28 to 34
- Moisture Sensitivity: Level 3 (Pb-Free)
  (For Additional Information, see Application Note AND8003/D)
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

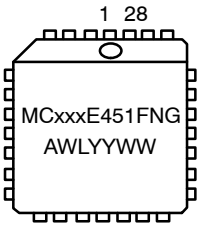
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**PLCC−28**
**FN SUFFIX**
**CASE 776−02**

### MARKING DIAGRAM*




| | |
|---|---|
| xxx | = 10 or 100 |
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G | = Pb-Free Package |

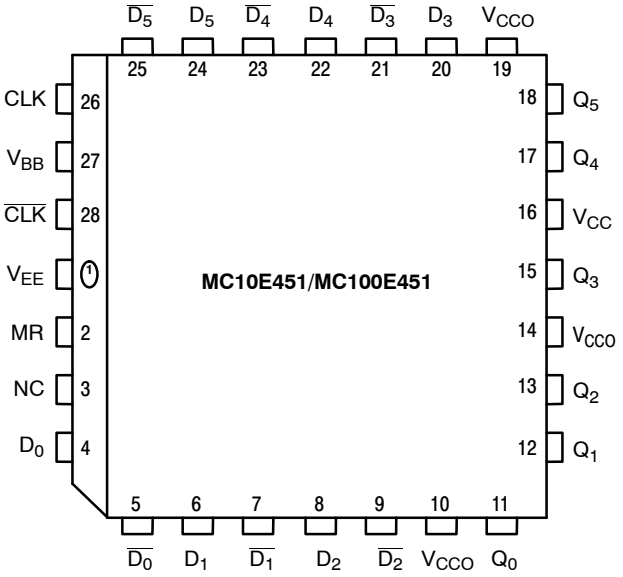
*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC10E451FNG | PLCC−28 (Pb-Free) | 37 Units / Tube |
| MC10E451FNR2G | PLCC−28 (Pb-Free) | 500 Tape & Reel |
| MC100E451FNG | PLCC−28 (Pb-Free) | 37 Units / Tube |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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* All $V_{CC}$ and $V_{CCO}$ pins are tied together on the die.

Warning: All $V_{CC}$, $V_{CCO}$, and $V_{EE}$ pins must be externally connected to Power Supply to guarantee proper operation.

**Figure 1. 28-Lean Pinout Assignment** (Top View)

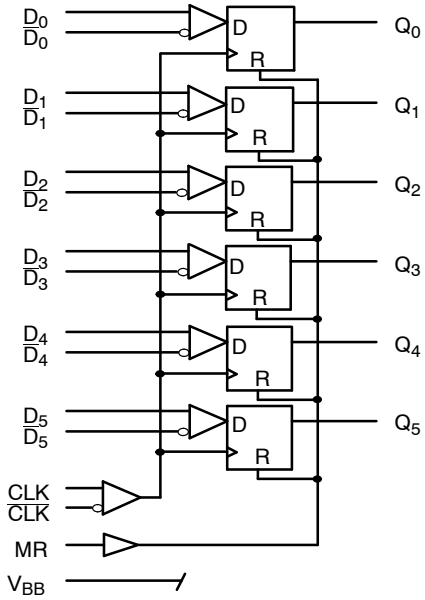



**Figure 2. Logic Diagram**

**Table 1. PIN DESCRIPTION**

| PIN | FUNCTION |
|---|---|
| $D_0 - D_5$, $\overline{D_0} - \overline{D_5}$ | ECL Differential Data Input |
| CLK, $\overline{CLK}$ | ECL Differential Clock Input |
| MR | ECL Master Reset Input |
| $Q_0 - Q_5$ | ECL Data Outputs |
| $V_{BB}$ | Reference Voltage Output |
| $V_{CC}$, $V_{CCO}$ | Positive Supply |
| $V_{EE}$ | Negative Supply |
| NC | No Connect |

**Table 2. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | PECL Mode Power Supply | $V_{EE}$ = 0 V | | 8 | V |
| $V_{EE}$ | NECL Mode Power Supply | $V_{CC}$ = 0 V | | −8 | V |
| $V_I$ | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE}$ = 0 V<br>$V_{CC}$ = 0 V | $V_I \le V_{CC}$<br>$V_I \ge V_{EE}$ | 6<br>−6 | V |
| $I_{out}$ | Output Current | Continuous<br>Surge | | 50<br>100 | mA |
| $I_{BB}$ | $V_{BB}$ Sink/Source | | | ±0.5 | mA |
| $T_A$ | Operating Temperature Range | | | 0 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm | PLCC−28<br>PLCC−28 | 63.5<br>43.5 | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case) | Standard Board | PLCC−28 | 22 to 26 | °C/W |
| $T_{sol}$ | Wave Solder (Pb-Free) | | | 265 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 3. 10E SERIES PECL DC CHARACTERISTICS** ($V_{CCx}$ = 5.0 V; $V_{EE}$ = 0.0 V (Note 1))

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | | 84 | 101 | | 84 | 101 | | 84 | 101 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | 3980 | 4070 | 4160 | 4020 | 4105 | 4190 | 4090 | 4185 | 4280 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | 3050 | 3210 | 3370 | 3050 | 3210 | 3370 | 3050 | 3227 | 3405 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | 3830 | 3995 | 4160 | 3870 | 4030 | 4190 | 3940 | 4110 | 4280 | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | 3050 | 3285 | 3520 | 3050 | 3285 | 3520 | 3050 | 3302 | 3555 | mV |
| $V_{BB}$ | Output Voltage Reference | 3.62 | | 3.74 | 3.65 | | 3.75 | 3.69 | | 3.81 | V |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | 2.2 | | 4.6 | 2.2 | | 4.6 | 2.2 | | 4.6 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.25 | | 0.3 | 0.2 | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary −0.46 V / +0.06 V.
2. Outputs are terminated through a 50 Ω resistor to $V_{CC}$ − 2.0 V.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, max varies 1:1 with $V_{CC}$.

**Table 4. 10E SERIES NECL DC CHARACTERISTICS** ($V_{CCx}$ = 0.0 V; $V_{EE}$ = −5.0 V (Note 1))

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | | 84 | 101 | | 84 | 101 | | 84 | 101 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | −1020 | −930 | −840 | −980 | −895 | −810 | −910 | −815 | −720 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | −1950 | −1790 | −1630 | −1950 | −1790 | −1630 | −1950 | −1773 | −1595 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | −1170 | −1005 | −840 | −1130 | −970 | −810 | −1060 | −890 | −720 | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | −1950 | −1715 | −1480 | −1950 | −1715 | −1480 | −1950 | −1698 | −1445 | mV |
| $V_{BB}$ | Output Voltage Reference | −1.38 | | −1.27 | −1.35 | | −1.25 | −1.31 | | −1.19 | V |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | −2.8 | | −0.4 | −2.8 | | −0.4 | −2.8 | | −0.4 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.065 | | 0.3 | 0.2 | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary −0.46 V / +0.06 V.
2. Outputs are terminated through a 50 Ω resistor to $V_{CC}$ − 2.0 V.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, max varies 1:1 with $V_{CC}$.

**Table 5. 100E SERIES PECL DC CHARACTERISTICS** ($V_{CCx}$ = 5.0 V; $V_{EE}$ = 0.0 V (Note 1))

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | | 84 | 101 | | 84 | 101 | | 97 | 116 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | 3975 | 4050 | 4120 | 3975 | 4050 | 4120 | 3975 | 4050 | 4120 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | 3190 | 3295 | 3380 | 3190 | 3255 | 3380 | 3190 | 3260 | 3380 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | 3835 | 3975 | 4120 | 3835 | 3975 | 4120 | 3835 | 3975 | 4120 | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | 3190 | 3355 | 3525 | 3190 | 3355 | 3525 | 3190 | 3355 | 3525 | mV |
| $V_{BB}$ | Output Voltage Reference | 3.62 | | 3.74 | 3.62 | | 3.74 | 3.62 | | 3.74 | V |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | 2.2 | | 4.6 | 2.2 | | 4.6 | 2.2 | | 4.6 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.25 | | 0.5 | 0.2 | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary −0.46 V / +0.8 V.
2. Outputs are terminated through a 50 Ω resistor to $V_{CC}$ − 2.0 V.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, max varies 1:1 with $V_{CC}$.

**Table 6. 100E SERIES NECL DC CHARACTERISTICS** ($V_{CCx}$ = 0.0 V; $V_{EE}$ = −5.0 V (Note 1))

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | | 84 | 101 | | 84 | 101 | | 97 | 116 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | −1025 | −950 | −880 | −1025 | −950 | −880 | −1025 | −950 | −880 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | −1810 | −1705 | −1620 | −1810 | −1745 | −1620 | −1810 | −1740 | −1620 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | −1165 | −1025 | −880 | −1165 | −1025 | −880 | −1165 | −1025 | −880 | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | −1810 | −1645 | −1475 | −1810 | −1645 | −1475 | −1810 | −1645 | −1475 | mV |
| $V_{BB}$ | Output Voltage Reference | −1.38 | | −1.26 | −1.38 | | −1.26 | −1.38 | | −1.26 | V |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | −2.8 | | −0.4 | −2.8 | | −0.4 | −2.8 | | −0.4 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.25 | | 0.5 | 0.2 | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.46 V / −0.8 V.
2. Outputs are terminated through a 50 Ω resistor to $V_{CC}$ − 2.0 V.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, max varies 1:1 with $V_{CC}$.

**Table 7. AC CHARACTERISTICS** ($V_{CCx}$ = 5.0 V; $V_{EE}$ = 0.0 V or $V_{CCx}$ = 0.0 V; $V_{EE}$ = −5.0 V (Note 1))

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Toggle Frequency | 1.1 | | | 1.1 | | | 1.1 | | | GHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay to Output<br>CLK (Differential), CLK (Single-Ended), MR | 625 | | 1050 | 625 | | 1050 | 625 | | 1050 | ps |
| $t_s$ | Setup Time D | 150 | −100 | | 150 | −100 | | 150 | −100 | | ps |
| $t_h$ | Hold Time D | 250 | 100 | | 250 | 100 | | 250 | 100 | | ps |
| $t_{RR}$ | Reset Recovery Time | 750 | 600 | | 750 | 600 | | 750 | 600 | | ps |
| $t_{PW}$ | Minimum Pulse Width<br>CLK, MR | 400 | | | 400 | | | 400 | | | ps |
| $t_{SKEW}$ | Within-Device Skew (Note 2) | | 100 | | | 100 | | | 100 | | ps |
| $t_{JITTER}$ | Random Clock Jitter (RMS) | | <1.0 | | | <1.0 | | | <1.0 | | ps |
| $V_{PP}$ | Input Voltage Swing (Differential Configuration) | 150 | | 1000 | 150 | | 1000 | 150 | | 1000 | mV |
| $t_r$<br>$t_f$ | Rise/Fall Times (20−80%) | 275 | 450 | 800 | 275 | 450 | 800 | 275 | 450 | 800 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. 10 Series: $V_{EE}$ can vary −0.46 V / +0.06 V.
   100 Series: $V_{EE}$ can vary −0.46 V / +0.8 V.
2. Within−device skew is defined as identical transitions on similar paths through a device.

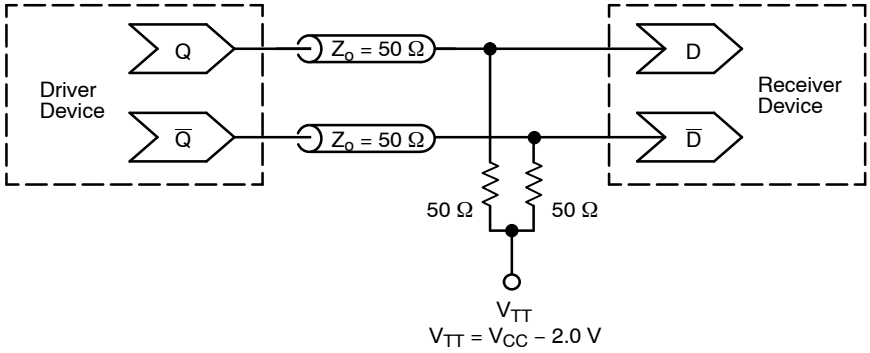



**Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices)**

### Resource Reference of Application Notes

**AN1405/D** – ECL Clock Distribution Techniques

**AN1406/D** – Designing with PECL (ECL at +5.0 V)

**AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit

**AN1504/D** – Metastability and the ECLinPS Family

**AN1568/D** – Interfacing Between LVDS and ECL

**AN1672/D** – The ECL Translator Guide

**AND8001/D** – Odd Number Counters Design

**AND8002/D** – Marking and Date Codes

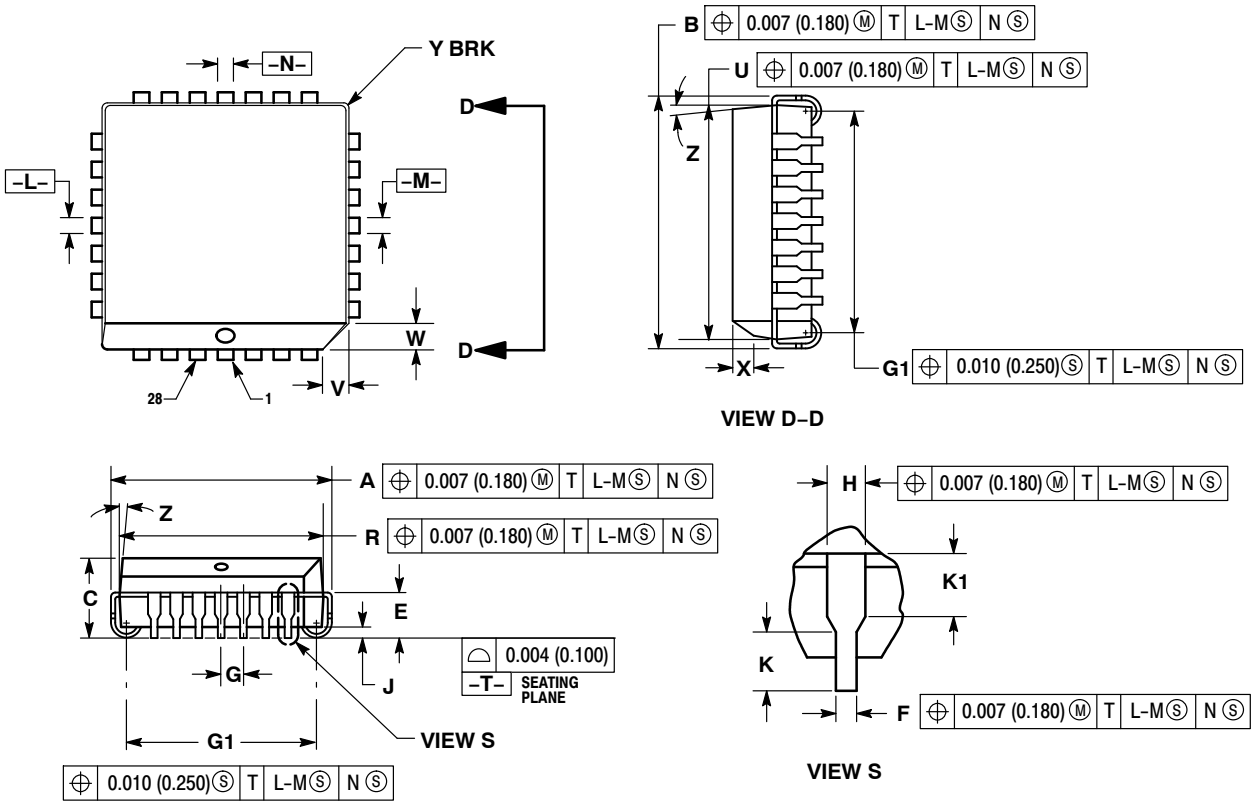
**AND8020/D** – Termination of ECL Logic Devices

**AND8066/D** – Interfacing with ECLinPS

**AND8090/D** – AC Characteristics of ECL Devices

## PACKAGE DIMENSIONS

**28 LEAD PLLC**
**FN SUFFIX**
CASE 776−02
ISSUE F




NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.485 | 0.495 | 12.32 | 12.57 |
| B | 0.485 | 0.495 | 12.32 | 12.57 |
| C | 0.165 | 0.180 | 4.20 | 4.57 |
| E | 0.090 | 0.110 | 2.29 | 2.79 |
| F | 0.013 | 0.021 | 0.33 | 0.53 |
| G | 0.050 BSC | | 1.27 BSC | |
| H | 0.026 | 0.032 | 0.66 | 0.81 |
| J | 0.020 | --- | 0.51 | --- |
| K | 0.025 | --- | 0.64 | --- |
| R | 0.450 | 0.456 | 11.43 | 11.58 |
| U | 0.450 | 0.456 | 11.43 | 11.58 |
| V | 0.042 | 0.048 | 1.07 | 1.21 |
| W | 0.042 | 0.048 | 1.07 | 1.21 |
| X | 0.042 | 0.056 | 1.07 | 1.42 |
| Y | --- | 0.020 | --- | 0.50 |
| Z | 2° | 10° | 2° | 10° |
| G1 | 0.410 | 0.430 | 10.42 | 10.92 |
| K1 | 0.040 | --- | 1.02 | --- |

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