MC100EL14

5V ECL 1:5 Clock Distribution Chip

The MC100EL14 is a low skew 1:5 clock distribution chip designed explicitly for low skew clock distribution applications. The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The EL14 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

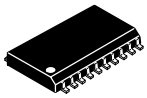
The common enable ($\overline{EN}$) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

Features

- 50 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Multiplexed Clock Input
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC} = 4.2 V to 5.7 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = −4.2 V to −5.7 V
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Internal Input Pull−down Resistors on All Inputs, Pull−up Resistors on Inverted Inputs

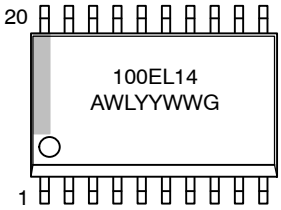
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SOIC−20L
DW SUFFIX
CASE 751D

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

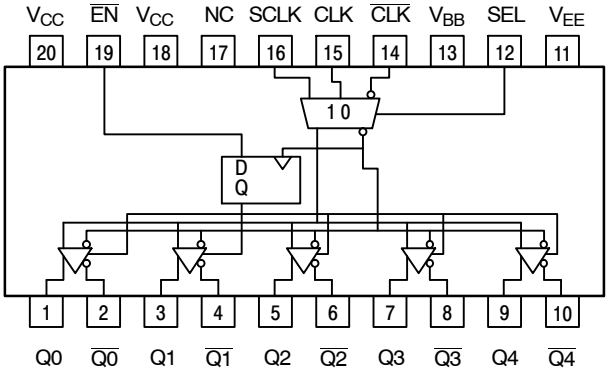
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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- Pb−Free Packages are Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



* All V_{CC} pins are tied together on the die.

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Logic Diagram and Pinout Assignment

Table 1. PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Diff Clock Inputs
SCLK	ECL Scan Clock Input
EN	ECL Sync Enable
SEL	ECL Clock Select Input
Q_{0-4}, $\overline{Q_{0-4}}$	ECL Diff Clock Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

Table 2. FUNCTION TABLE

CLK*	SCLK*	SEL*	$\overline{EN}$*	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L (Note)

1. On next negative transition of CLK or SCLK
**Pins will default low when left open.

Table 3. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		75 kΩ
ESD Protection	Human Body Model Machine Model Charge Device Model	> 2 kV > 200 V > 4 kV
Moisture Sensitivity (Note 2)	 Pb Pb−Free	 Level 1 Level 3
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		303 Devices
Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

2. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		−8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 −6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	SOIC−20L SOIC−20L	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	SOIC−20L	30 to 35	°C/W
T_{sol}	Wave Solder Pb Pb−Free	<2 to 3 sec @ 248°C <2 to 3 sec @ 260°C		265 265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. 100EL SERIES PECL DC CHARACTERISTICS V_{CC} = 5.0 V; V_{EE} = 0.0 V (Note 3)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		32	40		32	40		34	42	mA
V_{OH}	Output HIGH Voltage (Note 4)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 4)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single−Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Common Mode Range (Differential Configuration) (Note 5) V_{PP} < 500 mV $V_{PP} \geq$ 500 mV	1.3 1.5		4.6 4.6	1.2 1.4		4.6 4.6	1.2 1.4		4.6 4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Input and output parameters vary 1:1 with V_{CC}.V_{EE} can vary +0.8 V / −0.5 V.
4. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 V.
5. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}.The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak−to−peak voltage lies between V_{PP}(min) and 1 V.

Table 6. 100EL SERIES NECL DC CHARACTERISTICS V_{CC} = 0.0 V; V_{EE} = −5.0 V (Note 6)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		32	40		32	40		34	42	mA
V_{OH}	Output HIGH Voltage (Note 7)	−1085	−1005	−880	−1025	−955	−880	−1025	−955	−880	mV
V_{OL}	Output LOW Voltage (Note 7)	−1830	−1695	−1555	−1810	−1705	−1620	−1810	−1705	−1620	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	−1165		−880	−1165		−880	−1165		−880	mV
V_{IL}	Input LOW Voltage (Single−Ended)	−1810		−1475	−1810		−1475	−1810		−1475	mV
V_{BB}	Output Voltage Reference	−1.38		−1.26	−1.38		−1.26	−1.38		−1.26	V
V_{IHCMR}	Common Mode Range (Differential Configuration) (Note 8) V_{PP} < 500 mV $V_{PP} \geq$ 500 mV	−3.7 −3.5		−0.4 −0.4	−3.8 −3.6		−0.4 −0.4	−3.8 −3.6		−0.4 −0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. Input and output parameters vary 1:1 with V_{CC}.V_{EE} can vary +0.8 V / −0.5 V.
7. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 V.
8. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}.The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak−to−peak voltage lies between V_{PP}(min)and 1 V.

Table 7. AC CHARACTERISTICS V_{CC} = 5.0 V; V_{EE} = 0.0 V or V_{CC} = 0.0 V; V_{EE} = −5.0 V (Note 9)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency (See Figure 2, f_{MAX}/Jitter)		1			1			1		GHz
t_{PLH} t_{PHL}	Prop CLK to Q (Diff) Delay CLK to Q (SE) SCLK to Q	520 470 470		720 770 770	580 530 530	680 680 680	780 830 830	630 580 580		830 880 880	ps
t_{SKEW}	Part-to-Part Skew Within-Device Skew (Note 10)			200 50			200 50			200 50	ps
t_{JITTER}	Random Clock Jitter (RMS) @ 1 GHz (See Figure 2, f_{MAX}/Jitter)		1			1			1		ps
t_S	Setup Time $\overline{EN}$	0			0	−133		0			ps
t_H	Hold Time $\overline{EN}$	250			250	140		250			ps
V_{PP}	Input Swing (Note 11)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% − 80%)	230		500	230		500	230		500	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9. V_{EE} can vary +0.8 V / −0.5 V. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 V.
10. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.
11. V_{PP}(min) is the minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

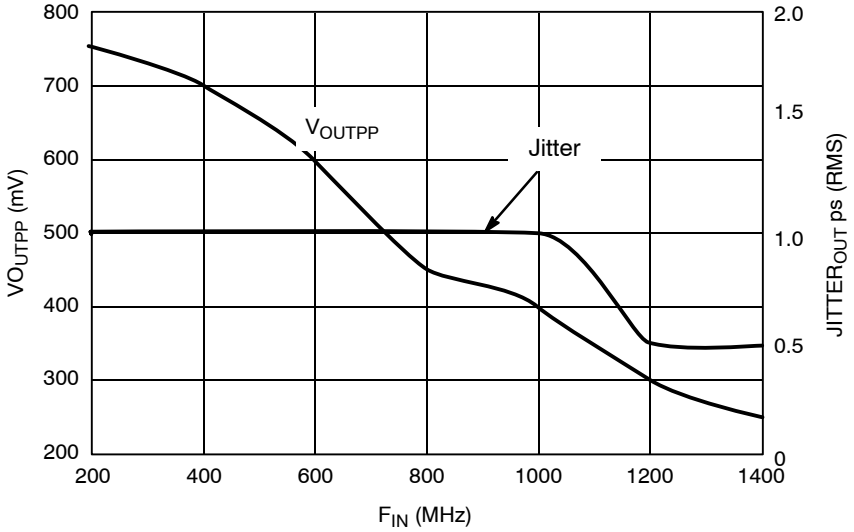


Figure 2. Output Voltage Amplitude / RMS Jitter vs. Input Frequency at Ambient Temperature (Typical)

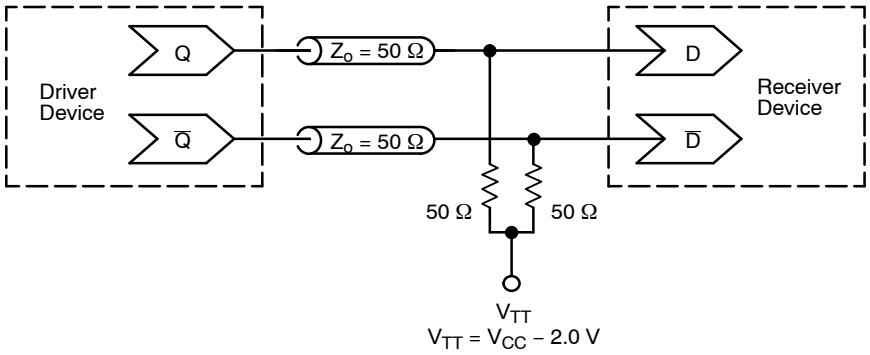


Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION4

Device	Package	Shipping†
MC100EL14DW	SOIC−20L	38 Units / Rail
MC100EL14DWG	SOIC−20L (Pb−Free)	38 Units / Rail
MC100EL14DWR2	SOIC−20L	1000 / Tape & Reel
MC100EL14DWR2G	SOIC−20L (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

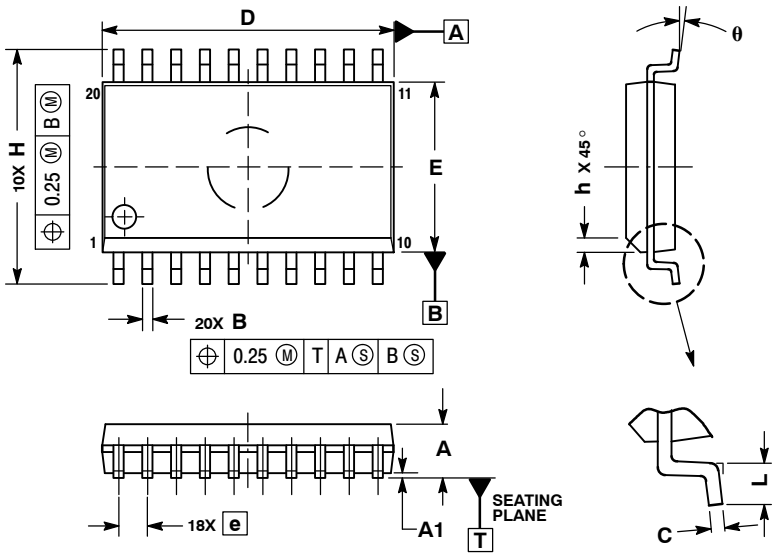
AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

SO−20 WB
CASE 751D−05
ISSUE G



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

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