MC100EP16VS

3.3V / 5V ECL Differential Receiver/Driver with Variable Output Swing



ON Semiconductor®

http://onsemi.com

Description

The MC100EP16VS is a differential receiver with variable output amplitude. The device is functionally equivalent to the 100EP16 with an input pin that controls the amplitude of the outputs.

The V_{CTRL} input pin controls the output amplitude of the EP16VS and is referenced to V_{CC}. (See Figure 4.) The operational range of the V_{CTRL} input is from ≤ V_{BB} (max output amplitude) to V_{CC} (min output amplitude). (See Figure 3.) A variable resistor between the V_{CC} and V_{BB} pins, with the wiper driving V_{CTRL}, can control the output amplitude. Typical application circuits and a V_{CTRL} Voltage vs. Output Amplitude graph are described in this data sheet. When left open, the V_{CTRL} pin will be internally pulled down to V_{EE} and operate as a standard EP16, with 100% output amplitude.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single−ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

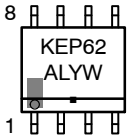
Features

- 220 ps Propagation Delay
- Maximum Frequency > 4 GHz Typical (See Graph)
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC} = 3.0 V to 5.5 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = −3.0 V to −5.5 V
- Open Input Default State
- Q Output Will Default LOW with Inputs Open or at V_{EE}
- Pb−Free Packages are Available

MARKING DIAGRAMS*

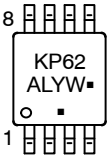


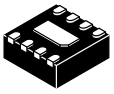
SOIC−8
D SUFFIX
CASE 751



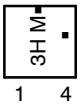


TSSOP−8
DT SUFFIX
CASE 948R





DFN8
MN SUFFIX
CASE 506AA



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

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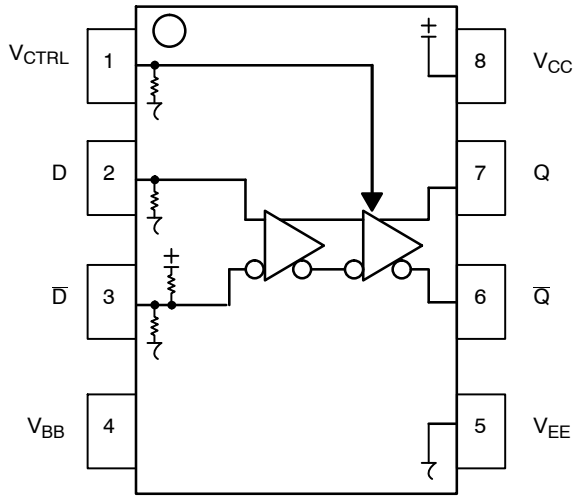


Figure 1. 8−Lead Pinout (Top View) **and Logic Diagram**

Table 1. PIN DESCRIPTION

PIN	FUNCTION	
D*, $\overline{D}$**	ECL Data Inputs	2, 3
Q, $\overline{Q}$	ECL Data Outputs	6, 7
V_{CTRL}*	Output Swing Control	1
V_{BB}	Reference Voltage Output	4
V_{CC}	Positive Supply	8
V_{EE}	Negative Supply	5
NC	No Connect	
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.	−

* Pins will default LOW when left open.

** Pins will default to $V_{CC}/2$ when left open.

Table 2. ATTRIBUTES

Characteristics		Value	
Internal Input Pulldown Resistor		75 kΩ	
Internal Input Pullup Resistor		37.5 kΩ	
ESD Protection	Human Body Model Machine Model Charged Device Model	> 4 kV > 200 V > 2 kV	
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Pb Pkg	Pb−Free Pkg
	SOIC−8 TSSOP−8 DFN8	Level 1 Level 1 Level 1	Level 1 Level 3 Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
Transistor Count		140 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test			

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		−6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 −6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	8 TSSOP	41 to 44 ± 5%	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	°C/W °C/W
T_{sol}	Wave Solder Pb Pb−Free	<2 to 3 sec @ 248°C <2 to 3 sec @ 260°C		265 265	°C
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 2)	DFN8	35 to 40	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board − 2S2P (2 signal, 2 power)

Table 4. DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 3)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	30	36	42	31	38	44	32	40	48	mA
V_{OH}	Output HIGH Voltage (Max Swing) (Note 4) $V_{CC} \geq V_{CTRL} \geq V_{EE}$	2155		2405	2155		2405	2155		2405	mV
V_{OL}	Output LOW Voltage (Max Swing) (Note 4) $V_{CTRL} \leq V_{BB}$	1355	1490	1605	1355	1520	1605	1355	1520	1605	mV
	$VCC \geq V_{CTRL} > V_{BB}$		See Fig.2			See Fig.2			See Fig.2		
	$V_{CTRL} = V_{CC}$ (Min Swing)	2105	2230	2355	2095	2220	2345	2065	2190	2315	
V_{IH}	D, $\overline{D}$ Input HIGH Voltage (Single−Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	D, $\overline{D}$ Input LOW Voltage (Single−Ended)	1355		1675	1355		1675	1355		1675	mV
V_{BB}	Output Voltage Reference	1805	1905	2005	1805	1905	2005	1805	1905	2005	mV
V_{CTRL}	Input Voltage (V_{CTRL})	V_{EE}		V_{CC}	V_{EE}		V_{CC}	V_{EE}		V_{CC}	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 5)	2.0		2.9	2.0		2.9	2.0		2.9	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 −150			0.5 −150			0.5 −150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to −2.2 V.
4. All loading with 50 Ω to V_{CC} − 2.0 V. V_{OH} does not change with V_{CTRL}. V_{OL} changes with V_{CTRL}. V_{CTRL} is referenced to V_{CC}.
5. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 5. DC CHARACTERISTICS, PECL V_{CC} = 5.0 V, V_{EE} = 0 V (Note 6)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	30	36	42	31	38	44	32	40	48	mA
V_{OH}	Output HIGH Voltage (Note 7) $V_{CC} > V_{CTRL} > V_{EE}$	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V_{OL}	Output LOW Voltage (Max Swing) (Note 7) $V_{CTRL} \le V_{BB}$	3055	3190	3305	3055	3220	3305	3055	3220	3305	mV
	$VCC \ge V_{CTRL} > V_{BB}$		See Fig.2			See Fig.2			See Fig.2		
	$V_{CTRL} = V_{CC}$ (Min Swing)	3805	3930	4055	3795	3920	4045	3765	3890	4015	
V_{IH}	D, $\overline{D}$ Input HIGH Voltage (Single−Ended)	3775		4120	3775		4120	3775		4120	mV
V_{IL}	D, $\overline{D}$ Input LOW Voltage (Single−Ended)	3055		3375	3055		3375	3055		3375	mV
V_{CTRL}	Input Voltage (V_{CTRL})	V_{EE}		V_{CC}	V_{EE}		V_{CC}	V_{EE}		V_{CC}	mV
V_{BB}	Output Voltage Reference	3505	3605	3705	3505	3605	3705	3505	3605	3705	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 8)	2.0		4.6	2.0		4.6	2.0		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 −150			0.5 −150			0.5 −150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +2.0 V to −0.5 V.
7. All loading with 50 Ω to V_{CC} − 2.0 V. V_{OH} does not change with V_{CTRL}. V_{OL} changes with V_{CTRL}. V_{CTRL} is referenced to V_{CC}.
8. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 6. DC CHARACTERISTICS, NECL V_{CC} = 0 V; V_{EE} = −5.5 V to −3.0 V (Note 9)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	30	36	42	31	38	44	32	40	48	mA
V_{OH}	Output HIGH Voltage (Note 10) $V_{CC} > V_{CTRL} > V_{EE}$	−1145	−1020	−895	−1145	−1020	−895	−1145	−1020	−895	mV
V_{OL}	Output LOW Voltage (Max Swing) (Note 10) $V_{CTRL} \le V_{BB}$	−1945	−1810	−1695	−1945	−1780	−1695	−1945	−1780	−1695	mV
	$VCC \ge V_{CTRL} > V_{BB}$		See Fig.2			See Fig.2			See Fig.2		
	$V_{CTRL} = V_{CC}$ (Min Swing)	−1195	−1070	−945	−1205	−1080	−955	−1235	−1110	−985	
V_{IH}	D, $\overline{D}$ Input HIGH Voltage (Single−Ended)	−1225		−880	−1225		−880	−1225		−880	mV
V_{IL}	D, $\overline{D}$ Input LOW Voltage (Single−Ended)	−1945		−1625	−1945		−1625	−1945		−1625	mV
V_{BB}	Output Voltage Reference	−1525	−1425	−1325	−1525	−1425	−1325	−1525	−1425	−1325	mV
V_{CTRL}	Input Voltage (V_{CTRL})	V_{EE}		V_{CC}	V_{EE}		V_{CC}	V_{EE}		V_{CC}	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 11)	V_{EE}+2.0		−0.4	V_{EE}+2.0		−0.4	V_{EE}+2.0		−0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 −150			0.5 −150			0.5 −150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9. Input and output parameters vary 1:1 with V_{CC}.
10. All loading with 50 Ω to V_{CC} − 2.0 V. V_{OH} does not change with V_{CTRL}. V_{OL} changes with V_{CTRL}. V_{CTRL} is referenced to V_{CC}.
11. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7. AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = −3.0 V to −5.5 V or V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0 V (Note 12)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency (See Figure 6. F_{max}/JITTER)		> 4			> 4			> 4		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential Max Swing Min Swing	150 90	220 150	280 210	150 90	220 150	280 210	160 100	240 160	300 220	ps
t_{SKEW}	Duty Cycle Skew (Note 13)		5.0	20		5.0	20		5.0	20	ps
t_{JITTER}	Cycle−to−Cycle Jitter (See Figure 6. F_{max}/JITTER)		0.2	< 1		0.2	< 1		0.2	< 1	ps
V_{PP}	Input Voltage Swing (Differential Configuration) (Note 14)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times Max Swing Q (20% − 80%) Min Swing	70 30	120 80	170 130	80 20	130 70	180 120	100 20	150 70	200 120	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

12. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} − 2.0 V.
13. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
14. V_{PP}(min) is minimum input swing for which AC parameters are guaranteed.

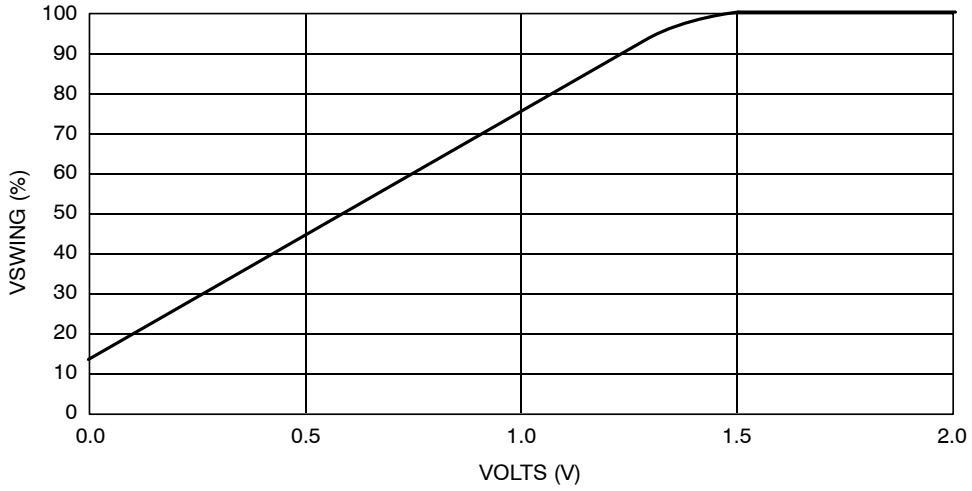


Figure 2. V_{CC} − V_{CTRL} (pin #1)

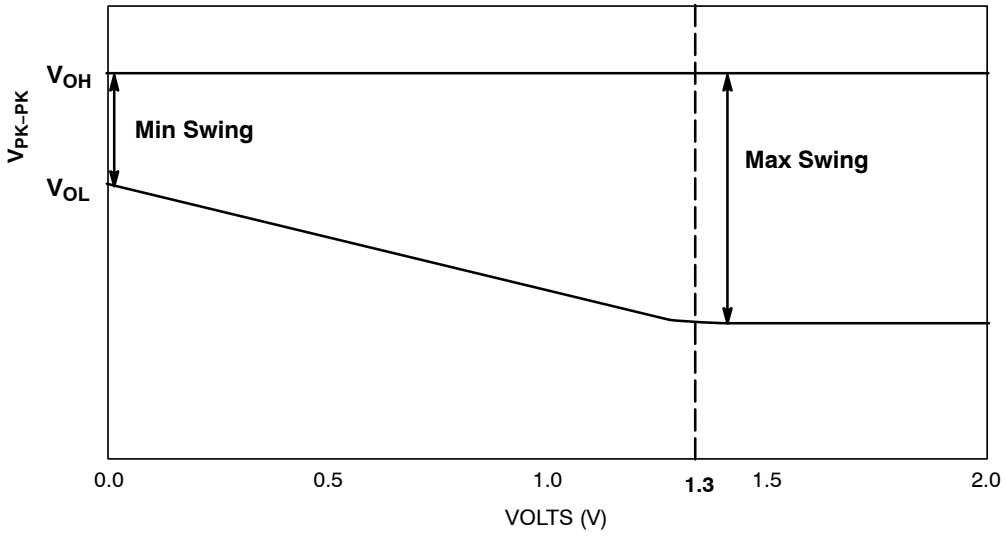


Figure 3. V_{CC} − V_{CTRL}

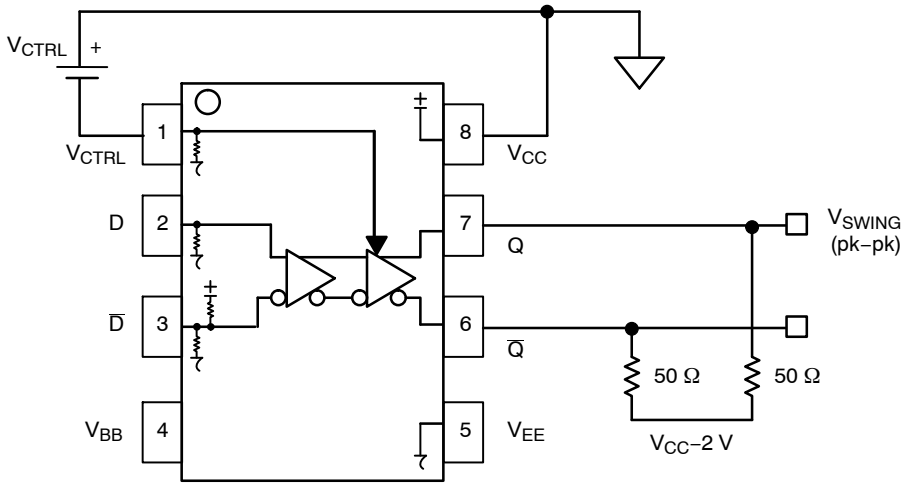


Figure 4. Voltage Source Implementation

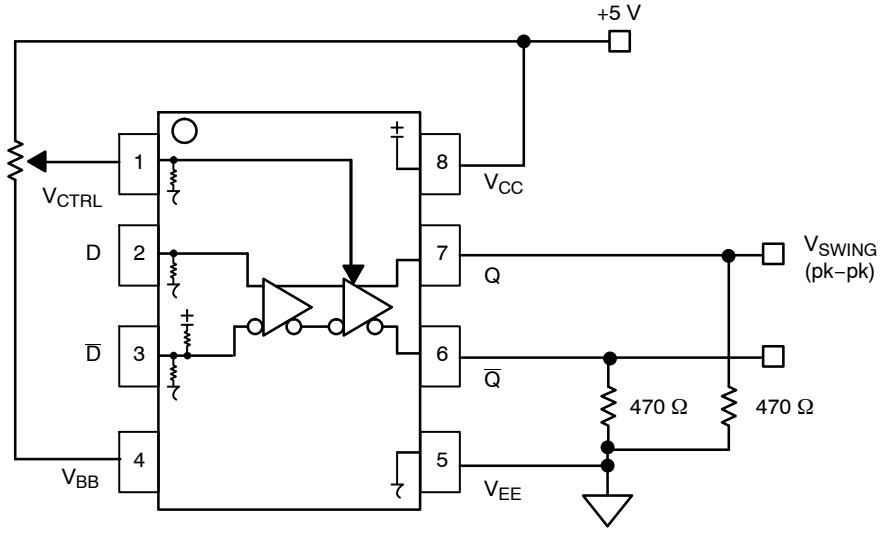


Figure 5. Alternative Implementation

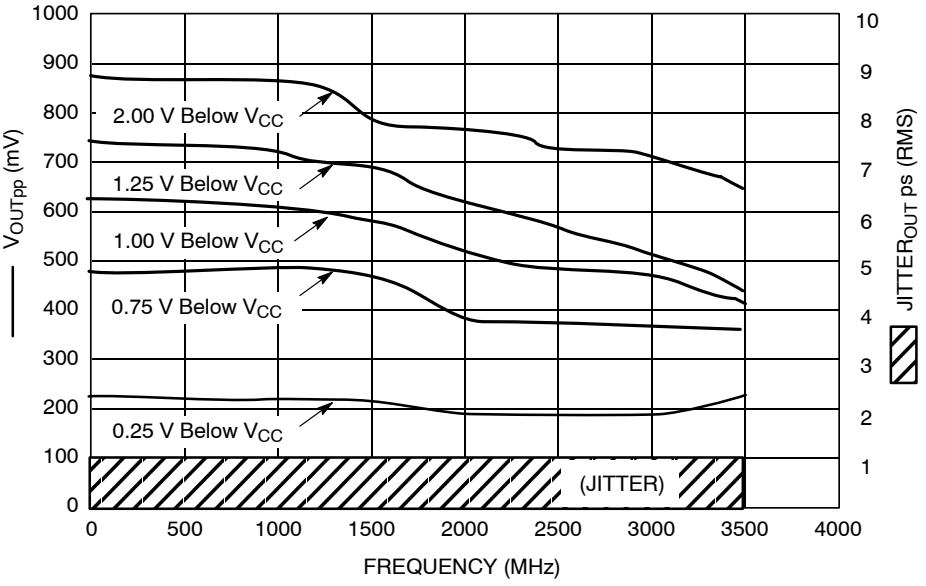


Figure 6. F_{max}/Jitter

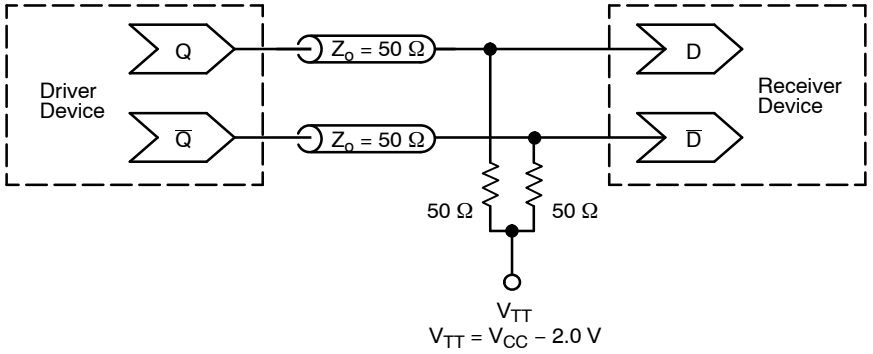


Figure 7. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Shipping†
MC100EP16VSD	SOIC−8	98 Units / Rail
MC100EP16VSDG	SOIC−8 (Pb−Free)	98 Units / Rail
MC100EP16VSDR2	SOIC−8	2500 / Tape & Reel
MC100EP16VSDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
MC3100EP16VSDT	TSSOP−8	100 Units / Rail
MC3100EP16VSDTG	TSSOP−8 (Pb−Free)	100 Units / Rail
MC100EP16VSDTR2	TSSOP−8	2500 / Tape & Reel
MC100EP16VSDTR2G	TSSOP−8 (Pb−Free)	2500 / Tape & Reel
MC100EP16VSMNR4	DFN8	1000 / Tape & Reel
MC100EP16VSMNR4G	DFN8 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

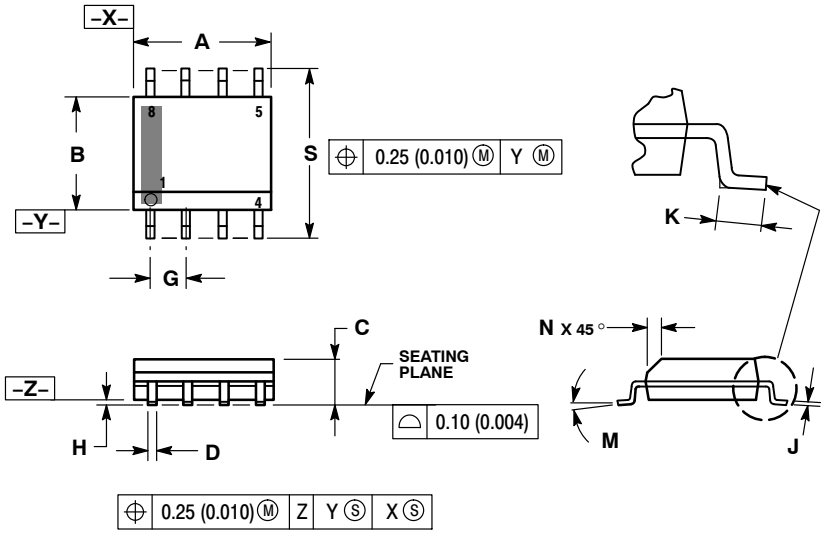
AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

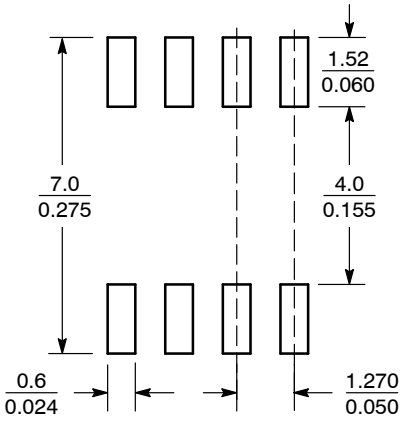
SOIC−8 NB
CASE 751−07
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

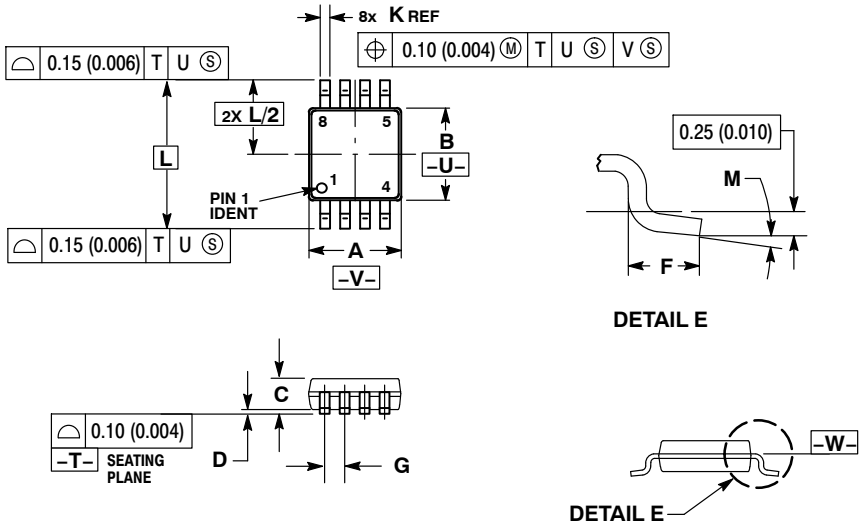


SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TSSOP−8
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948R−02
ISSUE A

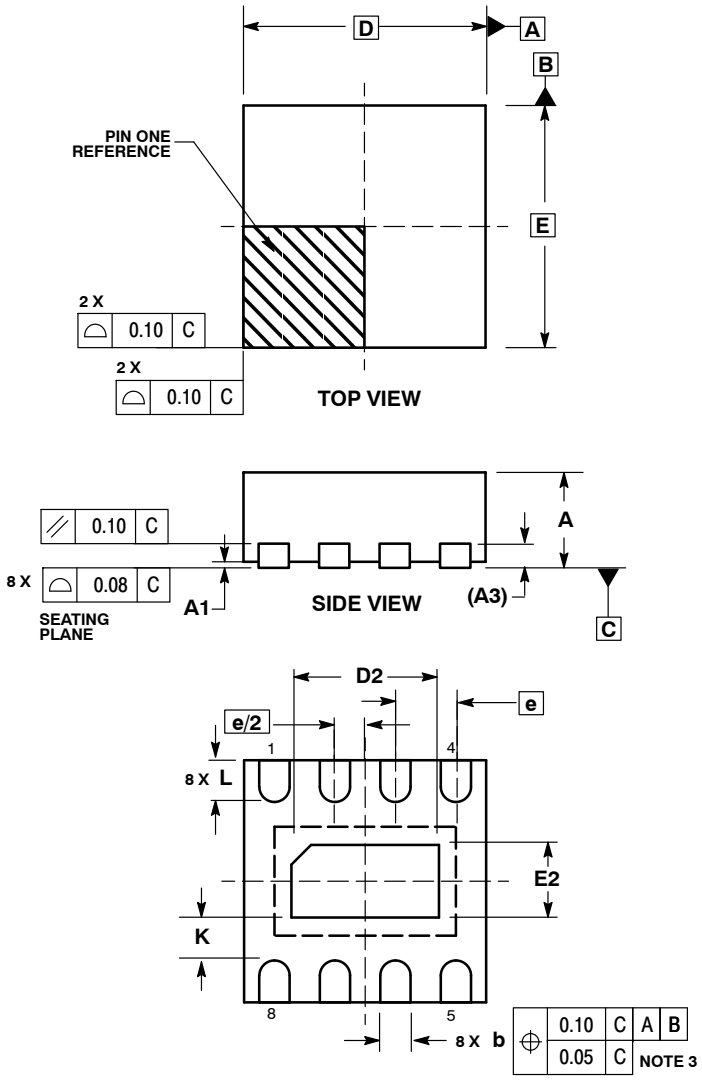


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

PACKAGE DIMENSIONS

DFN8
CASE 506AA−01
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.20	−−−
L	0.25	0.35

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