56F8322/56F8122

Data Sheet

Preliminary Technical Data

56F8300
16-bit Digital Signal Controllers

MC56F8322
Rev. 16
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Document Revision History

Version History	Description of Change
Rev 1.0	Pre-Release version, Alpha customers only
Rev 2.0	Initial Public Release
Rev 3.0	Corrected typo in **Table 10-4**, Flash Endurance is 10,000 cycles. Addressed additional grammar issues
Rev 4.0	Added Package Pins to GPIO table in Section 8. Clarification of $\overline{\text{TRST}}$ usage in this device. Replacing TBD Typical Min with values in **Table 10-17**. Editing grammar, spelling, consistency of language throughout family. Updated values in Regulator Parameters, **Table 10-9**, External Clock Operation Timing Requirements **Table 10-13**, SPI Timing, **Table 10-18**, ADC Parameters, **Table 10-24**, and IO Loading Coefficients at 10MHz, **Table 10-25**
Rev 5.0	Updated values in Power-On Reset Low Voltage **Table 10-6**.
Rev 6.0	Added **Section 4.8** , added addition text to **Section 6.9** on POR reset, added the word “access” to FM Error Interrupt in **Table 4-3**, removed min and max numbers; only documenting Typ. numbers for LVI in **Table 10-6**.
Rev 7.0	Updated numbers in **Table 10-7** and **Table 10-8** with more recent data, Corrected typo in **Table 10-3** in Pd characteristics
Rev 8.0	Replace any reference to Flash Interface Unit with Flash Memory Module; corrected typo on page 1 for ADC channel; changed example in **Section 2.2** ; added note on $V_{REFH}$and V_{REFLO} in **Table 2-2** and **Table 11-1**; corrected typo FIVAL1 and FIVAH1 in **Table 4-12**; removed unneccessary notes in **Table 10-12**; corrected temperature range in **Table 10-14**; added ADC calibration information to **Table 10-24** and new graphs in **Figure 10-20**.
Rev 9.0	Clarification to **Table 10-23**, corrected Digital Input Current Low (pull-up enabled) numbers in **Table 10-5**. Removed text and Table 10-2; replaced with note to **Table 10-1**.
Rev 10.0	Added 56F8122 information; edited to indicate differences in 56F8322 and 56F8122. Reformatted to reflect Freescale look and feel. Updated Temperature Sensor and ADC tables, then updated balance of electrical tables for consistency throughout family. Clarified I/O power description in **Table 2-2**, added note to **Table 10-7** and clarified **Section 12.3**.
Rev 11.0	Added output voltage maximum value and note to clarify in **Table 10-1**; also removed overall life expectancy note, since life expectancy is dependent on customer usage and must be determined by reliability engineering. Clarified value and unit measure for Maximum allowed P_D in **Table 10-3**. Corrected note about average value for Flash Data Retention in **Table 10-4**. Added new RoHS-compliant orderable part numbers in **Table 13-1**.
Rev 12.0	Deleted formula for Max Ambient Operating Temperature (Automotive) and Max Ambient Operating Temperature (Industrial) in **Table 10-4**. Added RoHS-compliance and “pb-free” language to back cover.
Rev 13.0	Added information/corrected state during reset in **Table 2-2**. Clarified external reference crystal frequency for PLL in **Table 10-14** by increasing maximum value to 8.4MHz.

Document Revision History (Continued)

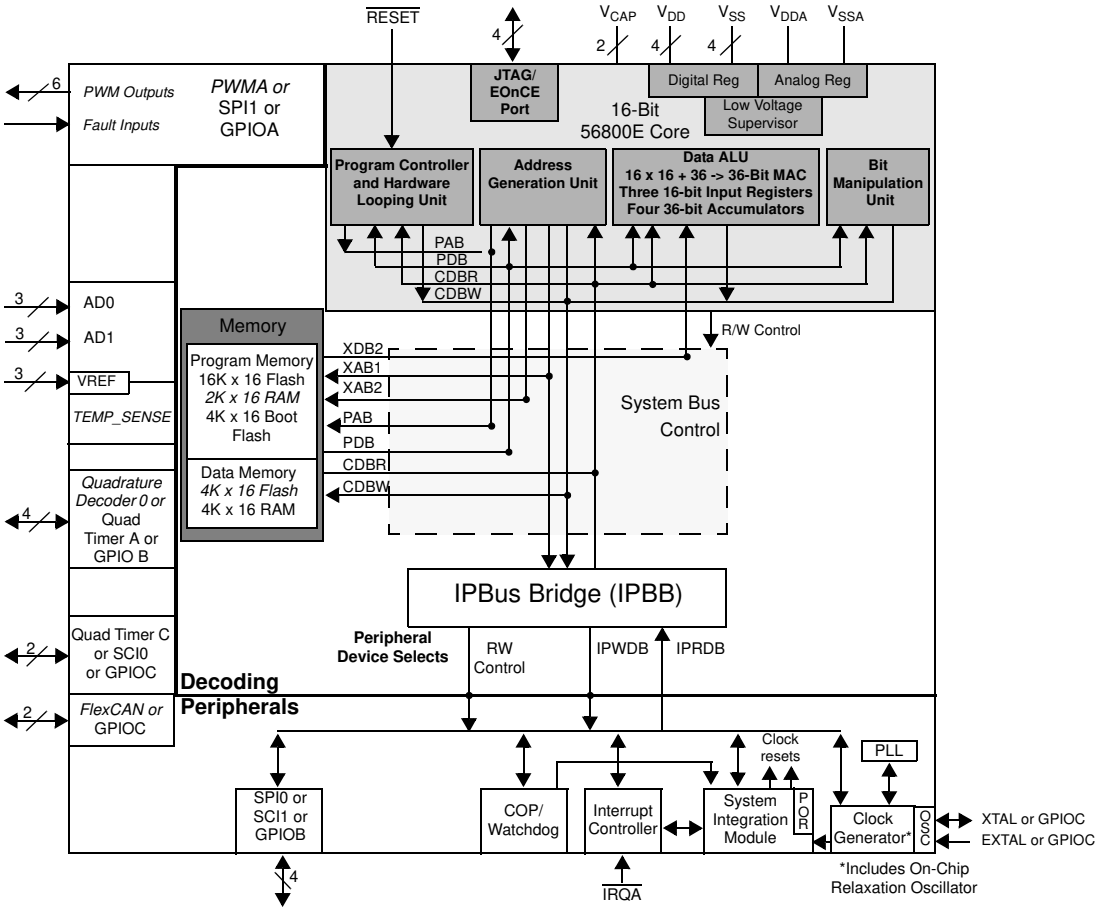
Version History	Description of Change
Rev 14.0	Replaced “Tri-stated” with an explanation in State During Reset column in **Table 2-2**.
Rev. 15	Added the following note to the description of the TMS signal in **Table 2-2**: **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.
Rev. 16	Changed the “Frequency Accuracy” specification in **Table 10-16** (was ±2.0%, is +2 / -3%).

Please see http://www.freescale.com for the most current data sheet revision.

56F8322/56F8122 General Description

Note: *Features in italics are NOT available in the 56F8122 device.*

- Up to 60 MIPS at 60MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- 32KB Program Flash
- *4KB Program RAM*
- *8KB Data Flash*
- 8KB Data RAM
- 8KB Boot Flash
- *One 6-channel PWM module*
- Two 3-channel 12-bit ADCs
- *Temperature Sensor*
- *One Quadrature Decoder*
- *FlexCAN module*
- Up to two Serial Communication Interfaces (SCIs)
- Up to two Serial Peripheral Interfaces (SPIs)
- Two general-purpose Quad Timers
- Computer Operating Properly (COP)/Watchdog
- On-Chip Relaxation Oscillator
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging
- Up to 21 GPIO lines
- 48-pin LQFP Package



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Part 1 Overview

1.1 56F8322/56F8122 Features

1.1.1 Core

- Efficient 16-bit 56800E family controller engine with dual Harvard architecture
- Up to 60 Million Instructions Per Second (MIPS) at 60MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- Arithmetic and logic multi-bit shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses
- Four internal data buses
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/EOnCE debug programming interface

1.1.2 Differences Between Devices

Table 1-1 outlines the key differences between the 56F8322 and 56F8122 devices.

Table 1-1 Device Differences

Feature	56F8322	56F8122
Guaranteed Speed	60MHz/60 MIPS	40MHz/40 MIPS
Program RAM	4KB	Not Available
Data Flash	8KB	Not Available
PWM	1 x 6	Not Available
CAN	1	Not Available
Quadrature Decoder	1 x 4	Not Available
Temperature Sensor	1	Not Available
Dedicated GPIO	—	5

1.1.3 Memory

Note: *Features in italics are NOT available in the 56F8122 device.*

- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Flash security protection
- On-chip memory, including a low-cost, high-volume Flash solution
  - 32KB of Program Flash
  - *4KB of Program RAM*
  - *8KB of Data Flash*
  - 8KB of Data RAM
  - 8KB of Boot Flash
- EEPROM emulation capability

1.1.4 Peripheral Circuits

Note: *Features in italics are NOT available in the 56F8122 device.*

- *One Pulse Width Modulator module with six PWM outputs and one Fault input; fault-tolerant design with dead time insertion; supports both center-aligned and edge-aligned modes*
- Two 12-bit, Analog-to-Digital Converters (ADCs), which support two simultaneous conversions with dual, 3-pin multiplexed inputs; ADC *and PWM modules* can be synchronized through Timer C, Channel 2
- *Temperature Sensor is tied internally to analog input (ANA7) to monitor the on-chip temperature*
- Two 16-bit Quad Timer modules (TMR) totaling six pins:
  - In the 56F8322, Timer A works in conjunction with Quad Decoder 0 and Timer C works in conjunction with the PWMA and ADCA
  - In the 56F8122, Timer C works in conjunction with ADCA
- *One Quadature Decoder which works in conjunction with Quad Timer A*
- *FlexCAN (Can Version 2.0 B-compliant) module with 2-pin port for transmit and receive*
- Up to two Serial Communication Interfaces (SCIs)
- Up to two Serial Peripheral Interfaces (SPIs)
- Computer Operating Properly (COP)/Watchdog timer
- One dedicated external interrupt pin
- 21 General Purpose I/O (GPIO) pins
- Integrated Power-On Reset and Low-Voltage Interrupt Module
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, processor speed-independent, real-time debugging
- Software-programmable, Phase Lock Loop (PLL)
- On-chip relaxation oscillator

1.1.5 Energy Information

- Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs
- On-board 3.3V down to 2.6V voltage regulator for powering internal logic and memories
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Wait and Stop modes available
- ADC smart power management
- Each peripheral can be individually disabled to save power

1.2 Device Description

The 56F8322 and 56F8122 are members of the 56800E core-based family of controllers. Each combines, on a single chip, the processing power of a Digital Signal Processor (DSP) and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of their low cost, configuration flexibility, and compact program code, the 56F8322 and 56F8122 are well-suited for many applications. These devices include many peripherals that are especially useful for *automotive* control (56F8322 only); industrial control and networking; motion control; home appliances; general purpose inverters; smart sensors; fire and security systems; power management; and medical monitoring applications.

The 56800E core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C Compilers to enable rapid development of optimized control applications.

The 56F8322 and 56F8122 support program execution from internal memories. Two data operands can be accessed from the on-chip data RAM per instruction cycle. These devices also provide one external dedicated interrupt line and up to 21 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

1.2.1 56F8322 Features

The 56F8322 controller includes 32KB of Program Flash and 8KB of Data Flash, each programmable through the JTAG port, and 4KB of Program RAM and 8KB of Data RAM. A total of 8KB of Boot Flash is incorporated for easy customer inclusion of field-programmable software routines that can be used to program the main Program and Data Flash memory areas. Both Program and Data Flash memories can be independently bulk erased or erased in pages. Program Flash page erase size is 1KB. Boot and Data Flash page erase size is 512 bytes. The Boot Flash memory can also be either bulk or page erased.

A key application-specific feature of the 56F8322 is the inclusion of one Pulse Width Modulator (PWM) module. This module incorporates three complementary, individually programmable PWM signal output pairs and is also capable of supporting six independent PWM functions to enhance motor control functionality. Complementary operation permits programmable dead time insertion, distortion correction via current sensing by software, and separate top and bottom output polarity control. The up-counter value

is programmable to support a continuously variable PWM frequency. Edge-aligned and center-aligned synchronous pulse width control (0% to 100% modulation) is supported. The device is capable of controlling most motor types: ACIM (AC Induction Motors); both BDC and BLDC (Brush and Brushless DC motors); SRM and VRM (Switched and Variable Reluctance Motors); and stepper motors. The PWM incorporates fault protection and cycle-by-cycle current limiting with sufficient output drive capability to directly drive standard optoisolators. A “smoke-inhibit”, write-once protection feature for key parameters is also included. A patented PWM waveform distortion correction circuit is also provided. Each PWM is double-buffered and includes interrupt controls to permit integral reload rates to be programmable from 1/2 (center-aligned mode only) to 16. The PWM module provides reference outputs to synchronize the Analog-to-Digital Converters (ADCs) through Quad Timer C, channel 2.

The 56F8322 incorporates one Quadrature Decoder capable of capturing all four transitions on the two-phase inputs, permitting generation of a number proportional to actual position. Speed computation capabilities accommodate both fast- and slow-moving shafts. An integrated watchdog timer in the Quadrature Decoder can be programmed with a time-out value to alarm when no shaft motion is detected. Each input is filtered to ensure only true transitions are recorded.

This controller also provides a full set of standard programmable peripherals that include two Serial Communications Interfaces (SCIs), two Serial Peripheral Interfaces (SPIs), two Quad Timers and FlexCAN. Any of these interfaces can be used as General Purpose Input/Outputs (GPIOs) if that function is not required. A Flex Controller Area Network interface (CAN Version 2.0 B-compliant) and an internal interrupt controller are also a part of the 56F8322.

1.2.2 56F8122 Features

The 56F8122 controller includes 32KB of Program Flash, programmable through the JTAG port, and 8KB of Data RAM. A total of 8KB of Boot Flash is incorporated for easy customer inclusion of field-programmable software routines that can be used to program the main Program Flash memory area. The Program Flash memory can be independently bulk erased or erased in pages; Program Flash page erase size is 1KB. The Boot Flash memory can also be either bulk or page erased.

This controller also provides a full set of standard programmable peripherals that include two Serial Communications Interfaces (SCIs), two Serial Peripheral Interfaces (SPIs), and two Quad Timers. Any of these interfaces can be used as General Purpose Input/Outputs (GPIOs) if that function is not required. An internal interrupt controller is also a part of the 56F8122.

1.3 Award-Winning Development Environment

Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.

The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs), demonstration board kit and development system cards will support concurrent engineering. Together, PE, CodeWarrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Architecture Block Diagram

Note: *Features in italics are NOT available in the 56F8122 device and are shaded in the following figures.*

The 56F8322/56F8122 architecture is shown in **Figure 1-1** and **Figure 1-2**. **Figure 1-1** illustrates how the 56800E system buses communicate with internal memories and the IPBus Bridge. **Table 1-2** lists the internal buses in the 56800E architecture and provides a brief description of their function. **Figure 1-2** shows the peripherals and control blocks connected to the IPBus Bridge. The figures do not show the on-board regulator and power and ground signals. They also do not show the multiplexing between peripherals or the dedicated GPIOs. Please see **Part 2 Signal/Connection Descriptions**, to see which signals are multiplexed with those of other peripherals.

Also shown in **Figure 1-2** are connections between the *PWM*, Timer C and ADC blocks. These connections allow the *PWM and/or* Timer C to control the timing of the start of ADC conversions. The Timer C, Channel 2, output can generate periodic start (SYNC) signals to the ADC to start its conversions. *In another operating mode, the PWM load interrupt (SYNC output) signal is routed internally to the Timer C, Channel 2, input as indicated. The timer can then be used to introduce a controllable delay before generating its output signal. The timer output then triggers the ADC.* To fully understand this interaction, please see the **56F8300 Peripheral User Manual** for clarification on the operation of all three of these peripherals.

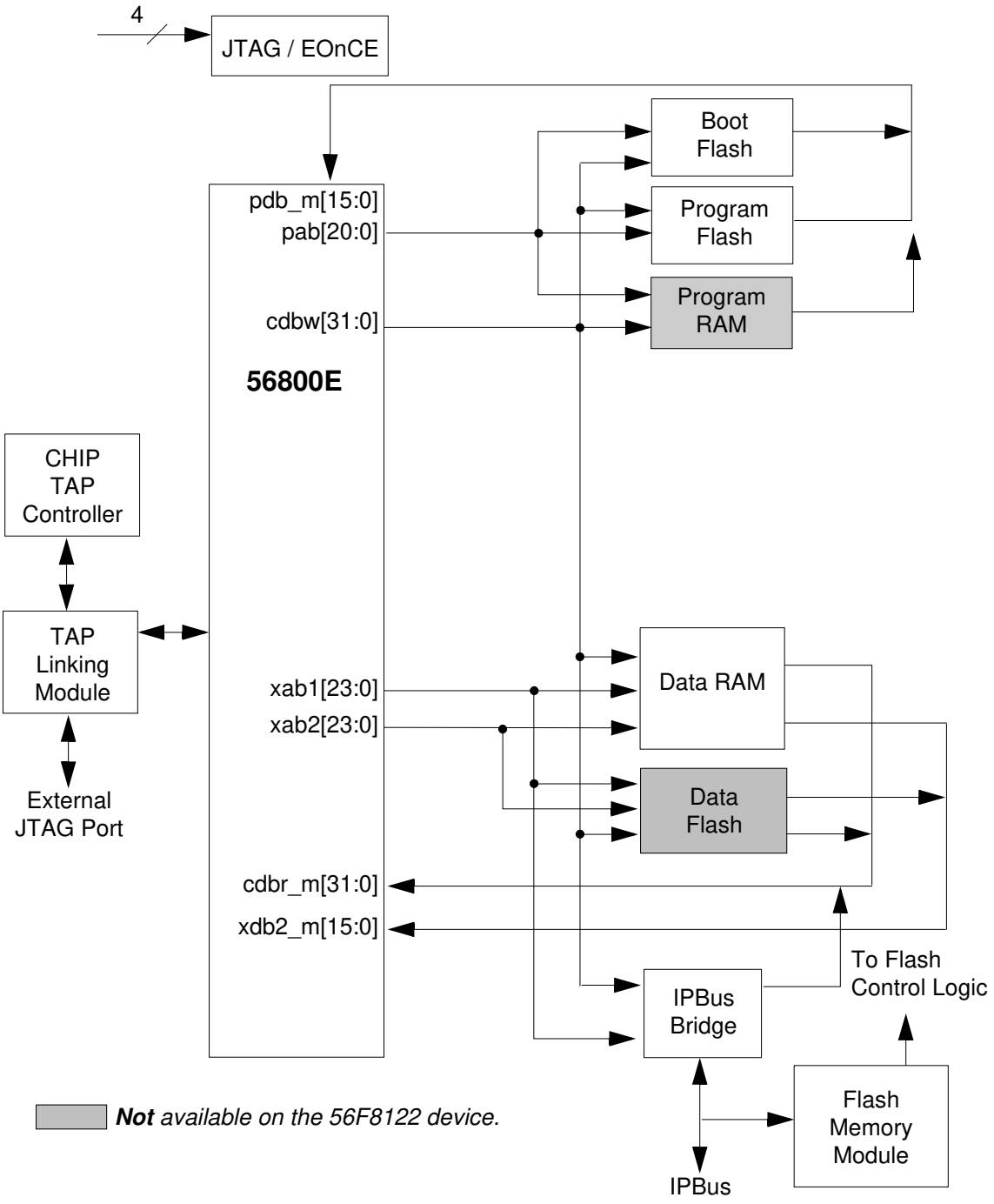


Figure 1-1 System Bus Interfaces

Note: Flash memories are encapsulated within the Flash Memory Module (FM). Flash control is accomplished by the I/O to the FM over the peripheral bus, while reads and writes are completed between the core and the Flash memories.

Note: The primary data RAM port is 32 bits wide. Other data ports are 16 bits.

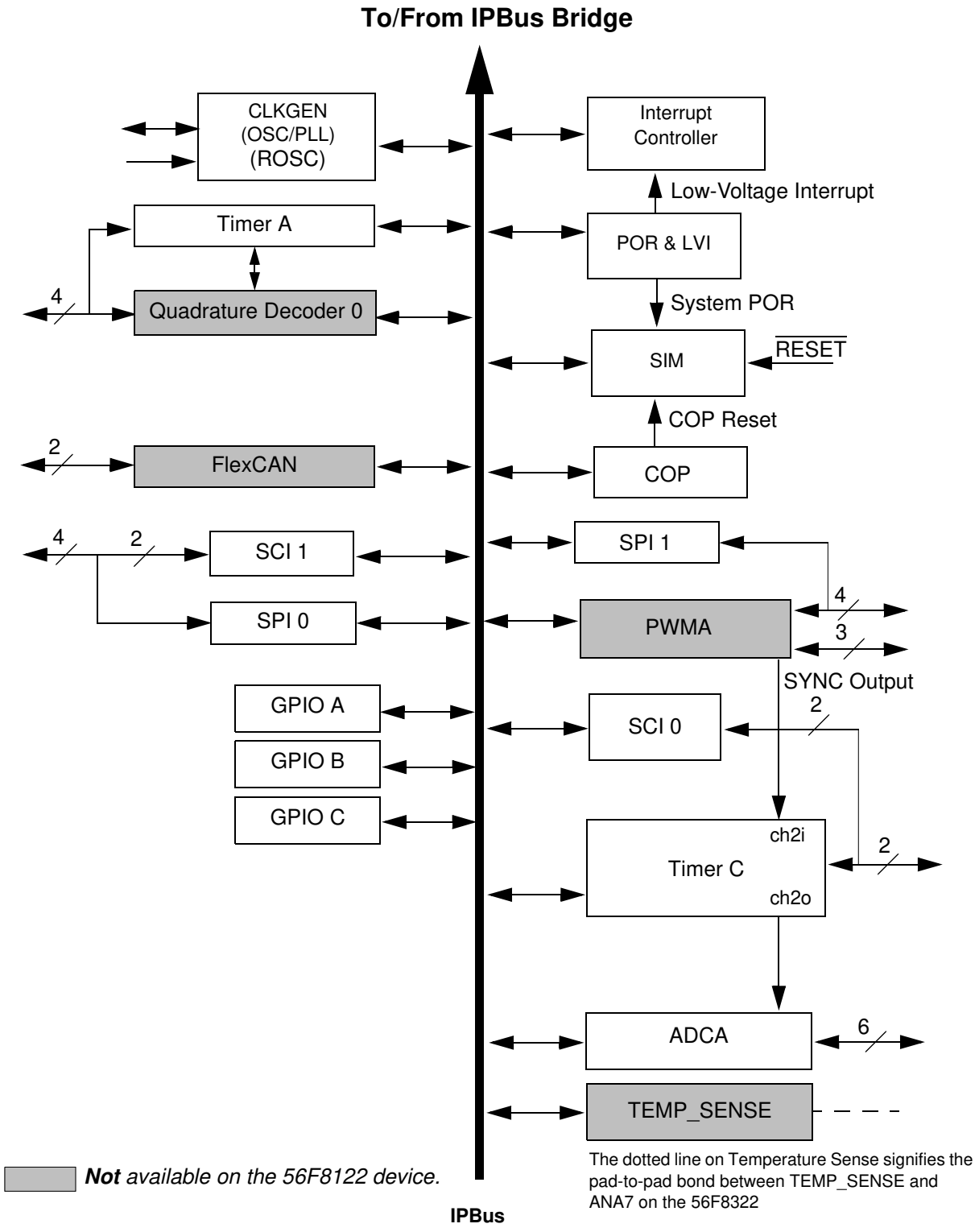


Figure 1-2 Peripheral Subsystem

Table 1-2 Bus Signal Names

Name	Function
Program Memory Interface	
pdb_m[15:0]	Program data bus for instruction word fetches or read operations.
cdbw[15:0]	Primary core data bus used for program memory writes. (Only these 16 bits of the cdbw[31:0] bus are used for writes to program memory.)
pab[20:0]	Program memory address bus. Data is returned on pdb_m bus.
Primary Data Memory Interface Bus	
cdbr_m[31:0]	Primary core data bus for memory reads. Addressed via xab1 bus.
cdbw[31:0]	Primary core data bus for memory writes. Addressed via xab1 bus.
xab1[23:0]	Primary data address bus. Capable of addressing bytes[1], words, and long data types. Data is written on cdbw and returned on cdbr_m. Also used to access memory-mapped I/O.
Secondary Data Memory Interface	
xdb2_m[15:0]	Secondary data bus used for secondary data address bus xab2 in the dual memory reads.
xab2[23:0]	Secondary data address bus used for the second of two simultaneous accesses. Capable of addressing only words. Data is returned on xdb2_m.
Peripheral Interface Bus	
IPBus [15:0]	Peripheral bus accesses all on-chip peripherals registers. This bus operates at the same clock rate as the Primary Data Memory and therefore generates no delays when accessing the processor. Write data is obtained from cdbw. Read data is provided to cdbr_m.

1. Byte accesses can only occur in the bottom half of the memory address space. The MSB of the address will be forced to 0.

1.5 Product Documentation

The documents listed in **Table 1-3** are required for a complete description and proper design with the 56F8322 and 56F8122 devices. Documentation is available from local Freescale distributors, Freescale semiconductor sales offices, Freescale Literature Distribution Centers, or online at **http://www.freescale.com/semiconductors/**.

Table 1-3 Chip Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E family architecture, 16-bit controller core processor, and the instruction set	DSP56800ERM
56F8300 Peripheral User Manual	Detailed description of peripherals of the 56800E family of devices	MC56F8300UM
56F8300 SCI/CAN Bootloader User Manual	Detailed description of the SCI/CAN Bootloaders 56F8300 family of devices	MC56F83xxBLUM
56F8322/56F8122 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	MC56F8322
Errata	Details any chip issues that might be present	MC56F8322E MC56F8122E

1.6 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
“asserted”	A high true (active high) signal is high or a low true (active low) signal is low.
“deasserted”	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:

Signal/Symbol	Logic State	Signal State	Voltage[1]
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

2.1 Introduction

The input and output signals of the 56F8322 and 56F8122 devices are organized into functional groups, as detailed in **Table 2-1** and as illustrated in **Figure 2-1** and **Figure 2-2**. In **Table 2-2**, each table row describes the signal or signals present on a pin.

Table 2-1 Functional Group Pin Allocations

Functional Group	Number of Pins in Package	
	56F8322	56F8122
Power (V_{DD} or V_{DDA})	5	5
Ground (V_{SS} or V_{SSA})	5	5
Supply Capacitors & V_{PP}[1]	2	2
PLL and Clock	2	2
Interrupt and Program Control	2	2
Pulse Width Modulator (PWM) Ports[2]	7	—
Serial Peripheral Interface (SPI) Port 0[3]	4	8
Quadrature Decoder Port 0[4]	4	—
CAN Ports	2	—
Analog to Digital Converter (ADC) Ports	9	9
Timer Module Port C[5]	2	2
Timer Module Port A	—	4
JTAG/Enhanced On-Chip Emulation (EOnCE)	4	4
Temperature Sense[6]	0	—
Dedicated GPIO	—	5

1. The V_{PP} input shares the $\overline{IRQA}$ input
2. Pins in this section can function as SPI #1 and GPIO.
3. Pins in this section can function as SCI #1 and GPIO.
4. Alternately, can function as Quad Timer A pins or GPIO.
5. Pins can function as SCI #0 and GPIO.
6. Tied internally to ANA7

Note: See **Table 1-1** for 56F8122 functional differences.

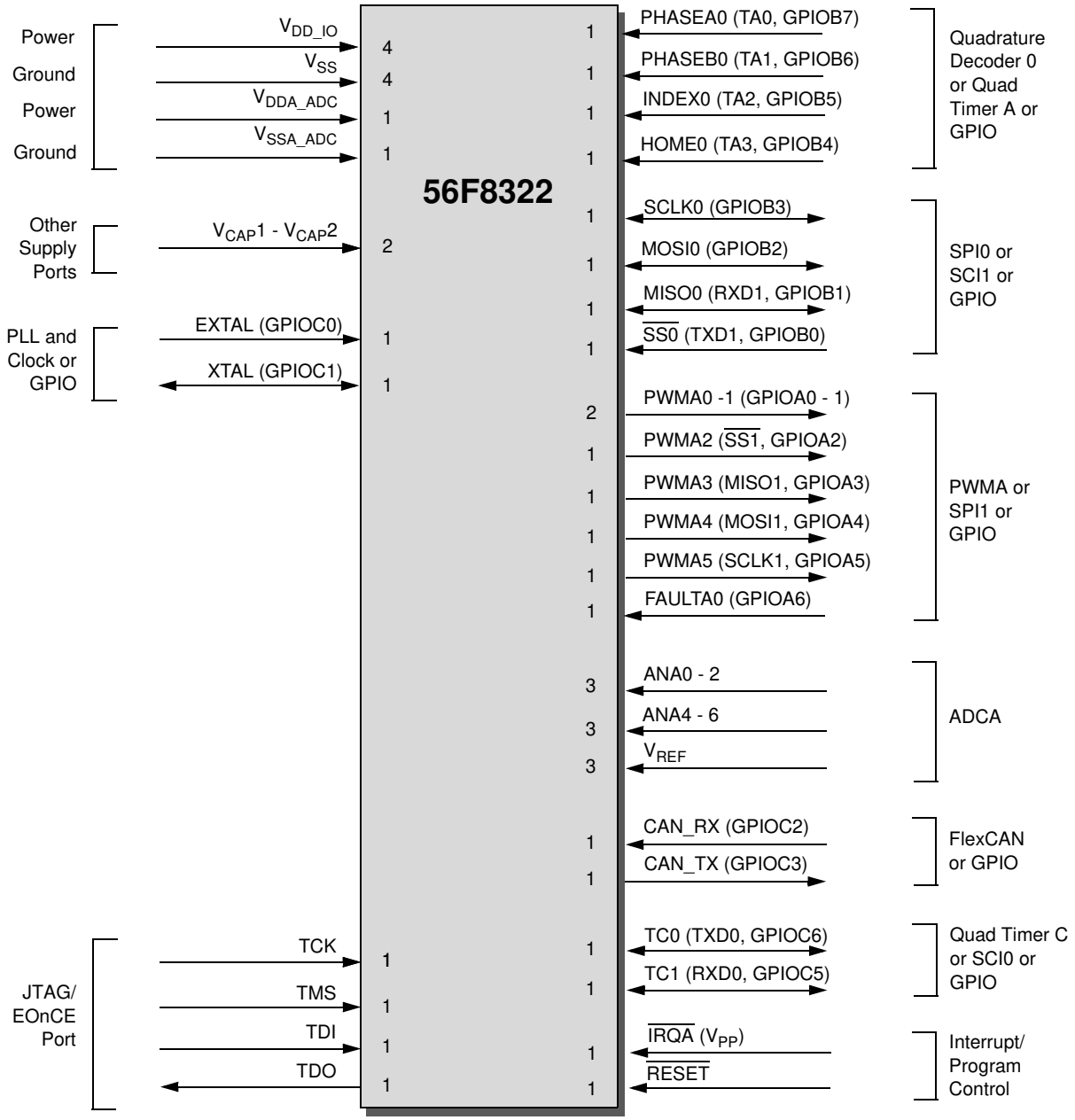


Figure 2-1 56F8322 Signals Identified by Functional Group (48-Pin LQFP)

Note: V_{REFH} is tied to V_{DDA} and V_{REFLO} is tied to V_{SSA} inside this package

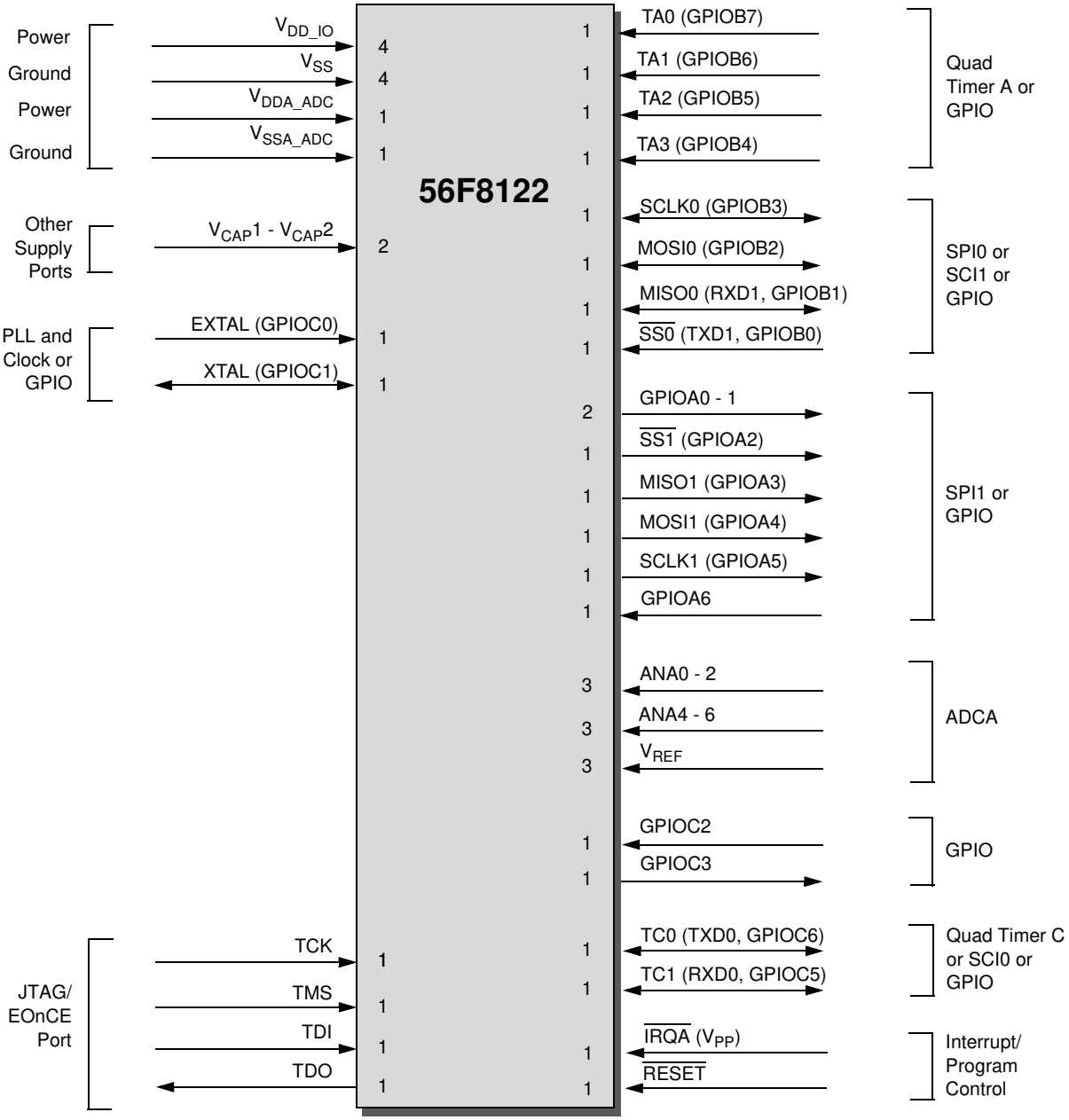


Figure 2-2 56F8122 Signals Identified by Functional Group (48-Pin LQFP)

2.2 Signal Pins

After reset, each pin is configured for its primary function (listed first). In the 56F8122, after reset, each pin must be configured for the desired function. The initialization software will configure each pin for the function listed first for each pin, as shown in Table 2-2. Any alternate functionality must be programmed.

Note: *Signals in italics are not available in the 56F8122 device.*

If the "State During Reset" lists more than one state for a pin, the first state is the actual reset state. Other states show the reset condition of the alternate function, which you get if the alternate pin function is selected without changing the configuration of the alternate peripheral. For example, the SCLK0/GPIOB3 pin shows that it is tri-stated during reset. If the GPIOB_PER is changed to select the GPIO function of the pin, it will become an input if no other registers are changed.

Table 2-2 Signal and Package Information for the 48-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
V_{DD_IO}	5	Supply		**I/O Power** — This pin supplies 3.3V power to the chip I/O interface and also the Processor core throught the on-chip voltage regulator, if it is enabled.
V_{DD_IO}	14			
V_{DD_IO}	34			
V_{DD_IO}	44			
V_{DDA_ADC}	30	Supply		**ADC Power** — This pin supplies 3.3V power to the ADC modules. It must be connected to a clean analog power supply.
V_{SS}	10	Supply		**Ground** — These pins provide ground for chip logic and I/O drivers.
V_{SS}	13			
V_{SS}	31			
V_{SS}	45			
V_{SSA_ADC}	29	Supply		**ADC Analog Ground** — This pin supplies an analog ground to the ADC modules.
$V_{CAP}1$	43	Supply	Supply	V_{CAP}**1 - 2** — Connect each pin to a 2.2µF or greater bypass capacitor in order to bypass the core logic voltage regulator, required for proper chip operation.
$V_{CAP}2$	17			

Table 2-2 Signal and Package Information for the 48-Pin LQFP (Continued)

Signal Name	Pin No.	Type	State During Reset	Signal Description
EXTAL **(GPIOC0)**	32	Input/ Schmitt Input/ Output	Input	**External Crystal Oscillator Input** — This input can be connected to an 8MHz external crystal. If an external clock is used, XTAL must be used as the input and EXTAL connected to V_{SS}. The input clock can be selected to provide the clock directly to the core. This input clock can also be selected as the input clock for the on-chip PLL. **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is an EXTAL input with pull-ups disabled.
XTAL **(GPIOC1)**	33	Output Schmitt Input/ Output	Output	**Crystal Oscillator Output** — This output connects the internal crystal oscillator output to an external crystal. If an external clock is used, XTAL must be used as the input and EXTAL connected to V_{SS}. The input clock can be selected to provide the clock directly to the core. This input clock can also be selected as the input clock for the on-chip PLL. **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is an XTAL input with pull-ups disabled.
TCK	39	Schmitt Input	Input, pulled low internally	**Test Clock Input** — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pull-down resistor. A Schmitt trigger input is used for noise immunity.
TMS	40	Schmitt Input	Input, pulled high internally	**Test Mode Select Input** — This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.
TDI	41	Schmitt Input	Input, pulled high internally	**Test Data Input** — This input pin provides a serial input data stream to the JTAG/EOnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
TDO	42	Output	In reset, output is disabled, pull-up is enabled	**Test Data Output** — This tri-stateable output pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and changes on the falling edge of TCK.

Table 2-2 Signal and Package Information for the 48-Pin LQFP (Continued)

Signal Name	Pin No.	Type	State During Reset	Signal Description
PHASEA0	38	Schmitt Input	Input, pull-up enabled	**Phase A** — Quadrature Decoder 0, PHASEA input
(TA0)		Schmitt Input/ Output		**TA0** — Timer A, Channel 0
(GPIOB7)		Schmitt Input/ Output		**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(oscillator_ clock)		Output		**Clock Output** - can be used to monitor the internal oscillator clock signal (see **Section 6.5.7** CLKO Select Register, SIM_CLKOSR). In the 56F8322, the default state after reset is PHASEA0. In the 56F8122, the default state is not one of the functions offered and must be reconfigured.
PHASEB0	37	Schmitt Input	Input, pull-up enabled	**Phase B** — Quadrature Decoder 0, PHASEB input
(TA1)		Schmitt Input/ Output		**TA1** — Timer A ,Channel 1
(GPIOB6)		Schmitt Input/ Output		**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(SYS_CLK2)		Output		**Clock Output** - can be used to monitor the internal SYS_CLK2 signal (see **Section 6.5.7** CLKO Select Register, SIM_CLKOSR). In the 56F8322, the default state after reset is PHASEB0. In the 56F8122, the default state is not one of the functions offered and must be reconfigured.

Table 2-2 Signal and Package Information for the 48-Pin LQFP (Continued)

Signal Name	Pin No.	Type	State During Reset	Signal Description
INDEX0	36	Schmitt Input	Input, pull-up enabled	**Index** — Quadrature Decoder 0, INDEX input
(TA2)		Schmitt Input/ Output		**TA2** — Timer A, Channel 2
(GPIOB5)		Schmitt Input/ Output		**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(SYS_CLK)		Output		**Clock Output** - can be used to monitor the internal SYS_CLK signal (see **Section 6.5.7** CLKO Select Register, SIM_CLKOSR). In the 56F8322, the default state after reset is INDEX0. In the 56F8122, the default state is not one of the functions offered and must be reconfigured.
HOME0	35	Schmitt Input	Input, pull-up enabled	**Home** — Quadrature Decoder 0, HOME input
(TA3)		Schmitt Input/ Output		**TA3** — Timer A, Channel 3
(GPIOB4)		Schmitt Input/ Output		**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(prescaler_ clock)		Output		**Clock Output** - can be used to monitor the internal prescaler_clock signal (see **Section 6.5.7** CLKO Select Register, SIM_CLKOSR). In the 56F8322, the default state after reset is HOME0. In the 56F8122, the default state is not one of the functions offered and must be reconfigured.
SCLK0	19	Schmitt Input/ Output	Tri-Input, pull-up enabled	**SPI 0 Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. A Schmitt trigger input is used for noise immunity.
(GPIOB3)		Schmitt Input/ Output		**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCLK0.

Table 2-2 Signal and Package Information for the 48-Pin LQFP (Continued)

Signal Name	Pin No.	Type	State During Reset	Signal Description
MOSI0	18	Schmitt Input/ Output	In reset, output is disabled, pull-up is enabled	**SPI 0 Master Out/Slave In** — This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge the slave device uses to latch the data.
(GPIOB2)		Schmitt Input/ Output		**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is MOSI0.
MISO0	16	Schmitt Input/ Output	Input, pull-up enabled	**SPI 0 Master In/Slave Out** — This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. The slave device places data on the MISO line a half-cycle before the clock edge the master device uses to latch the data.
(RXD1)		Schmitt Input		**Receive Data** — SCI1 receive data input
(GPIOB1)		Schmitt Input/ Output		**Port B GPIO** - This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is MISO0.
$\overline{\text{SS0}}$	15	Schmitt Input	Input, pull-up enabled	**SPI 0 Slave Select** — $\overline{\text{SS0}}$ is used in slave mode to indicate to the SPI module that the current transfer is to be received.
(TXD1)		Schmitt Output		**Transmit Data** — SCI1 transmit data output
(GPIOB0)		Schmitt Input/ Output		**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is $\overline{\text{SS0}}$.
PWMA0	3	Schmitt Output	In reset, output is disabled, pull-up is enabled	**PWMA0** — This is one of six PWMA output pins.
(GPIOA0)		Schmitt Input/ Output		**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8322, the default state after reset is PWMA0. In the 56F8122, the default state is not one of the functions offered and must be reconfigured.

Table 2-2 Signal and Package Information for the 48-Pin LQFP (Continued)

Signal Name	Pin No.	Type	State During Reset	Signal Description
PWMA1 **(GPIOA1)**	4	Schmitt Output Schmitt Input/ Output	In reset, output is disabled, pull-up is enabled	**PWMA1** — This is one of six PWMA output pins. **Port A GPIO** - This GPIO pin can be individually programmed as an input or output pin. In the 56F8322, the default state after reset is PWMA1. In the 56F8122, the default state is not one of the functions offered and must be reconfigured.
PWMA2 **($\overline{\text{SS1}}$)** **(GPIOA2)**	6	Output Schmitt Input Schmitt Input/ Output	In reset, output is disabled, pull-up is enabled	**PWMA2** — This is one of six PWMA output pins. **SPI 1 Slave Select** — $\overline{\text{SS1}}$ is used in slave mode to indicate to the SPI module that the current transfer is to be received. **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8322, the default state after reset is PWMA2. In the 56F8122, the default state is not one of the functions offered and must be reconfigured.
PWMA3 **(MISO1)** **(GPIOA3)**	7	Output Schmitt Input/ Output Schmitt Input/ Output	In reset, output is disabled, pull-up is enabled	**PWMA3** — This is one of six PWMA output pins. **SPI 1 Master In/Slave Out** — This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. The slave device places data on the MISO line a half-cycle before the clock edge the master device uses to latch the data. **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8322, the default state after reset is PWMA3. In the 56F8122, the default state is not one of the functions offered and must be reconfigured.

Table 2-2 Signal and Package Information for the 48-Pin LQFP (Continued)

Signal Name	Pin No.	Type	State During Reset	Signal Description
PWMA4	8	Output	In reset, output is disabled, pull-up is enabled	**PWMA4** — This is one of six PWMA output pins.
(MOSI1)		Schmitt Input/ Output		**SPI 1 Master Out/Slave In** — This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge the slave device uses to latch the data.
(GPIOA4)		Schmitt Input/ Output		**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8322, the default state after reset is PWMA4. In the 56F8122, the default state is not one of the functions offered and must be reconfigured.
PWMA5	9	Output	In reset, output is disabled, pull-up is enabled	**PWMA5** — This is one of six PWMA output pins.
(SCLK1)		Schmitt Input/ Output		**SPI 1 Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. A Schmitt trigger input is used for noise immunity.
(GPIOA5)		Schmitt Input/ Output		**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8322, the default state after reset is PWMA5. In the 56F8122, the default state is not one of the functions offered and must be reconfigured.
FAULTA0	12	Schmitt Input	Input	**FAULTA0** — This fault input pin is used for disabling selected PWMA outputs in cases where fault conditions originate off-chip.
(GPIOA6)		Schmitt Input/ Output		**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8322, the default state after reset is FAULTA0. In the 56F8122, the default state is not one of the functions offered and must be reconfigured.
ANA0	20	Input	Analog Input	**ANA0 - 2** — Analog inputs to ADCA, Channel 0
ANA1	21			
ANA2	22			
ANA4	23	Input	Analog Input	**ANA4 - 6** — Analog inputs to ADCA, Channel 1
ANA5	24			
ANA6	25			

Table 2-2 Signal and Package Information for the 48-Pin LQFP (Continued)

Signal Name	Pin No.	Type	State During Reset	Signal Description
V_{REFP}	28	Input/ Output	Analog Input/ Output	**V_{REFP}, V_{REFMID} & V_{REFN}** — Internal pins for voltage reference which are brought off-chip so that they can be bypassed. Connect to a 0.1μF ceramic low ESR capacitor.
V_{REFMID}	27			
V_{REFN}	26			
CAN_RX	46	Schmitt Input	Input, pull-up enabled	**FlexCAN Receive Data** — This is the CAN input. This pin has an internal pull-up resistor.
(GPIOC2)		Schmitt Input/ Output		**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8322, the default state after reset is CAN_RX. In the 56F8122, the default state is not one of the functions offered and must be reconfigured.
CAN_TX	47	Open Drain Output	Open Drain Output	**FlexCAN Transmit Data** — CAN output with internal pull-up enable at reset.* * **Note**: If a pin is configured as open drain output mode, internal pull-up will automatically be disabled when it outputs low. Internal pull-up will be enabled unless it has been manually disabled by clearing the corresponding bit in the PUREN register of the GPIO module, when it outputs high. If a pin is configured as push-pull output mode, internal pull-up will automatically be disabled, whether it outputs low or high.
(GPIOC3)		Schmitt Input/ Output		**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8322, the default state after reset is CAN_TX. In the 56F8122, the default state is not one of the functions offered and must be reconfigured.
TC0	1	Schmitt Input/ Output	Input, pull-up enabled	**TC0** — Timer C, Channel 0
(TXD0)		Schmitt Input		**Transmit Data** — SCI0 transmit data output
(GPIOC6)		Schmitt Input/ Output		**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TC0.

Table 2-2 Signal and Package Information for the 48-Pin LQFP (Continued)

Signal Name	Pin No.	Type	State During Reset	Signal Description
TC1 **(RXD0)** **(GPIOC5)**	48	Schmitt Input/ Output Output Schmitt Input/ Output	Input, pull-up enabled	**TC1** — Timer C, Channel 1 **Receive Data** — SCI0 receive data input **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TC1.
$\overline{\text{IRQA}}$ **(V_{PP})**	11	Schmitt Input	Input, pull-up enabled	**External Interrupt Request A** — The $\overline{\text{IRQA}}$ input is an asynchronous external interrupt request during Stop and Wait mode operation. During other operating modes, it is a synchronized external interrupt request which indicates an external device is requesting service. It can be programmed to be level-sensitive or negative-edge-triggered. **V_{PP}** — This pin is used for Flash debugging purposes.
$\overline{\text{RESET}}$	2	Schmitt Input	Input, pull-up enabled	**Reset** — This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the hybrid controller is initialized and placed in the reset state. A Schmitt trigger input is used for noise immunity. The internal reset signal will be deasserted synchronous with the internal clocks after a fixed number of internal clocks. To ensure complete hardware reset, $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$ should be asserted together. The only exception occurs in a debugging environment when a hardware DSP reset is required and it is necessary not to reset the JTAG/EOnCE module. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$.

Part 3 On-Chip Clock Synthesis (OCCS)

3.1 Introduction

Refer to the OCCS chapter of the **56F8300 Peripheral User Manual** for a full description of the OCCS. The material contained here identifies the specific features of the OCCS design.

3.2 External Clock Operation

The system clock can be derived from an external crystal, ceramic resonator or an external system clock signal. To generate a reference frequency using the internal oscillator, a reference crystal or ceramic resonator must be connected between the EXTAL and XTAL pins.

3.2.1 Crystal Oscillator

The internal oscillator is designed to interface with a parallel-resonant crystal resonator in the frequency range specified for the external crystal in **Table 10-15**. A recommended crystal oscillator circuit is shown in **Figure 3-1**. Follow the crystal supplier's recommendations when selecting a crystal, since crystal parameters determine the component values required to provide maximum stability and reliable start-up. The crystal and associated components should be mounted as near as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time.

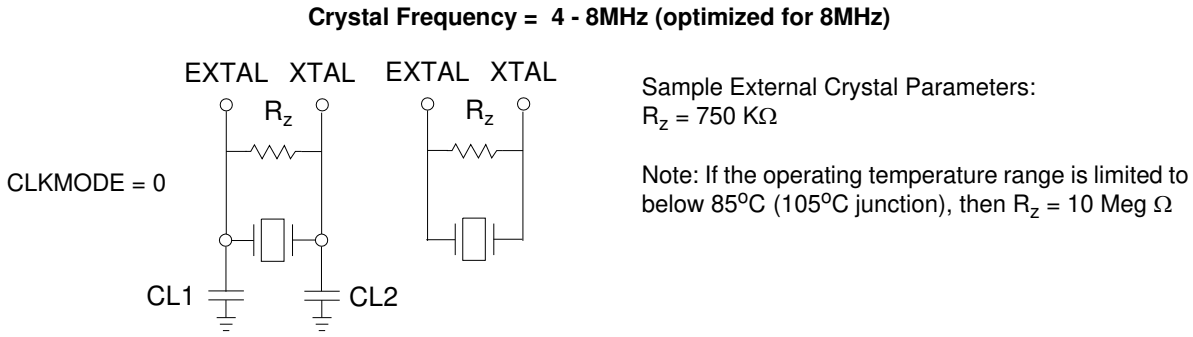


Figure 3-1 Connecting to a Crystal Oscillator

Note: The OCCS_COHL bit should be set to 1 when a crystal oscillator is used. The reset condition on the OCCS_COHL bit is 0. Please see the COHL bit in the Oscillator Control (OSCTL) register, discussed in the **56F8300 Peripheral User Manual**.

3.2.2 Ceramic Resonator (Default)

It is also possible to drive the internal oscillator with a ceramic resonator, assuming the overall system design can tolerate the reduced signal integrity. A typical ceramic resonator circuit is shown in **Figure 3-2**. Refer to the supplier's recommendations when selecting a ceramic resonator and associated components. The resonator and components should be mounted as near as possible to the EXTAL and XTAL pins.

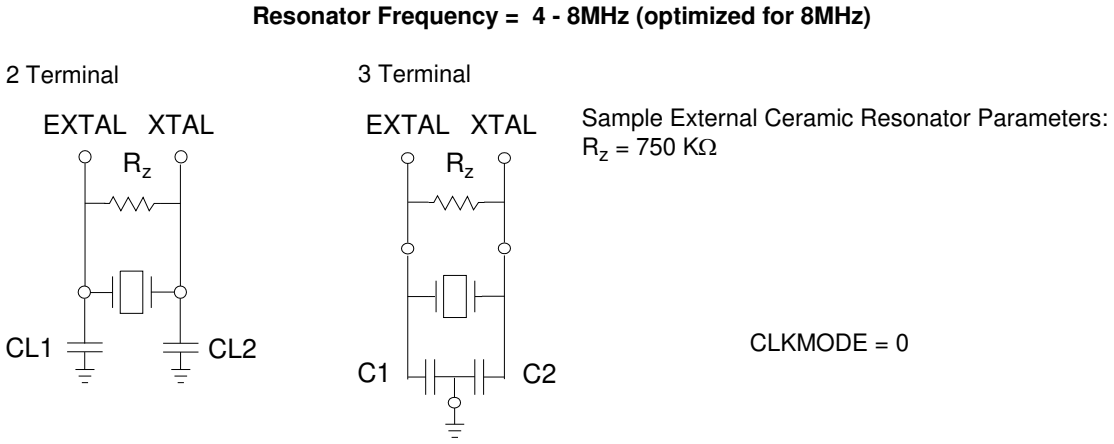


Figure 3-2 Connecting a Ceramic Resonator

Note: The OCCS_COHL bit must be set to 0 when a crystal resonator is used. The reset condition on the OCCS_COHL bit is 0. Please see the COHL bit in the Oscillator Control (OSCTL) register, discussed in the **56F8300 Peripheral User Manual**.

3.2.3 External Clock Source

The recommended method of connecting an external clock is illustrated in **Figure 3-3**. The external clock source is connected to XTAL and the EXTAL pin is grounded.

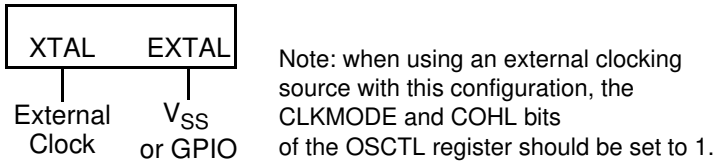


Figure 3-3 Connecting an External Clock Register

3.3 Use of On-Chip Relaxation Oscillator

An internal relaxtion oscillator can supply the reference frequency when an external frequency source of crystal is not used. During a boot or reset sequence, the relaxation oscillator is enabled by default, and the PRECS bit in the PLLCR word is set to 0. If an external oscillator is connected, the relaxation oscillator can be deselected instead by setting the PRECS bit in the PLLCR to 1. If a changeover between internal and external oscillators is required at start up, internal device circuits compensate for any asynchronous transitions between the two clock signals so that no glitches occur in the resulting master clock to the chip. When changing clocks, the user must ensure that the clock source is not switched until the desired clock is enabled and stable.

To compensate for variances in the device manufacturing process, the accuracy of the relaxation oscillator can be incrementally adjusted to within $\pm$ 0.1% of 8MHz by trimming an internal capacitor. Bits 0-9 of the OSCTL (oscillator control) register allow the user to set in an additional offset (trim) to this preset value to increase or decrease capacitance. Upon power-up, the default value of this trim is 512 units. Each unit added or deleted changes the output frequency by about 0.1%, allowing incremental adjustment until the desired frequency accuracy is achieved.

The internal oscillator is calibrated at the factory to 8MHz and the TRIM value is stored in the Flash information block and loaded to the FMOPT1 register at reset. When using the relaxation oscillator, the boot code should read the FMOPT1 register and set this value as OSCTL TRIM. For further information, see the **56F8300 Peripheral User Manual**.

3.4 Internal Clock Operation

At reset, both oscillators will be powered up; however, the relaxation oscillator will be the default clock reference for the PLL. Software should power down the block not being used and program the PLL for the correct frequency.

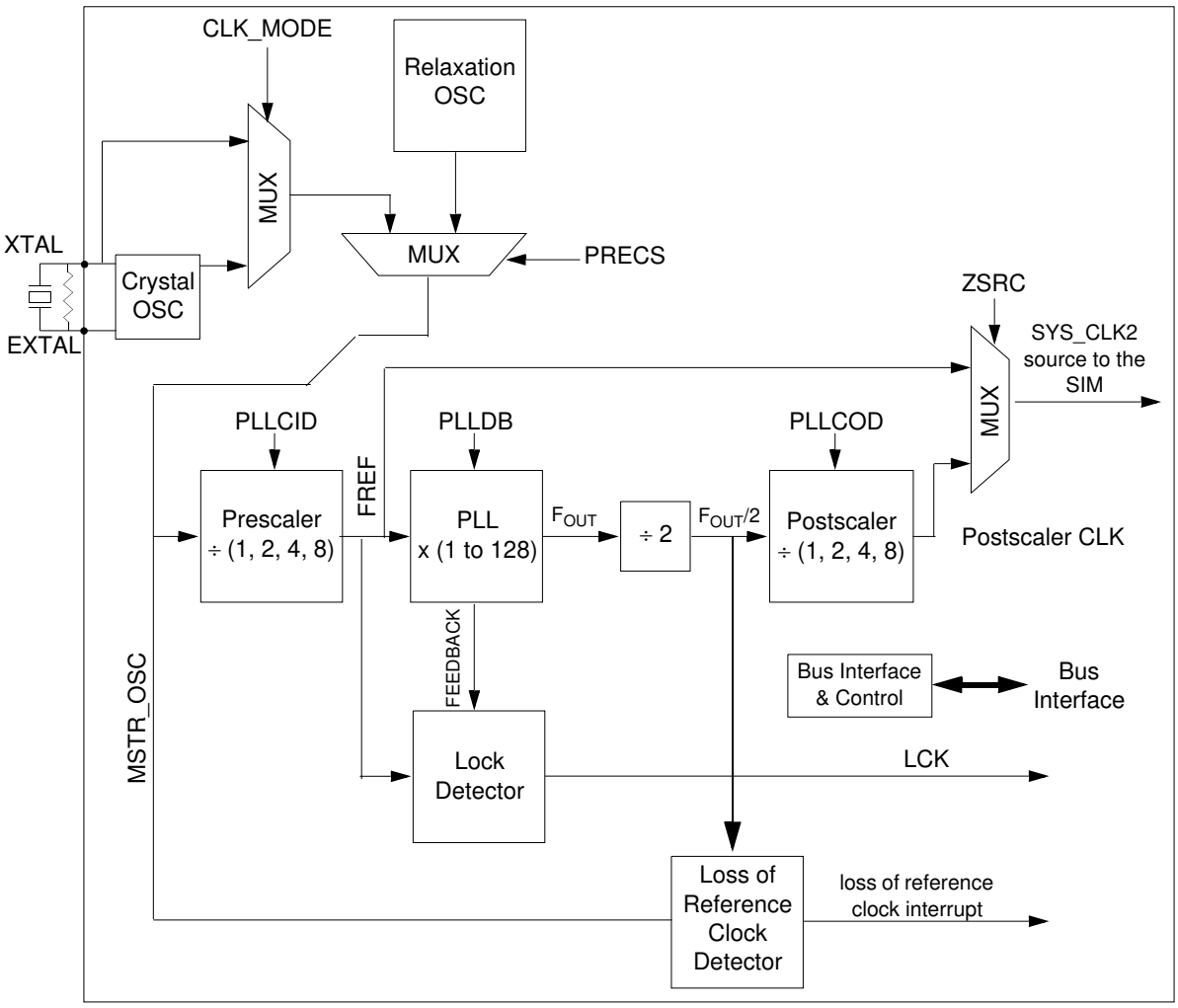


Figure 3-4 Internal Clock Operation

3.5 Registers

When referring to the register definitions for the OCCS in the **56F8300 Peripheral User Manual**, use the register definitions **with** the internal Relaxation Oscillator, since the 56F8322 and 56F8122 contain this oscillator.

Part 4 Memory Map

4.1 Introduction

The 56F8322 and 56F8122 devices are 16-bit motor-control chips based on the 56800E core. These parts use a Harvard-style architecture with two independent memory spaces for Data and Program. On-chip RAM and Flash memories are used in both spaces.

This section provides memory maps for:

- Program Address Space, including the Interrupt Vector Table
- Data Address Space, including the EOnCE Memory and Peripheral Memory Maps

On-chip memory sizes for the device are summarized in **Table 4-1.** Flash memories' restrictions are identified in the "Use Restrictions" column of **Table 4-1.**

Note: *Data Flash and Program RAM are NOT available on the 56F8122 device.*

Table 4-1 Chip Memory Configurations

On-Chip Memory	56F8322	56F8122	Use Restrictions
Program Flash	32KB	32KB	Erase / Program via Flash interface unit and word writes to CDBW
Data Flash	8KB	—	Erase / Program via Flash interface unit and word writes to CDBW. Data Flash can be read via either CDBR or XDB2, but not by both simultaneously.
Program RAM	4KB	—	None
Data RAM	8KB	8KB	None
Program Boot Flash	8KB	8KB	Erase / Program via Flash Interface unit and word writes to CDBW

4.2 Program Map

The Program Memory map is located in **Table 4-2**. The operating mode control bits (MA and MB) in the Operating Mode Register (OMR) usually control the Program Memory map. Because the 56F8322 and 56F8122 do not include EMI, the OMR MA bit, which is used to decide internal or external BOOT, will have no effect on the Program Memory Map. OMR MB reflects the security status of the Program Flash. After reset, changing the OMR MB bit will have no effect on the Program Flash.

Note: *Program RAM is NOT available on the 56F8122 device.*

Table 4-2 Program Memory Map at Reset

Begin/End Address	Memory Allocation
P: $1F FFFF P: $03 0000	RESERVED
P: $02 FFFF P: $02 F800	*On-Chip Program RAM* 4KB
P: $02 F7FF P: $02 1000	RESERVED
P: $02 0FFF P: $02 0000	Boot Flash 8KB Cop Reset Address = $02 0002 Boot Location = $02 0000
P: $01 FFFF P: $00 4000	RESERVED
P: $00 3FFF P: $00 0000	Internal Program Flash 32KB

4.3 Interrupt Vector Table

Table 4-3 provides the device's reset and interrupt priority structure, including on-chip peripherals. The table is organized with higher-priority vectors at the top and lower-priority interrupts lower in the table. As indicated, the priority of an interrupt can be assigned to different levels, allowing some control over interrupt priorities. All level 3 interrupts will be serviced before level 2, and so on. For a selected priority level, the lowest vector number has the highest priority.

The location of the vector table is determined by the Vector Base Address (VBA). Please see Section 5.6.11 for the reset value of the VBA.

In some configurations, the reset address and COP reset address will correspond to vector 0 and 1 of the interrupt vector table. In these instances, the first two locations in the vector table must contain branch or JMP instructions. All other entries must contain JSR instructions.

Note: *PWM, CAN and Quadrature Decoder are NOT available on the 56F8122 device.*

Table 4-3 Interrupt Vector Table Contents[1]

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
				Reserved for Reset Overlay[2]
				Reserved for COP Reset Overlay[2]
core	2	3	P:$04	Illegal Instruction
core	3	3	P:$06	SW Interrupt 3
core	4	3	P:$08	HW Stack Overflow
core	5	3	P:$0A	Misaligned Long Word Access

Table 4-3 Interrupt Vector Table Contents[1] (Continued)

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
core	6	1-3	P:$0C	OnCE Step Counter
core	7	1-3	P:$0E	OnCE Breakpoint Unit 0
				Reserved
core	9	1-3	P:$12	OnCE Trace Buffer
core	10	1-3	P:$14	OnCE Transmit Register Empty
core	11	1-3	P:$16	OnCE Receive Register Full
				Reserved
core	14	2	P:$1C	SW Interrupt 2
core	15	1	P:$1E	SW Interrupt 1
core	16	0	P:$20	SW Interrupt 0
core	17	0-2	P:$22	IRQA
				Reserved
LVI	20	0-2	P:$28	Low-Voltage Detector (power sense)
PLL	21	0-2	P:$2A	PLL
FM	22	0-2	P:$2C	FM Access Error Interrupt
FM	23	0-2	P:$2E	FM Command Complete
FM	24	0-2	P:$30	FM Command, data and address Buffers Empty
				Reserved
FLEXCAN	26	0-2	P:$34	FLEXCAN Bus Off
FLEXCAN	27	0-2	P:$36	FLEXCAN Error
FLEXCAN	28	0-2	P:$38	FLEXCAN Wake Up
FLEXCAN	29	0-2	P:$3A	FLEXCAN Message Buffer Interrupt
				Reserved
GPIOC	33	0-2	P:$42	GPIO C
GPIOB	34	0-2	P:$44	GPIO B
GPIOA	35	0-2	P:$46	GPIO A
				Reserved
SPI1	38	0-2	P:$4C	SPI 1 Receiver Full
SPI1	39	0-2	P:$4E	SPI 1 Transmitter Empty
SPI0	40	0-2	P:$50	SPI 0 Receiver Full
SPI0	41	0-2	P:$52	SPI 0 Transmitter Empty
SCI1	42	0-2	P:$54	SCI 1 Transmitter Empty
SCI1	43	0-2	P:$56	SCI 1Transmitter Idle
				Reserved
SCI1	45	0-2	P:$5A	SCI 1 Receiver Error
SCI1	46	0-2	P:$5C	SCI 1 Receiver Full
				Reserved
DEC0	49	0-2	P:$62	Quadrature Decoder #0 Home Switch or Watchdog
DEC0	50	0-2	P:$64	Quadrature Decoder #0 INDEX Pulse

Table 4-3 Interrupt Vector Table Contents[1] (Continued)

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
				Reserved
TMRC	56	0-2	P:$70	Timer C Channel 0
TMRC	57	0-2	P:$72	Timer C Channel 1
TMRC	58	0-2	P:$74	Timer C Channel 2
TMRC	59	0-2	P:$76	Timer C Channel 3
				Reserved
TMRA	64	0-2	P:$80	Timer A Channel 0
TMRA	65	0-2	P:$82	Timer A Channel 1
TMRA	66	0-2	P:$84	Timer A Channel 2
TMRA	67	0-2	P:$86	Timer A Channel 3
SCI0	68	0-2	P:$88	SCI 0 Transmitter Empty
SCI0	69	0-2	P:$8A	SCI 0 Transmitter Idle
				Reserved
SCI0	71	0-2	P:$8E	SCI 0 Receiver Error
SCI0	72	0-2	P:$90	SCI 0 Receiver Full
				Reserved
ADCA	74	0-2	P:$94	ADC A Conversion Complete / End of Scan
				Reserved
ADCA	76	0-2	P:$98	ADC A Zero Crossing or Limit Error
				Reserved
PWMA	78	0-2	P:$9C	Reload PWM A
				Reserved
PWMA	80	0-2	P:$A0	PWM A Fault
core	81	- 1	P:$A2	SW Interrupt LP
	82	0 - 2	P:$A4	

1. Two words are allocated for each entry in the vector table. This does not allow the full address range to be referenced from the vector table, providing only 19 bits of address.
2. If the VBA is set to $0200, the first two locations of the vector table will overlay the chip reset addresses.

4.4 Data Map

Note: *Data Flash is NOT available on the 56F8122 device.*

Table 4-4 Data Memory Map[1]

Begin/End Address	Memory Allocation
X:$FF FFFF X:$FF FF00	EOnCE 256 locations allocated
X:$FF FEFF X:$01 0000	RESERVED
X:$00 FFFF X:$00 F000	On-Chip Peripherals 4096 locations allocated
X:$00 EFFF X:$00 2000	RESERVED
X:$00 1FFF X:$00 1000	*On-Chip Data Flash* 8KB
X:$00 0FFF X:$00 0000	On-Chip Data RAM 8KB[2]

1. All addresses are 16-bit Word addresses.
2. The Data RAM is organized as a 2K x 32-bit memory to allow single-cycle, long-word operations

4.5 Flash Memory Map

Figure 4-1 illustrates the Flash Memory (FM) map on the system bus.

Flash Memory is divided into three functional blocks. The Program and boot memories reside on the Program Memory buses. They are controlled by one set of banked registers. Data Memory Flash resides on the Data Memory buses and is controlled separately by its own set of banked registers.

The top nine words of the Program Memory Flash are treated as special memory locations. The content of these words is used to control the operation of the Flash Controller. Because these words are part of the Flash Memory content, their state is maintained during power-down and reset. During chip initialization, the content of these memory locations is loaded into Flash Memory control registers, detailed in the Flash Memory chapter of the **56F8300 Peripheral User Manual**. These configure parameters are located between $00_3FF7 and $00_3FFF.

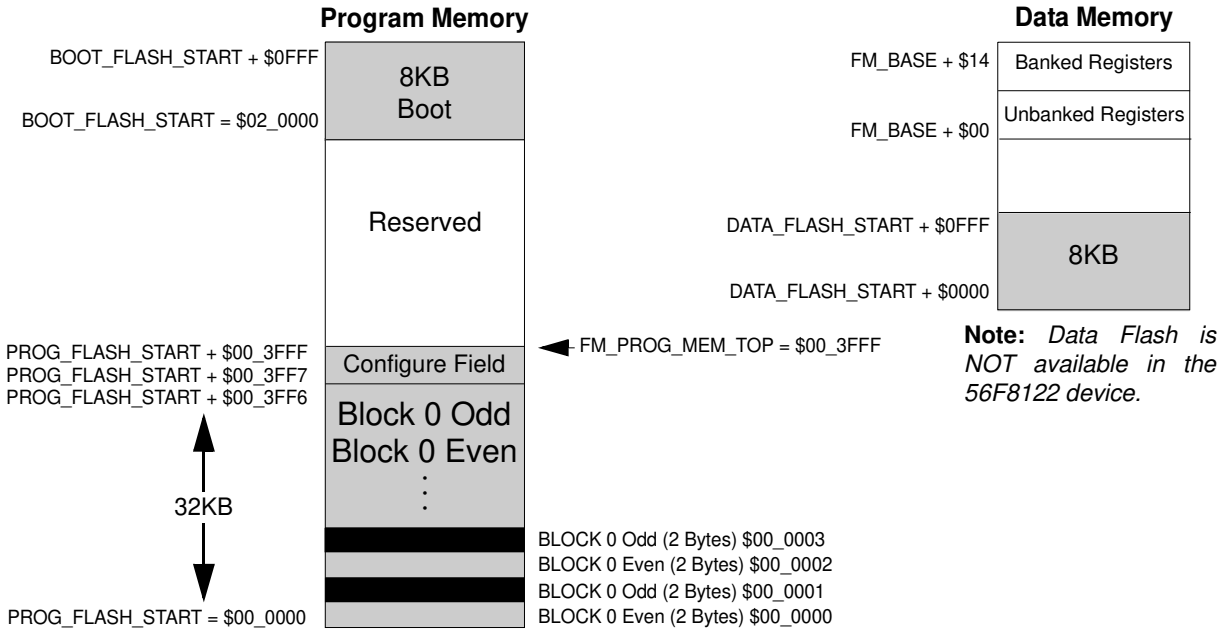


Figure 4-1 Flash Array Memory Maps

Table 4-5 shows the page and sector sizes used within each Flash memory block on the chip.

Note: *Data Flash is NOT available on the 56F8122 device.*

Table 4-5 Flash Memory Partitions

	Flash Size	Sectors	Sector Size	Page Size
Program Flash	32KB	16	1K x 16 bits	512 x 16 bits
Data Flash	8KB	16	256 x 16 bits	256 x 16 bits
Boot Flash	8KB	4	1K x 16 bits	256 x 16 bits

Please see the **56F8300 Peripheral User Manual** for additional Flash information.

4.6 EOnCE Memory Map

Table 4-6 EOnCE Memory Map

Address	Register Acronym	Register Name
		Reserved
X:$FF FF8A	OESCR	External Signal Control Register
		Reserved
X:$FF FF8E	OBCNTR	Breakpoint Unit [0] Counter
		Reserved
X:$FF FF90	OBMSK (32 bits)	Breakpoint 1 Unit [0] Mask Register
X:$FF FF91	—	Breakpoint 1 Unit [0] Mask Register
X:$FF FF92	OBAR2 (32 bits)	Breakpoint 2 Unit [0] Address Register
X:$FF FF93	—	Breakpoint 2 Unit [0] Address Register
X:$FF FF94	OBAR1 (24 bits)	Breakpoint 1 Unit [0] Address Register
X:$FF FF95	—	Breakpoint 1 Unit [0] Address Register
X:$FF FF96	OBCR (24 bits)	Breakpoint Unit [0] Control Register
X:$FF FF97	—	Breakpoint Unit [0] Control Register
X:$FF FF98	OTB (21-24 bits/stage)	Trace Buffer Register Stages
X:$FF FF99	—	Trace Buffer Register Stages
X:$FF FF9A	OTBPR (8 bits)	Trace Buffer Pointer Register
X:$FF FF9B	OTBCR	Trace Buffer Control Register
X:$FF FF9C	OBASE (8 bits)	Peripheral Base Address Register
X:$FF FF9D	OSR	Status Register
X:$FF FF9E	OSCNTR (24 bits)	Instruction Step Counter
X:$FF FF9F	—	Instruction Step Counter
X:$FF FFA0	OCR (bits)	Control Register
		Reserved
X:$FF FFFC	OCLSR (8 bits)	Core Lock / Unlock Status Register
X:$FF FFFD	OTXRXSR (8 bits)	Transmit and Receive Status and Control Register
X:$FF FFFE	OTX / ORX (32 bits)	Transmit Register / Receive Register
X:$FF FFFF	OTX1 / ORX1	Transmit Register Upper Word Receive Register Upper Word

4.7 Peripheral Memory Mapped Registers

On-chip peripheral registers are part of the data memory map on the 56800E series. These locations may be accessed with the same addressing modes used for ordinary Data memory, except all peripheral registers should be read/written using word accesses only.

Table 4-7 summarizes base addresses for the set of peripherals on the 56F8322 and 56F8122 devices. Peripherals are listed in order of the base address.

The following tables list all of the peripheral registers required to control or access the peripherals.

Note: *Features in italics are NOT available on the 56F8122 device.*

Table 4-7 Data Memory Peripheral Base Address Map Summary

Peripheral	Prefix	Base Address	Table Number
Timer A	TMRA	X:$00 F040	4-8
Timer C	TMRC	X:$00 F0C0	4-9
PWM A	PWMA	X:$00 F140	4-10
Quadrature Decoder 0	DEC0	X:$00 F180	4-11
ITCN	ITCN	X:$00 F1A0	4-12
ADC A	ADCA	X:$00 F200	4-13
Temperature Sensor	TSENSOR	X:$00 F270	4-14
SCI #0	SCI0	X:$00 F280	4-15
SCI #1	SCI1	X:$00 F290	4-16
SPI #0	SPI0	X:$00 F2A0	4-17
SPI #1	SPI1	X:$00 F2B0	4-18
COP	COP	X:$00 F2C0	4-19
PLL, OSC	CLKGEN	X:$00 F2D0	4-20
GPIO Port A	GPIOA	X:$00 F2E0	4-21
GPIO Port B	GPIOB	X:$00 F300	4-22
GPIO Port C	GPIOC	X:$00 F310	4-23
SIM	SIM	X:$00 F350	4-24
Power Supervisor	LVI	X:$00 F360	4-25
FM	FM	X:$00 F400	4-26
FlexCAN	FC	X:$00 F800	4-27

Table 4-8 Quad Timer A Registers Address Map (TMRA_BASE = $00 F040)

Register Acronym	Address Offset	Register Description
TMRA0_CMP1	$0	Compare Register 1
TMRA0_CMP2	$1	Compare Register 2
TMRA0_CAP	$2	Capture Register
TMRA0_LOAD	$3	Load Register
TMRA0_HOLD	$4	Hold Register
TMRA0_CNTR	$5	Counter Register
TMRA0_CTRL	$6	Control Register
TMRA0_SCR	$7	Status and Control Register
TMRA0_CMPLD1	$8	Comparator Load Register 1

Table 4-8 Quad Timer A Registers Address Map (Continued) (TMRA_BASE = $00 F040)

Register Acronym	Address Offset	Register Description
TMRA0_CMPLD2	$9	Comparator Load Register 2
TMRA0_COMSCR	$A	Comparator Status and Control Register
		Reserved
TMRA1_CMP1	$10	Compare Register 1
TMRA1_CMP2	$11	Compare Register 2
TMRA1_CAP	$12	Capture Register
TMRA1_LOAD	$13	Load Register
TMRA1_HOLD	$14	Hold Register
TMRA1_CNTR	$15	Counter Register
TMRA1_CTRL	$16	Control Register
TMRA1_SCR	$17	Status and Control Register
TMRA1_CMPLD1	$18	Comparator Load Register 1
TMRA1_CMPLD2	$19	Comparator Load Register 2
TMRA1_COMSCR	$1A	Comparator Status and Control Register
		Reserved
TMRA2_CMP1	$20	Compare Register 1
TMRA2_CMP2	$21	Compare Register 2
TMRA2_CAP	$22	Capture Register
TMRA2_LOAD	$23	Load Register
TMRA2_HOLD	$24	Hold Register
TMRA2_CNTR	$25	Counter Register
TMRA2_CTRL	$26	Control Register
TMRA2_SCR	$27	Status and Control Register
TMRA2_CMPLD1	$28	Comparator Load Register 1
TMRA2_CMPLD2	$29	Comparator Load Register 2
TMRA2_COMSCR	$2A	Comparator Status and Control Register
		Reserved
TMRA3_CMP1	$30	Compare Register 1
TMRA3_CMP2	$31	Compare Register 2
TMRA3_CAP	$32	Capture Register
TMRA3_LOAD	$33	Load Register
TMRA3_HOLD	$34	Hold Register
TMRA3_CNTR	$35	Counter Register
TMRA3_CTRL	$36	Control Register
TMRA3_SCR	$37	Status and Control Register
TMRA3_CMPLD1	$38	Comparator Load Register 1
TMRA3_CMPLD2	$39	Comparator Load Register 2
TMRA3_COMSCR	$3A	Comparator Status and Control Register

Table 4-9 Quad Timer C Registers Address Map (TMRC_BASE = $00 F0C0)

Register Acronym	Address Offset	Register Description
TMRC0_CMP1	$0	Compare Register 1
TMRC0_CMP2	$1	Compare Register 2
TMRC0_CAP	$2	Capture Register
TMRC0_LOAD	$3	Load Register
TMRC0_HOLD	$4	Hold Register
TMRC0_CNTR	$5	Counter Register
TMRC0_CTRL	$6	Control Register
TMRC0_SCR	$7	Status and Control Register
TMRC0_CMPLD1	$8	Comparator Load Register 1
TMRC0_CMPLD2	$9	Comparator Load Register 2
TMRC0_COMSCR	$A	Comparator Status and Control Register
		Reserved
TMRC1_CMP1	$10	Compare Register 1
TMRC1_CMP2	$11	Compare Register 2
TMRC1_CAP	$12	Capture Register
TMRC1_LOAD	$13	Load Register
TMRC1_HOLD	$14	Hold Register
TMRC1_CNTR	$15	Counter Register
TMRC1_CTRL	$16	Control Register
TMRC1_SCR	$17	Status and Control Register
TMRC1_CMPLD1	$18	Comparator Load Register 1
TMRC1_CMPLD2	$19	Comparator Load Register 2
TMRC1_COMSCR	$1A	Comparator Status and Control Register
		Reserved
TMRC2_CMP1	$20	Compare Register 1
TMRC2_CMP2	$21	Compare Register 2
TMRC2_CAP	$22	Capture Register
TMRC2_LOAD	$23	Load Register
TMRC2_HOLD	$24	Hold Register
TMRC2_CNTR	$25	Counter Register
TMRC2_CTRL	$26	Control Register
TMRC2_SCR	$27	Status and Control Register
TMRC2_CMPLD1	$28	Comparator Load Register 1
TMRC2_CMPLD2	$29	Comparator Load Register 2
TMRC2_COMSCR	$2A	Comparator Status and Control Register
		Reserved
TMRC3_CMP1	$30	Compare Register 1

Table 4-9 Quad Timer C Registers Address Map (Continued) (TMRC_BASE = $00 F0C0)

Register Acronym	Address Offset	Register Description
TMRC3_CMP2	$31	Compare Register 2
TMRC3_CAP	$32	Capture Register
TMRC3_LOAD	$33	Load Register
TMRC3_HOLD	$34	Hold Register
TMRC3_CNTR	$35	Counter Register
TMRC3_CTRL	$36	Control Register
TMRC3_SCR	$37	Status and Control Register
TMRC3_CMPLD1	$38	Comparator Load Register 1
TMRC3_CMPLD2	$39	Comparator Load Register 2
TMRC3_COMSCR	$3A	Comparator Status and Control Register

Table 4-10 Pulse Width Modulator A Registers Address Map (PWMA_BASE = $00 F140)

PWM is NOT available in the 56F8122 device

Register Acronym	Address Offset	Register Description
PWMA_PMCTRL	$0	Control Register
PWMA_PMFCTRL	$1	Fault Control Register
PWMA_PMFSA	$2	Fault Status Acknowledge Register
PWMA_PMOUT	$3	Output Control Register
PWMA_PMCNT	$4	Counter Register
PWMA_PWMCM	$5	Counter Modulo Register
PWMA_PWMVAL0	$6	Value Register 0
PWMA_PWMVAL1	$7	Value Register 1
PWMA_PWMVAL2	$8	Value Register 2
PWMA_PWMVAL3	$9	Value Register 3
PWMA_PWMVAL4	$A	Value Register 4
PWMA_PWMVAL5	$B	Value Register 5
PWMA_PMDEADTM	$C	Dead Time Register
PWMA_PMDISMAP1	$D	Disable Mapping Register 1
PWMA_PMDISMAP2	$E	Disable Mapping Register 2
PWMA_PMCFG	$F	Configure Register
PWMA_PMCCR	$10	Channel Control Register
PWMA_PMPORT	$11	Port Register
PWMA_PMICCR	$12	Internal Correction Control

Table 4-11 Quadrature Decoder 0 Registers Address Map (DEC0_BASE = $00 F180)
Quadrature Decoder is NOT available in the 56F8122 device

Register Acronym	Address Offset	Register Description
DEC0_DECCR	$0	Decoder Control Register
DEC0_FIR	$1	Filter Interval Register
DEC0_WTR	$2	Watchdog Time-out Register
DEC0_POSD	$3	Position Difference Counter Register
DEC0_POSDH	$4	Position Difference Counter Hold Register
DEC0_REV	$5	Revolution Counter Register
DEC0_REVH	$6	Revolution Hold Register
DEC0_UPOS	$7	Upper Position Counter Register
DEC0_LPOS	$8	Lower Position Counter Register
DEC0_UPOSH	$9	Upper Position Hold Register
DEC0_LPOSH	$A	Lower Position Hold Register
DEC0_UIR	$B	Upper Initialization Register
DEC0_LIR	$C	Lower Initialization Register
DEC0_IMR	$D	Input Monitor Register

Table 4-12 Interrupt Control Registers Address Map (ITCN_BASE = $00 F1A0)

Register Acronym	Address Offset	Register Description
IPR0	$0	Interrupt Priority Register 0
IPR1	$1	Interrupt Priority Register 1
IPR2	$2	Interrupt Priority Register 2
IPR3	$3	Interrupt Priority Register 3
IPR4	$4	Interrupt Priority Register 4
IPR5	$5	Interrupt Priority Register 5
IPR6	$6	Interrupt Priority Register 6
IPR7	$7	Interrupt Priority Register 7
IPR8	$8	Interrupt Priority Register 8
IPR9	$9	Interrupt Priority Register 9
VBA	$A	Vector Base Address Register
FIM0	$B	Fast Interrupt Match Register 0
FIVAL0	$C	Fast Interrupt Vector Address Low 0 Register
FIVAH0	$D	Fast Interrupt Vector Address High 0 Register
FIM1	$E	Fast Interrupt Match Register 1
FIVAL1	$F	Fast Interrupt Vector Address Low 1 Register
FIVAH1	$10	Fast Interrupt Vector Address High 1 Register

Table 4-12 Interrupt Control Registers Address Map (Continued) (ITCN_BASE = $00 F1A0)

Register Acronym	Address Offset	Register Description
IRQP 0	$11	IRQ Pending Register 0
IRQP 1	$12	IRQ Pending Register 1
IRQP 2	$13	IRQ Pending Register 2
IRQP 3	$14	IRQ Pending Register 3
IRQP 4	$15	IRQ Pending Register 4
IRQP 5	$16	IRQ Pending Register 5
		Reserved
ICTL	$1D	Interrupt Control Register

Table 4-13 Analog to Digital Converter Registers Address Map (ADCA_BASE = $00 F200)

Register Acronym	Address Offset	Register Description
ADCA_CR1	$0	Control Register 1
ADCA_CR2	$1	Control Register 2
ADCA_ZCC	$2	Zero Crossing Control Register
ADCA_LST 1	$3	Channel List Register 1
ADCA_LST 2	$4	Channel List Register 2
ADCA_SDIS	$5	Sample Disable Register
ADCA_STAT	$6	Status Register
ADCA_LSTAT	$7	Limit Status Register
ADCA_ZCSTAT	$8	Zero Crossing Status Register
ADCA_RSLT 0	$9	Result Register 0
ADCA_RSLT 1	$A	Result Register 1
ADCA_RSLT 2	$B	Result Register 2
ADCA_RSLT 3	$C	Result Register 3
ADCA_RSLT 4	$D	Result Register 4
ADCA_RSLT 5	$E	Result Register 5
ADCA_RSLT 6	$F	Result Register 6
ADCA_RSLT 7	$10	Result Register 7
ADCA_LLMT 0	$11	Low Limit Register 0
ADCA_LLMT 1	$12	Low Limit Register 1
ADCA_LLMT 2	$13	Low Limit Register 2
ADCA_LLMT 3	$14	Low Limit Register 3
ADCA_LLMT 4	$15	Low Limit Register 4
ADCA_LLMT 5	$16	Low Limit Register 5
ADCA_LLMT 6	$17	Low Limit Register 6
ADCA_LLMT 7	$18	Low Limit Register 7
ADCA_HLMT 0	$19	High Limit Register 0

Table 4-13 Analog to Digital Converter Registers Address Map (Continued) (ADCA_BASE = $00 F200)

Register Acronym	Address Offset	Register Description
ADCA_HLMT 1	$1A	High Limit Register 1
ADCA_HLMT 2	$1B	High Limit Register 2
ADCA_HLMT 3	$1C	High Limit Register 3
ADCA_HLMT 4	$1D	High Limit Register 4
ADCA_HLMT 5	$1E	High Limit Register 5
ADCA_HLMT 6	$1F	High Limit Register 6
ADCA_HLMT 7	$20	High Limit Register 7
ADCA_OFS 0	$21	Offset Register 0
ADCA_OFS 1	$22	Offset Register 1
ADCA_OFS 2	$23	Offset Register 2
ADCA_OFS 3	$24	Offset Register 3
ADCA_OFS 4	$25	Offset Register 4
ADCA_OFS 5	$26	Offset Register 5
ADCA_OFS 6	$27	Offset Register 6
ADCA_OFS 7	$28	Offset Register 7
ADCA_POWER	$29	Power Control Register
ADCA_CAL	$2A	ADC Calibration Register

Table 4-14 Temperature Sensor Register Address Map (TSENSOR_BASE = $00 F270)
Temperature Sensor is NOT available in the 56F8122 device

Register Acronym	Address Offset	Register Description
TSENSOR_CNTL	$0	Control Register

Table 4-15 Serial Communication Interface 0 Registers Address Map (SCI0_BASE = $00 F280)

Register Acronym	Address Offset	Register Description
SCI0_SCIBR	$0	Baud Rate Register
SCI0_SCICR	$1	Control Register
		Reserved
SCI0_SCISR	$3	Status Register
SCI0_SCIDR	$4	Data Register

Table 4-16 Serial Communication Interface 1 Registers Address Map (SCI1_BASE = $00 F290)

Register Acronym	Address Offset	Register Description
SCI1_SCIBR	$0	Baud Rate Register
SCI1_SCICR	$1	Control Register
		Reserved
SCI1_SCISR	$3	Status Register
SCI1_SCIDR	$4	Data Register

Table 4-17 Serial Peripheral Interface 0 Registers Address Map (SPI0_BASE = $00 F2A0)

Register Acronym	Address Offset	Register Description
SPI0_SPSCR	$0	Status and Control Register
SPI0_SPDSR	$1	Data Size Register
SPI0_SPDRR	$2	Data Receive Register
SPI0_SPDTR	$3	Data Transmitter Register

Table 4-18 Serial Peripheral Interface 1 Registers Address Map (SPI1_BASE = $00 F2B0)

Register Acronym	Address Offset	Register Description
SPI1_SPSCR	$0	Status and Control Register
SPI1_SPDSR	$1	Data Size Register
SPI1_SPDRR	$2	Data Receive Register
SPI1_SPDTR	$3	Data Transmitter Register

Table 4-19 Computer Operating Properly Registers Address Map (COP_BASE = $00 F2C0)

Register Acronym	Address Offset	Register Description
COPCTL	$0	Control Register
COPTO	$1	Time-Out Register
COPCTR	$2	Counter Register

Table 4-20 Clock Generation Module Registers Address Map (CLKGEN_BASE = $00 F2D0)

Register Acronym	Address Offset	Register Description
PLLCR	$0	Control Register
PLLDB	$1	Divide-By Register
PLLSR	$2	Status Register
		Reserved
SHUTDOWN	$4	Shutdown Register
OSCTL	$5	Oscillator Control Register

Table 4-21 GPIOA Registers Address Map (GPIOA_BASE = $00 F2E0)

Register Acronym	Address Offset	Register Description	Reset Value
GPIOA_PUR	$0	Pull-up Enable Register	0 x 0FFF
GPIOA_DR	$1	Data Register	0 x 0000
GPIOA_DDR	$2	Data Direction Register	0 x 0000
GPIOA_PER	$3	Peripheral Enable Register	0 x 0FFF
GPIOA_IAR	$4	Interrupt Assert Register	0 x 0000
GPIOA_IENR	$5	Interrupt Enable Register	0 x 0000
GPIOA_IPOLR	$6	Interrupt Polarity Register	0 x 0000
GPIOA_IPR	$7	Interrupt Pending Register	0 x 0000
GPIOA_IESR	$8	Interrupt Edge-Sensitive Register	0 x 0000
GPIOA_PPMODE	$9	Push-Pull Mode Register	0 x 0FFF
GPIOA_RAWDATA	$A	Raw Data Input Register	—

Table 4-22 GPIOB Registers Address Map (GPIOB_BASE = $00 F300)

Register Acronym	Address Offset	Register Description	Reset Value
GPIOB_PUR	$0	Pull-up Enable Register	0 x 00FF
GPIOB_DR	$1	Data Register	0 x 0000
GPIOB_DDR	$2	Data Direction Register	0 x 0000
GPIOB_PER	$3	Peripheral Enable Register	0 x 00FF
GPIOB_IAR	$4	Interrupt Assert Register	0 x 0000
GPIOB_IENR	$5	Interrupt Enable Register	0 x 0000
GPIOB_IPOLR	$6	Interrupt Polarity Register	0 x 0000
GPIOB_IPR	$7	Interrupt Pending Register	0 x 0000
GPIOB_IESR	$8	Interrupt Edge-Sensitive Register	0 x 0000
GPIOB_PPMODE	$9	Push-Pull Mode Register	0 x 00FF
GPIOB_RAWDATA	$A	Raw Data Input Register	—

Table 4-23 GPIOC Registers Address Map (GPIOC_BASE = $00F310)

Register Acronym	Address Offset	Register Description	Reset Value
GPIOC_PUR	$0	Pull-up Enable Register	0 x 007C
GPIOC_DR	$1	Data Register	0 x 0000
GPIOC_DDR	$2	Data Direction Register	0 x 0000
GPIOC_PER	$3	Peripheral Enable Register	0 x 007F
GPIOC_IAR	$4	Interrupt Assert Register	0 x 0000
GPIOC_IENR	$5	Interrupt Enable Register	0 x 0000
GPIOC_IPOLR	$6	Interrupt Polarity Register	0 x 0000
GPIOC_IPR	$7	Interrupt Pending Register	0 x 0000
GPIOC_IESR	$8	Interrupt Edge-Sensitive Register	0 x 0000
GPIOC_PPMODE	$9	Push-Pull Mode Register	0 x 007F
GPIOC_RAWDATA	$A	Raw Data Input Register	—

Table 4-24 System Integration Module Registers Address Map (SIM_BASE = $00 F350)

Register Acronym	Address Offset	Register Description
SIM_CONTROL	$0	Control Register
SIM_RSTSTS	$1	Reset Status Register
SIM_SCR0	$2	Software Control Register 0
SIM_SCR1	$3	Software Control Register 1
SIM_SCR2	$4	Software Control Register 2
SIM_SCR3	$5	Software Control Register 3
SIM_MSH_ID	$6	Most Significant Half JTAG ID
SIM_LSH_ID	$7	Least Significant Half JTAG ID
SIM_PUDR	$8	Pull-up Disable Register
		Reserved
SIM_CLKOSR	$A	Clock Out Select Register
SIM_GPS	$B	GPIO Peripheral Select Register
SIM_PCE	$C	Peripheral Clock Enable Register
SIM_ISALH	$D	I/O Short Address Location High Register
SIM_ISALL	$E	I/O Short Address Location Low Register

Table 4-25 Power Supervisor Registers Address Map (LVI_BASE = $00 F360)

Register Acronym	Address Offset	Register Description
LVI_CONTROL	$0	Control Register
LVI_STATUS	$1	Status Register

Table 4-26 Flash Module Registers Address Map (FM_BASE = $00 F400)

Register Acronym	Address Offset	Register Description
FMCLKD	$0	Clock Divider Register
FMMCR	$1	Module Control Register
		Reserved
FMSECH	$3	Security High Half Register
FMSECL	$4	Security Low Half Register
		Reserved
		Reserved
FMPROT	$10	Protection Register (Banked)
FMPROTB	$11	Protection Boot Register (Banked)
		Reserved
FMUSTAT	$13	User Status Register (Banked)
FMCMD	$14	Command Register (Banked)
		Reserved
		Reserved
FMOPT 0	$1A	16-Bit Information Option Register 0 Hot temperature ADC reading of Temperature Sensor; value set during factory test
FMOPT 1	$1B	16-Bit Information Option Register 1 Trim cap setting of the relaxation oscillator
FMOPT 2	$1C	16-Bit Information Option Register 2 Room temperature ADC reading of Temperature Sensor; value set during factory test

Table 4-27 FlexCAN Registers Address Map (FC_BASE = $00 F800)

FlexCAN is NOT available in the 56F8122 device

Register Acronym	Address Offset	Register Description
FCMCR	$0	Module Configuration Register
		Reserved
FCCTL0	$3	Control Register 0 Register
FCCTL1	$4	Control Register 1 Register
FCTMR	$5	Free-Running Timer Register
FCMAXMB	$6	Maximum Message Buffer Configuration Register
		Reserved
FCRXGMASK_H	$8	Receive Global Mask High Register
FCRXGMASK_L	$9	Receive Global Mask Low Register

Table 4-27 FlexCAN Registers Address Map (Continued)
(FC_BASE = $00 F800)
FlexCAN is NOT available in the 56F8122 device

Register Acronym	Address Offset	Register Description
FCRX14MASK_H	$A	Receive Buffer 14 Mask High Register
FCRX14MASK_L	$B	Receive Buffer 14 Mask Low Register
FCRX15MASK_H	$C	Receive Buffer 15 Mask High Register
FCRX15MASK_L	$D	Receive Buffer 15 Mask Low Register
		Reserved
FCSTATUS	$10	Error and Status Register
FCIMASK1	$11	Interrupt Masks 1 Register
FCIFLAG1	$12	Interrupt Flags 1 Register
FCR/T_ERROR_CNTRS	$13	Receive and Transmit Error Counters Register
		Reserved
		Reserved
		Reserved
FCMB0_CONTROL	$40	Message Buffer 0 Control / Status Register
FCMB0_ID_HIGH	$41	Message Buffer 0 ID High Register
FCMB0_ID_LOW	$42	Message Buffer 0 ID Low Register
FCMB0_DATA	$43	Message Buffer 0 Data Register
FCMB0_DATA	$44	Message Buffer 0 Data Register
FCMB0_DATA	$45	Message Buffer 0 Data Register
FCMB0_DATA	$46	Message Buffer 0 Data Register
		Reserved
FCMSB1_CONTROL	$48	Message Buffer 1 Control / Status Register
FCMSB1_ID_HIGH	$49	Message Buffer 1 ID High Register
FCMSB1_ID_LOW	$4A	Message Buffer 1 ID Low Register
FCMB1_DATA	$4B	Message Buffer 1 Data Register
FCMB1_DATA	$4C	Message Buffer 1 Data Register
FCMB1_DATA	$4D	Message Buffer 1 Data Register
FCMB1_DATA	$4E	Message Buffer 1 Data Register
		Reserved
FCMB2_CONTROL	$50	Message Buffer 2 Control / Status Register
FCMB2_ID_HIGH	$51	Message Buffer 2 ID High Register
FCMB2_ID_LOW	$52	Message Buffer 2 ID Low Register
FCMB2_DATA	$53	Message Buffer 2 Data Register
FCMB2_DATA	$54	Message Buffer 2 Data Register
FCMB2_DATA	$55	Message Buffer 2 Data Register
FCMB2_DATA	$56	Message Buffer 2 Data Register
		Reserved

Table 4-27 FlexCAN Registers Address Map (Continued)
(FC_BASE = $00 F800)
FlexCAN is NOT available in the 56F8122 device

Register Acronym	Address Offset	Register Description
FCMB3_CONTROL	$58	Message Buffer 3 Control / Status Register
FCMB3_ID_HIGH	$59	Message Buffer 3 ID High Register
FCMB3_ID_LOW	$5A	Message Buffer 3 ID Low Register
FCMB3_DATA	$5B	Message Buffer 3 Data Register
FCMB3_DATA	$5C	Message Buffer 3 Data Register
FCMB3_DATA	$5D	Message Buffer 3 Data Register
FCMB3_DATA	$5E	Message Buffer 3 Data Register
		Reserved
FCMB4_CONTROL	$60	Message Buffer 4 Control / Status Register
FCMB4_ID_HIGH	$61	Message Buffer 4 ID High Register
FCMB4_ID_LOW	$62	Message Buffer 4 ID Low Register
FCMB4_DATA	$63	Message Buffer 4 Data Register
FCMB4_DATA	$64	Message Buffer 4 Data Register
FCMB4_DATA	$65	Message Buffer 4 Data Register
FCMB4_DATA	$66	Message Buffer 4 Data Register
		Reserved
FCMB5_CONTROL	$68	Message Buffer 5 Control / Status Register
FCMB5_ID_HIGH	$69	Message Buffer 5 ID High Register
FCMB5_ID_LOW	$6A	Message Buffer 5 ID Low Register
FCMB5_DATA	$6B	Message Buffer 5 Data Register
FCMB5_DATA	$6C	Message Buffer 5 Data Register
FCMB5_DATA	$6D	Message Buffer 5 Data Register
FCMB5_DATA	$6E	Message Buffer 5 Data Register
		Reserved
FCMB6_CONTROL	$70	Message Buffer 6 Control / Status Register
FCMB6_ID_HIGH	$71	Message Buffer 6 ID High Register
FCMB6_ID_LOW	$72	Message Buffer 6 ID Low Register
FCMB6_DATA	$73	Message Buffer 6 Data Register
FCMB6_DATA	$74	Message Buffer 6 Data Register
FCMB6_DATA	$75	Message Buffer 6 Data Register
FCMB6_DATA	$76	Message Buffer 6 Data Register
		Reserved
FCMB7_CONTROL	$78	Message Buffer 7 Control / Status Register
FCMB7_ID_HIGH	$79	Message Buffer 7 ID High Register
FCMB7_ID_LOW	$7A	Message Buffer 7 ID Low Register
FCMB7_DATA	$7B	Message Buffer 7 Data Register

Table 4-27 FlexCAN Registers Address Map (Continued)
(FC_BASE = $00 F800)
FlexCAN is NOT available in the 56F8122 device

Register Acronym	Address Offset	Register Description
FCMB7_DATA	$7C	Message Buffer 7 Data Register
FCMB7_DATA	$7D	Message Buffer 7 Data Register
FCMB7_DATA	$7E	Message Buffer 7 Data Register
		Reserved
FCMB8_CONTROL	$80	Message Buffer 8 Control / Status Register
FCMB8_ID_HIGH	$81	Message Buffer 8 ID High Register
FCMB8_ID_LOW	$82	Message Buffer 8 ID Low Register
FCMB8_DATA	$83	Message Buffer 8 Data Register
FCMB8_DATA	$84	Message Buffer 8 Data Register
FCMB8_DATA	$85	Message Buffer 8 Data Register
FCMB8_DATA	$86	Message Buffer 8 Data Register
		Reserved
FCMB9_CONTROL	$88	Message Buffer 9 Control / Status Register
FCMB9_ID_HIGH	$89	Message Buffer 9 ID High Register
FCMB9_ID_LOW	$8A	Message Buffer 9 ID Low Register
FCMB9_DATA	$8B	Message Buffer 9 Data Register
FCMB9_DATA	$8C	Message Buffer 9 Data Register
FCMB9_DATA	$8D	Message Buffer 9 Data Register
FCMB9_DATA	$8E	Message Buffer 9 Data Register
		Reserved
FCMB10_CONTROL	$90	Message Buffer 10 Control / Status Register
FCMB10_ID_HIGH	$91	Message Buffer 10 ID High Register
FCMB10_ID_LOW	$92	Message Buffer 10 ID Low Register
FCMB10_DATA	$93	Message Buffer 10 Data Register
FCMB10_DATA	$94	Message Buffer 10 Data Register
FCMB10_DATA	$95	Message Buffer 10 Data Register
FCMB10_DATA	$96	Message Buffer 10 Data Register
		Reserved
FCMB11_CONTROL	$98	Message Buffer 11 Control / Status Register
FCMB11_ID_HIGH	$99	Message Buffer 11 ID High Register
FCMB11_ID_LOW	$9A	Message Buffer 11 ID Low Register
FCMB11_DATA	$9B	Message Buffer 11 Data Register
FCMB11_DATA	$9C	Message Buffer 11 Data Register
FCMB11_DATA	$9D	Message Buffer 11 Data Register
FCMB11_DATA	$9E	Message Buffer 11 Data Register
		Reserved

Table 4-27 FlexCAN Registers Address Map (Continued)
(FC_BASE = $00 F800)
FlexCAN is NOT available in the 56F8122 device

Register Acronym	Address Offset	Register Description
FCMB12_CONTROL	$A0	Message Buffer 12 Control / Status Register
FCMB12_ID_HIGH	$A1	Message Buffer 12 ID High Register
FCMB12_ID_LOW	$A2	Message Buffer 12 ID Low Register
FCMB12_DATA	$A3	Message Buffer 12 Data Register
FCMB12_DATA	$A4	Message Buffer 12 Data Register
FCMB12_DATA	$A5	Message Buffer 12 Data Register
FCMB12_DATA	$A6	Message Buffer 12 Data Register
		Reserved
FCMB13_CONTROL	$A8	Message Buffer 13 Control / Status Register
FCMB13_ID_HIGH	$A9	Message Buffer 13 ID High Register
FCMB13_ID_LOW	$AA	Message Buffer 13 ID Low Register
FCMB13_DATA	$AB	Message Buffer 13 Data Register
FCMB13_DATA	$AC	Message Buffer 13 Data Register
FCMB13_DATA	$AD	Message Buffer 13 Data Register
FCMB13_DATA	$AE	Message Buffer 13 Data Register
		Reserved
FCMB14_CONTROL	$B0	Message Buffer 14 Control / Status Register
FCMB14_ID_HIGH	$B1	Message Buffer 14 ID High Register
FCMB14_ID_LOW	$B2	Message Buffer 14 ID Low Register
FCMB14_DATA	$B3	Message Buffer 14 Data Register
FCMB14_DATA	$B4	Message Buffer 14 Data Register
FCMB14_DATA	$B5	Message Buffer 14 Data Register
FCMB14_DATA	$B6	Message Buffer 14 Data Register
		Reserved
FCMB15_CONTROL	$B8	Message Buffer 15 Control / Status Register
FCMB15_ID_HIGH	$B9	Message Buffer 15 ID High Register
FCMB15_ID_LOW	$BA	Message Buffer 15 ID Low Register
FCMB15_DATA	$BB	Message Buffer 15 Data Register
FCMB15_DATA	$BC	Message Buffer 15 Data Register
FCMB15_DATA	$BD	Message Buffer 15 Data Register
FCMB15_DATA	$BE	Message Buffer 15 Data Register
		Reserved

4.8 Factory-Programmed Memory

The Boot Flash memory block is programmed during manufacturing with a default Serial Bootloader program. The Serial Bootloader application can be used to load a user application into the Program and *Data Flash* (*not available on the 56F8122*) memories of the device. The **56F83xx SCI/CAN Bootloader User Manual** provides detailed information on this firmware. An application note, **Production Flash Programming**, details how the Serial Bootloader program can be used to perform production Flash programming of the on-board Flash memories as well as other optional methods.

Like all the Flash memory blocks, the Boot Flash can be erased and programmed by the user. The Serial Bootloader application is programmed as an aid to the end user, but is not required to be used or maintained in the Boot Flash memory.

Part 5 Interrupt Controller (ITCN)

5.1 Introduction

The Interrupt Controller (ITCN) module is used to arbitrate between various interrupt requests (IRQs), to signal to the 56800E core when an interrupt of sufficient priority exists, and to what address to jump in order to service this interrupt.

5.2 Features

The ITCN module design includes these distinctive features:

- Programmable priority levels for each IRQ
- Two programmable Fast Interrupts
- Notification to SIM module to restart clocks out of Wait and Stop modes
- Drives initial address on the address bus after reset

For further information, see **Table 4-3**, Interrupt Vector Table Contents.

5.3 Functional Description

The Interrupt Controller is a slave on the IPBus. It contains registers allowing each of the 82 interrupt sources to be set to one of four priority levels, excluding certain interrupts of fixed priority. Next, all of the interrupt requests of a given level are priority encoded to determine the lowest numerical value of the active interrupt requests for that level. Within a given priority level, 0 is the highest priority, while number 81 is the lowest.

5.3.1 Normal Interrupt Handling

Once the ITCN has determined that an interrupt is to be serviced and which interrupt has the highest priority, an interrupt vector address is generated. Normal interrupt handling concatenates the VBA and the vector number to determine the vector address. In this way, an offset is generated into the vector table for each interrupt.

5.3.2 Interrupt Nesting

Interrupt exceptions may be nested to allow an IRQ of higher priority than the current exception to be serviced. The following tables define the nesting requirements for each priority level.

Table 5-1 Interrupt Mask Bit Definition

SR[9][1]	SR[8][1]	Permitted Exceptions	Masked Exceptions
0	0	Priorities 0, 1, 2, 3	None
0	1	Priorities 1, 2, 3	Priority 0
1	0	Priorities 2, 3	Priorities 0, 1
1	1	Priority 3	Priorities 0, 1, 2

1. Core status register bits indicating current interrupt mask within the core.

Table 5-2. Interrupt Priority Encoding

IPIC_LEVEL[1:0][1]	Current Interrupt Priority Level	Required Nested Exception Priority
00	No Interrupt or SWILP	Priorities 0, 1, 2, 3
01	Priority 0	Priorities 1, 2, 3
10	Priority 1	Priorities 2, 3
11	Priorities 2 or 3	Priority 3

1. See IPIC field definition in Section 5.6.30.2

5.3.3 Fast Interrupt Handling

Fast interrupts are described in the **DSP56800E Reference Manual**. The interrupt controller recognizes fast interrupts before the core does.

A fast interrupt is defined (to the ITCN) by:

1. Setting the priority of the interrupt as level 2, with the appropriate field in the IPR registers
2. Setting the FIMn register to the appropriate vector number
3. Setting the FIVALn and FIVAHn registers with the address of the code for the fast interrupt

When an interrupt occurs, its vector number is compared with the FIM0 and FIM1 register values. If a match occurs, and it is a level 2 interrupt, the ITCN handles it as a fast interrupt. The ITCN takes the vector address from the appropriate FIVALn and FIVAHn registers, instead of generating an address that is an offset from the VBA.

The core then fetches the instruction from the indicated vector adddress and if it is not a JSR, the core starts its fast interrupt handling.

5.4 Block Diagram

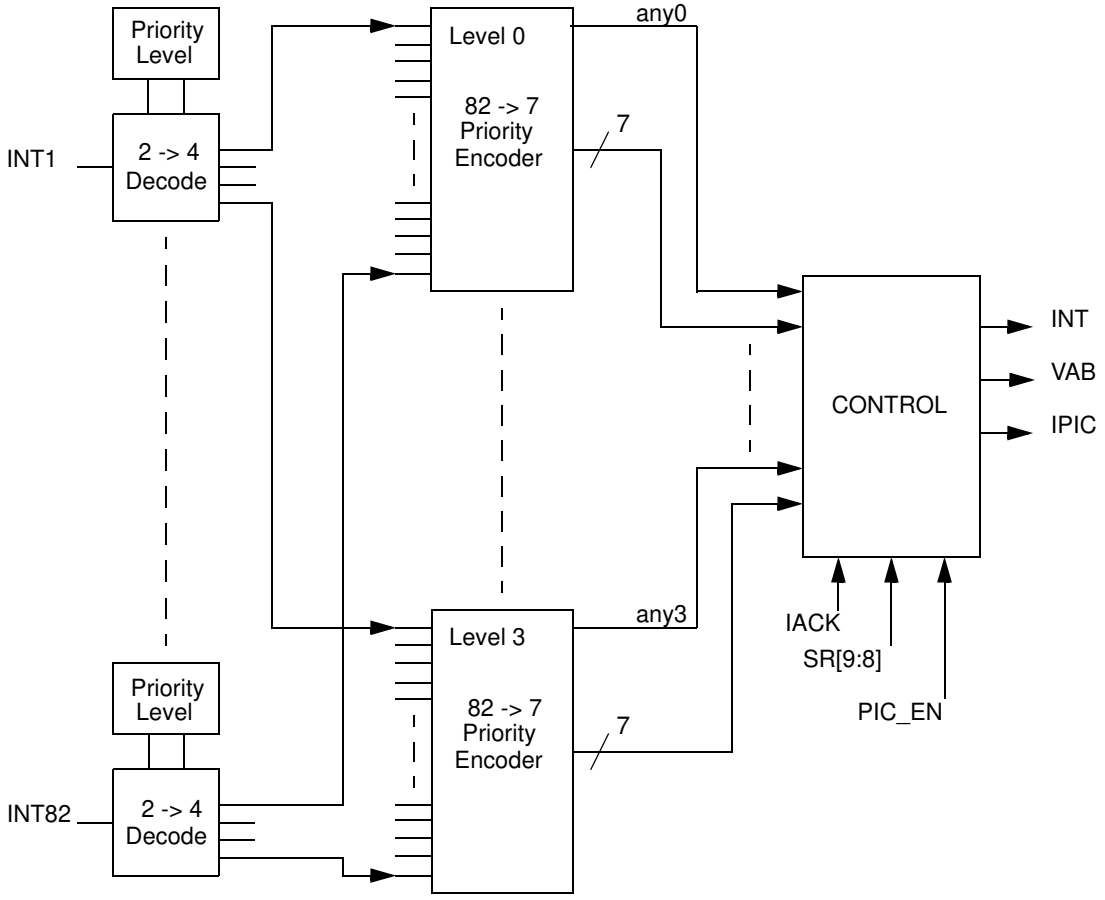


Figure 5-1 Interrupt Controller Block Diagram

5.5 Operating Modes

The ITCN module design contains two major modes of operation:

- **Functional Mode**
  The ITCN is in this mode by default.
- **Wait and Stop Modes**
  During Wait and Stop modes, the system clocks and the 56800E core are turned off. The ITCN will signal a pending IRQ to the System Integration Module (SIM) to restart the clocks and service the IRQ. An IRQ can only wake up the core if the IRQ is enabled prior to entering the Wait or Stop mode. Also, the $\overline{\text{IRQA}}$ signal automatically becomes low-level sensitive in these modes, even if the control register bits are set to make them falling-edge sensitive. This is because there is no clock available to detect the falling edge.

  A peripheral which requires a clock to generate interrupts will not be able to generate interrupts during Stop mode. The FlexCAN module can wake the device from Stop mode, and a reset will do just that, or $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ can wake it up.

5.6 Register Descriptions

A register address is the sum of a base address and an address offset. The base address is defined at the system level and the address offset is defined at the module level. The ITCN peripheral has 24 registers.

Table 5-3 ITCN Register Summary (ITCN_BASE = $00 F1A0)

Register Acronym	Base Address +	Register Name	Section Location
IPR0	$0	Interrupt Priority Register 0	5.6.1
IPR1	$1	Interrupt Priority Register 1	5.6.2
IPR2	$2	Interrupt Priority Register 2	5.6.3
IPR3	$3	Interrupt Priority Register 3	5.6.4
IPR4	$4	Interrupt Priority Register 4	5.6.5
IPR5	$5	Interrupt Priority Register 5	5.6.6
IPR6	$6	Interrupt Priority Register 6	5.6.7
IPR7	$7	Interrupt Priority Register 7	5.6.8
IPR8	$8	Interrupt Priority Register 8	5.6.9
IPR9	$9	Interrupt Priority Register 9	5.6.10
VBA	$A	Vector Base Address Register	5.6.11
FIM0	$B	Fast Interrupt 0 Match Register	5.6.12
FIVAL0	$C	Fast Interrupt 0 Vector Address Low Register	5.6.13
FIVAH0	$D	Fast Interrupt 0 Vector Address High Register	5.6.14
FIM1	$E	Fast Interrupt 1 Match Register	5.6.15
FIVAL1	$F	Fast Interrupt 1 Vector Address Low Register	5.6.16
FIVAH1	$10	Fast Interrupt 1 Vector Address High Register	5.6.17
IRQP0	$11	IRQ Pending Register 0	5.6.18
IRQP1	$12	IRQ Pending Register 1	5.6.19
IRQP2	$13	IRQ Pending Register 2	5.6.20
IRQP3	$14	IRQ Pending Register 3	5.6.21
IRQP4	$15	IRQ Pending Register 4	5.6.22
IRQP5	$16	IRQ Pending Register 5	5.6.23
		Reserved	
ICTL	$1D	Interrupt Control Register	5.6.30

Add. Offset	Register Name		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	IPR0	R	0	0	BKPT_ U0 IPL		STPCNT IPL		0	0	0	0	0	0	0	0	0	0
		W																
$1	IPR1	R	0	0	0	0	0	0	0	0	0	0	RX_REG IPL		TX_REG IPL		TRBUF IPL	
		W																
$2	IPR2	R	FMCBE IPL		FMCC IPL		FMERR IPL		LOCK IPL		LVI IPL		0	0	0	0	IRQA IPL	
		W																
$3	IPR3	R	0	0	0	0	0	0	FCMSGBUF IPL		FCWKUP IPL		FCERR IPL		FCBOFF IPL		0	0
		W																
$4	IPR4	R	SPI0_RCV IPL		SPI1_XMIT IPL		SPI1_RCV IPL		0	0	0	0	GPIOA IPL		GPIOB IPL		GPIOC IPL	
		W																
$5	IPR5	R	0	0	0	0	SCI1_RCV IPL		SCI1_RERR IPL		0	0	SCI1_TIDL IPL		SCI1_XMIT IPL		SPI0_XMIT IPL	
		W																
$6	IPR6	R	TMRC0 IPL		0	0	0	0	0	0	0	0	0	0	DEC0_XIRQ IPL		DEC0_HIRQ IPL	
		W											0	0				
$7	IPR7	R	TMRA0 IPL		0	0	0	0	0	0	0	0	TMRC3 IPL		TMRC2 IPL		TMRC1 IPL	
		W																
$8	IPR8	R	SCI0_RCV IPL		SCI0_RERR IPL		0	0	SCI0_TIDL IPL		SCI0_XMIT IPL		TMRA3 IPL		TMRA2 IPL		TMRA1 IPL	
		W																
$9	IPR9	R	PWMA F IPL		0	0	PWMA_RL IPL		0	0	ADCA_ZC IPL		0	0	ADCA_CC IPL		0	0
		W																
$A	VBA	R	0	0	0	VECTOR BASE ADDRESS												
		W																
$B	FIM0	R	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0						
		W																
$C	FIVAL0	R	FAST INTERRUPT 0 VECTOR ADDRESS LOW															
		W																
$D	FIVAH0	R	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0 VECTOR ADDRESS HIGH				
		W																
$E	FIM1	R	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1						
		W																
$F	FIVAL1	R	FAST INTERRUPT 1 VECTOR ADDRESS LOW															
		W																
$10	FIVAH1	R	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1 VECTOR ADDRESS HIGH				
		W																
$11	IRQP0	R	PENDING [16:2]															1
		W																
$12	IRQP1	R	PENDING [32:17]															
		W																
$13	IRQP2	R	PENDING [48:33]															
		W																
$14	IRQP3	R	PENDING [64:49]															
		W																
$15	IRQP4	R	PENDING [80:65]															
		W																
$16	IRQP5	R	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	PEND-ING [81]
		W																
	Reserved																	
$1D	ICTL	R	INT	IPIC			VAB						INT_ DIS	1	0	IRQA STATE	0	$\overline{\text{IRQA}}$ EDG
		W																

= Reserved

Figure 5-2 ITCN Register Map Summary

5.6.1 Interrupt Priority Register 0 (IPR0)

Base + $0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	BKPT_U0IPL		STPCNT IPL		0	0	0	0	0	0	0	0	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-3 Interrupt Priority Register 0 (IPR0)

5.6.1.1 Reserved—Bits 15–14

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.1.2 EOnCE Breakpoint Unit 0 Interrupt Priority Level (BKPT_U0 IPL)—Bits13–12

This field is used to set the interrupt priority levels for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.3 EOnCE Step Counter Interrupt Priority Level (STPCNT IPL)—Bits 11–10

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.4 Reserved—Bits 9–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.2 Interrupt Priority Register 1 (IPR1)

Base + $1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	RX_REG IPL		TX_REG IPL		TRBUF IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-4 Interrupt Priority Register 1 (IPR1)

5.6.2.1 Reserved—Bits 15–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.2.2 EOnCE Receive Register Full Interrupt Priority Level (RX_REG IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.2.3 EOnCE Transmit Register Empty Interrupt Priority Level (TX_REG IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.2.4 EOnCE Trace Buffer Interrupt Priority Level (TRBUF IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.3 Interrupt Priority Register 2 (IPR2)

Base + $2	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FMCBE IPL		FMCC IPL		FMERR IPL		LOCK IPL		LVI IPL		0	0	0	0	IRQA IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-5 Interrupt Priority Register 2 (IPR2)

5.6.3.1 Flash Memory Command, Data, Address Buffers Empty Interrupt Priority Level (FMCBE IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.2 Flash Memory Command Complete Priority Level (FMCC IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.3 Flash Memory Error Interrupt Priority Level (FMERR IPL)—Bits 11–10

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.4 PLL Loss of Lock Interrupt Priority Level (LOCK IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.5 Low Voltage Detector Interrupt Priority Level (LVI IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.6 Reserved—Bits 5–2

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.3.7 External IRQ A Interrupt Priority Level (IRQA IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4 Interrupt Priority Register 3 (IPR3)

Base + $3	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	FCMSGBUF IPL		FCWKUP IPL		FCERR IPL		FCBOFF IPL		0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-6 Interrupt Priority Register 3 (IPR3)

5.6.4.1 Reserved—Bits 15–10

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.4.2 FlexCAN Message Buffer Interrupt Priority Level (FCMSGBUF IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4.3 FlexCAN Wake Up Interrupt Priority Level (FCWKUP IPL)— Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4.4 FlexCAN Error Interrupt Priority Level (FCERR IPL)— Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4.5 FlexCAN Bus Off Interrupt Priority Level (FCBOFF IPL)— Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4.6 Reserved—Bits 1–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.5 Interrupt Priority Register 4 (IPR4)

Base + $4	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	SPI0_RCV IPL		SPI1_XMIT IPL		SPI1_RCV IPL		0	0	0	0	GPIOA IPL		GPIOB IPL		GPIOC IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-7 Interrupt Priority Register 4 (IPR4)

5.6.5.1 SPI0 Receiver Full Interrupt Priority Level (SPI0_RCV IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.2 SPI1 Transmit Empty Interrupt Priority Level (SPI1_XMIT IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.3 SPI1 Receiver Full Interrupt Priority Level (SPI1_RCV IPL)—Bits 11–10

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.4 Reserved—Bits 9–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.5.5 GPIO_A Interrupt Priority Level (GPIOA IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.6 GPIO_B Interrupt Priority Level (GPIOB IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.7 GPIO_C Interrupt Priority Level (GPIOC IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6 Interrupt Priority Register 5 (IPR5)

Base + $5	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	SCI1_RCV IPL		SCI1_RERR IPL		0	0	SCI1_TIDL IPL		SCI1_XMIT IPL		SPI0_XMIT IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-8 Interrupt Priority Register 5 (IPR5)

5.6.6.1 Reserved—Bits 15–12

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.6.2 SCI1 Receiver Full Interrupt Priority Level (SCI1_RCV IPL)—Bits 11–10

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.3 SCI1 Receiver Error Interrupt Priority Level (SCI1_RERR IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.4 Reserved—Bits 7–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.6.5 SCI1 Transmitter Idle Interrupt Priority Level (SCI1_TIDL IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.6 SCI1 Transmitter Empty Interrupt Priority Level (SCI1_XMIT IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.7 SPI0 Transmitter Empty Interrupt Priority Level (SPI0_XMIT IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7 Interrupt Priority Register 6 (IPR6)

Base + $6	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	TMRC0 IPL		0	0	0	0	0	0	0	0	0	0	DEC0_XIRQ IPL		DEC0_HIRQ IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-9 Interrupt Priority Register 6 (IPR6)

5.6.7.1 Timer C, Channel 0 Interrupt Priority Level (TMRC_0 IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.2 Reserved—Bits 13–4

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.7.3 Quadrature Decoder 0, INDEX Pulse Interrupt Priority Level (DEC0_XIRQ IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.4 Quadrature Decoder 0, HOME Signal Transition or Watchdog Timer Interrupt Priority Level (DEC0_HIRQ IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8 Interrupt Priority Register 7 (IPR7)

Base + $7	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	TMRA0 IPL		0	0	0	0	0	0	0	0	TMRC3 IPL		TMRC2 IPL		TMRC1 IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-10 Interrupt Priority Register (IPR7)

5.6.8.1 Timer A, Channel 0 Interrupt Priority Level (TMRA0 IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8.2 Reserved—Bits 13–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.8.3 Timer C, Channel 3 Interrupt Priority Level (TMRC3 IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8.4 Timer C, Channel 2 Interrupt Priority Level (TMRC2 IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8.5 Timer C, Channel 1 Interrupt Priority Level (TMRC1 IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9 Interrupt Priority Register 8 (IPR8)

Base + $8	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	SCI0_RCV IPL		SCI0_RERR IPL		0	0	SCI0_TIDL IPL		SCI0_XMIT IPL		TMRA3 IPL		TMRA2 IPL		TMRA1 IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-11 Interrupt Priority Register 8 (IPR8)

5.6.9.1 SCI0 Receiver Full Interrupt Priority Level (SCI0_RCV IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.2 SCI0 Receiver Error Interrupt Priority Level (SCI0_RERR IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.3 Reserved—Bits 11–10

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.9.4 SCI0 Transmitter Idle Interrupt Priority Level (SCI0_TIDL IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.5 SCI0 Transmitter Empty Interrupt Priority Level (SCI0_XMIT IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.6 Timer A, Channel 3 Interrupt Priority Level (TMRA3 IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.7 Timer A, Channel 2 Interrupt Priority Level (TMRA2 IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.8 Timer A, Channel 1 Interrupt Priority Level (TMRA1 IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10 Interrupt Priority Register 9 (IPR9)

Base + $9	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PWMAF IPL		0	0	PWMA_RL IPL		0	0	ADCA_ZC IPL		0	0	ADCA_CC IPL		0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-12 Interrupt Priority Register 9 (IPR9)

5.6.10.1 PWM A Fault Interrupt Priority Level (PWMAF IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10.2 Reserved—Bits 13–12

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.10.3 Reload PWM A Interrupt Priority Level (PWMA_RL IPL)—Bits 11–10

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10.4 Reserved—Bits 9–8

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.10.5 ADC A Zero Crossing or Limit Error Interrupt Priority Level (ADCA_ZC IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10.6 Reserved—Bits 5–4

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.10.7 ADC A Conversion Complete Interrupt Priority Level (ADCA_CC IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10.8 Reserved—Bits 1–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.11 Vector Base Address Register (VBA)

Base + $A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	VECTOR BASE ADDRESS												
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-13 Vector Base Address Register (VBA)

5.6.11.1 Reserved—Bits 15–13

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.11.2 Interrupt Vector Base Address (VECTOR BASE ADDRESS)—Bits 12–0

The contents of this register determine the location of the Vector Address Table. The value in this register is used as the upper 13 bits of the interrupt vector address. The lower eight bits of the ISR address are determined based upon the highest-priority interrupt; see **Section 5.3.1** for details.

5.6.12 Fast Interrupt 0 Match Register (FIM0)

Base + $B	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0						
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-14 Fast Interrupt 0 Match Register (FIM0)

5.6.12.1 Reserved—Bits 15–7

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.12.2 Fast Interrupt 0 Vector Number (FAST INTERRUPT 0)—Bits 6–0

This value determines which IRQ will be a Fast Interrupt 0. Fast interrupts vector directly to a service routine based on values in the Fast Interrupt Vector Address registers without having to go to a jump table first; see **Section 5.3.3** for details. IRQs used as fast interrupts *must* be set to priority level 2. Unexpected results will occur if a fast interrupt vector is set to any other priority. Fast interrupts automatically become the highest-priority level 2 interrupt, regardless of their location in the interrupt table, prior to being declared as fast interrupt. Fast Interrupt 0 has priority over Fast Interrupt 1. To determine the vector number of each IRQ, refer to **Table 4-3**.

5.6.13 Fast Interrupt 0 Vector Address Low Register (FIVAL0)

Base + $C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FAST INTERRUPT 0 VECTOR ADDRESS LOW															
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-15 Fast Interrupt 0 Vector Address Low Register (FIVAL0)

5.6.13.1 Fast Interrupt 0 Vector Address Low (FIVAL0)—Bits 15–0

The lower 16 bits of the vector address used for Fast Interrupt 0. This register is combined with FIVAH0 to form the 21-bit vector address for Fast Interrupt 0 defined in the FIM0 register.

5.6.14 Fast Interrupt 0 Vector Address High Register (FIVAH0)

Base + $D	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0 VECTOR ADDRESS HIGH				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-16 Fast Interrupt 0 Vector Address High Register (FIVAH0)

5.6.14.1 Reserved—Bits 15–5

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.14.2 Fast Interrupt 0 Vector Address High (FIVAH0)—Bits 4–0

The upper five bits of the vector address used for Fast Interrupt 0. This register is combined with FIVAL0 to form the 21-bit vector address for Fast Interrupt 0 defined in the FIM0 register.

5.6.15 Fast Interrupt 1 Match Register (FIM1)

Base + $E	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1						
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-17 Fast Interrupt 1 Match Register (FIM1)

5.6.15.1 Reserved—Bits 15–7

This bit field is reserved or not implemented. It is read as 0, but cannot be modified by writing.

5.6.15.2 Fast Interrupt 1 Vector Number (FAST INTERRUPT 1)—Bits 6–0

This value determines which IRQ will be a Fast Interrupt 1. Fast interrupts vector directly to a service routine based on values in the Fast Interrupt Vector Address registers without having to go to a jump table first; see **Section 5.3.3** for details. IRQs used as fast interrupts *must* be set to priority level 2. Unexpected results will occur if a fast interrupt vector is set to any other priority. Fast interrupts automatically become the highest-priority level 2 interrupt, regardless of their location in the interrupt table, prior to being declared as fast interrupt. Fast Interrupt 0 has priority over Fast Interrupt 1. To determine the vector number of each IRQ, refer to **Table 4-3**.

5.6.16 Fast Interrupt 1 Vector Address Low Register (FIVAL1)

Base + $F	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FAST INTERRUPT 1 VECTOR ADDRESS LOW															
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-18 Fast Interrupt 1 Vector Address Low Register (FIVAL1)

5.6.16.1 Fast Interrupt 1 Vector Address Low (FIVAL1)—Bits 15–0

The lower 16 bits of the vector address used for Fast Interrupt 1. This register is combined with FIVAH1 to form the 21-bit vector address for Fast Interrupt 1 defined in the FIM1 register.

5.6.17 Fast Interrupt 1 Vector Address High Register (FIVAH1)

Base + $10	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1 VECTOR ADDRESS HIGH				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-19 Fast Interrupt 1 Vector Address High Register (FIVAH1)

5.6.17.1 Reserved—Bits 15–5

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.17.2 Fast Interrupt 1 Vector Address High (FIVAH1)—Bits 4–0

The upper five bits of the vector address are used for Fast Interrupt 1. This register is combined with FIVAL1 to form the 21-bit vector address for Fast Interrupt 1 defined in the FIM1 register.

5.6.18 IRQ Pending 0 Register (IRQP0)

Base + $11	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [16:2]															1
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-20 IRQ Pending 0 Register (IRQP0)

5.6.18.1 IRQ Pending (PENDING)—Bits 16–2

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.18.2 Reserved—Bit 0

This bit is reserved or not implemented. It is read as 1 and cannot be modified by writing.

5.6.19 IRQ Pending 1 Register (IRQP1)

$Base + $12	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [32:17]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-21 IRQ Pending 1 Register (IRQP1)

5.6.19.1 IRQ Pending (PENDING)—Bits 32–17

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.20 IRQ Pending 2 Register (IRQP2)

Base + $13	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [48:33]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-22 IRQ Pending 2 Register (IRQP2)

5.6.20.1 IRQ Pending (PENDING)—Bits 48–33

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.21 IRQ Pending 3 Register (IRQP3)

Base + $14	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [64:49]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-23 IRQ Pending 3 Register (IRQP3)

5.6.21.1 IRQ Pending (PENDING)—Bits 64–49

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.22 IRQ Pending 4 Register (IRQP4)

Base + $15	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [80:65]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-24 IRQ Pending 4 Register (IRQP4)

5.6.22.1 IRQ Pending (PENDING)—Bits 80–65

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.23 IRQ Pending 5 Register (IRQP5)

Base + $16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	PEND-ING [81]
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-25 IRQ Pending Register 5 (IRQP5)

5.6.23.1 Reserved—Bits 96–82

This bit field is reserved or not implemented. The bits are read as 1 and cannot be modified by writing.

5.6.23.2 IRQ Pending (PENDING)—Bit 81

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.24 Reserved—Base + 17

5.6.25 Reserved—Base + 18

5.6.26 Reserved—Base + 19

5.6.27 Reserved—Base + 1A

5.6.28 Reserved—Base + 1B

5.6.29 Reserved—Base + 1C

5.6.30 ITCN Control Register (ICTL)

Base + $1D	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	INT	IPIC		VAB							INT_DIS	1	0	$\overline{\text{IRQA}}$ STATE	0	$\overline{\text{IRQA}}$ EDG
Write																
RESET	0	0	0	1	0	0	0	0	0	0	0	1	1	1	0	0

Figure 5-26 ITCN Control Register (ICTL)

5.6.30.1 Interrupt (INT)—Bit 15

This *read-only* bit reflects the state of the interrupt to the 56800E core.

- 0 = No interrupt is being sent to the 56800E core
- 1 = An interrupt is being sent to the 56800E core

5.6.30.2 Interrupt Priority Level (IPIC)—Bits 14–13

These *read-only* bits reflect the state of the new interrupt priority level bits being presented to the 56800E core at the time the last IRQ was taken. This field is only updated when the 56800E core jumps to a new interrupt service routine.

Note: Nested interrupts may cause this field to be updated before the original interrupt service routine can read it.

- 00 = Required nested exception priority levels are 0, 1, 2, or 3
- 01 = Required nested exception priority levels are 1, 2, or 3
- 10 = Required nested exception priority levels are 2 or 3
- 11 = Required nested exception priority level is 3

5.6.30.3 Vector Number - Vector Address Bus (VAB)—Bits 12–6

This *read-only* field shows the vector number (VAB[7:1]) used at the time the last IRQ was taken. This field is only updated when the 56800E core jumps to a new interrupt service routine.

Note: Nested interrupts may cause this field to be updated before the original interrupt service routine can read it.

5.6.30.4 Interrupt Disable (INT_DIS)—Bit 5

This bit allows all interrupts to be disabled.

- 0 = Normal operation (default)
- 1 = All interrupts disabled

5.6.30.5 Reserved—Bit 4

This bit field is reserved or not implemented. It is read as 1 and cannot be modified by writing.

5.6.30.6 Reserved—Bit 3

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.30.7 $\overline{\text{IRQA}}$ State Pin ($\overline{\text{IRQA}}$ STATE)—Bit 2

This *read-only* bit reflects the state of the external $\overline{\text{IRQA}}$ pin.

5.6.30.8 $\overline{\text{Reserved}}$—Bit 1

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.30.9 $\overline{\text{IRQA}}$ Edge Pin ($\overline{\text{IRQA}}$ Edg)—Bit 0

This bit controls whether the external $\overline{\text{IRQA}}$ interrupt is edge- or level-sensitive. During Stop and Wait modes, it is automatically level-sensitive.

- 0 = $\overline{\text{IRQA}}$ interrupt is a low-level sensitive (default)
- 1 = $\overline{\text{IRQA}}$ interrupt is falling-edge sensitive

5.7 Resets

5.7.1 Reset Handshake Timing

The ITCN provides the 56800E core with a reset vector address whenever $\overline{\text{RESET}}$ is asserted. The reset vector will be presented until the second rising clock edge after $\overline{\text{RESET}}$ is released.

5.7.2 ITCN After Reset

After reset, all of the ITCN registers are in their default states. This means all interrupts are disabled, except the core IRQs with fixed priorities:

- Illegal Instruction
- SW Interrupt 3
- HW Stack Overflow
- Misaligned Long Word Access
- SW Interrupt 2
- SW Interrupt 1
- SW Interrupt 0
- SW Interrupt LP

These interrupts are enabled at their fixed priority levels.

Part 6 System Integration Module (SIM)

6.1 Introduction

The SIM module is a system catchall for the glue logic that ties together the system-on-chip. It controls distribution of resets and clocks and provides a number of control features. The system integration module is responsible for the following functions:

- Reset sequencing
- Clock control & distribution
- Stop/Wait control
- Pull-up enables for selected peripherals
- System status registers
- Registers for software access to the JTAG ID of the chip
- Enforcing Flash security

These are discussed in more detail in the sections that follow.

6.2 Features

The SIM has the following features:

- Flash security feature prevents unauthorized access to code/data contained in on-chip flash memory
- Power-saving clock gating for peripherals
- Three power modes (Run, Wait, Stop) to control power utilization
  - — Stop mode shuts down the 56800E core, system clock, and peripheral clock
  - — Stop mode entry can optionally disable PLL and Oscillator (low power vs. fast restart)
  - — Wait mode shuts down the 56800E core and unnecessary system clock operation
  - — Run mode supports full part operation
- Controls to enable/disable the 56800E core WAIT and STOP instructions
- Controls reset sequencing after reset
- Software-initiated reset
- Four 16-bit registers reset only by a Power-On Reset usable for general purpose software control
- System Control Register
- Registers for software access to the JTAG ID of the chip

6.3 Operating Modes

Since the SIM is responsible for distributing clocks and resets across the chip, it must understand the various chip operating modes and take appropriate action. These are:

- **Reset Mode,** which has two submodes:
  - — Total Reset Mode
    - – 56800E Core and all peripherals are reset
  - — Core-Only Reset Mode
    - – 56800E Core in reset, peripherals are active
    - – This mode is required to provide the on-chip Flash interface module time to load data from Flash into FM registers
- **Run Mode**
  This is the primary mode of operation for this device. In this mode, the 56800E controls chip operation.
- **Debug Mode**
  The 56800E is controlled via JTAG/EOnCE when in debug mode. All peripherals, except the COP and PWMs, continue to run. COP is disabled and PWM outputs are optionally switched off to disable any motor from being driven; see the PWM chapter in the **56F8300 Peripheral User Manual** for details.
- **Wait Mode**
  In Wait mode, the core clock and memory clocks are disabled. Optionally, the COP can be stopped. Similarly, it is an option to switch off PWM outputs to disable any motor from being driven. All other peripherals continue to run.
- **Stop Mode**
  56800E, memory and most peripheral clocks are shut down. Optionally, the COP and CAN can be stopped. For lowest power consumption in Stop mode, the PLL can be shut down. This must be done explicitly before entering Stop mode, since there is no automatic mechanism for this. The CAN (along with any non-gated interrupt) is capable of waking the chip up from Stop mode, but is not fully functional in Stop mode.

6.4 Operating Mode Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NL							CM	XP	SD	R	SA	EX	0	MB	MA
Type	R/W							R/W	R/W	R/W	R/W	R/W	R/W		R/W	R/W
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X	0

Figure 6-1 OMR

The reset state for the MB bit will depend on the Flash secured state. See **Section 4.2** and **Part 7** for detailed information on how the Operating Mode Register (OMR) MA and MB bits operate in this device. The EX bit is not functional in this device since there is no external memory interface. For all other bits, see the **56F8300 Peripheral User Manual**.

Note: The OMR is not a Memory Map register; it is directly accessible in code through the acronym OMR.

6.5 Register Descriptions

Table 6-1 SIM Registers (SIM_BASE = $00 F350)

Address Offset	Address Acronym	Register Name	Section Location
Base + $0	SIM_CONTROL	Control Register	6.5.1
Base + $1	SIM_RSTSTS	Reset Status Register	6.5.2
Base + $2	SIM_SCR0	Software Control Register 0	6.5.3
Base + $3	SIM_SCR1	Software Control Register 1	6.5.3
Base + $4	SIM_SCR2	Software Control Register 2	6.5.3
Base + $5	SIM_SCR3	Software Control Register 3	6.5.3
Base + $6	SIM_MSH_ID	Most Significant Half of JTAG ID	6.5.4
Base + $7	SIM_LSH_ID	Least Significant Half of JTAG ID	6.5.5
Base + $8	SIM_PUDR	Pull-up Disable Register	6.5.6
		Reserved	
Base + $A	SIM_CLKOSR	CLKO Select Register	6.5.7
Base + $B	SIM_GPS	GPIO Peripheral Select Register	6.5.8
Base + $C	SIM_PCE	Peripheral Clock Enable Register	6.5.9
Base + $D	SIM_ISALH	I/O Short Address Location High Register	6.5.10
Base + $E	SIM_ISALL	I/O Short Address Location Low Register	6.5.10

Add. Offset	Register Name		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	SIM_ CONTROL	R	0	0	0	0	0	0	0	0	0	0	ONCE EBL	SW RST	STOP_ DISABLE		WAIT_ DISABLE	
		W																
$1	SIM_ RSTSTS	R	0	0	0	0	0	0	0	0	0	0	SWR	COPR	EXTR	POR	0	0
		W																
$2	SIM_SCR0	R	FIELD															
		W																
$3	SIM_SCR1	R	FIELD															
		W																
$4	SIM_SCR2	R	FIELD															
		W																
$5	SIM_SCR3	R	FIELD															
		W																
$6	SIM_MSH_ID	R	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0
		W																
$7	SIM_LSH_ID	R	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
		W																
$8	SIM_PUDR	R	0	0	0	0	$\overline{\text{RESET}}$	IRQ	0	0	0	0	0	0	JTAG	0	0	0
		W																
	Reserved																	
$A	SIM_ CLKOSR	R	0	0	0	0	0	0	$\overline{\text{PHSA}}$	$\overline{\text{PHSB}}$	$\overline{\text{INDEX}}$	$\overline{\text{HOME}}$	CLK DIS	CLKOSEL				
		W																
$B	SIM_GPS	R	0	0	0	0	0	0	0	0	C6	C5	B1	B0	A5	A4	A3	A2
		W																
$C	SIM_PCE	R	1	1	ADCA	CAN	1	DEC0	1	TMRC	1	TMRA	SCI1	SCI0	SPI1	SPI0	1	PWMA
		W																
$D	SIM_ISALH	R	1	1	1	1	1	1	1	1	1	1	1	1	1	1	ISAL[23:22]	
		W																
$E	SIM_ISALL	R	ISAL[21:6]															
		W																

= Reserved

Figure 6-2 SIM Register Map Summary

6.5.1 SIM Control Register (SIM_CONTROL)

Base + $0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	ONCE EBL	SW RST	STOP_ DISABLE		WAIT_ DISABLE	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-3 SIM Control Register (SIM_CONTROL)

6.5.1.1 Reserved—Bits 15–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.1.2 OnCE Enable (ONCE EBL)—Bit 5

- 0 = OnCE clock to 56800E core enabled when core TAP is enabled
- 1 = OnCE clock to 56800E core is always enabled

6.5.1.3 Software Reset (SW RST)—Bit 4

Writing 1 to this field will cause the part to reset.

6.5.1.4 Stop Disable (STOP_DISABLE)—Bits 3–2

- 00 = Stop mode will be entered when the 56800E core executes a STOP instruction
- 01 = The 56800E STOP instruction will not cause entry into Stop mode; STOP_DISABLE can be reprogrammed in the future
- 10 = The 56800E STOP instruction will not cause entry into Stop mode; STOP_DISABLE can then only be changed by resetting the device
- 11 = Same operation as 10

6.5.1.5 Wait Disable (WAIT_DISABLE)—Bits 1–0

- 00 = Wait mode will be entered when the 56800E core executes a WAIT instruction
- 01 = The 56800E WAIT instruction will not cause entry into Wait mode; WAIT_DISABLE can be reprogrammed in the future
- 10 = The 56800E WAIT instruction will not cause entry into Wait mode; WAIT_DISABLE can then only be changed by resetting the device
- 11 = Same operation as 10

6.5.2 SIM Reset Status Register (SIM_RSTSTS)

Bits in this register are set upon any system reset and are initialized only by a Power-On Reset (POR). A reset (other than POR) will only set bits in the register; bits are not cleared. Only software should clear this register.

Base + $1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	SWR	COPR	EXTR	POR	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0					0	0

Figure 6-4 SIM Reset Status Register (SIM_RSTSTS)

6.5.2.1 Reserved—Bits 15–6

This bit field is reserved or not implemented. It is read as zero and cannot be modified by writing.

6.5.2.2 Software Reset (SWR)—Bit 5

When 1, this bit indicates that the previous reset occurred as a result of a software reset (write to SW RST bit in the SIM_CONTROL register). This bit will be cleared by any hardware reset or by software. Writing a 0 to this bit position will set the bit, while writing a 1 to the bit will clear it.

6.5.2.3 COP Reset (COPR)—Bit 4

When 1, the COPR bit indicates the Computer Operating Properly (COP) timer-generated reset has occurred. This bit will be cleared by a Power-On Reset or by software. Writing a 0 to this bit position will set the bit, while writing a 1 to the bit will clear it.

6.5.2.4 External Reset (EXTR)—Bit 3

If 1, the EXTR bit indicates an external system reset has occurred. This bit will be cleared by a Power-On Reset or by software. Writing a 0 to this bit position will set the bit while writing a 1 to the bit position will clear it. Basically, when the EXTR bit is 1, the previous system reset was caused by the external $\overline{\text{RESET}}$ pin being asserted low.

6.5.2.5 Power-On Reset (POR)—Bit 2

When 1, the POR bit indicates a Power-On Reset occurred some time in the past. This bit can be cleared only by software or by another type of reset. Writing a 0 to this bit will set the bit, while writing a 1 to the bit position will clear the bit. In summary, if the bit is 1, the previous system reset was due to a Power-On Reset.

6.5.2.6 Reserved—Bits 1–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.3 SIM Software Control Registers (SIM_SCR0, SIM_SCR1, SIM_SCR2, and SIM_SCR3)

Only SIM_SCR0 is shown in this section. SIM_SCR1, SIM_SCR2, and SIM_SCR3 are identical in functionality.

Base + $2	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FIELD															
Write																
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-5 SIM Software Control Register 0 (SIM_SCR0)

6.5.3.1 Software Control Data 1 (FIELD)—Bits 15–0

This register is reset only by the Power-On Reset (POR). It has no part-specific functionality and is intended for use by a software developer to contain data that will be unaffected by the other reset sources ($\overline{\text{RESET}}$ pin, software reset, and COP reset).

6.5.4 Most Significant Half of JTAG ID (SIM_MSH_ID)

This read-only register displays the most significant half of the JTAG ID for the chip. This register reads $01F4.

Base + $6	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0
Write																
RESET	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0

Figure 6-6 Most Significant Half of JTAG ID (SIM_MSH_ID)

6.5.5 Least Significant Half of JTAG ID (SIM_LSH_ID)

This read-only register displays the least significant half of the JTAG ID for the chip. This register reads $001D.

Base + $7	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1

Figure 6-7 Least Significant Half of JTAG ID (SIM_LSH_ID)

6.5.6 SIM Pull-up Disable Register (SIM_PUDR)

Most of the pins on the chip have on-chip pull-up resistors. Pins which can operate as GPIO can have these resistors disabled via the GPIO function. Non-GPIO pins can have their pull-ups disabled by setting the appropriate bit in this register. Disabling pull-ups is done on a peripheral-by-peripheral basis (for pins not muxed with GPIO). Each bit in the register (see **Figure 6-8**) corresponds to a functional group of pins. See **Table 2-2** to identify which pins can deactivate the internal pull-up resistor.

Base + $8	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	$\overline{\text{RESET}}$	IRQ	0	0	0	0	0	0	JTAG	0	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-8 SIM Pull-up Disable Register (SIM_PUDR)

6.5.6.1 Reserved—Bits 15–12

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.6.2 $\overline{\text{RESET}}$—Bit 11

This bit controls the pull-up resistors on the $\overline{\text{RESET}}$ pin.

6.5.6.3 IRQ—Bit 10

This bit controls the pull-up resistors on the $\overline{\text{IRQA}}$ pin.

6.5.6.4 Reserved—Bits 9–4

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.6.5 JTAG—Bit 3

This bit controls the pull-up resistors on the $\overline{\text{TRST}}$ (This pin is always tied inactive on the 56F8322), TMS and TDI pins.

6.5.6.6 Reserved—Bits 2–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.7 CLKO Select Register (SIM_CLKOSR)

The CLKO select register can be used to multiplex out any one of the clocks generated inside the clock generation and SIM modules. The default value is SYS_CLK. All other clocks primarily muxed out are for test purposes only, and are subject to significant unspecified latencies at high frequencies.

The upper four bits of the GPIOB register can function as GPIO, Quad Decoder #0 signals, or as additional clock output signals. GPIO has priority and is enabled/disabled via the GPIOB_PER. If GPIOB[7:4] are programmed to operate as peripheral outputs, then the choice between Quad Decoder #0 and additional clock outputs is made here in the CLKOSR. The default state is for the peripheral function of GPIOB[7:4] to be programmed as Quad Decoder #0. This can be changed by altering $\overline{\text{PHASE0}}$ through $\overline{\text{INDEX}}$ as shown in **Figure 6-9**.

The CLKOUT pin is not bonded out in this device. Instead, it is offered only as a pad for die-level testing.

Base + $A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	$\overline{\text{PHSA}}$	$\overline{\text{PHSB}}$	$\overline{\text{INDEX}}$	$\overline{\text{HOME}}$	CLK DIS	CLKOSEL				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Figure 6-9 CLKO Select Register (SIM_CLKOSR)

6.5.7.1 Reserved—Bits 15–10

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.7.2 PHASEA0 ($\overline{\text{PHSA}}$)—Bit 9

- 0 = Peripheral output function of GPIOB[7] is defined to be PHASEA0
- 1 = Peripheral output function of GPI B[7] is defined to be the oscillator clock (MSTR_OSC, see **Figure 3-4**)

6.5.7.3 PHASEB0 ($\overline{\text{PHSB}}$)—Bit 8

- 0 = Peripheral output function of GPIOB[6] is defined to be PHASEB0
- 1 = Peripheral output function of GPIOB[6] is defined to be SYS_CLK2

6.5.7.4 INDEX0 ($\overline{\text{INDEX}}$)—Bit 7

- 0 = Peripheral output function of GPIOB[5] is defined to be INDEX0
- 1 = Peripheral output function of GPIOB[5] is defined to be SYS_CLK

6.5.7.5 HOME0 ($\overline{\text{HOME}}$)—Bit 6

- 0 = Peripheral output function of GPIOB[4] is defined to be HOME0
- 1 = Peripheral output function of GPIOB[4] is defined to be the prescaler clock (FREF, see **Figure 3-4**)

6.5.7.6 Clockout Disable (CLKDIS)—Bit 5

- 0 = CLKOUT output is enabled and will output the signal indicated by CLKOSEL
- 1 = CLKOUT is tri-stated

6.5.7.7 CLockout Select (CLKOSEL)—Bits 4–0

Selects clock to be muxed out on the CLKO pin.

- 00000 = SYS_CLK (from ROCS - DEFAULT)
- 00001 = Reserved for factory test—56800E clock
- 00010 = Reserved for factory test—XRAM clock
- 00011 = Reserved for factory test—PFLASH odd clock
- 00100 = Reserved for factory test—PFLASH even clock
- 00101 = Reserved for factory test—BFLASH clock
- 00110 = Reserved for factory test—DFLASH clock
- 00111 = MSTR_OSC Oscillator output
- 01000 = F_{out} (from OCCS)
- 01001 = Reserved for factory test—IPB clock
- 01010 = Reserved for factory test—Feedback (from OCCS, this is path to PLL)
- 01011 = Reserved for factory test—Prescaler clock (from OCCS)
- 01100 = Reserved for factory test—Postscaler clock (from OCCS)
- 01101 = Reserved for factory test—SYS_CLK2 (from OCCS)
- 01110 = Reserved for factory test—SYS_CLK_DIV2
- 01111 = Reserved for factory test—SYS_CLK_D
- 10000 = ADCA clock

6.5.8 SIM GPIO Peripheral Select Register (SIM_GPS)

All of the peripheral pins on the 56F8322 and 56F8122 share their I/O with GPIO ports. To select peripheral or GPIO control, program the GPIOx_PER register. When SPI 0 and SCI 1, Quad Timer C and SCI 0, or *PWMA* and SPI 1 are multiplexed, there are two possible peripherals as well as the GPIO functionality available for control of the I/O. The SIM_GPS register is used to determine which peripheral has control. The default peripherals are SPI 0, Quad Timer C, and *PWMA*.

Note: *PWM is NOT available in the 56F8122 device.*

As shown in **Figure 6-10**, the GPIO has the final control over which pin controls the I/O. SIM_GPS simply decides which peripheral will be routed to the I/O.

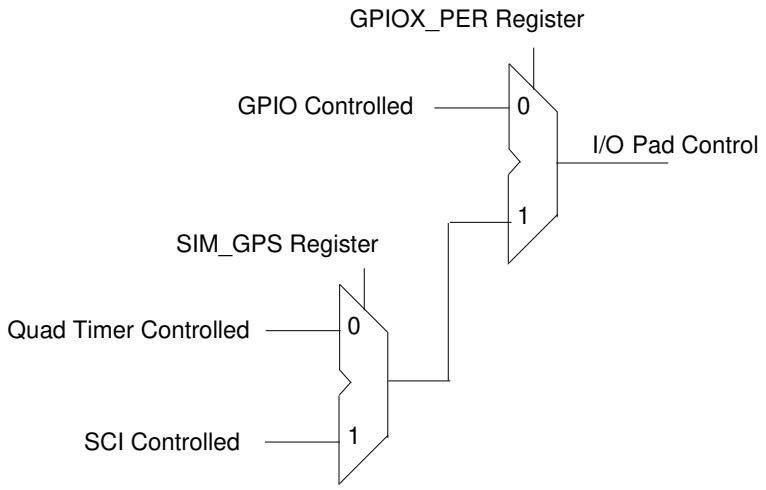


Figure 6-10 Overall Control of Pads Using SIM_GPS Control

Base + $B	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	C6	C5	B1	B0	A5	A4	A3	A2
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-11 GPIO Peripheral Select Register (SIM_GPS)

6.5.8.1 Reserved—Bits 15–8

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.8.2 GPIO C6 (C6)—Bit 7

This bit selects the alternate function for GPIOC6.

- 0 = TC0 (default)
- 1 = TXD0

6.5.8.3 GPIOC5 (C5)—Bit 6

This bit selects the alternate function for GPIOC5.

- 0 = TC1 (default)
- 1 = RXD0

6.5.8.4 GPIOB1 (B1)—Bit 5

This bit selects the alternate function for GPIOB1.

- 0 = MISO0 (default)
- 1 = RXD1

6.5.8.5 GPIOB0 (B0)—Bit 4

This bit selects the alternate function for GPIOB0.

- 0 = $\overline{SS0}$ (default)
- 1 = TXD1

6.5.8.6 GPIOA5 (A5)—Bit 3

This bit selects the alternate function for GPIOA5.

- 0 = PWMA5
- 1 = SCLK1

6.5.8.7 GPIOA4 (A4)—Bit 2

This bit selects the alternate function for GPIOA4.

- 0 = PWMA4
- 1 = MOS1

6.5.8.8 GPIOA3 (A3)—Bit 1

This bit selects the alternate function for GPIOA3.

- 0 = PWMA3
- 1 = MISO1

6.5.8.9 GPIOA2 (A2)—Bit 0

This bit selects the alternate function for GPIOA2.

- 0 = PWMA2
- 1 = $\overline{SS1}$

6.5.9 Peripheral Clock Enable Register (SIM_PCE)

The Peripheral Clock Enable register is used to enable or disable clocks to the peripherals as a power savings feature. The clocks can be individually controlled for each peripheral on the chip.

Base + $C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	1	1	ADCA	CAN	1	DEC0	1	TMRC	1	TMRA	SCI 1	SCI 0	SPI1	SPI0	1	PWMA
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 6-12 Peripheral Clock Enable Register (SIM_PCE)

6.5.9.1 Reserved—Bits 15–14

This bit field is reserved or not implemented. It is read as 1 and cannot be modified by writing.

6.5.9.2 Analog-to-Digital Converter A Enable (ADCA)—Bit 13

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.3 FlexCAN Enable (CAN)—Bit 12

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.4 Reserved—Bit 11

This bit field is reserved or not implemented. It is read as 1 and cannot be modified by writing.

6.5.9.5 Decoder 0 Enable (DEC0)—Bit 10

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.6 Reserved—Bit 9

This bit field is reserved or not implemented. It is read as 1 and cannot be modified by writing.

6.5.9.7 Quad Timer C Enable (TMRC)—Bit 8

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.8 Reserved—Bit 7

This bit field is reserved or not implemented. It is read as 1 and cannot be modified by writing.

6.5.9.9 Quad Timer A Enable (TMRA)—Bit 6

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.10 Serial Communications Interface 1 Enable (SCI1)—Bit 5

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.11 Serial Communications Interface 0 Enable (SCI0)—Bit 4

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.12 Serial Peripheral Interface 1 Enable (SPI1)—Bit 3

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.13 Serial Peripheral Interface 0 Enable (SPI0)—Bit 2

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.14 Reserved—Bit 1

This bit field is reserved or not implemented. It is read as 1 and cannot be modified by writing.

6.5.9.15 Pulse Width Modulator A Enable (PWMA)—Bit 0

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.10 I/O Short Address Location Register (SIM_ISALH and SIM_ISALL)

The I/O Short Address Location registers are used to specify the memory referenced via the I/O short address mode. The I/O short address mode allows the instruction to specify the lower six bits of address; the upper address bits are not directly controllable. This register set allows limited control of the full address, as shown in **Figure 6-13**.

Note: If this register is set to something other than the top of memory (EOnCE register space) and the EX bit in the OMR is set to 1, the JTAG port cannot access the on-chip EOnCE registers, and debug functions will be affected.

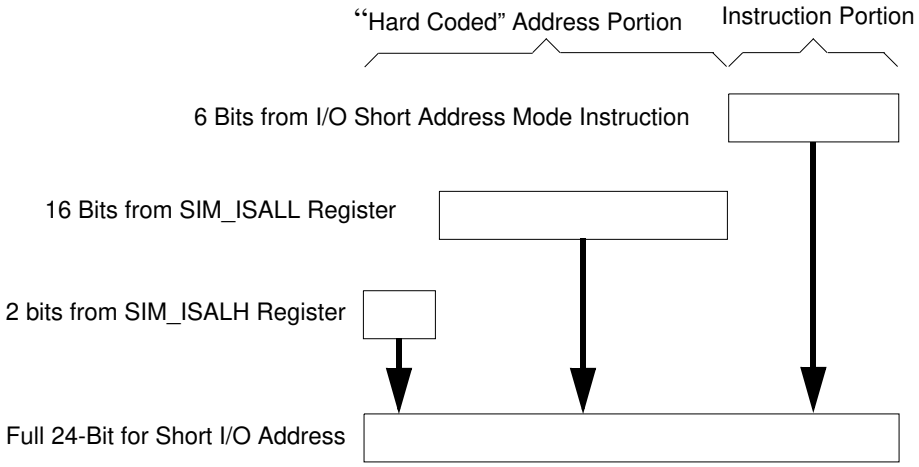


Figure 6-13 I/O Short Address Determination

With this register set, an interrupt driver can set the SIM_ISALL register pair to point to its peripheral registers and then use the I/O Short addressing mode to reference them. The ISR should restore this register to its previous contents prior to returning from interrupt.

Note: The default value of this register set points to the EOnCE registers.

Note: The pipeline delay between setting this register set and using short I/O addressing with the new value is five cycles.

Base + $D	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	1	1	1	1	1	1	1	1	1	1	1	1	1	1	ISAL[23:22]	
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 6-14 I/O Short Address Location High Register (SIM_ISALH)

6.5.10.1 Input/Output Short Address Low (ISAL[23:22])—Bit 1–0

This field represents the upper two address bits of the “hard coded” I/O short address.

Base + $E	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	ISAL[21:6]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 6-15 I/O Short Address Location Low Register (SIM_ISALL)

6.5.10.2 Input/Output Short Address Low (ISAL[21:6])—Bit 15–0

This field represents the lower 16 address bits of the “hard coded” I/O short address.

6.6 Clock Generation Overview

The SIM uses an internal master clock from the OCCS (CLKGEN) module to produce the peripheral and system (core and memory) clocks. The maximum master clock frequency is 120MHz. Peripheral and system clocks are generated at half the master clock frequency and therefore at a maximum 60MHz. The SIM provides power modes (Stop, Wait) and clock enables (SIM_PCE register, CLK_DIS, ONCE_EBL) to control which clocks are in operation. The OCCS, power modes, and clock enables provide a flexible means to manage power consumption.

Power utilization can be minimized in several ways. In the OCCS, the relaxation oscillator, crystal oscillator, and PLL may be shut down when not in use. When the PLL is in use, its prescaler and postscaler can be used to limit PLL and master clock frequency. Power modes permit system and/or peripheral clocks to be disabled when unused. Clock enables provide the means to disable individual clocks. Some peripherals provide further controls to disable unused subfunctions. Refer to **Part 3 On-Chip Clock Synthesis (OCCS)**, and the **56F8300 Peripheral User Manual** for further details.

The memory, peripheral and core clocks all operate at the same frequency (60MHz max).

6.7 Power-Down Modes

The 56F8322/56F8122 operate in one of three power-down modes, as shown in **Table 6-2**.

Table 6-2 Clock Operation in Power-Down Modes

Mode	Core Clocks	Peripheral Clocks	Description
Run	Active	Active	Device is fully functional
Wait	Core and memory clocks disabled	Active	Peripherals are active and can produce interrupts if they have not been masked off. Interrupts will cause the core to come out of its suspended state and resume normal operation. Typically used for power-conscious applications.
Stop	System clocks continue to be generated in the SIM, but most are gated prior to reaching memory, core and peripherals.		The only possible recoveries from Stop mode are: 1. CAN traffic (1st message will be lost) 2. Non-clocked interrupts ($\overline{\text{IRQA}}$) 3. COP reset 4. External reset 5. Power-on reset

All peripherals, except the COP/watchdog timer, run off the IPBus clock frequency, which is the same as the main processor frequency in this architecture. The maximum frequency of operation is SYS_CLK = 60MHz.

Refer to the PCE register in **Section 6.5.9** and ADC power modes. Power is a function of the system frequency, which can be controlled through the OCCS.

6.8 Stop and Wait Mode Disable Function

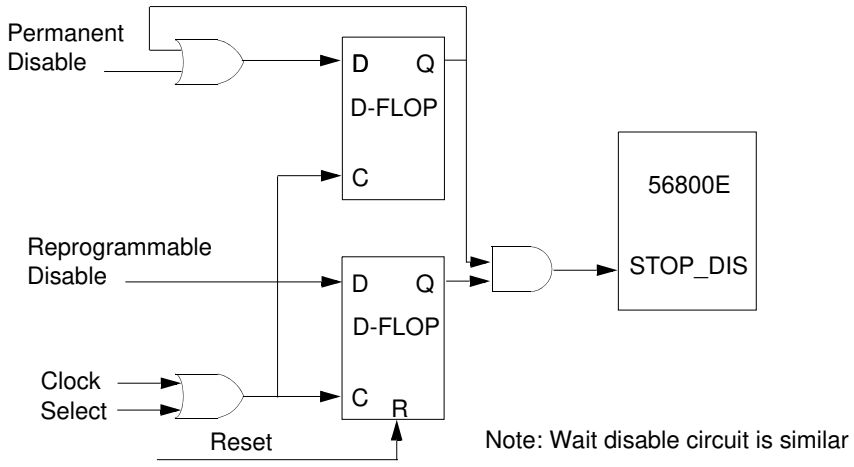


Figure 6-16 Internal Stop Disable Circuit

The 56800E core contains both STOP and WAIT instructions. Both put the CPU to sleep. For lowest power consumption in Stop mode, the PLL can be shut down. This must be done explicitly before entering Stop mode, since there is no automatic mechanism for this. When the PLL is shut down, the 56800E system clock must be set equal to the prescaler output.

Some applications require the 56800E STOP and WAIT instructions be disabled. To disable those instructions, write to the SIM control register (SIM_CONTROL) described in **Section 6.5.1** . This procedure can be on either a permanent or temporary basis. Permanently assigned applications last only until their next reset.

6.9 Resets

The SIM supports four sources of reset. The two asynchronous sources are the external $\overline{\text{RESET}}$ pin and the Power-On Reset (POR). The two synchronous sources are the software reset, which is generated within the SIM itself, by writing to the SIM_CONTROL register, and the COP reset.

Reset begins with the assertion of any of the reset sources. Release of reset to various blocks is sequenced to permit proper operation of the device. A POR reset is declared when reset is removed and any of the three voltage detectors (1.8V POR, 2.2V core voltage, or 2.7V I/O voltage) indicate a low supply voltage condition. POR will continue to be asserted until all voltage detectors indicate a stable supply is available (note that as power is removed POR is not declared until the 1.8V core voltage threshold is reached.) A POR reset is then extended for 64 clock cycles to permit stabilization of the clock source, followed by a 32 clock window in which SIM clocking is initiated. It is then followed by a 32 clock window in which peripherals are released to implement Flash security, and, finally, followed by a 32 clock window in which the core is initialized. After completion of the described reset sequence, application code will begin execution.

Resets may be asserted asynchronously, but are always released internally on a rising edge of the system clock.

Part 7 Security Features

The 56F8322/56F8122 offer security features intended to prevent unauthorized users from reading the contents of the Flash Memory (FM) array. The Flash security consists of several hardware interlocks that block the means by which an unauthorized user could gain access to the Flash array.

However, part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program, as this code would defeat the purpose of security. At the same time, the user may also wish to put a "backdoor" in his program. As an example, the user downloads a security key through the SCI, allowing access to a programming routine that updates parameters stored in another section of the Flash.

7.1 Operation with Security Enabled

Once the user has programmed the Flash with his application code, the device can be secured by programming the security bytes located in the FM configuration field, which occupies a portion of the FM array. These non-volatile bytes will keep the part secured through reset and through power-down of the device. Only two bytes within this field are used to enable or disable security. Refer to the Flash Memory chapter in the **56F8300 Peripheral User Manual** for the state of the security bytes and the resulting state of security. When Flash security mode is enabled in accordance with the method described in the Flash Memory module specification, the device will disable the core EOnCE debug capabilities. Normal program execution is otherwise unaffected.

7.2 Flash Access Blocking Mechanisms

The 56F8322/56F8122 have several operating functional and test modes. Effective Flash security must address operating mode selection and anticipate modes in which the on-chip Flash can be compromised and read without explicit user permission. Methods to block these are outlined in the next subsections.

7.2.1 Forced Operating Mode Selection

At boot time, the SIM determines in which functional modes the device will operate. These are:

- Unsecured Mode
- Secure Mode (EOnCE disabled)

When Flash security is enabled as described in the Flash Memory module specification, the device will disable the EOnCE debug interface.

7.2.2 Disabling EOnCE Access

On-chip Flash can be read by issuing commands across the EOnCE port, which is the debug interface for the 56800E CPU. The $\overline{\text{TRST}}$, TCLK, TMS, TDO, and TDI pins comprise a JTAG interface onto which the EOnCE port functionality is mapped. When the device boots, the chip-level JTAG TAP (Test Access Port) is active and provides the chip's boundary scan capability and access to the ID register.

Proper implementation of Flash security requires that no access to the EOnCE port is provided when security is enabled. The 56800E core has an input which disables reading of internal memory via the JTAG/EOnCE. The FM sets this input at reset to a value determined by the contents of the FM security bytes.

7.2.3 Flash Lockout Recovery

If a user inadvertently enables Flash security on the device, a built-in lockout recovery mechanism can be used to reenable access to the device. This mechanism completely reases all on-chip Flash, thus disabling Flash security. Access to this recovery mechanism is built into CodeWarrior via an instruction in memory configuration (*.cfg*) files. Add, or uncomment the following configuration command:

unlock_flash_on_connect 1

For more information, please see **CodeWarrior MC56F83xx/DSP5685x Family Targeting Manual**.

The LOCKOUT_RECOVERY instruction has an associated 7-bit Data Register (DR) that is used to control the clock divider circuit within the FM module. This divider, FM_CLKDIV[6:0], is used to control the period of the clock used for timed events in the FM erase algorithm. This register must be set with appropriate values before the lockout sequence can begin. Refer to the **56F8300 Peripheral User Manual** for more details on setting this register value.

The value of the JTAG FM_CLKDIV[6:0] will replace the value of the FM register FMCLKD that divides down the system clock for timed events, as illustrated in **Figure 7-1**. FM_CLKDIV[6] will map to the PRDIV8 bit, and FM_CLKDIV[5:0] will map to the DIV[5:0] bits. The combination of PRDIV8 and DIV must divide the FM input clock down to a frequency of 150kHz-200kHz. The **"Writing the FMCLKD Register**" section in the Flash Memory chapter of the **56F8300 Peripheral User Manual** gives specific equations for calculating the correct values.

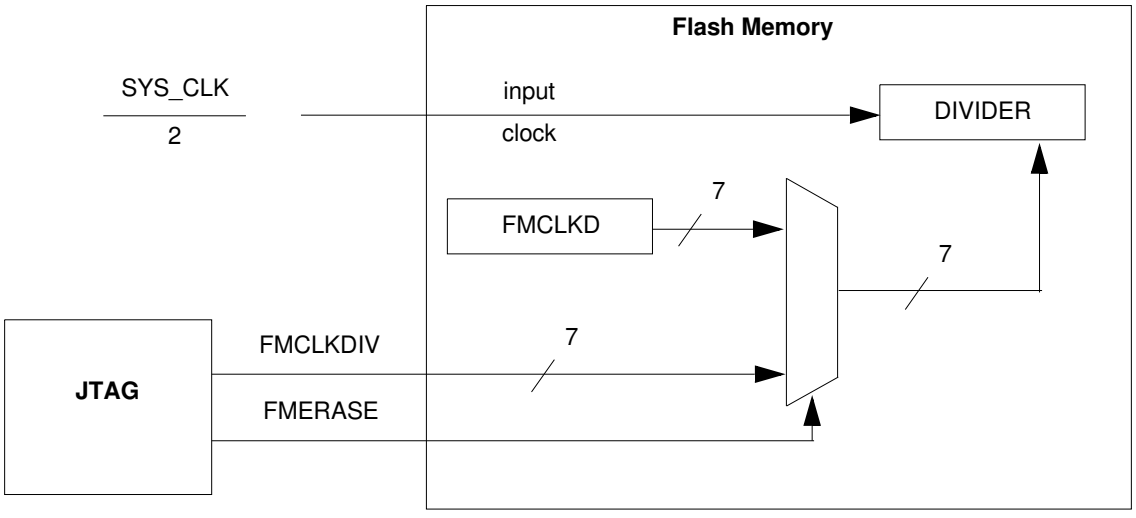


Figure 7-1 JTAG to FM Connection for Lockout Recovery

Two examples of FM_CLKDIV calculations follow.

EXAMPLE 1: If the system clock is the 8MHz crystal frequency because the PLL has not been set up, the input clock will be below 12.8MHz, so PRDIV8=FM_CLKDIV[6]=0. Using the following equation yields a DIV value of 19 for a clock of 200kHz, and a DIV value of 20 for a clock of 190kHz. This translates into an FM_CLKDIV[6:0] value of $13 or $14, respectively.

$$150[\text{kHz}] < \frac{\left(\frac{\text{SYS_CLK}}{(2)}\right)}{(\text{DIV} + 1)} < 200[\text{kHz}]$$

EXAMPLE 2: In this example, the system clock has been set up with a value of 32MHz, making the FM input clock 16MHz. Because that is greater than 12.8MHz, PRDIV8=FM_CLKDIV[6]=1.Using the following equation yields a DIV value of 9 for a clock of 200kHz, and a DIV value of 10 for a clock of 181kHz. This translates to an FM_CLKDIV[6:0] value of $49 or $4A, respectively.

$$150[\text{kHz}] < \frac{\left(\frac{\text{SYS_CLK}}{(2)(8)}\right)}{(\text{DIV} + 1)} < 200[\text{kHz}]$$

Once the LOCKOUT_RECOVERY instruction has been shifted into the instruction register, the clock divider value must be shifted into the corresponding 7-bit data register. After the data register has been updated, the user must transition the TAP controller into the RUN-TEST/IDLE state for the lockout sequence to commence. The controller must remain in this state until the erase sequence has completed. For details, see the JTAG Section in the **56F8300 Peripheral User Manual**.

Note: Once the lockout recovery sequence has completed, the user must reset both the JTAG TAP controller (by asserting $\overline{\text{TRST}}$) and the device (by asserting external chip reset) to return to normal unsecured operation.

7.2.4 Product Analysis

The recommended method of unsecuring a programmed device for product analysis of field failures is via the backdoor key access. The customer would need to supply Technical Support with the backdoor key and the protocol to access the backdoor routine in the Flash. Additionally, the KEYEN bit that allows backdoor key access must be set.

An alternative method for performing analysis on a secured microcontroller would be to mass-erase and reprogram the Flash with the original code, but modify the security bytes.

To insure that a customer does not inadvertently lock himself out of the device during programming, it is recommended that he program the backdoor access key first, his application code second and the security bytes within the FM configuration field last.

Part 8 General Purpose Input/Output (GPIO)

8.1 Introduction

This section is intended to supplement the GPIO information found in the **56F8300 Peripheral User Manual** and contains only chip-specific information. This information supercedes the generic information in the **56F8300 Peripheral User Manual**.

8.2 Configuration

There are three GPIO ports defined on the 56F8322/56F8122. The width of each port and the associated peripheral function is shown in **Table 8-1** and **Table 8-2**. The specific mapping of GPIO port pins is shown in **Table 8-3**.

Table 8-1 56F8322 GPIO Ports Configuration

GPIO Port	Port Width	Available Pins in 56F8322	Peripheral Function	Reset Function
A	12	7	PWM, SPI 1	PWM
B	8	8	SPI 0, DEC 0, TMRA, SCI 1	SPI 0, DEC 0
C	7	6	XTAL, EXTAL, CAN, TMRC, SCI 0	XTAL, EXTAL, CAN, TMRC

Table 8-2 56F8122 GPIO Ports Configuration

GPIO Port	Port Width	Available Pins in 56F8122	Peripheral Function	Reset Function
A	12	7	SPI 1	Must be reconfigured
B	8	8	SPI 0, SCI1, TMRA	SPI 0, other pins must be reconfigured
C	7	6	XTAL, EXTAL, TMRC, SCI 0	XTAL, EXTAL, TMRC; other pins must be reconfigured

Table 8-3 GPIO External Signals Map

Pins in shaded rows are not available in 56F8322 / 56F8122

Pins in italics are NOT available in the 56F8122 device

GPIO Function	Peripheral Function	Package Pin	Notes
GPIOA0	*PWMA0*	3	*PWM is NOT available in 56F8122*
GPIOA1	*PWMA1*	4	*PWM is NOT available in 56F8122*
GPIOA2	*PWMA2* / $\overline{SSI}$	6	SIM register SIM_GPS is used to select between SPI1 and PWMA on a pin-by-pin basis *PWM is NOT available in 56F8122*
GPIOA3	*PWMA3* / MISO1	7	SIM register SIM_GPS is used to select between SPI1 and PWMA on a pin-by-pin basis *PWM is NOT available in 56F8122*
GPIOA4	*PWMA4* / MOSI1	8	SIM register SIM_GPS is used to select between SPI1 and PWMA on a pin-by-pin basis *PWM is NOT available in 56F8122*
GPIOA5	*PWMA5* / SCLK1	9	SIM register SIM_GPS is used to select between SPI1 and PWMA on a pin-by-pin basis *PWM is NOT available in 56F8122*
GPIOA6	*FAULTA0*	12	
GPIOA7	FAULTA1		
GPIOA8	FAULTA2		
GPIOA9	ISA0		
GPIOA10	ISA1		
GPIOA11	ISA2		
GPIOB0	$\overline{SS0}$ / TXD1	15	SIM register SIM_GPS is used to select between SPI1 and PWMA on a pin-by-pin basis
GPIOB1	MISO0 / RXD1	16	SIM register SIM_GPS is used to select between SPI1 and PWMA on a pin-by-pin basis
GPIOB2	MOSI0	18	
GPIOB3	SCLK0	19	
GPIOB4	*HOME0* / TA3	35	Quad Decoder 0 register DECCR is used to select between Decoder 0 and Timer A *Quad Dec is NOT available in 56F8122*
GPIOB5	*INDEX0* / TA2	36	Quad Decoder 0 register DECCR is used to select between Decoder 0 and Timer A *Quad Dec is NOT available in 56F8122*
GPIOB6	*PHASEB0* / TA1	37	Quad Decoder 0 register DECCR is used to select between Decoder 0 and Timer A *Quad Dec is NOT available in 56F8122*

Table 8-3 GPIO External Signals Map (Continued)
Pins in shaded rows are not available in 56F8322 / 56F8122
Pins in italics are NOT available in the 56F8122 device

GPIO Function	Peripheral Function	Package Pin	Notes
GPIOB7	*PHASEA0* / TA0	38	Quad Decoder 0 register DECCR is used to select between Decoder 0 and Timer A *Quad Dec is NOT available in 56F8122*
GPIOC0	EXTAL	32	Pull-ups should default to disabled
GPIOC1	XTAL	33	Pull-ups should default to disabled
GPIOC2	*CAN_RX*	46	*CAN is NOT available in 56F8122*
GPIOC3	*CAN_TX*	47	*CAN is NOT available in 56F8122*
GPIOC4	TC3		
GPIOC5	TC1 / RXD0	48	SIM register SIM_GPS is used to select between Timer C and SCI0 on a pin-by-pin basis
GPIOC6	TC0 / TXD0	1	SIM register SIM_GPS is used to select between Timer C and SCI0 on a pin-by-pin basis

8.3 Memory Maps

The width of the GPIO port defines how many bits are implemented in each of the GPIO registers. Based on this and the default function of each of the GPIO pins, the reset values of the GPIOx_PUR and GPIOx_PER registers change from port to port. Tables **4-21** through **4-23** define the actual reset values of these registers.

Part 9 Joint Test Action Group (JTAG)

9.1 JTAG Information

Please contact your Freescale marketing representative or authorized distributor for device/package-specific BSDL information.

The $\overline{\text{TRST}}$ pin is not available in this package. The pin is tied to V_{DD} in the package.

The JTAG state machine is reset during POR and can also be reset via a soft reset by holding TMS high for five rising edges of TCK, as described in the **56F8300 Peripheral User Manual**.

Part 10 Specifications

10.1 General Characteristics

The 56F8322/56F8122 are fabricated in high-density CMOS with 5V-tolerant TTL-compatible digital inputs. The term “5V-tolerant” refers to the capability of an I/O pin, built on a 3.3V-compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V- and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during normal operation without causing damage). This 5V-tolerant capability therefore offers the power savings of 3.3V I/O levels combined with the ability to receive 5V levels without damage.

Absolute maximum ratings in **Table 10-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Note: All specifications meet both Automotive and Industrial requirements unless individual specifications are listed.

Note: *The 56F8122 device is guaranteed to 40MHz and specified to meet Industrial requirements only.*

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Note: *The 56F8122 device is specified to meet Industrial requirements only; PWM, CAN and Quad Decoder are NOT available on the 56F8122 device.*

Table 10-1 Absolute Maximum Ratings

(V_{SS} = V_{SSA_ADC} = 0)

Characteristic	Symbol	Notes	Min	Max	Unit
Supply voltage	V_{DD_IO}		- 0.3	4.0	V
ADC Supply Voltage	V_{DDA_ADC}, V_{REFH}	V_{REFH} must be less than or equal to V_{DDA_ADC}	- 0.3	4.0	V
Oscillator / PLL Supply Voltage	$V_{DDA_OSC_PLL}$		- 0.3	4.0	V
Internal Logic Core Supply Voltage	V_{DD_CORE}	OCR_DIS is High	- 0.3	3.0	V
Input Voltage (digital)	V_{IN}	Pin Groups 1, 3, 4, 5	-0.3	6.0	V
Input Voltage (analog)	V_{INA}	Pin Group 7	-0.3	4.0	V
Output Voltage	V_{OUT}	Pin Groups 1, 2, 3	-0.3	4.0 6.0[1]	V
Output Voltage (open drain)	V_{OD}	GPIO pins used in open drain mode	-0.3	6.0	V
Ambient Temperature (Automotive)	T_A		-40	125	°C
Ambient Temperature (Industrial)	T_A		-40	105	°C
Junction Temperature (Automotive)	T_J		-40	150	°C
Junction Temperature (Industrial)	T_J		-40	125	°C
Storage Temperature (Automotive)	T_{STG}		-55	150	°C
Storage Temperature (Industrial)	T_{STG}		-55	150	°C

1. If corresponding GPIO pin is configured as open drain.

Note: *Pins in italics are NOT available in the 56F8122 device.*

Pin Group 1: TC0-1, *FAULTA0*, $\overline{SS0}$, MISO0, MOSI0, SCLK0, *HOME0*, *INDEX0*, *PHASEA0*, *PHASEB0*, *CAN_RX*, *CAN_TX*

Pin Group 2: TDO

Pin Group 3: *PWMA0-5*

Pin Group 4: $\overline{RESET}$, TMS, TDI, $\overline{IRQA}$

Pin Group 5: TCK

Pin Group 6: XTAL, EXTAL

Pin Group 7: ANA0-6

Table 10-2 56F8322/56F8122 ElectroStatic Discharge (ESD) Protection

Characteristic	Min	Typ	Max	Unit
ESD for Human Body Model (HBM)	2000	—	—	V
ESD for Machine Model (MM)	200	—	—	V
ESD for Charge Device Model (CDM)	500	—	—	V

Table 10-3 Thermal Characteristics[6]

Characteristic	Comments	Symbol	Value	Unit	Notes
			48-pin LQFP		
Junction to ambient Natural Convection		$R_{\theta JA}$	41	°C/W	2
Junction to ambient (@1m/sec)		$R_{\theta JMA}$	34	°C/W	2
Junction to ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JMA}$ (2s2p)	34	°C/W	1,2
Junction to ambient (@1m/sec)	Four layer board (2s2p)	$R_{\theta JMA}$	29	°C/W	1,2
Junction to case		$R_{\theta JC}$	8	°C/W	3
Junction to center of case		Ψ_{JT}	2	°C/W	4, 5
I/O pin power dissipation		$P_{I/O}$	User-determined	W	
Power dissipation		P_D	$P_D = (I_{DD} \times V_{DD} + P_{I/O})$	W	
Maximum allowed P_D		P_{DMAX}	$(TJ - TA) / R\theta JA$[7]	W	

1. Theta-JA determined on 2s2p test boards is frequently lower than would be observed in an application. Determined on 2s2p thermal test board.
2. Junction to ambient thermal resistance, Theta-JA (R_{qJA}), was simulated to be equivalent to the JEDEC specification JESD51-2 in a horizontal configuration in natural convection. Theta-JA was also simulated on a thermal test board with two internal planes (2s2p, where “s” is the number of signal layers and “p” is the number of planes) per JESD51-6 and JESD51-7. The correct name for Theta-JA for forced convection or with the non-single layer boards is Theta-JMA.
3. Junction to case thermal resistance, Theta-JC (R_{qJC}), was simulated to be equivalent to the measured values using the cold plate technique with the cold plate temperature used as the "case" temperature. The basic cold plate measurement technique is described by MIL-STD 883D, Method 1012.1. This is the correct thermal metric to use to calculate thermal performance when the package is being used with a heat sink.
4. Thermal Characterization Parameter, Psi-JT (Y_{JT}), is the "resistance" from junction to reference point thermocouple on top center of case as defined in JESD51-2. Y_{JT} is a useful value to use to estimate junction temperature in steady-state customer environments.
5. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
6. See **Section 12.1** for more details on thermal design considerations.
7. TJ = Junction temperature
   TA = Ambient temperature

Note: *The 56F8122 device is guaranteed to 40MHz and specified to meet Industrial requirements only; PWM, CAN and Quad Decoder are NOT available on the 56F8122 device.*

Table 10-4 Recommended Operating Conditions

(V_{REFLO} = 0V, V_{SS} = V_{SSA_ADC} = 0V, V_{DDA} = V_{DDA_ADC} = $V_{DDA_OSC_PLL}$)

Characteristic	Symbol	Notes	Min	Typ	Max	Unit
Supply voltage	V_{DD_IO}		3	3.3	3.6	V
ADC Supply Voltage	V_{DDA_ADC}, V_{REFH}	V_{REFH} must be less than or equal to V_{DDA_ADC}	3	3.3	3.6	V
Oscillator / PLL Supply Voltage	$V_{DDA_OSC_PLL}$		3	3.3	3.6	V
Internal Logic Core Supply Voltage	V_{DD_CORE}	OCR_DIS is High	2.25	2.5	2.75	V
Device Clock Frequency	FSYSCLK		0	—	60/40	MHz
Input High Voltage (digital)	V_{IN}	Pin Groups 1, 3 ,4, 5	2	—	5.5	V
Input High Voltage (XTAL/EXTAL, XTAL is not driven by an external clock)	V_{IHC}	Pin Group 6	V_{DDA}-0.8	—	V_{DDA}+0.3	V
Input high voltage (XTAL/EXTAL, XTAL is driven by an external clock)	V_{IHC}	Pin Group 6	2	—	V_{DDA}+0.3	V
Input Low Voltage	V_{IL}	Pin Groups 1, 3, 4, 5, 6	-0.3	—	0.8	V
Output High Source Current V_{OH} = 2.4V (V_{OH} min.)	I_{OH}	Pin Groups 1, 2	—	—	-4	mA
		Pin Group 3	—	—	-12	
Output Low Sink Current V_{OL} = 0.4V (V_{OL} max)	I_{OL}	Pin Groups 1, 2	—	—	4	mA
		Pin Group 3	—	—	12	
Ambient Operating Temperature (Automotive)	T_A		-40	—	125	°C
Ambient Operating Temperature (Industrial)	T_A		-40	—	105	°C
Flash Endurance (Automotive) (Program Erase Cycles)	N_F	T_A = -40°C to 125°C	10,000	—	—	Cycles
Flash Endurance (Industrial) (Program Erase Cycles)	N_F	T_A = -40°C to 105°C	10,000	—	—	Cycles
Flash Data Retention	T_R	T_J <= 85°C avg	15	—	—	Years

Note: Total chip source or sink current cannot exceed 150mA.

Note: *Pins in italics are NOT available in the 56F8122 device.*

See Pin Groups in **Table 10-1**

10.2 DC Electrical Characteristics

Note: *The 56F8122 device is specified to meet Industrial requirements only; PWM, CAN and Quad Decoder are NOT available on the 56F8122 device.*

Table 10-5 DC Electrical Characteristics

At Recommended Operating Conditions; see Table 10-4

Characteristic	Symbol	Notes	Min	Typ	Max	Unit	Test Conditions
Output High Voltage	V_{OH}		2.4	—	—	V	$I_{OH} = I_{OHmax}$
Output Low Voltage	V_{OL}		—	—	0.4	V	$I_{OL} = I_{OLmax}$
Digital Input Current High pull-up enabled or disabled	I_{IH}	Pin Groups 1, 3, 4	—	0	+/- 2.5	µA	V_{IN} = 3.0V to 5.5V
Digital Input Current High with pull-down	I_{IH}	Pin Group 5	40	80	160	µA	V_{IN} = 3.0V to 5.5V
ADC Input Current High	I_{IHADC}	Pin Group 7	—	0	+/- 3.5	µA	$V_{IN} = V_{DDA}$
Digital Input Current Low pull-up enabled	I_{IL}	Pin Groups 1, 3, 4	-200	-100	-50	µA	V_{IN} = 0V
Digital Input Current Low pull-up disabled	I_{IL}	Pin Groups 1, 3, 4	—	0	+/- 2.5	µA	V_{IN} = 0V
Digital Input Current Low with pull-down	I_{IL}	Pin Group 5	—	0	+/- 2.5	µA	V_{IN} = 0V
ADC Input Current Low	I_{ILADC}	Pin Group 7	—	0	+/- 3.5	µA	V_{IN} = 0V
EXTAL Input Current Low clock input	I_{EXTAL}		—	0	+/- 2.5	µA	$V_{IN} = V_{DDA}$ or 0V
XTAL Input Current Low clock input	I_{XTAL}	CLKMODE = High	—	0	+/- 2.5	µA	$V_{IN} = V_{DDA}$ or 0V
		CLKMODE = Low	—	—	200	µA	$V_{IN} = V_{DDA}$ or 0V
Output Current High Impedance State	I_{OZ}	Pin Groups 1, 2, 3	—	0	+/- 2.5	µA	V_{OUT} = 3.0V to 5.5V or 0V
Schmitt Trigger Input Hysteresis	V_{HYS}	Pin Groups 1, 3, 4, 5	—	0.3	—	V	—
Input Capacitance (EXTAL/XTAL)	C_{INC}		—	4.5	—	pF	—
Output Capacitance (EXTAL/XTAL)	C_{OUTC}		—	5.5	—	pF	—
Input Capacitance	C_{IN}		—	6	—	pF	—
Output Capacitance	C_{OUT}		—	6	—	pF	—

See Pin Groups in Table 10-1

Table 10-6 Power-On Reset Low Voltage Parameters

Characteristic	Symbol	Min	Typ	Max	Units
POR Trip Point Rising[1]	POR_R	—	—	—	V
POR Trip Point Falling	POR_F	1.75	1.8	1.9	V
LVI, 2.5V Supply, trip point[2]	$V_{EI2.5}$	—	2.14	—	V
LVI, 3.3V supply, trip point[3]	$V_{EI3.3}$	—	2.7	—	V
Bias Current	I_{bias}	—	110	130	μA

1. Both $V_{EI2.5}$ and $V_{EI3.3}$ thresholds must be met for POR to be released on power-up.
2. When V_{DD_CORE} drops below $V_{EI2.5}$, an interrupt is generated.
3. When V_{DD_CORE} drops below $V_{EI3.3}$, an interrupt is generated.

Table 10-7 Current Consumption per Power Supply Pin (Typical)
On-Chip Regulator Enabled (OCR_DIS = Low)

Mode	I_{DD_IO}[1]	I_{DD_ADC}	$I_{DD_OSC_PLL}$	Test Conditions
RUN1_MAC	115mA	25mA	2.5mA	• 60MHz Device Clock • All peripheral clocks are enabled • Continuous MAC instructions with fetches from Data RAM • ADC powered on and clocked
Wait3	60mA	35μA	2.5mA	• 60MHz Device Clock • All peripheral clocks are enabled • ADC powered off
Stop1	5.7mA	0μA	360μA	• 4MHz Device Clock • All peripheral clocks are off • Relaxation oscillator is on • ADC powered off • PLL powered off
Stop2	5mA	0μA	145μA	• Relaxation oscillator is off • All peripheral clocks are off • ADC powered off • PLL powered off

1. No Output Switching (Output switching current can be estimated from I = CVf for each output)
2. Includes Processor Core current supplied by internal voltage regulator

Table 10-8 Current Consumption per Power Supply Pin (Typical)
On-Chip Regulator Disabled (OCR_DIS = High)

Mode	I_{DD_Core}	I_{DD_IO}[1]	I_{DD_ADC}	$I_{DD_OSC_PLL}$	Test Conditions
RUN1_MAC	110mA	13µA	25mA	2.5mA	• 60MHz Device Clock • All peripheral clocks are enabled • Continuous MAC instructions with fetches from Data RAM • ADC powered on and clocked
Wait3	55mA	13µA	35µA	2.5mA	• 60MHz Device Clock • All peripheral clocks are enabled • ADC powered off
Stop1	700µA	13µA	0µA	360µA	• 4MHz Device Clock • All peripheral clocks are off • Relaxation oscillator is on • ADC powered off • PLL powered off
Stop2	100µA	13µA	0µA	145µA	• Relaxation oscillator is off • All peripheral clocks are off • ADC powered off • PLL powered off

1. No Output Switching

10.2.1 Voltage Regulator Specifications

The 56F8322/56F8122 have two on-chip regulators. One supplies the PLL and has no external pins; therefore, it has no external characteristics which must be guaranteed (other than proper operation of the device). The second regulator supplies approximately 2.6V to the device's core logic. This regulator requires two external 2.2µF, or greater, capacitors for proper operation. Ceramic and tantalum capacitors tend to provide better performance tolerances. The output voltage can be measured directly on the V_{CAP} pins. The specifications for this regulator are shown in **Table 10-6**.

Table 10-9. Regulator Parameters

Characteristic	Symbol	Min	Typical	Max	Unit
Unloaded Output Voltage (0mA Load)	V_{RNL}	2.25	—	2.75	V
Loaded Output Voltage (200mA load)	V_{RL}	2.25	—	2.75	V
Line Regulation @ 200mA load (V_{DD}33 ranges from 3.0V to 3.6V)	V_R	2.25	—	2.75	V
Short Circuit Current (output shorted to ground)	Iss	—	—	700	mA
Bias Current	I_{bias}	—	5.8	7	mA
Power-down Current	I_{pd}	—	0	2	μA
Short-Circuit Tolerance (output shorted to ground)	T_{RSC}	—	—	30	minutes

Table 10-10. PLL Parameters

Characteristics	Symbol	Min	Typical	Max	Unit
PLL Start-up time	T_{PS}	0.3	0.5	10	ms
Resonator Start-up time	T_{RS}	0.1	0.18	1	ms
Min-Max Period Variation	T_{PV}	120	—	200	ps
Peak-to-Peak Jitter	T_{PJ}	—	—	175	ps
Bias Current	I_{BIAS}	—	1.5	2	mA
Quiescent Current, power-down mode	I_{PD}	—	100	150	μA

10.2.2 Temperature Sense

Note: *Temperature Sensor is NOT available in the 56F8122 device.*

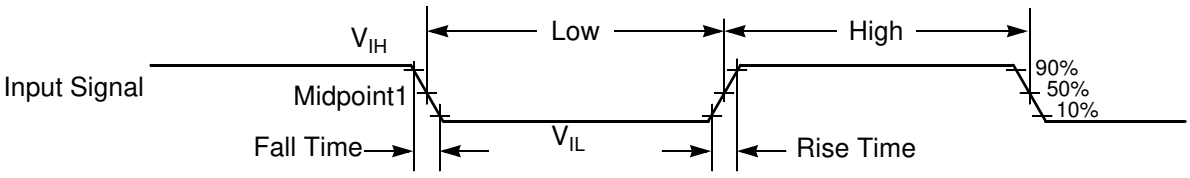
Table 10-11 Temperature Sense Parametrics

Characteristics	Symbol	Min	Typical	Max	Unit
Slope (Gain)[1]	m	—	7.762	—	mV/°C
Room Trim Temp. [1, 2]	T_{RT}	24	26	28	°C
Hot Trim Temp. (Industrial)[1,2]	T_{HT}	122	125	128	°C
Hot Trim Temp. (Automotive)[1,2]	T_{HT}	147	150	153	°C
Output Voltage @ V_{DDA_ADC} = 3.3V, T_J =0°C[1]	V_{TS0}	—	1.370	—	V
Supply Voltage	V_{DDA_ADC}	3.0	3.3	3.6	V
Supply Current - OFF	I_{DD-OFF}	—	—	10	µA
Supply Current - ON	I_{DD-ON}	—	—	250	µA
Accuracy[3,1] from -40°C to 150°C Using V_{TS} = mT + V_{TS0}	T_{ACC}	-6.7	0	6.7	°C
Resolution[4, 5,1]	R_{ES}	—	0.104	—	°C / bit

1. Includes the ADC conversion of the analog Temperature Sense voltage.
2. The ADC is not calibrated for the conversion of the Temperature Sensor trim value stored in the Flash Memory at FMOPT0 and FMOPT1.
3. See Application Note, AN1980, for methods to increase accuracy.
4. Assuming a 12-bit range from 0V to 3.3V.
5. Typical resolution calculated using equation, $R_{ES} = \frac{(V_{REFH} - V_{REFLO}) \times 1}{2^{12} \quad m}$

10.3 AC Electrical Characteristics

Tests are conducted using the input levels specified in **Table 10-5**. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in **Figure 10-1**.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 10-1 Input Signal Measurement References

Figure 10-2 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

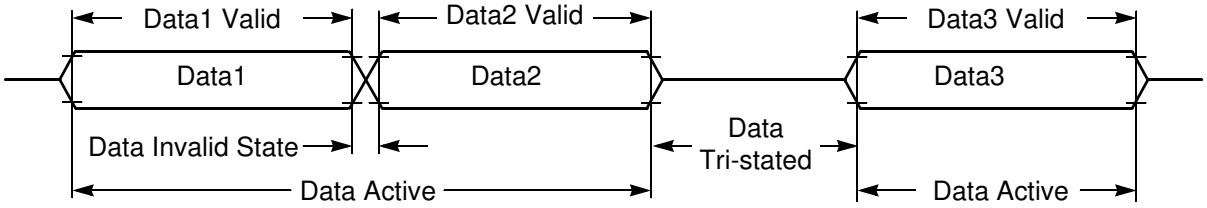


Figure 10-2 Signal States

10.4 Flash Memory Characteristics

Table 10-12 Flash Timing Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Program time[1]	Tprog	20	—	—	µs
Erase time[2]	Terase	20	—	—	ms
Mass erase time	Tme	100	—	—	ms

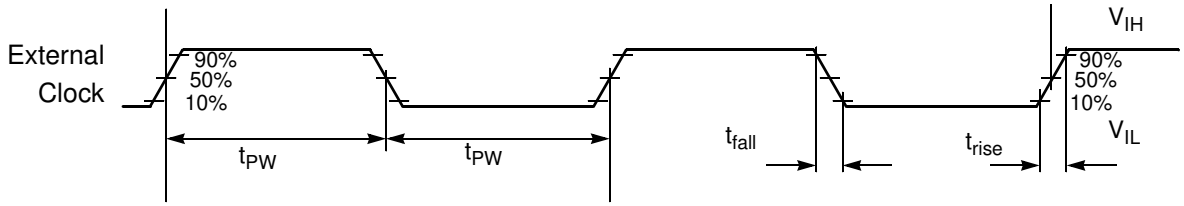
1. There is additional overhead which is part of the programming sequence. See the **56F8300 Peripheral User Manual** for details. Program time is per 16-bit word in Flash memory. Two words at a time can be programmed within the Program Flash module, as it contains two interleaved memories.
2. Specifies page erase time. There are 512 bytes per page in the Data and Boot Flash memories. The Program Flash module uses two interleaved Flash memories, increasing the effective page size to 1024 bytes.

10.5 External Clock Operation Timing

Table 10-13 External Clock Operation Timing Requirements[1]

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[2]—56F8322	f_{osc}	0	—	120	MHz
Frequency of operation (external clock driver)[2]—56F8122	f_{osc}	0	—	80	MHz
Clock Pulse Width[3]	t_{PW}	3.0	—	—	ns
External clock input rise time[4]	t_{rise}	—	—	15	ns
External clock input fall time[5]	t_{fall}	—	—	15	ns

1. Parameters listed are guaranteed by design.
2. See **Figure 10-3** for details on using the recommended connection of an external clock driver.
3. The high or low pulse width must be no smaller than 8.0ns or the chip will not function.
4. External clock input rise time is measured from 10% to 90%.
5. External clock input fall time is measured from 90% to 10%.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 10-3 External Clock Timing

10.6 Phase Locked Loop Timing

Table 10-14 PLL Timing

Characteristic	Symbol	Min	Typ	Max	Unit
External reference crystal frequency for the PLL[1]	f_{osc}	4	8	8.4	MHz
PLL output frequency[2] (f_{OUT})—56F8322	f_{op}	160	—	260	MHz
PLL output frequency[2] (f_{OUT})—56F8122	f_{op}	160	—	160	MHz
PLL stabilization time[3] -40° to +125°C	t_{plls}	—	1	10	ms

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8MHz input crystal.
2. ZCLK may not exceed 60MHz. For additional information on ZCLK and (f_{OUT}/2), please refer to the OCCS chapter in the **56F8300 Peripheral User Manual**.
3. This is the minimum time required after the PLL set up is changed to ensure reliable operation.

10.7 Oscillator Parameters

Table 10-15 Crystal Oscillator Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Crystal Start-up time	T_{CS}	4	5	10	ms
Resonator Start-up time	T_{RS}	0.1	0.18	1	ms
Crystal ESR	R_{ESR}	—	—	120	ohms
Crystal Peak-to-Peak Jitter	T_D	70	—	250	ps
Crystal Min-Max Period Variation	T_{PV}	0.12	—	1.5	ns
Resonator Peak-to-Peak Jitter	T_{RJ}	—	—	300	ps
Resonator Min-Max Period Variation	T_{RP}	—	—	300	ps
Bias Current, high-drive mode	I_{BIASH}	—	250	290	µA
Bias Current, low-drive mode	I_{BIASL}	—	80	110	µA
Quiescent Current, power-down mode	I_{PD}	—	0	1	µA

Table 10-16 Relaxation Oscillator Parameters

Characteristic	Min	Typ	Max	Units
Center Frequency	—	8	—	MHz
Minimum Tuning Step Size (See Note)	—	82	—	ps
Maximum Tuning Step Size (See Note)	—	41	—	ns
Frequency Accuracy -50°C to +150°C (See **Figure 10-4**)	—	+/- 1.78	+2 /-3	%
Maximum Cycle-to-Cycle Jitter	—	—	500	ps
Stabilization Time from Power-up	—	—	4	µs

Note: An LSB change in the tuning code results in an 82ps shift in the frequency period, while an MSB change in the tuning code results in a 41ns shift in the frequency period.

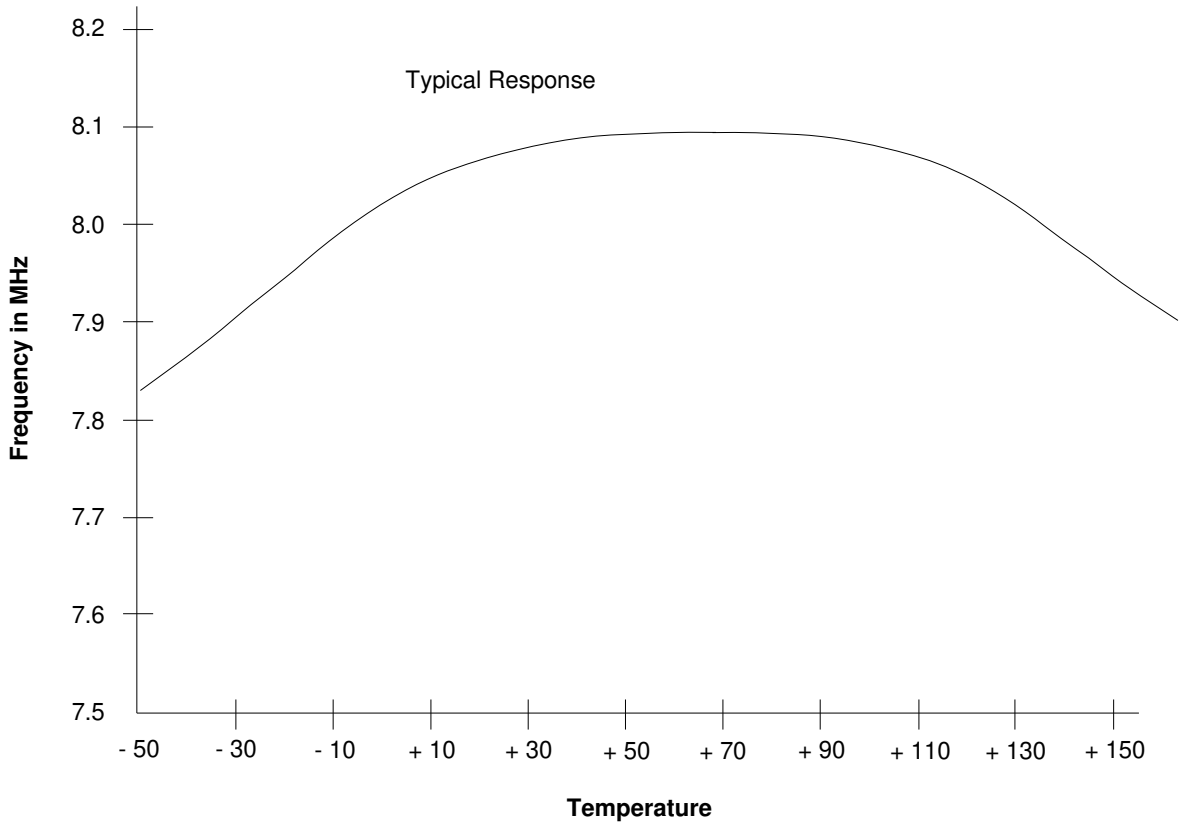


Figure 10-4 Frequency versus Temperature

10.8 Reset, Stop, Wait, Mode Select, and Interrupt Timing

Note: All address and data buses described here are internal.

Table 10-17 Reset, Stop, Wait, Mode Select, and Interrupt Timing[1,2]

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
Minimum $\overline{\text{RESET}}$ Assertion Duration	t_{RA}	16T	—	ns	10-5
Edge-sensitive Interrupt Request Width	t_{IRW}	1.5T	—	ns	10-6
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to General Purpose Output Valid, caused by first instruction execution in the interrupt service routine	t_{IG}	18T	—	ns	10-7
	$t_{IG - FAST}$	14T	—		
$\overline{\text{IRQA}}$ Width Assertion to Recover from Stop State[3]	t_{IW}	1.5T	—	ns	10-8

1. In the formulas, T = clock cycle. For an operating frequency of 60MHz, T = 16.67ns. At 8MHz (used during Reset and Stop modes), T = 125ns.
2. Parameters listed are guaranteed by design.
3. The interrupt instruction fetch is visible on the pins only in Mode 3.

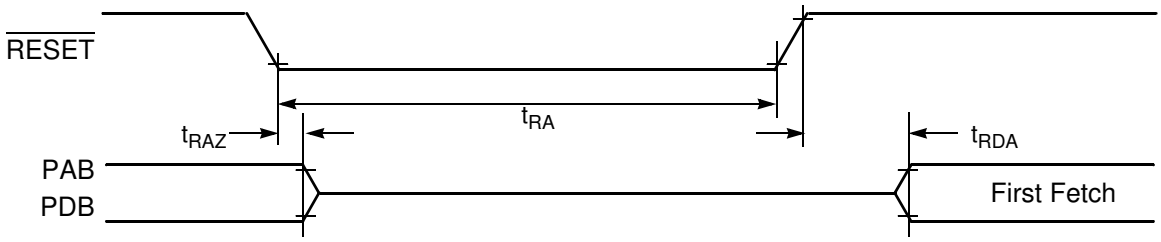


Figure 10-5 Asynchronous Reset Timing

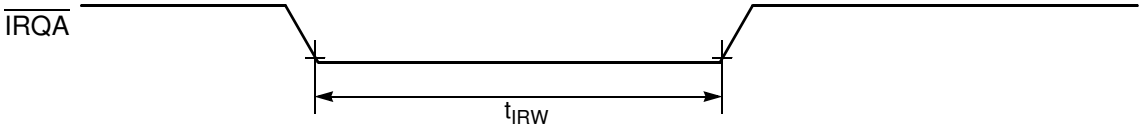


Figure 10-6 External Interrupt Timing (Negative Edge-Sensitive)

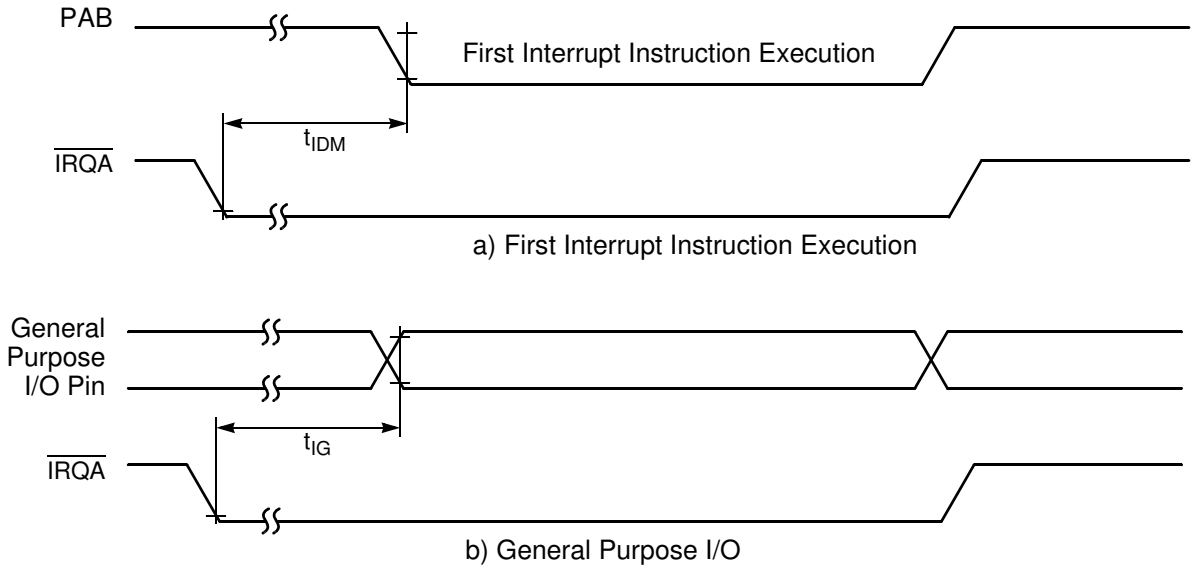


Figure 10-7 External Level-Sensitive Interrupt Timing

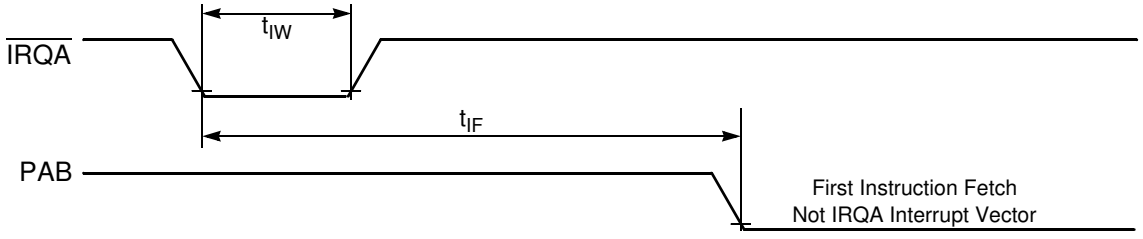


Figure 10-8 Recovery from Stop State Using Asynchronous Interrupt Timing

10.9 Serial Peripheral Interface (SPI) Timing

Table 10-18 SPI Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 50 50	 — —	 ns ns	10-9, 10-10, 10-11, 10-12
Enable lead time Master Slave	t_{ELD}	 — 25	 — —	 ns ns	10-12
Enable lag time Master Slave	t_{ELG}	 — 100	 — —	 ns ns	10-12
Clock (SCK) high time Master Slave	t_{CH}	 17.6 25	 — —	 ns ns	10-9, 10-10, 10-11, 10-12
Clock (SCK) low time Master Slave	t_{CL}	 16 16.67	 — —	 ns ns	10-12
Data set up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	10-9, 10-10, 10-11, 10-12
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	10-9, 10-10, 10-11, 10-12
Access time (time to data active from high-impedance state) Slave	t_A	4.8	15	ns	10-12
Disable time (hold time to high-impedance state) Slave	t_D	3.7	15.2	ns	10-12
Data Valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	10-9, 10-10, 10-11, 10-12
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	10-9, 10-10, 10-11, 10-12
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	10-9, 10-10, 10-11, 10-12
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	10-9, 10-10, 10-11, 10-12

1. Parameters listed are guaranteed by design.

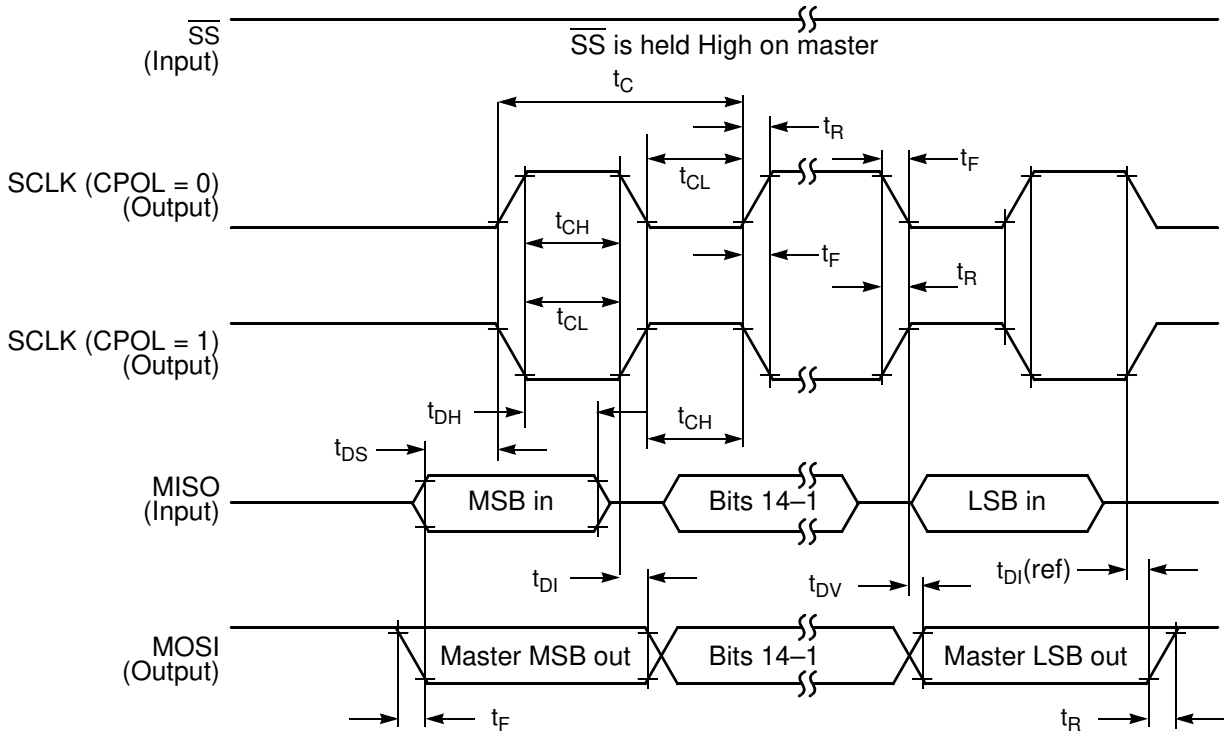


Figure 10-9 SPI Master Timing (CPHA = 0)

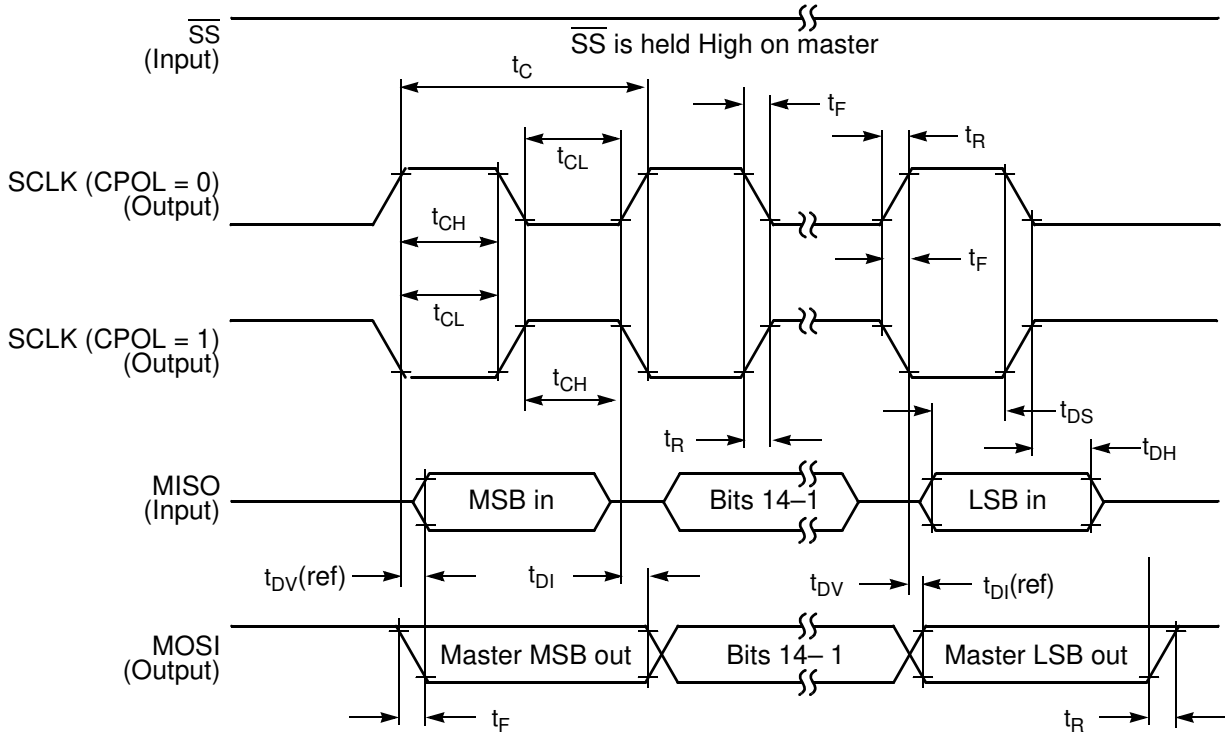


Figure 10-10 SPI Master Timing (CPHA = 1)

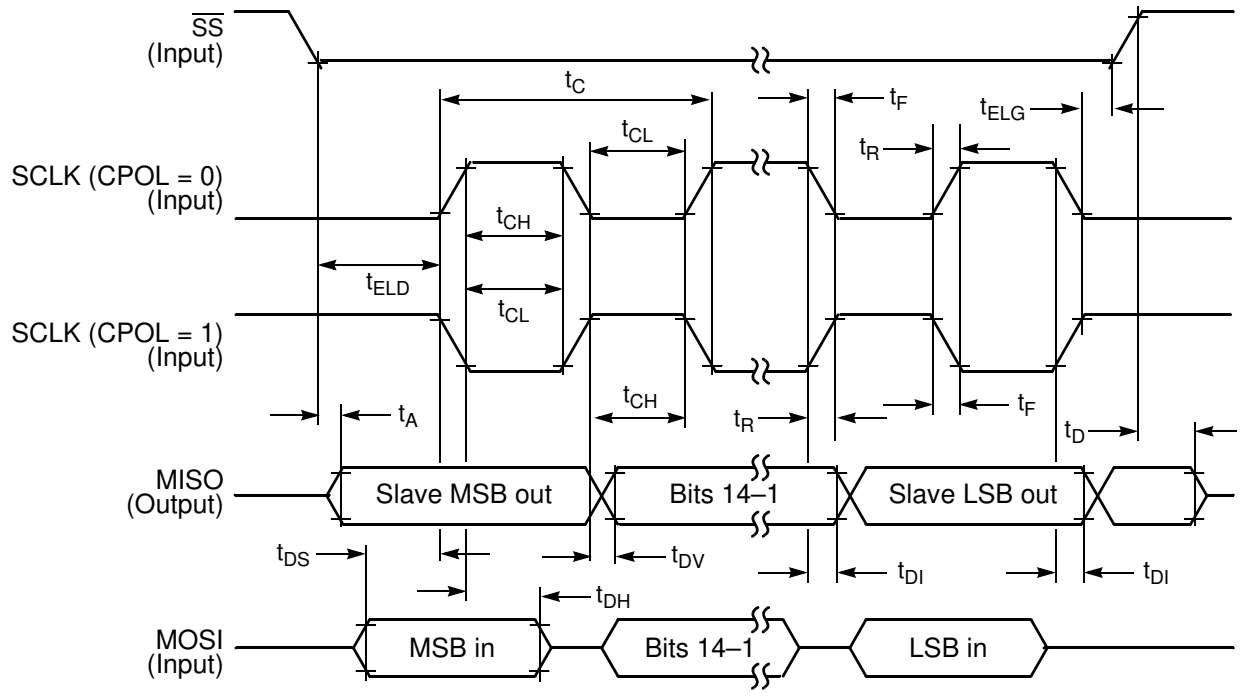


Figure 10-11 SPI Slave Timing (CPHA = 0)

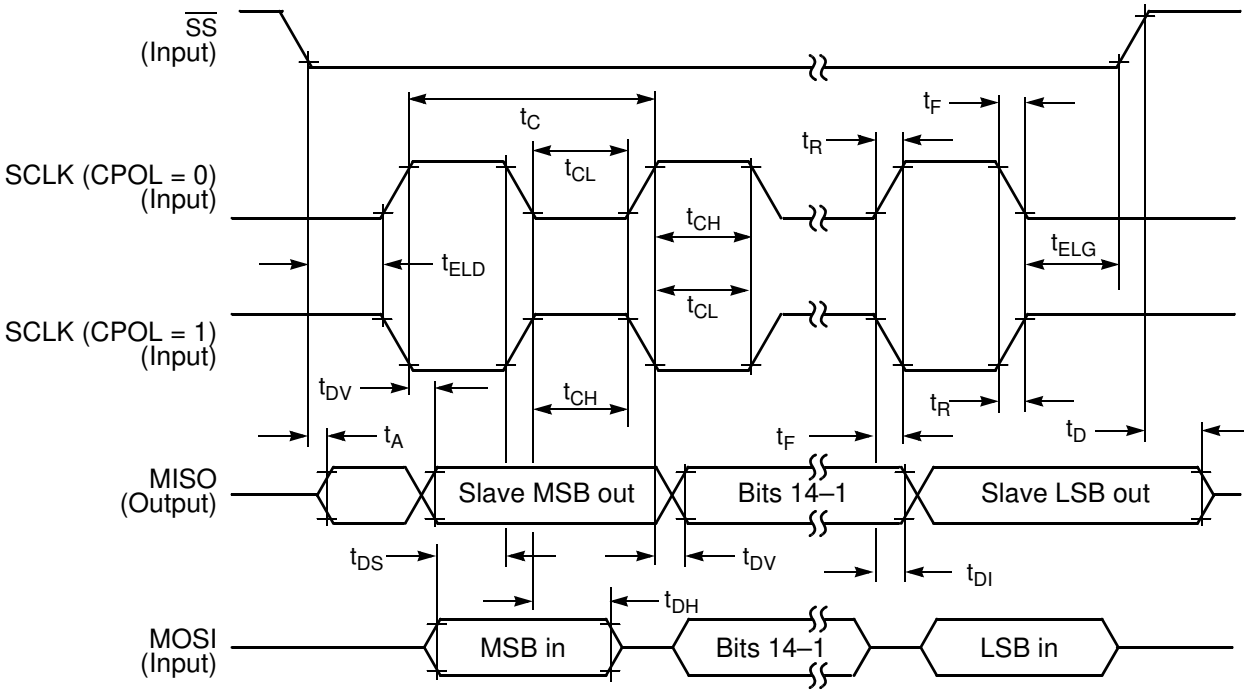


Figure 10-12 SPI Slave Timing (CPHA = 1)

10.10 Quad Timer Timing

Table 10-19 Timer Timing[1, 2]

Characteristic	Symbol	Min	Max	Unit	See Figure
Timer input period	P_{IN}	2T + 6	—	ns	10-13
Timer input high / low period	P_{INHL}	1T + 3	—	ns	10-13
Timer output period	P_{OUT}	1T - 3	—	ns	10-13
Timer output high / low period	P_{OUTHL}	0.5T - 3	—	ns	10-13

1. In the formulas listed, T = the clock cycle. For 60MHz operation, T = 16.67ns.
2. Parameters listed are guaranteed by design.

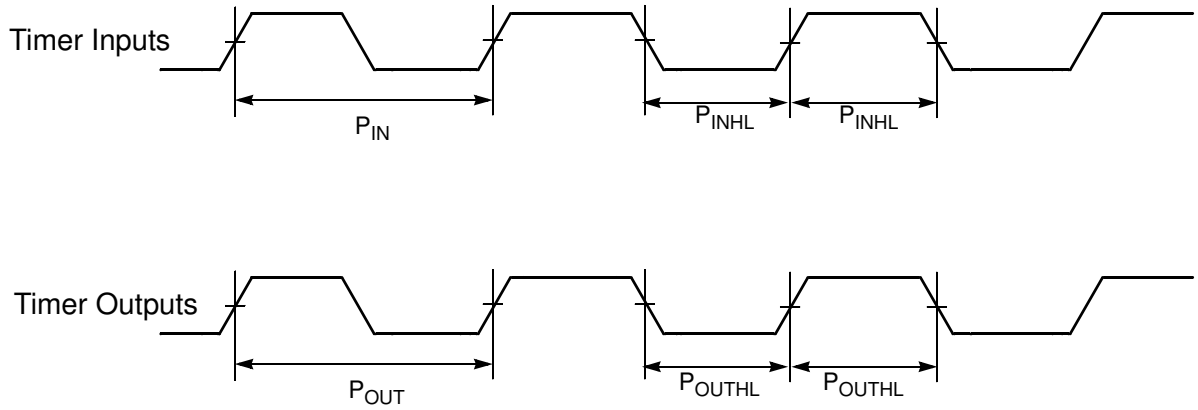


Figure 10-13 Timer Timing

10.11 Quadrature Decoder Timing

Note: *The Quadrature Decoder is NOT available in the 56F8122 device.*

Table 10-20 Quadrature Decoder Timing[1, 2]

Characteristic	Symbol	Min	Max	Unit	See Figure
Quadrature input period	P_{IN}	4T + 12	—	ns	10-14
Quadrature input high / low period	P_{HL}	2T + 6	—	ns	10-14
Quadrature phase period	P_{PH}	1T + 3	—	ns	10-14

1. In the formulas listed, T = the clock cycle. For 60MHz operation, T=16.67ns.
2. Parameters listed are guaranteed by design.

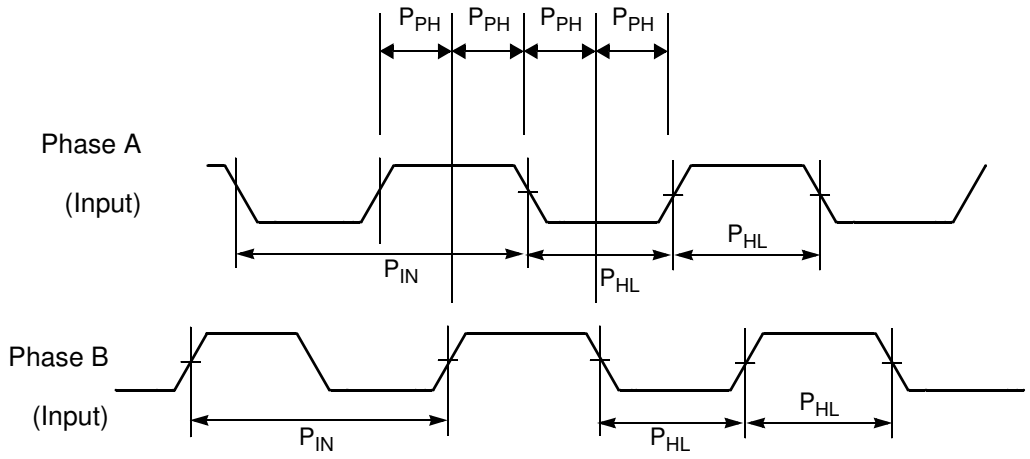


Figure 10-14 Quadrature Decoder Timing

10.12 Serial Communication Interface (SCI) Timing

Table 10-21 SCI Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Baud Rate[2]	BR	—	(f_{MAX}/16)	Mbps	—
RXD[3] Pulse Width	RXD_{PW}	0.965/BR	1.04/BR	ns	10-15
TXD[4] Pulse Width	TXD_{PW}	0.965/BR	1.04/BR	ns	10-16

1. Parameters listed are guaranteed by design.
2. f_{MAX} is the frequency of operation of the system clock in MHz, which is 60MHz for the 56F8322 device and 40MHz for the 56F8122 device.
3. The RXD pin in SCI0 is named RXD0 and the RXD pin in SCI1 is named RXD1.
4. The TXD pin in SCI0 is named TXD0 and the TXD pin in SCI1 is named TXD1.

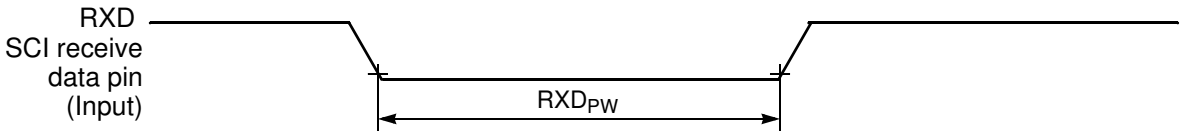


Figure 10-15 RXD Pulse Width

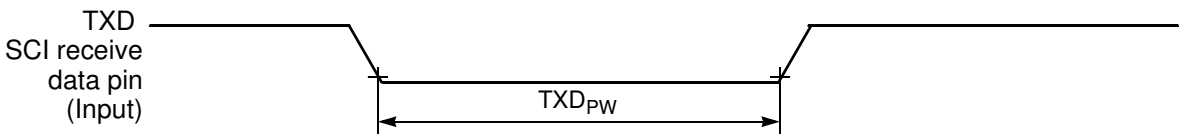


Figure 10-16 TXD Pulse Width

10.13 Controller Area Network (CAN) Timing

Note: *CAN is NOT available in the 56F8122 device.*

Table 10-22 CAN Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Baud Rate	BR_{CAN}	—	1	Mbps	—
Bus Wake-up detection	T_{WAKEUP}	T_{IPBUS}	—	µs	10-17

1. Parameters listed are guaranteed by design

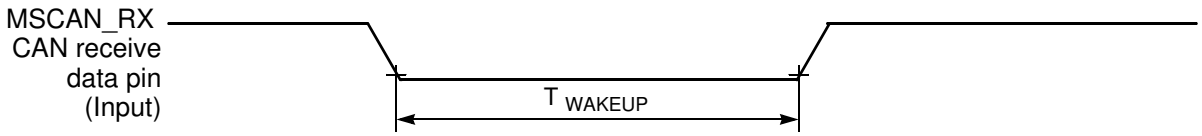


Figure 10-17 Bus Wakeup Detection

10.14 JTAG Timing

Table 10-23 JTAG Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation using EOnCE[1]	f_{OP}	DC	SYS_CLK/8	MHz	10-18
TCK frequency of operation not using EOnCE[1]	f_{OP}	DC	SYS_CLK/4	MHz	10-18
TCK clock pulse width	t_{PW}	50	—	ns	10-18
TMS, TDI data set-up time	t_{DS}	5	—	ns	10-19
TMS, TDI data hold time	t_{DH}	5	—	ns	10-19
TCK low to TDO data valid	t_{DV}	—	30	ns	10-19
TCK low to TDO tri-state	t_{TS}	—	30	ns	10-19

1. TCK frequency of operation must be less than 1/8 the processor rate.

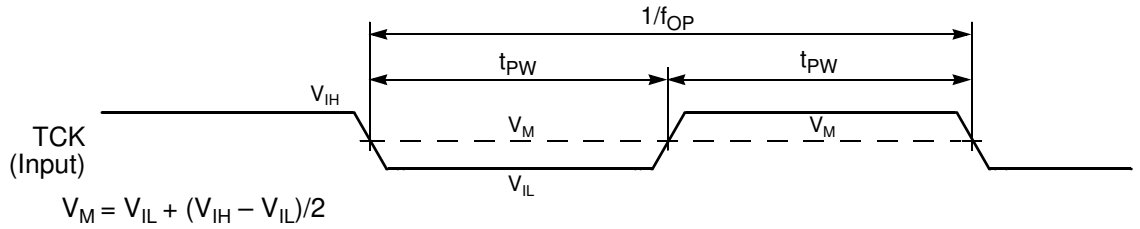


Figure 10-18 Test Clock Input Timing Diagram

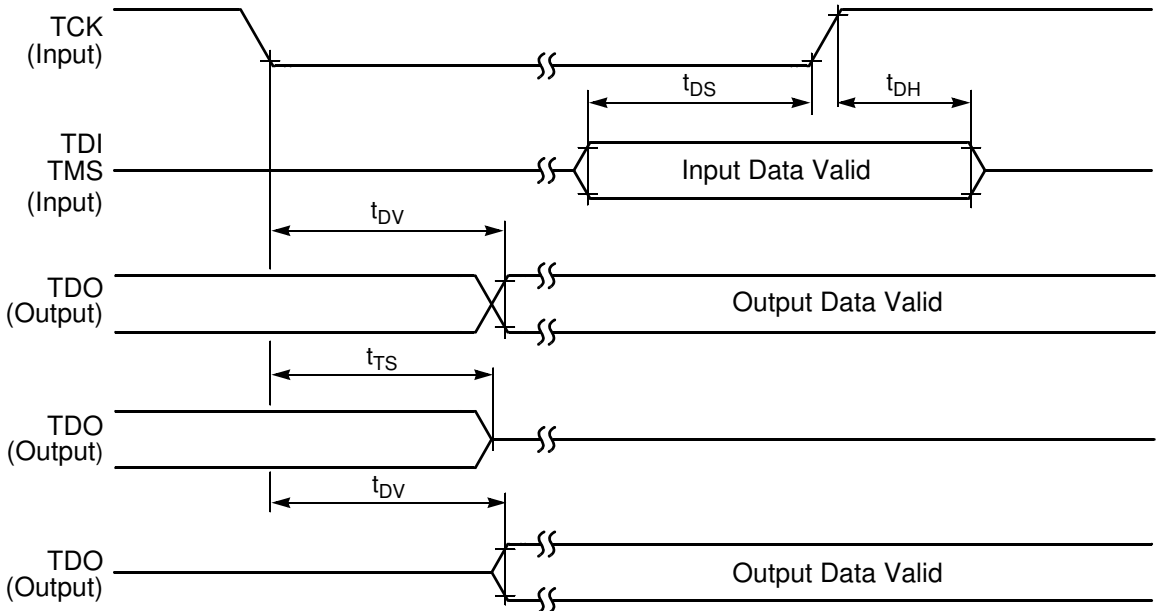


Figure 10-19 Test Access Port Timing Diagram

10.15 Analog-to-Digital Converter (ADC) Parameters

Table 10-24 ADC Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Input voltages	V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Resolution	R_{ES}	12	—	12	Bits
Integral Non-Linearity[1]	INL	—	+/- 2.4	+/- 3.2	LSB[2]
Differential Non-Linearity	DNL	—	+/- 0.7	< +1	LSB[2]
Monotonicity	GUARANTEED				
ADC internal clock	f_{ADIC}	0.5	—	5	MHz
Conversion range	R_{AD}	V_{REFL}	—	V_{REFH}	V

Table 10-24 ADC Parameters (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
ADC channel power-up time	t_{ADPU}	5	6	16	t_{AIC} cycles[3]
ADC reference circuit power-up time[4]	t_{VREF}	—	—	25	ms
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[3]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[3]
Input capacitance	C_{ADI}	—	5	—	pF
Input injection current[5], per pin	I_{ADI}	—	—	3	mA
Input injection current, total	I_{ADIT}	—	—	20	mA
V_{REFH} current	I_{VREFH}	—	1.2	3	mA
ADC A current	I_{ADCA}	—	25	—	mA
ADC B current	I_{ADCB}	—	25	—	mA
Quiescent current	I_{ADCQ}	—	0	10	μA
Uncalibrated Gain Error (ideal)	E_{GAIN}	—	+/- .004	+/- .01	—
Uncalibrated Offset Voltage	V_{OFFSET}	—	+/- 26	+/- 32	mV
Calibrated Absolute Error[6]	AE_{CAL}	—	See **Figure 10-20**	—	LSBs
Calibration Factor 1[7]	CF1	—	0.008597	—	—
Calibration Factor 2[7]	CF2	—	-2.8	—	—
Crosstalk between channels	—	—	-60	—	dB
Common Mode Voltage	V_{common}	—	$(V_{REFH} - V_{REFLO}) / 2$	—	V
Signal-to-noise ratio	SNR	—	64.6	—	db
Signal-to-noise plus distortion ratio	SINAD	—	59.1	—	db
Total Harmonic Distortion	THD	—	60.6	—	db
Spurious Free Dynamic Range	SFDR	—	61.1	—	db
Effective Number Of Bits[8]	ENOB	—	9.6	—	Bits

1. INL measured from $V_{in} = .1V_{REFH}$ to $V_{in} = .9V_{REFH}$ 10% to 90% Input Signal Range
2. LSB = Least Significant Bit
3. ADC clock cycles
4. Assumes each voltage reference pin is bypassed with 0.1μF ceramic capacitors to ground
5. The current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC. This allows the ADC to operate in noisy industrial environments where inductive flyback is possible.
6. Absolute error includes the effects of both gain error and offset error.
7. Please see the **56F8300 Peripheral User's Manual** for additional information on ADC calibration.
8. ENOB = (SINAD - 1.76)/6.02

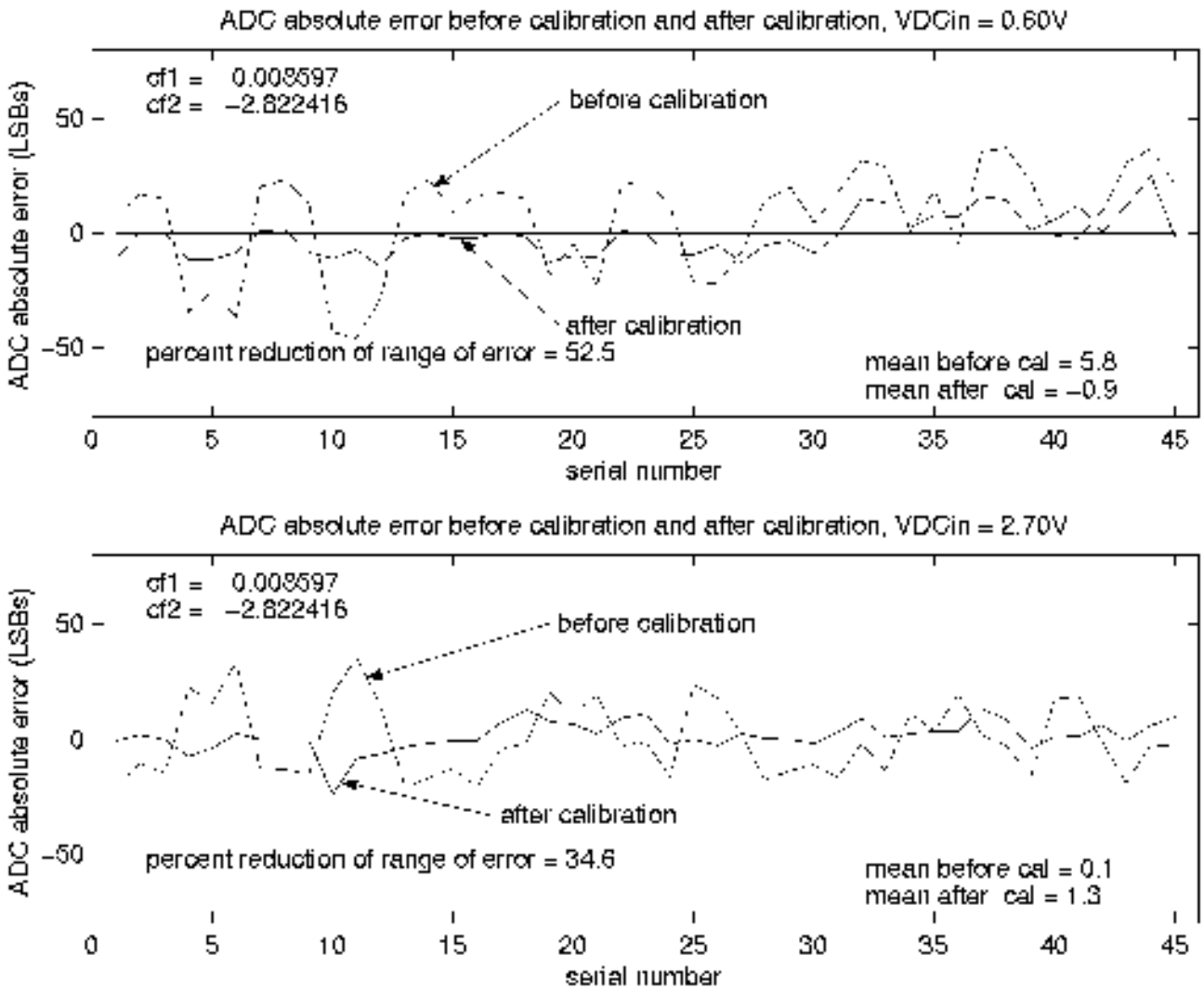


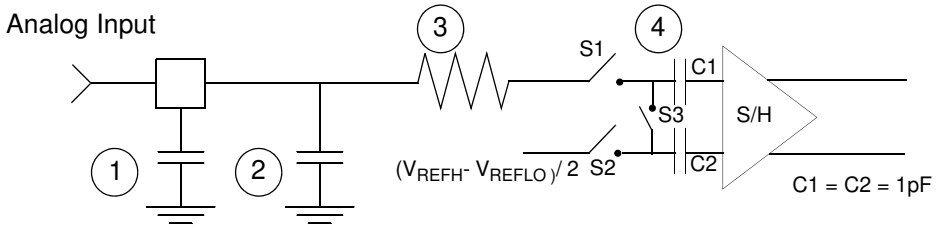
Figure 10-20 ADC Absolute Error Over Processing and Temperature Extremes Before and After Calibration for VDC_{in} = 0.60V and 2.70V

Note: The absolute error data shown in the graphs above reflects the effects of both gain error and offset error. The data was taken on 15 parts: three each from four processing corner lots as well as three from one nominally processed lot, each at three temperatures: -40°C, 27°C, and 150°C (giving the 45 data points shown above), for two input DC voltages: 0.60V and 2.70V. The data indicates that for the given population of parts, calibration significantly reduced (by as much as 34%) the collective variation (spread) of the absolute error of the population. It also significantly reduced (by as much as 80% when VDCin was 0.6V) the mean (average) of the absolute error and thereby brought it significantly closer to the ideal value of zero. Although not guaranteed, it is believed that calibration will produce results similar to those shown above for any population of parts, including those which represent processing and temperature extremes.

10.16 Equivalent Circuit for ADC Inputs

Figure 10-21 illustrates the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 closed & S3 open, one input of the sample and hold circuit moves to (V_{REFH}-V_{REFLO})/2, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about (V_{REFH}-V_{REFLO})/2. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). Note that there are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase.

One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, V_{REF} and the ADC clock frequency.



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8pf
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pf
3. Equivalent resistance for the ESD isolation resistor and the channel select mux; 500 ohms
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1pf

Figure 10-21 Equivalent Circuit for A/D Loading

10.17 Power Consumption

See Section 10.1 for a list of IDD requirements for the device. This section provides additional detail which can be used to optimize power consumption for a given application.

Power consumption is given by the following equation:

Total power = A: internal [static component]
+B: internal [state-dependent component]
+C: internal [dynamic component]
+D: external [dynamic component]
+E: external [static]

A, the internal [static component], is comprised of the DC bias currents for the oscillator, leakage currents, PLL, and voltage references. These sources operate independently of processor state or operating frequency.

B, the internal [state-dependent component], reflects the supply current required by certain on-chip resources only when those resources are in use. These include RAM, Flash memory and the ADCs.

C, the internal [dynamic component], is classic $C*V^2*F$ CMOS power dissipation corresponding to the 56800E core and standard cell logic.

D, the external [dynamic component], reflects power dissipated on-chip as a result of capacitive loading on the external pins of the chip. This is also commonly described as $C*V^2*F$, although simulations on two of the IO cell types used on the 56800E reveal that the power-versus-load curve does have a non-zero Y-intercept.

Note: V_{REFH} is tied to V_{DDA} and V_{REFLO} is tied to V_{SSA} inside this package.

Table 10-25 IO Loading Coefficients at 10MHz

	Intercept	Slope
PDU08DGZ_ME	1.3	0.11mW / pF
PDU04DGZ_ME	1.15mW	0.11mW / pF

Power due to capacitive loading on output pins is (first order) a function of the capacitive load and frequency at which the outputs change. Table 10-25 provides coefficients for calculating power dissipated in the IO cells as a function of capacitive load. In these cases:

$$TotalPower = \Sigma((\text{Intercept} + \text{Slope}*\text{Cload})*\text{frequency}/10\text{MHz})$$

where:

- Summation is performed over all output pins with capacitive loads
- TotalPower is expressed in mW
- Cload is expressed in pF

Because of the low duty cycle on most device pins, power dissipation due to capacitive loads was found to be fairly low when averaged over a period of time.

E, the external [static component], reflects the effects of placing resistive loads on the outputs of the device. Sum the total of all V^2/R or IV to arrive at the resistive load contribution to power. Assume V = 0.5 for the purposes of these rough calculations. For instance, if there is a total of eight PWM outputs driving 10mA into LEDs, then P = 8*.5*.01 = 40mW.

In previous discussions, power consumption due to parasitics associated with pure input pins is ignored, as it is assumed to be negligible.

Part 11 Packaging

11.1 56F8322 Package and Pin-Out Information

This section contains package and pin-out information for the 56F8322. This device comes in a 48-pin Low-profile Quad Flat Pack (LQFP). **Figure 11-1** shows the package outline for the 48-pin LQFP, **Figure 12-1** shows the mechanical parameters for this package, and **Table 11-1** lists the pin-out for the 48-pin LQFP.

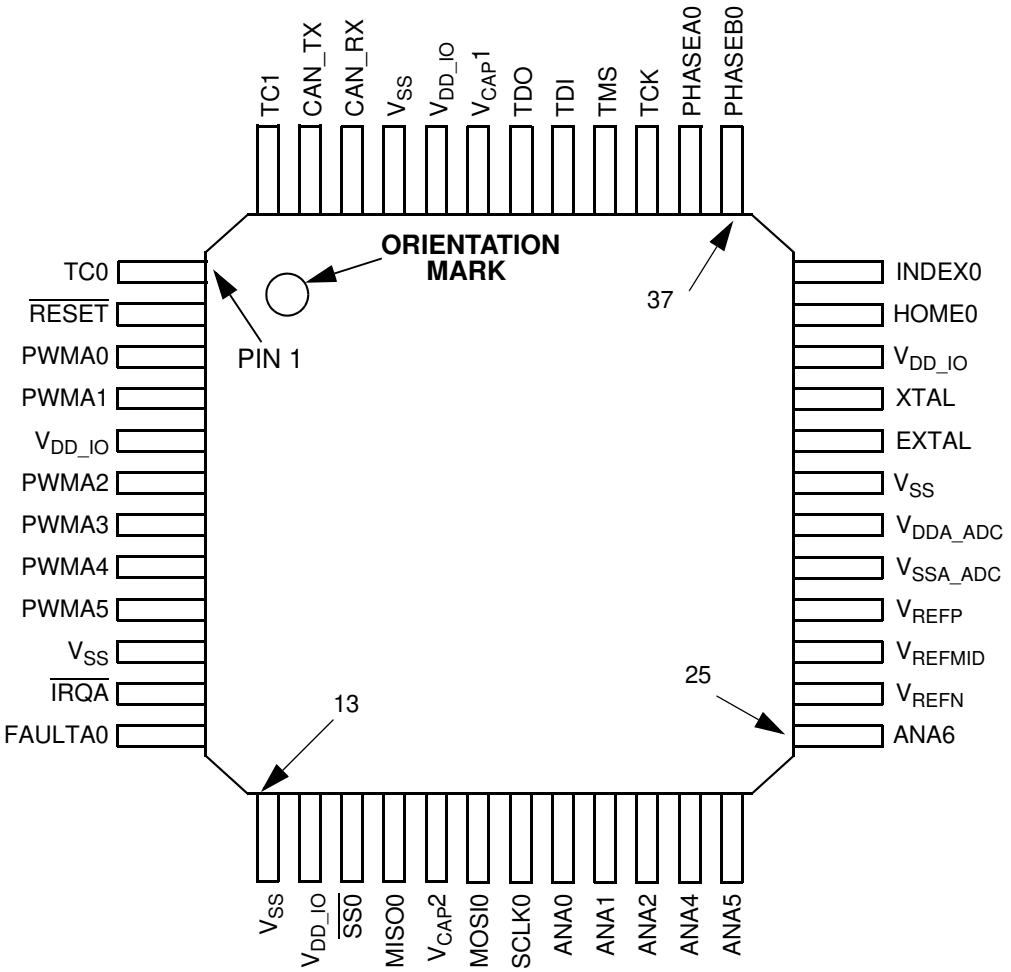


Figure 11-1 Top View, 56F8322 48-Pin LQFP Package

Table 11-1 56F8322 48-Pin LQFP Package Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	TC0	13	V_{SS}	25	ANA6	37	PHASEB
2	$\overline{\text{RESET}}$	14	V_{DD_IO}	26	V_{REFN}	38	PHASEA
3	PWMA0	15	$\overline{\text{SS0}}$	27	V_{REFMID}	39	TCK
4	PWMA1	16	MISO0	28	V_{REFP}	40	TMS
5	V_{DD_IO}	17	$V_{CAP}2$	29	V_{SSA_ADC}	41	TDI
6	PWMA2	18	MOSI0	30	V_{DDA_ADC}	42	TDO
7	PWMA3	19	SCLK0	31	V_{SS}	43	$V_{CAP}1$
8	PWMA4	20	ANA0	32	EXTAL	44	V_{DD_IO}
9	PWMA5	21	ANA1	33	XTAL	45	V_{SS}
10	V_{SS}	22	ANA2	34	V_{DD_IO}	46	CAN_RX
11	$\overline{\text{IRQA}}$	23	ANA4	35	HOME0	47	CAN_TX
12	FAULTA0	24	ANA5	36	INDEX0	48	TC1

11.2 56F8122 Package and Pin-Out Information

This section contains package and pin-out information for the 56F8122. This device comes in a 48-pin Low-profile Quad Flat Pack (LQFP). **Figure 11-1** shows the package outline for the 48-pin LQFP, **Figure 12-1** shows the mechanical parameters for this package, and **Table 11-1** lists the pin-out for the 48-pin LQFP.

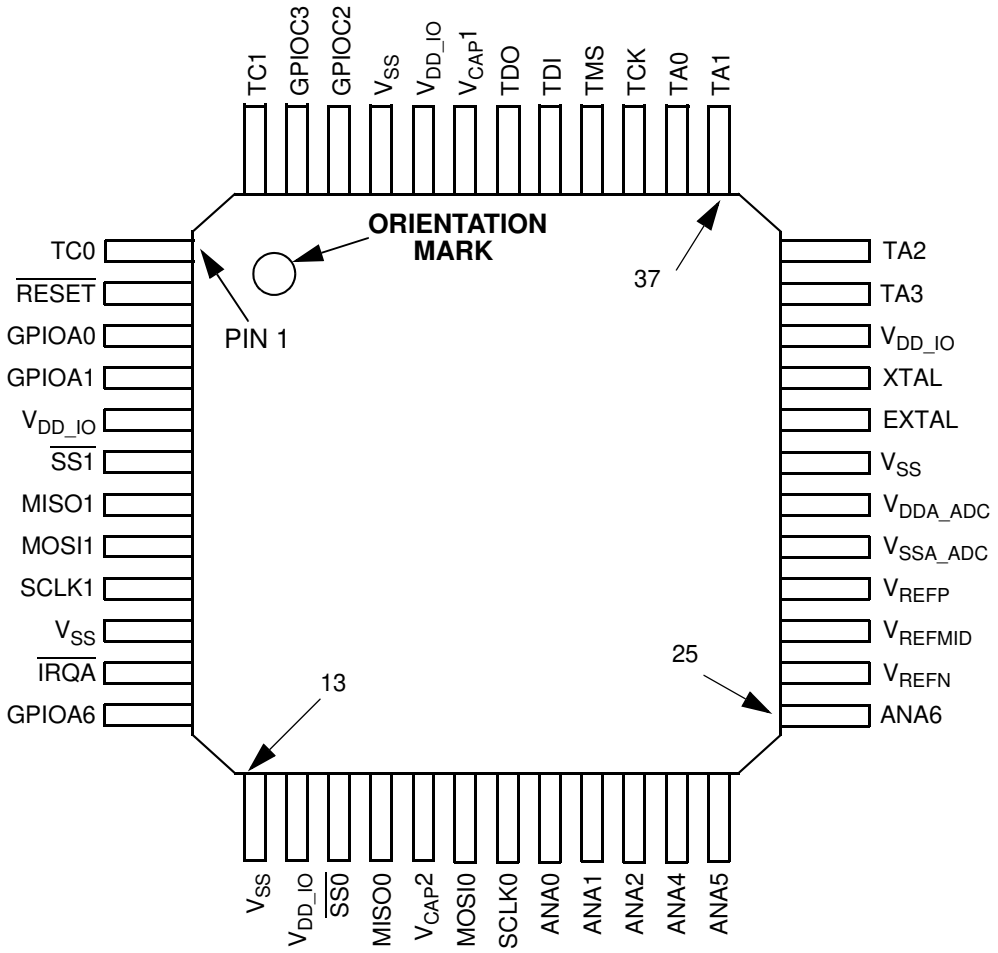
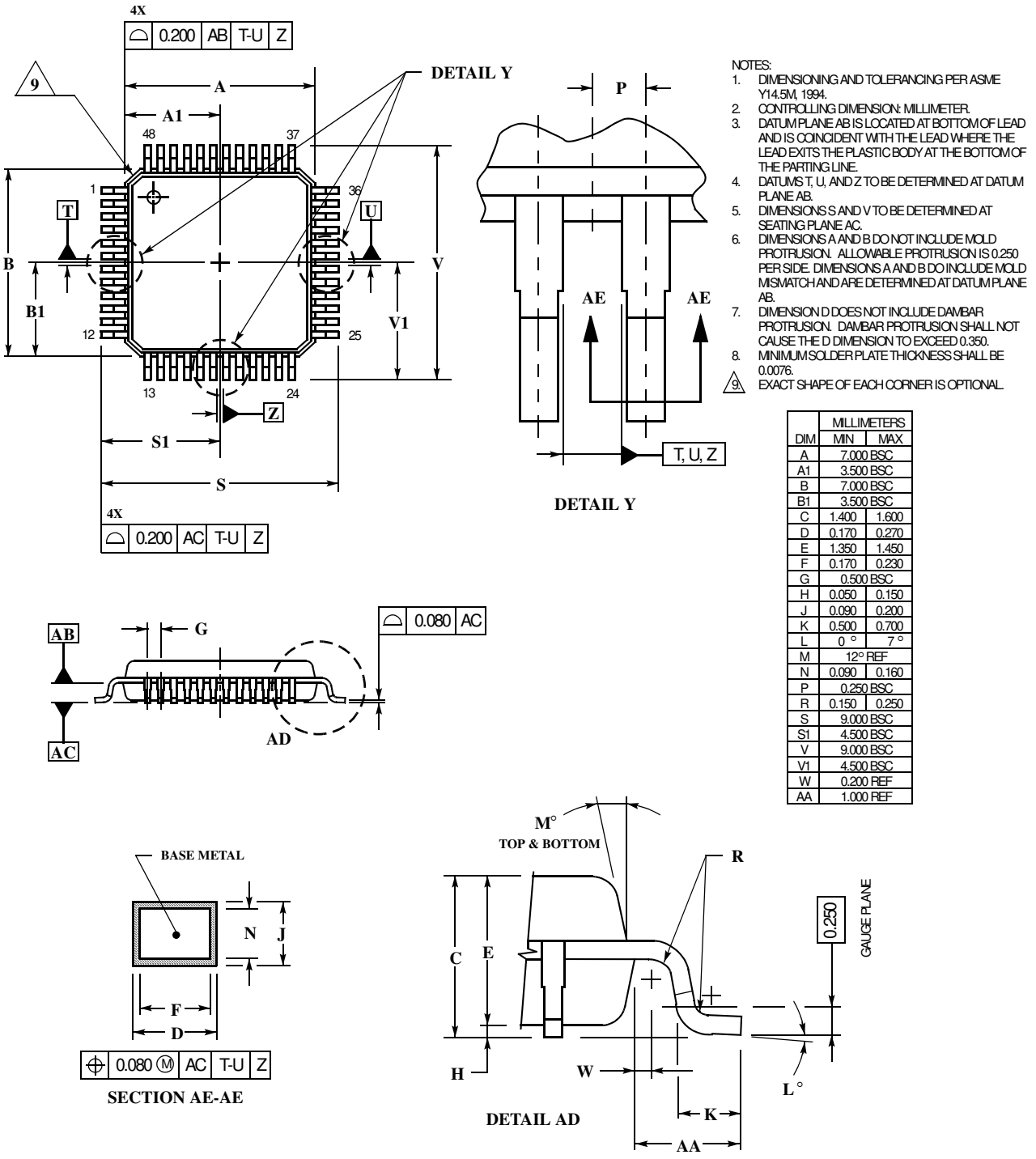


Figure 11-2 Top View, 56F8122 48-Pin LQFP Package

Table 11-2 56F8122 48-Pin LQFP Package Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	TC0	13	V_{SS}	25	ANA6	37	TA1
2	$\overline{\text{RESET}}$	14	V_{DD_IO}	26	V_{REFN}	38	TA0
3	GPIOA0	15	$\overline{\text{SS0}}$	27	V_{REFMID}	39	TCK
4	GPIOA1	16	MISO0	28	V_{REFP}	40	TMS
5	V_{DD_IO}	17	$V_{CAP}2$	29	V_{SSA_ADC}	41	TDI
6	$\overline{\text{SS1}}$	18	MOSI0	30	V_{DDA_ADC}	42	TDO
7	MISO1	19	SCLK0	31	V_{SS}	43	$V_{CAP}1$
8	MOSI1	20	ANA0	32	EXTAL	44	V_{DD_IO}
9	SCLK1	21	ANA1	33	XTAL	45	V_{SS}
10	V_{SS}	22	ANA2	34	V_{DD_IO}	46	GPIOC2
11	$\overline{\text{IRQA}}$	23	ANA4	35	TA3	47	GPIOC3
12	GPIOA6	24	ANA5	36	TA2	48	TC1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS	
DIM	MIN	MAX
A	7.000 BSC	
A1	3.500 BSC	
B	7.000 BSC	
B1	3.500 BSC	
C	1.400	1.600
D	0.170	0.270
E	1.350	1.450
F	0.170	0.230
G	0.500 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
L	0 °	7 °
M	12° REF	
N	0.090	0.160
P	0.250 BSC	
R	0.150	0.250
S	9.000 BSC	
S1	4.500 BSC	
V	9.000 BSC	
V1	4.500 BSC	
W	0.200 REF	
AA	1.000 REF	

Figure 11-3 48-Pin LQFP Mechanical Information

Please see **www.freescale.com** for the most current case outline.

Part 12 Design Considerations

12.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$T_J = T_A + (R_{\theta JA} \times P_D)$

where:

T_A = Ambient temperature for the package (^oC)
$R_{\theta JA}$ = Junction to ambient thermal resistance ($^oC/W$)
P_D = Power dissipation in the package (W)

The junction to ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low-power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

$R_{\theta JA}$ = Package junction to ambient thermal resistance °C/W
$R_{\theta JC}$ = Package junction to case thermal resistance °C/W
$R_{\theta CA}$ = Package case to ambient thermal resistance °C/W

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T = Thermocouple temperature on top of package (^oC)
Ψ_{JT} = Thermal characterization parameter (^oC)/W
P_D = Power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

12.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the 56F8322/56F8122:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the device and from the board ground to each V_{SS} (GND) pin
- The minimum bypass requirement is to place six 0.01–0.1µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including $V_{DDA}/V_{SSA.}$ Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are less than 0.5 inch per capacitor lead
- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for V_{DD} and V_{SS}
- Bypass the V_{DD} and V_{SS} layers of the PCB with approximately 100µF, preferably with a high-grade capacitor such as a tantalum capacitor
- Because the device's output signals have fast rise and fall times, PCB trace lengths should be minimal

- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF}, V_{DDA} and V_{SSA} pins
- Because the Flash memory is programmed through the JTAG/EOnCE port, the designer should provide an interface to this port to allow in-circuit Flash programming

12.3 Power Distribution and I/O Ring Implementation

Figure 12-1 illustrates the general power control incorporated in the 56F8322/56F8122. This chip contains two internal power regulators. One of them is powered from the $V_{DDA_OSC_PLL}$ pin and cannot be turned off. This regulator controls power to the internal clock generation circuitry. The other regulator is powered from the V_{DD_IO} pins and provides power to all of the internal digital logic of the core, all peripherals and the internal memories. This regulator can be turned off, if an external V_{DD_CORE} voltage is externally applied to the V_{CAP} pins.

In summary, the entire chip can be supplied from a single 3.3 volt supply if the large core regulator is enabled. If the regulator is not enabled, a dual supply 3.3V/2.5V configuration can also be used.

Notes:

- Flash, RAM and internal logic are powered from the core regulator output
- $V_{PP}1$ and $V_{PP}2$ are not connected in the customer system
- All circuitry, analog *and* digital, shares a common V_{SS} bus

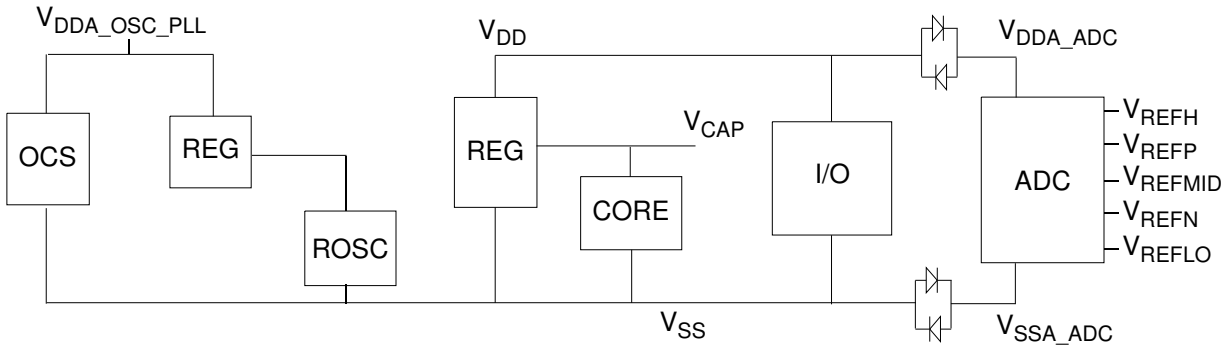


Figure 12-1 Power Management

Part 13 Ordering Information

Table 13-1 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 13-1 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Temperature Range	Order Number
MC56F8322	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	48	60	-40° to + 105° C	MC56F8322VFA60
MC56F8322	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	48	60	-40° to + 125° C	MC56F8322MFA60
MC56F8122	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	48	40	-40° to + 105° C	MC56F8122VFA
MC56F8322	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	48	60	-40° to + 105° C	MC56F8322VFAE*
MC56F8322	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	48	60	-40° to + 125° C	MC56F8322MFAE*
MC56F8122	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	48	40	-40° to + 105° C	MC56F8122VFAE*

*This part is RoHS compliant.

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