# MC74HC175A

# Quad D Flip-Flop with Common Clock and Reset

## High−Performance Silicon−Gate CMOS

The MC74HC175A is identical in pinout to the LS175. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of four D flip−flops with common Reset and Clock inputs, and separate D inputs. Reset (active−low) is asynchronous and occurs when a low level is applied to the Reset input. Information at a D input is transferred to the corresponding Q output on the next positive going edge of the Clock input.

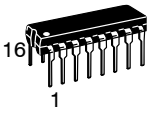
### Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity 166 FETs or 41.5 Equivalent Gates
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

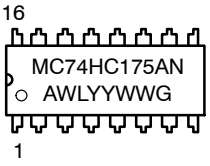
**ON Semiconductor®**

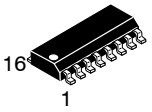
**http://onsemi.com**

**MARKING DIAGRAMS**



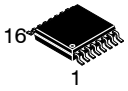

**PDIP−16**
**N SUFFIX**
**CASE 648**



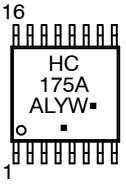



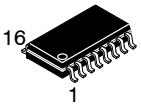

**SOIC−16**
**D SUFFIX**
**CASE 751B**



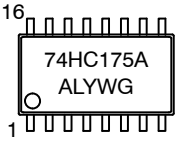




**TSSOP−16**
**DT SUFFIX**
**CASE 948F**




**SOEIAJ−16**
**F SUFFIX**
**CASE 966**




| | | |
|---|---|---|
| A | = | Assembly Location |
| L, WL | = | Wafer Lot |
| Y, YY | = | Year |
| W, WW | = | Work Week |
| G or ▪ | = | Pb−Free Package |

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

© Semiconductor Components Industries, LLC, 2011

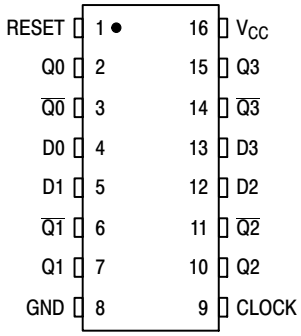



**Figure 1. Pin Assignment**

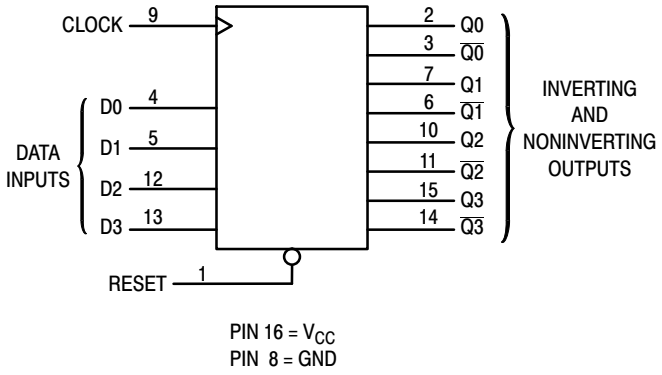



**Figure 2. Logic Diagram**

**FUNCTION TABLE**

| Inputs | | | Outputs | |
|---|---|---|---|---|
| **Reset** | **Clock** | **D** | **Q** | **$\overline{Q}$** |
| L | X | X | L | H |
| H | ↗ | H | H | L |
| H | ↗ | L | L | H |
| H | L | X | No Change | |

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| MC74HC175ANG | PDIP−16 | 500 Units / Rail |
| MC74HC175ADG | SOIC−16 (Pb−Free) | 48 Units / Rail |
| MC74HC175ADR2G | SOIC−16 (Pb−Free) | 2500 Units / Reel |
| MC74HC175ADTR2G | TSSOP−16* | 2500 Units / Reel |
| MC74HC175AFELG | SOEIAJ−16 (Pb−Free) | 2000 Units / Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

## MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | – 0.5 to + 7.0 | V |
| $V_{in}$ | DC Input Voltage (Referenced to GND) | – 0.5 to $V_{CC}$ + 0.5 | V |
| $V_{out}$ | DC Output Voltage (Referenced to GND) | – 0.5 to $V_{CC}$ + 0.5 | V |
| $I_{in}$ | DC Input Current, per Pin | ± 20 | mA |
| $I_{out}$ | DC Output Current, per Pin | ± 25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ± 50 | mA |
| $P_D$ | Power Dissipation in Still Air, Plastic DIP†<br>SOIC Package†<br>TSSOP Package† | 750<br>500<br>450 | mW |
| $T_{stg}$ | Storage Temperature | – 65 to + 150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package) | 260 | °C |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | | 2.0 | 6.0 | V |
| $V_{in}$, $V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | | – 55 | + 125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time (Figure 1) | $V_{CC}$ = 2.0 V<br>$V_{CC}$ = 3.0 V<br>$V_{CC}$ = 4.5 V<br>$V_{CC}$ = 6.0 V | 0<br>0<br>0 | 1000<br>600<br>500<br>400 | ns |

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $V_{IH}$ | Minimum High–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ – 0.1 V<br>$\|I_{out}\|$ ≤ 20 μA | 2.0<br>3.0<br>4.5<br>6.0 | 1.5<br>2.1<br>3.15<br>4.2 | 1.5<br>2.1<br>3.15<br>4.2 | 1.5<br>2.1<br>3.15<br>4 2 | V |
| $V_{IL}$ | Maximum Low–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ – 0.1 V<br>$\|I_{out}\|$ ≤ 20 μA | 2.0<br>3.0<br>4.5<br>6.0 | 0.5<br>0.9<br>1.35<br>1.80 | 0.5<br>0.9<br>1.35<br>1.80 | 0.5<br>0.9<br>1.35<br>1.80 | V |
| $V_{OH}$ | Minimum High–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\|$ ≤ 20 μA | 2.0<br>4.5<br>6.0 | 1.9<br>4.4<br>5.9 | 1.9<br>4.4<br>5.9 | 1.9<br>4.4<br>5.9 | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$ $\|I_{out}\|$ ≤ 2.4 mA<br>$\|I_{out}\|$ ≤ 4.0 mA<br>$\|I_{out}\|$ ≤ 5.2 mA | 3.0<br>4.5<br>6.0 | 2.48<br>3.98<br>5.48 | 2.34<br>3.84<br>5.34 | 2.20<br>3.70<br>5.20 | |

**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $V_{OL}$ | Maximum Low–Level Output Voltage | $V_{in} = V_{IH}$ or $V_{IL}$<br>$\|I_{out}\| \leq 20$ μA | 2.0<br>4.5<br>6.0 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | V |
| | | $V_{in} = V_{IH}$ or $V_{IL}$ $\|I_{out}\| \leq 2.4$ mA<br>$\|I_{out}\| \leq 4.0$ mA<br>$\|I_{out}\| \leq 5.2$ mA | 3.0<br>4.5<br>6.0 | 0.26<br>0.26<br>0.26 | 0.33<br>0.33<br>0.33 | 0.40<br>0.40<br>0.40 | |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in} = V_{CC}$ or GND | 6.0 | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in} = V_{CC}$ or GND<br>$I_{out} = 0$ μA | 6.0 | 4 | 40 | 160 | μA |

**AC ELECTRICAL CHARACTERISTICS** ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $f_{max}$ | Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4) | 2.0<br>3.0<br>4.5<br>6.0 | 6<br>10<br>30<br>35 | 4.8<br>8.0<br>24<br>28 | 4<br>6<br>20<br>24 | MHz |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figures 1 and 4) | 2.0<br>3.0<br>4.5<br>6.0 | 150<br>75<br>26<br>22 | 190<br>90<br>32<br>28 | 225<br>110<br>38<br>33 | ns |
| $t_{PHL}$ | Maximum Propagation Delay, Reset to Q or $\overline{Q}$ (Figures 2 and 4) | 2.0<br>3.0<br>4.5<br>6.0 | 125<br>70<br>22<br>19 | 155<br>85<br>27<br>24 | 190<br>110<br>34<br>30 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, Any Output (Figures 1 and 4) | 2.0<br>3.0<br>4.5<br>6.0 | 75<br>27<br>15<br>13 | 95<br>32<br>19<br>16 | 110<br>36<br>22<br>19 | ns |
| $C_{in}$ | Maximum Input Capacitance | — | 10 | 10 | 10 | pF |

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Flip–Flop)* | 35 | pF |

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

**TIMING REQUIREMENTS** (Input $t_r = t_f = 6$ ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $t_{su}$ | Minimum Setup Time, Data to Clock (Figure 3) | 2.0<br>3.0<br>4.5<br>6.0 | 100<br>45<br>20<br>17 | 125<br>65<br>25<br>21 | 150<br>85<br>30<br>26 | ns |
| $t_h$ | Minimum Hold Time, Clock to Data (Figure 3) | 2.0<br>3.0<br>4.5<br>6.0 | 5<br>3<br>3<br>3 | 5<br>3<br>3<br>3 | 5<br>3<br>3<br>3 | ns |
| $t_{rec}$ | Minimum Recovery Time, Reset Inactive to Clock (Figure 2) | 2.0<br>3.0<br>4.5<br>6.0 | 100<br>45<br>20<br>17 | 125<br>65<br>25<br>21 | 150<br>85<br>30<br>26 | ns |
| $t_w$ | Minimum Pulse Width, Clock (Figure 1) | 2.0<br>3.0<br>4.5<br>6.0 | 80<br>45<br>16<br>14 | 100<br>65<br>20<br>17 | 120<br>85<br>24<br>20 | ns |
| $t_w$ | Minimum Pulse Width, Reset (Figure 2) | 2.0<br>3.0<br>4.5<br>6.0 | 80<br>45<br>16<br>14 | 100<br>65<br>20<br>17 | 120<br>85<br>24<br>20 | ns |
| $t_r$, $t_f$ | Maximum Input Rise and Fall Times (Figure 1) | 2.0<br>3.0<br>4.5<br>6.0 | 1000<br>800<br>500<br>400 | 1000<br>800<br>500<br>400 | 1000<br>800<br>500<br>400 | ns |

## SWITCHING WAVEFORMS

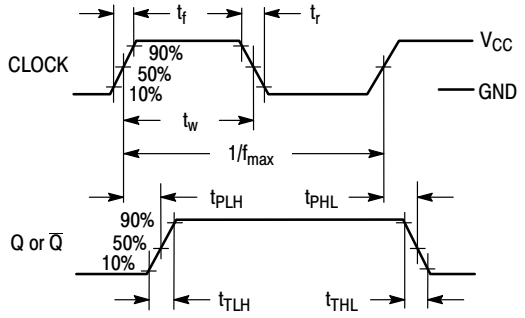



**Figure 3.**

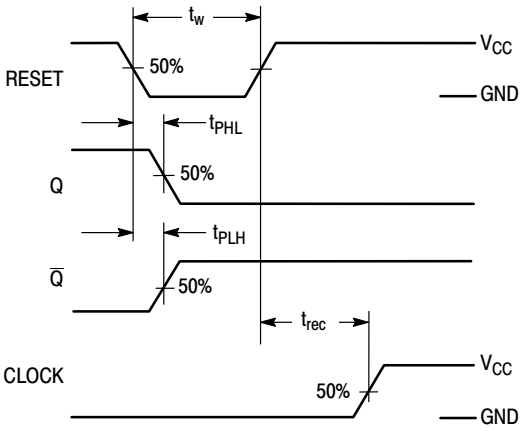



**Figure 4.**

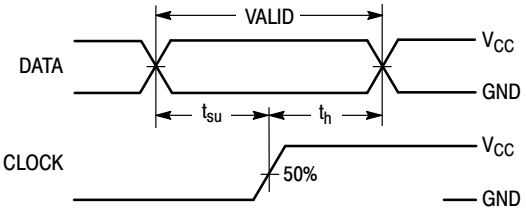
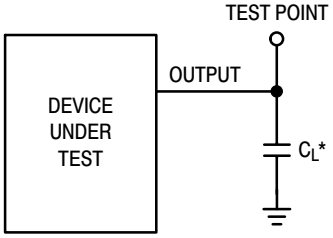



**Figure 5.**

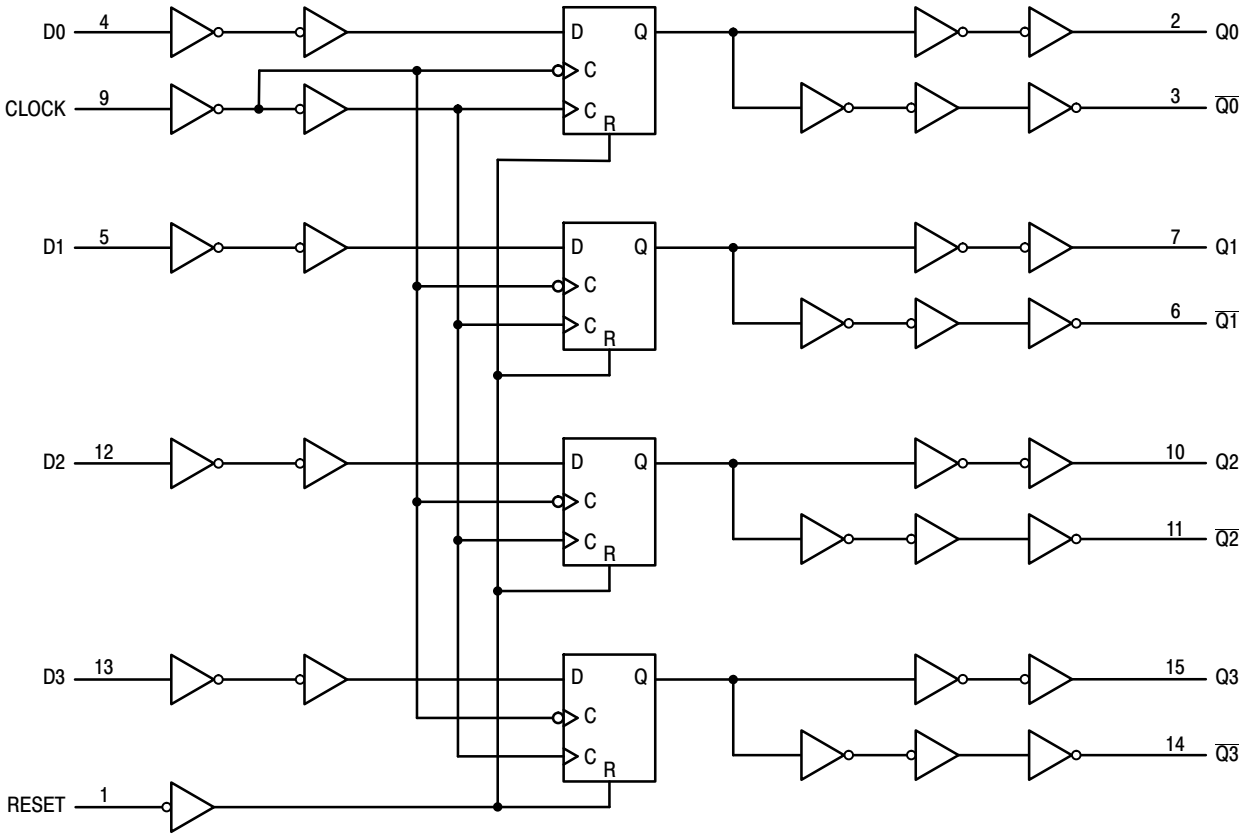
## TEST CIRCUIT




*Includes all probe and jig capacitance

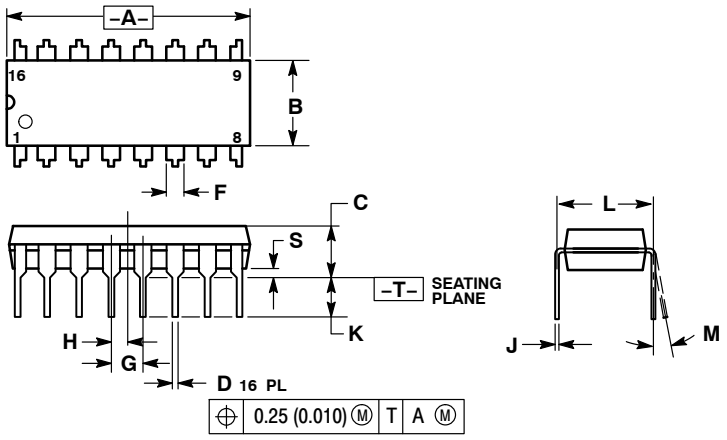
**Figure 6.**

## EXPANDED LOGIC DIAGRAM



## PACKAGE DIMENSIONS

**PDIP−16**
CASE 648−08
ISSUE T

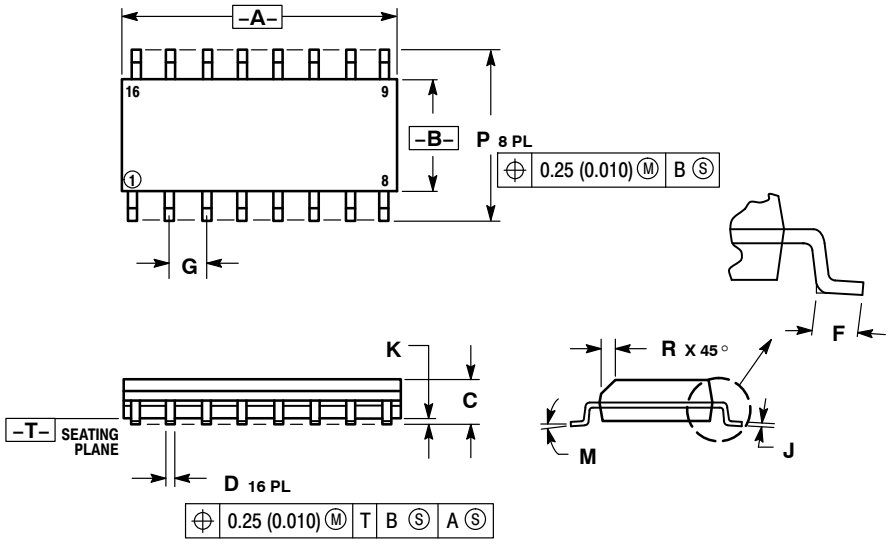



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

## PACKAGE DIMENSIONS

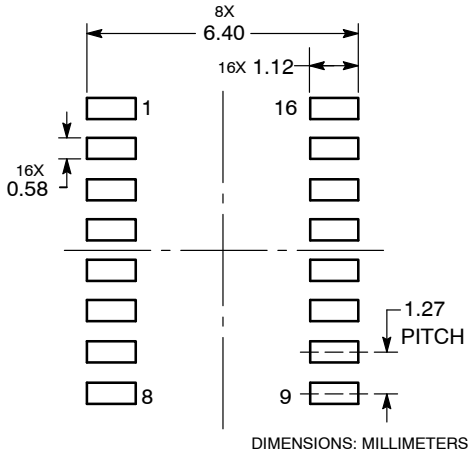
**SOIC−16**
CASE 751B−05
ISSUE K




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

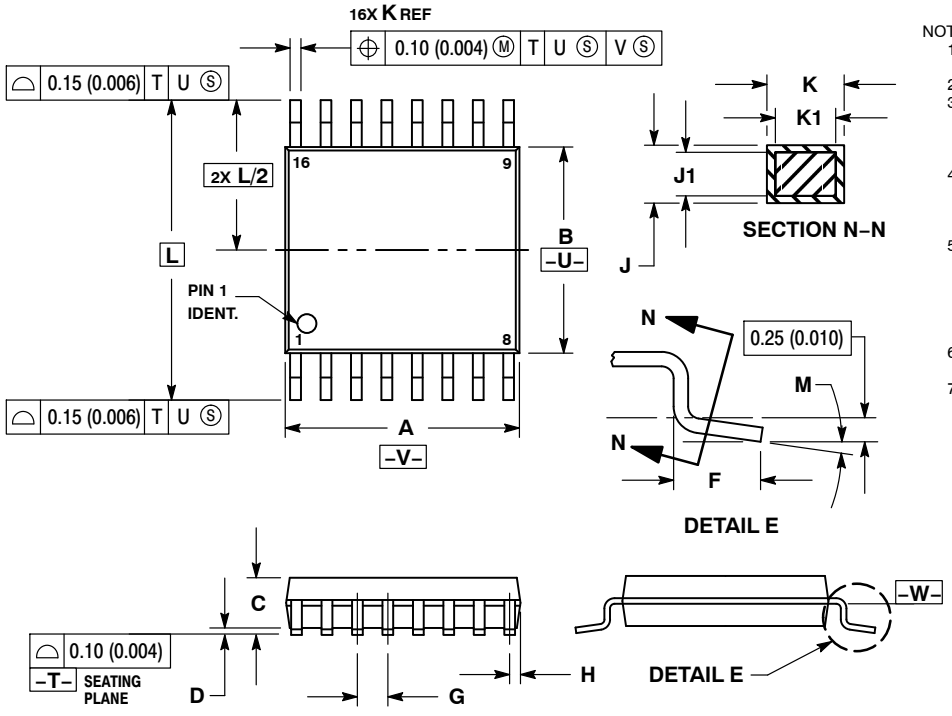
## SOLDERING FOOTPRINT




DIMENSIONS: MILLIMETERS

## PACKAGE DIMENSIONS

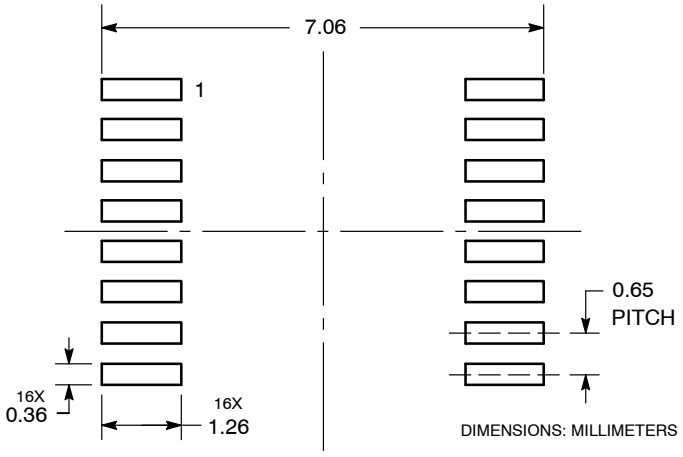
**TSSOP−16**
CASE 948F−01
ISSUE B




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

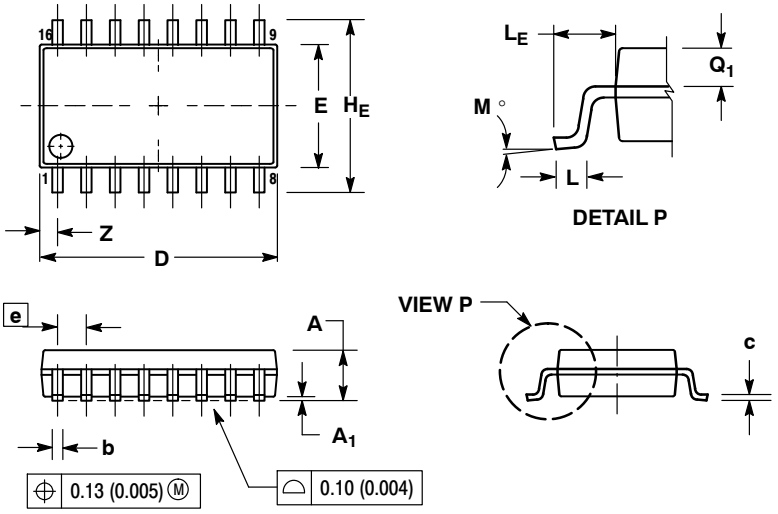
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

## SOLDERING FOOTPRINT



## PACKAGE DIMENSIONS

**SOEIAJ−16**
CASE 966−01
ISSUE A




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 ( 0.018).

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| $A_1$ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.10 | 0.20 | 0.007 | 0.011 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| $H_E$ | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| $L_E$ | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| $Q_1$ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 0.78 | --- | 0.031 |

**ON Semiconductor** and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. “Typical” parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

**PUBLICATION ORDERING INFORMATION**

**LITERATURE FULFILLMENT**:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
**Phone**: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
**Fax**: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
**Email**: orderlit@onsemi.com

**N. American Technical Support**: 800−282−9855 Toll Free USA/Canada
**Europe, Middle East and Africa Technical Support:**
Phone: 421 33 790 2910
**Japan Customer Focus Center**
Phone: 81−3−5773−3850

**ON Semiconductor Website**: **www.onsemi.com**

**Order Literature**: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative