MC9S08PB16

MC9S08PB16 Data Sheet

Supports: MC9S08PB16 and MC9S08PB8

Key features

- 8-Bit S08 central processor unit (CPU)
  - Up to 20 MHz bus at 2.7 V to 5.5 V across operating temperature range
  - Supporting up to 30 interrupt/reset sources
  - Supporting up to four-level nested interrupt
  - On-chip memory
  - Up to 16 KB flash read/program/erase over full operating voltage and temperature
  - Up to 1 KB random-access memory (RAM)
  - Flash and RAM access protection
- Power-saving modes
  - One low power stop mode; reduced power wait mode
  - Peripheral clock enable register can disable clocks to unused modules, reducing currents; allows clocks to remain enabled to specific peripherals in stop3 mode
- Clocks
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution; 1% deviation across temperature range of 0 ºC to 70ºC, 1.5% deviation across temperature range of –40 ºC to 105 ºC and 2% deviation across temperature range of –40 ºC to 125 ºC; Up to 20 MHz
  - Oscillator (XOSC) — Loop-controlled Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 39.0625 kHz or 4 MHz to 20 MHz
- System protection
  - Watchdog with independent clock source
  - Low-voltage detection with reset or interrupt; selectable trip points
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- Peripherals
  - ADC - 12-channel, 12-bit resolution; 2.5 µs conversion time; eight-level data FIFO with optional watermark; automatic compare function; 1.7 mV/ºC temperature sensor; internal bandgap reference channel; operation in stop; optional hardware trigger
  - FTM - Two flex timer modulators (FTM) modules including one 6-channel (FTM2) and one 2-channel (FTM0) backward compatible with TPM modules; 16-bit counter; each channel can be configured for input capture, output compare, edge- or center-aligned PWM mode
  - FDS - Shut down output pin upon fault detection; the fault sources can be optional enabled separately; the output pin can be configured as output 1,0 and high impedance when a fault occurs based on module configuration
  - MTIM - Two modulo timers with 8-bit prescaler and overflow interrupt
  - PWT — One pulse width timer used to captures a pulse width and pulse period
  - SCI - One serial communications interface (SCI/UART) modules optional 13-bit break; Full duplex non-return to zero (NRZ); LIN extension support
  - I2C - One inter-integrated circuit module; up to 400 kbps; multi-master operation; programmable slave address; supporting broadcast mode and 10-bit addressing; supporting SMBUS
  - ACMP - Two analog comparators with both positive and negative inputs; selectable voltage reference provided by on-chip 6-bit DAC; separately selectable interrupt on rising and falling comparator output
  - OPAMP — One analog amplifier (OPAMP) with fixed gain x20, supporting up to 100 mV single-ended input.
  - RTC - 16-bit real timer counter (RTC)
  - CRC - Cyclic Redundancy Check with programmable 16-/32-bit polynomial generator
  - KBI — Up to 8 keyboard interrupt inputs

NXP reserves the right to change the production detail specifications as may be required to permit improvements in the design of its products.

- Development support
  - Single-wire background debug interface
  - Breakpoint capability to allow three breakpoints setting during in-circuit debugging
  - On-chip in-circuit emulator (ICE) debug module containing two comparators and nine trigger modes
- Input/Output
  - Up to 18 GPIOs including one output-only pin (PTA4)
  - One 8-bit keyboard interrupt modules (KBI)
  - One true open drain pin (PTB0)
- Package options
  - 20-pin TSSOP
  - 16-pin TSSOP

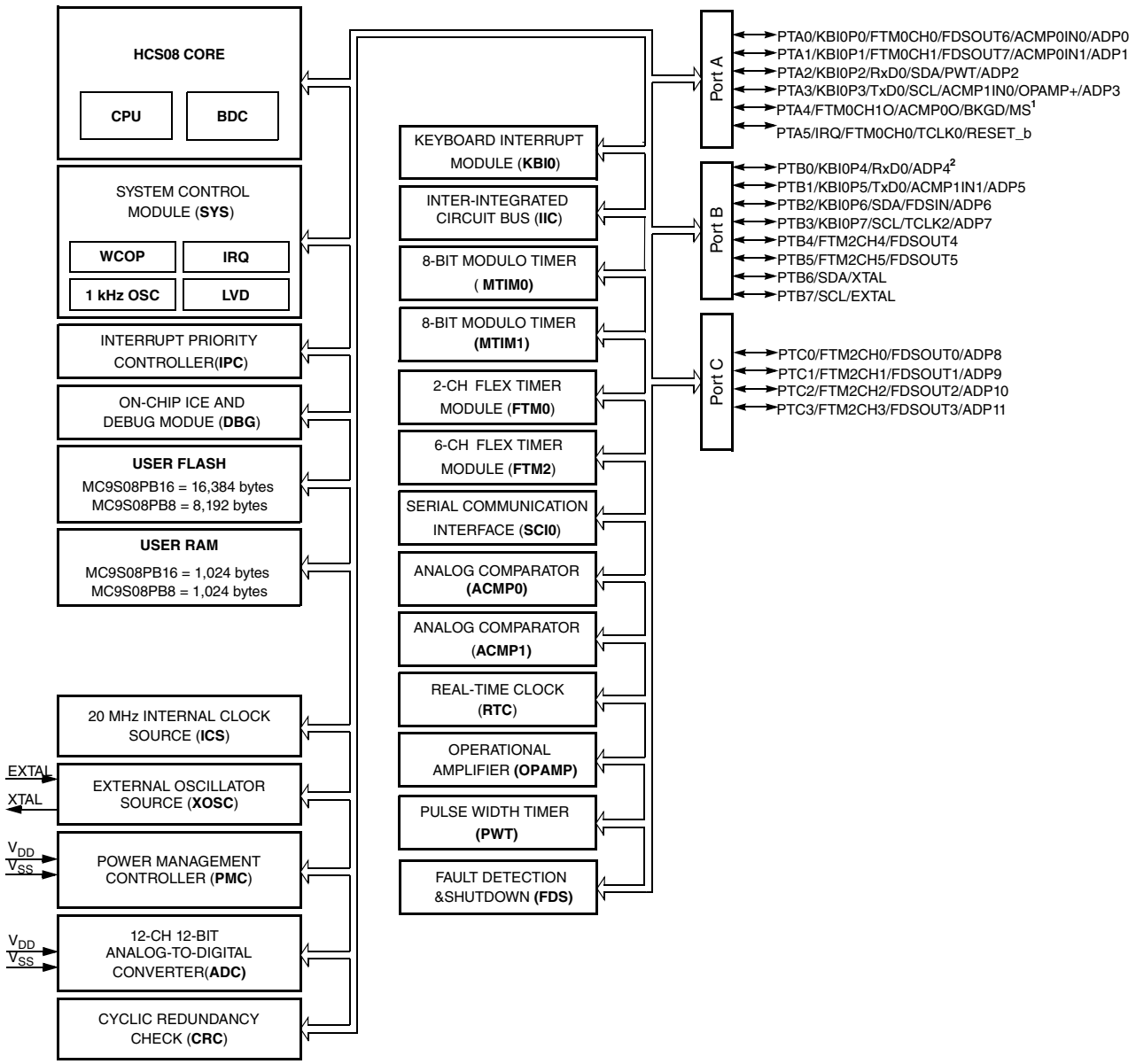
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1 Overview

1.1 MCU block diagram

The block diagram below shows the structure of the MCUs.



1. PTA4/FTM0CH1O/ACMP0O/BKGD/MS is an output-only pin when used as port pin.
2. PTB0 operates as true-open drain when working as output.

Figure 1. MCU block diagram

1.2 Peripheral register addresses

The register definitions vary in different memory sizes. The register addresses of unused peripherals are reserved. The following table shows the register availability of the devices.

Table 1. Peripheral register addresses

Address	Size (Byte)	Peripheral
0x0000-0x0002	3	Port data
0x0010-0x0017	8	ADC
0x0018-0x001B	4	MTIM0
0x001C-0x001F	4	MTIM1
0x0020-0x002A	11	FTM0
0x002C-0x002F	4	ACMP0
0x003B-0x003B	1	IRQ
0x003C-0x003C	1	KBI0
0x003E-0x003F	2	IPC
0x3000-0x300B	12	SYS
0x300C-0x300F	4	SCG
0x3010-0x301F	16	DBG
0x3020-0x302C	13	NVM
0x3030-0x3037	8	PWT
0x3038-0x303C	5	ICS
0x303E-0x303E	1	OSC
0x3040-0x3041	2	PMC
0x304A-0x304B	2	SYS (ILLA)
0x3050-0x305A	11	IPC
0x305C-0x305F	4	ACMP1
0x3060-0x3068	9	CRC
0x306A-0x306F	6	RTC
0x3070-0x307B	12	I^2C
0x307C-0x307D	2	KBI0
0x3080-0x3087	8	SCI0
0x30AC-0x30AD	2	ADC
0x30B0-0x30B2	3	Port output enable
0x30B8-0x30BA	3	Port input enable
0x30C0-0x30D6	23	FTM2
0x30DD-0x30E2	6	FDS
0x30EC-0x30EF	4	Port filter
0x30F0-0x30F2	3	Port pullup
0x30F8-0x30FF	8	SYS (UUID)

1.3 System interconnection

This device contains a set of system-level logics for module-to-module interconnection for flexible configuration. These interconnections provide the hardware trigger function between modules with least software configuration, which is ideal for infrared communication, serial communication baudrate detection, low-end motor control, metering clock calibration, and other general-purpose applications.

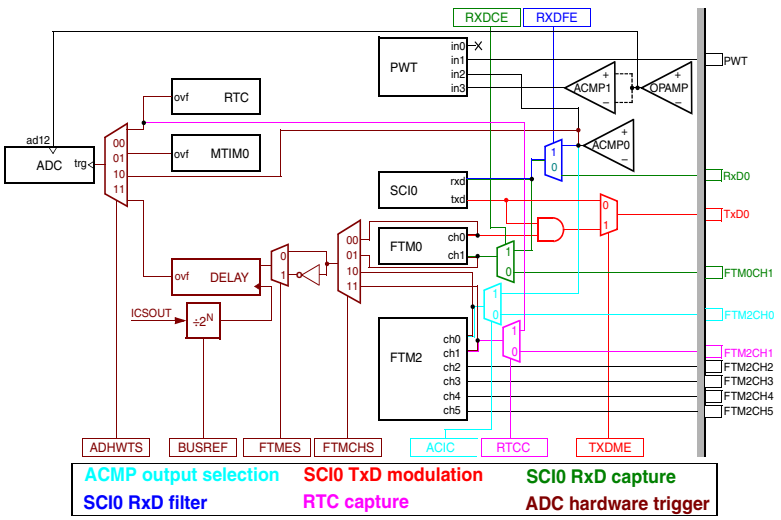


Figure 2. System interconnection diagram

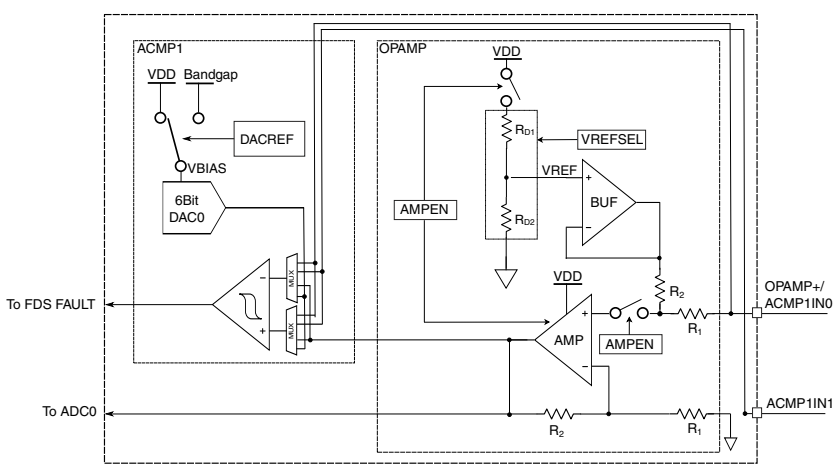


Figure 3. OPAMP and ACMP1 interconnection

2 Orderable part numbers

The following table summarizes the part numbers of the devices covered by this document.

Table 2. Orderable part numbers summary

Feature	MC9S08PB16		MC9S08PB8	
Part Number	VTJ	VTG	VTJ	VTG
	MTJ	MTG	MTJ	MTG
Max. frequency (MHz)	20	20	20	20
Flash memory (KB)	16	16	8	8
RAM (KB)	1	1	1	1
12-bit ADC	12ch	8ch	12ch	8ch
ACMP	2	2	2	2
OPAMP	1	1	1	1
16-bit FlexTimer	6ch+2ch	2ch+2ch	6ch+2ch	2ch+2ch
8-bit Modulo timer	2	2	2	2
RTC	Yes	Yes	Yes	Yes
PWT	1	1	1	1
I2C	1	1	1	1
SCI (LIN Capable)	1	1	1	1
WCOP	Yes	Yes	Yes	Yes
CRC	Yes	Yes	Yes	Yes
FDS	Yes	Yes	Yes	Yes
FDS pins	8	4	8	4
KBI pins	8	8	8	8
GPIO	18	14	18	14
Package	20-TSSOP	16-TSSOP	20-TSSOP	16-TSSOP

3 Part identification

3.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

3.2 Format

Part numbers for this device have the following format:

MC 9 S08 PB AA B CC

3.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
MC	Qualification status	• MC = fully qualified, general market flow
9	Memory	• 9 = flash based
S08	Core	• S08 = 8-bit CPU
PB	Device family	• PB
AA	Approximate flash size in KB	• 16 = 16 KB • 8 = 8 KB
B	Operating temperature range (°C)	• V = -40 to 105 • M = -40 to 125
CC	Package designator	• TJ = 20-TSSOP • TG = 16-TSSOP

3.4 Example

This is an example part number:

MC9S08PB16VTG

4 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 3. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.

Table continues on the next page...

Table 3. Parameter Classifications (continued)

C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled "C" in the parameter tables where appropriate.

5 Ratings

5.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-6000	+6000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 125 °C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78D, IC Latch-up Test.
   - Test was performed at 125 °C case temperature (Class II).
   - I/O pins pass +100/-100 mA I-test with I_{DD} current limit at 400 mA.
   - I/O pins pass +30/-100 mA I-test with I_{DD} current limit at 1000mA.
   - Supply groups pass 1.5 Vccmax.
   - RESET_b pin was only tested with negative I-test due to product conditioning requirement.

5.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in below table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Symbol	Description	Min.	Max.	Unit
V_{DD}	Supply voltage	–0.3	6.0	V
I_{DD}	Maximum current into V_{DD}	—	120	mA
V_{DIO}	Digital input voltage (except $\overline{\text{RESET}}$, EXTAL, XTAL, or true open drain pin)	–0.3	V_{DD} + 0.3	V
	Digital input voltage (true open drain pin)	-0.3	6	V
V_{AIO}	Analog[1], $\overline{\text{RESET}}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V

1. All digital I/O pins, except open-drain pin , are internally clamped to V_{SS} and V_{DD}. is only clamped to V_{SS}.

6 General

6.1 Nonswitching electrical specifications

6.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 4. DC characteristics

Symbol	C	Descriptions			Min	Typical[1]	Max	Unit
—	—	Operating voltage		—	2.7	—	5.5	V
V_{OH}	P	Output high voltage	All I/O pins, standard-drive strength	5 V, I_{load} = -5 mA	V_{DD} - 0.8	—	—	V
	C			3 V, I_{load} = -2.5 mA	V_{DD} - 0.8	—	—	V
I_{OHT}	D	Output high current	Max total I_{OH} for all ports	5 V	—	—	-100	mA
				3 V	—	—	-50	
V_{OL}	P	Output low voltage	All I/O pins, standard-drive strength	5 V, I_{load} = 5 mA	—	—	0.8	V
	C			3 V, I_{load} = 2.5 mA	—	—	0.8	V
I_{OLT}	D	Output low current	Max total I_{OL} for all ports	5 V	—	—	100	mA
				3 V	—	—	50	
V_{IH}	P	Input high voltage	All digital inputs	V_{DD}>4.5V	0.70 × V_{DD}	—	—	V
	C			V_{DD}>2.7V	0.75 × V_{DD}	—	—	
V_{IL}	P	Input low voltage	All digital inputs	V_{DD}>4.5V	—	—	0.30 × V_{DD}	V
	C			V_{DD}>2.7V	—	—	0.35 × V_{DD}	
V_{hys}	C	Input hysteresis	All digital inputs	—	0.06 × V_{DD}	—	—	mV
$\lvert I_{In}\rvert$	P	Input leakage current	All input only pins (per pin)	V_{IN} = V_{DD} or V_{SS}	—	0.1	1	µA
$\lvert I_{OZ}\rvert$	P	Hi-Z (off-state) leakage current	All input/output (per pin)	V_{IN} = V_{DD} or V_{SS}	—	0.1	1	µA
$\lvert I_{OZTOT}\rvert$	C	Total leakage combined for all inputs and Hi-Z pins	All input only and I/O	V_{IN} = V_{DD} or V_{SS}	—	—	2	µA
R_{PU}	P	Pullup resistors	All digital inputs, when enabled (all I/O pins other than PTB0)	—	30.0	—	50.0	kΩ

Table continues on the next page...

Table 4. DC characteristics (continued)

Symbol	C	Descriptions			Min	Typical[1]	Max	Unit
R_{PU}[2]	P	Pullup resistors	PTB0 pin	—	30.0	—	60.0	kΩ
I_{IC}	D	DC injection current[3, 4, 5]	Single pin limit	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	-0.2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	
C_{In}	C	Input capacitance, all pins		—	—	—	7	pF
V_{RAM}	C	RAM retention voltage		—	2.0	—	—	V

1. Typical values are measured at 25 °C. Characterized, not tested.
2. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
3. All functional non-supply pins, except for PTB0, are internally clamped to V_{SS} and V_{DD}.
4. Input must be current-limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the large one.
5. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is higher than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 5. LVD and POR Specification

Symbol	C	Description		Min	Typ	Max	Unit
V_{POR}	D	POR re-arm voltage[1, 2]		1.5	1.75	2.0	V
V_{LVDH}	C	Falling low-voltage detect threshold - high range (LVDV = 1)[3]		4.2	4.3	4.4	V
V_{LVW1H}	C	Falling low-voltage warning threshold - high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V_{LVW2H}	C		Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V_{LVW3H}	C		Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V_{LVW4H}	C		Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V_{HYSH}	C	High range low-voltage detect/warning hysteresis		—	100	—	mV
V_{LVDL}	C	Falling low-voltage detect threshold - low range (LVDV = 0)		2.56	2.61	2.66	V
V_{LVDW1L}	C	Falling low-voltage warning threshold - low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V_{LVDW2L}	C		Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V_{LVDW3L}	C		Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V

Table continues on the next page...

Table 5. LVD and POR Specification (continued)

Symbol	C	Description		Min	Typ	Max	Unit
V_{LVDW4L}	C		Level 4 falling (LVWV = 11)	2.92	3.0	3.08	V
V_{HYSDL}	C	Low range low-voltage detect hysteresis		—	40	—	mV
V_{HYSWL}	C	Low range low-voltage warning hysteresis		—	80	—	mV
V_{BG}	P	Buffered bandgap output [4]		1.14	1.16	1.18	V

1. Maximum is highest voltage that POR is guaranteed.
2. POR ramp time must be longer than 20us/V to get a stable startup.
3. Rising thresholds are falling threshold + hysteresis.
4. Voltage factory trimmed at V_{DD} = 5.0 V, Temp = 25 °C

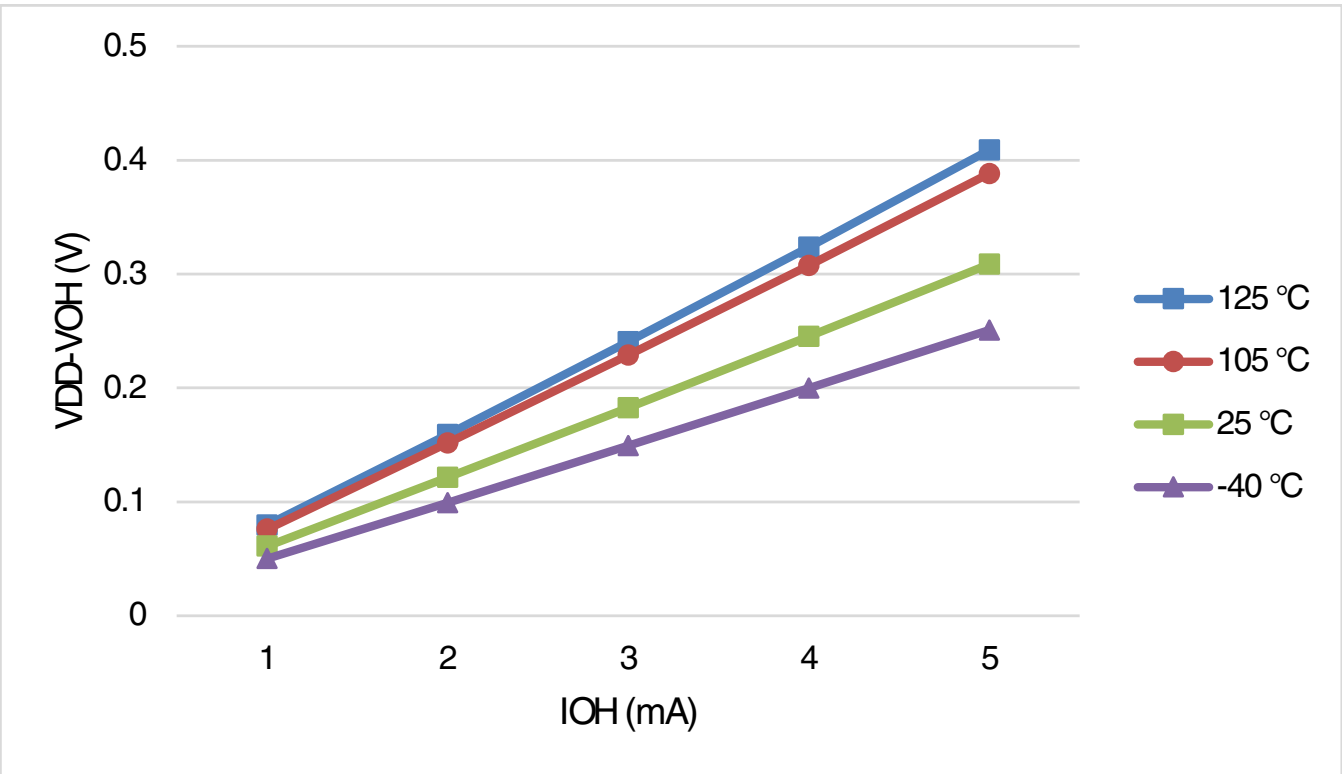


Figure 4. Typical I_{OH} Vs. V_{DD}-V_{OH} (standard drive strength) (V_{DD} = 5 V)

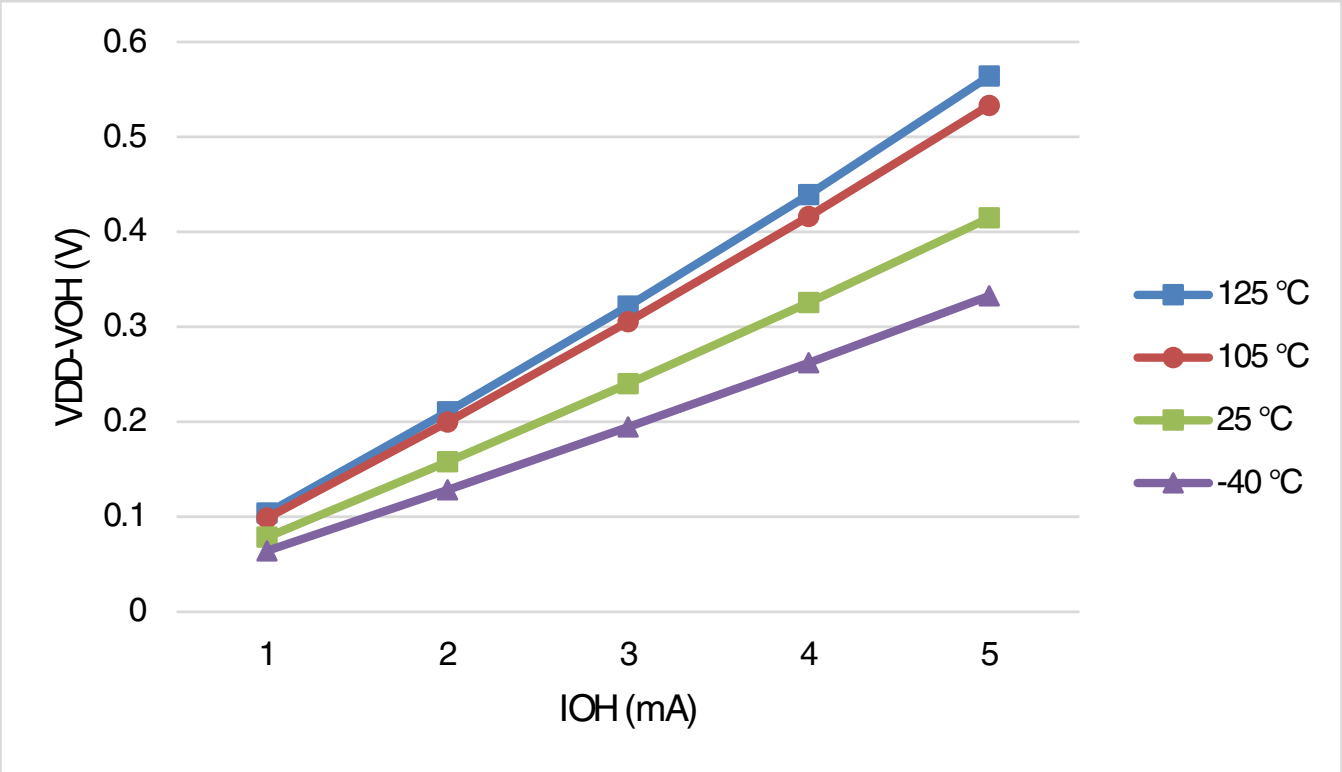


Figure 5. Typical I_{OH} Vs. V_{DD}-V_{OH} (standard drive strength) (V_{DD} = 3.5 V)

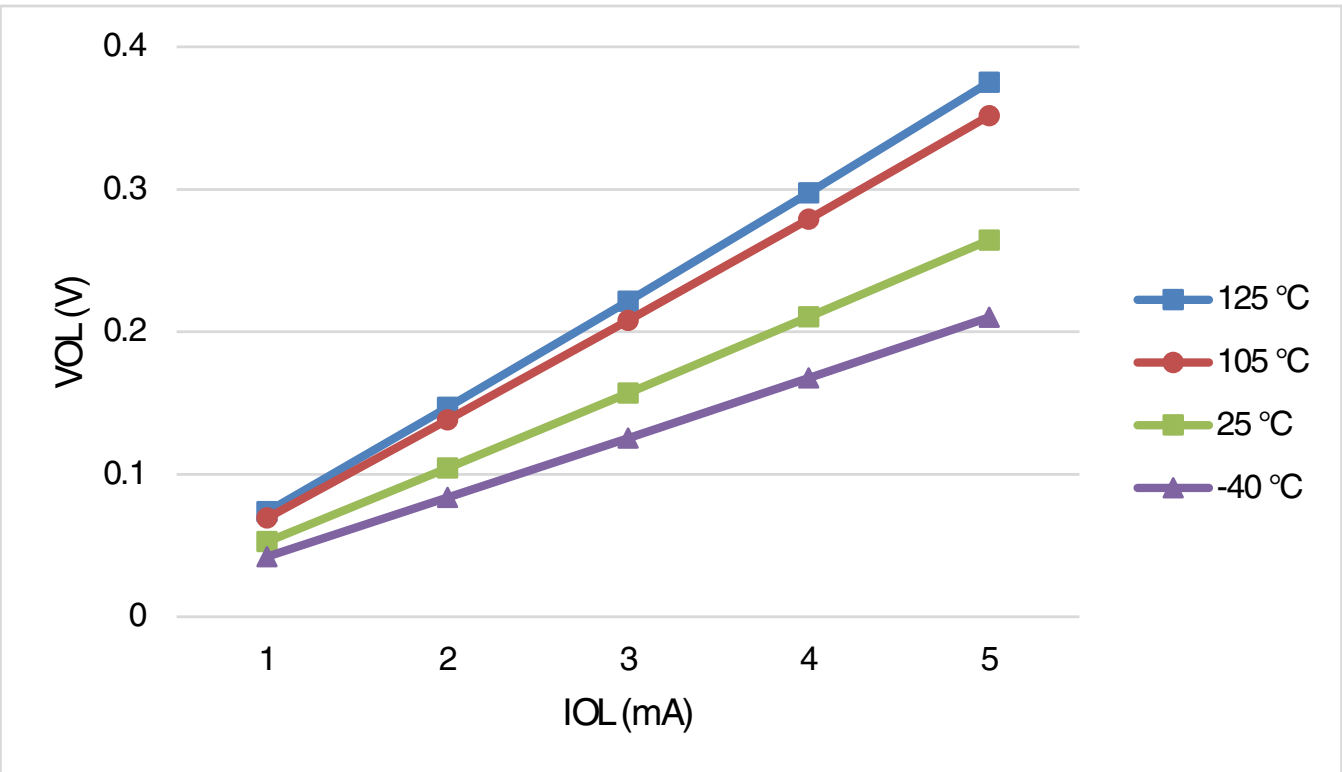


Figure 6. Typical I_{OL} Vs. V_{OL} (standard drive strength) (V_{DD} = 5 V)

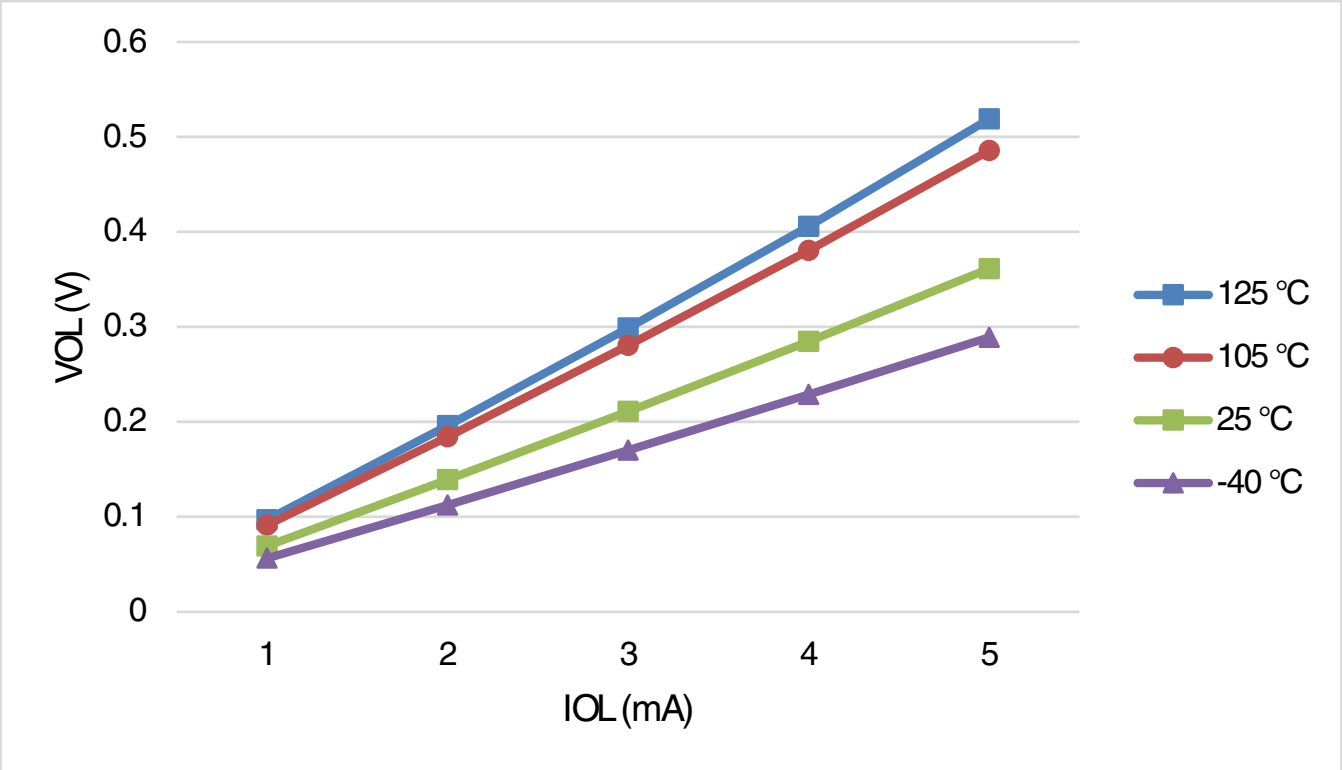


Figure 7. Typical I_{OL} Vs. V_{OL} (standard drive strength) (V_{DD} = 3.5 V)

6.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 6. Supply current characteristics in operating temperature range

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit
1	C	Run supply current FEI mode, all modules on; run from flash	RI_{DD}	20 MHz	5	5.60	—	mA
	C			10 MHz		3.91	—	
				1 MHz		2.34	—	
	C			20 MHz	3	5.57	—	
	C			10 MHz		3.91	—	
				1 MHz		2.34	—	
2	C	Run supply current FEI mode, all modules off and gated; run from flash	RI_{DD}	20 MHz	5	4.44	—	mA
	C			10 MHz		3.34	—	
				1 MHz		2.29	—	
	C			20 MHz	3	4.43	—	
	C			10 MHz		3.34	—	
				1 MHz		2.29	—	

Table continues on the next page...

Table 6. Supply current characteristics in operating temperature range (continued)

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit
3	P	Run supply current FBE mode, all modules on; run from RAM	RI_{DD}	20 MHz	5	5.52	7	mA
	C			10 MHz		3.51	—	
				1 MHz		1.70	—	
	C			20 MHz	3	5.51	—	
	C			10 MHz		3.50	—	
				1 MHz		1.69	—	
4	P	Run supply current FBE mode, all modules off and gated; run from RAM	RI_{DD}	20 MHz	5	4.37	5.5	mA
	C			10 MHz		2.94	—	
				1 MHz		1.64	—	
	C			20 MHz	3	4.36	—	
	C			10 MHz		2.93	—	
				1 MHz		1.64	—	
5	C	Wait mode current FEI mode, all modules on	WI_{DD}	20 MHz	5	4.17	—	mA
	C			10 MHz		2.87	—	
				1 MHz		1.64	—	
	C			20 MHz	3	4.16	—	
				10 MHz		2.87	—	
				1 MHz		1.63	—	
6	C	Stop3 mode supply current no clocks active (except 1 kHz LPO clock)[2, 3]	$S3I_{DD}$	—	5	1.3	—	µA
	C			—	3	1.2	—	
7	C	ADC adder to stop3	—	—	5	85	—	µA
	C	ADLPC = 1 ADLSMP = 1 ADCO = 1 MODE = 10B ADICLK = 11B	—	—	3	80	—	
8	C	LVD adder to stop3[4]	—	—	5	126	—	µA
	C				3	123	—	

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. RTC adder cause <1 µA I_{DD} increase typically, RTC clock source is 1 kHz LPO clock.
3. ACMP adder cause <10 µA I_{DD} increase typically.
4. LVD is periodically woken up from stop3 by 5% duty cycle. The period is equal to or less than 2 ms.

6.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software

operation all play a significant role in EMC performance. The system designer should consult NXP applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

6.2 Switching specifications

6.2.1 Control timing

Table 7. Control timing

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	P	Bus frequency (t_{cyc} = 1/f_{Bus})		f_{Bus}	DC	—	20	MHz
2	P	Internal low power oscillator frequency		f_{LPO}	0.67	1.0	1.25	KHz
3	D	External reset pulse width[2]		t_{extrst}	1.5 × t_{cyc}	—	—	ns
4	D	Reset low drive		t_{rstdrv}	34 × t_{cyc}	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes		t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes[3]		t_{MSH}	100	—	—	ns
7	D	IRQ pulse width	Asynchronous path[2]	t_{ILIH}	100	—	—	ns
	D		Synchronous path[4]	t_{IHIL}	1.5 × t_{cyc}	—	—	ns
8	D	Keyboard interrupt pulse width	Asynchronous path[2]	t_{ILIH}	100	—	—	ns
	D		Synchronous path	t_{IHIL}	1.5 × t_{cyc}	—	—	ns
9	C	Port rise and fall time - standard drive strength (load = 50 pF)[5]	—	t_{Rise}	—	10.2	—	ns
	C			t_{Fall}	—	9.5	—	ns
	C	Port rise and fall time - high drive strength (load = 50 pF)[5]	—	t_{Rise}	—	5.4	—	ns
	C			t_{Fall}	—	4.6	—	ns

1. Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a reset pin request.
3. To enter BDM mode following a POR, BKGD/MS must be held low during the powerup and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.
4. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
5. Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels in operating temperature range.

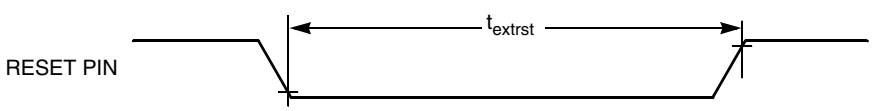


Figure 8. Reset timing

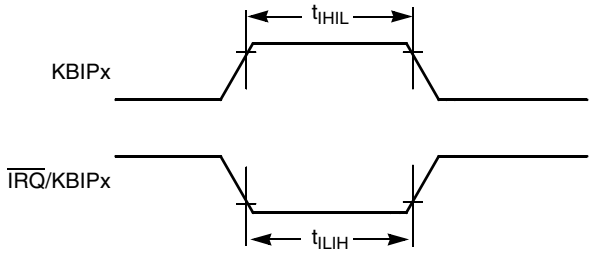


Figure 9. IRQ/KBIPx timing

6.2.2 Debug trace timing specifications

Table 8. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
t_{cyc}	Clock period	Frequency dependent		MHz
t_{wl}	Low pulse width	2	—	ns
t_{wh}	High pulse width	2	—	ns
t_r	Clock and data rise time	—	3	ns
t_f	Clock and data fall time	—	3	ns
t_s	Data setup	3	—	ns
t_h	Data hold	2	—	ns

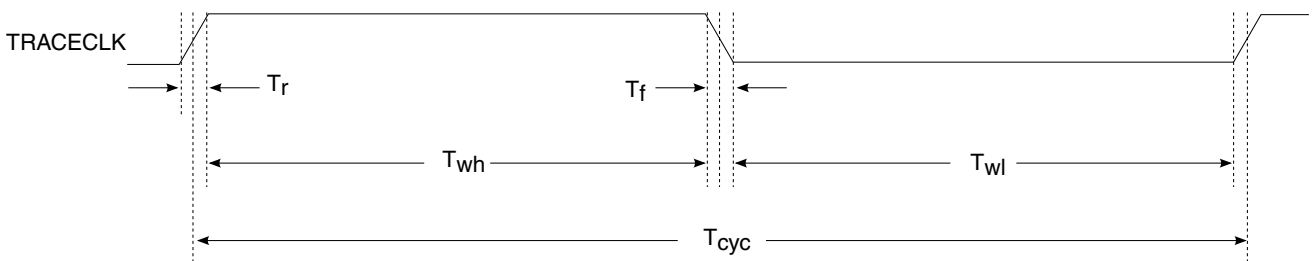


Figure 10. TRACE_CLKOUT specifications

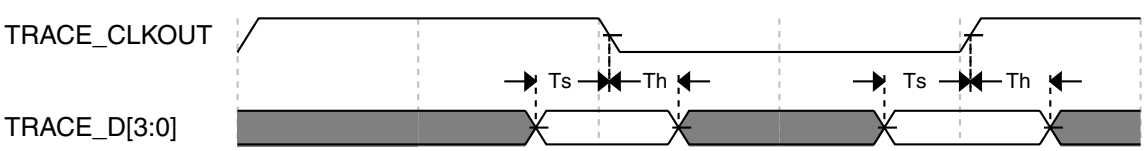


Figure 11. Trace data specifications

6.2.3 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 9. FTM input timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

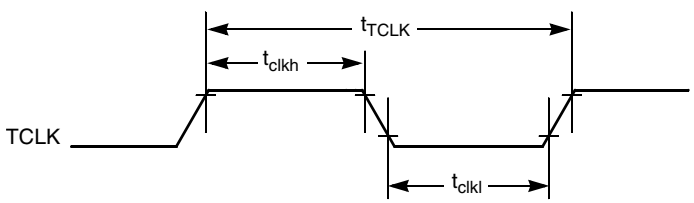


Figure 12. Timer external clock

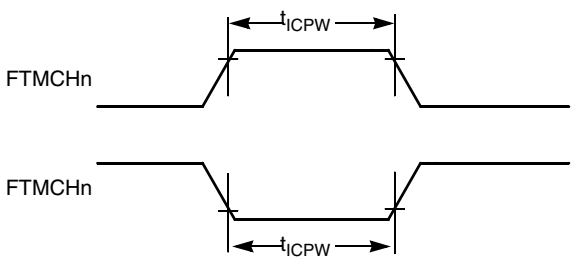


Figure 13. Timer input capture pulse

6.3 Thermal specifications

6.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 10. Thermal characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A[1]	T_L to T_H • V part: -40 to 105 • M part: -40 to 125	°C
Junction temperature range	T_J	• V part: -40 to 125 • M part: -40 to 135	°C
Thermal resistance single-layer board			
20-pin TSSOP	$R_{\theta JA}$	116	°C/W
16-pin TSSOP	$R_{\theta JA}$	130	°C/W
Thermal resistance four-layer board			
20-pin TSSOP	$R_{\theta JA}$	76	°C/W
16-pin TSSOP	$R_{\theta JA}$	87	°C/W

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA}$ x chip power dissipation.

7 Peripheral operating requirements and behaviors

7.1 External oscillator (XOSC) and ICS characteristics

Table 11. XOSC and ICS specifications in operating temperature range

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator	Low range (RANGE = 0)	f_{lo}	31.25	32.768	39.0625	kHz

Table continues on the next page...

Table 11. XOSC and ICS specifications in operating temperature range (continued)

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
	C		High range (RANGE = 1) FEE or FBE mode[2]	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), high gain (HGO = 1), FBELP mode	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), low power (HGO = 0), FBELP mode	f_{hi}	4	—	20	MHz
2	D	Load capacitors		C1, C2	See Note[3]			
3	D	Feedback resistor	Low Frequency, Low-Power Mode[4]	R_F	—	—	—	MΩ
			Low Frequency, High-Gain Mode		—	10	—	MΩ
			High Frequency, Low-Power Mode		—	1	—	MΩ
			High Frequency, High-Gain Mode		—	1	—	MΩ
4	D	Series resistor - Low Frequency	Low-Power Mode [4]	R_S	—	—	—	kΩ
			High-Gain Mode		—	200	—	kΩ
5	D	Series resistor - High Frequency	Low-Power Mode[4]	R_S	—	—	—	kΩ
	D	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
	D		8 MHz		—	0	—	kΩ
	D		16 MHz		—	0	—	kΩ
6	C	Crystal start-up time Low range = 32.768 kHz crystal; High range = 20 MHz crystal[5, 6]	Low range, low power	t_{CSTL}	—	1000	—	ms
	C		Low range, high power		—	800	—	ms
	C		High range, low power	t_{CSTH}	—	3	—	ms
	C		High range, high power		—	1.5	—	ms
7	T	Internal reference start-up time		t_{IRST}	—	20	50	µs
8	D	Square wave input clock frequency	FEE or FBE mode[2]	f_{extal}	0.03125	—	5	MHz
	D		FBELP mode		0	—	20	MHz
9	P	Average internal reference frequency - trimmed		f_{int_t}	—	31.25	—	kHz
10	P	DCO output frequency range - trimmed		f_{dco_t}	16	—	20	MHz
11	P	Total deviation of DCO output from trimmed frequency[5]	Over full voltage and temperature range	Δf_{dco_t}	—	—	±2	$\%f_{dco}$
	C		Over fixed voltage and temperature range of 0 to 70 °C				±1.0	
12	C	FLL acquisition time[5, 7]		$t_{Acquire}$	—	—	2	ms
13	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[8]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

2. When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
3. See crystal or resonator manufacturer's recommendation.
4. Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
5. This parameter is characterized and not tested on each device.
6. Proper PC board layout procedures must be followed to achieve specifications.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

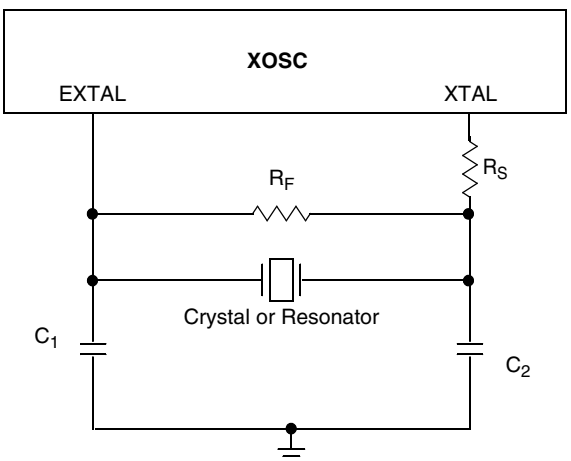


Figure 14. Typical crystal or resonator circuit

7.2 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash memories.

Table 12. Flash clock timing characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit[1]
D	NVM Bus frequency	f_{NVMBUS}	1	—	20	MHz
D	NVM Operating frequency	f_{NVMOP}	0.8	1.0	1.05	MHz
C	FLASH Program/erase endurance across operating temperature	n_{FLPE}	10 k	100 k	—	Cycles
C	Data retention at an average junction temperature of T_{Javg} = 85 °C after up to 10,000 program/erase cycles	t_{D_ret}	15	100	—	years

1. $t_{cyc} = 1 / f_{NVMBUS}$

All timing parameters are a function of the bus clock frequency, F_{NVMBUS}. All program and erase times are also a function of the NVM operating frequency, f_{NVMOP}.

Each command timing is given by:

$t_{command}=f_{NVMOP}$ cycle × $1/f_{NVMOP}$ + f_{NVMBUS} cycle × $1/f_{NVMBUS}$

Table 13. Flash timing characteristics

C	Characteristic	Symbol	f_{NVMOP} cycle	f_{NVMBUS} cycle
D	Erase Verify All Blocks	t_{VFYALL}	—	5050
D	Erase Verify Flash Block	t_{RD1BLK}	—	4631
D	Erase Verify Flash Section	t_{RD1SEC}	—	494
D	Read Once	t_{RDONCE}	—	450
D	Program Flash (2 word)	t_{PGM2}	68	1407
D	Program Flash (4 word)	t_{PGM4}	122	2138
D	Program Once	$t_{PGMONCE}$	122	2090
D	Erase All Blocks	t_{ERSALL}	100066	5455
D	Erase Flash Block	t_{ERSBLK}	100060	4954
D	Erase Flash Sector	t_{ERSPG}	20015	878
D	Unsecure Flash	t_{UNSECU}	100066	5442
D	Verify Backdoor Access Key	t_{VFYKEY}	—	464
D	Set User Margin Level	t_{MLOADU}	—	413

Program and erase operations do not require any special power sources other than the normal V_{DDX} supply. For more detailed information about program/erase operations, see the Flash Memory Module section in the reference manual.

7.3 Analog

7.3.1 ADC characteristics

Table 14. 5 V 12-bit ADC operating conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
	Delta to V_{DD} (V_{DD}-V_{DDAD})	ΔV_{DDA}	-100	0	+100	mV	
Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSA})[2]	ΔV_{SSA}	-100	0	+100	mV	
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	3	5	kΩ	—

Table continues on the next page...

Table 14. 5 V 12-bit ADC operating conditions (continued)

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Analog source resistance	12-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz	R_{AS}	— —	— —	2 5	kΩ	External to MCU
	10-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz		— —	— —	5 10		
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock frequency	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.

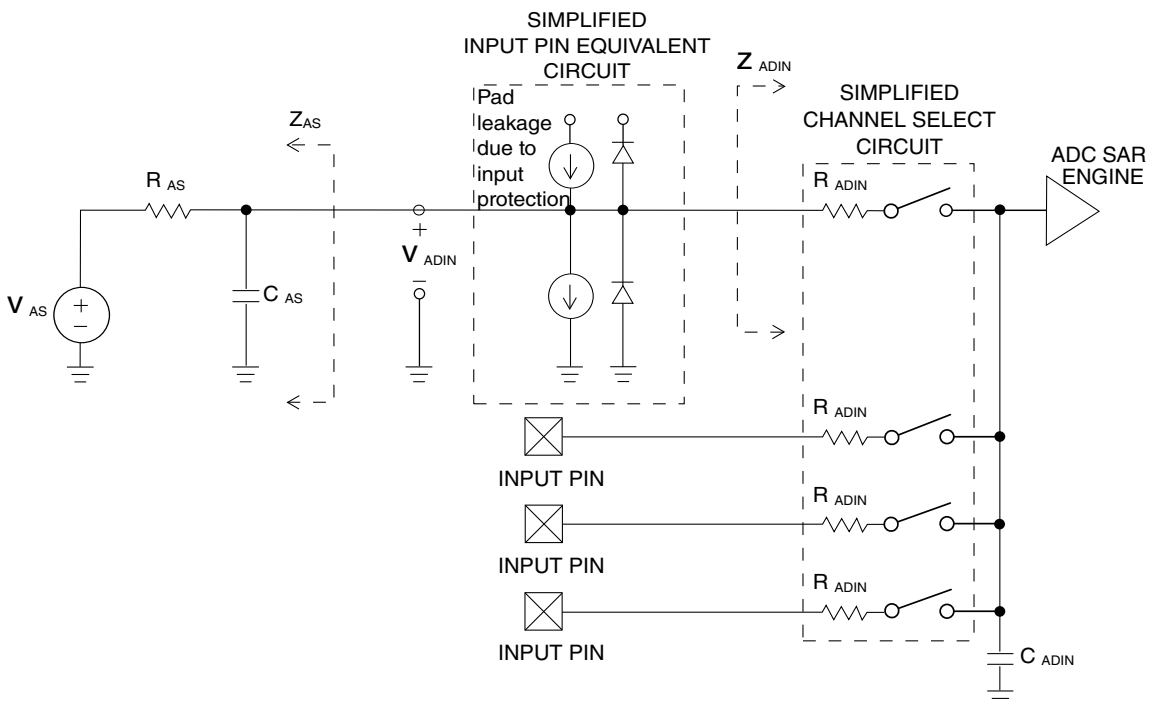


Figure 15. ADC input impedance equivalency diagram

Table 15. 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1		T	I_{DDA}	—	133	—	μA

Table continues on the next page...

Table 15. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
ADCO = 1							
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	218	—	µA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	µA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	582	990	µA
Supply current	Stop, reset, module off	T	I_{DDA}	—	0.011	1	µA
ADC asynchronous clock source	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error[2]	12-bit mode	T	E_{TUE}	—	±5.0	—	LSB[3]
	10-bit mode	P		—	±1.5	±2.0	
	8-bit mode	P		—	±0.7	±1.0	
Differential Non-Linearity	12-bit mode	T	DNL	—	±1.0	—	LSB[3]
	10-bit mode[4]	P		—	±0.25	±0.5	
	8-bit mode[4]	P		—	±0.15	±0.25	
Integral Non-Linearity	12-bit mode	T	INL	—	±1.0	—	LSB[3]
	10-bit mode	T		—	±0.3	±0.5	
	8-bit mode	T		—	±0.15	±0.25	
Zero-scale error[5]	12-bit mode	C	E_{ZS}	—	±2.0	—	LSB[3]
	10-bit mode	P		—	±0.25	±1.0	
	8-bit mode	P		—	±0.65	±1.0	
Full-scale error[6]	12-bit mode	T	E_{FS}	—	±2.5	—	LSB[3]
	10-bit mode	T		—	±0.5	±1.0	

Table continues on the next page...

Table 15. 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
	8-bit mode	T		—	±0.5	±1.0	
Quantization error	≤12 bit modes	D	E_Q	—	—	±0.5	LSB[3]
Input leakage error[7]	all modes	D	E_{IL}	I_{In} * R_{AS}			mV
Temp sensor slope	-40°C– 25°C	D	m	—	3.266	—	mV/°C
	25°C– 125°C			—	3.638	—	
Temp sensor voltage	25°C	D	V_{TEMP25}	—	1.396	—	V

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization.
3. 1 LSB = (V_{REFH} - V_{REFL})/2^N
4. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
5. V_{ADIN} = V_{SSA}
6. V_{ADIN} = V_{DDA}
7. I_{In} = leakage current (refer to DC characteristics)

7.3.2 Analog comparator (ACMP) electricals

Table 16. Comparator electrical specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DDA}	2.7	—	5.5	V
T	Supply current (Operation mode)	I_{DDA}	—	10	20	µA
D	Analog input voltage	V_{AIN}	V_{SS} - 0.3	—	V_{DDA}	V
P	Analog input offset voltage	V_{AIO}	—	—	40	mV
C	Analog comparator hysteresis (HYST=0)	V_H	—	15	20	mV
C	Analog comparator hysteresis (HYST=1)	V_H	—	20	30	mV
T	Supply current (Off mode)	I_{DDAOFF}	—	60	—	nA
C	Propagation Delay	t_D	—	0.4	1	µs

7.3.3 Operational amplifier (OPAMP) electricals

Table 17. OPAMP electrical specifications

Characteristic		Symbol	Min	Typical	Max	Unit
Internal resistor 1 for voltage divider	SYS_COPT6[VREFSEL]=00	RD1	—	257.04	—	kΩ
	SYS_COPT6[VREFSEL]=01		—	220.32	—	
	SYS_COPT6[VREFSEL]=10		—	146.88	—	
Internal resistor 2 for voltage divider	SYS_COPT6[VREFSEL]=00	RD2	—	36.72	—	kΩ
	SYS_COPT6[VREFSEL]=01		—	73.44	—	
	SYS_COPT6[VREFSEL]=10		—	146.88	—	

Table continues on the next page...

Table 17. OPAMP electrical specifications (continued)

Characteristic		Symbol	Min	Typical	Max	Unit
OPAMP internal resistor 1		R1	—	6.4	—	kΩ
OPAMP internal resistor 2		R2	—	128	—	kΩ
Power supply		V_{DDX}	2.7	—	5.5	V
Input dynamic range		V_{IN}	0	—	100	mV
Offset voltage		V_{OS}	—	3	—	mV
OPAMP supply current		I_{DD}	—	—	300	µA
OPAMP GBW		GBW	—	10	—	MHz
OPAMP start up time		$T_{Start-up}$	—	—	2.5	µs

7.3.4 Inter-Integrated Circuit Interface (I2C) timing

Table 18. I2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I^2C bus devices	t_{HD}; DAT	0[1]	3.45[2]	0[3]	0.9[1]	µs
Data set-up time	t_{SU}; DAT	250[4]	—	100[2, 5]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[6]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[5]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
3. Input signal Slew = 10 ns and Output Load = 50 pF
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode I^2C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\,DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\,DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I^2C bus specification) before the SCL line is released.
6. C_b = total capacitance of the one bus line in pF.

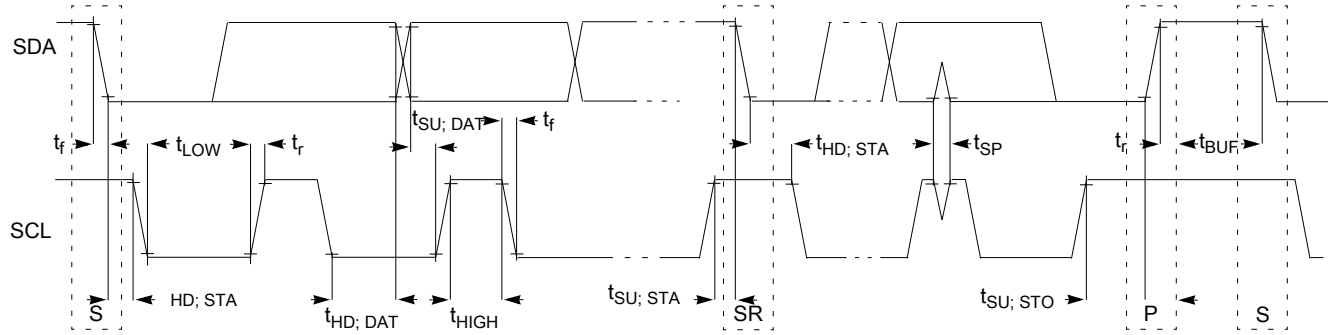


Figure 16. Timing definition for fast and standard mode devices on the I^2C bus

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
16-pin TSSOP	98ASH70247A
20-pin TSSOP	98ASH70169A

9 Pinout

9.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

Table 19. Pin availability by package pin-count

Pin number		Lowest Priority <-- --> Highest					
20-TSSOP	16-TSSOP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4	Alt 5
1	1	PTA5	IRQ	FTM0CH0	TCLK0	-	RESET
2	2	PTA4	-	FTM0CH1	ACMP0O	BKGD	MS

Table continues on the next page...

Table 19. Pin availability by package pin-count (continued)

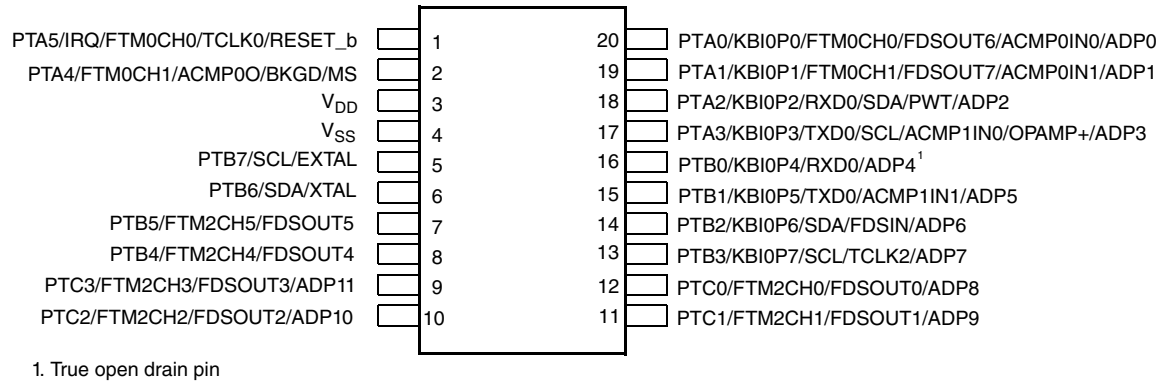
Pin number		Lowest Priority <-- --> Highest					
20-TSSOP	16-TSSOP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4	Alt 5
3	3	-	-	-	-	-	VDD
4	4	-	-	-	-	-	VSS
5	5	PTB7	-	-	SCL	-	EXTAL
6	6	PTB6	-	-	SDA	-	XTAL
7	7	PTB5	-	FTM2CH5	-	FDSOUT5	-
8	8	PTB4	-	FTM2CH4	-	FDSOUT4	-
9	-	PTC3	-	FTM2CH3	-	FDSOUT3	ADP11
10	-	PTC2	-	FTM2CH2	-	FDSOUT2	ADP10
11	-	PTC1	-	FTM2CH1	-	FDSOUT1	ADP9
12	-	PTC0	-	FTM2CH0	-	FDSOUT0	ADP8
13	9	PTB3	KBI0P7	SCL	TCLK2	-	ADP7
14	10	PTB2	KBI0P6	SDA	-	FDSIN	ADP6
15	11	PTB1	KBI0P5	TXD0	-	-	ACMP1IN1/ ADP5
16	12	PTB0 [1]	KBI0P4	RXD0	-	-	ADP4
17	13	PTA3	KBI0P3	TXD0	SCL	-	ACMP1IN0/ OPAMP+/ ADP3
18	14	PTA2	KBI0P2	RXD0	SDA	PWT	ADP2
19	15	PTA1	KBI0P1	FTM0CH1	-	FDSOUT7	ACMP0IN1/ ADP1
20	16	PTA0	KBI0P0	FTM0CH0	-	FDSOUT6	ACMP0IN0/ ADP0

1. This is a true open-drain pin when operating as output.

NOTE

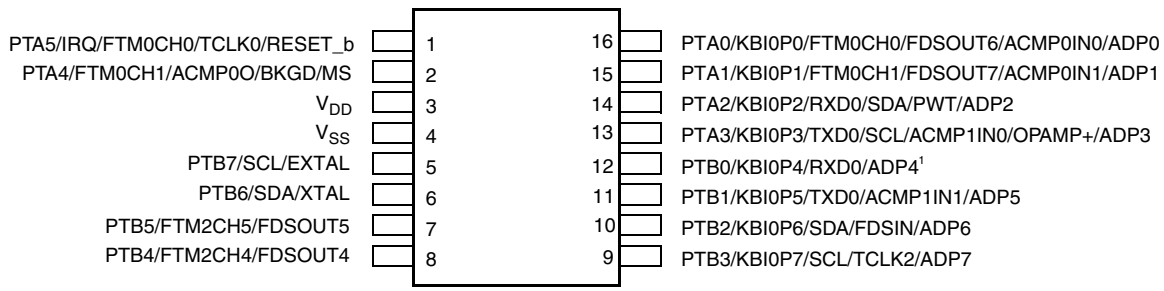
When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. The table above illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

9.2 Device pin assignment



1. True open drain pin

Figure 17. 20-pin TSSOP package



1. True open drain pin

Figure 18. 16-pin TSSOP package

10 Hardware design consideration

This device contains protective circuitry to guard against damage due to high static voltage or electric fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit.

- Place connectors or cables on one edge of the board and do not place digital circuits between connectors.
- Drivers and filters for I/O functions must be placed as close to the connectors as possible. Connect TVS devices at the connector to a good ground. Connect filter capacitors at the connector to a good ground. Consider to add ferrite bead or inductor to some sensitive lines.
- Physically isolate analog circuits from digital circuits if possible.
- Place input filter capacitors as close to the MCU as possible.
- Place the filtering capacitor (0.01 μF - 0.1 μF typically) as close as possible to the device pin on the application board for better ESD protection.
- Keep unused I/O pins floating, and then set them as output low in software.

11 Revision history

The following table provides a revision history for this document.

Table 20. Revision history

Rev. No.	Date	Substantial Changes
2	10/2019	Initial public release.
2.1	11/2019	• Updated the Δf_{dco_t} in the External oscillator (XOSC) and ICS characteristics. • Added note to the I_{LAT} in the ESD handling ratings. • Added Hardware design consideration.

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