MC9S12B Family

16-bit Microcontroller

1 Introduction

Designed for automotive multiplexing applications, members of the MC9S12B-Family of 16 bit Flash-based microcontrollers are fully pin compatible and enable users to choose between different memory and peripheral options for scalable designs. All MC9S12B-Family members are composed of standard on-chip peripherals including a 16-bit central processing unit (CPU12), up to 256K bytes of Flash EEPROM, 8K bytes of RAM, 2K bytes of EEPROM, two asynchronous serial communications interfaces (SCI), serial peripheral interface (SPI), an input capture/output compare timer (TIM), 16-channel, 10-bit analog-to-digital converter (ADC), an 8-channel pulse-width modulator (PWM), one CAN 2.0 A, B software compatible module (MSCAN12) and an Inter-IC Bus. System resource mapping, clock generation, interrupt control and bus interfacing are managed by the lite integration module (LIM). The MC9S12B-Family has full 16-bit data paths throughout, however, the external bus can operate in an 8-bit narrow mode so single 8-bit wide memory can be interfaced for lower cost systems. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. In addition to the I/O ports available in each module, up to 22 I/O ports are available with Wake-Up capability from STOP or WAIT mode.

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2 Features

NOTE

Not all features listed here are available in all configurations.
Additional information about D and B family inter-operability is given in:
EB386 “HCS12 D-Family Compatibility Considerations” and
EB388 “Using the HCS12 D_Family as a development platform for the HCS12 B family”

- 16-bit CPU12
  - Upward compatible with M68HC11 instruction set
  - Interrupt stacking and programmer’s model identical to M68HC11
  - 20-bit ALU
  - Instruction queue
  - Enhanced indexed addressing
- Multiplexed bus
  - Single chip or expanded
  - 16 address/16 data wide or 16 address/8 data narrow modes
  - External address space 1MByte for Data and Program space (112 pin package only)
- Wake-up interrupt inputs depending on the package option
  - 8-bit port H
  - 4-bit port J
  - 8-bit port P shared with PWM
- Memory options
  - 64K, 128K, 256K Byte Flash EEPROM
  - 1K, 2K Byte EEPROM
  - 2K, 4K and 8K Byte RAM
- Analog-to-Digital Converter
  - 16-channels for 112 Pin Package, 8 channels for 80 Pin package options, 10-bit resolution
  - External conversion trigger capability
- 1M bit per second, CAN 2.0 A, B software compatible module
  - Five receive and three transmit buffers
  - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  - Four separate interrupt channels for Rx, Tx, error and wake-up
  - Low-pass filter wake-up function
  - Loop-back for self test operation
- Input Capture/Output Compare Timer (TIM)

  - 16-bit Counter with 7-bit Prescaler
  - 8 programmable input capture or output compare channels
  - Simple PWM Mode
  - Modulo Reset of Timer Counter
  - 16-bit Pulse Accumulator
  - External Event Counting
  - Gated Time Accumulation
- 8 PWM channels with programmable period and duty cycle (7 channels on 80 Pin Packages)
  - 8-bit 8-channel or 16-bit 4-channel
  - Separate control for each pulse width and duty cycle
  - Center- or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
- Serial interfaces
  - Two asynchronous serial communications interfaces (SCI)
  - synchronous serial peripheral interface (SPI)
- Inter-IC Bus (IIC)
  - Compatible with I2C Bus standard
  - Multi-master operation
  - Software programmable for one of 256 different serial clock frequencies
- SIM (System Integration Module)
  - CRG (windowed COP watchdog, real time interrupt, clock monitor, clock generation and reset)
  - MEBI (multiplexed external bus interface)
  - MMC (memory map and interface)
  - INT (interrupt control)
  - BKP (breakpoints)
  - BDM (background debug mode)
- Clock generation
  - Phase-locked loop clock frequency multiplier
  - Limp home mode in absence of external clock
  - Clock Monitor
  - Low power 0.5 to 16 MHz crystal oscillator reference clock
- Operation frequency
  - 50MHz equivalent to 25MHz Bus Speed for single chip
  - 50MHz equivalent to 25MHz Bus Speed in expanded bus modes

- Internal 5V to 2.5V Regulator
- 112-Pin or 80-Pin LQFP package
  - I/O lines with 5V input and drive capability
  - 5VA/D converter inputs
  - Dual supply - 5V for I/O and A/D, 2.5V logic
- Development support
  - Single-wire background debug™ mode (BDM)
  - On-chip hardware breakpoints

Table 1. List of MC9S12B-Family members

Flash	RAM	EEPROM	Package	Device	CAN	SCI	SPI	IIC	A/D	PWM	TIM	I/O
256K	8K	2K	112LQFP	MC9S12B256	1	2	1	1	16ch	8ch	8ch	91
			80QFP	MC9S12B256	1	2	1	1	8ch	7ch	8ch	59
128K	4K	1K	112LQFP	MC9S12B128	1	2	1	1	16ch	8ch	8ch	91
			80QFP	MC9S12B128	1	2	1	1	8ch	7ch	8ch	59
64K	2K	1K	112LQFP	MC9S12B64	1	2	1	1	16ch	8ch	8ch	91
			80QFP	MC9S12B64	1	2	1	1	8ch	7ch	8ch	59

- Pin out explanations:
  - I/O is the sum of ports capable to act as digital input or output

    For 112 Pin Versions:

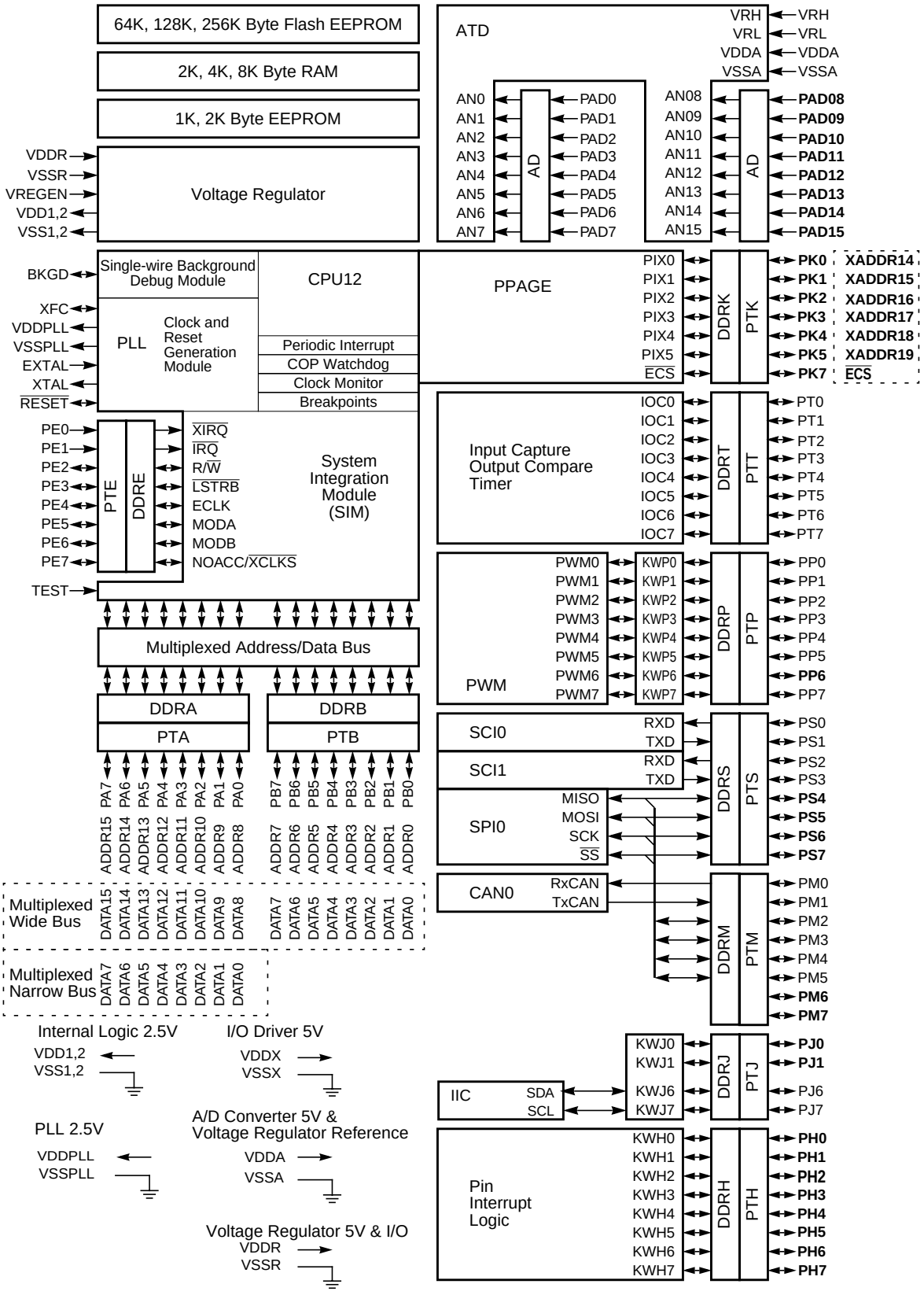
    Port A = 8, B = 8, E = 6 + 2 input only, H = 8, J = 4, K = 7, M = 8, P = 8, S = 8, T = 8, PAD = 16 input only.

    22 inputs provide Interrupt capability (H =8, P= 8, J = 4, IRQ, XIRQ

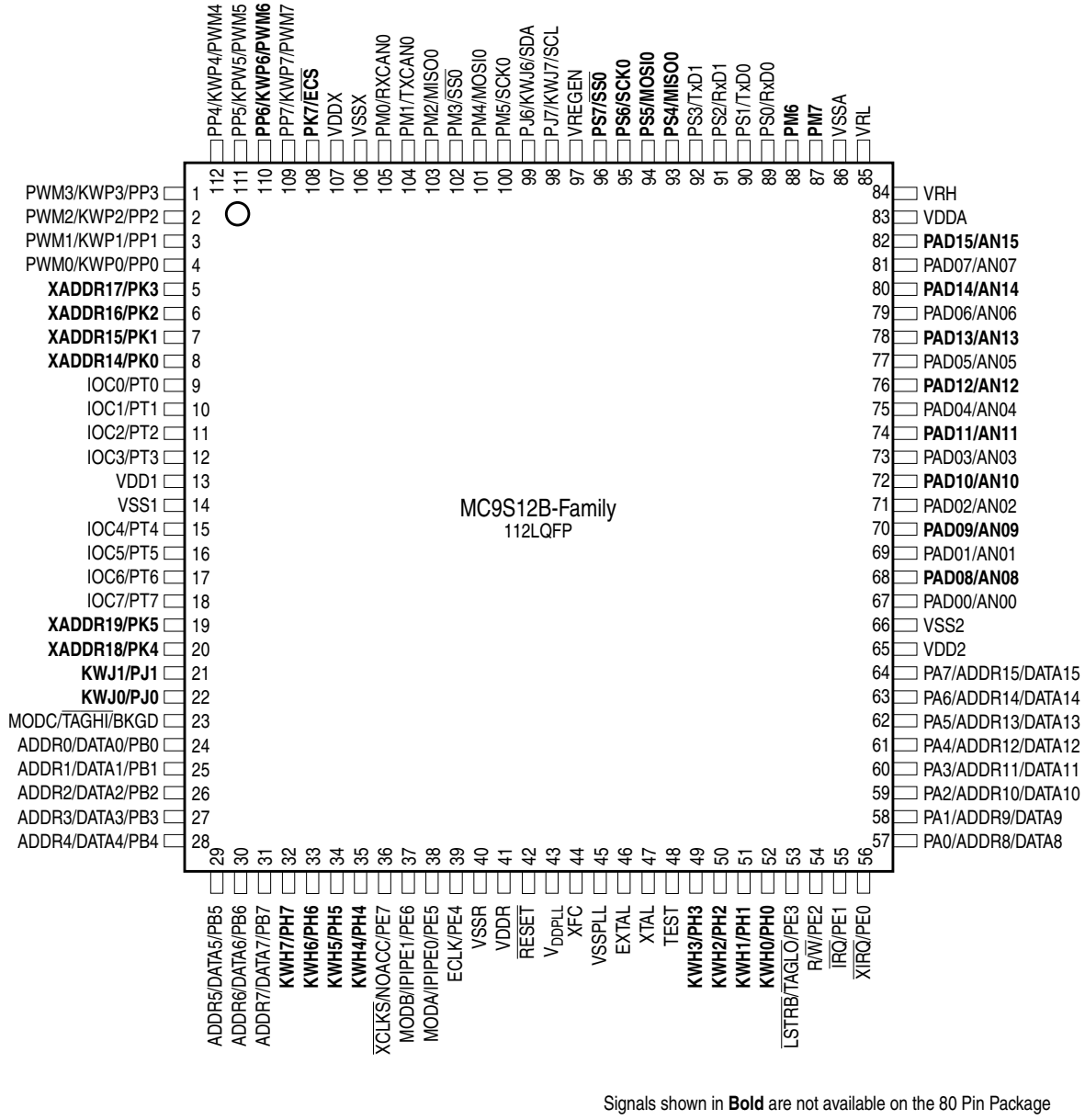
    For 80 Pin Versions:

    Port A = 8, B = 8, E = 6 + 2 input only, J = 2, M = 6, P = 7, S = 4, T = 8, PAD = 8 input only.

    11 inputs provide Interrupt capability (P= 7, J = 2, IRQ, XIRQ)



Not all functionality shown in this
Block diagram is available in all Versions!



Signals shown in **Bold** are not available on the 80 Pin Package

Figure 1. Pin assignments 112 QFP for MC9S12B-Family

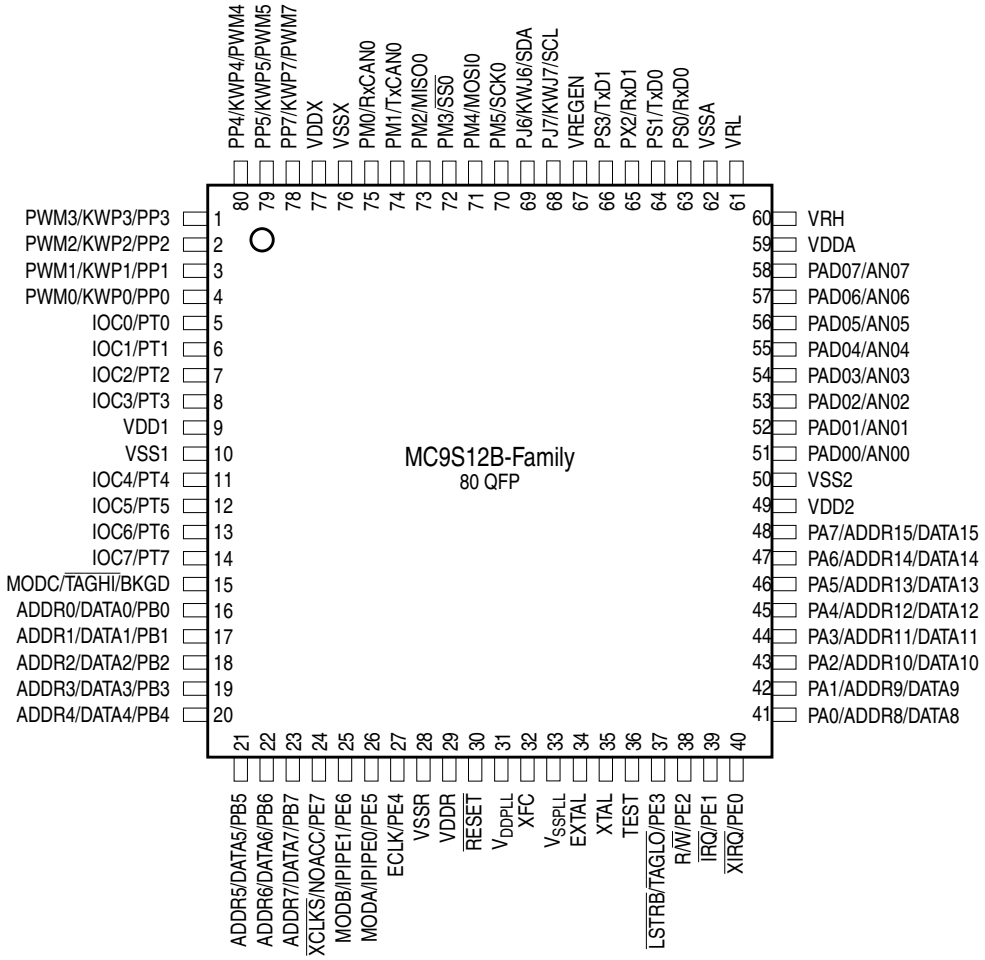
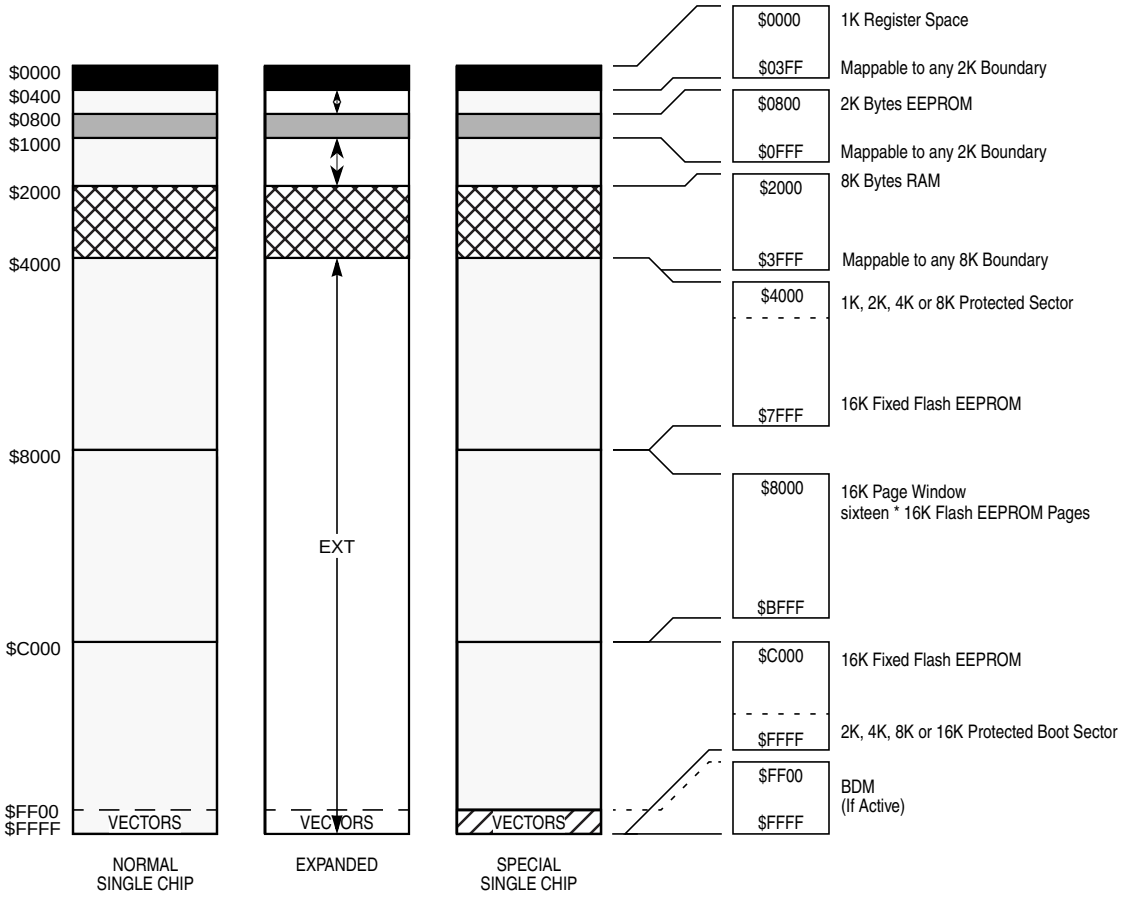


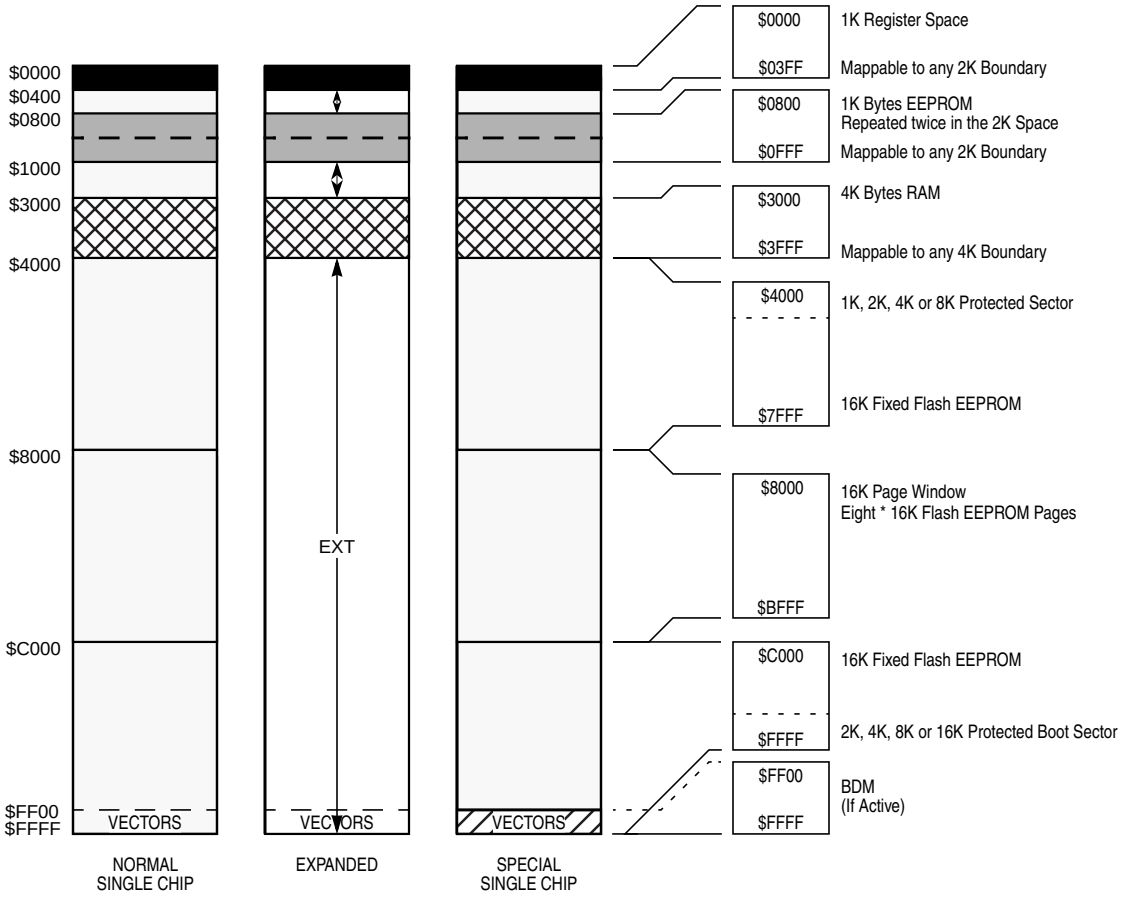
Figure 2. Pin Assignments in 80 QFP for MC9S12B-Family



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$0000 - $1FFF: 8K RAM (only 7K visible $0400 - $1FFF)
$0000 - $07FF: 2K EEPROM (not visible)
$2000 - $3FFF: 8K Flash

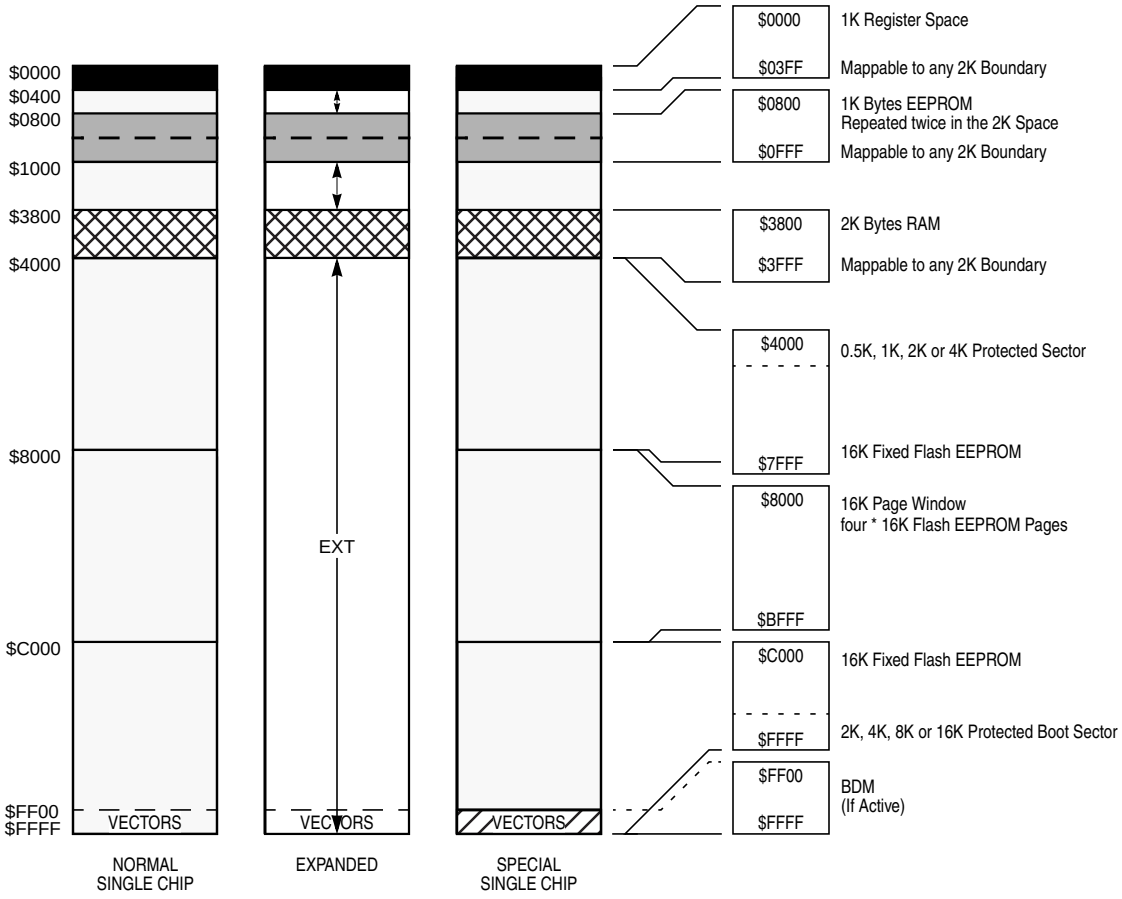
Figure 3. MC9S12Bx256 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$0000 - $0FFF: 4K RAM (only 3K visible $0400 - $0FFF)
$0000 - $07FF: 1K EEPROM (not visible)
$2000 - $3FFF: 12K Flash

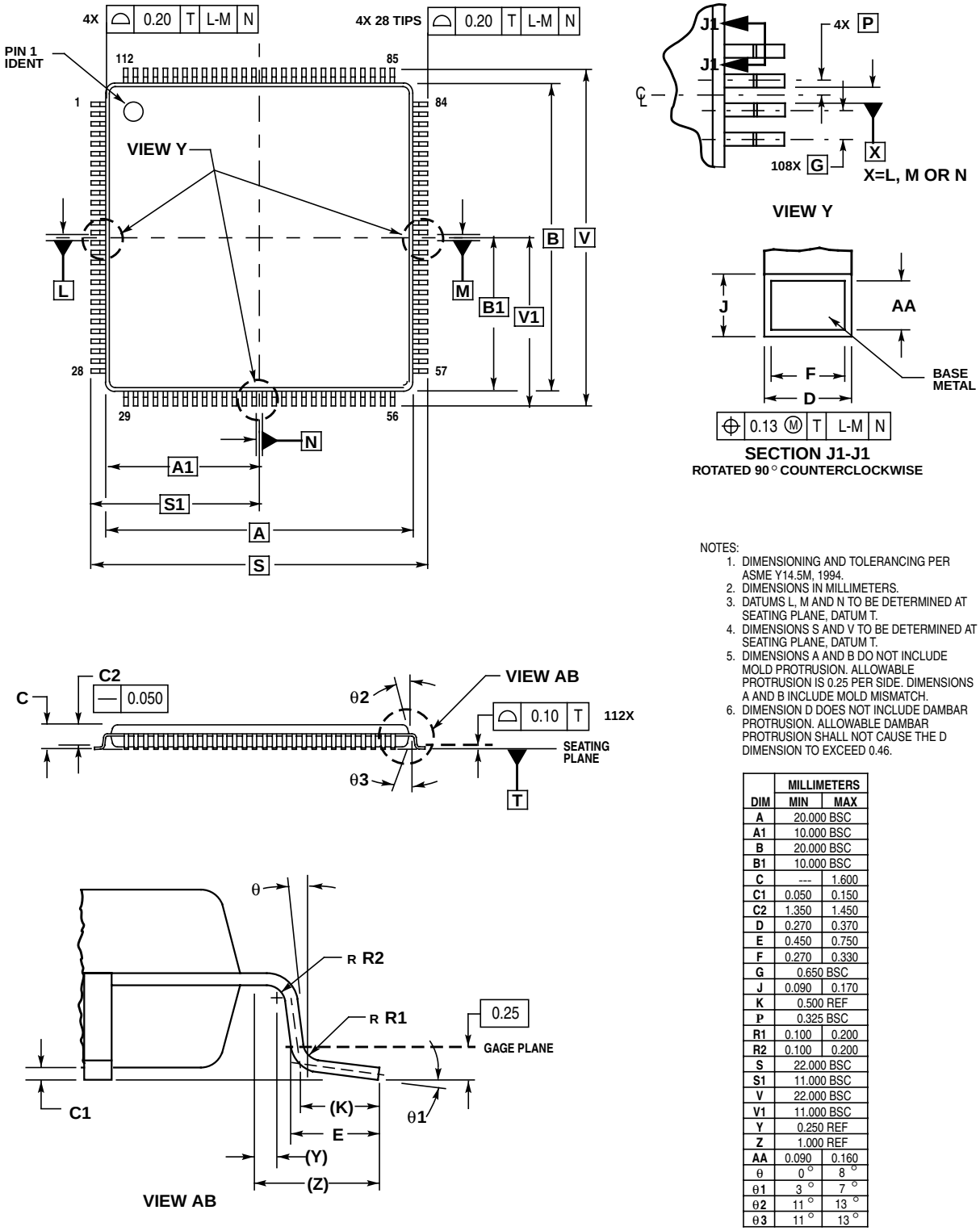
Figure 4. MC9S12Bx128 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$0800 - $0FFF: 2K RAM
$0400 - $07FF: 1K EEPROM
$2000 - $3FFF: 12K Flash

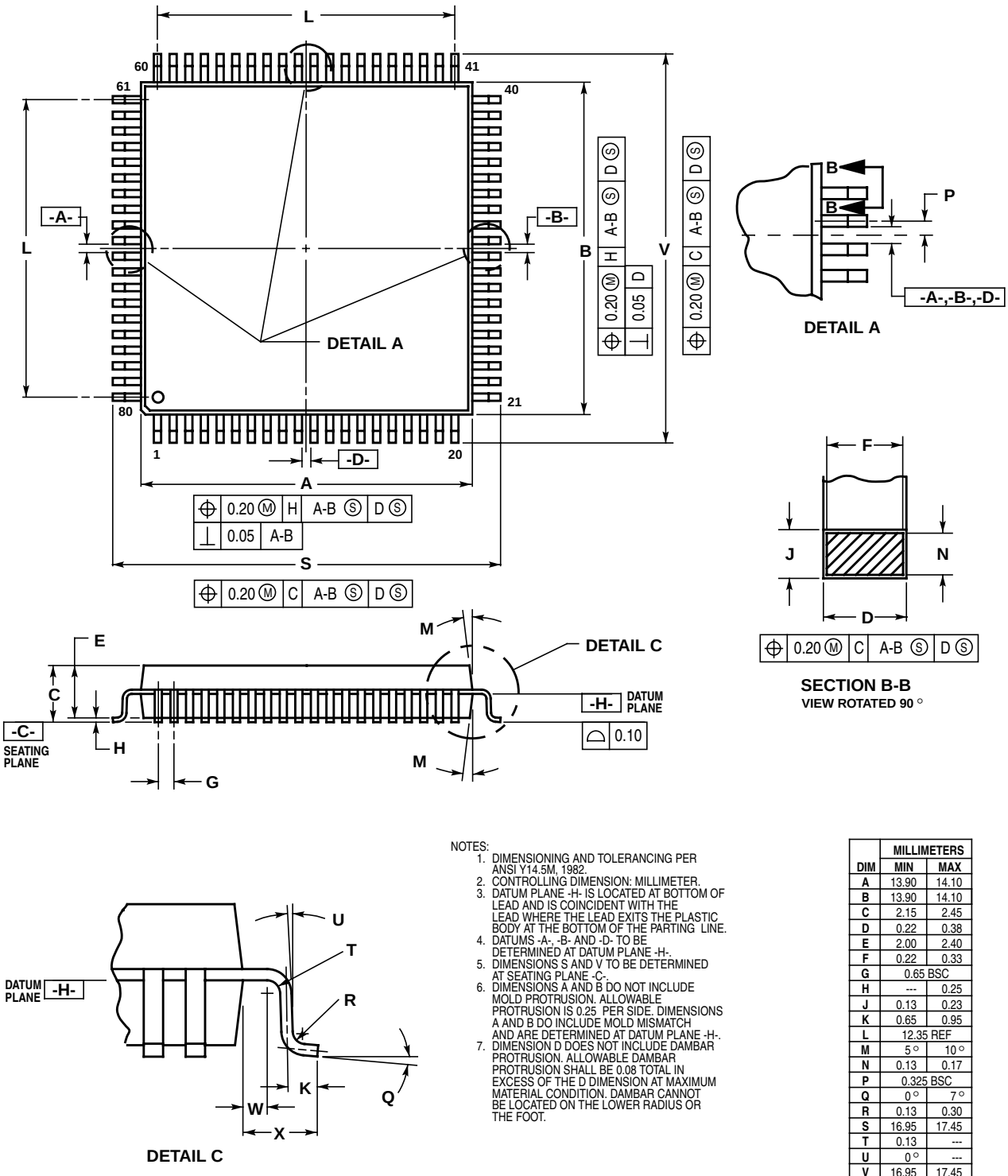
Figure 5. MC9S12Bx64 User Configurable Memory Map



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B INCLUDE MOLD MISMATCH.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.46.

	MILLIMETERS	
DIM	MIN	MAX
A	20.000 BSC	
A1	10.000 BSC	
B	20.000 BSC	
B1	10.000 BSC	
C	---	1.600
C1	0.050	0.150
C2	1.350	1.450
D	0.270	0.370
E	0.450	0.750
F	0.270	0.330
G	0.650 BSC	
J	0.090	0.170
K	0.500 REF	
P	0.325 BSC	
R1	0.100	0.200
R2	0.100	0.200
S	22.000 BSC	
S1	11.000 BSC	
V	22.000 BSC	
V1	11.000 BSC	
Y	0.250 REF	
Z	1.000 REF	
AA	0.090	0.160
θ	0°	8°
θ1	3°	7°
θ2	11°	13°
θ3	11°	13°

Figure 6. 112-pin LQFP Mechanical Dimensions (case no. 987)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS	
DIM	MIN	MAX
A	13.90	14.10
B	13.90	14.10
C	2.15	2.45
D	0.22	0.38
E	2.00	2.40
F	0.22	0.33
G	0.65 BSC	
H	---	0.25
J	0.13	0.23
K	0.65	0.95
L	12.35 REF	
M	5°	10°
N	0.13	0.17
P	0.325 BSC	
Q	0°	7°
R	0.13	0.30
S	16.95	17.45
T	0.13	---
U	0°	---
V	16.95	17.45
W	0.35	0.45
X	1.6 REF	

Figure 7. 80-pin QFP Mechanical Dimensions (case no. 841B)

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HCS12BFAMILYPP
Rev. 2.8, 7/2005

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