MCP16502

High-Performance PMIC for SAMA5DX/SAM9X6 MPUs

Features

- Input Voltage: 2.7V to 5.5V
- Four 1A Output Current Buck Channels with 100% Maximum Duty Cycle Capability
- 2 MHz Buck Channels PWM Operation
- Two Auxiliary 300 mA Low-Dropout Linear Regulators (LDOs)
- ±1% Voltage Accuracy for DDR (Buck2 Output), Core (Buck3 Output) and CPU (Buck4 Output)
- Pin-Selectable Output Voltages for Buck2: 1.2V, 1.35V, 1.8V
- MPU-Specific Built-in Default Channel Sequencing and nRSTO Assertion Delay
- Support of Hibernate, Low-Power and High-Performance Modes with DVS
- Push Button Long Press Time-out Function
- 1 MHz I^2C Interface for Programming and Diagnostics
- Low Noise, Forced PWM (FPWM) and Low I_Q, Light Load, High-Efficiency Mode Available
- I^2C-Selectable Displacement (±16.5%) of PWM Switching Frequency
- Leakage-Free Interfacing to MPU in Any Operating Condition through Optimized ESD Protection
- Less than 300 µA Low-Power Mode Typical Quiescent Current Bucks and LDO1 On, No Load
- 10 µA Maximum Shutdown Current (V_{IN} = 4.5V, T_J = +105°C)
- Cost and Size-Optimized BOM
- Thermal Shutdown and Current Limit Protection
- User-Programmable Overcurrent Fault Response
- 32-Pin 5 mm × 5 mm VQFN Package
- -40°C to +125°C Junction Temperature Range

Applications

- High-Performance MPUs Power Supply Solutions
- µC/µP, FPGA and DSP Power

Description

The MCP16502 is an optimally integrated PMIC, compatible with Microchip's EMPUs (Embedded Microprocessor Units), requiring Dynamic Voltage Scaling (DVS) with the use of High-Performance mode (HPM). It is compatible with SAMA5DX and SAM9X6 MPUs, which are supported by dedicated device variants that optimize the solution BOM.

The MCP16502 integrates four DC-DC Buck regulators and two auxiliary LDOs, and provides a comprehensive interface to the MPU, which includes an interrupt flag and a 1 MHz I^2C interface.

All Buck channels can support loads up to 1A and are 100% duty cycle-capable.

Two 300 mA LDOs are provided such that sensitive analog loads can be supported.

The DDR memory voltage (Buck2 output) is selectable by means of a 3-state input pin. This method allows greater precision in the output voltage setting by eliminating inaccuracies due to external feedback resistors, while minimizing external component count. The voltage selection set allows easy migration across different generations of memory.

The default power channel sequencing is built-in according to the requirements of the MPU. A dedicated pin (LPM) facilitates the transition to Low-Power modes and the implementation of Backup mode with DDR in self-refresh (Hibernate mode).

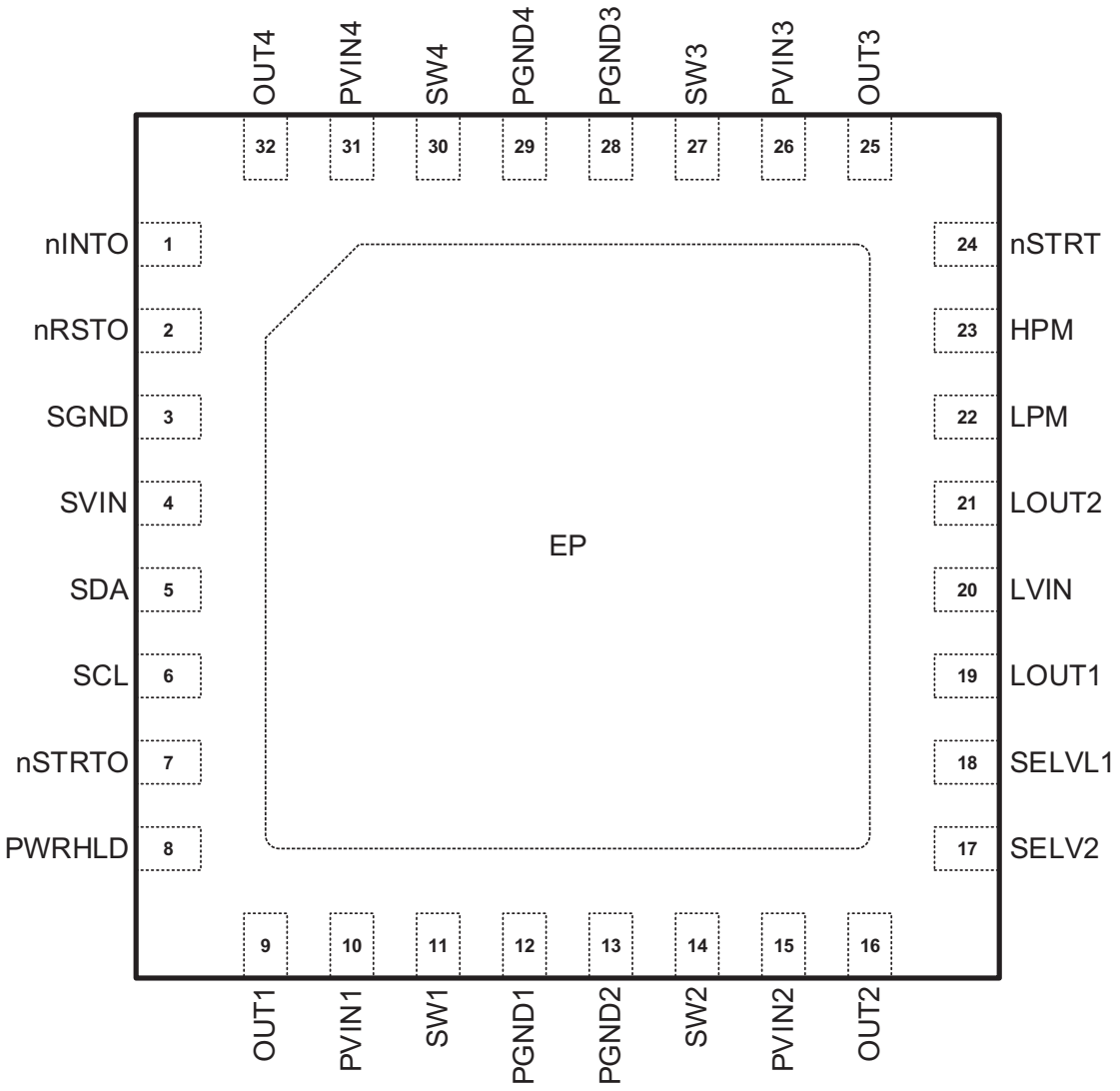
The MCP16502 features a low no-load operational quiescent current and it draws less than 10 µA in full shutdown.

Active discharge resistors are provided on each output. All Buck channels support safe start-up into pre-biased outputs.

The MCP16502 is available in a 32-pin 5 mm x 5 mm VQFN package with an operating junction temperature range from -40°C to +125°C.

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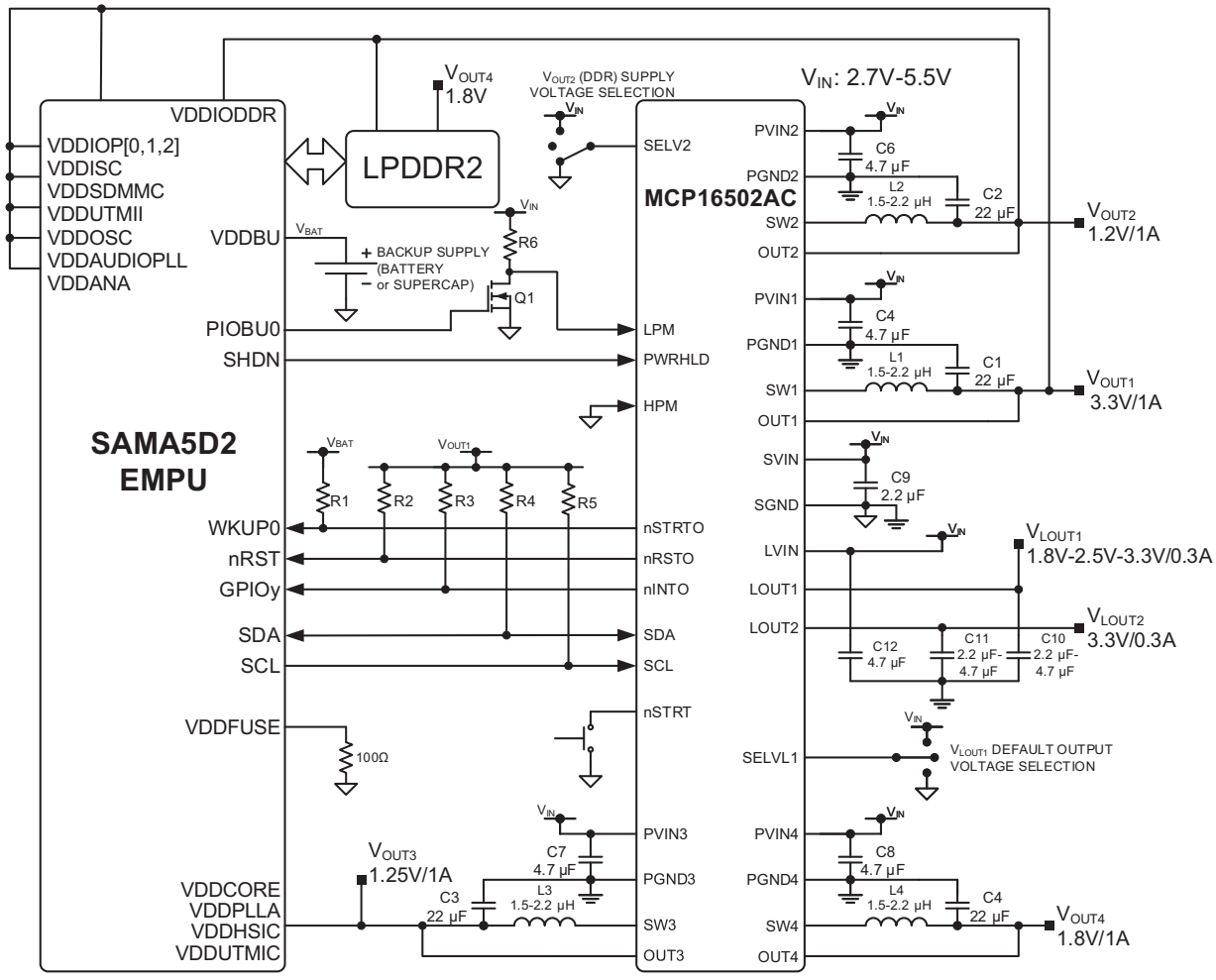
Package Types



32-Pin 5 mm x 5 mm VQFN – Top View

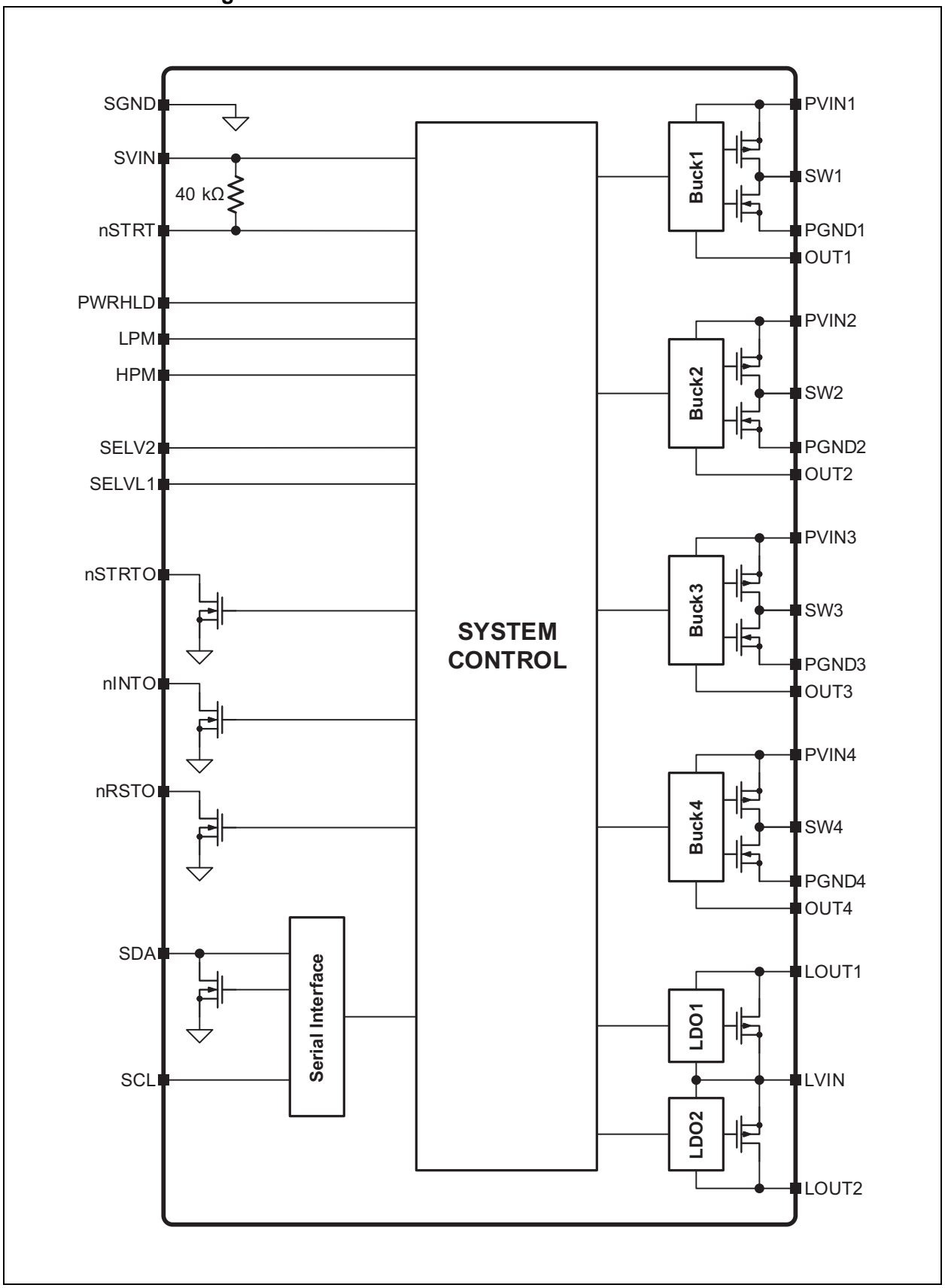
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Typical Application Circuit



Application Schematic of MCP16502AC with SAMA5D2 and LPDDR2 (Wireless SOM Application)

Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

SVIN to SGND ..... -0.3V to +6V
Power Supply Voltage Pins PVINx to PGNDx ..... -0.3V to +6V
Power Supply Voltage Pins PVINx to SVIN ..... -0.3V to +0.3V
OUTx Sense Pins to SGND ..... -0.3V to +6V
LVIN to SGND ..... -0.3V to V_{SVIN} + 0.3V
Output Switch Voltage SWx to PGNDx ..... -0.3V to V_{PVINx} + 0.3V
PGNDx to SGND ..... -0.3V to +0.3V
nSTRT, SELV2, SELVL1 to SGND ..... -0.3V to V_{SVIN} + 0.3V
SDA, SCL, LPM, HPM, PWRHLD, nRSTO, nSTRTO, nINTO to SGND ..... -0.3V to +6V
Maximum Junction Temperature ..... 150°C
Storage Temperature ..... -65°C to +150°C
ESD Protection on All Pins:
HBM ..... 2 kV
MM 200V
CDM 1000V

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise specified: $T_A = T_J$ = +25°C; V_{IN} = SVIN = PVINx = LVIN = 5V; L1 = L2 = L3 = L4 = 2.2 µH; C_{OUT1}, C_{OUT2}, C_{OUT3}, C_{OUT4} = 22 µF. **Boldface** type applies for junction temperatures T_J of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
System Input Supply						
Supply Voltage Range	V_{IN}	**2.7**	—	**5.5**	V	
Undervoltage Lockout Threshold	V_{UVLO_TH}	**2.4**	2.55	**2.7**	V	Turn-on
Undervoltage Lockout Hysteresis	V_{UVLO_HYS}	—	125		mV	
Shutdown (Off) Current	I_{SHDN}	—	7	**11**	µA	PWRHLD = LPM = HPM = 0, nSTRT, nRSTO, nSTRTO, nINTO floating, V_{IN} = 5.5V
	I_{SHDN_105} (1)	—	6	10	µA	PWRHLD = LPM = HPM = 0, nSTRT, nRSTO, nSTRTO, nINTO floating, V_{IN} = 4.5V, T_J = -40°C to +105°C
Hibernate Mode Non-Switching Quiescent Current	I_{QNS_HIB}	—	120	**150**	µA	I_{OUT2} = 0 mA, Buck2 on, all other channels off, $V_{OUT2} > V_{OUT2_NOM}$, LPM = 1, PWRHLD = HPM = 0
Hibernate Mode Operational Quiescent Current (Switching, One Buck Channel On) **(Note 2)**	I_{QOP_HIB1}	—	120	—	µA	I_{OUT2} = 0 mA, Buck2 on (V_{OUT2} = 1.2V), all other channels off, LPM = 1, PWRHLD = HPM = 0

Note 1: Maximum limit for T_J = -40°C to +105°C based on characterization data.
2: Not production tested.
3: Typical value from bench characterization, maximum value production tested.
4: Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

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AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified: $T_A = T_J = +25°C$; V_{IN} = SVIN = PVINx = LVIN = 5V; L1 = L2 = L3 = L4 = 2.2 µH; C_{OUT1}, C_{OUT2},, C_{OUT3}, C_{OUT4} = 22 µF. **Boldface** type applies for junction temperatures T_J of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Hibernate Mode Operational Quiescent Current (Switching, Two Buck Channels On) **(Note 2)**	I_{QOP_HIB2}	—	165	—	µA	I_{OUT2} = I_{OUT4} = 0 mA, Buck2 and Buck4 on (V_{OUT2} = 1.2V, V_{OUT4} = 1.8V), all other channels off, LPM = 1, PWRHLD = HPM = 0
Low-Power Mode Operational Quiescent Current (Switching) **(Note 2)**	I_{QOP_LPM}	—	290	—	µA	I_{OUTx} = 0 mA, all channels on except LDO2, default settings, PWRHLD = LPM = 1, HPM = 0
Active Mode Operational Quiescent Current (Switching)**(Note 2)**	I_{QOP_ACT}	—	16	—	mA	I_{OUTx} = 0 mA, all channels enabled, default settings, PWRHLD = 1, LPM = HPM = 0
High-Performance Active Mode Operational Quiescent Current (Switching) **(Note 2)**	I_{QOP_HPM}	—	16	—	mA	I_{OUTx} = 0 mA, all channels enabled, default settings, PWRHLD = HPM = 1, LPM = 0
Time Base						
Time Base Accuracy	ACC_TB	**-10**	—	**+10**	%	FSD[1:0] = 00, 01
Thermal Protection and Warning						
Overtemperature Shutdown Threshold **(Note 2)**	T_{TSD}	—	160	—	°C	Bit TSD to '1'
Overtemperature Shutdown Hysteresis **(Note 2)**	T_{TSD_HYS}	—	20	—	°C	Bit TSD to '0'
Overtemperature Warning Threshold **(Note 2)**	T_{TWR}	—	135	—	°C	Bit TWR to '1'
Overtemperature Warning Hysteresis **(Note 2)**	T_{TWR_HYS}	—	10	—	°C	Bit TWR to '0'
Buck1						
Input Operating Voltage Range	V_{PVIN1}	**2.7**	—	**5.5**	V	
Output Voltage Range	V_{OUT1}	1.2	—	3.7	V	50 mV steps
Output Voltage Step	V_{step}	—	50	—	mV	
PVIN1 Shutdown Current	I_{PVIN1_SHDN}	—	0.05	**2**	µA	Regulator disabled, V_{PVIN1} = 5V
Operational Quiescent Current, Auto-PFM, Default Setting **(Note 2)**	I_{QOP_PFM1}	—	45	—	µA	I_{OUT1} = 0 mA, Auto-PFM, PWRHLD = LPM = 1, HPM = 0, B1HCEN = 0 (default), ΔI_Q for Buck1 activated
Operational Quiescent Current, Auto-PFM + HCM **(Note 2)**	I_{QOP_HCM}	—	47	—	µA	I_{OUT1} = 0 mA, Auto-PFM, PWRHLD = LPM = 1, HPM = 0, B1HCEN = 1, ΔI_Q for Buck1 activated
Output Voltage Accuracy, FPWM	ACC_OUT_{PWM1}	**-2**	—	**+2**	%	I_{OUT1} = 0 mA
Output Voltage Accuracy, Auto-PFM	ACC_OUT_{PFM1}	**-2**	—	**+2**	%	I_{OUT1} = 0 mA, B1HCEN = 0

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AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified: $T_A = T_J = +25°C$; V_{IN} = SVIN = PVINx = LVIN = 5V; L1 = L2 = L3 = L4 = 2.2 µH; C_{OUT1}, C_{OUT2}, C_{OUT3}, C_{OUT4} = 22 µF. **Boldface** type applies for junction temperatures T_J of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output Voltage Line Regulation (Note 2)	$LINE_REG_{PWM1}$	—	0.03	—	%	I_{OUT1} = 0 mA, FPWM, V_{IN} = PVIN1 = SVIN = 3.6V to 5.5V
	$LINE_REG_{PFM1}$	—	0.07	—		I_{OUT1} = 0 mA, Auto-PFM, V_{IN} = PVIN1 = SVIN = 3.6V to 5.5V
Output Voltage Load Regulation (Note 2)	$LOAD_REG_{PWM1}$	—	0.3	—	%	I_{OUT1} = 0A to 1A, FPWM
	$LOAD_REG_{PFM1}$	—	0.5	—	%	I_{OUT1} = 0A to 1A, Auto-PFM
Hysteretic Control Mode Upper Regulation Threshold, Auto-PFM	HCM_TH	**1.7**	2.9	**4.3**	%	I_{OUT1} = 0 mA, PWRHLD = LPM = 1, HPM = 0, B1HCEN = 1, SVIN = PVIN1 = 1.06, V_{OUT1_NOM}, OUT1 rising, % of V_{OUT1_NOM}
Hysteretic Control Mode Disable Threshold, Auto-PFM	HCM_DIS	—	11.1	—	%	I_{OUT1} = 0 mA, PWRHLD = LPM = 1, HPM = 0, B1HCEN = 1, SVIN = PVIN1 rising, % of V_{OUT1_NOM}
Hysteretic Control Mode Enable Threshold, Auto-PFM	HCM_EN	**5**	9	**13**	%	I_{OUT1} = 0 mA, PWRHLD = LPM = 1, HPM = 0, B1HCEN = 1, SVIN = PVIN1 falling, % of V_{OUT1_NOM}
Switching Frequency	f_{sw}	**1.8**	2	**2.2**	MHz	FPWM, FSD[1:0] = 00, 01
Switching Frequency Displacement	FSD_10	—	-16.5	—	%	FPWM, FSD[1:0] = 10
	FSD_11	—	+16.5	—	%	FPWM, FSD[1:0] = 11
Maximum Duty Cycle	D_{MAX}	100	—	—	%	Functionality test
Minimum On Time	T_{ON_MIN1}	—	35	—	ns	FPWM
High-Side Switch On-Resistance	R_{DsonP1}	—	140	160	mΩ	PVIN1 = SVIN = 3.6V
Low-Side Switch On-Resistance	R_{DsonN1}	—	120	140	mΩ	PVIN1 = SVIN = 3.6V
POK (Power OK) Threshold	POK_TH1	**90**	92.5	**95**	%	OUT1 rising, % of V_{OUT1_NOM}
POK Hysteresis	POK_HYS1	—	4	—	%	OUT1 falling, % of V_{OUT1_NOM}
Start-up POK Bypass Threshold	$V_{POKB_TH_B1}$	**360**	400	**440**	mV	PVIN1 – OUT1, OUT1 rising, PVIN1 = 3.0V, V_{OUT1_NOM} = 3.3V
Start-up POK Bypass Threshold Hysteresis	$V_{POKB_HYS_B1}$	—	50	—	mV	OUT1 falling, PVIN1 = 3.0V
Soft Start Rate (Switching Frequency Clock Cycles per DAC Step)	SSR_00	—	16	—	cycles/ step	SSR[1:0] = 00 (default)
	SSR_01	—	32	—		SSR[1:0] = 01
	SSR_10	—	48	—		SSR[1:0] = 10
	SSR_11	—	64	—		SSR[1:0] = 11
Dynamic Voltage Scaling Rate (Switching Frequency Clock Cycles Per DAC Step)	DVSR_00		16		cycles/ step	DVSR[1:0] = 00 (default)
	DVSR_01		32			DVSR[1:0] = 01
	DVSR_10		48			DVSR[1:0] = 10
	DVSR_11		64			DVSR[1:0] = 11
High-Side Peak Current Limit (Cycle by Cycle)	I_{LIM_HS1}	**1.2**	1.8	**2.4**	A	

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AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified: $T_A = T_J = +25°C$; V_{IN} = SVIN = PVINx = LVIN = 5V; L1 = L2 = L3 = L4 = 2.2 µH; C_{OUT1}, C_{OUT2}, C_{OUT3}, C_{OUT4} = 22 µF. **Boldface** type applies for junction temperatures T_J of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Current Limit Frequency Foldback V_{OUT1} Threshold	V_{TH_FFB1}	—	500	—	mV	
Hiccup Mode Short-Circuit Protection Wait Time	t_{HICCUP}	—	3x Soft Start Time	—		
Low-Side Negative Peak Current Limit (FPWM)	I_{LIM_NEG1}	-1.4	-1	-0.8	A	
Zero Current Detection Threshold	I_{ZCD1}	0	50	110	mA	
Active Discharge Resistance	R_{DISCH_OUT1}	—	25	—	Ω	DISCH = 1, enabled when regulator is disabled
Buck2, Buck3, Buck4						
Input Operating Voltage Range	V_{PVINx}	**2.7**	—	**5.5**	V	
Output Voltage Range	V_{OUTx}	0.6	—	1.85	V	25 mV steps
Output Voltage Step	V_{step}	—	25	—	mV	
PVINx Shutdown Current	I_{PVINx_SHDN}	—	0.05	**2**	µA	Regulator disabled, PVINx = 5V
Operational Quiescent Current, Auto-PFM (**Note 2**)	I_{QOP_PFMx}	—	45	—	µA	I_{OUTx} = 0 mA, Auto-PFM, PWRHLD = LPM = 1, HPM = 0, ΔI_Q for one Buck activated
Output Voltage Accuracy, FPWM	ACC_OUT_{PWMx}	**-1**	—	**+1**	%	I_{OUTx} = 0 mA, 0.9V ≤ V_{OUTx} ≤ 1.3V
		-1.5	—	**+1.5**		I_{OUTx} = 0 mA, V_{OUTx} < 0.9V or V_{OUTx} > 1.3V
Output Voltage Accuracy, Auto-PFM	ACC_OUT_{PFMx}	**-1**	—	**+1**	%	I_{OUTx} = 0 mA, 0.9V ≤ V_{OUTx} ≤ 1.3V
		-1.5	—	**+1.5**		I_{OUTx} = 0 mA, V_{OUTx} < 0.9V or V_{OUTx} > 1.3V
Output Voltage Line Regulation (**Note 2**)	$LINE_REG_{PWMx}$	—	0.03	—	%	I_{OUT1} = 0 mA, FPWM, V_{IN} = PVIN1 = SVIN = 3.6V to 5.5V
	$LINE_REG_{PFMx}$	—	0.07	—		I_{OUT1} = 0 mA, Auto-PFM, V_{IN} = PVIN1 = SVIN = 3.6V to 5.5V
Output Voltage Load Regulation (**Note 2**)	$LOAD_REG_{PWMx}$	—	0.3	—	%	I_{OUTx} = 0A to 1A, FPWM
	$LOAD_REG_{PFMx}$	—	0.5	—		I_{OUTx} = 0A to 1A, Auto-PFM
Switching Frequency	f_{sw}	**1.8**	2	**2.2**	MHz	FPWM, FSD[1:0] = 00, 01
Switching Frequency Displacement	FSD_10	—	-16.5	—	%	FPWM, FSD[1:0] = 10
	FSD_11	—	16.5	—	%	FPWM, FSD[1:0] = 11
Maximum Duty Cycle	D_{MAX}	100	—	—	%	Functionality test
Minimum On Time	T_{ON_MINx}	—	35	—	ns	FPWM
High-Side Switch On-Resistance	R_{DSonPx}	—	140	160	mΩ	PVINx = SVIN = 3.6V
Low-Side Switch On-Resistance	R_{DSonNx}	—	120	140	mΩ	PVINx = SVIN = 3.6V
POK (Power OK) Threshold	POK_THx	**90**	92.5	**95**	%	OUTx rising, % of $V_{OUTx(NOM)}$
POK Hysteresis	POK_HYSx	—	4	—	%	OUTx falling, % of $V_{OUTx(NOM)}$

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AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified: $T_A = T_J = +25°C$; V_{IN} = SVIN = PVINx = LVIN = 5V; L1 = L2 = L3 = L4 = 2.2 µH; C_{OUT1}, C_{OUT2}, C_{OUT3}, C_{OUT4} = 22 µF. **Boldface** type applies for junction temperatures T_J of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Soft Start Rate (Switching Frequency Clock Cycles per DAC Step)	SSR_00	—	16	—	cycles/ step	SSR[1:0] = 00 (default)
	SSR_01	—	32	—		SSR[1:0] = 01
	SSR_10	—	48	—		SSR[1:0] = 10
	SSR_11	—	64	—		SSR[1:0] = 11
Dynamic Voltage Scaling Rate (Switching Frequency Clock Cycles per DAC Step)	DVSR_00	—	16	—	cycles/ step	DVSR[1:0] = 00 (default)
	DVSR_01	—	32	—		DVSR[1:0] = 01
	DVSR_10	—	48	—		DVSR[1:0] = 10
	DVSR_11	—	64	—		DVSR[1:0] = 11
High-Side Peak Current Limit (Cycle-by-Cycle)	I_{LIM_HSx}	**1.2**	1.8	**2.4**	A	
Current Limit Frequency Foldback V_{OUTx} Threshold	V_{TH_FFBx}	—	500	—	mV	
Hiccup Mode Short-Circuit Protection Wait Time	t_{HICCUP}	—	3x Soft Start Time	—		
Low-Side Negative Peak Current Limit (FPWM)	I_{LIM_NEGx}	-1.4	-1	-0.8	A	
Zero Current Detection Threshold	I_{ZCDx}	0	33	110	mA	
Active Discharge Resistance	R_{DISCH_OUTx}	—	25	—	Ω	DISCH = 1, enabled when regulator is disabled
LDO1, LDO2						
Input Operating Voltage Range	V_{LVIN}	**2.7**	—	**5.5**	V	
Output Voltage Range	V_{LOUTx}	1.2	—	3.7	V	
Output Voltage Step	V_{step}	—	50	—	mV	
Stable Output Capacitor Range (**Note 2**)	C_{LOUTx}	2.2	—	20	µF	$I_{LOUT1,2}$ ≤ 150 mA – application requirement
		4.7	—	20	µF	$I_{LOUT1,2}$ ≤ 300 mA – application requirement
LVIN Shutdown Current	I_{LVIN_SHDN}	—	—	**2**	µA	LDOs disabled, LVIN = 5V
Operational Quiescent Current	I_{LVIN_Qx}	—	40	—	µA	$I_{LOUT1,2}$ = 0 mA, one LDO block
Output Voltage Accuracy	ACC_LOUTx	**-3**	—	**+3**	%	LVIN = SVIN = 3.6V, $I_{LOUT1,2}$ = 0.1 mA
Dropout Voltage (**Note 3**)	V_{DOx}	—	170	**500**	mV	$I_{LOUT1,2}$ = 300 mA
Output Voltage Line Regulation	LINE_REGx	—	0.024	—	%	LVIN = SVIN = 3.6V to 5.5V, $I_{LOUT1,2}$ = 0.1 mA
Output Voltage Load Regulation	LOAD_REGx	—	0.3	—	%	$I_{LOUT1,2}$ = 0.1 mA to 300 mA

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AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified: $T_A = T_J = +25°C$; V_{IN} = SVIN = PVINx = LVIN = 5V; L1 = L2 = L3 = L4 = 2.2 µH; C_{OUT1}, C_{OUT2},, C_{OUT3}, C_{OUT4} = 22 µF. **Boldface** type applies for junction temperatures T_J of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
PSRR (Note 2)	PSRRx	—	63	—	dB	f = 1 kHz, I_{OUT} = 20 mA, $V_{LOUT1,2}$ = 1.8V, SVIN and LVIN modulated
		—	63	—	dB	f = 1 kHz, I_{OUT} = 20 mA, $V_{LOUT1,2}$ = 1.8V, SVIN = 5V, LVIN modulated
		—	46	—	dB	f = 10 kHz, I_{OUT} = 20 mA, $V_{LOUT1,2}$ = 1.8V, SVIN and LVIN modulated
		—	47	—	dB	f = 10 kHz, I_{OUT} = 20 mA, $V_{LOUT1,2}$ = 1.8V, SVIN = 5V, LVIN modulated
POK (Power OK) Threshold	POK_THL	**90**	92.3	**95**	%	LOUT1,2 rising, % of $V_{LOUT1,2(NOM)}$
POK Hysteresis	POK_HYSL	—	4	—	%	LOUT1,2 falling, % of $V_{LOUT1,2(NOM)}$
Start-up POK Bypass Threshold	$V_{POKB_TH_Lx}$	**400**	500	**600**	mV	LVIN – LOUTx, LOUTx rising, LVIN = 3.0V, V_{LOUTx_NOM} = 3.3V
Start-up POK Bypass Threshold Hysteresis (Note 2)	$V_{POKB_HYS_Lx}$	—	50	—	mV	LOUTx falling, LVIN = 3.0V
Soft Start Rate (Switching Frequency Clock Cycles per DAC Step)	SSR_00	—	16	—	cycles/ step	SSR[1:0] = 00 (default)
	SSR_01	—	32	—		SSR[1:0] = 01
	SSR_10	—	48	—		SSR[1:0] = 10
	SSR_11	—	64	—		SSR[1:0] = 11
Dynamic Voltage Scaling Rate (Switching Frequency Clock Cycles per DAC Step) – Rising Only	DVSR_00	—	16	—	cycles/ step	DVSR[1:0] = 00 (default)
	DVSR_01	—	32	—		DVSR[1:0] = 01
	DVSR_10	—	48	—		DVSR[1:0] = 10
	DVSR_11	—	64	—		DVSR[1:0] = 11
Current Limit	I_{LIM_LOUTx}	**310**	420	**550**	mA	SVIN = LVIN = 4.5V, $V_{LOUT1,2}$ = 80% of nominal
Active Discharge Resistance	R_{DISCH_LOUTx}	—	25	—	Ω	DISCH = 1, enabled when regulator is disabled and during negative DVS
nSTRT Input						
Logic High Input Voltage, V_{IH}	V_{IH_nSTRT}	**0.66 V_{SVIN}**	—	—	V	SVIN = 3.6V-5.5V
Logic Low Input Voltage, V_{IL}	V_{IL_nSTRT}	—	—	**0.36 V_{SVIN}**	V	SVIN = 3.6V-5.5V
Pull-up Resistance	R_{PU_nSTRT}	—	40	—	kΩ	
nSTRT Deglitch Time	t_{DT_nSTRT}	—	10	—	µs	Falling edge of nSTRT pin

Note 1: Maximum limit for T_J = -40°C to +105°C based on characterization data.

2: Not production tested.

3: Typical value from bench characterization, maximum value production tested.

4: Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

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AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified: $T_A = T_J = +25°C$; V_{IN} = SVIN = PVINx = LVIN = 5V; L1 = L2 = L3 = L4 = 2.2 µH; C_{OUT1}, C_{OUT2}, C_{OUT3}, C_{OUT4} = 22 µF. **Boldface** type applies for junction temperatures T_J of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
SELV2, SELVL1 Three-State Inputs (x = 2, L1)						
High State Threshold Voltage, V_{IHT}	V_{IHT_SELVx}	**V_{SVIN} – 0.9V**	—	**V_{SVIN} – 0.4V**	V	
Low State Threshold Voltage, V_{ILT}	V_{ILT_SELVx}	**0.5**	—	**1.0**	V	
Input Leakage Current High	I_{lkgH_SELVx}	—	0.01	**1**	µA	SELVx = SVIN – 0.4V
Input Leakage Current Low	I_{lkgL_SELVx}	**-1**	0.01	—	µA	SELVx = 0.4V
PWRHLD, LPM, HPM Logic Inputs (x= PWRHLD, LPM, HPM)						
Logic High Input Voltage, V_{IH}	V_{IH_x}	**1.5**	—	—	V	SVIN = 3.6V-5.5V
Logic Low Input Voltage, V_{IL}	V_{IL_x}	—	—	**0.4**	V	SVIN = 3.6V-5.5V
Input Leakage Current	I_{lkg_x}	**-1**	—	**1**	µA	
Deglitch Time	t_{DT_x}	—	10	—	µs	
nRSTO, nSTRTO, nINTO Logic Outputs (x = nRSTO, nSTRTO, nINTO)						
Output Voltage Low, V_{OL}	V_{OL_x}	—	—	**0.4**	V	SVIN = 3.6V-5.5V, I_{OL} = 2 mA
Leakage Current	I_{lkg_x}	—	—	**1**	µA	5.5V applied, output driver off
SDA, SCL I^2C Interface Pins (x = SDA, SCL)						
SCL, SDA Logic High Input Voltage, V_{IH}	V_{IH_x}	**1.5**	—	—	V	SVIN = 3.6V-5.5V
SCL, SDA Logic Low Input Voltage, V_{IL}	V_{IL_x}	—	—	**0.4**	V	SVIN = 3.6V-5.5V
Hysteresis of Schmitt Trigger Inputs	V_{hys_x}	—	0.2	—	V	SVIN = 3.6V-5.5V
SDA, SCL Leakage Current	I_{lkg_x}	—	—	**1**	µA	SDA driver off, V_{SDA} = 5.5V, V_{SCL} = 5.5V
SDA Output Voltage Low, V_{OL}	V_{OL}	—	—	**0.4**	V	SVIN = 3.6V-5.5V, I_{OL} = 20 mA
Maximum SCL Clock Frequency	f_{SCL}	—	1	—	MHz	Functional test only
Maximum Pulse Width of Input Spikes that Must be Suppressed **(Notes 2, 4)**	t_{SP}	—	50	—	ns	Functional test only

Note 1: Maximum limit for T_J = -40°C to +105°C based on characterization data.
2: Not production tested.
3: Typical value from bench characterization, maximum value production tested.
4: Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

TEMPERATURE SPECIFICATIONS(1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	-40	—	+125	°C	Steady state
Maximum Junction Temperature	T_{J_MAX}	—	—	+150	°C	Transient
Package Thermal Resistance	θ_{JA}	—	25.8	—	°C/W	

Note 1: $T_A = +25°C$; V_{IN} = SVIN = PVINx = LVIN = 5V; unless otherwise specified.
Bold values indicate -40°C ≤ T_J ≤ +125°C.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

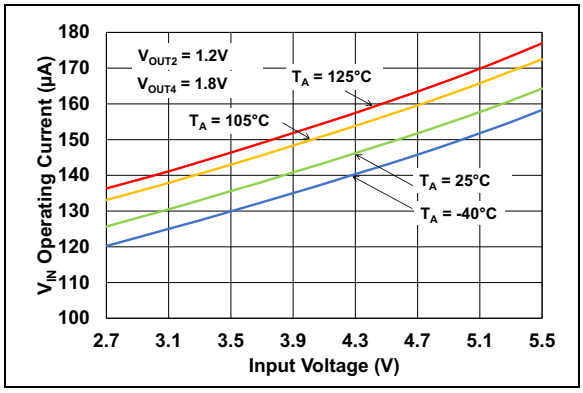


FIGURE 2-1: *V_{IN} Operating Current vs. Input Voltage and Temperature – Hibernate Mode (LPM = High, PWRHLD = HPM = Low).*

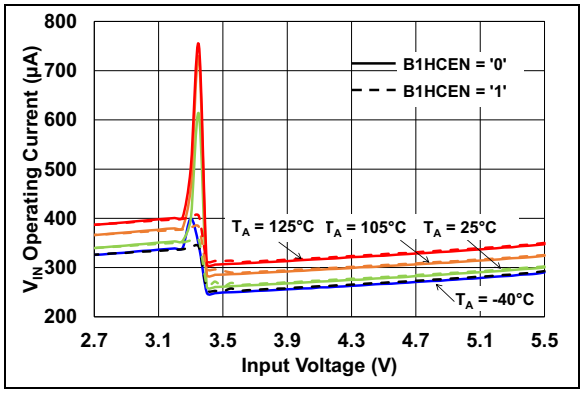


FIGURE 2-2: *V_{IN} Quiescent Current vs. Input Voltage and Temperature – Low-Power Mode (LPM = PWRHLD = High, HPM = Low).*

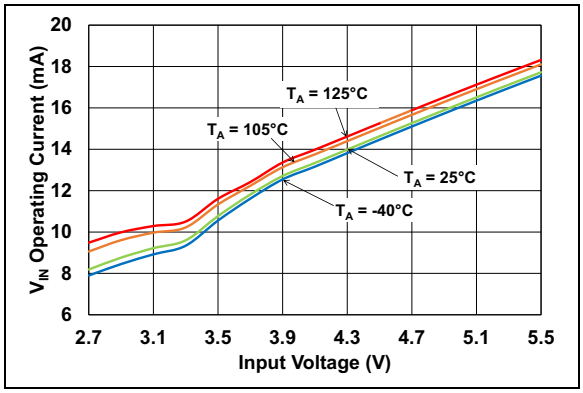


FIGURE 2-3: *V_{IN} Quiescent Current vs. Input Voltage and Temperature – Active Mode (LPM = Low, PWRHLD = High, HPM = Low).*

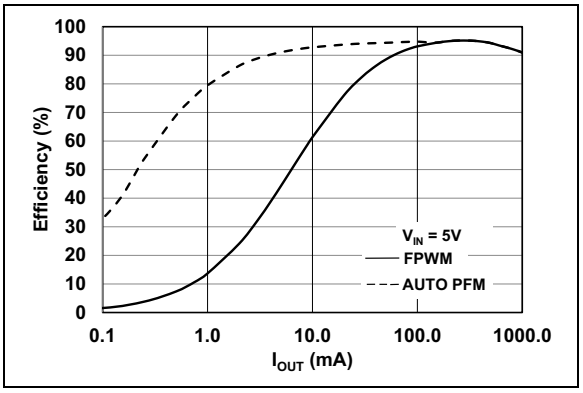


FIGURE 2-4: *Buck1 Efficiency vs. Load Current (V_{OUT1} = 3.3V).*

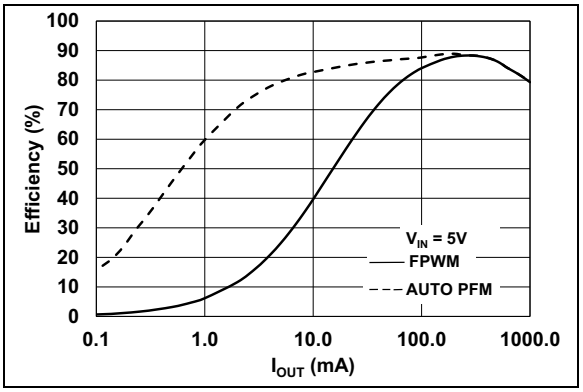


FIGURE 2-5: *Buck2 Efficiency vs. Load Current (V_{OUT2} = 1.2V).*

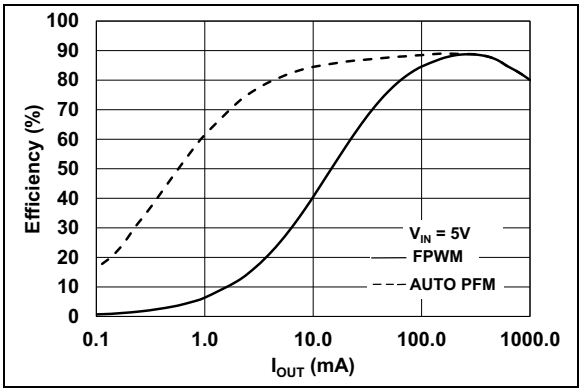


FIGURE 2-6: *Buck3 Efficiency vs. Load Current (V_{OUT3} = 1.25V).*

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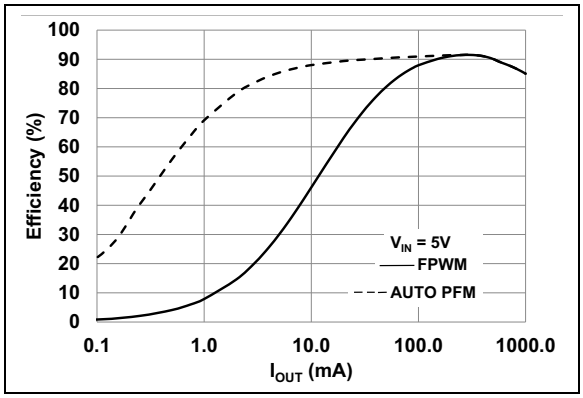


FIGURE 2-7: *Buck4 Efficiency vs. Load Current (V_{OUT3} = 1.8V).*

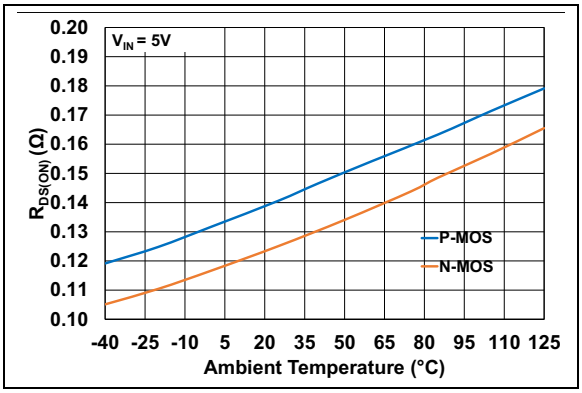


FIGURE 2-10: *MOSFET $R_{DS(ON)}$ vs. Temperature.*

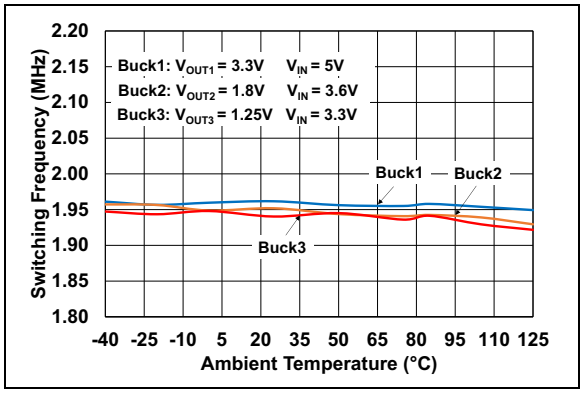


FIGURE 2-8: *Switching Frequency vs. Temperature – Active Mode (LPM = Low, PWRHLD = High, HPM = Low).*

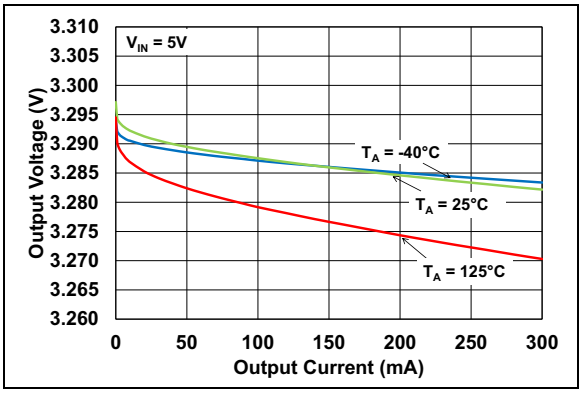


FIGURE 2-11: *LDO1 Output Voltage vs. Output Current and Temperature (Load Regulation – V_{LOUT1} = 3.3V).*

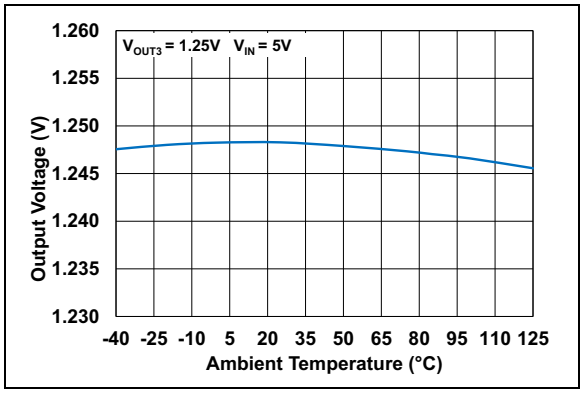


FIGURE 2-9: *Buck3 Output Voltage vs. Temperature – V_{OUT3} = 1.25V, Active Mode (LPM = Low, PWRHLD = High, HPM = Low).*

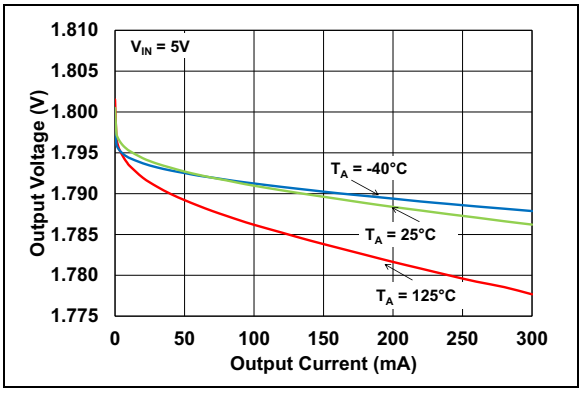


FIGURE 2-12: *LDO2 Output Voltage vs. Output Current and Temperature (V_{LOUT2} = 1.8V).*

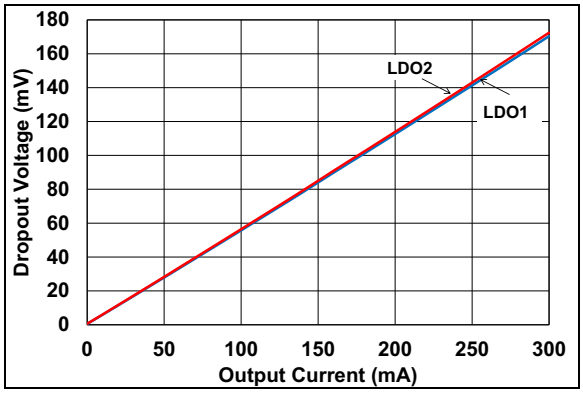


FIGURE 2-13: *LDO1, LDO2 Dropout Voltage vs. Load Current.*

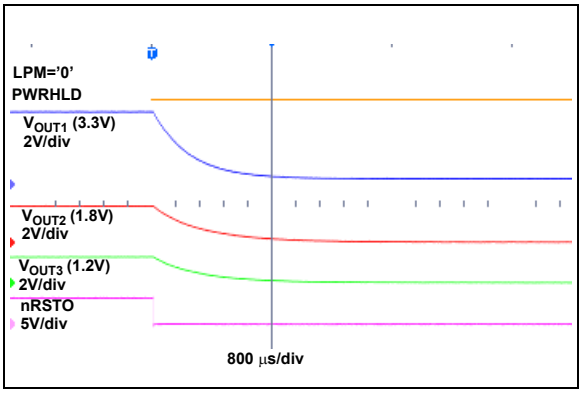


FIGURE 2-16: *PWRHLD Shutdown Sequence.*

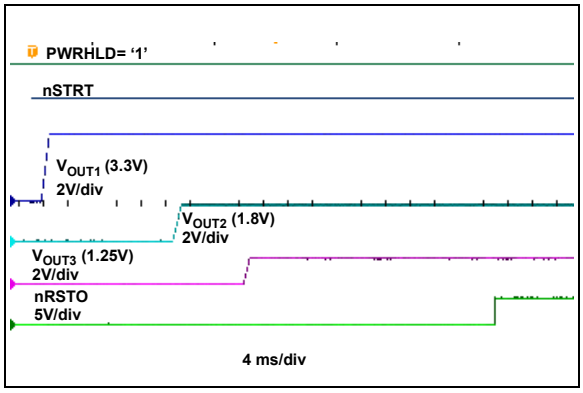


FIGURE 2-14: *nSTRT Start-up Sequence.*

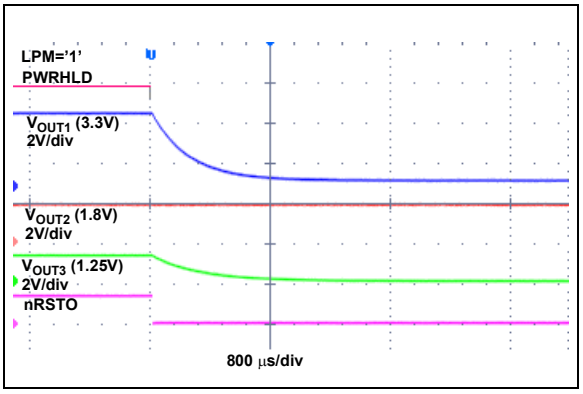


FIGURE 2-17: *Entering Hibernate Mode.*

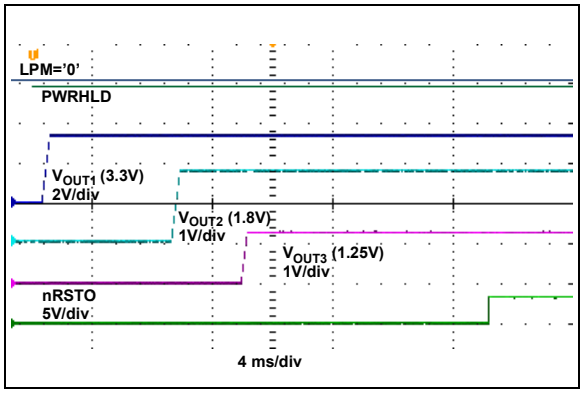


FIGURE 2-15: *PWRHLD Start-up Sequence.*

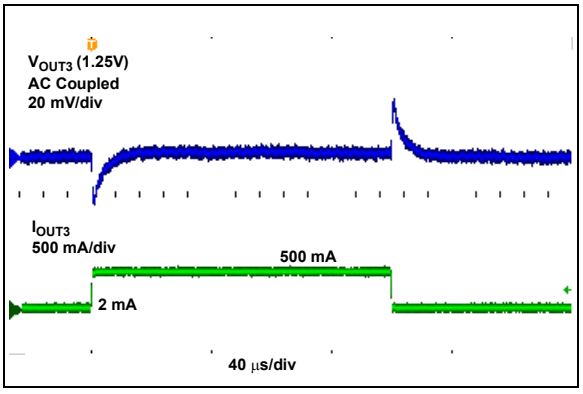


FIGURE 2-18: *Buck3 Transient Response (Active Mode, V_{OUT3} = 1.25V).*

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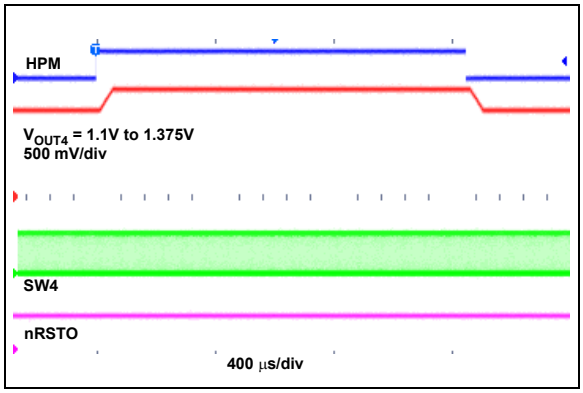


FIGURE 2-19: *Buck4 DVS Transition.*

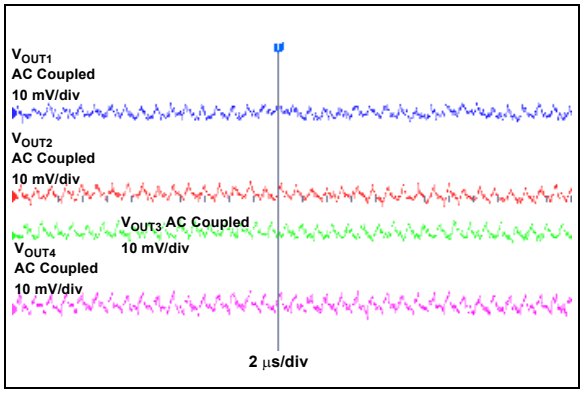


FIGURE 2-22: *Buck Channels Output Voltage Ripple, Active (FPWM) Mode.*

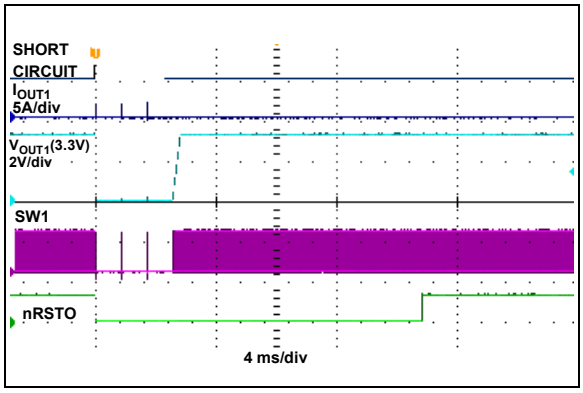


FIGURE 2-20: *Output Short Circuit on V_{OUT1} – HCPEN = 1.*

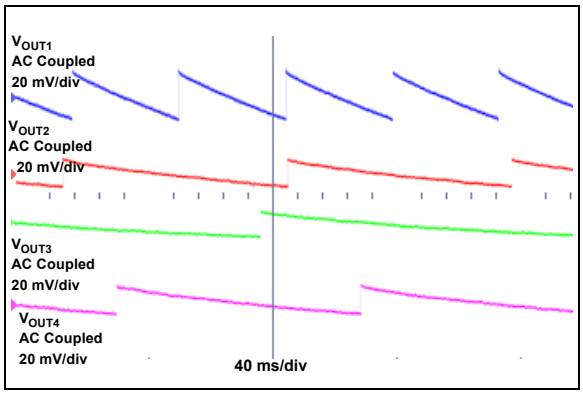


FIGURE 2-23: *Buck Channels Output Voltage Ripple, Low-Power (Auto-PFM) Mode.*

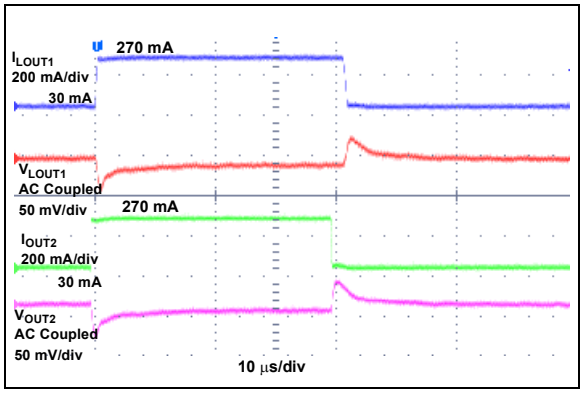


FIGURE 2-21: *LDO1, LDO2 Load Transient Response.*

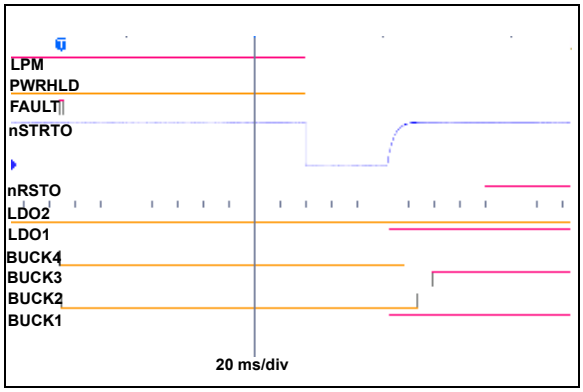


FIGURE 2-24: *Automatic Wake-up Pulse, Hibernate Mode.*

3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Name	Pin Number	Description
1	nINTO	Active-Low, Open-Drain Interrupt Output.
2	nRSTO	Active-Low, Open-Drain Reset Output.
3	SGND	Signal Ground. Connect to reference ground plane.
4	SVIN	Input Voltage for the Analog Control Circuitry. Decouple SVIN to SGND with a 1 µF (minimum) ceramic capacitor.
5	SDA	I^2C Interface Serial Data.
6	SCL	I^2C Interface Serial Clock.
7	nSTRTO	Active-Low, Open-Drain Start Event Output. nSTRTO is asserted low whenever nSTRT is low.
8	PWRHLD	Power Hold Input. Typically asserted as high by the MPU to maintain power after the initial start-up is triggered by nSTRT. PWRHLD is to be asserted as low by the MPU to initiate a PMIC shutdown sequence.
9	OUT1	Output Sensing for Buck Channel 1. Connect to the regulation point for V_{OUT1}.
10	PVIN1	Power Input Voltage of Buck Channel 1. Connect a ceramic capacitor from PVIN1 to the PGND1 pin, to localize pulsed current loops and decouple switching noise.
11	SW1	Switch Node of Buck Channel 1. Internal power MOSFET switches and external inductor connection.
12	PGND1	Power Ground of Buck Channel 1.
13	PGND2	Power Ground of Buck Channel 2.
14	SW2	Switch Node of Buck Channel 2. Internal power MOSFET switches and external inductor connection.
15	PVIN2	Power Input Voltage of Buck Channel 2. Connect a ceramic capacitor from PVIN2 to the PGND2 pin to localize pulsed current loops and decouple switching noise.
16	OUT2	Output Sensing for Buck Channel 2. Connect to the regulation point for V_{OUT2}.
17	SELV2	Buck Channel 2 Output Voltage Selection Pin. Three-state input.
18	SELVL1	LDO1 Default Output Voltage Selection Pin. Three-state input.
19	LOUT1	LDO1 Output. Decouple LOUT1 to ground with a 2.2 µF (minimum) ceramic capacitor. Default start-up state is on. LDO1 can be disabled by I^2C.
20	LVIN	Input Voltage for LDO1 and LDO2. Decouple LVIN to ground with a 2.2 µF (minimum) ceramic capacitor.
21	LOUT2	LDO2 Output. If LDO2 is in use, decouple LOUT2 to SGND with a 2.2 µF (minimum) ceramic capacitor.
22	LPM	Low-Power Mode Input Pin. In combination with PWRHLD and HPM, this pin defines the power mode status of the MCP16502.
23	HPM	High-Performance Mode Input Pin. In combination with PWRHLD and LPM, this pin defines the power mode status of the MCP16502. Connect to ground if not used.
24	nSTRT	Start Event Input. Drive nSTRT to low to initiate a start-up sequence. nSTRT is pulled up internally. A capacitor can be connected to nSTRT to automatically initiate a power-up sequence when the main supply rises.
25	OUT3	Output Sensing for Buck Channel 3. Connect to the regulation point for V_{OUT3}.
26	PVIN3	Power Input Voltage of Buck Channel 3. Connect a ceramic capacitor from PVIN3 to the PGND3 pin to localize pulsed current loops and decouple switching noise.
27	SW3	Switch Node of Buck Channel 3. Internal power MOSFET switches and external inductor connection.

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TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)

Pin Name	Pin Number	Description
28	PGND3	Power Ground of Buck Channel 3.
29	PGND4	Power Ground of Buck Channel 4.
30	SW4	Switch Node of Buck Channel 4. Internal power MOSFET switches and external inductor connection.
31	PVIN4	Power Input Voltage of Buck Channel 4. Connect a ceramic capacitor from PVIN4 to the PGND4 pin to localize pulsed current loops and decouple switching noise.
32	OUT4	Output Sensing for Buck Channel 4. Connect to the regulation point for V_{OUT4}.
-	EP	Exposed Pad. Connect to ground plane with vias to ensure good thermal properties.

4.0 DEVICE OPTIONS

The MCP16502 is offered in different options, depending on the target MPU platform and external memory type. The options currently available, also shown in Table 4-1, are the following:

1. MCP16502AA

This variant is intended for a high-performance (i.e., 500 MHz) SAMA5D2 application; therefore, the voltage of Buck3 (core voltage) is set to 1.25V by default.

Buck4 is typically not used by the SAMA5D2 MPU, so it is disabled during the start-up sequence. If needed, it can be turned on through I^2C commands after the start-up sequence has concluded.

Buck4 components can therefore be left not populated if the end user does not need Buck4, thus saving board space and BOM cost.

2. MCP16502AB

This variant is intended for use cases where MPUs with DVS support use ordinary DDRx memories.

3. MCP16502AC

This variant is intended for an efficiency optimized, high-performance (i.e., 500 MHz) SAMA5D2 application with LPDDR2 memories.

Buck3 (core voltage) is therefore set to 1.25V for 500 MHz operation. Buck2 will be used for the 1.2V rail of the LPDDR2, while Buck4 will be used for the 1.8V rail of the LPDDR2 and will have a different sequencing than in other variants. Buck2 should NOT be set to any other voltage but 1.2V. Buck4 will also stay on during Hibernate mode. LDO2 is not part of the start-up sequence and is free for other purposes (turned on by I^2C command).

4. MCP16502AD

This variant is intended for use cases where MPUs with DVS support use LPDDRx memories.

5. MCP16502AE

This variant is intended for the SAM9X6 MPU series.

Buck3 default voltage has been set to 1.15V to enable 600 MHz core and CPU operation.

Buck4 is excluded from the start-up sequence and is, by default, off in any power state. Therefore, Buck4 external components can be removed if not needed, thus saving overall cost and board space.

Buck4 components can also be populated and Buck4 can always be activated outside of the start-up sequence by an I^2C command.

The SAM9X6 series, just like its predecessor, SAM9X5 series, can ONLY support 1.8V memories (DDR2/ LPSDR/LPDDR). This implies that Buck2 should be set accordingly.

Note:	All device variants are generated at the factory with One-Time-Programmable memory, which configures default settings at power-up. Please contact your nearest Microchip Sales Office for further assistance on the development of customized device variants.

TABLE 4-1: DEFAULT CONFIGURATIONS

Device Options	MCP16502AA	MCP16502AB	MCP16502AC	MCP16502AD	MCP16502AE
V_{OUT1}	3.3V	3.3V	3.3V	3.3V	3.3V
V_{OUT2}	SELV2 Selectable	SELV2 Selectable	SELV2 Selectable (set to 1.2V)	SELV2 Selectable (set to 1.2V)	SELV2 Selectable
V_{OUT3}	1.25V	1.15V	1.25V	1.15V	1.15V
V_{OUT4}	Off	1.15V	1.8V	1.15V	Off
V_{LOUT1}	SELVL1 Selectable	SELVL1 Selectable	SELVL1 Selectable	SELVL1 Selectable	SELVL1 Selectable
V_{LOUT2}	Off	Off	Off	1.8V	Off
Platform	SAMA5D2	Reserved	SAMA5D2 with LPDDR2	Reserved	SAM9X6

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4.1 Buck Channels and Related External Components

The MCP16502 Buck channels are based on Peak Current mode control architecture and have internal frequency compensation for the voltage regulation loop. The slope compensation is optimized for inductors in the 1.5 µH to 2.2 µH range. A minimum output capacitor of 22 µF is required for stability. Output capacitance can be increased if necessary; however, the maximum output capacitance value should be limited to avoid engaging the Hiccup mode overcurrent protection during the initial soft start ramp and during DVS operation. Further details are given in **Section 5.6 "Maximum Simultaneous Capacitive and DC Loading in Soft Start and DVS"**.

The recommended input decoupling capacitance on each Buck channel is 4.7 µF.

The Buck channels can operate in either Forced PWM mode (Continuous Inductor Current mode), where the inductor current is allowed to go negative, or in Automatic PFM mode, where the inductor current is prevented from going negative through Zero-Current Detection (ZCD) and diode emulation of the low-side MOSFET.

The switching frequency in Forced PWM Mode is nominally 2 MHz and can be displaced through I^2C by ±16.5% to prevent interference with other sensitive system blocks.

4.2 LDO Channels and Related External Components

The MCP16502 LDOs are designed for operation with low-ESR ceramic output capacitors of 2.2 µF (minimum value) for loads up to 150 mA, and of 4.7 µF (minimum value) for loads up to 300 mA. The total output capacitance should not exceed 20 µF. The LDOs can be used with an input voltage (V_{LVIN}) less than or equal to the voltage at pin SVIN. As such, they can operate as post-regulators cascaded to the Buck1 output if its output voltage is programmed above 2.7V. Recommended capacitor part numbers are given in **Section 5.1 "Recommended External Components"**.

4.3 Control Signals and Power States

4.3.1 INTERFACING SIGNALS

The MCP16502 is interfaced to the host MPU by means of the following signals: nSTRTO (open-drain output), nRSTO (open-drain output), nINTO (open-drain output), PWRHLD (input), LPM (input) and HPM (input). SDA and SCL are I^2C interface pins. The MCP16502 is a slave only device without clock stretching capability, and therefore, the SCL pin is an input only. Further details about the I^2C interface of the MCP16502 are given in **Section 4.8 "I^2C Interface Description"**. The ESD protection on each interfacing signal is purposely designed to prevent any leakage from the MPU I/Os, even in the case where the main input power is removed from the MCP16502.

4.3.2 nSTRT, nSTRTO, PWRHLD FUNCTIONALITY

The nSTRT (push button input) serves as an external wake-up input to the PMIC+MPU system. nSTRT is internally pulled up to SVIN and monitored. When the nSTRT is pulled/detected as low (e.g., by means of a push button or any other pull-down device) for longer than a minimum debouncing time, the MCP16502 initiates the turn-on sequence.

The nSTRTO signal is asserted low whenever the nSTRT is detected to be low; otherwise, it is High-Z (typically, nSTRTO has an external pull-up resistor). The only exception to this input (nSTRT)/output (nSTRTO) relationship is the so called Automatic Wake-up Pulse (AWKP) that is described in **Section 4.4.6 "Restart Sequence After Fault and Automatic Wake-up Pulse (AWKP) Generation"**.

After the start-up sequence has been initiated, the MCP16502 expects the assertion of the PWRHLD signal (Power-Hold) from the MPU to validate the start-up. PWRHLD could already be high in a typical application using a backup supply. If PWRHLD has not been asserted high by the MPU before the completion of the start-up sequence (i.e., when nRSTO is about to be asserted high), the MCP16502 will automatically initiate a turn-off sequence.

After the assertion of PWRHLD, nSTRT should be released before the long press time-out timer expires (see **Section 4.4.4 "Typical Power-Down Sequence and Timing"**). During run time (PWRHLD = High), the nSTRT (thus nSTRTO) can again be asserted low. No automatic action is taken by the MCP16502 in this case unless the push button interrupt assertion time-out delay expires without any action from the MPU.

4.3.3 nSTRT/PWRHLD TYPICAL USE CASES

Depending on the presence of a backup supply and the availability of an external wake-up signal connected at nSTRT ("Button"), four different scenarios can be defined for the turn-on of the MCP16502, as described in Figure 4-1.

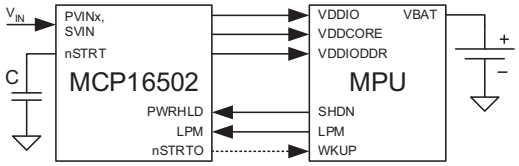
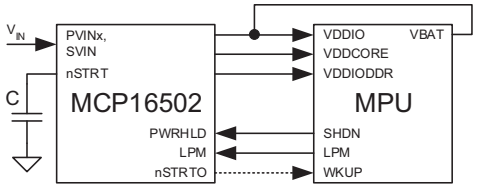
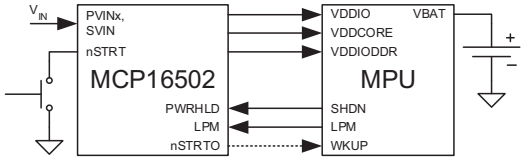
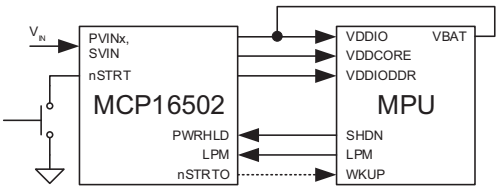
	Applications With a Backup Supply	Applications Without a Backup Supply
Applications Without Start-up Push Button		
	The application starts when V_{IN} ramps up because of the capacitor C, which delays the rise of nSTRT with respect to V_{IN} and causes nSTRT to appear low as soon as the MCP16502 is powered. Note that PWRHLD (= SHDN from MPU) was set to '1' at the time the battery was mounted on the PCB (i.e., at the time of manufacturing). The power channels of MCP16502 are turned off by the MPU by setting SHDN = 0. The MPU is then in Backup mode. If supported, the DDR can also be placed in Backup Self-Refresh (BSR) mode by setting LPM = 1 before SHDN = 0. To wake up the application from Backup mode, a wake-up event must be generated for the SHDWC (Shutdown and Wake-up Controller) of the MPU. This can be an internal event (e.g., RTC, RTT alarm, TAMPER detection) or an event on an I/O of the SHDWC (e.g., wake-up from a wireless module). The MPU will then set SHDN = 1 and the low-to-high transition of PWRHLD will cause the MCP16502 to restart. If V_{IN} is cycled while the MPU is in Backup mode (SHDN = 0), the MCP16502 restarts automatically and sends a wake-up event to the MPU on nSTRTO (WKUP). If this wake-up event was not enabled in the MPU SHDWC configuration, SHDN will stay low and the MCP16502 will turn off at the end of the start-up sequence, because PWRHLD has not been set high. If this wake-up event is enabled, SHDN will immediately go high, thus confirming the start-up sequence for the MCP16502 and the application will restart.	The application starts when V_{IN} ramps up because of the capacitor C, which delays the rise of nSTRT with respect to V_{IN} and causes nSTRT to appear low as soon as the MCP16502 is powered. PWRHLD (= SHDN from MPU) is set to '1' as soon as VBAT (= VDDIO) is above its internal POR threshold (around 1.5V). The power channels of MCP16502 are turned off by the MPU by setting SHDN = 0. In this case, the MPU is not in Backup mode; it is simply completely off. LPM cannot be used, nor can SHDN be set to '1' because the supply voltage of the SHDWC controller is missing. From the OFF state, the application can only be restarted by cycling power on V_{IN}.
Applications With Start-up Push Button (at nSTRT)		
	The application does not immediately start when V_{IN} ramps up. The button must be pressed (nSTRT = Low) to start the MCP16502. Note that PWRHLD (= SHDN from MPU) was set to '1' at the time the battery was mounted on the PCB (i.e., at the time of manufacturing). The power channels of MCP16502 are turned off by the MPU by setting SHDN = 0. The MPU is then in Backup mode. If supported, the DDR can also be placed in backup self-refresh mode (BSR) by setting LPM = 1 before SHDN = 0. To wake up the application from Backup mode, a wake-up event must be generated for the SHDWC (Shutdown and Wake-up Controller) of the MPU. This can be an internal event (e.g., RTC, RTT alarm, TAMPER detection) or an event on an I/O of the SHDWC (e.g., wake-up from a wireless module). The MPU will then set SHDN = 1 and the low-to-high transition of PWRHLD will cause the MCP16502 to restart. If V_{IN} is cycled while the MPU is in Backup mode (SHDN = 0), the MCP16502 does not restart automatically. To restart the application, the button must be pressed and nSTRTO (WKUP) be an enabled wake-up event. The DDR supply loss, due to an input power loss while in BSR mode, will be managed by software (i.e., by reloading the contents of the DDR).	The application does not immediately start when V_{IN} ramps up. The button must be pressed to start the MCP16502. PWRHLD (= SHDN from MPU) is set to '1' as soon as VBAT (= VDDIO) is above its internal POR threshold (around 1.5V). The power channels of MCP16502 are turned off by the MPU by setting SHDN = 0. In this case, the MPU is not in Backup mode; it is simply completely off. LPM cannot be used, nor can SHDN be set to '1' because the supply voltage of the SHDWC controller is missing. To restart the application, the push button must be pressed.

FIGURE 4-1: *Illustration of Start-up Mechanisms for Various MPU Configurations.*

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4.3.4 PWRHLD, LPM, HPM AND POWER STATES DEFINITIONS

PWRHLD, LPM and HPM define different power states which are illustrated in Table 4-2. These are default definitions for the targeted typical application scenario of the SAMA5D2 MPU when powering LPDDR2 DDR memories (MCP16502AC), and therefore, may be different for other application configurations and product variants.

The logic value of the HPM input pin is masked (processed by the internal logic as '0') until a specific I^2C command is issued (HPMEN bit must be set to '1'), because HPM is a generic GPIO with a status at the MPU power-up time that can be undefined.

After the software has issued the unmask HPM command through I^2C, it is safe to assume that the HPM status is well defined and the HPM signal can be used to enter and exit the High-Performance mode.

TABLE 4-2: DEFAULT POWER STATES DEFINITION (MCP16502AC)

PWRHLD	LPM	HPM	Buck1	Buck2	Buck3	Buck4	LDO1	LDO2	nRSTO	Power State
0	0	0	Off	Off	Off	Off	Off	Off	Low	Off
0	1	0	Off	On Auto-PFM	Off	On Auto-PFM	Off	Off	Low	Hibernate mode
1	1	0	On Auto-PFM	On Auto-PFM	On Auto-PFM	On Auto-PFM	On	Off	High-Z	Low-Power mode
1	0	0	On FPWM	On FPWM	On FPWM	On FPWM	On	Off	High-Z	Active
1	0	1	On FPWM	On FPWM	On FPWM	On FPWM	On	Off	High-Z	High-Performance Active (not used by SAMA5D2, SAM9X6)

Other logic combinations of PWRHLD, LPM and HPM (occurring after the HPM unmasking) are forbidden. The initial state is the OFF state (shutdown).

The process by which the MCP16502 abandons the OFF state and enters the other possible power states is defined as the power-up sequence, which is described in **Section 4.4.1 "Typical Power-up Sequence and Timing"**. The following state diagram in Figure 4-2 illustrates the power states of MCP16502 and their typical and/or permissible dynamic transitions.

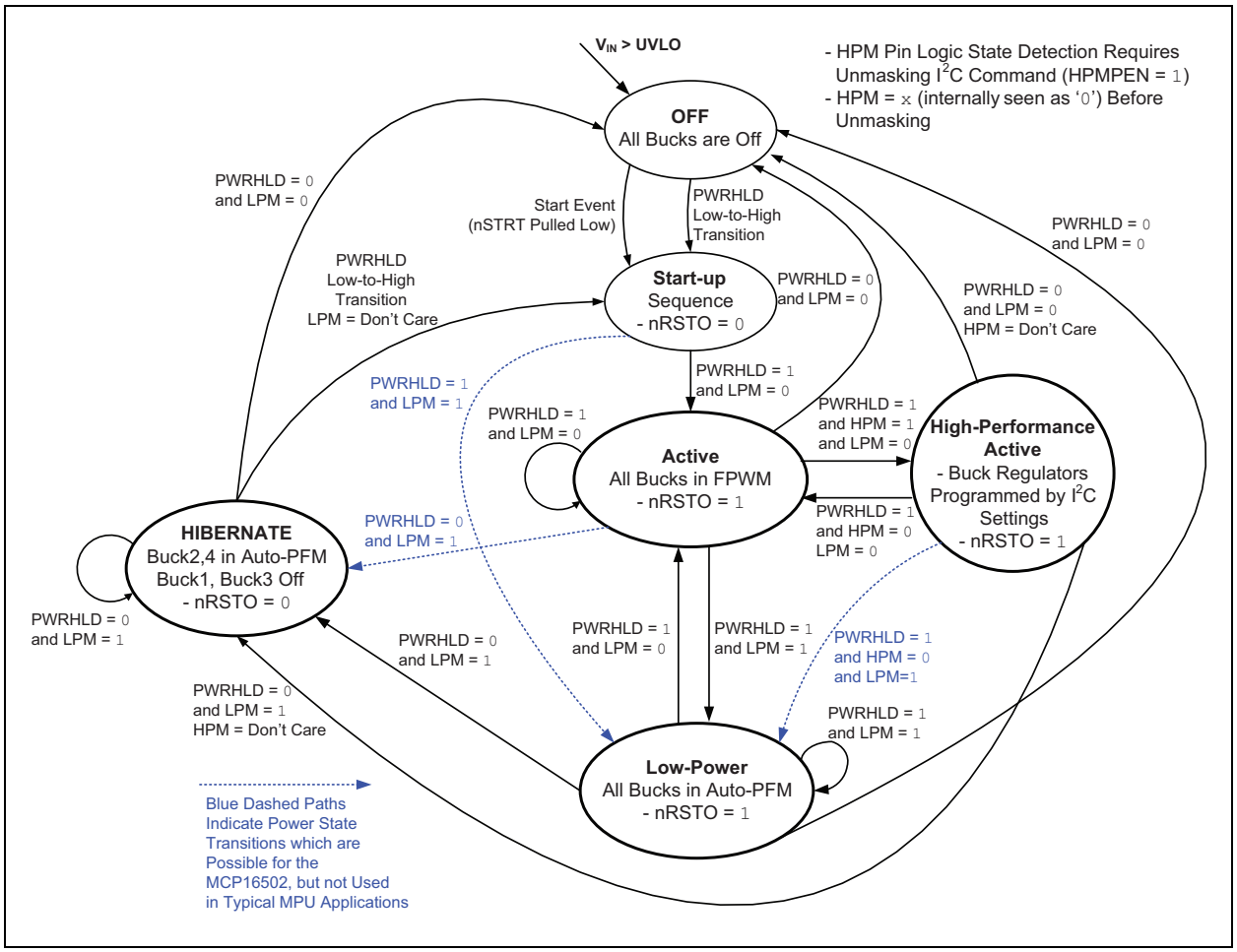


FIGURE 4-2: *Finite State Machine (FSM) States Diagram for MCP16502AC.*

4.3.5 SELVL1 AND SELV2 PINS

Pins SELVL1 and SELV2 are meant to program the default settings of some rails that must be activated during the power-up sequence, but whose voltage values are application-dependent. These are LDO1 and Buck2, the latter being dedicated to DDRx/LPDDRx power.

The default values are selectable among three options, corresponding to three different states of the relevant pin: connected to ground (Low), connected to input supply (High) or left unconnected (High-Z).

The LDO1 default voltage can be selected by means of the SELVL1 pin as follows:

TABLE 4-3: V_{LOUT1} VOLTAGE VS. SELVL1 PIN

SELVL1 Status	V_{LOUT1} Voltage
Low	1.8V
High-Z	2.5V
High	3.3V

The Buck2 default voltage can be selected by means of the SELV2 pin as follows:

TABLE 4-4: V_{OUT2} DEFAULT VOLTAGE VS. SELV2 PIN

SELV2 Status	V_{OUT2} Voltage	DDR Type
Low	1.2V	LPDDR2, LPDDR3
High-Z	1.35V	DDR3L
High	1.8V	DDR2

Note: SELVL1 and SELV2 are always hardwired in the final application and they cannot be changed on-the-fly during operation.

The statuses of SELVL1 and SELV2 are frozen in a snapshot as soon as the SVIN voltage exceeds the turn-on Undervoltage Lockout Threshold (UVLO), as specified in the **"Electrical Characteristics"** table. Any changes of the SELVL1 and SELV2 pins will have no effect after the snapshot, and SVIN must fall under the turn-off (lower) UVLO threshold to unfreeze the snapshot.

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Both pins are intended to be connected to GND (0V), to SVIN or left floating in the application. When left floating, internal circuitry is initially activated to bias SELVL1 and SELV2 at start-up for proper three-state (floating state) detection.

For **"Electrical Characteristics"** table specification purposes, the High State Threshold Voltage (V_{IHT}) and Low State Threshold Voltage (V_{ILT}) of pins SELVL1 and SELV2 are given. They have both a minimum and a maximum value specification.

At the time the snapshot is taken, those Min. and Max. values should be used and interpreted as follows:

- If $V_{IHT}(MAX) < V(SELVx) \leq V(SVIN)$ → SELVx is considered HIGH
- If $0V \leq V(SELVx) < V_{ILT}(MIN)$ → SELVx is considered LOW
- If $V_{ILT}(MAX) < V(SELVx) < V_{IHT}(MIN)$ → SELVx is considered floating

If $V_{IHT}(MIN) \leq V(SELVx) \leq V_{IHT}(MAX)$ or $V_{ILT}(MIN) \leq V(SELVx) \leq V_{ILT}(MAX)$, then the logic status of SELVx may not be interpreted correctly. Therefore, if the end user chooses a connection different than the recommended connection to GND, SVIN or no connection, then any usage of the SELVx pins within those boundaries should be avoided. This is also illustrated in Figure 4-3 shown below:

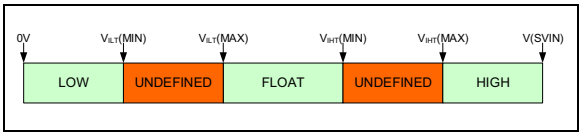


FIGURE 4-3: *SELVx High, Low and Float States Threshold.*

4.3.6 nINTO (INTERRUPT OUTPUT) PIN

Pin nINTO is an active-low, open-drain interrupt output pin. The nINTO pin goes low every time a Fault is detected and the corresponding interrupt masking bit is cleared.

By default, all interrupt generating events are masked (masking bits are '1' by default) and the end user needs to unmask those to enable interrupt generation on Faults.

Only one interrupt generation event is always enabled and cannot be disabled (i.e., the long press push button time-out described in **Section 4.4.4 "Typical Power-Down Sequence and Timing"**).

4.3.7 nRSTO (RESET OUTPUT) PIN

Pin nRSTO is an active-low, open-drain output pin that keeps the MPU in a Reset state. The nRSTO pin is released (i.e., goes High-Z) with a programmable delay upon successful completion of a start-up sequence. The Reset delay is programmable over a wide range of values, as shown in **Section 4.5.4 "Reset Deassertion Delay (t_4) Programming Bits"**, and defaults to 16 ms on all MCP16502 variants. nRSTO is immediately asserted low when either the SVIN voltage falls below the UVLO threshold, or a Fault condition is detected at system level (such as a Thermal Shutdown) or an overcurrent condition is detected on the Buck channels. Please see **Section 5.5 "Protections"** for more details on the Faults that would cause the nRSTO signal low assertion. nRSTO also goes low when the Hibernate mode is entered.

4.4 Power-up/Power-Down/Hibernate Sequences and Timings

4.4.1 TYPICAL POWER-UP SEQUENCE AND TIMING

The typical scenario applies to MPU applications, where:

- I/O voltage (VDDIO) and, if applicable, auxiliary LDO rails (LDOx) are started first (at time t_1).
- DDR supply/DDRIO voltage (VDDIODDR) is started next after delay t_2. From the MPU perspective, t_2 is not mandatory, but it facilitates the use of an external 1.8V DC-DC or LDO for LPDDR2/3 (VDDIODDR being the 1.2V supply of the LPDDR2/3). This DC-DC can be initially sequenced to VDDIO at start-up and maintained on by VDDIODDR for Hibernate mode (backup self-refresh).
- VDDCORE (and VDDCPU for other MPUs) voltages are started last, after a delay of t_3.
- Upon successful start-up of all the rails in the power-up sequence, after delay t_4, the Reset signal (nRSTO) is deasserted and software execution can start.

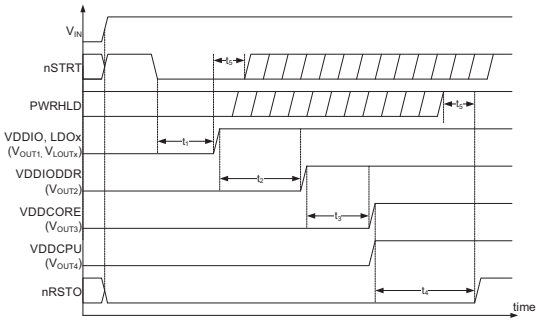
The start-up sequence can be initiated in two different ways, also depending on the presence of a back-up supply in the application:

1. **nSTRT event (nSTRT pin pulled low), maintained by PWRHLD assertion.** In applications with a backup battery, the PWRHLD signal is typically already high before the nSTRT event.
2. **A low-to-high transition of the PWRHLD signal, regardless of the nSTRT event.** This is only possible in applications with backup supply. This mode is typically originated by an external wake-up event asserted by a peripheral device of the MPU Shutdown and Wake-up Controller (SHDWC), which is still powered in Backup mode.

Note:	The nSTRT event needs the assertion of PWRHLD to have the power-up sequence completed successfully. If PWRHLD is not yet high at the time nRSTO is to be asserted, the MCP16502 automatically initiates a turn-off sequence without any positive glitches on nRSTO.

Delay t_1 acts as a debouncing delay of the nSTRT event. Therefore, nSTRT must be detected as low continuously during t_1 to validate the start-up event and initiate the first sequence step. After the first sequence step is started (at t_1), nSTRT can be released to its high level at any time (provided that the push button time-out delay is not exceeded, see **Section 4.4.4 "Typical Power-Down Sequence and Timing"**). Also, subsequent high-low-high toggling of nSTRT during the execution of the start-up sequence, while visible at the nSTRTO output, will be ignored by the sequencer and it will NOT reset the start-up sequence under execution.

The following timing diagram in Figure 4-4 shows the typical sequence for Case 1:



Where:

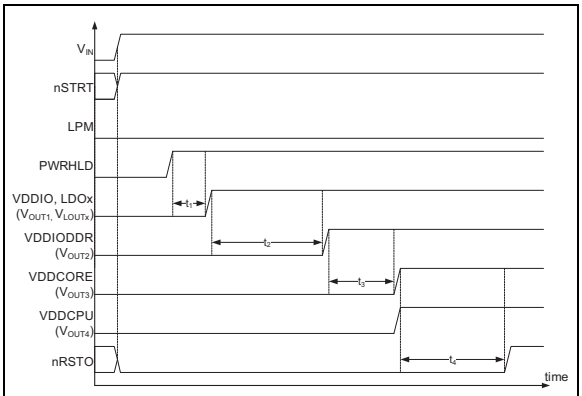
- t_1 = Delay from nSTRT falling to first output V_{OUT1} starting (SEQ[1:0] = 00, default DELAY[2:0] = 001; i.e., 0.5 ms + device wake-up time, about 100 µs)
- t_2 = Time from V_{OUT1} established to V_{OUT2} starting (SEQ[1:0] = 01, default DELAY[2:0] = 101; i.e., 8 ms)
- t_3 = Time from V_{OUT2} established to V_{OUT3}, V_{OUT4} starting (SEQ[1:0] = 10, default DELAY[2:0] = 100; i.e., 4 ms)
- t_4 = Time from V_{OUT3} established to nRSTO deassertion (default RSTDLY[2:0] = 100; i.e., 16 ms)
- t_5 = Setup/hold times, min. 0 µs (internal filtering applies)

FIGURE 4-4: *Start-up from nSTRT Timing Diagram.*

t_1 to t_3 are programmable through the DELAY[2:0] bits; t_4 is programmable through the RSTDLY[2:0] bits, as described in the respective tables in **Section 4.5.4 "Reset Deassertion Delay (t_4) Programming Bits"** and **Section 4.5.5 "Soft Start, Start-up Sequence Step Assignment and Sequence Step Delay (t_1, t_2, t_3) Programming Bits"**.

For power supplies starting at t_1, the DELAY[2:0] bits value is the additional delay time interval added to the device wake-up time.

The following timing diagram in Figure 4-5 shows the typical sequence for Case 2:



Where:

- t_1 = Delay from PWRHLD asserted to first output V_{OUT1} starting (SEQ[1:0] = 00, default DELAY[2:0] = 001; i.e., 0.5 ms + device wake-up time, about 100 µs)
- t_2 = Time from V_{OUT1} established to V_{OUT2} starting (SEQ[1:0] = 01, default DELAY[2:0] = 101; i.e. 8 ms)
- t_3 = Time from V_{OUT2} established to V_{OUT3}, V_{OUT4} starting (SEQ[1:0] = 10, default DELAY[2:0] = 100; i.e., 4 ms)
- t_4 = Time from V_{OUT3} established to nRSTO deassertion (default RSTDLY[2:0] = 100; i.e., 16 ms)

FIGURE 4-5: *Start-up from PWRHLD Timing Diagram.*

For all sequences described above, LPM can be assumed to be low. The MPU will assert LPM after some time, based on software decision, to enter the Low-Power mode.

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4.4.2 POWER-UP SEQUENCE PROGRAMMING AND FLOWCHART

The power-up sequence management is flexible enough to accommodate different power-up sequences than the typical one.

The start-up sequence is divided into three steps and each regulator (Bucks and LDOs) is included in the start-up sequence ONLY if its SEQEN bit is set. Each regulator is then assigned to a specific sequence step:

- Step 1 (SEQ[1:0] = 00): Enabled (SEQEN = 1) regulator(s) are started after a delay (t_1) from the start-up event. If the start-up event is no longer valid as the instant t_1 expires, the start-up sequence is aborted before the first regulator is started.
- Step 2 (SEQ[1:0] = 01): Enabled (SEQEN = 1) regulator(s) are started after a delay (t_2) since the completion of the sequence Step 1 (all regulators enabled at Step 1 have been powered up correctly).
- Step 3 (SEQ[1:0] = 1x): Enabled (SEQEN = 1) regulator(s) are started after a delay (t_3) from the completion of the sequence Step 2 (all regulators enabled at Steps 1 and 2 have been powered up correctly).

If more than one regulator is assigned to power up at a given sequence step, their DELAY[2:0] bits might still be different. Therefore, they might initiate their soft start ramps at different times, even if they are assigned to the same sequence step. This is useful to reduce input inrush currents at start-up.

The subsequent assertion of nRSTO is determined only by the status of all regulators that have been turned on during the power-up sequence (SEQEN = 1). Their status is checked before starting counter t_4 and again checked at the expiration of t_4 to have nRSTO deasserted.

The status of the regulators that have NOT been turned on during the power-up sequence (SEQEN = 0) is not taken into account for the deassertion of nRSTO.

After the completion of the power-up sequence (i.e., at the time instant nRSTO is deasserted), the MCP16502 will enter the Power modes state machine operation defined by the LPM, HPM and PWRHLD signals, and the content of registers, 0x10-0x13, 0x20-0x23, 0x30-0x33, 0x40-0x43, 0x50-0x53 and 0x60-0x63, applies.

Note that there might be a conflict between the enable status of regulator(s) which have been powered up (SEQEN = 1), or left off (SEQEN = 0) during the start-up sequence, and their EN bit (ON or OFF state) in the Power modes states (i.e., bit 7 of registers, 0x10-0x13, and so on).

For example, LDO2 might not have been enabled to turn on during the power-up sequence (SEQEN = 0), but it is defined as on in the Power Modes Definition registers, 0x60-0x63.

In this case, the Power Modes Definition registers, 0x60-0x63, prevail as soon as the power-up sequence is completed; so LDO2 will be turned on immediately after nRSTO has been deasserted.

Some regulators which are supposed to turn on in the power-up sequence may fail to power up correctly.

In this case, the sequencing engine adds a 32 ms waiting time to allow the affected regulators to recover. After the expiration of the 32 ms period, if the affected regulators have still not recovered, the start-up sequence is aborted and the MCP16502 returns to its OFF state.

The start-up sequence flowchart is described in Figure 4-6 on the next page.

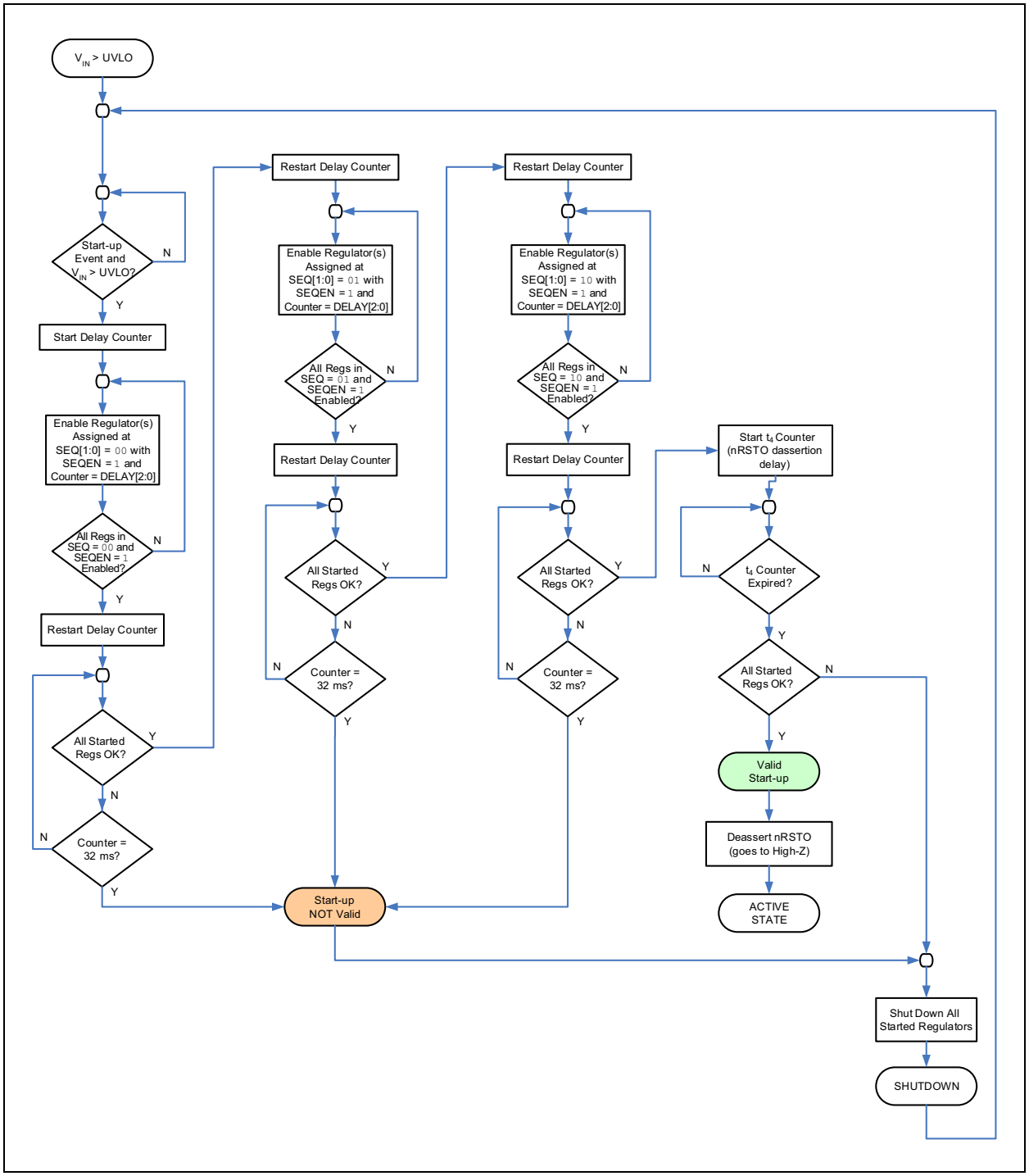


FIGURE 4-6: *Start-up Sequence Flowchart.*

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4.4.3 DROPOUT SAFE START-UP SEQUENCE FEATURE

The start-up sequence management of MCP16502 ensures predictable timing between subsequent steps, even if some power channels may operate in dropout conditions with moderate loading.

This situation might occur for Buck1 or the LDOs because their achievable output voltage range (up to 3.7V) is overlapping the input supply range (2.7V-5.5V).

This operating condition is frequently encountered in battery-powered applications. For example, some loads designed for a 3.3V nominal supply voltage may not be able to withstand the fully replenished battery voltage (around 4.2V), and therefore, they would require a front-end regulator. However, they could still operate when the battery voltage has decreased low enough to push their front-end regulator into dropout.

For example, if the battery voltage is around 3.1V and the Buck1 output voltage is also set to 3.3V, it is still desirable to start Buck1 and proceed throughout the start-up sequence, even if the POK (Power OK) threshold for Buck1 may not be reached, since Buck1 is still delivering a voltage within the I/O operating voltage range. This would allow a better exploitation of the battery because the cutoff voltage is no longer dictated by the onset of the dropout of the 3.3V regulator (Buck1) and by its POK threshold.

By means of a dedicated circuit that monitors the input-output differential during start-up of the potentially affected regulators, the MCP16502 can still ensure a proper start-up and report an out-of-regulation condition of the relevant voltage rail (i.e., POK = 0) after the start-up sequence has been completed. The MPU can then detect the anomaly and decide either to continue operation or to shut down the system.

The Start-up POK Bypass Threshold is the relevant **"Electrical Characteristics"** table parameter that defines the acceptable level of input-output differential, to continue through the start-up sequence, in lack of the normal POK.

4.4.4 TYPICAL POWER-DOWN SEQUENCE AND TIMING

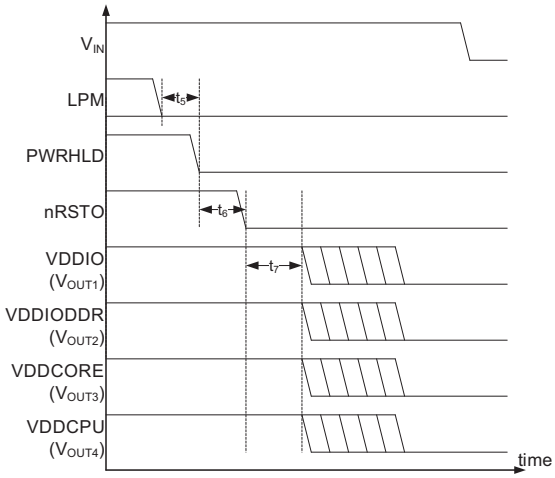
The power-down (shutdown) sequence can be initiated in two ways:

1. Initiated by the MPU by deasserting PWRHLD (LPM being already low or deasserted simultaneously). This is the usual method, which assumes that the MCP16502 is in any operating state (i.e., is outside the start-up sequence).
2. Initiated externally by long press of nSTRT, after t_8 (push button time-out delay) + t_9 (push button interrupt assertion time-out delay) if no action is taken by the MPU within t_9. This is the push button long press time-out function.

After PWRHLD has been deasserted or t_9 has reached End-of-Count (EOC), nRSTO will immediately be asserted low by the MCP16502. After that, all active channels will be turned off.

The turn-off of each channel also activates the active discharge (if enabled by bit DISCH) on the same channel.

The timing diagram in Figure 4-7 shows the typical sequence for Case 1:



Where:

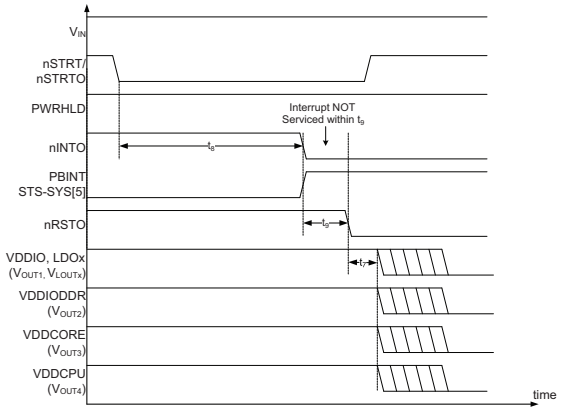
t_5 = Setup time, LPM = 0 to PWRHLD = 0: Min. 0 µs (internal filtering applies)

t_6 = Delay from PWRHLD deasserted to nRSTO asserted: Min. 0 µs, max. 10 µs (not a strict requirement)

t_7 = Delay from nRSTO asserted to first V_{OUTx} turn-off: Min. 0 µs, max. 10 µs (not a strict requirement)

FIGURE 4-7: *Power-Down (Shutdown) Sequence Timing Diagram.*

The following timing diagram in Figure 4-8 shows the typical sequence for Case 2:



Where:

t_8 = Push button (nSTRT long press) time-out delay (default PBTO[1:0] = 01; i.e., 4s)

t_9 = Push button interrupt assertion time-out delay (default PBINTTO[1:0] = 01; i.e., 0.5s)

t_7 = Delay from nRSTO asserted to first V_{OUTX} turn-off: Min. 0 µs, max. 10 µs (not a strict requirement)

FIGURE 4-8: *Push Button Long Press Time-out Shutdown Sequence Timing Diagram.*

If nSTRT is pressed continuously for the entire t_8 duration, an interrupt signal will be asserted (nINTO goes low) and bit PBINT (Push Button Interrupt) in STS-SYS register 0x04h (STS-SYS[5]) will be set. This interrupt is not maskable.

If the MPU reads the STS-SYS register before t_9 expires, bit PBINT is acquired and Reset-on-Read. Then, the MPU can decide either to continue operating or to initiate a shutdown by deasserting PWRHLD.

Once the PBINT bit is cleared by the MPU upon reading the STS-SYS register, the MCP16502 deasserts the interrupt line nINTO, stops the t_9 counting, resets both t_8 (which reached EOC) and t_9, and if the push button condition (nSTRT = low) is no longer active, it does not take any countermeasure and continues operating.

If the MPU does NOT read the STS-SYS register before t_9 expires, then the MCP16502 will go into shutdown (OFF state). A new valid start-up event will be needed to retrieve operation.

If the MPU reads the STS-SYS register before the t_9 expires and decides to take no action, but the push button condition is still present, the t_8 (and then t_9) counter starts again. This way, the long press condition can be extended indefinitely by simply reading the STS-SYS register each time the nINTO signal is asserted.

The push button time-out delay t_8 is user-programmable with the PBTO[1:0] bits, from 2s to 16s (2s-4s-8s-16s).

The push button interrupt assertion time-out delay t_9 is user-programmable with the PBINTTO[1:0] bits, from 100 ms to 2s (100 ms-500 ms-1s-2s).

It may happen that during run time (i.e., PWRHLD = 1), the nSTRT input goes low first, and then PWRHLD is set low by the MPU before the expiration of t_8 + t_9. In this case, no automatic restart action is generated by the steady nSTRT = Low condition.

If PWRHLD goes low during run-time, that means the MPU software has decided to go to off/Hibernate mode (by deasserting SHDN from the SHDWC controller), regardless of the nSTRTO pin status (which is also monitored in the SHDWC controller).

Therefore, the MCP16502 will NOT attempt a new start-up based on a prior nSTRT = Low Level.

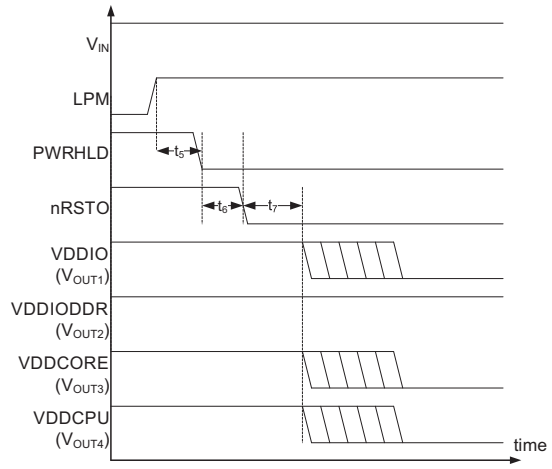
To initiate another start-up sequence after PWRHLD has entered low status following a prior nSTRT = Low (yet not long enough to trigger the push button time-out), nSTRT should be at first released (i.e., go high), then pressed again (for longer than t_1) to generate a new valid wake-up event.

4.4.5 TYPICAL HIBERNATE SEQUENCES AND TIMING

The Hibernate mode entering sequence is similar to the power-down, with the only difference is that LPM will be asserted high by the MPU before deassertion of PWRHLD, or at least at the same time PWRHLD is deasserted (due to internal filtering, the setup time t_5 can be as low as 0 µs). For example, taking the MCP16502AB variant into consideration, the V_{OUT2} rail (and/or other rails which are defined as on in Hibernate mode by overwriting the default settings) will remain active, while V_{OUT1}, V_{OUT3}, V_{OUT4} and V_{LOUT1} will be immediately disabled. In Hibernate mode, the DDRx/LPDDRx will typically be in Backup Self-Refresh mode (BSR).

The following timing diagram in Figure 4-9 shows the typical Hibernate mode sequence for a device variant that keeps only V_{OUT2} on in Hibernate mode (such as MCP16502AB).

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Where:

t_5 = Setup time, LPM = 1 to PWRHLD = 0: Min. 0 µs (internal filtering applies)

t_6 = Delay from PWRHLD deasserted to nRSTO asserted: Min. 0 µs, max. 10 µs (not a strict requirement)

t_7 = Delay from nRSTO asserted to first V_{OUTX} turn-off: Min. 0 µs, max. 10 µs (not a strict requirement)

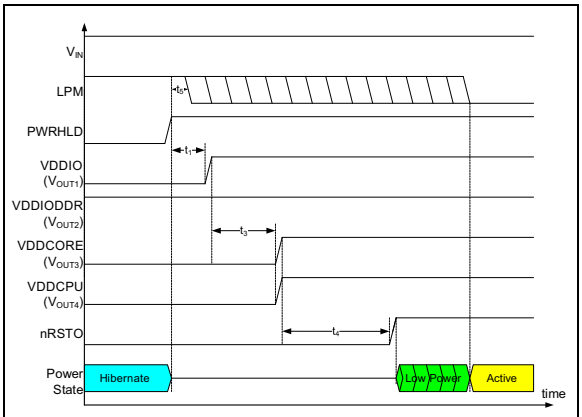
FIGURE 4-9: *Entering Hibernate Mode Timing Diagram.*

From the Hibernate state, the system can:

1. Move to OFF state (if LPM also goes low, the V_{OUT2} can be immediately turned off); or
2. Initiate another start-up sequence (with the exception of Buck2 which is already active and has its SEQEN = 1) by a low-to-high transition of PWRHLD.

The timing diagram of a start-up sequence from Hibernate mode is shown in Figure 4-10. After the assertion of PWRHLD, the MPU may deassert LPM at any time. Due to internal filtering, simultaneous transition of LPM and PWRHLD is allowed (hold time t_5 can be 0 µs).

Depending on the time at which LPM is deasserted, the MCP16502 may transition through the Low-Power state or not.



Where:

t_1 = Delay from PWRHLD asserted to first supply V_{OUT1} starting (SEQ[1:0] = 00, default DELAY[2:0] = 001; i.e., 0.5 ms)

t_3 = Time from V_{OUT1} established to V_{OUT3}, V_{OUT4} starting (SEQ[1:0] = 10, default DELAY[2:0] = 100; i.e., 4 ms)

t_4 = Time from V_{OUT3}, V_{OUT4} established to nRSTO deassertion (default RSTDLY[2:0] = 100; i.e., 16 ms)

t_5 = Minimum hold time, PWRHLD = 1 to LPM = 0: Min. 0 µs (internal filtering applies)

FIGURE 4-10: *Start-up Sequence Exiting Hibernate Mode Timing Diagram.*

Note: Upon exit of Hibernate mode, Buck2 is not part of the sequence because it is already on (being in Auto-PFM mode) and its SEQEN = 1. However, also depending on the instant at which the MPU deasserts LPM, it can toggle to FPWM mode at the time nRSTO is deasserted.

Similar to Buck2, any other regulator defined as on in the Hibernate state with its bit SEQEN = 1, will NOT be turned off when exiting the Hibernate state for a new start-up sequence.

If the regulator is defined on in the Hibernate state, but its bit SEQEN = 0, it will be turned off as soon as the new start-up sequence is initiated.

In conclusion, for a regulator to stay on continuously from the Hibernate state throughout the new start-up sequence, two conditions must be satisfied:

1. The regulator is set on in the Hibernate state.
2. SEQEN bit = 1.

4.4.6 RESTART SEQUENCE AFTER FAULT AND AUTOMATIC WAKE-UP PULSE (AWKP) GENERATION

The power-up sequence is also automatically executed when reacting to severe Fault conditions. Please see **Section 5.5 "Protections"** for information on which Faults may trigger a new restart sequence. In the default configuration (i.e., HCPEN bit is '0' for the Buck channels), as soon as a Fault is detected, the power delivery on all channels is terminated and the MCP16502 waits for 100 ms. After this wait time, a new start-up sequence is generated in the attempt to restart the system correctly.

A special feature is provided to enable system recovery if there is a restart sequence after a Fault occurs while in Hibernate mode. In Hibernate mode, the PWRHLD had been previously set to low by the MPU and the MPU expects a wake-up event in order to set PWRHLD to high again. This must be a hardware event, which is flagged to some I/O inside the MPU Shutdown and Wake-up Controller (SHDWC) block (e.g., a logic transition on a WKUPx or PIOBUx pin).

However, if a Fault (e.g., a short circuit on a Buck channel having HCPEN = 0 and left on during Hibernate) causes a restart sequence while in Hibernate mode, the restart sequence is not successfully completed until a wake-up event is generated for the MPU SHDWC, because the PWRHLD remains low. It is necessary for the PWRHLD signal to be high just prior to the completion of the start-up sequence so that nRSTO can be deasserted.

This is solved by generating from the MCP16502 an Automatic Wake-up Pulse (AWKP) on the nSTRTO output if the Fault that generates a restart sequence has occurred while in Hibernate mode.

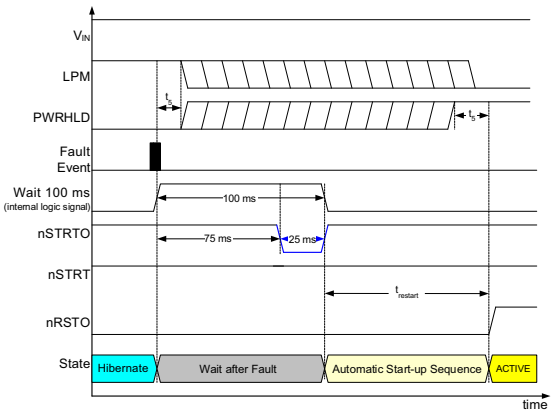
The Automatic Wake-up Pulse generation can be optionally disabled by the user by setting the AWKPDIS bit (bit 4) in the SYS-CFG register (0x03). The AWKP function is enabled by default.

The timing diagram of a restart sequence caused by a Fault while in Hibernate mode is shown in Figure 4-11.

Just before initiating the restart sequence, the MCP16502 generates a 25 ms (nominal duration) Automatic Wake-up Pulse on the nSTRTO output, even in lack of a low level on the nSTRT input. This is the only situation where the nSTRTO logic level does not reflect the nSTRT input status. The duration of the AWK Pulse erodes into the 100 ms waiting time that precedes the automatic restart sequence.

PWRHLD will typically return high as soon as the nSTRTO signal is detected to be low by the MPU SHDWC. If LPM stays high for any reason, the MCP16502 will go in Low-Power mode immediately after the automatic start-up sequence. This behavior is shown in Figure 2-24 in **Section 2.0 "Typical Performance Curves"**.

If the restart sequence after a Fault is executed in any other operational state but Hibernate, PWRHLD will either be already high (in applications with backup power) or it would return high as soon as the VDDIO rail is started, thus making the generation of the Automatic Wake-up Pulse not necessary.



Where:

$t_{restart}$ = Duration of the automatic start-up (restart) sequence

t_5 = Minimum setup/hold time: Min. 0 µs (internal filtering applies)

FIGURE 4-11: *Automatic Wake-up Pulse Generation Timing Diagram (Fault during Hibernate).*

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4.5 Configuration Words, Register Definitions and Maps

The position of the Configuration Word bits in the global register maps is described in **Section 4.6 "I²C Registers Maps and Bit Definitions"**.

4.5.1 VSET[5:0] CODES DEFINITION

For Buck regulators (OUTx) and LDOs (LOUTx), the voltage code definitions listed in Table 4-5 below apply:

TABLE 4-5: VOLTAGE CODE DEFINITION BITS (VSET[5:0])

VSET[5:0]	Buck1, LDO1, LDO2	Buck2, Buck3, Buck4	VSET[5:0]	Buck1, LDO1, LDO2	Buck2, Buck3, Buck4
	V_{OUT} (V)	V_{OUT} (V)		V_{OUT} (V)	V_{OUT} (V)
111111	**3.700**	**1.850**	100101	**2.400**	**1.200**
111110	**3.650**	**1.825**	100100	**2.350**	**1.175**
111101	**3.600**	**1.800**	100011	**2.300**	**1.150**
111100	**3.550**	**1.775**	100010	**2.250**	**1.125**
111011	**3.500**	**1.750**	100001	**2.200**	**1.100**
111010	**3.450**	**1.725**	100000	**2.150**	**1.075**
111001	**3.400**	**1.700**	011111	**2.100**	**1.050**
111000	**3.350**	**1.675**	011110	**2.050**	**1.025**
110111	**3.300**	**1.650**	011101	**2.000**	**1.000**
110110	**3.250**	**1.625**	011100	**1.950**	**0.975**
110101	**3.200**	**1.600**	011011	**1.900**	**0.950**
110100	**3.150**	**1.575**	011010	**1.850**	**0.925**
110011	**3.100**	**1.550**	011001	**1.800**	**0.900**
110010	**3.050**	**1.525**	011000	**1.750**	**0.875**
110001	**3.000**	**1.500**	010111	**1.700**	**0.850**
110000	**2.950**	**1.475**	010110	**1.650**	**0.825**
101111	**2.900**	**1.450**	010101	**1.600**	**0.800**
101110	**2.850**	**1.425**	010100	**1.550**	**0.775**
101101	**2.800**	**1.400**	010011	**1.500**	**0.750**
101100	**2.750**	**1.375**	010010	**1.450**	**0.725**
101011	**2.700**	**1.350**	010001	**1.400**	**0.700**
101010	**2.650**	**1.325**	010000	**1.350**	**0.675**
101001	**2.600**	**1.300**	001111	**1.300**	**0.650**
101000	**2.550**	**1.275**	001110	**1.250**	**0.625**
100111	**2.500**	**1.250**	001101	**1.200**	**0.600**
100110	**2.450**	**1.225**	<001101	1.200	0.600

4.5.2 SWITCHING (OSCILLATOR) FREQUENCY DISPLACEMENT PROGRAMMING BITS

TABLE 4-6: SWITCHING FREQUENCY DISPLACEMENT BITS (FSD[1:0])

FSD[1:0]	Frequency Displacement
00	0%
01	0%
10	-16.5%
11	+16.5%

The frequency displacement acts on the main oscillator. The switching frequencies of all regulators and all timings are shifted accordingly.

4.5.3 PUSH BUTTON TIME-OUT DELAY (t_8) AND PUSH BUTTON INTERRUPT ASSERTION TIME-OUT DELAY (t_9) PROGRAMMING BITS

TABLE 4-7: PUSH BUTTON TIME-OUT DELAY BITS (PBTO[1:0])

PBTO[1:0]	Push Button Time-out Delay t_8 (s)
00	2
01	4
10	8
11	16

TABLE 4-8: PUSH BUTTON INTERRUPT ASSERTION TIME-OUT DELAY BITS (PBINTTO[1:0])

PBINTTO[1:0]	Push Button Interrupt Assertion Time-out Delay t_9 (s)
00	0.1
01	0.5
10	1
11	2

4.5.4 RESET DEASSERTION DELAY (t_4) PROGRAMMING BITS

TABLE 4-9: RESET DEASSERTION DELAY BITS (RSTDLY[2:0])

RSTDLY[2:0]	Delay (ms)
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

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4.5.5 SOFT START, START-UP SEQUENCE STEP ASSIGNMENT AND SEQUENCE STEP DELAY (t_1, t_2, t_3) PROGRAMMING BITS

For each regulator, the SSR[1:0] bits define the soft start rate in terms of time duration of each voltage step (t_{ramp}).

TABLE 4-10: SOFT START RATE BITS SSR[1:0]

SSR[1:0]	2 MHz Clock Division	t_{ramp} (µs)	Buck2,3,4 25 mV Step – Average Ramp Rate (V/ms)	Buck1,LDO1,2 50 mV Step – Average Ramp Rate (V/ms)	C_{OUT} (µF)	Average C_{OUT} Capacitor Current (mA) 25 mV Step	Average C_{OUT} Capacitor Current (mA) 50 mV Step
00	16	8	3.125	6.250	22	69	138
01	32	16	1.563	3.125	22	34	69
10	48	24	1.042	2.083	22	23	46
11	64	32	0.781	1.563	22	17	34

The SEQ[1:0] bits assign each regulator at a determined step in the start-up sequence. Assignment SEQ[1:0] = 00 (first sequence step) means the regulator is started upon a valid start-up event.

However, each regulator is allowed to turn on at its assigned start-up sequence step only if its SEQEN bit is set. If SEQEN = 0, the regulator will NOT turn on, and it will be disregarded in the sequence generation and nRSTO deassertion algorithm.

Upon exiting Hibernate mode, all regulators (typically, Buck2) which were already on in Hibernate mode and have SEQEN = 1, will stay on continuously throughout the execution of the start-up sequence.

TABLE 4-11: START-UP SEQUENCE STEP ASSIGNMENT BITS (SEQ[1:0])

SEQ[1:0]	Start-up Sequence Step
00	1
01	2
10	3
11	3

TABLE 4-12: SEQUENCE STEP DELAY BITS (DELAY[2:0])

DELAY[2:0]	Delay (ms)
000	0
001	0.5
010	1
011	2
100	4
101	8
110	12
111	16

For each regulator, these bits program the delay (t_1 to t_3) from the completion of the previous sequence step to the beginning of its turn-on (beginning of soft start if SEQEN = 1).

For regulators assigned to the first sequence step (SEQ[1:0] = 00); i.e., starting at t_1, this is the additional delay after the device wake-up time since the start-up event (e.g., nSTRT high-to-low or PWRHLD low-to-high).

This way, by setting DELAY[2:0] = 001 or higher, it is possible to define a debouncing time of the nSTRT event.

4.5.6 DYNAMIC VOLTAGE SCALING RATE PROGRAMMING BITS (t_{ramp})

The DVSR[1:0] bits define the Dynamic Voltage Scaling rate in terms of time duration of each voltage step (t_{ramp}).

Due to the output capacitor voltage change rate, additional current is required at the output during DVS. The average current for 22 µF (recommended output capacitor value) is also given in Table 4-13. In case the output capacitance is increased, see **Section 5.6 "Maximum Simultaneous Capacitive and DC Loading in Soft Start and DVS"**.

TABLE 4-13: DYNAMIC VOLTAGE SCALING RATE BITS (DVSR[1:0])

DVSR[1:0]	2 MHz Clock Division	t_{ramp} (s)	Buck2,3,4 25 mV Step – Average Ramp Rate (V/ms)	Buck1,LDO1,2 50 mV Step – Average Ramp Rate (V/ms)	C_{OUT} (µF)	Average C_{OUT} Capacitor Current (mA) 25 mV Step	Average C_{OUT} Capacitor Current (mA) 50 mV Step
00	16	8	3.125	6.250	22	69	138
01	32	16	1.563	3.125	22	34	69
10	48	24	1.042	2.083	22	23	46
11	64	32	0.781	1.563	22	17	34

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4.6 I²C Registers Maps and Bit Definitions

On each Buck regulator, and for all power state registers (-A, -LPM, -HIB, -HPM), the default values can be reprogrammed through I²C. This way, it is possible to redefine the voltages, on/off status and mode of operation (FPWM or Auto-PFM) for each power state. For LDOs, mode of operation is not applicable.

The following provides the register mappings of all the bits available in the user register space of MCP16502AC.

The same mapping structure also applies to other product variants, but the default values of some bits are different.

The default register contents corresponding to each different product variant of MCP16502 are listed in Table 4-15.

In Table 4-14, each **BLACK** bit in the volatile (I²C-accessible) registers has a corresponding bit in the OTP bank. The default values of the **BLACK** bits in the volatile registers are loaded from the OTP bank.

It is possible to program the OTP at the factory to generate additional product variants with different default values for the **BLACK** bits. Please contact your nearest Microchip Sales Office for further assistance on the development of customized default configurations.

Each **RED** bit has no corresponding bit in the OTP bank.

The default values of the **RED** bits are:

- Either hardwired in metal mask; or
- For the VSET[5:0] bits in **RED**, copied over from the corresponding VSET[5:0] bits in the OUTx-A and LDOx-A registers. Note that for Buck4, this strategy implies I²C reprogramming of the voltage for HPM status if the VDDCPU has to be increased in HPM with respect to other states. This update can be done when or before the HPMPEN bit is set; or
- For B7 (EN) and B6 (MODE, where applicable) in the OUTx-HPM and LDOx-HPM registers, copied over from the corresponding bits in the OUTx-A and LDOx-A registers.

Table 4-14 provides the bits/bit field values within the registers.

TABLE 4-14: MCP16502AC GLOBAL REGISTERS MAP

Register Name	Address	—	Bits							
			B7	B6	B5	B4	B3	B2	B1	B0
SYSTEM REGISTERS										
SYS-ADR	0x00	NAME	Reserved	ADR[6]	ADR[5]	ADR[4]	ADR[3]	ADR[2]	ADR[1]	ADR[0]
		DEFAULT	R-1	R-1	R-0	R-1	R-1	R-0	R-1	R-1
SYS-ID	0x01	NAME	ID[3]	ID[2]	ID[1]	ID[0]	REV[3]	REV[2]	REV[1]	REV[0]
		DEFAULT	R-0	R-0	R-1	R-1	R-0	R-0	R-0	R-0
SYS-TMG	0x02	NAME	PBTO[1]	PBTO[0]	PBINTTO[1]	PBINTTO[0]	Reserved	RSTDLY[2]	RSTDLY[1]	RSTDLY[0]
		DEFAULT	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0
SYS-CFG	0x03	NAME	TSDMSK	TWRMSK	HPMPEN	AWKPDIS	FSD[1]	FSD[0]	B1HCEN	USER
		DEFAULT	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYSTEM AND POWER CHANNELS STATUS REGISTERS										
STS-SYS	0x04	NAME	TSD	TWR	PBINT	Reserved	Reserved	Reserved	Reserved	Reserved
		DEFAULT	R/RoR-0	R/RoR-0	R/RoR-0	R-0	R-0	R-0	R-0	R-0
STS-B1	0x05	NAME	FLT	HICCUP	ILIMNEG	ZCD	Reserved	SSD	POK	ENS
		DEFAULT	R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	R-0	R-0	R-0	R-0
STS-B2	0x06	NAME	FLT	HICCUP	ILIMNEG	ZCD	Reserved	SSD	POK	ENS
		DEFAULT	R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	R-0	R-0	R-0	R-0
STS-B3	0x07	NAME	FLT	HICCUP	ILIMNEG	ZCD	Reserved	SSD	POK	ENS
		DEFAULT	R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	R-0	R-0	R-0	R-0
STS-B4	0x08	NAME	FLT	HICCUP	ILIMNEG	ZCD	Reserved	SSD	POK	ENS
		DEFAULT	R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	R-0	R-0	R-0	R-0
STS-L1	0x09	NAME	FLT	Reserved	Reserved	Reserved	ILIM	SSD	POK	ENS
		DEFAULT	R/RoR-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
STS-L2	0x0A	NAME	FLT	Reserved	Reserved	Reserved	ILIM	SSD	POK	ENS
		DEFAULT	R/RoR-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Legend: R = Read access; R/W = Read/Write access; RoR = Reset-on-Read (after bit value has been read, it is cleared automatically); x = Default values ('0' or '1').

TABLE 4-14: MCP16502AC GLOBAL REGISTERS MAP (CONTINUED)

Register Name	Address	—	Bits							
			B7	B6	B5	B4	B3	B2	B1	B0
BUCK REGULATOR REGISTERS										
Buck1										
OUT1-A	0x10	NAME	EN	MODE	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-1	R/W-1	R/W – 11 0111 (3.3V, see VSET[5:0] table)					
OUT1-LPM	0x11	NAME	EN	MODE	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-1	R/W-0	R/W – 11 0111 (3.3V, see VSET[5:0] table)					
OUT1-HIB	0x12	NAME	EN	MODE	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-0	R/W-0	R/W – 11 0111 (3.3V, see VSET[5:0] table)					
OUT1-HPM	0x13	NAME	EN	MODE	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-1	R/W-1	R/W – 11 0111 (3.3V, see VSET[5:0] table)					
OUT1-SEQ	0x14	NAME	SSR[1]	SSR[0]	SEQ[1]	SEQ[0]	SEQEN	DELAY[2]	DELAY[1]	DELAY[0]
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1
OUT1-CFG	0x15	NAME	FLTMSK	HCPEN	DISCH	PHASE	DVSR[1]	DVSR[0]	REN	RCON
		DEFAULT	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
Buck2										
OUT2-A	0x20	NAME	EN	MODE	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-1	R/W-1	R/W – Default code is pin-defined (see VSET[5:0] table)					
OUT2-LPM	0x21	NAME	EN	MODE	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-1	R/W-0	R/W – Default code is pin-defined (see VSET[5:0] table)					
OUT2-HIB	0x22	NAME	EN	MODE	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-1	R/W-0	R/W – Default code is pin-defined (see VSET[5:0] table)					
OUT2-HPM	0x23	NAME	EN	MODE	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-1	R/W-1	R/W – Default code is pin-defined (see VSET[5:0] table)					
OUT2-SEQ	0x24	NAME	SSR[1]	SSR[0]	SEQ[1]	SEQ[0]	SEQEN	DELAY[2]	DELAY[1]	DELAY[0]
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-1
OUT2-CFG	0x25	NAME	FLTMSK	HCPEN	DISCH	PHASE	DVSR[1]	DVSR[0]	REN	RCON
		DEFAULT	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Buck3										
OUT3-A	0x30	NAME	EN	MODE	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-1	R/W-1	R/W – 10 0111 (1.25V, see VSET[5:0] table)					
OUT3-LPM	0x31	NAME	EN	MODE	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-1	R/W-0	R/W – 10 0111 (1.25V, see VSET[5:0] table)					
OUT3-HIB	0x32	NAME	EN	MODE	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-0	R/W-0	R/W – 10 0111 (1.25V, see VSET[5:0] table)					
OUT3-HPM	0x33	NAME	EN	MODE	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-1	R/W-1	R/W – 10 0111 (1.25V, see VSET[5:0] table)					
OUT3-SEQ	0x34	NAME	SSR[1]	SSR[0]	SEQ[1]	SEQ[0]	SEQEN	DELAY[2]	DELAY[1]	DELAY[0]
		DEFAULT	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
OUT3-CFG	0x35	NAME	FLTMSK	HCPEN	DISCH	PHASE	DVSR[1]	DVSR[0]	REN	RCON
		DEFAULT	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
Buck4										
OUT4-A	0x40	NAME	EN	MODE	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-1	R/W-1	R/W – 11 1101 (1.8V, see VSET[5:0] table)					
OUT4-LPM	0x41	NAME	EN	MODE	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-1	R/W-0	R/W – 11 1101 (1.8V, see VSET[5:0] table)					
OUT4-HIB	0x42	NAME	EN	MODE	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-1	R/W-0	R/W – 11 1101 (1.8V, see VSET[5:0] table)					
OUT4-HPM	0x43	NAME	EN	MODE	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-1	R/W-1	R/W – 11 1101 (1.8V, see VSET[5:0] table)					

Legend: R = Read access; R/W = Read/Write access; RoR = Reset-on-Read (after bit value has been read, it is cleared automatically); x = Default values ('0' or '1').

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TABLE 4-14: MCP16502AC GLOBAL REGISTERS MAP (CONTINUED)

Register Name	Address	—	Bits							
			B7	B6	B5	B4	B3	B2	B1	B0
OUT4-SEQ	0x44	NAME	SSR[1]	SSR[0]	SEQ[1]	SEQ[0]	SEQEN	DELAY[2]	DELAY[1]	DELAY[0]
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
OUT4-CFG	0x45	NAME	FLTMSK	HCPEN	DISCH	PHASE	DVSR[1]	DVSR[0]	REN	RCON
		DEFAULT	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LDO REGISTERS										
LDO1										
LDO1-A	0x50	NAME	EN	Reserved	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-1	R/W-0	R/W – Default code is pin-defined (see VSET[5:0] table)					
LDO1-LPM	0x51	NAME	EN	Reserved	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-1	R/W-0	R/W – Default code is pin-defined (see VSET[5:0] table)					
LDO1-HIB	0x52	NAME	EN	Reserved	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-0	R/W-0	R/W – Default code is pin-defined (see VSET[5:0] table)					
LDO1-HPM	0x53	NAME	EN	Reserved	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-1	R/W-0	R/W – Default code is pin-defined (see VSET[5:0] table)					
LDO1-SEQ	0x54	NAME	SSR[1]	SSR[0]	SEQ[1]	SEQ[0]	SEQEN	DELAY[2]	DELAY[1]	DELAY[0]
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1
LDO1-CFG	0x55	NAME	FLTMSK	Reserved	DISCH	Reserved	DVSR[1]	DVSR[0]	REN	RCON
		DEFAULT	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LDO2										
LDO2-A	0x60	NAME	EN	Reserved	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-0	R/W-0	R/W – 11 0111 (3.3V, see VSET[5:0] table)					
LDO2-LPM	0x61	NAME	EN	Reserved	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-0	R/W-0	R/W – 11 0111 (3.3V, see VSET[5:0] table)					
LDO2-HIB	0x62	NAME	EN	Reserved	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-0	R/W-0	R/W – 11 0111 (3.3V, see VSET[5:0] table)					
LDO2-HPM	0x63	NAME	EN	Reserved	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT	R/W-0	R/W-0	R/W – 11 0111 (3.3V, see VSET[5:0] table)					
LDO2-SEQ	0x64	NAME	SSR[1]	SSR[0]	SEQ[1]	SEQ[0]	SEQEN	DELAY[2]	DELAY[1]	DELAY[0]
		DEFAULT	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
LDO2-CFG	0x65	NAME	FLTMSK	Reserved	DISCH	Reserved	DVSR[1]	DVSR[0]	REN	RCON
		DEFAULT	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Legend: R = Read access; R/W = Read/Write access; RoR = Reset-on-Read (after bit value has been read, it is cleared automatically); x = Default values ('0' or '1').

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REGISTER 4-1: SYS-ADR (0x00)

r-1	R-1	R-0	R-1	R-1	R-0	R-1	R-1
—	ADR[6:0]						
bit 15							bit 8

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Reserved:** Default is always ‘1’ for factory programmed units

bit 6-0 **ADR[6:0]:** I^2C Address bits (default is 0x5B)

REGISTER 4-2: SYS-ID (0x01)

R-0	R-0	R-1	R-1	R-0	R-0	R-0	R-0
ID[3:0]				REV[3:0]			
bit 15							bit 8

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4 **ID[3:0]:** Device ID bits

bit 3-0 **REV[3:0]:** Revision/Version Identification bits

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REGISTER 4-3: SYS-TMG: SYSTEM TIMING SETTINGS (0x02)

R/W-0	R/W-1	R/W-0	R/W-1	r-0	R/W-1	R/W-0	R/W-0
PBTO[1:0]		PBINTTO[1:0]		—	RSTDLY[2:0]		
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **PBTO[1:0]:** Push Button Time-out bits
Push button nSTRT time-out delay programming bits, default is '01' (4 seconds).

bit 5-4 **PBINTTO[1:0]:** Push Button Interrupt Assertion Time-out Delay bits
Push button interrupt assertion time-out delay programming bits, default is '01' (0.5 second).

bit 3 **Reserved:** Maintain as '0'

bit 2-0 **RSTDLY[2:0]:** nRSTO Deassertion Delay Programming bits
nRSTO deassertion delay programming bits (t_4 in the start-up sequence), default is '100' (16 ms).

REGISTER 4-4: SYS-CFG: SYSTEM CONFIGURATION (0x03)

R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TSDMSK	TWRMSK	HPMPEN	AWKPDIS	FSD[1:0]		B1HCEN	USER
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **TSDMSK:** Thermal Shutdown Masking bit
If this bit is '1', it will prevent nINTO from being asserted low upon TSD = 1. Default is '1' (Thermal Shutdown (TSD) will not be flagged by nINTO).

bit 6 **TWRMSK:** Thermal Warning Masking bit
If this bit is '1', it will prevent nINTO from being asserted low upon a Thermal Warning event. Default is '1' (Thermal Warning will not be flagged by nINTO).

bit 5 **HPMPEN:** High-Performance Mode Enable Pin bit
This bit must be set to '1' through an I^2C command in order to enable the HPM pin. If the bit is '0', setting the HPM pin high will have no effect on the power status state machine.

bit 4 **AWKPDIS:** Automatic Wake-up Pulse Disable bit
If this bit is set to '1', it disables the generation of a wake-up pulse on pin nSTRTO before an automatic start-up sequence after a Fault (Thermal Shutdown or hiccup with HCPEN = 0) occurred in Hibernate mode.

bit 3-2 **FSD[1:0]:** Switching (Oscillator) Frequency Displacement bits
Default is '00' (no displacement).

bit 1 **B1HCEN:** Buck1 Hysteretic Control Mode Enable bit
When set, this bit enables the Hysteretic Control mode for Buck1 in Auto-PFM operation.

bit 0 **USER:** User-Accessible bit
This bit an be used to store system information. It is volatile and is cleared with SVIN UVLO.

REGISTER 4-5: STS-SYS: SYSTEM STATUS (0x04)

R/RoR-0	R/RoR-0	R/RoR-0	r-0	r-0	r-0	r-0	r-0
TSD	TWR	PBINT	—	—	—	—	—
bit 7							bit 0

Legend:	r = Reserved bit	RoR = Reset-on-Read bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **TSD:** Thermal Shutdown Fault Flag bit (latched)

If a Thermal Shutdown occurs, the TSD bit will be set to '1'. It will not automatically return to '0' after the Thermal Shutdown condition has ceased. If the Fault condition is no longer present, a Read operation will automatically also clear the flag (Reset-on-Read, RoR). If the corresponding masking bit, TSDMSK, is '0', TSD = 1 will cause nINTO to be asserted low.

bit 6 **TWR:** Thermal Warning Fault Flag bit (latched)

If a Thermal Warning occurs, the TWR bit will be set to '1'. It will not automatically return to '0' after the Thermal Warning condition has ceased. If the Fault condition is no longer present, a Read operation will automatically also clear the flag (Reset-on-Read, RoR). If the corresponding masking bit, TWRMSK, is '0', TWR = 1 will cause nINTO to be asserted low.

bit 5 **PBINT:** Push Button Interrupt Flag bit

This bit is set as soon as the push button on time-out has expired. A Read action will reset the PBINT flag and also reset the push button time-out counter.

bit 4-0 **Reserved:** Maintain as '0'

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REGISTER 4-6: STS-B1: BUCK1 STATUS (0x05)

R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	r-0	R-0	R-0	R-0
FLT	HICCUP	ILIMNEG	ZCD	—	SSD	POK	ENS
bit 7							bit 0

Legend:	r = Reserved bit	RoR = Reset-on-Read bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **FLT:** Fault Flag bit (latched)
FLT is set to '1' if HICCUP = 1 or if (ENS = 1 and SSD = 1 and POK = 0).

bit 6 **HICCUP:** Hiccup Flag bit (latched)
If the HS OC event counter reaches EOC and POK is low, the HICCUP flag is latched. The behavior of the system is determined by the HCPEN bit.

bit 5 **ILIMNEG:** Negative Current Limit Flag bit (latched)
If the negative current limit threshold is reached, the ILIMNEG flag is latched.

bit 4 **ZCD:** Zero Current Crossing Detection Flag bit (latched)
This bit is set every time the ZCD is enabled (in Auto-PFM mode) and the ZCD comparator trips.

bit 3 **Reserved:** Maintain as '0'

bit 2 **SSD:** Soft Start Done Status bit (not latched)
SSD = 1 means the regulator is enabled and has completed the soft start ramp.

bit 1 **POK:** Power OK Status bit (not latched)
POK reflects the instantaneous value of the POK comparator output.

bit 0 **ENS:** Enable Status bit (not latched)
ENS = 1 means the regulator is currently enabled.

REGISTER 4-7: STS-B2: BUCK2 STATUS (0x06)

R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	r-0	R-0	R-0	R-0
FLT	HICCUP	ILIMNEG	ZCD	—	SSD	POK	ENS
bit 7							bit 0

Legend:	r = Reserved bit	RoR = Reset-on-Read bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **FLT:** Fault flag bit (latched)
FLT is set to '1' if HICCUP = 1 or if (ENS = 1 and SSD = 1 and POK = 0).

bit 6 **HICCUP:** Hiccup Flag bit (latched)
If the HS OC event counter reaches EOC and POK is low, the HICCUP flag is latched. The behavior of the system is determined by the HCPEN bit.

bit 5 **ILIMNEG:** Negative Current Limit Flag bit (latched)
If the negative current limit threshold is reached, the ILIMNEG flag is latched.

bit 4 **ZCD:** Zero Current Crossing Detection Flag bit (latched)
This bit is set every time the ZCD is enabled (in Auto-PFM mode) and the ZCD comparator trips.

bit 3 **Reserved:** Maintain as '0'

bit 2 **SSD:** Soft Start Done status bit (not latched)
SSD = 1 means the regulator is enabled and has completed the soft start ramp.

bit 1 **POK:** Power OK Status bit (not latched)
POK reflects the instantaneous value of the POK comparator output.

bit 0 **ENS:** Enable Status bit (not latched)
ENS = 1 means the regulator is currently enabled.

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REGISTER 4-8: STS-B3: BUCK3 STATUS (0x07)

R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	r-0	R-0	R-0	R-0
FLT	HICCUP	ILIMNEG	ZCD	—	SSD	POK	ENS
bit 7							bit 0

Legend:	r = Reserved bit	RoR = Reset-on-Read bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **FLT:** Fault Flag bit (latched)
FLT is set to '1' if HICCUP = 1 or if (ENS = 1 and SSD = 1 and POK = 0).

bit 6 **HICCUP:** Hiccup Flag bit (latched)
If the HS OC event counter reaches EOC and POK is low, the HICCUP flag is latched. The behavior of the system is determined by the HCPEN bit.

bit 5 **ILIMNEG:** Negative Current Limit Flag bit (latched)
If the negative current limit threshold is reached, the ILIMNEG flag is latched.

bit 4 **ZCD:** Zero Current Crossing Detection Flag bit (latched)
This bit is set every time the ZCD is enabled (in Auto-PFM mode) and the ZCD comparator trips.

bit 3 **Reserved:** Maintain as '0'

bit 2 **SSD:** Soft Start Done Status bit (not latched)
SSD = 1 means the regulator is enabled and has completed the soft start ramp.

bit 1 **POK:** Power OK Status bit (not latched)
POK reflects the instantaneous value of the POK comparator output.

bit 0 **ENS:** Enable Status bit (not latched)
ENS = 1 means the regulator is currently enabled.

REGISTER 4-9: STS-B4: BUCK4 STATUS (0x08)

R/RoR-0	R/RoR-0	R/RoR-0	R/RoR-0	r-0	R-0	R-0	R-0
FLT	HICCUP	ILIMNEG	ZCD	—	SSD	POK	ENS
bit 7							bit 0

Legend:	r = Reserved bit	RoR = Reset-on-Read bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **FLT:** Fault flag bit (latched)
FLT is set to '1' if HICCUP = 1 or if (ENS = 1 and SSD = 1 and POK = 0).

bit 6 **HICCUP:** Hiccup Flag bit (latched)
If the HS OC event counter reaches EOC and POK is low, the HICCUP flag is latched. The behavior of the system is determined by the HCPEN bit.

bit 5 **ILIMNEG:** Negative Current Limit Flag bit (latched)
If the negative current limit threshold is reached, the ILIMNEG flag is latched.

bit 4 **ZCD:** Zero Current Crossing Detection Flag bit (latched)
This bit is set every time the ZCD is enabled (in Auto-PFM mode) and the ZCD comparator trips.

bit 3 **Reserved:** Maintain as '0'

bit 2 **SSD:** Soft Start Done Status bit (not latched)
SSD = 1 means the regulator is enabled and has completed the soft start ramp.

bit 1 **POK:** Power OK Status bit (not latched)
POK reflects the instantaneous value of the POK comparator output.

bit 0 **ENS:** Enable Status bit (not latched)
ENS = 1 means the regulator is currently enabled.

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REGISTER 4-10: STS-L1: LDO1 STATUS (0x09)

R/RoR-0	r-0	r-0	r-0	R-0	R-0	R-0	R-0
FLT	—	—	—	ILIM	SSD	POK	ENS
bit 7							bit 0

Legend:	r = Reserved bit	RoR = Reset-on-Read bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **FLT:** Fault flag bit (latched)
FLT is set to '1' if (ENS = 1 and SSD = 1 and POK = 0).

bit 6-4 **Reserved:** Maintain as '0'

bit 3 **ILIM:** Current Limit Status bit (not latched)
ILIM = 1 means the regulator is in current limit.

bit 2 **SSD:** Soft Start Done Status bit (not latched)
SSD = 1 means the regulator is enabled and has completed the soft start ramp.

bit 1 **POK:** Power OK Status bit (not latched)
POK reflects the instantaneous value of the POK comparator output.

bit 0 **ENS:** Enable Status bit (not latched)
ENS = 1 means the regulator is currently enabled.

REGISTER 4-11: STS-L2: LDO2 STATUS (0x0A)

R/RoR-0	r-0	r-0	r-0	R-0	R-0	R-0	R-0
FLT	—	—	—	ILIM	SSD	POK	ENS
bit 7							bit 0

Legend:	r = Reserved bit	RoR = Reset-on-Read bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **FLT:** Fault flag bit (latched)
FLT is set to '1' if (ENS = 1 and SSD = 1 and POK = 0).

bit 6-4 **Reserved:** Maintain as '0'

bit 3 **ILIM:** Current Limit Status bit (not latched)
ILIM = 1 means the regulator is in current limit.

bit 2 **SSD:** Soft Start Done Status bit (not latched)
SSD = 1 means the regulator is enabled and has completed the soft start ramp.

bit 1 **POK:** Power OK Status bit (not latched)
POK reflects the instantaneous value of the POK comparator output.

bit 0 **ENS:** Enable Status bit (not latched)
ENS = 1 means the regulator is currently enabled.

REGISTER 4-12: OUT1-A: BUCK1 ACTIVE MODE (0x10)

R/W-1	R/W-1	R/W-1(1)	R/W-1(1)	R/W-0(1)	R/W-1(1)	R/W-1(1)	R/W-1(1)
EN	MODE	VSET[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in Active Status bit
If EN = 1, the regulator is enabled.

bit 6 **MODE:** Mode in Active Status bit
If MODE = 1, then the Buck will run in FPWM, else if MODE = 0, then the Buck will run in Auto-PFM.

bit 5-0 **VSET[5:0]:** Output Voltage Selection for Active Status bits
Default = 3.3V.

Note 1: Default = 3.3V, see the VSET[5:0] table.

REGISTER 4-13: OUT1-LPM: BUCK1 LOW-POWER MODE (0x11)

R/W-1	R/W-0	R/W-1(1)	R/W-1(1)	R/W-0(1)	R/W-1(1)	R/W-1(1)	R/W-1(1)
EN	MODE	VSET[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in Low-Power Modes Status bit
If EN = 1, then the regulator is enabled.

bit 6 **MODE:** Mode in Low-Power Mode Status bit
If MODE = 1, then the Buck will run in FPWM, else if MODE = 0, then the Buck will run in Auto-PFM.

bit 5-0 **VSET[5:0]:** Output Voltage Selection bits
Output voltage selection bits for Low-Power modes status (Default = 3.3V).

Note 1: Default = 3.3V, see the VSET[5:0] table.

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REGISTER 4-14: OUT1-HIB: BUCK1 HIBERNATE MODE (0x12)

R/W-0	R/W-0	R/W-1(1)	R/W-1(1)	R/W-0(1)	R/W-1(1)	R/W-1(1)	R/W-1(1)
EN	MODE	VSET[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in Hibernate Mode Status bit
If EN = 1, then it is regulator-enabled.

bit 6 **MODE:** Mode in Hibernate Mode Status bit
If MODE = 1, then the Buck will run in FPWM, else if MODE = 0, then the Buck will run in Auto-PFM.

bit 5-0 **VSET[5:0]:** Output Voltage Selection bits
Output voltage selection bits for Hibernate mode status (Default = 3.3V).

Note 1: Default = 3.3V, see the VSET[5:0] table.

REGISTER 4-15: OUT1-HPM: BUCK1 HIGH-PERFORMANCE MODE (0x13)

R/W-1	R/W-1	R/W-1(1)	R/W-1(1)	R/W-0(1)	R/W-1(1)	R/W-1(1)	R/W-1(1)
EN	MODE	VSET[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in High-Performance Mode Status bit
If EN = 1, then it is regulator-enabled.

bit 6 **MODE:** Mode in High-Performance Mode Status bit
If MODE = 1, then the Buck will run in FPWM, else if MODE = 0, then the Buck will run in Auto-PFM.

bit 5-0 **VSET[5:0]:** Output Voltage Selection bits
Output voltage selection bits for High-Performance mode status (Default = 3.3V).

Note 1: Default = 3.3V, see the VSET[5:0] table.

REGISTER 4-16: OUT1-SEQ: BUCK1 SEQUENCING (0x14)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1
SSR[1:0]		SEQ[1:0]		SEQEN	DELAY[2:0]		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **SSR[1:0]:** Soft Start Rate bits

Soft start rate selection bits.

bit 5-4 **SEQ[1:0]:** Start-up Sequence Step bits

Start-up sequence step assignment bits.

bit 3 **SEQEN:** Start-up Sequence Enable bit

SEQEN = 0 regulator will NOT start at the assigned step. If SEQEN = 0, the SSD and POK flags will be neglected in the start-up sequence.

bit 2-0 **DELAY[2:0]:** Time Delay bits

Time delay from the completion of the previous start-up sequence step or start-up event to the turn-on (beginning of soft start).

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REGISTER 4-17: OUT1-CFG: BUCK1 CONFIGURATION (0x15)

R/W-1	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
FLTMSK	HCPEN	DISCH	PHASE	DVSR[1:0]		REN	RCON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **FLTMSK:** Fault Masking bit
If this bit is '1', it will prevent nINTO from being asserted low upon FLT = 1.

bit 6 **HCPEN:** Short-Circuit Protection Hiccup Mode Enable bit
If HCPEN = 1, a short-circuit event will cause a Hiccup mode response with unlimited soft start retries, without shutting down the other channels.
If HCPEN = 0, a short-circuit event on the channel will cause immediate shutdown of ALL channels and a new start-up sequence will automatically be attempted after a 100 ms delay.

bit 5 **DISCH:** Active Output Discharge Control bit
DISCH = 1 enables active output discharge when channel is turned off; DISCH = 0 disables it.

bit 4 **PHASE:** Regulator Phase Control bit
Set bit to '1' for regulator to operate 180° out of phase with the oscillator; clear bit to '0' for regulator to operate in phase with the oscillator.

bit 3-2 **DVSR[1:0]:** Dynamic Voltage Scaling Rate bits
Dynamic Voltage Scaling rate programming bits.

bit 1 **REN:** Register Enable bit
Used in combination with RCON. If RCON = 0, the value of REN has no effect. If RCON = 1, setting REN = 1 enables channel and REN = 0 disables it, regardless of the current status.
Mode of operation (FPWM or Auto-PFM) is still controlled by the MODE bits.

bit 0 **RCON:** Register Enable Control bit
Used in combination with the REN bit.

REGISTER 4-18: OUT2-A: BUCK2 ACTIVE MODE (0x20)

R/W-1	R/W-1	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)
EN	MODE	VSET[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in Active Status bit
If EN = 0, the regulator is enabled.

bit 6 **MODE:** Mode in Active Status bit
If MODE = 1, then the Buck will run in FPWM, else if MODE = 0, then the Buck will run in Auto-PFM.

bit 5-0 **VSET[5:0]:** Output Voltage Selection for Active Status bits
Default is pin-selectable.

Note 1: Default is pin-selectable.

REGISTER 4-19: OUT2-LPM: BUCK2 LOW-POWER MODE (0x21)

R/W-1	R/W-0	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)
EN	MODE	VSET[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in Low-Power Modes Status bit
If EN = 1, then it is regulator-enabled.

bit 6 **MODE:** Mode in Low-Power Mode Status bit
If MODE = 1, then the Buck will run in FPWM, else if MODE = 0, then the Buck will run in Auto-PFM.

bit 5-0 **VSET[5:0]:** Output Voltage Selection for Low-Power Modes Status bits
Default value is pin-selectable.

Note 1: Default is pin-selectable.

REGISTER 4-20: OUT2-HIB: BUCK2 HIBERNATE MODE (0x22)

R/W-1	R/W-0	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)
EN	MODE	VSET[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in Hibernate Mode Status bit
If EN = 1, then it is regulator-enabled.

bit 6 **MODE:** Mode in Hibernate Mode Status bit
If MODE = 1, then the Buck will run in FPWM, else if MODE = 0, then the Buck will run in Auto-PFM.

bit 5-0 **VSET[5:0]:** Output Voltage Selection for Hibernate Mode Status bits
Default value is pin-selectable.

Note 1: Default is pin-selectable.

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REGISTER 4-21: OUT2-HPM: BUCK2 HIGH-PERFORMANCE MODE (0x23)

R/W-1	R/W-1	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)
EN	MODE	VSET[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in High-Performance Mode Status bit
If EN = 1, then it is regulator-enabled.

bit 6 **MODE:** Mode in High-Performance Mode Status bit
If MODE = 1, then the Buck will run in FPWM, else if MODE = 0, then the Buck will run in Auto-PFM.

bit 5-0 **VSET[5:0]:** Output Voltage Selection for High-Performance Mode Status bits
Default value is pin-selectable.

Note 1: Default is pin-selectable.

REGISTER 4-22: OUT2-SEQ: BUCK2 SEQUENCING (0x24)

R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-1
SSR[1:0]		SEQ[1:0]		SEQEN	DELAY[2:0]		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **SSR[1:0]:** Soft Start Rate bits
Soft start rate selection bits.

bit 5-4 **SEQ[1:0]:** Start-up Sequence Step bits
Start-up sequence step assignment bits.

bit 3 **SEQEN:** Start-up Sequence Enable bit
SEQEN = 0 regulator will NOT start at the assigned step. If SEQEN = 0, the SSD and POK flags will be neglected in the start-up sequence.

bit 2-0 **DELAY[2:0]:** Time Delay bits
Time delay from the completion of the previous start-up sequence step or start-up event to the turn-on (beginning of soft start).

REGISTER 4-23: OUT2-CFG: BUCK2 CONFIGURATION (0x25)

R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTMSK	HCPEN	DISCH	PHASE	DVSR[1:0]		REN	RCON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **FLTMSK:** Fault Masking bit
If this bit is '0', it will prevent nINTO from being asserted low upon FLT = 1.

bit 6 **HCPEN:** Short-Circuit Protection Hiccup Mode Enable bit
If HCPEN = 1, a short-circuit event will cause a Hiccup mode response with unlimited soft start retries, without shutting down the other channels.
If HCPEN = 0, a short-circuit event on the channel will cause immediate shutdown of ALL channels and a new start-up sequence will automatically be attempted after a 100 ms delay.

bit 5 **DISCH:** Active Output Discharge Control bit
DISCH = 1 enables active output discharge when the channel is turned off, DISCH = 0 disables it.

bit 4 **PHASE:** Regulator Phase Control bit
Set this bit to '1' for the regulator to operate 180° out of phase with the oscillator; clear bit to '0' for regulator to operate in phase with the oscillator.

bit 3-2 **DVSR[1:0]:** Dynamic Voltage Scaling Rate bits
Dynamic Voltage Scaling rate programming bits.

bit 1 **REN:** Register Enable bit
This bit is used in combination with RCON. If RCON = 0, the value of REN has no effect. If RCON = 1, setting REN = 1 enables the channel and REN = 0 disables it, regardless of the current status.
Mode of operation (FPWM or Auto-PFM) is still controlled by the MODE bits

bit 0 **RCON:** Register Enable Control bit
This bit is used in combination with the REN bit.

REGISTER 4-24: OUT3-A: BUCK3 ACTIVE MODE (0x30)

R/W-1	R/W-1	R/W-1(1)	R/W-0(1)	R/W-0(1)	R/W-1(1)	R/W-1(1)	R/W-1(1)
EN	MODE	VSET[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in Active Status bit
If EN = 1, the regulator is enabled.

bit 6 **MODE:** Mode in Active Status bit
If MODE = 1, then the Buck will run in FPWM, else if MODE = 0, then the Buck will run in Auto-PFM.

bit 5-0 **VSET[5:0]:** Output Voltage Selection for Active Status bits
Default = 1.25V for MCP16502AC.

Note 1: Default = 1.25V, see the VSET[5:0] table.

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REGISTER 4-25: OUT3-LPM: BUCK3 LOW-POWER MODE (0x31)

R/W-1	R/W-0	R/W-1(1)	R/W-0(1)	R/W-0(1)	R/W-1(1)	R/W-1(1)	R/W-1(1)
EN	MODE	VSET[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in Low-Power Modes Status bit
If EN = 1, then it is regulator-enabled.

bit 6 **MODE:** Mode in Low-Power Mode Status bit
If MODE = 1, then the Buck will run in FPWM, else if MODE = 0, then the Buck will run in Auto-PFM.

bit 5-0 **VSET[5:0]:** Output Voltage Selection for Low-Power Modes Status bits
Default = 1.25V for MCP16502AC.

Note 1: Default = 1.25V, see the VSET[5:0] table.

REGISTER 4-26: OUT3-HIB: BUCK3 HIBERNATE MODE (0x32)

R/W-0	R/W-0	R/W-1(1)	R/W-0(1)	R/W-0(1)	R/W-1(1)	R/W-1(1)	R/W-1(1)
EN	MODE	VSET[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in Hibernate Mode Status bit
If EN = 1, then it is regulator-enabled.

bit 6 **MODE:** Mode in Hibernate Mode Status bit
If MODE = 1, then the Buck will run in FPWM, else if MODE = 0, then the Buck will run in Auto-PFM.

bit 5-0 **VSET[5:0]:** Output Voltage Selection for Hibernate Mode Status bits
Default = 1.25V for MCP16502AC.

Note 1: Default = 1.25V, see the VSET[5:0] table.

REGISTER 4-27: OUT3-HPM: BUCK3 HIGH-PERFORMANCE MODE (0x33)

R/W-1	R/W-1	R/W-1(1)	R/W-0(1)	R/W-0(1)	R/W-1(1)	R/W-1(1)	R/W-1(1)
EN	MODE	VSET[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in High-Performance Mode Status bit
If EN = 1, then it is regulator-enabled.

bit 6 **MODE:** Mode in High-Performance Mode Status bit
If MODE = 1, then the Buck will run in FPWM, else if MODE = 0, then the Buck will run in Auto-PFM.

bit 5-0 **VSET[5:0]:** Output Voltage Selection for High-Performance Mode Status bits
Default = 1.25V for MCP16502AC.

Note 1: Default = 1.25V, see the VSET[5:0] table.

REGISTER 4-28: OUT3-SEQ: BUCK3 SEQUENCING (0x34)

R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
SSR[1:0]		SEQ[1:0]		SEQEN	DELAY[2:0]		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **SSR[1:0]:** Soft-Start Rate bits
Soft start rate selection bits.

bit 5-4 **SEQ[1:0]:** Start-up Sequence Step bits
Start-up sequence step assignment bits.

bit 3 **SEQEN:** Start-up Sequence Enable bit
SEQEN = 0 regulator will NOT start at the assigned step. If SEQEN = 0, the SSD and POK flags will be neglected in the start-up sequence.

bit 2-0 **DELAY[2:0]:** Time Delay bits
Time delay from the completion of the previous start-up sequence step or start-up event to the turn-on (beginning of soft start).

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REGISTER 4-29: OUT3-CFG: BUCK3 CONFIGURATION (0x35)

R/W-1	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
FLTMSK	HCPEN	DISCH	PHASE	DVSR[1:0]		REN	RCON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **FLTMSK:** Fault Masking bit

If this bit is 1, it will prevent nINTO from being asserted low upon FLT = 1.

bit 6 **HCPEN:** Short-Circuit Protection Hiccup Mode Enable bit

If HCPEN = 1, a short-circuit event will cause a Hiccup mode response with unlimited soft start retries, without shutting down the other channels.

If HCPEN = 0, a short-circuit event on the channel will cause immediate shutdown of ALL channels and a new start-up sequence will automatically be attempted after a 100 ms delay.

bit 5 **DISCH:** Active Output Discharge Control bit

DISCH = 1 enables active output discharge when channel is turned off; DISCH = 0 disables it.

bit 4 **PHASE:** Regulator Phase Control bit

Set this bit to '1' for regulator to operate 180° out of phase with the oscillator, clear this bit to '0' for regulator to operate in phase with the oscillator.

bit 3-2 **DVSR[1:0]:** Dynamic Voltage Scaling Rate bits

Dynamic Voltage Scaling rate programming bits.

bit 1 **REN:** Register Enable bit

Register Enable Bit, used in combination with RCON.

If RCON = 0, the value of REN has no effect. If RCON = 1, setting REN = 1 enables channel and REN = 0 disables it, regardless of the current status.

Mode of operation (FPWM or Auto-PFM) is still controlled by the MODE bits.

bit 0 **RCON:** Register Enable Control bit

This bit is used in combination with the REN bit.

REGISTER 4-30: OUT4-A: BUCK4 ACTIVE MODE (0x41)

R/W-1	R/W-1	R/W-1(1)	R/W-1(1)	R/W-1(1)	R/W-1(1)	R/W-0(1)	R/W-1(1)
EN	MODE	VSET[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in Active Status bit
If EN = 1, the regulator is enabled.

bit 6 **MODE:** Mode in Active Status bit
If MODE = 1, then the Buck will run in FPWM, else if MODE = 0, then the Buck will run in Auto-PFM.

bit 5-0 **VSET[5:0]:** Output Voltage Selection for Active Status bits
Default = 1.8V for MCP16502AC.

Note 1: Default = 1.8V, see the VSET[5:0] table.

REGISTER 4-31: OUT4-LPM: BUCK4 LOW-POWER MODE (0x30)

R/W-1	R/W-0	R/W-1(1)	R/W-1(1)	R/W-1(1)	R/W-1(1)	R/W-0(1)	R/W-1(1)
EN	MODE	VSET[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in Low-Power Modes Status bit
If EN = 1, then it is regulator-enabled.

bit 6 **MODE:** Mode in Low-Power Mode Status bit
If MODE = 1, then the Buck will run in FPWM, else if MODE = 0, then the Buck will run in Auto-PFM.

bit 5-0 **VSET[5:0]:** Output Voltage Selection for Low-Power Modes Status bits
Default = 1.8V for MCP16502AC.

Note 1: Default = 1.8V, see the VSET[5:0] table.

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REGISTER 4-32: OUT4-HIB: BUCK4 HIBERNATE MODE (0x42)

R/W-1	R/W-0	R/W-1(1)	R/W-1(1)	R/W-1(1)	R/W-1(1)	R/W-0(1)	R/W-1(1)
EN	MODE	VSET[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in Hibernate Mode Status bit
If EN = 1, then it is regulator-enabled.

bit 6 **MODE:** Mode in Hibernate Mode Status bit
If MODE = 1, then the Buck will run in FPWM, else if MODE = 0, then the Buck will run in Auto-PFM.

bit 5-0 **VSET[5:0]:** Output Voltage Selection for Hibernate Mode Status bits
Default = 1.8V for MCP16502AC.

Note 1: Default = 1.8V, see the VSET[5:0] table.

REGISTER 4-33: OUT4-HPM: BUCK4 HIGH-POWER MODE (0x43)

R/W-1	R/W-1	R/W-1(1)	R/W-1(1)	R/W-1(1)	R/W-1(1)	R/W-0(1)	R/W-1(1)
EN	MODE	VSET[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in High-Performance Mode Status bit
If EN = 1, then it is regulator-enabled.

bit 6 **MODE:** Mode in High-Performance Mode Status bit
If MODE = 1, then the Buck will run in FPWM, else if MODE = 0, then the Buck will run in Auto-PFM.

bit 5-0 **VSET[5:0]:** Output Voltage Selection for High-Performance Mode Status bits
Default = 1.8V for MCP16502AC.

Note 1: Default = 1.8V, see the VSET[5:0] table.

REGISTER 4-34: OUT4-SEQ: BUCK4 SEQUENCING (0x44)

R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
SSR[1:0]		SEQ[1:0]		SEQEN	DELAY[2:0]		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **SSR[1:0]:** Soft Start Rate bits
Soft start rate selection bits.

bit 5-4 **SEQ[1:0]:** Start-up Sequence Step bits
Start-up sequence step assignment bits.

bit 3 **SEQEN:** Start-up Sequence Enable bit
SEQEN = 0 regulator will NOT start at the assigned step. If SEQEN = 0, the SSD and POK flags will be neglected in the start-up sequence.

bit 2-0 **DELAY[2:0]:** Time Delay bits
Time delay from the completion of the previous start-up sequence step or start-up event to the turn-on (beginning of soft start).

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REGISTER 4-35: OUT4-CFG: BUCK4 CONFIGURATION (0x45)

R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTMSK	HCPEN	DISCH	PHASE	DVSR[1:0]		REN	RCON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **FLTMSK:** Fault Masking bit
If this bit is '1', it will prevent nINTO from being asserted low upon FLT = 1.

bit 6 **HCPEN:** Short-Circuit Protection Hiccup Mode Enable bit
If HCPEN = 1, a short-circuit event will cause a Hiccup mode response with unlimited soft start retries, without shutting down the other channels.
If HCPEN = 0, a short-circuit event on the channel will cause immediate shutdown of ALL channels and a new start-up sequence will automatically be attempted after a 100 ms delay.

bit 5 **DISCH:** Active Output Discharge Control bit
DISCH = 0 enables active output discharge when the channel is turned off; DISCH = 0 disables it.

bit 4 **PHASE:** Regulator Phase Control bit
Set this bit to '1' for the regulator to operate 180° out of phase with the oscillator; clear this bit to '0' for the regulator to operate in phase with the oscillator.

bit 3-2 **DVSR[1:0]:** Dynamic Voltage Scaling Rate bits
Dynamic Voltage Scaling rate programming bits.

bit 1 **REN:** Register Enable bit
This bit is used in combination with RCON. If RCON = 0, the value of REN has no effect. If RCON = 1, setting REN = 1 enables the channel and REN = 0 disables it, regardless of the current status.
Mode of operation (FPWM or Auto-PFM) is still controlled by the MODE bits.

bit 0 **RCON:** Register Enable Control bit
This bit is used in combination with the REN bit.

REGISTER 4-36: LDO1-A: LDO1 ACTIVE MODE (0x50)

R/W-1	r-0	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)
EN	—	VSET[5:0]					
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in Active Status bit
If EN = 1, the regulator is enabled.

bit 6 **Reserved:** Maintain as '0'

bit 5-0 **VSET[5:0]:** Output Voltage Selection for Active Status bits
Default value is pin-selectable.

Note 1: Default code is pin-selectable.

REGISTER 4-37: LDO1-LPM: LDO1 LOW-POWER MODE (0x51)

R/W-1	r-0	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)
EN	—	VSET[5:0]					
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in Low-Power Modes Status bit
If EN = 1, then it is regulator-enabled.

bit 6 **Reserved:** Maintain as '0'

bit 5-0 **VSET[5:0]:** Output Voltage Selection for Low-Power Modes Status bits
Default value is pin-selectable.

Note 1: Default code is pin-selectable.

REGISTER 4-38: LDO1-HIB: LDO1 HIBERNATE MODE (0x52)

R/W-0	r-0	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)
EN	—	VSET[5:0]					
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in Hibernate Mode Status bit
If EN = 1, then it is regulator-enabled.

bit 6 **Reserved:** Maintain as '0'

bit 5-0 **VSET[5:0]:** Output Voltage Selection for Hibernate Mode Status bits
Default value is pin-selectable.

Note 1: Default code is pin-selectable.

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REGISTER 4-39: LDO1-HPM: LDO1 HIGH-PERFORMANCE MODE (0x53)

R/W-1	r-0	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)
EN	—	VSET[5:0]					
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in High-Performance Mode Status bit
If EN = 1, then it is regulator-enabled.

bit 6 **Reserved:** Maintain as '0'

bit 5-0 **VSET[5:0]:** Output Voltage Selection for High-Performance Mode Status bits
Default value is pin-selectable.

Note 1: Default code is pin-selectable.

REGISTER 4-40: LDO1-SEQ: LDO1 SEQUENCING (0x54)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1
SSR[1:0]		SEQ[1:0]		SEQEN	DELAY[2:0]		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **SSR[1:0]:** Soft Start Rate bits
Soft start rate selection bits.

bit 5-4 **SEQ[1:0]:** Start-up Sequence Step bits
Start-up sequence step assignment bits.

bit 3 **SEQEN:** Start-up Sequence Enable bit
SEQEN = 0 regulator will NOT start at the assigned step. If SEQEN = 0, the SSD and POK flags will be neglected in the start-up sequence.

bit 2-0 **DELAY[2:0]:** Time Delay bits
Time delay from the completion of the previous start-up sequence step or start-up event to the turn-on (beginning of soft start).

REGISTER 4-41: LDO1-CFG: LDO1 CONFIGURATION (0x55)

R/W-1	r-0	R/W-1	r-1	R/W-0	R/W-0	R/W-0	R/W-0
FLTMSK	—	DISCH	—	DVSR[1:0]		REN	RCON
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **FLTMSK:** Fault Masking bit
If this bit is 1, it will prevent nINTO from being asserted low upon FLT = 1.

bit 6 **Reserved:** Maintain as '0'

bit 5 **DISCH:** Active Output Discharge Control bit
DISCH = 1 enables active output discharge when LDO is turned off; DISCH = 0 disables it.

bit 4 **Reserved:** Maintain as '1'

bit 3-2 **DVSR[1:0]:** Dynamic Voltage Scaling Rate bits
Dynamic Voltage Scaling rate programming bits.

bit 1 **REN:** Register Enable bit
This bit is used in combination with RCON. If RCON = 0, the value of REN has no effect. If RCON = 1, setting REN = 1 enables the channel and REN = 0 disables it, regardless of the current status.
Mode of operation (FPWM or Auto-PFM) is still controlled by the MODE bits.

bit 0 **RCON:** Register Enable Control bit
This bit is used in combination with REN.

REGISTER 4-42: LDO2-A: LDO2 ACTIVE MODE (0x60)

R/W-0	r-0	R/W-1(1)	R/W-1(1)	R/W-0(1)	R/W-1(1)	R/W-1(1)	R/W-1(1)
EN	—	VSET[5:0]					
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in Active Status bit
If EN = 1, the regulator is enabled.

bit 6 **Reserved:** Maintain as '0'

bit 5-0 **VSET[5:0]:** Output Voltage Selection for Active Status bits
Default value is 3.3V for MCP16502AC variant.

Note 1: Default = 3.3V, see the VSET[5:0] table.

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REGISTER 4-43: LDO2-LPM: LDO2 LOW-POWER MODE (0x61)

R/W-0	r-0	R/W-1[1]	R/W-1[1]	R/W-0[1]	R/W-1[1]	R/W-1[1]	R/W-1[1]
EN	—	VSET[5:0]					
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in Low-Power Modes Status bit
If EN = 1, then it is regulator-enabled.

bit 6 **Reserved:** Maintain as '0'

bit 5-0 **VSET[5:0]:** Output Voltage Selection for Low-Power Modes Status bits
Default value is 3.3V for MCP16502AC variant.

Note 1: Default = 3.3V, see the VSET[5:0] table.

REGISTER 4-44: LDO2-HIB: LDO2 HIBERNATE MODE (0x62)

R/W-0	r-0	R/W-1[1]	R/W-1[1]	R/W-0[1]	R/W-1[1]	R/W-1[1]	R/W-1[1]
EN	—	VSET[5:0]					
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in Hibernate Mode Status bit
If EN = 1, then it is regulator-enabled.

bit 6 **Reserved:** Maintain as '0'

bit 5-0 **VSET[5:0]:** Output Voltage Selection for Hibernate Mode Status bits
Default value is 3.3V for MCP16502AC variant.

Note 1: Default = 3.3V, see the VSET[5:0] table.

REGISTER 4-45: LDO2-HPM: LDO2 HIGH-POWER MODE (0x63)

R/W-0	r-0	R/W-1(1)	R/W-1(1)	R/W-0(1)	R/W-1(1)	R/W-1(1)	R/W-1(1)
EN	—	VSET[5:0]					
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN:** Enable in High-Performance Mode Status bit
If EN = 1, then it is regulator-enabled.

bit 6 **Reserved:** Maintain as '0'

bit 5-0 **VSET[5:0]:** Output Voltage Selection for High-Performance Mode Status bits
Default value is 3.3V for MCP16502AC variant.

Note 1: Default = 3.3V, see the VSET[5:0] table.

REGISTER 4-46: LDO2-SEQ: LDO2 SEQUENCING (0x64)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
SSR[1:0]		SEQ[1:0]		SEQEN	DELAY[2:0]		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **SSR[1:0]:** Soft Start Rate bits
Soft start rate selection bits.

bit 5-4 **SEQ[1:0]:** Start-up Sequence Step bits
Start-up sequence step assignment bits.

bit 3 **SEQEN:** Start-up Sequence Enable bit
SEQEN = 0 regulator will NOT start at the assigned step. If SEQEN = 0, the SSD and POK flags will be neglected in the start-up sequence.

bit 2-0 **DELAY[2:0]:** Time Delay bits
Time delay from the completion of the previous start-up sequence step or start-up event to the turn-on (beginning of soft start).

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REGISTER 4-47: LDO2-CFG: LDO2 CONFIGURATION (0x65)

R/W-1	r-0	R/W-1	r-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTMSK	—	DISCH	—	DVSR[1:0]		REN	RCON
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **FLTMSK:** Fault Masking bit

If this bit is '1', it will prevent nINTO from being asserted low upon FLT = 1.

bit 6 **Reserved:** Maintain as '0'

bit 5 **DISCH:** Discharge Control bit

SEQEN = 0 regulator will NOT start at the assigned step. If SEQEN = 0, the SSD and POK flags will be neglected in the start-up sequence.

bit 4 **Reserved:** Maintain as '0'

bit 3-2 **DVSR[1:0]:** Dynamic Voltage Scaling Rate bits

Dynamic Voltage Scaling rate programming bits.

bit 1 **REN:** Register Enable bit

This bit is used in combination with RCON. If RCON = 0, the value of REN has no effect. If RCON = 1, setting REN = 1 enables the channel and REN = 0 disables it, regardless of the current status.

Mode of operation (FPWM or Auto-PFM) is still controlled by the MODE bits.

bit 0 **RCON:** Register Enable Control bit

This bit is used in combination with REN.

4.7 Device Variants Default Settings

The summary of all currently available device variants with their default register settings is shown in Table 4-15 below:

TABLE 4-15: DEFAULT REGISTERS SETTINGS VS. MCP16502 DEVICE VARIANTS

SELVx Status	Register Name	Register Address	Register Default Settings of MCP16502 Variants				
			AA	AB	AC	AD	AE
Irrelevant	SYS-ADR	0x00	0xDB	0xDB	0xDB	0xDB	0xDB
Irrelevant	SYS-ID	0x01	0x10	0x20	0x30	0x40	0x50
Irrelevant	SYS-TMG	0x02	0x54	0x54	0x54	0x54	0x54
Irrelevant	SYS-CFG	0x03	0xC0	0xC0	0xC0	0xC0	0xC0
Irrelevant	STS-SYS	0x04	0x00	0x00	0x00	0x00	0x00
Irrelevant	STS-B1	0x05	0x00	0x00	0x00	0x00	0x00
Irrelevant	STS-B2	0x06	0x00	0x00	0x00	0x00	0x00
Irrelevant	STS-B3	0x07	0x00	0x00	0x00	0x00	0x00
Irrelevant	STS-B4	0x08	0x00	0x00	0x00	0x00	0x00
Irrelevant	STS-L1	0x09	0x00	0x00	0x00	0x00	0x00
Irrelevant	STS-L2	0x0A	0x00	0x00	0x00	0x00	0x00
Irrelevant	OUT1-A	0x10	0xF7	0xF7	0xF7	0xF7	0xF7
Irrelevant	OUT1-LPM	0x11	0xB7	0xB7	0xB7	0xB7	0xB7
Irrelevant	OUT1-HIB	0x12	0x37	0x37	0x37	0x37	0x37
Irrelevant	OUT1-HPM	0x13	0xF7	0xF7	0xF7	0xF7	0xF7
Irrelevant	OUT1-SEQ	0x14	0x09	0x09	0x09	0x09	0x09
Irrelevant	OUT1-CFG	0x15	0xB0	0xB0	0xB0	0xB0	0xB0
SELV2 = Low	OUT2-A	0x20	0xE5	0xE5	0xE5	0xE5	0xE5
SELV2 = High-Z	OUT2-A	0x20	0xEB	0xEB	0xEB	0xEB	0xEB
SELV2 = High	OUT2-A	0x20	0xFD	0xFD	0xFD	0xFD	0xFD
SELV2 = Low	OUT2-LPM	0x21	0xA5	0xA5	0xA5	0xA5	0xA5
SELV2 = High-Z	OUT2-LPM	0x21	0xAB	0xAB	0xAB	0xAB	0xAB
SELV2 = High	OUT2-LPM	0x21	0xBD	0xBD	0xBD	0xBD	0xBD
SELV2 = Low	OUT2-HIB	0x22	0xA5	0xA5	0xA5	0xA5	0xA5
SELV2 = High-Z	OUT2-HIB	0x22	0xAB	0xAB	0xAB	0xAB	0xAB
SELV2 = High	OUT2-HIB	0x22	0xBD	0xBD	0xBD	0xBD	0xBD
SELV2 = Low	OUT2-HPM	0x23	0xE5	0xE5	0xE5	0xE5	0xE5
SELV2 = High-Z	OUT2-HPM	0x23	0xEB	0xEB	0xEB	0xEB	0xEB
SELV2 = High	OUT2-HPM	0x23	0xFD	0xFD	0xFD	0xFD	0xFD
Irrelevant	OUT2-SEQ	0x24	0x1D	0x1D	0x1D	0x1D	0x1D
Irrelevant	OUT2-CFG	0x25	0xA0	0xA0	0xA0	0xA0	0xA0
Irrelevant	OUT3-A	0x30	0xE7	0xE3	0xE7	0xE3	0xE3
Irrelevant	OUT3-LPM	0x31	0xA7	0xA3	0xA7	0xA3	0xA3
Irrelevant	OUT3-HIB	0x32	0x27	0x23	0x27	0x23	0x23
Irrelevant	OUT3-HPM	0x33	0xE7	0xE3	0xE7	0xE3	0xE3
Irrelevant	OUT3-SEQ	0x34	0x2C	0x2C	0x2C	0x2C	0x2C
Irrelevant	OUT3-CFG	0x35	0xB0	0xB0	0xB0	0xB0	0xB0
Irrelevant	OUT4-A	0x40	0x61	0xE3	0xFD	0xE3	0x63
Irrelevant	OUT4-LPM	0x41	0x21	0xA3	0xBD	0xA3	0x23
Irrelevant	OUT4-HIB	0x42	0x21	0x23	0xBD	0x23	0x23

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TABLE 4-15: DEFAULT REGISTERS SETTINGS VS. MCP16502 DEVICE VARIANTS (CONTINUED)

SELVx Status	Register Name	Register Address	Register Default Settings of MCP16502 Variants				
			AA	AB	AC	AD	AE
Irrelevant	OUT4-HPM	0x43	0x61	0xE3	0xFD	0xE3	0x63
Irrelevant	OUT4-SEQ	0x44	0x24	0x2C	0x1C	0x2C	0x24
Irrelevant	OUT4-CFG	0x45	0xA0	0xA0	0xA0	0xA0	0xA0
SELVL1 = Low	LDO1-A	0x50	0x99	0x99	0x99	0x99	0x99
SELVL1 = High-Z	LDO1-A	0x50	0xA7	0xA7	0xA7	0xA7	0xA7
SELVL1 = High	LDO1-A	0x50	0xB7	0xB7	0xB7	0xB7	0xB7
SELVL1 = Low	LDO1-LPM	0x51	0x99	0x99	0x99	0x99	0x99
SELVL1 = High-Z	LDO1-LPM	0x51	0xA7	0xA7	0xA7	0xA7	0xA7
SELVL1 = High	LDO1-LPM	0x51	0xB7	0xB7	0xB7	0xB7	0xB7
SELVL1 = Low	LDO1-HIB	0x52	0x19	0x19	0x19	0x19	0x19
SELVL1 = High-Z	LDO1-HIB	0x52	0x27	0x27	0x27	0x27	0x27
SELVL1 = High	LDO1-HIB	0x52	0x37	0x37	0x37	0x37	0x37
SELVL1 = Low	LDO1-HPM	0x53	0x99	0x99	0x99	0x99	0x99
SELVL1 = High-Z	LDO1-HPM	0x53	0xA7	0xA7	0xA7	0xA7	0xA7
SELVL1 = High	LDO1-HPM	0x53	0xB7	0xB7	0xB7	0xB7	0xB7
Irrelevant	LDO1-SEQ	0x54	0x09	0x09	0x09	0x09	0x09
Irrelevant	LDO1-CFG	0x55	0xA0	0xA0	0xA0	0xA0	0xA0
Irrelevant	LDO2-A	0x60	0x37	0x37	0x37	0x99	0x37
Irrelevant	LDO2-LPM	0x61	0x37	0x37	0x37	0x99	0x37
Irrelevant	LDO2-HIB	0x62	0x37	0x37	0x37	0x99	0x37
Irrelevant	LDO2-HPM	0x63	0x37	0x37	0x37	0x99	0x37
Irrelevant	LDO2-SEQ	0x64	0x01	0x01	0x01	0x1C	0x01
Irrelevant	LDO2-CFG	0x65	0xA0	0xA0	0xA0	0xA0	0xA0

4.8 I²C Interface Description

The MCP16502 is a Fast-mode plus device, supporting data transfers at up to 1 Mbit/s as described in the I²C bus specification.

The MCP16502 is a slave only device without clock stretching capability.

The MCP16502 assumes that the I²C logic levels on the bus are generated by a device operating from a nominal supply voltage of 3.3V (with ±10% tolerance). This is typically the I/O voltage generated by Buck1 (VDDIO). Therefore, V_{IH} and V_{IL} levels are not related to the SVIN voltage value. Typically, the SDA and SCL lines should not be pulled up to the MCP16502 SVIN voltage, but to the VDDIO voltage I²C master interface supply voltage (3.3V nominal).

The MCP16502 I²C interface is always accessible, even in the OFF state, as long as the SVIN pin is powered and above the UVLO threshold. In the OFF state, the VDDIO voltage from Buck1 is turned off, and therefore, the I²C pull-up voltage rail must be provided externally.

4.8.1 DEVICE ADDRESS

The MCP16502 uses 7-bit addressing (0x5B by default).

4.8.2 ACKNOWLEDGE

The number of data bytes transferred between the Start and Stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one Acknowledge bit. The Acknowledge bit is a high level put on the bus by the transmitter, whereas the master generates an extra Acknowledge-related clock pulse. The device that Acknowledges has to pull down the SDA line during the Acknowledge clock pulse, so that the SDA line is a stable low during the high period of the Acknowledge-related clock pulse. Setup and hold times must be taken into account.

A slave receiver, which is addressed, must generate an Acknowledge after the reception of each byte.

Also, a master receiver must generate an Acknowledge after the reception of each byte that has been clocked out of the slave transmitter, except on the last received byte. A master receiver must signal an end of data to the transmitter by not generating an Acknowledge on the last byte that has been clocked out of the slave transmitter. In this event, the transmitter must leave the data line high to enable the master to generate a Stop condition.

4.8.3 BUS TRANSACTIONS

4.8.3.1 Single Write

The first seven bits of the first byte make up the slave address. The eighth bit is the LSB (Least Significant Bit). It determines the direction of the message (R/W). A '0' in the least significant position of the first byte means that the master will write information to a selected slave. A '1' in this position means that the master will read information from the slave. When an address is sent, each device in a system compares the first seven bits after the Start condition with its address. If they match, the device considers itself addressed by the master as a slave-receiver, or slave-transmitter, depending on the R/W bit.

A command byte is a data byte which selects a register on the device (address of the register that needs to be written).

The data to port are the 8-bit data that must be written to the selected register. This is followed by the Acknowledge from the slave and then the Stop condition.

The Write command is as follows and it is illustrated in the timing diagram from Figure 4-12 below.

1. Send start sequence.
2. Send 7-bit slave address.
3. Send the R/W bit – '0' to indicate a write operation.
4. Wait for Acknowledge from the slave.
5. Send the command byte – address that needs to be written.
6. Wait for Acknowledge from the slave.
7. Receive the 8-bit data from the master and write them to the Slave register indicated in Step 5, starting from the MSB.
8. Acknowledge from the slave.
9. Send stop sequence.

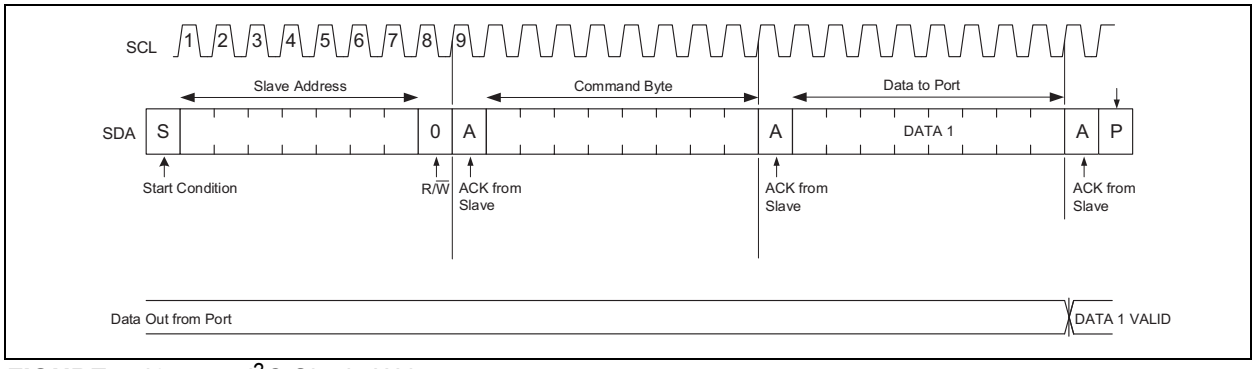


FIGURE 4-12: *I²C Single Write.*

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Writing to a read-only register, a non-existing or not user-accessible register will still generate an Acknowledge (ACK) by the MCP16502 after the command byte, but it will have no effect.

4.8.3.2 Block Write (Auto-Increment Mode)

The MCP16502 can receive multiple data bytes after a single address byte and automatically increments its Register Pointer to block fill internal volatile registers. This command writes the first data byte to a register that is specified through the command byte and all the following data bytes to the subsequent registers.

Byte data are latched after individual bytes are received, so multibyte transfers could be corrupted if interrupted midstream.

The Block/Auto-Increment Write command is as follows:

1. Send start sequence.
2. Send 7-bit slave address.
3. Send the R/W bit = 0 to indicate a Write operation.
4. Wait for Acknowledge from the slave.
5. Send the command byte – first register address that needs to be written.
6. Wait for Acknowledge from the slave.
7. Receive the 8-bit data from the master and write them to the Slave register indicated in Step 5, starting from the MSB.
8. Acknowledge from the slave
9. Receive the 8-bit data from the master and write them to the next slave register address, starting from MSB.
10. Acknowledge from the slave.
11. Repeat Steps 9 and 10 until the entire data are sent.
12. Send the stop sequence.

In Block Write, the register order will be automatically incremented by one step, regardless of the register order. So, for example, after writing to register location 0x15, the next register to be written will be 0x16, not 0x20.

Writing to non-existent or not accessible register addresses will still generate an ACK by the MCP16502, after the command byte, but it will have no effect.

If the master keeps writing data beyond the last register location, the MCP16502 still generates an ACK on each received byte, but these data do not have any effect on the MCP16502 (i.e., disregarded). There is no register address wraparound.

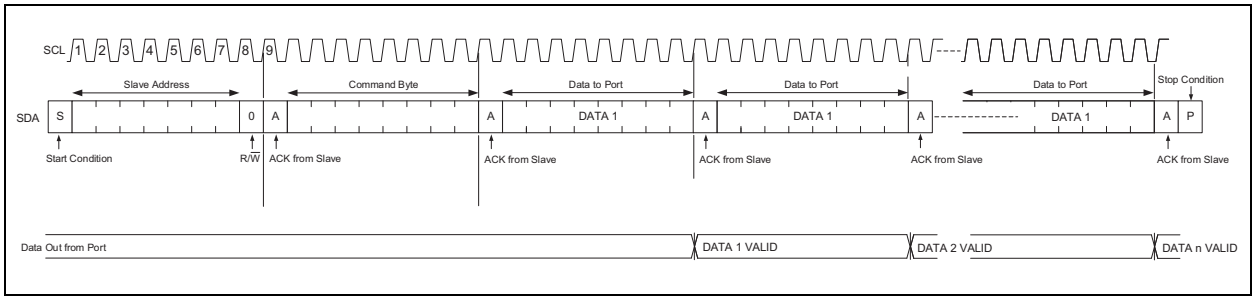


FIGURE 4-13: *Block Write.*

4.8.3.3 Single Read

In Single Read, a single byte is read from a device, from a designated register. The register is specified through the command byte.

The Read command is as follows, and is illustrated in the timing diagram in Figure 4-14.

1. Send start sequence.
2. Send 7-bit slave address.
3. Send the R/W bit = 0 to indicate a Write operation.
4. Wait for Acknowledge from the slave.
5. Send the register address that needs to be read.
6. Wait for Acknowledge from the slave.
7. Send start sequence again (Repeated Start condition).
8. Send the 7-bit slave address.
9. Send the R/W bit = 1 to indicate a Read operation.
10. Wait for Acknowledge from the slave.
11. Receive the 8-bit data from the slave, starting from MSB.
12. Acknowledge from the master (NACK to signal the end of data transfer).
13. Send the stop sequence.

If the Master attempts to read from an invalid register location, the MCP16502 will send out 0xFF data (all '1's).

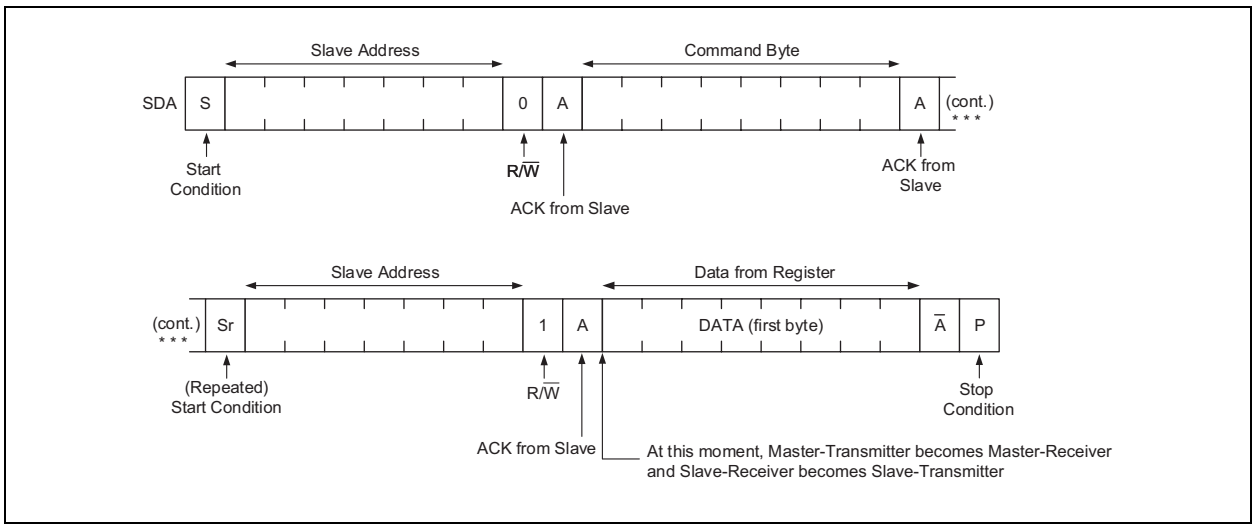


FIGURE 4-14: *Single Read.*

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4.8.3.4 Block Read (Auto-Increment Mode)

This command reads a block of bytes, starting from a designated register that is specified through the command byte. The address gets incremented by one automatically and the registers are read in order starting from the address provided by the command byte.

The Block/Auto-Increment Read command is as follows and it is illustrated in the timing diagram from Figure 4-15 below.

1. Send start sequence.
2. Send 7-bit slave address.
3. Send the R/W bit = 0 to indicate a Write operation.
4. Wait for Acknowledge from the slave.
5. Send the command byte – initial address that needs to be read.
6. Wait for Acknowledge from the slave.
7. Send start sequence again (Repeated Start, Sr).
8. Send the 7-bit slave address.
9. Send R/W bit = 1 to indicate a Read operation.
10. Wait for Acknowledge from the slave.
11. Receive the 8-bit data from the Slave register indicated in Step 5, starting from the MSB.
12. Acknowledge from the master receiver.
13. Receive the 8-bit data from the next register, starting from the MSB.
14. Acknowledge from the master receiver.
15. Repeat Steps 13 and 14 until the last byte.
16. Stop sequence is sent.

Note:	On the last byte, the master receiver issues a NACK in place of an ACK to signal the end of the data transfer.

In Block Read, the register order will be automatically incremented by one step, regardless of the register order. So, for example, after reading from register location 0x15, the next register address to be read will be 0x16, not 0x20.

Reading from non-existent or not accessible register addresses will stream out 0xFF.

Also note that if the master keeps reading data beyond the last register location, the MCP16502 streams out 0xFF (all '1's). There is no register address wraparound.

In Block Read Auto-Increment mode, the master receiver must signal an end-of-data to the transmitter by not generating an Acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line as high to enable the master to generate a Stop condition.

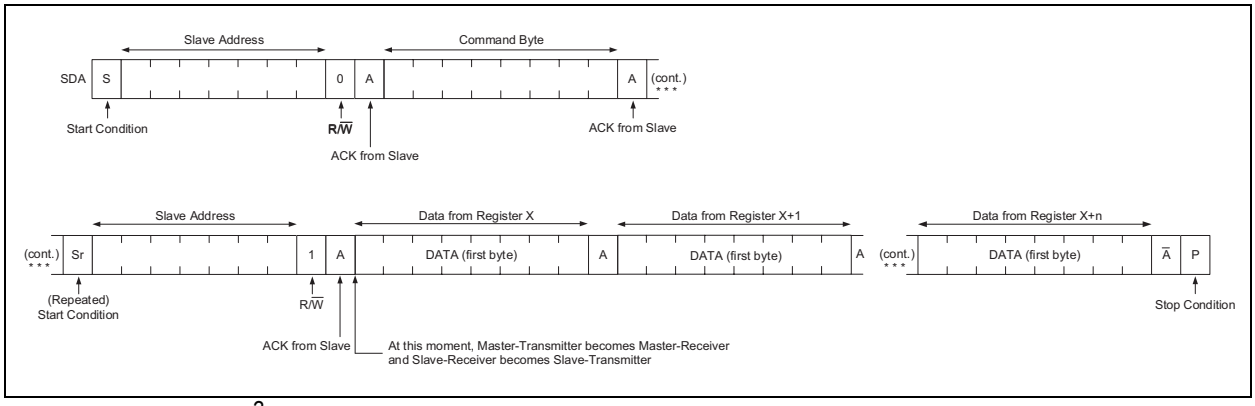


FIGURE 4-15: *I²C Block Read.*

4.8.3.5 I²C Interface Disable

While not necessarily contained in a well-designed implementation, the MCP16502 also supports I²C interface disabling.

This is achieved by issuing three separated single Write commands as follows (ADDRESS equals the device address in 7-bit format, default = 0x5B):

1. ADDRESS = 0x5B, COMMAND = 0xEA, DATA = 0xBD
2. ADDRESS = 0x5B, COMMAND = 0xE9, DATA = 0xBD
3. ADDRESS = 0x5B, COMMAND = 0xEC, DATA = 0xBD

Upon an ACK of the last byte, the I²C interface will no longer respond to the device address or any other bus transaction.

To enable the I²C interface again, power (SVIN) must be cycled.

5.0 APPLICATION INFORMATION

5.1 Recommended External Components

Table 5-1 lists possible part numbers that can be used in the MCP16502 application. Please refer to the **"Typical Application Circuit"** section for component designators' reference.

TABLE 5-1: RECOMMENDED EXTERNAL COMPONENTS

Item	Part Number	Manufacturer	Description
C1-C4	C1608X5R1A226M080AC	TDK Corporation	Capacitor, 22 µF, 6.3V/10V, X5R, 20%, Size 0603
	GRM188R61A226ME15D	Murata Electronics®	
	C1608X5R0J226M080AC	TDK Corporation	
	GRM188R60J226MEA0	Murata Electronics	
	JMK107BBJ226MA	Taiyo Yuden Co., Ltd.	
	CL10A226MQ8NRNC	Samsung Electro-Mechanics America, Inc.	
	06036D226MAT2A	AVX Corporation	
C5-C8, C10-C11 (for 300 mA max. LDO current), C12	C1005X5R1A475M050BC	TDK Corporation	Capacitor, 4.7 µF, 10V, X5R, 10%/20%, Size 0402
	GRM155R61A475MEAA	Murata Electronics	
	LMK105BBJ475MV	Taiyo Yuden Co., Ltd.	
	CL05A475M(K)P5NRNC	Samsung Electro-Mechanics America, Inc.	
	0402ZD475MAT2A	AVX Corporation	
C9, C10-C11 (for 150 mA max. LDO current)	C1005X5R1A225K050BC	TDK Corporation	Capacitor, 2.2 µF, 10V/16V, X5R, 10%, Size 0402
	GRM155R61C225KE11	Murata Electronics	
	LMK105BJ225KV	Taiyo Yuden Co., Ltd.	
	CL05A225KP5NSNC	Samsung Electro-Mechanics America, Inc.	
	0402ZD225KAT2A	AVX Corporation	
R1	RC0402KR-07100KL	Yageo Corporation	Resistor, 100 kΩ, 5%, Size 0402
R2-R3	RC0402KR-0710K0L	Yageo Corporation	Resistor, 10 kΩ, 5%, Size 0402
R4-R5	RC0402KR-072K20L	Yageo Corporation	Resistor, 2.2 kΩ, 5%, Size 0402
L1, L2, L3, L4	MLP2520W1R5MT0S1	TDK Corporation	1.5 µH, 1.8A, 75 mΩ, Size 2520, Multilayer Ferrite
	LQM2HPN1R5MGH	Murata Electronics	1.5 µH, 1.6A, 65 mΩ, Size 2520, Multilayer Ferrite
	VLS252012CX-1R5M	TDK Corporation	1.5 µH, 2.3A, 62 mΩ, Size 2520, Wirewound Ferrite
	LQH2HPN1R5MGR	Murata Electronics	1.5 µH, 1.85A, 87 mΩ, Size 2520, Wirewound Ferrite
	CDPH28D11FNP-1R5MC	Sumida Corporation	1.5 µH, 1.74A, 69 mΩ, Size 3.0 mm x 3.2 mm, Wirewound Ferrite
	DFE252012P-1R5M=P2	Murata Electronics	1.5 µH, 2.6A, 60 mΩ Max, Size 2520, Metal Alloy
	DFE252012P-2R2M=P2	Murata Electronics	2.2 µH, 2.2A, 84 mΩ Max, Size 2520, Metal Alloy
	VLS252012HBX-1R5M-1	TDK Corporation	1.5 µH, 2.5A, 68 mΩ, Size 2520, Metal Alloy
	VLS252012HBX-2R2M-1	TDK Corporation	2.2 µH, 2.04A, 85 mΩ, Size 2520, Metal Alloy
	74438324015	Würth Elektronik	1.5 µH, 2.2A, 82 mΩ, Size 2520, Metal Alloy
	74438324022	Würth Elektronik	2.2 µH, 1.6A, 123 mΩ, Size 2520, Metal Alloy
	74404024015	Würth Elektronik	1.5 µH, 1.9A, 65 mΩ, Size 2520, Wirewound Ferrite
	74405024022	Würth Elektronik	2.2 µH, 1.6A, 100 mΩ, Size 2520, Wirewound Ferrite

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5.2 Dynamic Voltage Scaling (DVS) Operation

Dynamic Voltage Scaling is not a special mode of operation. When the state machine moves from one state to another, and the content of the regulator voltage in the new state is different from the previous one (assuming the regulator is on in both the initial and final state), the output voltage of the regulator will be automatically updated in 25 mV (or 50 mV for Buck1 and LDOs) increments/decrements to reach the value which is defined for the final state.

This also happens if the regulator voltage is updated through I^2C without any power mode state change. The step rate is programmable and it is derived from the switching frequency clock. The values are described in **Section 4.5.6 "Dynamic Voltage Scaling Rate Programming Bits (t_{ramp})"**.

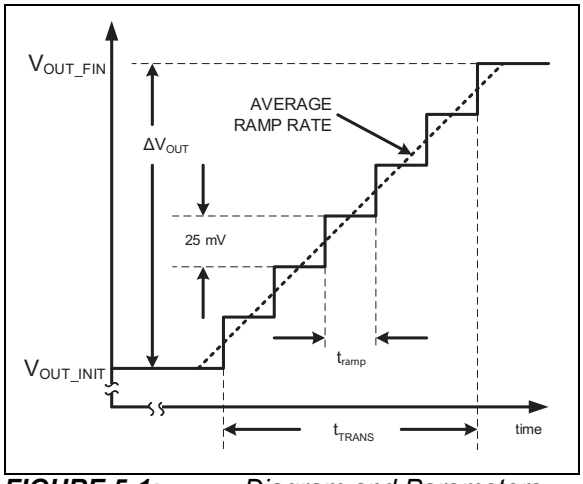


FIGURE 5-1: *Diagram and Parameters.*

Internal filtering time constants for the reference DAC steps and the finite response time of the control loop help in smoothing out the resulting ramp shape visible at the output of the regulator(s).

During DVS transitions:

- The Buck converters will operate in FPWM to allow a predictable transition time in both the rising and falling DVS transitions.
- LDO: When the transition happens in the negative direction (i.e., decreasing voltage), the active discharge load will be activated during the transition in order to speed up the transition time. This is to facilitate the support of dual voltage SD cards.

The POK will not be deasserted during rising DVS transitions because of change in the reference (DAC) voltage. During DVS transition, changes in POK logic value are inhibited until the transition has completed.

5.3 HPM Pin/HPMPEN Bit

The HPM pin is meant to be driven by a GPIO of the host MPU for the purpose of entering a Software-Defined High-Performance mode. Its usage is optional and it should be connected to ground if it is not used.

Other MPUs will typically use the HPM pin to switch Buck4 (VDDCPU rail) to higher voltage, such that higher clock frequencies can be supported (DVS operation, see **Section 5.2 "Dynamic Voltage Scaling (DVS) Operation"**). The required overdrive voltage level in HPM mode needs to be defined by I^2C prior to entering DVS operation. If no action is taken, the HPM voltage value will default to the Active mode default value.

The HPM pin needs to be enabled (unmasked) through I^2C by setting the HPMPEN bit in the SYS-CFG register. If the HPMPEN bit is not set, the internal logic will be insensitive to the HPM pin level, which will always appear internally as a logic '0'.

The HPMPEN bit is not automatically cleared due to a start-up or to a restart sequence after a Fault. Also, the DVS voltage level definition stored in the HPM registers is not reset to the Active mode level. Therefore, if for any reason the HPM pin remains high (or returns to high logic level) during the start-up/restart sequence while the HPMPEN bit has been previously set, the MCP16502 will move to the High-Performance mode immediately after the start-up/restart sequence has successfully terminated. Thus, if the DVS voltage level defined in HPM mode is different than the voltage level defined in Active mode, the channel under consideration will immediately move to the HPM mode voltage level as soon as nRSTO is deasserted.

While the DVS voltage level is normal for the VDDCPU rail generated by Buck4, if the behavior described above is not desirable, the following countermeasures can be considered:

- Connect the HPM pin to a GPIO which is low by default at start-up.
- Clear by software the relevant GPIO at the beginning of the software execution/configuration routine and/or clear the HPMPEN bit by an I^2C command.

Also note that the channel (typically Buck1, VDDIO) powering the MPU voltage domain, to which the GPIO driving the HPM pin belongs, should always be defined as on in HPM mode.

Failing to do so would set the HPM pin low again shortly after it has been set high, thereby generating a cyclic behavior where the relevant channel turns on and off indefinitely.

If the LPM pin goes high (with PWRHLD = High) while HPM is low, the MCP16502 will move to a Low-Power state. If HPM goes high after that, the MCP16502 will ignore it and it will stay in the Low-Power state as long as LPM = High.

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On the other hand, if HPM goes high first (thus PWRHLD = HPM = 1, LPM = 0), the device remains in the HPM state even if LPM is asserted high. To go to the Low-Power state, HPM must be deasserted first.

5.4 Buck1 Hysteretic Control Mode (HCM)/B1HCEN Bit

If Buck1 is set in Auto-PFM mode while the input voltage (e.g., a discharging battery) is decreasing and eventually pushing Buck1 to 100% duty cycle (Bypass mode), the operational no-load quiescent current of the MCP16502 shows some increase due to the augmented switching activity of Buck1.

This is intrinsic to the Auto-PFM architecture. The peaking in the quiescent current is in the 1 mA range, and it may or may not be detrimental to the overall system efficiency and/or battery life, depending mostly on the minimum loading of Buck1.

If the increase in quiescent current when approaching Bypass mode on Buck1 is an important factor for the application, the user can optionally activate a different mode of light load, high-efficiency operation (called Hysteretic Control mode, HCM), where the output voltage is controlled in a hysteretic fashion between the nominal output voltage and 2.9% of it. This is done by setting the B1HCEN bit (Buck1 Hysteretic Control Enable) in the SYS-CFG register through I^2C. This control method significantly reduces the average switching activity of Buck1, especially in the proximity of the bypass operation, at the expense of an increase of the output ripple amplitude.

The user should therefore carefully evaluate the need for activation of HCM for Buck1 and balance the increase in output ripple against the real benefit achieved in prolonging battery life. If the minimum loading on Buck1 is always significantly higher than 1 mA, activation of HCM is typically not needed.

The relevant EC Table parameter that defines the upper voltage regulation threshold (typically +2.9% of the nominal output voltage) is the Hysteretic Control Mode Upper Regulation Threshold.

Even if bit B1HCEN is set, HCM mode will only be activated when the input-to-output voltage differential decreases below a certain value. This is done to prevent fast inductor charging, which in turn may cause a poorer control of the effective upper regulation voltage.

The relevant **"Electrical Characteristics"** table parameter that defines the input voltage threshold (falling input voltage), below which HCM is enabled, is the Hysteretic Control Mode Enable Threshold and it is also expressed as a percentage of the nominal output voltage value (typically, +9%).

5.5 Protections

The MCP16502 offers the following:

- Thermal Shutdown
- Thermal Warning
- Overcurrent Protection

Thermal Shutdown protection will immediately terminate power delivery on all channels when the die temperature exceeds the upper Thermal Shutdown threshold. At the same time, nRSTO will be asserted low. If the corresponding masking bit is cleared, nINTO will also be asserted low.

After the die temperature has decreased below the lower Thermal Shutdown threshold (hysteresis = 20°C) and an additional 100 ms delay, the MCP16502 will automatically attempt a new start-up sequence without the need of an external Start condition (from nSTRT or PWRLHD).

Thermal Warning does not invoke any automatic action. If the die temperature exceeds the Thermal Warning upper threshold, and if the corresponding masking bit is cleared, it will only generate assertion (LOW) of the nINTO output. The host MPU can then interrogate the MCP16502 for diagnostic purposes.

5.5.1 OVERCURRENT PROTECTION (BUCK CHANNELS)

The overcurrent protection consists of a cycle-by-cycle, high-side current limit with digital filtering, followed by the Hiccup mode for protection against short-circuit conditions.

The cycle-by-cycle, high-side current limit includes frequency foldback. Because of Leading-Edge Blanking (LEB) in Peak Current mode control, frequency foldback (with a factor = 4) is used to allow more time for inductor discharge and prevent current runaway in a deep overload condition.

Frequency foldback operation is entered when:

1. A high-side current limit event has been detected; and
2. The feedback voltage is less than 500 mV (typical).

Cycle-by-cycle overcurrent protection with frequency foldback is always active and it is the first current limit protection mechanism.

The second current limit mechanism is Hiccup mode protection, which is also always enabled, including during the soft start ramp and DVS transitions.

Since the Hiccup mode protection is also active during soft start, there will be a limitation on the maximum simultaneous DC and capacitive loading to ensure that the Hiccup mode protection will not be engaged during the soft start ramp. This is further explained in **Section 5.6 "Maximum Simultaneous Capacitive and DC Loading in Soft Start and DVS"**.

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Hiccup mode is invoked based on digital counting of High-Side Overcurrent (HS OC) events, regardless of the frequency at which they take place (full switching frequency or foldback switching frequency).

Each time the overcurrent protection detects a high-side current limit event, the current on-time is terminated and a HS OC event counter is incremented. The length of the counter is four bits.

If the counter reaches its End-of-Count (EOC) while the instantaneous value of the POK signal is still low, the Buck converter is turned off (both high-side and low-side transistors are turned off) and Hiccup mode protection is triggered.

The intervention of Hiccup mode on any of the Buck channels can have two different behaviors, depending on the HCPEN bit value of the channel affected by overcurrent conditions. The HCPEN bit is user-accessible through I^2C.

If HCPEN = 0, the intervention of Hiccup mode will immediately terminate the power delivery on all channels, including LDOs. At the same time, nRSTO will be asserted low. If the corresponding masking bit is cleared, nINTO will also be asserted low.

After a 100 ms delay, the MCP16502 will automatically attempt a new start-up sequence without the need of an external Start condition (from nSTRT or PWRHLD).

If HCPEN = 1, the intervention of Hiccup mode only affects the responsible Buck channel. All other channels will continue to operate normally. If the affected channel is part of the power-up sequence, nRSTO will be asserted low, and if the corresponding masking bit is cleared, nINTO will also be asserted low.

The affected channel will be kept off for a certain Hiccup time (t_{HICCUP}), which corresponds to 3x soft start time on that channel, and after the Hiccup time, a new soft start is attempted.

If the short-circuit condition is removed and the affected channel resumes normal operation (POK returns high), nRSTO will be asserted high after the programmed Reset delay (t_4).

The HS OC event counter is reset only after 15 consecutive HS turn-on pulses without any overcurrent event. This counting is done by the Reset counter.

Note that all counting is switching event-based, so it is not relevant if the switching takes place at f_{sw} or at $f_{sw}/4$ (i.e., in frequency foldback).

The Hiccup mode flowchart is detailed in Figure 5-2. The overcurrent condition of each Buck is also reported through I^2C.

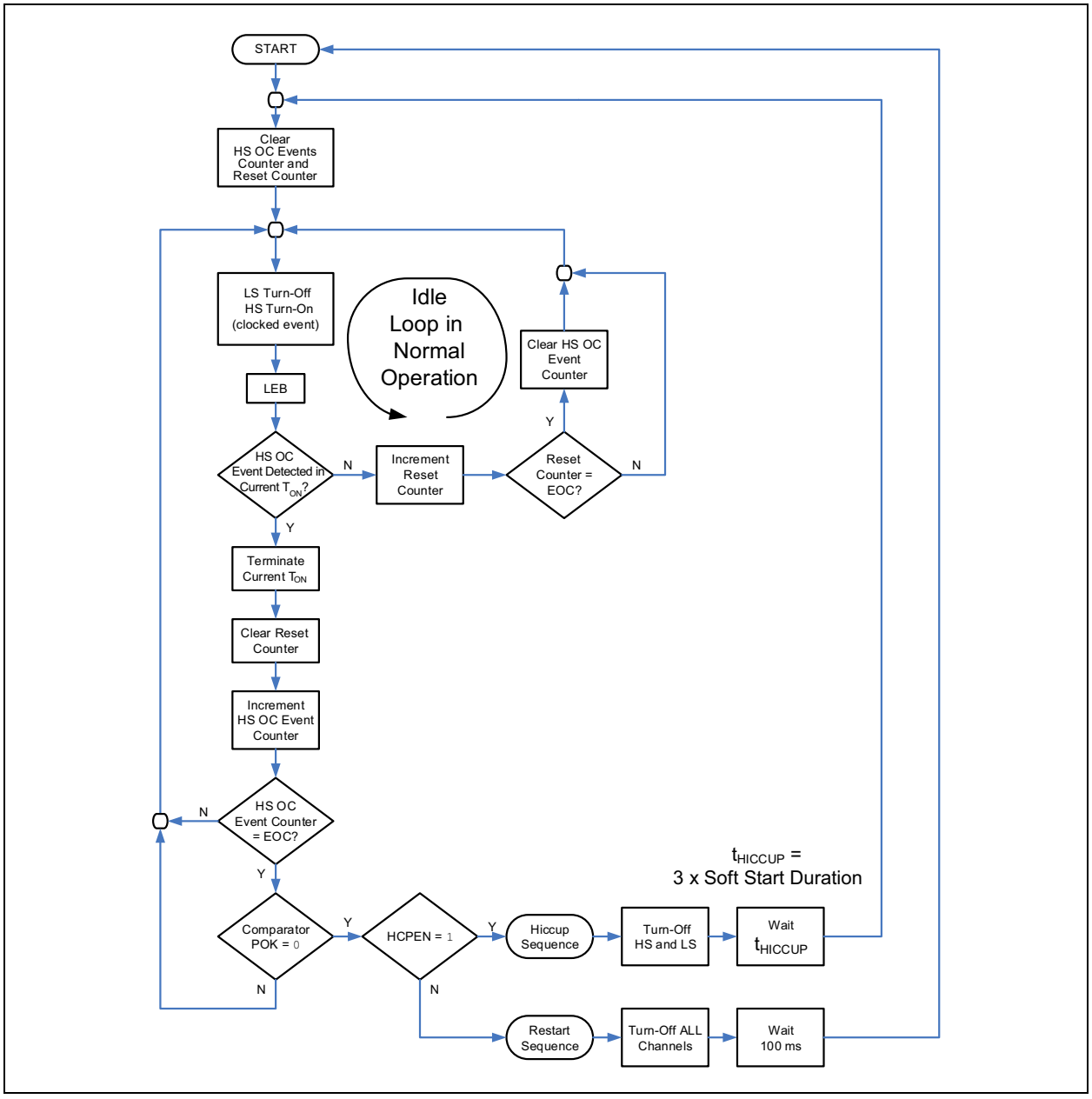


FIGURE 5-2: *Hiccup Mode Protection Flowchart.*

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5.5.2 PWM MODE NEGATIVE CURRENT LIMIT PROTECTION (BUCK CHANNELS)

The Buck channels of the MCP16502 also feature a negative inductor current limit protection when operating in Forced PWM mode. This prevents dangerous current levels in the power train. If the inductor current reaches the low-side Negative Peak Current Limit (I_{LIM_NEGx}) while the low-side MOSFET is conducting, the low-side MOSFET is turned off and the inductor current is pushed to the input voltage, either through the body diode of the high-side MOSFET (if off) or its channel (when turned on by the control loop). Since this feature is only intended to protect the device in some particular transient conditions (such as a large decrease of the ouput voltage setting associated with an extremely large capacitive load), it is only reported through I^2C, but it does not cause the assertion of the nRSTO (Reset) signal.

This protection should never be exercised continuously and/or without a large input bulk capacitor, because it may quickly destroy the device.

When this protection is engaged, energy is pumped back from the output into the input voltage. If the input supply has no sinking capability and/or the input bulk decoupling cap is not large enough, the input voltage will rise to the point where the device is permanently damaged.

5.5.3 LDO CURRENT LIMIT PROTECTION (BUCK CHANNELS)

LDOs are protected against short circuit by a linear constant-voltage/constant-current (i.e., brick wall) output characteristic. The output current under short-circuit conditions is not intermittent. Therefore, the internal power dissipation in the MCP16502 can reach high levels under LDO short-circuit conditions. The current limit condition of each LDO is also reported through I^2C. The intervention of the LDO current limit protection does not cause the assertion of the nRSTO (Reset) signal.

5.6 Maximum Simultaneous Capacitive and DC Loading in Soft Start and DVS

The Current-mode architecture of the Buck channels in the MCP16502 make them tolerant to additional capacitive loads from the stability point of view.

However, since the Hiccup mode overcurrent protection is also enabled during soft start and DVS ramping, the user needs to be aware that additional load capacitance, distributed on the application board, may cause the intervention of the Hiccup mode protections under dynamic conditions (rising output voltage).

This is especially important for Buck1 since the I/O rail (typically 3.3V) can be used for a wide variety of loads and its total distributed capacitive load could significantly exceed the minimum recommended nominal capacitance value (i.e., 22 µF).

Using the symbols listed in the **"AC/DC Characteristics"** table, Equation 5-1 establishes the maximum allowable capacitive load, C_{add_max}, to prevent the cycle-by-cycle current limit from being engaged.

Complying with this condition will ensure that Hiccup mode overcurrent protection will not be activated during the soft start ramp or DVS transitions in the positive direction.

Failing to comply with the condition formulated below does not necessarily mean that Hiccup mode protection will be engaged. The digital filtering provided in the Hiccup mode overcurrent algorithm, as described in **Section 5.5.1 "Overcurrent Protection (Buck Channels)"**, provides immunity to single, and even multiple cycle-by-cycle current limit events and allows operation in proximity of the high-side current limit for a significant amount of time during the soft start or DVS ramping.

EQUATION 5-1:

$$C_{add_max} = \left(\frac{I_{LIM_HS}}{r} - I_{OUT}\right) \cdot \frac{SSRXX}{V_{step} \cdot f_{sw}} - C_{OUT}$$

Where:

- I_{LIM_HS} = High-Side MOSFET Current Limit
- r = Ratio of the peak inductor current, I_{Lpk}, to average inductor current at the point where $I_{Lpk} = I_{LIM_HS}$. For simplicity, assume r = 1 since the peak-to-peak inductor current ripple will be small in comparison to the average inductor current value when the high-side current limit is engaged.
- I_{OUT} = Output Current of the Buck Converter
- V_{step} = Output Voltage Step in SS (or DVS)
- $SSRXX$ = Soft Start Rate (or DVS Rate), XX = 00, 01, 10, 11
- f_{sw} = Switching Frequency
- C_{OUT} = Output capacitance already present on the Buck converter output (typically, C_{OUT} = 22 µF)

As a consequence, the maximum value of additional capacitance, C_{add_max}, that can be observed by experiments is significantly higher than the limit calculated with the aforementioned formula.

5.7 nSTRT Capacitor for Automatic Turn-On on V_{IN} Ramping

As shown in Figure 4-1, it is possible to configure the MCP16502 for automatic start-up upon input voltage (V_{IN}) ramping/power cycling by connecting a capacitor on pin nSTRT. The purpose of the capacitor (C in Figure 4-1) is to delay the rise of the nSTRT pin when V_{IN} ramps up, such that after the SVIN pin voltage (connected to V_{IN}) has stabilized, the logic level of the nSTRT pin will still be low long enough to be interpreted as a valid start-up event (i.e., longer than t_1; see **Section 4.4.1 "Typical Power-up Sequence and Timing"**).

Under the assumption that the V_{IN} ramping is much shorter than the rise time of the nSTRT pin voltage, the recommended amount of capacitance needed for generation of a valid start-up event is given by the formula in Equation 5-2:

EQUATION 5-2:

$$C > \frac{t_1 + \Delta t}{R_{PU_nSTRT} \cdot \log e\left(\frac{V_{IN}}{V_{IN} - V_{IL_nSRT}}\right)} = \frac{t_1 + \Delta t}{R_{PU_nSTRT} \cdot \log e\left(\frac{1}{1 - 0.36}\right)} = 2.24 \cdot \frac{t_1 + \Delta t}{R_{PU_nSTRT}}$$

Where:

R_{PU_nSTRT} = nSTRT Pin Pull-up Resistance (40 kΩ typical value)

V_{IL_nSTRT} = nSTRT Logic Low Input Voltage (0.36 SVIN, maximum value)

V_{IN} = Input Voltage (SVIN is connected to the voltage V_{IN})

t_1 = Delay from nSTRT Falling to First Output V_{OUT1} Starting (≈ 0.5 ms); see **Section 4.4.1 "Typical Power-up Sequence and Timing"**

Δt = Additional Delay from SVIN Voltage established to the Detection of a Logic Low Level on nSTRT (due to internal logic wake-up time): ≈ 100 µs

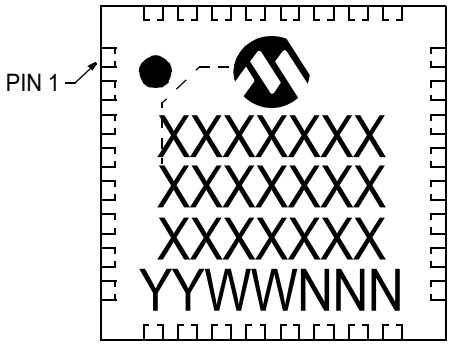
After the selection of capacitor C, the resulting C R_{PU_nSTRT} time constant must be compared to the actual V_{IN} ramping time to verify that indeed the nSTRT rise time is much slower.

The time constant C R_{PU_nSTRT} should be at least one order of magnitude larger than the slowest V_{IN} ramping time expected in the application. If this is not true, the capacitor value C must be increased further. Using a 1 µF capacitor for C, the C R_{PU_nSTRT} time constant will be 40 ms, which is adequate for V_{IN} ramping times in the ms range.

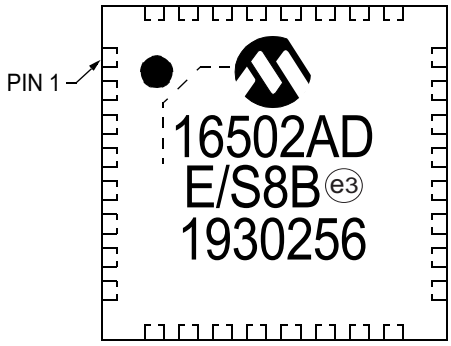
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6.0 PACKAGE MARKING INFORMATION

32-Lead VQFN (5 x 5 mm) **(MCP16502)**



Example

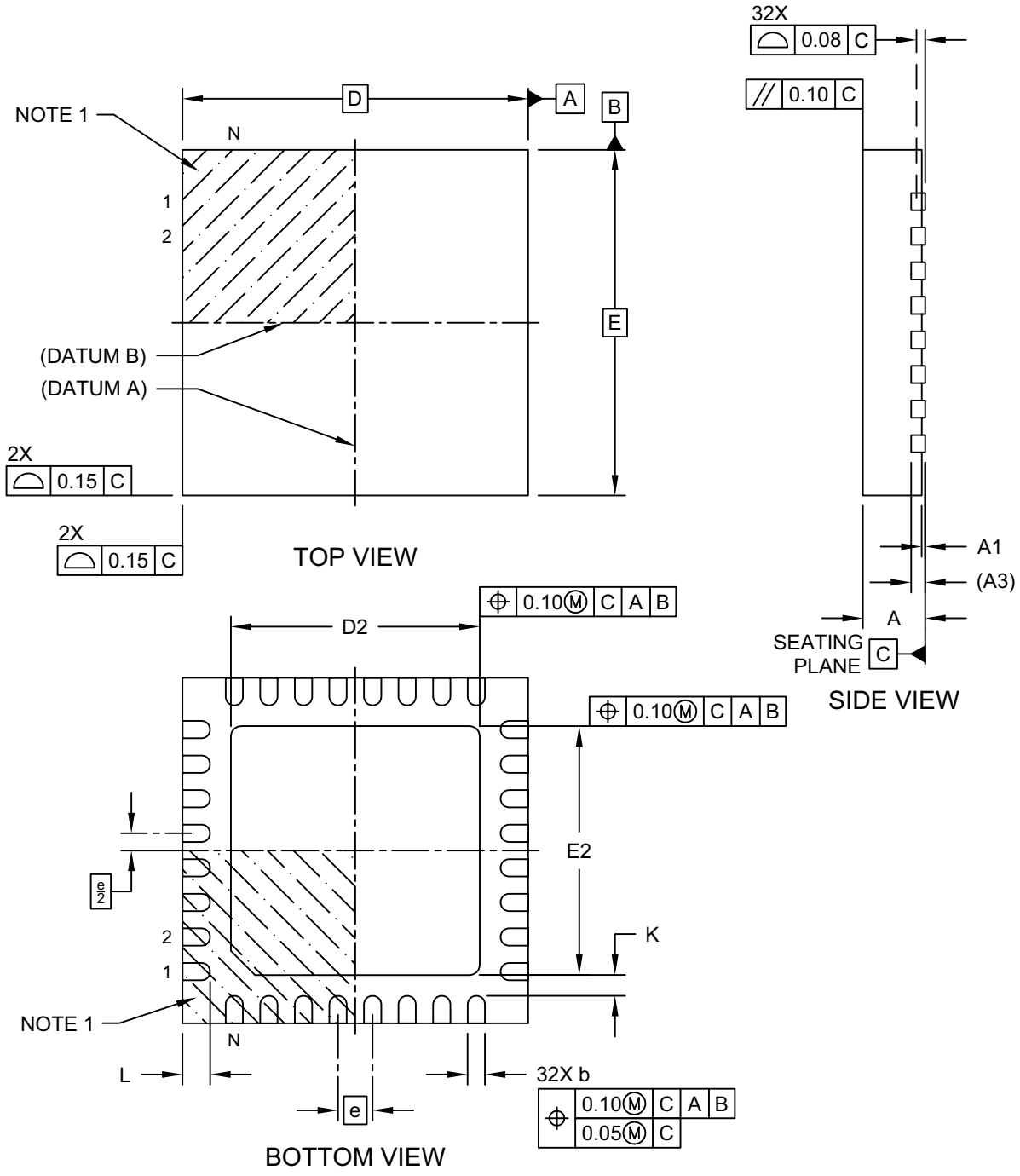


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

32-Lead Very Thin Plastic Quad Flat, No Lead Package (S8B) - 5x5 mm Body [VQFN] With 3.60 mm Exposed Pad; Atmel Legacy Global Package Code ZKV

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

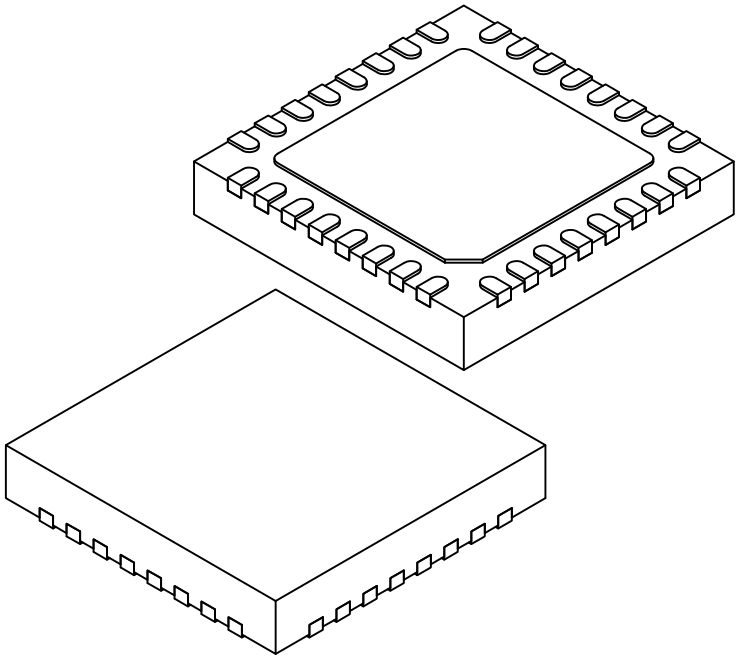


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32-Lead Very Thin Plastic Quad Flat, No Lead Package (S8B) - 5x5 mm Body [VQFN] With 3.60 mm Exposed Pad; Atmel Legacy Global Package Code ZKV

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.50	3.60	3.70
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.50	3.60	3.70
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

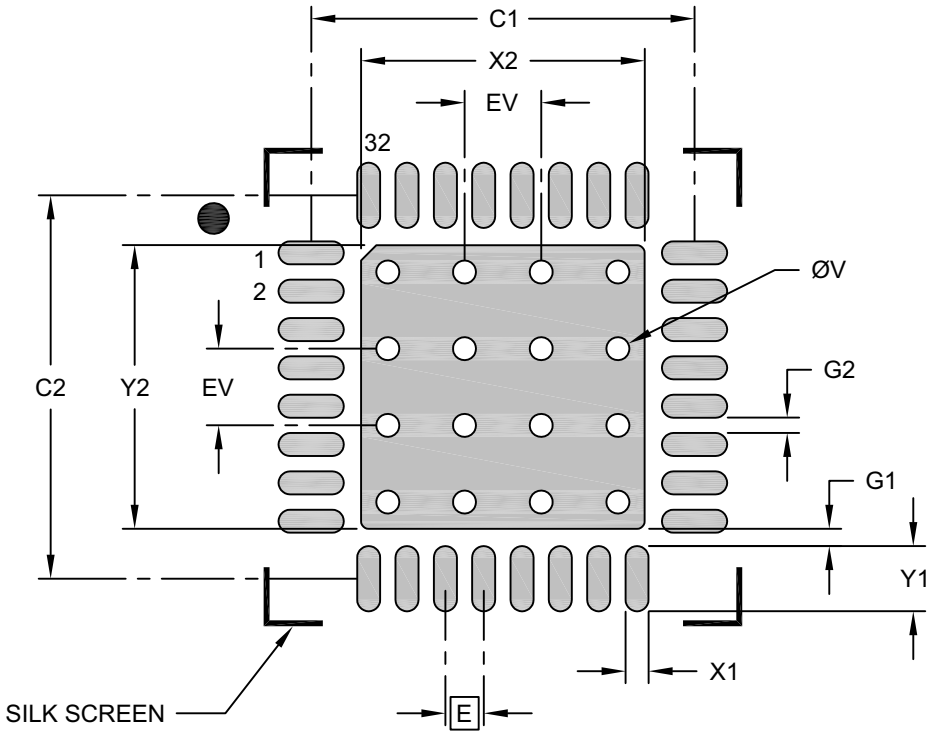
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21402 Rev A Sheet 1 of 2

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32-Lead Very Thin Plastic Quad Flat, No Lead Package (S8B) - 5x5 mm Body [VQFN] With 3.60 mm Exposed Pad; Atmel Legacy Global Package Code ZKV

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			3.70
Optional Center Pad Length	Y2			3.70
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X32)	X1			0.30
Contact Pad Length (X32)	Y1			0.85
Contact Pad to Center Pad (X32)	G1	0.23		
Contact Pad to Contact Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23402 Rev A

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APPENDIX A: REVISION HISTORY

Revision B (November 2019)

- Removed Automotive Qualification references.

Revision A (November 2019)

- Initial release of this document.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X(1)	XX	–	X	/XX
Device	Tape and Reel Option	Device Option		Junction Temperature Range	Package

Device:	MCP16502 High-Performance PMIC		
Tape and Reel Option:	Blank	=	Standard Packaging (tube or tray)
	T	=	Tape and Reel(1)
Device Option:	AA	=	AA Option
	AB	=	AB Option
	AC	=	AC Option
	AD	=	AD Option
	AE	=	AE Option
Junction Temperature Range:	E	=	-40°C to +125°C (Extended)
Package	S8B	=	32-Lead Very Thin Plastic Quad Flat, No Lead (VQFN) Package – 5 x 5 mm Body

Examples:

a) MCP16502AC-E/S8B: High-Performance PMIC, AC Option, -40°C to +125°C, 32-Lead 5 x 5 VQFN Package.

b) MCP16502TAC-E/S8B: High-Performance PMIC, Tape and Reel, AC Option, -40°C to +125°C, 32-Lead 5 x 5 VQFN Package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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