MCP3911

3.3V Two-Channel Analog Front End

Features

- Two Synchronous Sampling 16/24-bit Resolution Delta-Sigma A/D Converters
- 94.5 dB SINAD, -106.5 dBc Total Harmonic Distortion (THD) (up to 35th harmonic), 111 dB SFDR for Each Channel
- 2.7V-3.6V AV_{DD}, DV_{DD}
- Programmable Data Rate Up to 125 ksps:
  - 4 MHz Maximum Sampling Frequency
- Oversampling Ratio Up to 4096
- Ultra Low-Power Shutdown Mode with <2 µA
- -122 dB Crosstalk Between the Two Channels
- Low-Drift 1.2V Internal Voltage Reference: 7 ppm/°C
- Differential Voltage Reference Input Pins
- High-Gain Programmable Gain Amplifier (PGA) on Each Channel (up to 32V/V)
- Phase Delay Compensation with 1 µs Time Resolution
- Separate Modulator Output Pins for Each Channel
- Separate Data Ready Pin for Easy Synchronization
- Individual 24-Bit Digital Offset and Gain Error Correction for Each Channel
- High-Speed 20 MHz SPI Interface with Mode 0,0 and 1,1 Compatibility
- Continuous Read/Write Modes for Minimum Communication
- Low-Power Consumption (8.9 mW at 3.3V, 5.6 mW at 3.3V in Low-Power mode, typical)
- Available in Small 20-Lead QFN and SSOP Packages, Pin-to-Pin Compatible with MCP3901
- Extended Temperature Range: -40°C to +125°C

Applications

- Energy Metering and Power Measurement
- Automotive
- Portable Instrumentation
- Medical and Power Monitoring
- Audio/Voice Recognition

Description

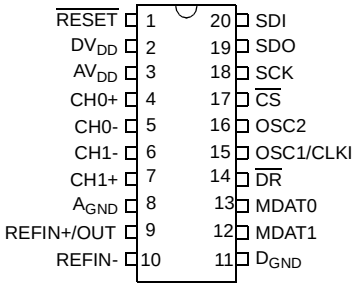
The MCP3911 is a 2.7V to 3.6V dual channel Analog Front End (AFE) containing two synchronous sampling Delta-Sigma Analog-to-Digital Converters (ADC), two PGAs, phase delay compensation block, low-drift internal voltage reference, modulator output block, Digital Offset and Gain Error Calibration registers and high-speed 20 MHz SPI compatible serial interface.

The MCP3911 ADCs are fully configurable with features, such as: 16/24-bit resolution, Oversampling Ratio (OSR) from 32 to 4096, gain from 1x to 32x, independent shutdown and Reset, dithering and auto-zeroing. The communication is largely simplified with the one-byte long commands, including various continuous Read/Write modes that can be accessed by the Direct Memory Access (DMA) of an MCU with a separate Data Ready pin that can be directly connected to an Interrupt Request (IRQ) input of an MCU.

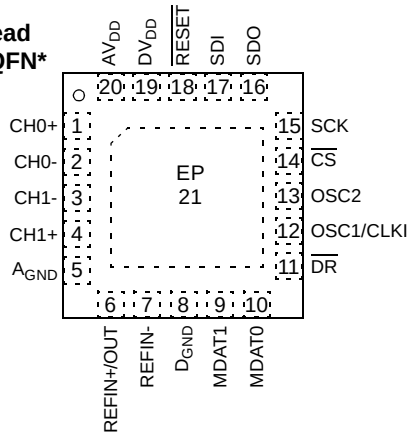
The MCP3911 is capable of interfacing a large variety of voltage and current sensors, including shunts, current transformers, Rogowski coils and Hall effect sensors.

Package Type

20-Lead SSOP



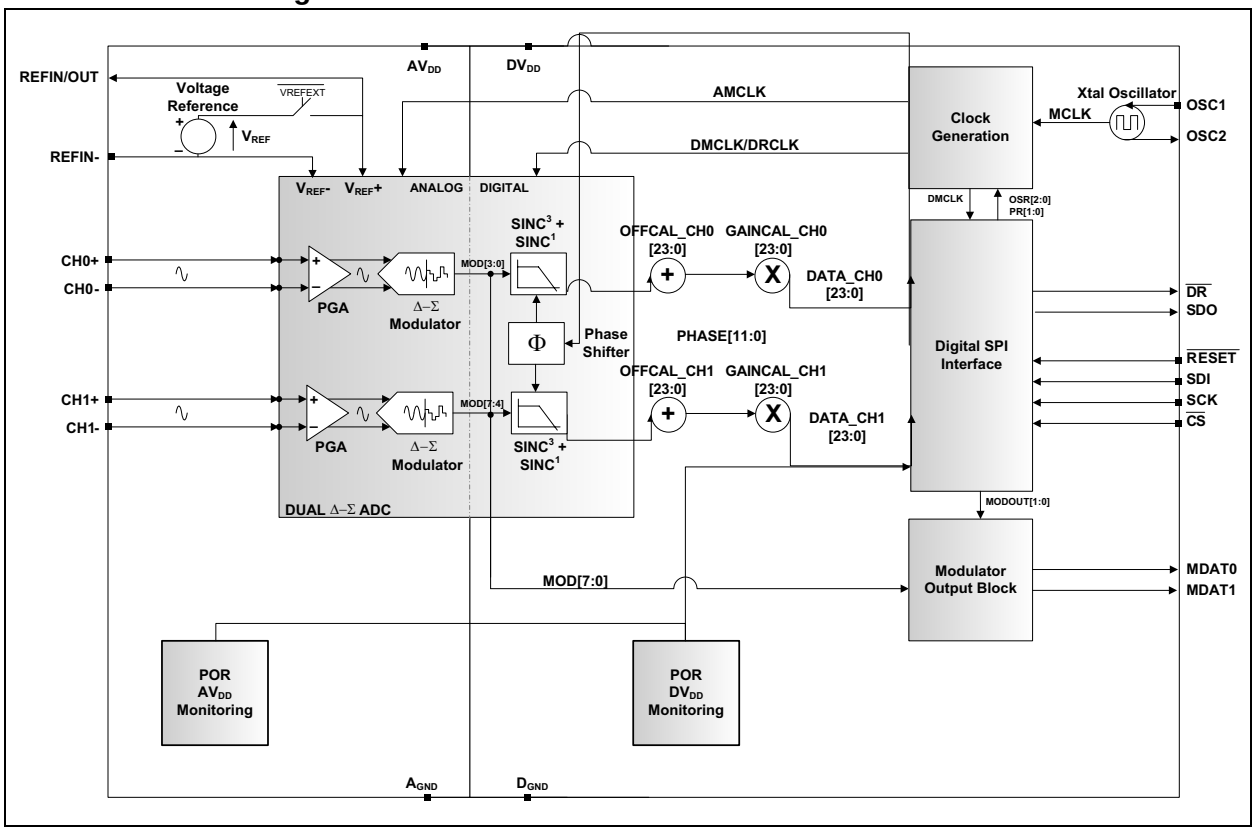
20-Lead 4x4 QFN*



*Includes Exposed Thermal Pad (EP); see Table 3-1.

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Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{DD} ..... -0.3V to 4.0V
Digital inputs and outputs w.r.t. A_{GND} ..... -0.3V to 4.0V
Analog input w.r.t. A_{GND} ..... -2V to +2V
V_{REF} input w.r.t. A_{GND} ..... -0.6V to V_{DD} + 0.6V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD on the analog inputs (HBM,MM) ..... 4.0 kV, 300V
ESD on all other pins (HBM,MM) ..... 4.0 kV, 300V

† **Notice**: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operational listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 Electrical Specifications

TABLE 1-1: ANALOG SPECIFICATIONS TARGET

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = DV_{DD} = 2.7V to 3.6V; MCLK = 4 MHz; PRE[1:0] = 00; OSR = 256; GAIN = 1; VREFEXT = 0; CLKEXT = 1; AZ_FREQ = 0; DITHER[1:0] = 11; BOOST[1:0] = 10; V_{CM} = 0V; T_A = -40°C to +125°C; V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} at 50/60 Hz on both channels.						
Characteristic	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
ADC Performance						
Resolution (No Missing Codes)		24	—	—	bits	OSR = 256 or greater
Sampling Frequency	f_S(DMCLK)	—	1	4	MHz	For maximum condition, BOOST[1:0] = 11
Output Data Rate	f_D(DRCLK)	—	4	125	ksps	For maximum condition, BOOST[1:0] = 11, OSR = 32
Analog Input Absolute Voltage on CH0+, CH0-, CH1+, CH1- Pins	CH0+/-	-1	—	+1	V	All analog input channels, measured to A_{GND}
Analog Input Leakage Current	I_{IN}	—	±1	—	nA	RESET[1:0] = 11, MCLK running continuously
Differential Input Voltage Range	(CHn+ – CHn-)	-600/GAIN	—	+600/GAIN	mV	V_{REF} = 1.2V, proportional to V_{REF}
Offset Error	V_{OS}	-2	0.2	+2	mV	**Note 4**
Offset Error Drift		—	0.5	—	µV/°C	
Gain Error	GE	-6	—	+6	%	**Note 4**

Note 1: This specification implies that the ADC output is valid over this entire differential range and that there is no distortion or instability across this input range. Dynamic performance specified at -0.5 dB below the maximum signal range, V_{IN} = 1.2 V_{PP} = 424 mV_{RMS}, V_{REF} = 1.2V at 50/60 Hz. See **Section 4.0, Terminologies and Formulas** for definition. This parameter is established by characterization and is not 100% tested. See performance graphs for other than default settings provided here.

2: For these operating currents, the following Configuration bit settings apply: SHUTDOWN[1:0] = 00, RESET[1:0] = 00, VREFEXT = 0, CLKEXT = 0.

3: For these operating currents, the following Configuration bit settings apply: SHUTDOWN[1:0] = 11, VREFEXT = 1, CLKEXT = 1.

4: Applies to all gains. Offset and gain errors depend on PGA gain setting; see **Section 2.0, Typical Performance Curves** for typical performance.

5: Outside of this range, the ADC accuracy is not specified. An extended input range of ±2V can be applied continuously to the part with no damage.

6: For proper operation and optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2 as a function of the BOOST and PGA settings chosen. MCLK can take larger values as long as the prescaler settings (PRE[1:0]) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2.

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TABLE 1-1: ANALOG SPECIFICATIONS TARGET (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = DV_{DD} = 2.7V to 3.6V; MCLK = 4 MHz; PRE[1:0] = 00; OSR = 256; GAIN = 1; VREFEXT = 0; CLKEXT = 1; AZ_FREQ = 0; DITHER[1:0] = 11; BOOST[1:0] = 10; V_{CM} = 0V; T_A = -40°C to +125°C; V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} at 50/60 Hz on both channels.						
Characteristic	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Gain Error Drift		—	1	—	ppm/°C	
Integral Nonlinearity	INL	—	5	—	ppm	
Differential Input Impedance	Z_{IN}	232	—	—	kΩ	G = 1, proportional to 1/AMCLK
		142	—	—	kΩ	G = 2, proportional to 1/AMCLK
		72	—	—	kΩ	G = 4, proportional to 1/AMCLK
		38	—	—	kΩ	G = 8, proportional to 1/AMCLK
		36	—	—	kΩ	G = 16, proportional to 1/AMCLK
		33	—	—	kΩ	G = 32, proportional to 1/AMCLK
Signal-to-Noise and Distortion Ratio **(Note 1)**	SINAD	92	94.5	—	dB	
Total Harmonic Distortion **(Note 1)**	THD	—	-106.5	-103	dBc	Includes the first 35 harmonics
Signal-to-Noise Ratio **(Note 1)**	SNR	92	95	—	dB	
Spurious-Free Dynamic Range **(Note 1)**	SFDR	—	111	—	dBFS	
Crosstalk (50, 60 Hz)	CTALK	—	-122	—	dB	
AC Power Supply Rejection	AC PSRR	—	-73	—	dB	AV_{DD} = DV_{DD} = 3.3V + 0.6V_{PP}, 50/60 Hz, 100/120 Hz
DC Power Supply Rejection	DC PSRR	—	-73	—	dB	AV_{DD} = DV_{DD} = 2.7V to 3.6V
DC Common-Mode Rejection	DC CMRR	—	-105	—	dB	V_{CM} from -1V to +1V

Note 1: This specification implies that the ADC output is valid over this entire differential range and that there is no distortion or instability across this input range. Dynamic performance specified at -0.5 dB below the maximum signal range, V_{IN} = 1.2 V_{PP} = 424 mV_{RMS}, V_{REF} = 1.2V at 50/60 Hz. See **Section 4.0, Terminologies and Formulas** for definition. This parameter is established by characterization and is not 100% tested. See performance graphs for other than default settings provided here.

2: For these operating currents, the following Configuration bit settings apply: SHUTDOWN[1:0] = 00, RESET[1:0] = 00, VREFEXT = 0, CLKEXT = 0.

3: For these operating currents, the following Configuration bit settings apply: SHUTDOWN[1:0] = 11, VREFEXT = 1, CLKEXT = 1.

4: Applies to all gains. Offset and gain errors depend on PGA gain setting; see **Section 2.0, Typical Performance Curves** for typical performance.

5: Outside of this range, the ADC accuracy is not specified. An extended input range of ±2V can be applied continuously to the part with no damage.

6: For proper operation and optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2 as a function of the BOOST and PGA settings chosen. MCLK can take larger values as long as the prescaler settings (PRE[1:0]) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2.

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TABLE 1-1: ANALOG SPECIFICATIONS TARGET (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = DV_{DD} = 2.7V to 3.6V; MCLK = 4 MHz; PRE[1:0] = 00; OSR = 256; GAIN = 1; VREFEXT = 0; CLKEXT = 1; AZ_FREQ = 0; DITHER[1:0] = 11; BOOST[1:0] = 10; V_{CM} = 0V; T_A = -40°C to +125°C; V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} at 50/60 Hz on both channels.						
Characteristic	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Internal Voltage Reference						
Tolerance	V_{REF}	1.176	1.2	1.224	V	VREFEXT = 0, T_A = +25°C only
Temperature Coefficient	TCV_{REF}	—	7	—	ppm/°C	T_A = -40°C to +125°C, VREFEXT = 0
Output Impedance	$ZOUTV_{REF}$	—	2	—	kΩ	VREFEXT = 0
Internal Voltage Reference Operating Current	$AI_{DD}V_{REF}$	—	25	—	µA	VREFEXT = 0, SHUTDOWN[1:0] = 11
Voltage Reference Input						
Input Capacitance		—	—	10	pF	
Differential Input Voltage Range (V_{REF}+ – V_{REF}-)	V_{REF}	1.1	—	1.3	V	VREFEXT = 1
Absolute Voltage on REFIN+ Pin	V_{REF}+	V_{REF}- + 1.1	—	V_{REF}- + 1.3	V	VREFEXT = 1
Absolute Voltage on REFIN- Pin	V_{REF}-	-0.1	—	+0.1	V	REFIN- should be connected to A_{GND} when VREFEXT = 0
Master Clock Input						
Master Clock Input Frequency Range	f_{MCLK}	—	—	20	MHz	CLKEXT = 1 **(Note 6)**
Crystal Oscillator Operating Frequency Range	f_{XTAL}	1	—	20	MHz	CLKEXT = 0 **(Note 6)**
Analog Master Clock	AMCLK	—	—	16	MHz	**Note 6**
Power Supply						
Operating Voltage, Analog	AV_{DD}	2.7	—	3.6	V	
Operating Voltage, Digital	DV_{DD}	2.7	—	3.6	V	
Operating Current, Analog **(Note 2)**	$I_{DD,A}$	—	1.5	2.3	mA	BOOST[1:0] = 00
		—	1.8	2.8	mA	BOOST[1:0] = 01
		—	2.5	3.5	mA	BOOST[1:0] = 10
		—	4.4	6.25	mA	BOOST[1:0] = 11

Note 1: This specification implies that the ADC output is valid over this entire differential range and that there is no distortion or instability across this input range. Dynamic performance specified at -0.5 dB below the maximum signal range, V_{IN} = 1.2 V_{PP} = 424 mV_{RMS}, V_{REF} = 1.2V at 50/60 Hz. See **Section 4.0, Terminologies and Formulas** for definition. This parameter is established by characterization and is not 100% tested. See performance graphs for other than default settings provided here.

2: For these operating currents, the following Configuration bit settings apply: SHUTDOWN[1:0] = 00, RESET[1:0] = 00, VREFEXT = 0, CLKEXT = 0.

3: For these operating currents, the following Configuration bit settings apply: SHUTDOWN[1:0] = 11, VREFEXT = 1, CLKEXT = 1.

4: Applies to all gains. Offset and gain errors depend on PGA gain setting; see **Section 2.0, Typical Performance Curves** for typical performance.

5: Outside of this range, the ADC accuracy is not specified. An extended input range of ±2V can be applied continuously to the part with no damage.

6: For proper operation and optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2 as a function of the BOOST and PGA settings chosen. MCLK can take larger values as long as the prescaler settings (PRE[1:0]) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2.

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TABLE 1-1: ANALOG SPECIFICATIONS TARGET (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = DV_{DD} = 2.7V to 3.6V; MCLK = 4 MHz; PRE[1:0] = 00; OSR = 256; GAIN = 1; VREFEXT = 0; CLKEXT = 1; AZ_FREQ = 0; DITHER[1:0] = 11; BOOST[1:0] = 10; V_{CM} = 0V; T_A = -40°C to +125°C; V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} at 50/60 Hz on both channels.						
Characteristic	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Operating Current, Digital	$I_{DD,D}$	—	0.2	0.3	mA	MCLK = 4 MHz, proportional to MCLK
		—	0.7	—	mA	MCLK = 16 MHz, proportional to MCLK
Shutdown Current, Analog	$I_{DDS,A}$	—	—	1	µA	AV_{DD} pin only **(Note 3)**
Shutdown Current, Digital	$I_{DDS,D}$	—	—	1	µA	DV_{DD} pin only (**Note 3**)

Note 1: This specification implies that the ADC output is valid over this entire differential range and that there is no distortion or instability across this input range. Dynamic performance specified at -0.5 dB below the maximum signal range, V_{IN} = 1.2 V_{PP} = 424 mV_{RMS}, V_{REF} = 1.2V at 50/60 Hz. See **Section 4.0, Terminologies and Formulas** for definition. This parameter is established by characterization and is not 100% tested. See performance graphs for other than default settings provided here.

2: For these operating currents, the following Configuration bit settings apply: SHUTDOWN[1:0] = 00, RESET[1:0] = 00, VREFEXT = 0, CLKEXT = 0.

3: For these operating currents, the following Configuration bit settings apply: SHUTDOWN[1:0] = 11, VREFEXT = 1, CLKEXT = 1.

4: Applies to all gains. Offset and gain errors depend on PGA gain setting; see **Section 2.0, Typical Performance Curves** for typical performance.

5: Outside of this range, the ADC accuracy is not specified. An extended input range of ±2V can be applied continuously to the part with no damage.

6: For proper operation and optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2 as a function of the BOOST and PGA settings chosen. MCLK can take larger values as long as the prescaler settings (PRE[1:0]) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2.

1.2 Serial Interface Characteristics

TABLE 1-2: SERIAL DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at DV_{DD} = 2.7 to 3.6V; T_A = -40°C to +125°C; C_{LOAD} = 30 pF; applies to all digital I/Os.						
Characteristics	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
High-Level Input Voltage	V_{IH}	0.7 DV_{DD}	—	—	V	Schmitt Triggered
Low-Level Input Voltage	V_{IL}	—	—	0.3 DV_{DD}	V	Schmitt Triggered
Input Leakage Current	I_{LI}	—	—	±1	µA	$\overline{CS}$ = DV_{DD}, V_{IN} = D_{GND} to DV_{DD}
Output leakage Current	I_{LO}	—	—	±1	µA	$\overline{CS}$ = DV_{DD}, V_{OUT} = D_{GND} or DV_{DD}
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	200	—	mV	DV_{DD} = 3.3V only **(Note 2)**
Low-Level Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = +2.1 mA, DV_{DD} = 3.3V
High-Level Output Voltage	V_{OH}	DV_{DD} – 0.5	—	—	V	I_{OH} = -2.1 mA, DV_{DD} = 3.3V
Internal Capacitance (all inputs and outputs)	C_{INT}	—	—	7	pF	T_A = +25°C, SCK = 1.0 MHz, DV_{DD} = 3.3V **(Note 1)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is established by characterization and not production tested.

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TABLE 1-3: SERIAL AC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at DV_{DD} = 2.7 to 3.6V, T_A = -40°C to +125°C, GAIN = 1, C_{LOAD} = 30 pF.						
Characteristics	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Serial Clock Frequency	f_{SCK}	—	—	20	MHz	
$\overline{CS}$ Setup Time	t_{CSS}	25	—	—	ns	
$\overline{CS}$ Hold Time	t_{CSH}	50	—	—	ns	
$\overline{CS}$ Disable Time	t_{CSD}	50	—	—	ns	
Data Setup Time	t_{SU}	5	—	—	ns	
Data Hold Time	t_{HD}	10	—	—	ns	
Serial Clock High Time	t_{HI}	20	—	—	ns	
Serial Clock Low Time	t_{LO}	20	—	—	ns	
Serial Clock Delay Time	t_{CLD}	50	—	—	ns	
Serial Clock Enable Time	t_{CLE}	50	—	—	ns	
Output Valid from SCK Low	t_{DO}	—	—	25	ns	
Modulator Output Valid from AMCLK High	t_{DOMDAT}	—	—	1/(2 x AMCLK)	s	
Output Hold Time	t_{HO}	0	—	—	ns	**Note 1**
Output Disable Time	t_{DIS}	—	—	25	ns	**Note 1**
Reset Pulse Width ($\overline{RESET}$)	t_{MCLR}	100	—	—	ns	
Data Transfer Time to $\overline{DR}$ (Data Ready)	t_{DODR}	—	—	25	ns	**Note 2**
Modulator Mode Entry to Modulator Data Present	t_{MODSU}	—	—	100	ns	
Data Ready Pulse Low Time	t_{DRP}	—	1/DMCLK	—	µs	

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is established by characterization and not production tested.

TABLE 1-4: TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = 2.7 to 3.6V; DV_{DD} = 2.7 to 3.6V.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 20-Lead QFN	θ_{JA}	—	43	—	°C/W	
Thermal Resistance, 20-Lead SSOP	θ_{JA}	—	87.3	—	°C/W	

Note 1: The internal junction temperature (T_J) must not exceed the absolute maximum specification of +150°C.

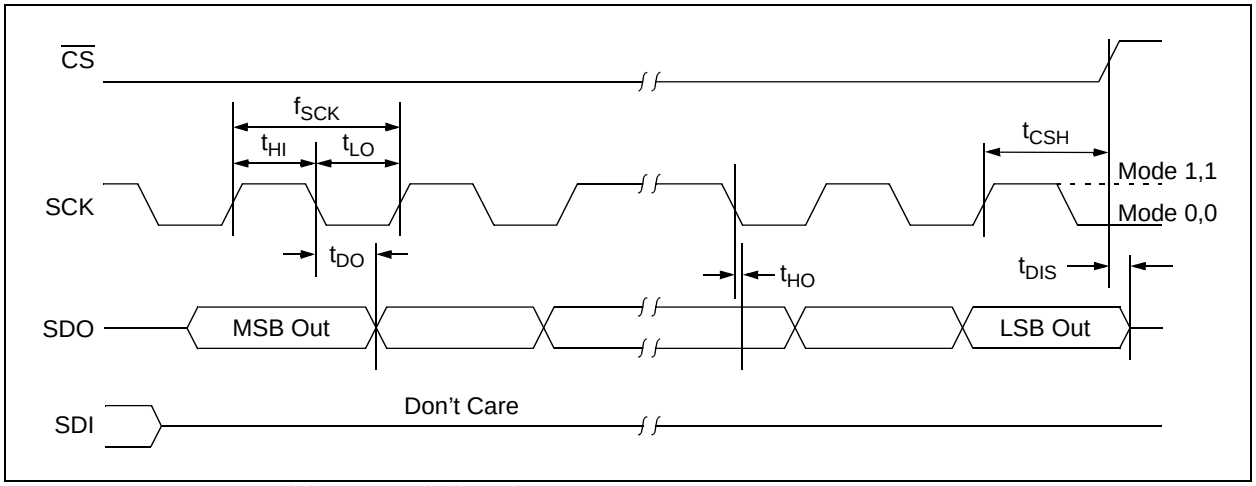


FIGURE 1-1: *Serial Output Timing Diagram.*

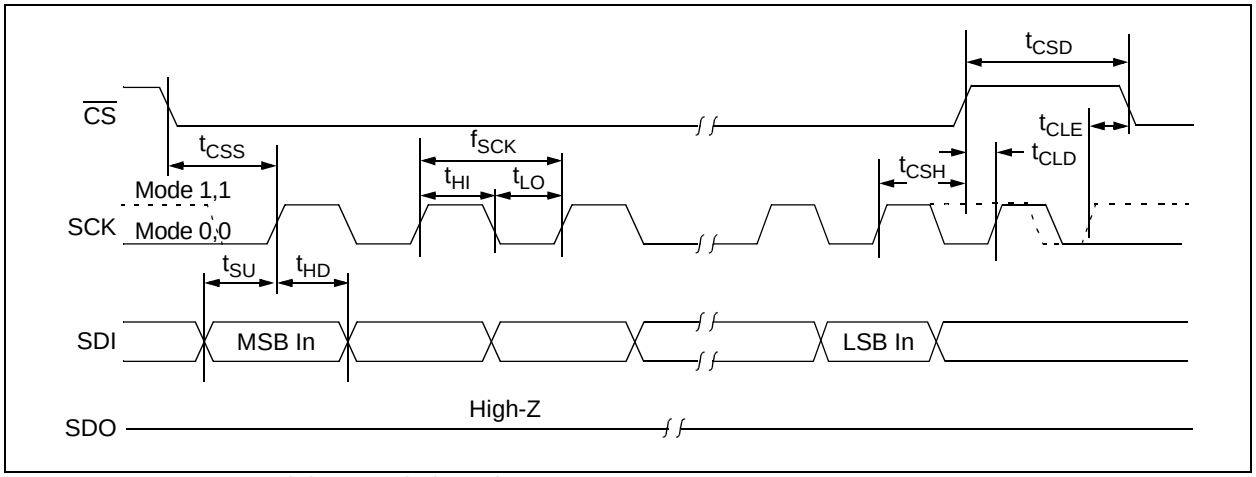


FIGURE 1-2: *Serial Input Timing Diagram.*

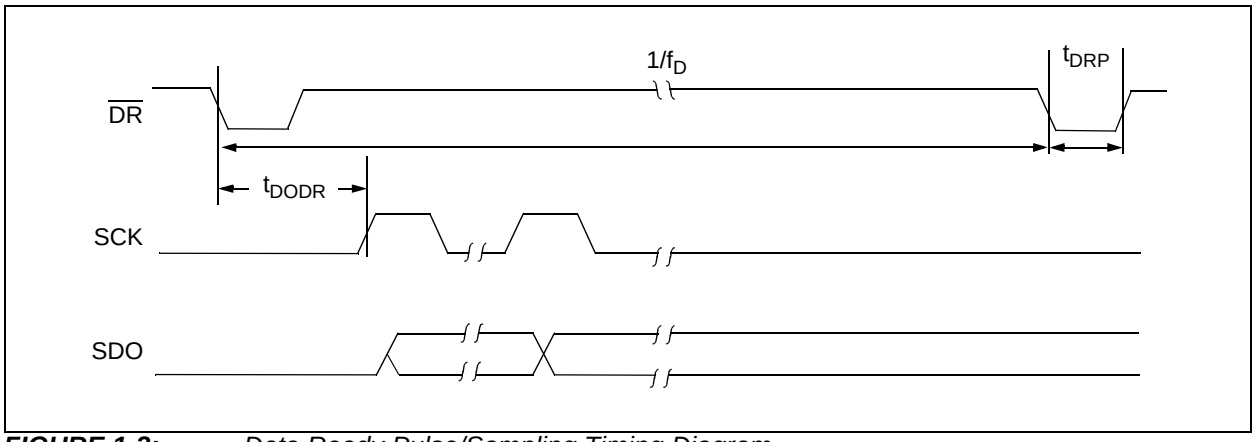


FIGURE 1-3: *Data Ready Pulse/Sampling Timing Diagram.*

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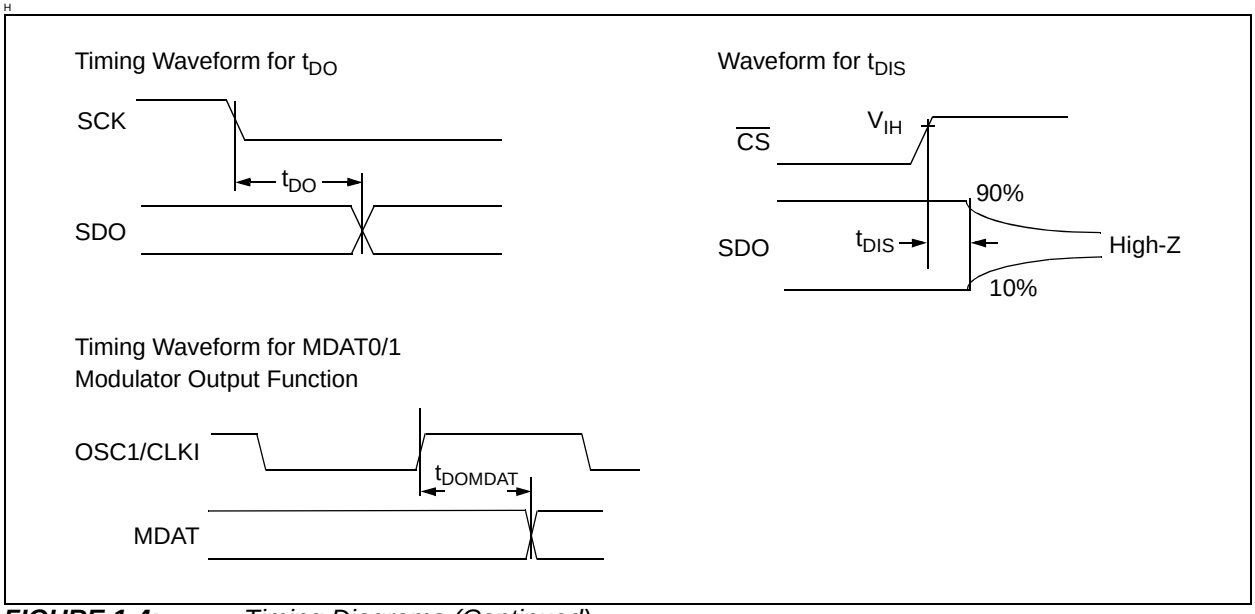


FIGURE 1-4: *Timing Diagrams (Continued).*

NOTES:

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, AV_{DD} = 3.3V; DV_{DD} = 3.3V; T_A = +25°C; MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS at 60 Hz; VREFEXT = 0; CLKEXT = 1; AZ_FREQ = 0; BOOST = 1x.

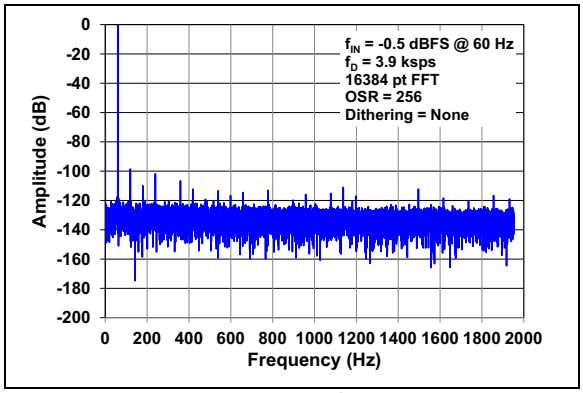


FIGURE 2-1: *Spectral Response.*

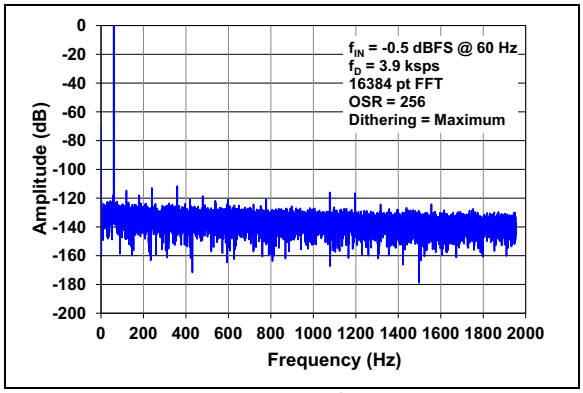


FIGURE 2-4: *Spectral Response.*

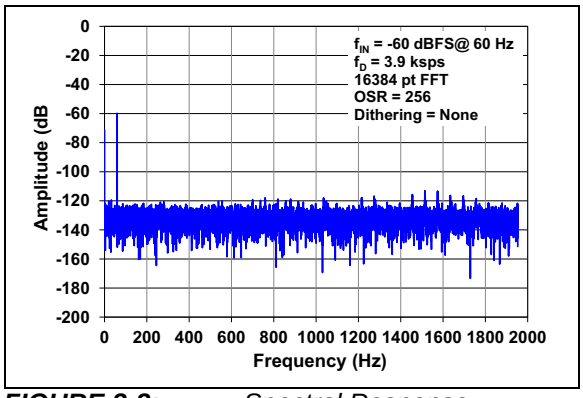


FIGURE 2-2: *Spectral Response.*

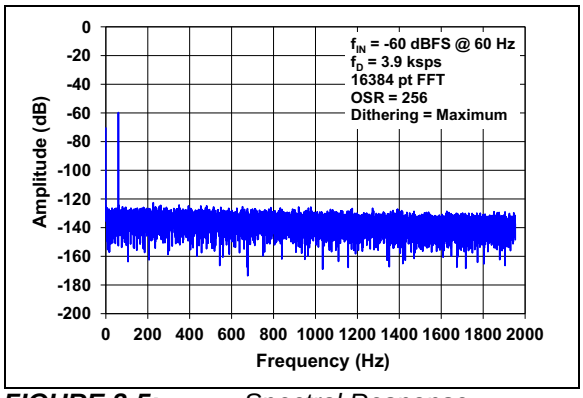


FIGURE 2-5: *Spectral Response.*

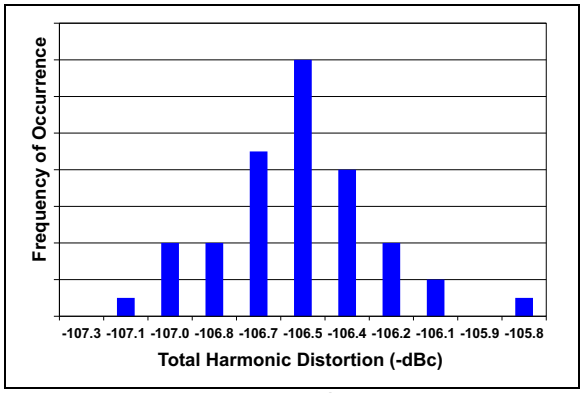


FIGURE 2-3: *THD Histogram.*

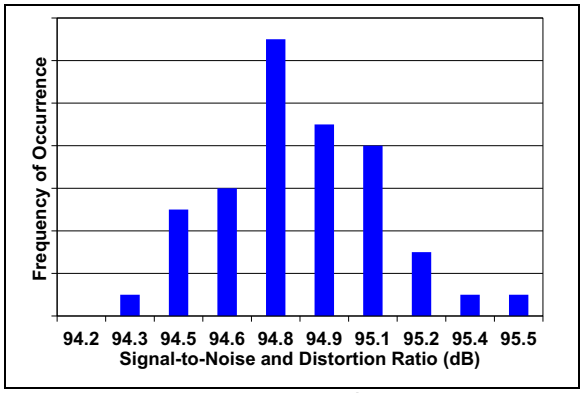


FIGURE 2-6: *SINAD Histogram.*

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Note: Unless otherwise indicated, AV_{DD} = 3.3V; DV_{DD} = 3.3V; T_A = +25°C; MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS at 60 Hz; VREFEXT = 0; CLKEXT = 1; AZ_FREQ = 0; BOOST = 1x.

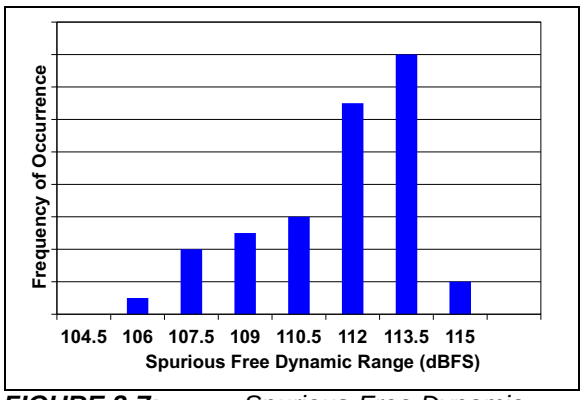


FIGURE 2-7: *Spurious-Free Dynamic Range Histogram.*

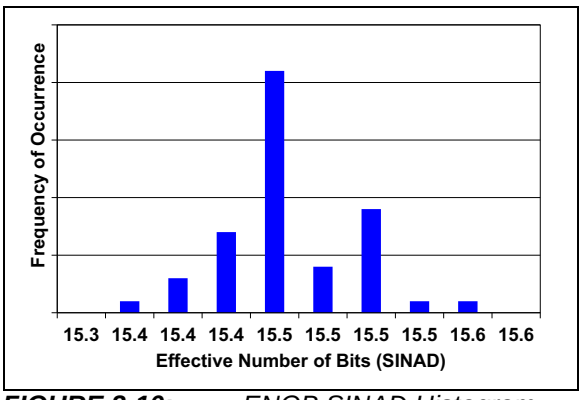


FIGURE 2-10: *ENOB SINAD Histogram.*

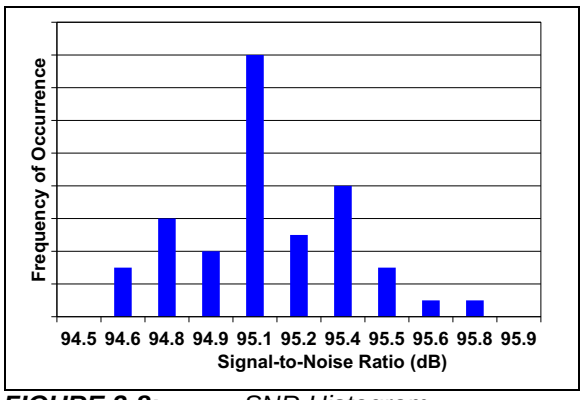


FIGURE 2-8: *SNR Histogram.*

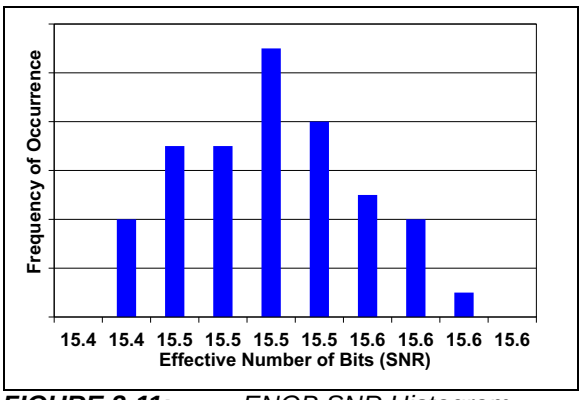


FIGURE 2-11: *ENOB SNR Histogram.*

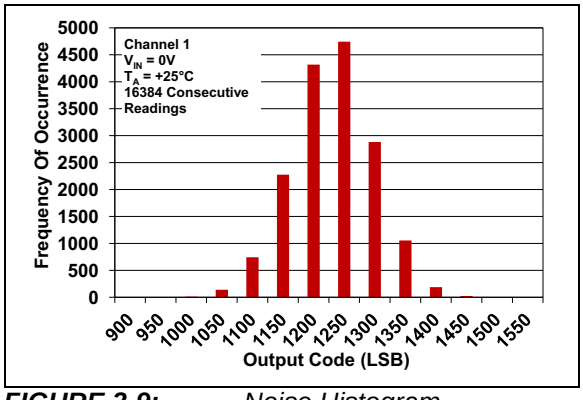


FIGURE 2-9: *Noise Histogram.*

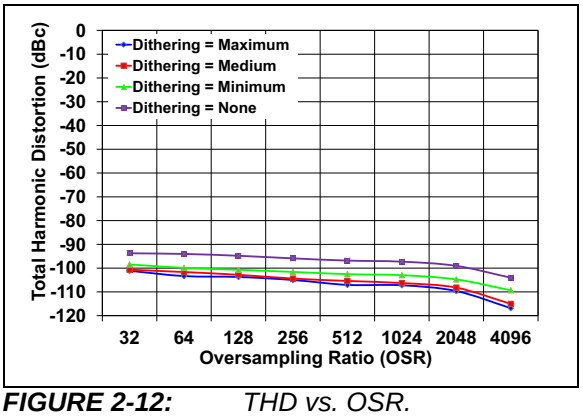


FIGURE 2-12: *THD vs. OSR.*

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Note: Unless otherwise indicated, AV_{DD} = 3.3V; DV_{DD} = 3.3V; T_A = +25°C; MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS at 60 Hz; VREFEXT = 0; CLKEXT = 1; AZ_FREQ = 0; BOOST = 1x.

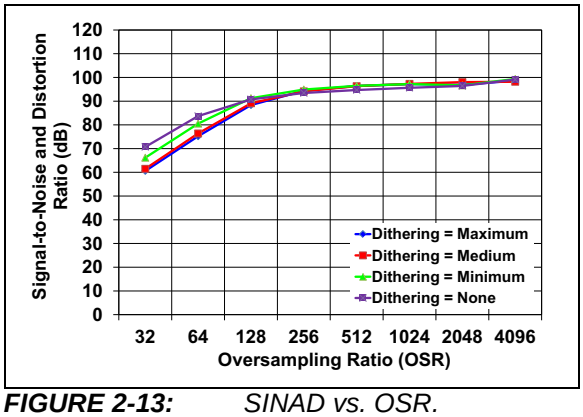


FIGURE 2-13: *SINAD vs. OSR.*

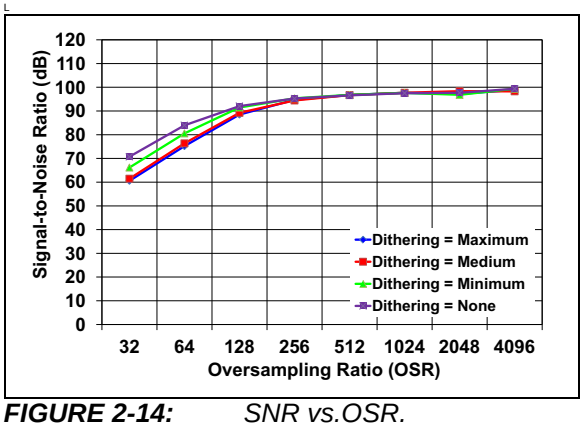


FIGURE 2-14: *SNR vs.OSR.*

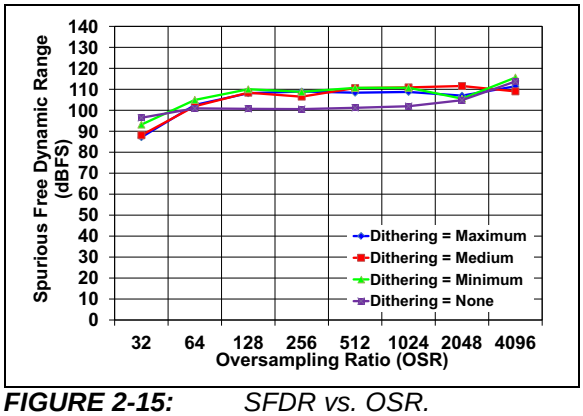


FIGURE 2-15: *SFDR vs. OSR.*

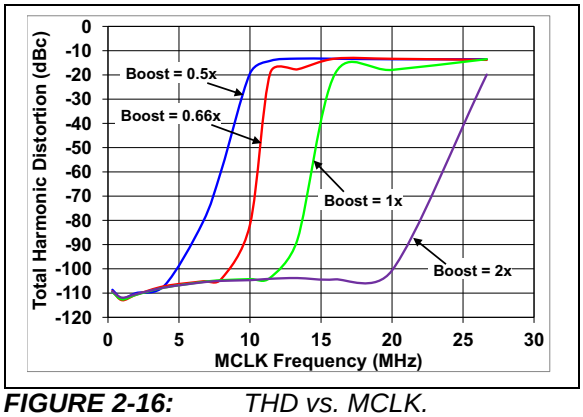


FIGURE 2-16: *THD vs. MCLK.*

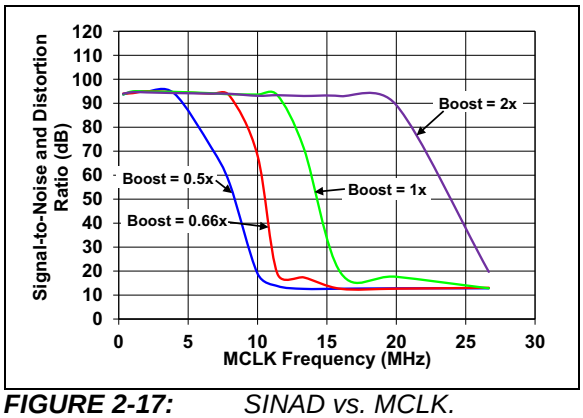


FIGURE 2-17: *SINAD vs. MCLK.*

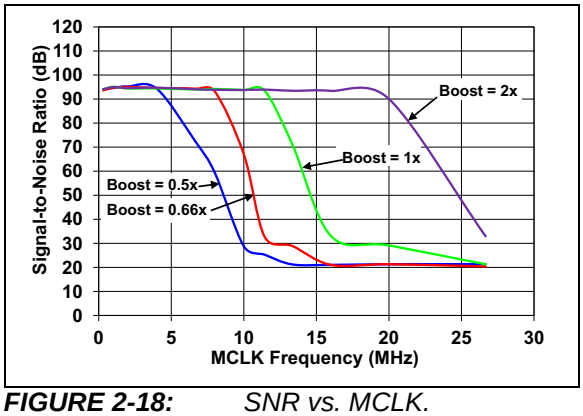


FIGURE 2-18: *SNR vs. MCLK.*

Note: Unless otherwise indicated, AV_{DD} = 3.3V; DV_{DD} = 3.3V; T_A = +25°C; MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS at 60 Hz; VREFEXT = 0; CLKEXT = 1; AZ_FREQ = 0; BOOST = 1x.

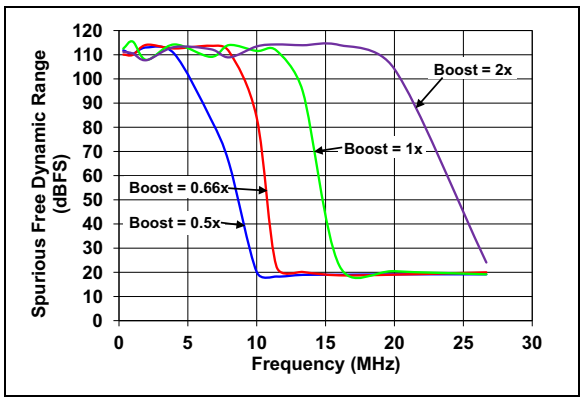


FIGURE 2-19: *SFDR vs. MCLK.*

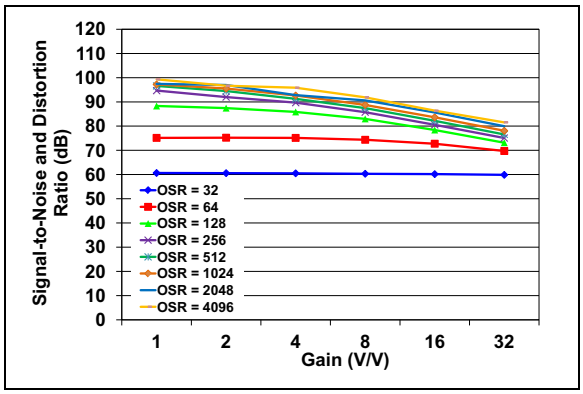


FIGURE 2-20: *SINAD vs. GAIN.*

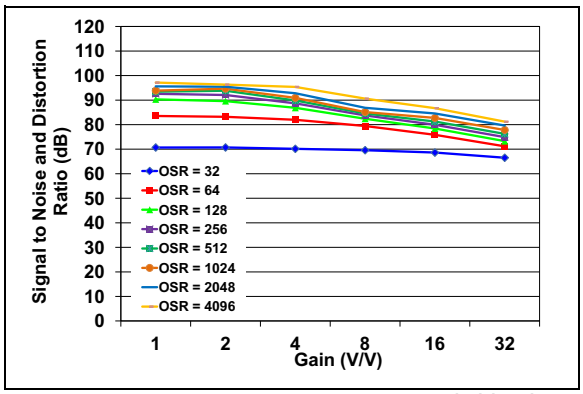


FIGURE 2-21: *SINAD vs. GAIN (Dithering Off).*

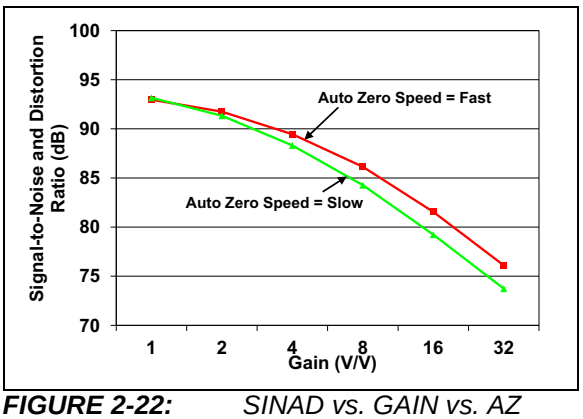


FIGURE 2-22: *SINAD vs. GAIN vs. AZ Speed Chart.*

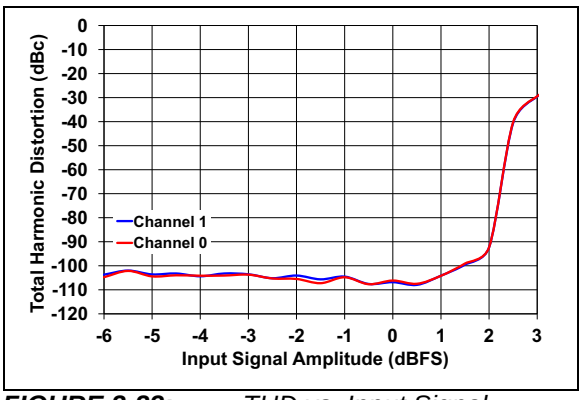


FIGURE 2-23: *THD vs. Input Signal Amplitude.*

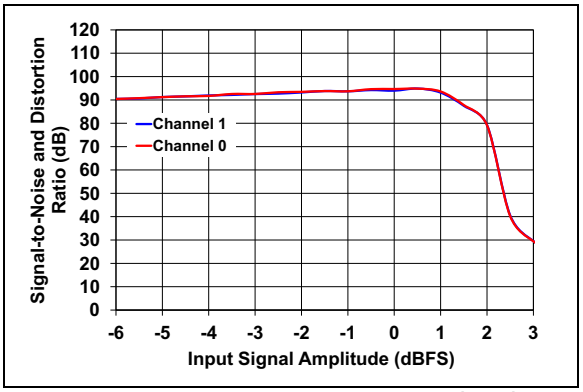


FIGURE 2-24: *SINAD vs. Input Signal Amplitude.*

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Note: Unless otherwise indicated, AV_{DD} = 3.3V; DV_{DD} = 3.3V; T_A = +25°C; MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS at 60 Hz; VREFEXT = 0; CLKEXT = 1; AZ_FREQ = 0; BOOST = 1x.

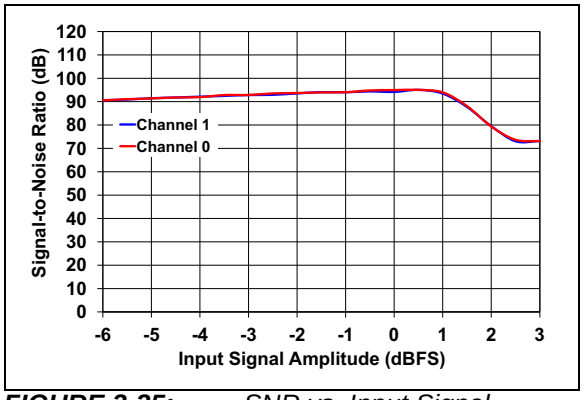


FIGURE 2-25: *SNR vs. Input Signal Amplitude.*

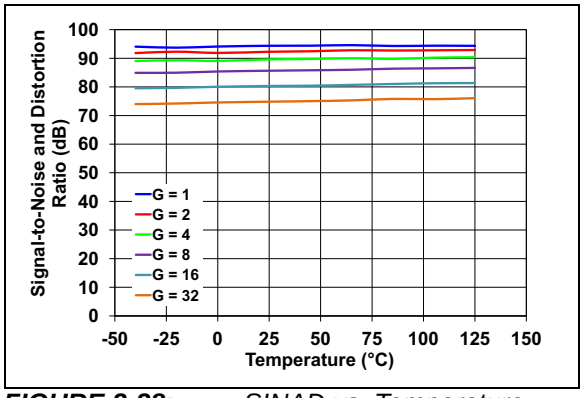


FIGURE 2-28: *SINAD vs. Temperature.*

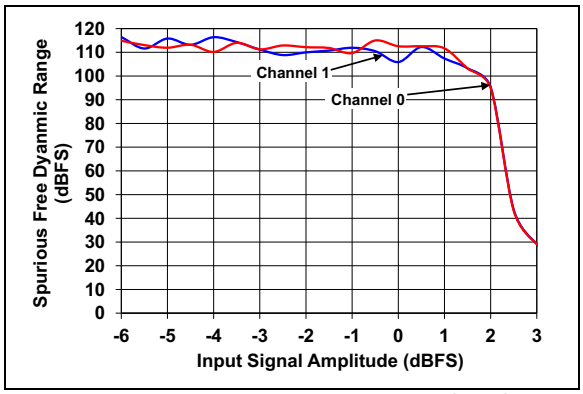


FIGURE 2-26: *SFDR vs. Input Signal Amplitude.*

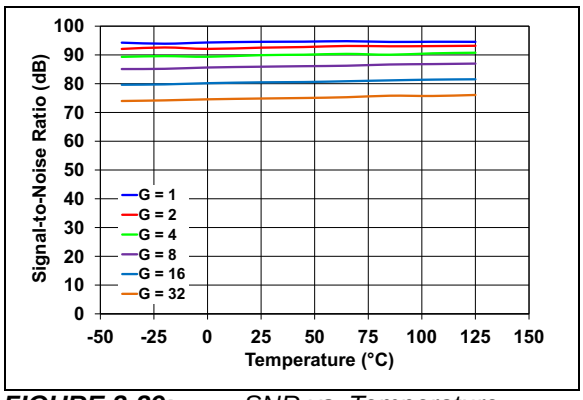


FIGURE 2-29: *SNR vs. Temperature.*

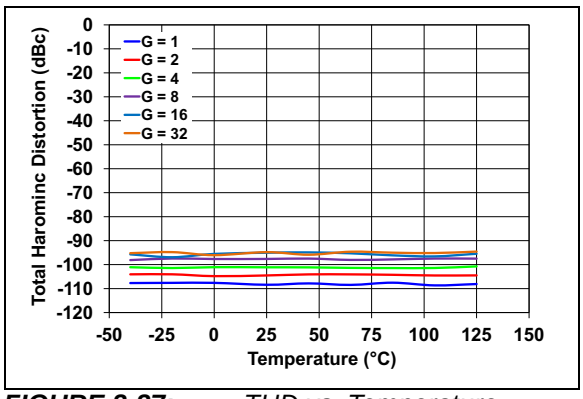


FIGURE 2-27: *THD vs. Temperature.*

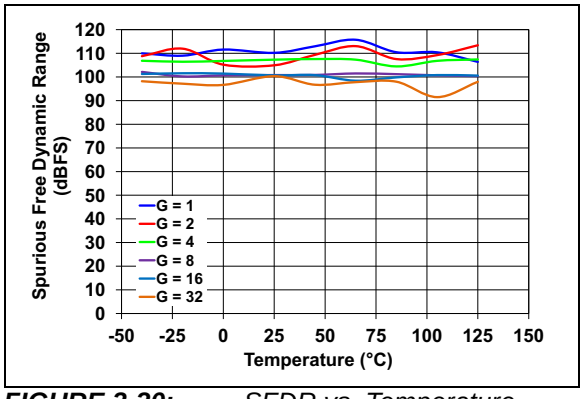


FIGURE 2-30: *SFDR vs. Temperature.*

Note: Unless otherwise indicated, AV_{DD} = 3.3V; DV_{DD} = 3.3V; T_A = +25°C; MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS at 60 Hz; VREFEXT = 0; CLKEXT = 1; AZ_FREQ = 0; BOOST = 1x.

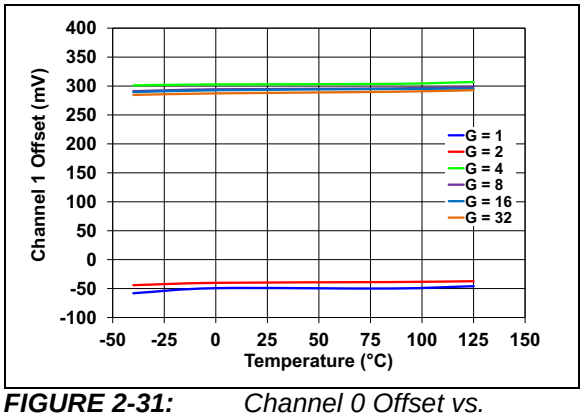


FIGURE 2-31: *Channel 0 Offset vs. Temperature.*

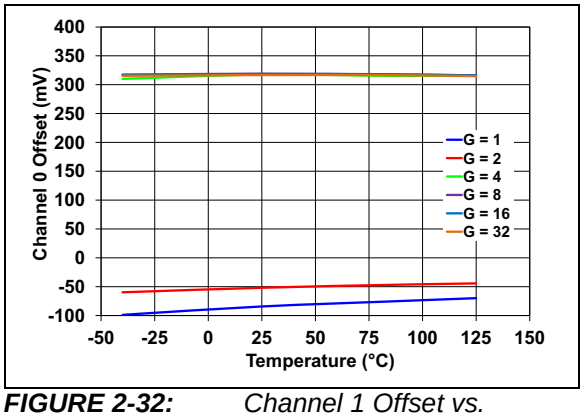


FIGURE 2-32: *Channel 1 Offset vs. Temperature.*

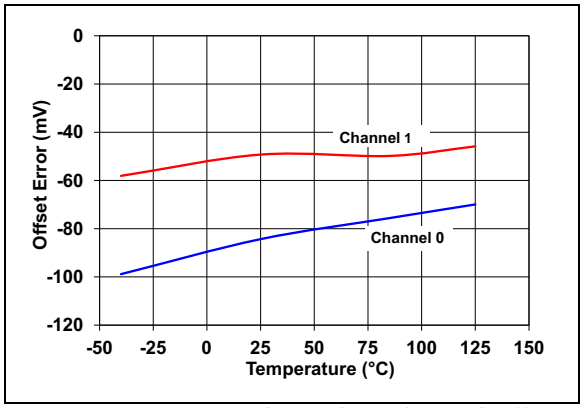


FIGURE 2-33: *Channel-to-Channel Offset Match vs. Temperature.*

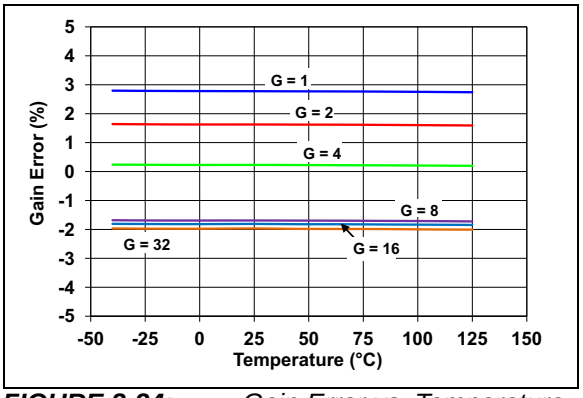


FIGURE 2-34: *Gain Error vs. Temperature.*

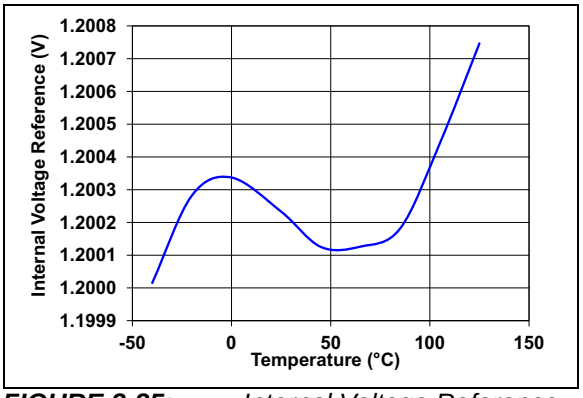


FIGURE 2-35: *Internal Voltage Reference vs. Temperature.*

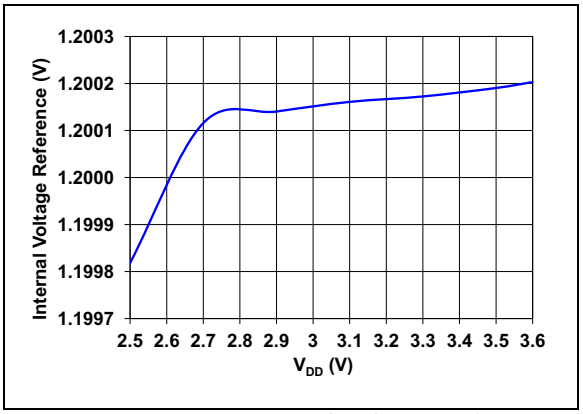


FIGURE 2-36: *Internal Voltage Reference vs. Supply Voltage.*

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Note: Unless otherwise indicated, AV_{DD} = 3.3V; DV_{DD} = 3.3V; T_A = +25°C; MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS at 60 Hz; VREFEXT = 0; CLKEXT = 1; AZ_FREQ = 0; BOOST = 1x.

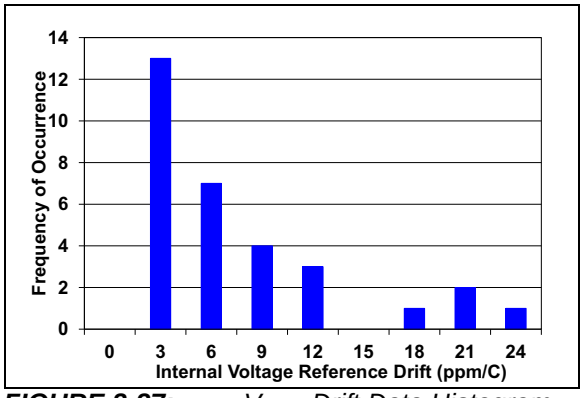


FIGURE 2-37: *V_{REF} Drift Data Histogram Chart.*

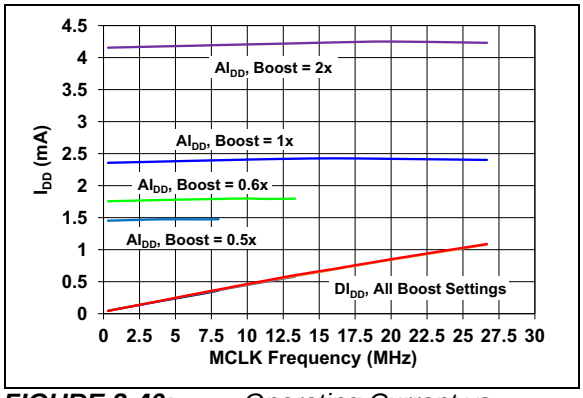


FIGURE 2-40: *Operating Current vs. MCLK, V_{DD} = 3.3V.*

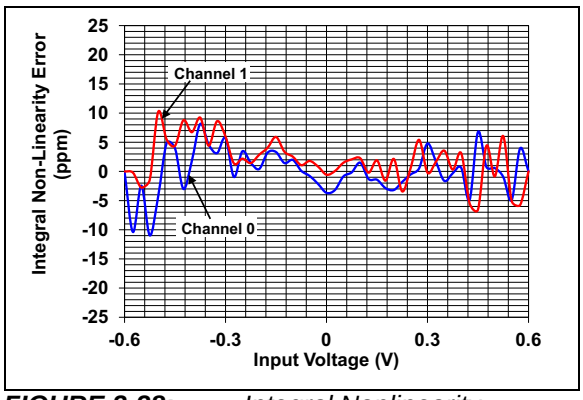


FIGURE 2-38: *Integral Nonlinearity (Dithering Maximum).*

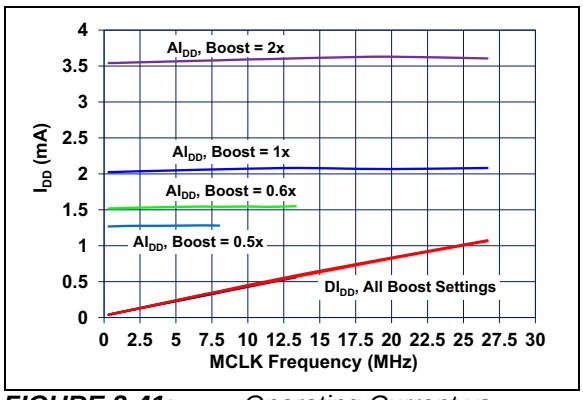


FIGURE 2-41: *Operating Current vs. MCLK, V_{DD} = 2.7V.*

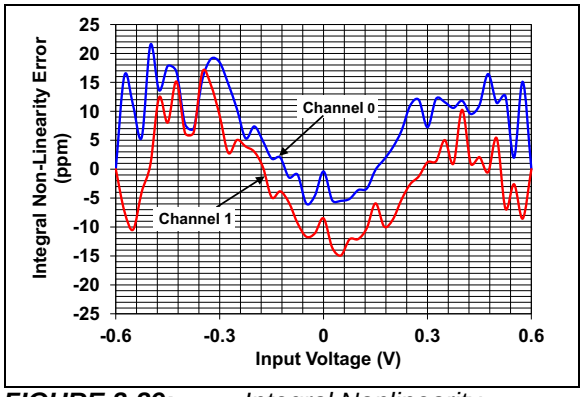


FIGURE 2-39: *Integral Nonlinearity (Dithering Off).*

NOTES:

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3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No. SSOP	Pin No. QFN	Symbol	Function
1	18	$\overline{RESET}$	Master Reset Logic Input Pin
2	19	DV_{DD}	Digital Power Supply Pin
3	20	AV_{DD}	Analog Power Supply Pin
4	1	CH0+	Noninverting Analog Input Pin for Channel 0
5	2	CH0-	Inverting Analog Input Pin for Channel 0
6	3	CH1-	Inverting Analog Input Pin for Channel 1
7	4	CH1+	Noninverting Analog Input Pin for Channel 1
8	5	A_{GND}	Analog Ground Pin, Return Path for Internal Analog Circuitry
9	6	REFIN+/OUT	Noninverting Voltage Reference Input and Internal Reference Output Pin
10	7	REFIN-	Inverting Voltage Reference Input Pin
11	8	D_{GND}	Digital Ground Pin, Return Path for Internal Digital Circuitry
12	9	MDAT1	Modulator Data Output Pin for Channel 1
13	10	MDAT0	Modulator Data Output Pin for Channel 0
14	11	$\overline{DR}$	Data Ready Signal Output Pin
15	12	OSC1/CLKI	Oscillator Crystal Connection Pin or External Clock Input Pin
16	13	OSC2	Oscillator Crystal Connection Pin
17	14	$\overline{CS}$	Serial Interface Chip Select Pin
18	15	SCK	Serial Interface Clock Input Pin
19	16	SDO	Serial Interface Data Input Pin
20	17	SDI	Serial Interface Data Input Pin
—	21	EP	Exposed Thermal Pad. Must be connected to A_{GND} or left floating.

3.1 Master Reset ($\overline{RESET}$)

This pin is active-low and places the entire chip in a Reset state when active.

When $\overline{RESET}$ = D_{GND}, all registers are reset to their default value and no communication can take place. No clock is distributed inside the part, except in the input structure, if MCLK is applied (if Idle, no clock is distributed). This state is equivalent to a POR state.

Since the default state of the ADCs is on, the analog power consumption when $\overline{RESET}$ = D_{GND} is equivalent to $\overline{RESET}$ = V_{DD}. Only the digital power consumption is largely reduced because this current consumption is essentially dynamic and is reduced drastically when there is no running clock.

All the analog biases are enabled during a Reset so that the part is fully operational just after a $\overline{RESET}$ rising edge, if the MCLK is applied during the rising edge. If not applied, there is a small time after $\overline{RESET}$ when the conversion may not be accurate, corresponding to the start-up of the charge pump of the input structure.

This input is Schmitt triggered.

3.2 Digital V_{DD} (DV_{DD})

DV_{DD} is the power supply pin for the digital circuitry within the MCP3911. For specified operation, this pin requires appropriate bypass capacitors and should be maintained between 2.7V and 3.6V.

3.3 Analog V_{DD} (AV_{DD})

AV_{DD} is the power supply pin for the analog circuitry within the MCP3911. For specified operation, this pin requires appropriate bypass capacitors and should be maintained between 2.7V and 3.6V.

3.4 ADC Differential Analog inputs (CHn+/CHn-)

The two fully differential analog voltage inputs for the Delta-Sigma ADCs are:

- CH0- and CH0+
- CH1- and CH1+

The linear and specified region of the channels is dependent on the PGA gain. This region corresponds to a differential voltage range of ±600 mV/GAIN with V_{REF} = 1.2V.

The maximum differential voltage is proportional to the V_{REF} voltage. The maximum absolute voltage, with respect to A_{GND}, for each CHn+/- input pin is ±1V with no distortion, and ±2V with no breaking after continuous voltage. This maximum absolute voltage is not proportional to the V_{REF} voltage.

3.5 Analog Ground (A_{GND})

A_{GND} is the ground connection to the internal analog circuitry (see the **Functional Block Diagram**). To ensure accuracy and noise cancellation, this pin must be connected to the same ground as D_{GND}, preferably with a star connection. If an analog ground plane is available, it is recommended that this pin is tied to this Printed Circuit Board (PCB) plane. This plane should also reference all other analog circuitry in the system.

3.6 Noninverting Reference Input, Internal Reference Output (REFIN+/OUT)

This pin is the noninverting side of the differential voltage reference input for both ADCs or the internal voltage reference output.

When VREFEXT = 1, an external voltage reference source can be used and the internal voltage reference is disabled. When using an external differential voltage reference, it should be connected to its V_{REF}+ pin. When using an external single-ended reference, it should be connected to this pin.

When VREFEXT = 0, the internal voltage reference is enabled and connected to this pin through a switch. If used as a voltage source, this voltage reference has a minimal drive capability, and thus needs proper buffering and bypass capacitances. A 0.1 µF ceramic capacitor is sufficient in most cases.

If the voltage reference is only used as an internal V_{REF}, adding bypass capacitance on REFIN+/OUT is not necessary for keeping ADC accuracy. If left floating, a minimal 0.1 µF ceramic capacitance can be connected to avoid EMI/EMC susceptibility issues due to the antenna created by the REFIN+/OUT pin.

3.7 Inverting Reference Input (REFIN-)

This pin is the inverting side of the differential voltage reference input for both ADCs. When using an external differential voltage reference, it should be connected to its V_{REF}- pin. When using an external single-ended voltage reference, or when VREFEXT = 0 (default) and using the internal voltage reference, this pin should be directly connected to A_{GND}.

3.8 Digital Ground Connection (D_{GND})

D_{GND} is the ground connection to the internal digital circuitry (see **Functional Block Diagram**). To ensure optimal accuracy and noise cancellation, D_{GND} must be connected to the same ground as A_{GND}, preferably with a star connection. If a digital ground plane is available, it is recommended that this pin is tied to this PCB plane. This plane should also reference all other digital circuitry in the system.

3.9 Modulator Data Output Pin for Channel 1 and Channel 0 (MDAT1/MDAT0)

MDAT0 and MDAT1 are the output pins for the modulator serial bit streams of ADC Channels 0 and 1, respectively. These pins are high-impedance when their corresponding MODOUT bit is logic low. When the MODOUT[1:0] bits are enabled, the modulator bit stream of the corresponding channel is present on the pin and updated at the AMCLK frequency (see **Section 5.4 "Modulator Output Block"** for a complete description of the modulator outputs). These pins can be directly connected to an MCU or a DSP when a specific digital filtering is needed.

3.10 Data Ready Output ($\overline{DR}$)

The Data Ready pin indicates that a new conversion result is ready to be read. The default state of this pin is high when $\overline{DR_HIZ}$ = 1 and is high-impedance when $\overline{DR_HIZ}$ = 0 (default). After each conversion is finished, a logic low pulse takes place on the Data Ready pin to indicate that the conversion result is ready as an interrupt. This pulse is synchronous with the master clock and has a defined and constant width.

The Data Ready pin is independent of the SPI interface and acts like an interrupt output. The Data Ready pin state is not latched and the pulse width (and period) are both determined by the MCLK frequency oversampling rate and internal clock prescale settings. The $\overline{DR}$ pulse width is equal to one DMCLK period and the frequency of the pulses is equal to DRCLK (see Figure 1-3).

Note:	This pin should not be left floating when the $\overline{DR_HIZ}$ bit is low; a 100 kΩ pull-up resistor connected to DV_{DD} is recommended.

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3.11 Oscillator and Master Clock Input Pins (OSC1/CLKI, OSC2)

OSC1/CLKI and OSC2 provide the Master Clock (MCLK) for the device. When CLKEXT = 0, a resonant crystal or clock source with a similar sinusoidal waveform must be placed across these pins to ensure proper operation. The typical clock frequency specified is 4 MHz. For proper operation and optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-3 as a function of the BOOST and PGA settings chosen. MCLK can take larger values as long as the prescaler settings (PRE[1:0]) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-3. For proper operation, appropriate load capacitance should be connected to these pins.

3.12 Chip Select ($\overline{CS}$)

This pin is the SPI chip select that enables the serial communication. When this pin is high, no communication can take place. A chip select falling edge initiates the serial communication and a chip select rising edge terminates the communication. No communication can take place when $\overline{CS}$ is low or when $\overline{RESET}$ is low.

This input is Schmitt triggered.

3.13 Serial Data Clock (SCK)

This is the serial clock pin for SPI communication.

Data are clocked into the device on the RISING edge and out of the device on the FALLING edge of SCK.

The MCP3911 interface is compatible with both SPI 0,0 and 1,1 modes. SPI modes can be changed during a $\overline{CS}$ high time.

The maximum clock speed specified is 20 MHz.

This input is Schmitt triggered.

3.14 Serial Data Output (SDO)

This is the SPI data output pin. Data are clocked out of the device on the FALLING edge of SCK.

This pin stays high-impedance during the first command byte. It also stays high-impedance during the whole communication for write commands and when the $\overline{CS}$ pin is high or when the $\overline{RESET}$ pin is low. This pin is active only when a read command is processed. Each read is processed by packet of eight bits.

3.15 Serial Data Input (SDI)

This is the SPI data input pin. Data are clocked into the device on the RISING edge of SCK.

When $\overline{CS}$ is low, this pin is used to communicate with a series of 8-bit commands.

The interface is half-duplex (inputs and outputs do not happen at the same time).

Each communication starts with a chip select falling edge, followed by an 8-bit command word entered through the SDI pin. Each command is either a read or write command. Toggling SDI during a read command has no effect.

This input is Schmitt triggered.

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NOTES:

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4.0 TERMINOLOGIES AND FORMULAS

This section defines the terms and formulas used throughout this data sheet. The following terms are defined:

- **MCLK – Master Clock**
- **AMCLK – Analog Master Clock**
- **DMCLK – Digital Master Clock**
- **DRCLK – Data Rate Clock**
- **OSR – Oversampling Ratio**
- **Offset Error**
- **Gain Error**
- **Integral Nonlinearity Error**
- **Signal-to-Noise Ratio (SNR)**
- **Signal-to-Noise Ratio and Distortion (SINAD)**
- **Total Harmonic Distortion (THD)**
- **Spurious-Free Dynamic Range (SFDR)**
- **MCP3911 Delta-Sigma Architecture**
- **Idle Tones**
- **Dithering**
- **Crosstalk**
- **PSRR**
- **CMRR**
- **ADC Reset Mode**
- **Hard Reset Mode (RESET = DGND)**
- **ADC Shutdown Mode**
- **Full Shutdown Mode**

4.1 MCLK – Master Clock

This is the fastest clock present in the device. This is the frequency of the crystal placed at the OSC1/OSC2 inputs when CLKEXT = 0 or the frequency of the clock input at the OSC1/CLKI when CLKEXT = 1. See Figure 4-1.

4.2 AMCLK – Analog Master Clock

This is the clock frequency that is present on the analog portion of the device after prescaling has occurred via the CONFIG PRE[1:0] register bits. The analog portion includes the PGAs and the two Delta-Sigma modulators.

$$AMCLK = \frac{MCLK}{PRESCALE}$$

TABLE 4-1: MCP3911 OVERSAMPLING RATIO SETTINGS

Config PRE[1:0]		Analog Master Clock Prescale
0	0	AMCLK = MCLK/1 (default)
0	1	AMCLK = MCLK/2
1	0	AMCLK = MCLK/4
1	1	AMCLK = MCLK/8

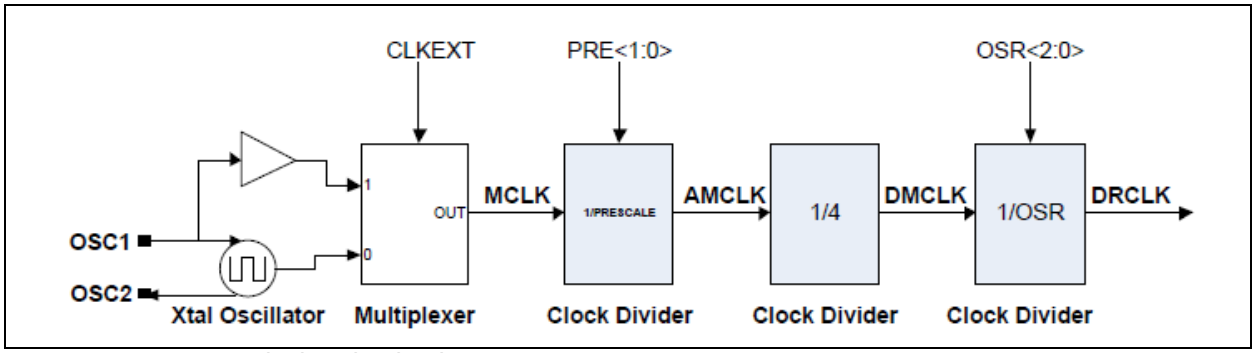


FIGURE 4-1: *Clock Sub-Circuitry.*

4.3 DMCLK – Digital Master Clock

This is the clock frequency that is present on the digital portion of the device after prescaling and division by four. This is also the sampling frequency, which is the rate at which the modulator outputs are refreshed. Each period of this clock corresponds to one sample and one modulator output. See Figure 4-1.

EQUATION 4-1:

$$DMCLK = \frac{AMCLK}{4} = \frac{MCLK}{4 \times PRESCALE}$$

4.4 DRCLK – Data Rate Clock

This is the output data rate (i.e., the rate at which the ADCs output new data). New data are signaled by a data ready pulse on the $\overline{DR}$ pin.

This data rate is dependent on the OSR and the prescaler with the following formula:

EQUATION 4-2:

$$DRCLK = \frac{DMCLK}{OSR} = \frac{AMCLK}{4 \times OSR} = \frac{MCLK}{4 \times OSR \times PRESCALE}$$

Since this is the output data rate and the decimation filter is a SINC (or notch) filter, there is a notch in the filter transfer function at each integer multiple of this rate.

The following table describes the various combinations of OSR and PRESCALE and their associated AMCLK, DMCLK and DRCLK rates.

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TABLE 4-2: DEVICE DATA RATES IN FUNCTION OF MCLK, OSR AND PRESCALE, MCLK = 4 MHz

PRE[1:0]		OSR[2:0]			OSR	AMCLK	DMCLK	DRCLK	DRCLK (ksps)	SINAD (dB)(1)	ENOB from SINAD (bits)(1)
1	1	1	1	1	4096	MCLK/8	MCLK/32	MCLK/131072	0.035	98	16
1	1	1	1	1	2048	MCLK/8	MCLK/32	MCLK/65536	0.061	98	16
1	1	1	1	1	1024	MCLK/8	MCLK/32	MCLK/32768	0.122	97	15.8
1	1	1	1	1	512	MCLK/8	MCLK/32	MCLK/16384	0.244	96	15.6
1	1	0	1	1	256	MCLK/8	MCLK/32	MCLK/8192	0.488	95	15.5
1	1	0	1	0	128	MCLK/8	MCLK/32	MCLK/4096	0.976	90	14.7
1	1	0	0	1	64	MCLK/8	MCLK/32	MCLK/2048	1.95	83	13.5
1	1	0	0	0	32	MCLK/8	MCLK/32	MCLK/1024	3.9	70	11.3
1	0	1	1	1	4096	MCLK/4	MCLK/16	MCLK/65536	0.061	98	16
1	0	1	1	1	2048	MCLK/4	MCLK/16	MCLK/32768	0.122	98	16
1	0	1	1	1	1024	MCLK/4	MCLK/16	MCLK/16384	0.244	97	15.8
1	0	1	1	1	512	MCLK/4	MCLK/16	MCLK/8192	0.488	96	15.6
1	0	0	1	1	256	MCLK/4	MCLK/16	MCLK/4096	0.976	95	15.5
1	0	0	1	0	128	MCLK/4	MCLK/16	MCLK/2048	1.95	90	14.7
1	0	0	0	1	64	MCLK/4	MCLK/16	MCLK/1024	3.9	83	13.5
1	0	0	0	0	32	MCLK/4	MCLK/16	MCLK/512	7.8125	70	11.3
0	1	1	1	1	4096	MCLK/2	MCLK/8	MCLK/32768	0.122	98	16
0	1	1	1	1	2048	MCLK/2	MCLK/8	MCLK/16384	0.244	98	16
0	1	1	1	1	1024	MCLK/2	MCLK/8	MCLK/8192	0.488	97	15.8
0	1	1	1	1	512	MCLK/2	MCLK/8	MCLK/4096	0.976	96	15.6
0	1	0	1	1	256	MCLK/2	MCLK/8	MCLK/2048	1.95	95	15.5
0	1	0	1	0	128	MCLK/2	MCLK/8	MCLK/1024	3.9	90	14.7
0	1	0	0	1	64	MCLK/2	MCLK/8	MCLK/512	7.8125	83	13.5
0	1	0	0	0	32	MCLK/2	MCLK/8	MCLK/256	15.625	70	11.3
0	0	1	1	1	4096	MCLK	MCLK/4	MCLK/16384	0.244	98	16
0	0	1	1	0	2048	MCLK	MCLK/4	MCLK/8192	0.488	98	16
0	0	1	0	1	1024	MCLK	MCLK/4	MCLK/4096	0.976	97	15.8
0	0	1	0	0	512	MCLK	MCLK/4	MCLK/2048	1.95	96	15.6
0	0	0	1	1	256	MCLK	MCLK/4	MCLK/1024	3.9	95	15.5
0	0	0	1	0	128	MCLK	MCLK/4	MCLK/512	7.8125	90	14.7
0	0	0	0	1	64	MCLK	MCLK/4	MCLK/256	15.625	83	13.5
0	0	0	0	0	32	MCLK	MCLK/4	MCLK/128	31.25	70	11.3

Note 1: For OSR = 32 and 64, DITHER = None. For OSR = 128 and higher, DITHER = Maximum. The SINAD values are given from GAIN = 1.

4.5 OSR – Oversampling Ratio

This is the ratio of the sampling frequency to the output data rate. OSR = DMCLK/DRCLK. The default OSR is 256 or with MCLK = 4 MHz, PRESCALE = 1, AMCLK = 4 MHz, f_S = 1 MHz, f_D = 3.90625 ksps. The following bits in the CONFIG register are used to change the Oversampling Ratio (OSR).

TABLE 4-3: MCP3911 OVERSAMPLING RATIO SETTINGS

CONFIG OSR[2:0]			Oversampling Ratio (OSR)
0	0	0	32
0	0	1	64
0	1	0	128
0	1	1	256 (default)
1	0	0	512
1	0	1	1024
1	1	0	2048
1	1	1	4096

4.6 Offset Error

This is the error induced by the ADC when the inputs are shorted together (V_{IN} = 0V). The specification incorporates both PGA and ADC offset contributions. This error varies with PGA and OSR settings. The offset is different on each channel and varies from chip-to-chip. The offset is specified in µV. The offset error can be digitally compensated independently on each channel through the OFFCAL registers with a 24-bit Calibration Word.

The offset on the MCP3911 has a low temperature coefficient (see **Section 2.0, Typical Performance Curves** for more information, see Figure 2-33).

4.7 Gain Error

This is the error induced by the ADC on the slope of the transfer function. It is the deviation expressed in percentage (%) compared to the ideal transfer function defined by Equation 5-3. The specification incorporates both PGA and ADC gain error contributions, but not the V_{REF} contribution (it is measured with an external V_{REF}).

This error varies with PGA and OSR settings. The gain error can be digitally compensated independently on each channel through the GAINCAL registers with a 24-bit Calibration Word.

The gain error on the MCP3911 has a low temperature coefficient. For more information, see Figure 2-34.

4.8 Integral Nonlinearity Error

Integral nonlinearity error is the maximum deviation of an ADC transition point from the corresponding point of an ideal transfer function, with the offset and gain errors removed or with the end points equal to zero.

It is the maximum remaining error after the calibration of offset and gain errors for a DC input signal.

4.9 Signal-to-Noise Ratio (SNR)

For the MCP3911 ADCs, the Signal-to-Noise Ratio is a ratio of the output fundamental signal power to the noise power (not including the harmonics of the signal), when the input is a sine wave at a predetermined frequency. It is measured in dB. Usually, only the maximum Signal-to-Noise Ratio is specified. The SNR figure depends mainly on the OSR and DITHER settings of the device.

EQUATION 4-3: SIGNAL-TO-NOISE RATIO

$$SNR(dB) = 10log\left(\frac{SignalPower}{NoisePower}\right)$$

4.10 Signal-to-Noise Ratio and Distortion (SINAD)

The most important figure of merit for the analog performance of the ADCs present on the MCP3911 is the Signal-to-Noise Ratio and Distortion (SINAD) specification.

Signal-to-Noise and Distortion Ratio is similar to Signal-to-Noise Ratio, with the exception that you must include the harmonics power in the noise power calculation. The SINAD specification depends mainly on the OSR and DITHER settings.

EQUATION 4-4: SINAD EQUATION

$$SINAD(dB) = 10log\left(\frac{SignalPower}{Noise + HarmonicsPower}\right)$$

The calculated combination of SNR and THD per the following formula also yields SINAD:

EQUATION 4-5: SINAD, THD AND SNR RELATIONSHIP

$$SINAD(dB) = 10log\left[10^{\left(\frac{SNR}{10}\right)} + 10^{\left(\frac{-THD}{10}\right)}\right]$$

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4.11 Total Harmonic Distortion (THD)

The Total Harmonic Distortion is the ratio of the output harmonics power to the fundamental signal power for a sine wave input and is defined by Equation 4-6.

EQUATION 4-6:

$$THD(dB) = 10log\left(\frac{HarmonicsPower}{FundamentalPower}\right)$$

The THD calculation includes the first 35 harmonics for the MCP3911 specifications. The THD is usually only measured with respect to the first ten harmonics. THD is sometimes expressed in percentage (%). Equation 4-7 converts the THD in percentage (%):

EQUATION 4-7:

$$THD(\%) = 100 \times 10^{\frac{THD(dB)}{20}}$$

This specification depends mainly on the DITHER setting.

4.12 Spurious-Free Dynamic Range (SFDR)

The ratio between the output power of the fundamental and the highest spur in the frequency spectrum. The spur frequency is not necessarily a harmonic of the fundamental, even though that is usually the case. This figure represents the dynamic range of the ADC when a full-scale signal is used at the input. This specification depends mainly on the DITHER setting.

EQUATION 4-8:

$$SFDR(dB) = 10log\left(\frac{FundamentalPower}{HighestSpurPower}\right)$$

4.13 MCP3911 Delta-Sigma Architecture

The MCP3911 incorporates two Delta-Sigma ADCs with a multibit architecture. A Delta-Sigma ADC is an oversampling converter that incorporates a built-in modulator, which is digitizing the quantity of charge integrated by the modulator loop (see Figure 5-1). The quantizer is the block that is performing the Analog-to-Digital conversion. The quantizer is typically one bit or a simple comparator which helps to maintain the linearity performance of the ADC (the DAC structure in this case is inherently linear).

Multibit quantizers help lower the quantization error (the error fed back in the loop can be very large with 1-bit quantizers) without changing the order of the modulator or the OSR, which leads to better SNR figures. However, typically, the linearity of such architectures is more difficult to achieve since the DAC is complicated and its linearity limits the THD of such ADCs.

The MCP3911's five-level quantizer is a Flash ADC composed of four comparators, arranged with equally spaced thresholds and a thermometer coding. The MCP3911 also includes proprietary five-level DAC architecture that is inherently linear for improved THD figures.

4.14 Idle Tones

A Delta-Sigma converter is an integrating converter. It also has a finite quantization step Least Significant Byte (LSB) which can be detected by its quantizer. A DC input voltage that is below the quantization step should only provide an all zeros result, since the input is not large enough to be detected. As an integrating device, any Delta-Sigma shows Idle tones in this case. This means that the output will have spurs in the frequency content that are depending on the ratio between quantization step voltage and the input voltage. These spurs are the result of the integrated sub-quantization step inputs that eventually cross the quantization steps after a long enough integration. This induces an AC frequency at the output of the ADC and can be shown in the ADC output spectrum.

These Idle tones are residues that are inherent to the quantization process and the fact that the converter is integrating at all times without being reset. They are residues of the finite resolution of the conversion process. They are very difficult to attenuate and they are heavily signal-dependent. They can degrade both SFDR and THD of the converter, even for DC inputs. They can be localized in the baseband of the converter and thus difficult to filter from the actual input signal.

For power metering applications, Idle tones can be very disturbing because energy can be detected even at the 50 or 60 Hz frequency, depending on the DC offset of the ADCs, while no power is really present at the inputs. The only practical way to suppress or attenuate Idle tones phenomenon is to apply dithering to the ADC. The Idle tone amplitudes are a function of the order of the modulator, the OSR and the number of levels in the quantizer of the modulator. A higher order, a higher OSR or a higher number of levels for the quantizer attenuate the Idle tones amplitude.

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4.15 Dithering

To suppress or attenuate the Idle tones present in any Delta-Sigma ADCs, dithering can be applied to the ADC. Dithering is the process of adding an error to the ADC feedback loop to “decorrelate” the outputs and “break” the Idle tone behavior. Usually, a random or pseudorandom generator adds an analog or digital error to the feedback loop of the Delta-Sigma ADC to ensure that no tonal behavior can happen at its outputs. This error is filtered by the feedback loop and typically has a zero average value, so that the converter static transfer function is not disturbed by the dithering process. However, the dithering process slightly increases the noise floor (it adds noise to the part) while reducing its tonal behavior, and thus improving SFDR and THD (see Figure 2-14 and Figure 2-18). The dithering process scrambles the Idle tones into baseband white noise and ensures that dynamic specs (SNR, SINAD, THD, SFDR) are less signal-dependent. The MCP3911 incorporates a proprietary dithering algorithm on both ADCs to remove Idle tones and improve THD, which is crucial for power metering applications.

4.16 Crosstalk

The crosstalk is defined as the perturbation caused by one ADC channel on the other ADC channel. It is a measurement of the isolation between the two ADCs present in the chip.

This measurement is a two-step procedure:

1. Measure one ADC input with no perturbation on the other ADC (ADC inputs shorted).
2. Measure the same ADC input with a perturbation sine wave signal on the other ADC at a certain predefined frequency.

The crosstalk is then the ratio between the output power of the ADC when the perturbation is present and when it is not divided by the power of the perturbation signal.

A lower crosstalk value implies more independence and isolation between the two channels.

The measurement of this signal is performed under the default conditions at MCLK = 4 MHz:

- GAIN = 1
- PRESCALE = 1
- OSR = 256
- MCLK = 4 MHz

Step 1

- CH0+ = CH0- = A_{GND}
- CH1+ = CH1- = A_{GND}

Step 2

- CH0+ = CH0- = A_{GND}
- CH1+ – CH1- = 1.2 V_{P-P} at 50/60 Hz (full-scale sine wave)

The crosstalk is then calculated with the following formula:

EQUATION 4-9:

$$CTalk(dB) = 10log\left(\frac{\Delta CH0Power}{\Delta CH1Power}\right)$$

4.17 PSRR

This is the ratio between a change in the power supply voltage and the ADC output codes. It measures the influence of the power supply voltage on the ADC outputs.

The PSRR specification can be DC (the power supply is taking multiple DC values) or AC (the power supply is a sine wave at a certain frequency with a certain Common-mode). In AC, the amplitude of the sine wave is representing the change in the power supply. It is defined in Equation 4-10:

EQUATION 4-10:

$$PSRR(dB) = 20log\left(\frac{\Delta V_{OUT}}{\Delta AV_{DD}}\right)$$

Where V_{OUT} is the equivalent input voltage that the output code translates to the ADC transfer function. In the MCP3911 specification, AV_{DD} varies from 2.7V to 3.6V. For AC PSRR, a 50/60 Hz sine wave is chosen, centered around 3.3V with a maximum 300 mV amplitude. The PSRR specification is measured with $AV_{DD} = DV_{DD}$.

4.18 CMRR

This is the ratio between a change in the Common-mode input voltage and the ADC output codes. It measures the influence of the Common-mode input voltage on the ADC outputs.

The CMRR specification can be DC (the Common-mode input voltage is taking multiple DC values) or AC (the Common-mode input voltage is a sine wave at a certain frequency with a certain Common-mode). In AC, the amplitude of the sine wave is representing the change in the power supply. It is defined in Equation 4-11:

EQUATION 4-11:

$$CMRR(dB) = 20log\left(\frac{\Delta V_{OUT}}{\Delta V_{CM}}\right)$$

Where V_{CM} = (CHn+ + CHn-)/2 is the Common-mode input voltage and V_{OUT} is the equivalent input voltage that the output code translates to using the ADC transfer function. In the MCP3911 specification, V_{CM} varies from -1V to +1V.

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4.19 ADC Reset Mode

ADC Reset mode (also called Soft Reset mode) can only be entered through setting the RESET[1:0] bits in the Configuration register high. This mode is defined as the condition where the converters are active, but their output is forced to '0'.

The registers are not affected in this Reset mode and retain their state, except the data registers of the corresponding channel, which are reset to '0'.

The ADCs can immediately output meaningful codes after leaving the Reset mode (and after the SINC filter settling time). This mode is both entered and exited through the setting of bits in the Configuration register.

Each converter can be placed in Soft Reset mode independently. The Configuration registers are not modified by the Soft Reset mode.

A data ready pulse is not generated by any ADC while in Reset mode.

Reset mode also affects the modulator output block (i.e., the MDAT pin corresponding to the channel in Reset). If enabled, it provides a bit stream corresponding to a zero output (a series of '0011' bits continuously repeated).

When an ADC exits the ADC Reset mode, any phase delay present before Reset was entered is still present. If one ADC is not in Reset mode, the ADC leaving the Reset mode automatically resynchronizes the phase delay relative to the other ADC channel, per the Phase Delay register block, and gives data ready pulses accordingly.

If an ADC is placed in Reset mode while the other is converting, it is not shutting down the internal clock. When going back out of Reset, it is automatically resynchronized with the clock that did not stop during Reset.

If both ADCs are in Soft Reset, the clock is no longer distributed to the digital core for low-power operation. Once any of the ADCs is back to normal operation, the clock is automatically distributed again.

However, when the two channels are in Soft Reset, the input structure is still clocking if MCLK is applied to properly bias the inputs so that no leakage current is observed. If MCLK is not applied, large analog input leakage currents can be observed for highly negative input voltages (typically below -0.6V, referred to A_{GND}).

4.20 Hard Reset Mode ($\overline{RESET}$ = D_{GND})

This mode is only available during a POR or when the $\overline{RESET}$ pin is pulled low. The $\overline{RESET}$ pin low state places the device in a Hard Reset mode.

In this mode, all internal registers are reset to their default state.

The DC biases for the analog blocks are still active (i.e., the MCP3911 is ready to convert). However, this pin clears all conversion data in the ADCs. In this mode, the MDAT outputs are in high-impedance. The comparator's outputs of both ADCs are forced to their Reset state ('0011'). The SINC filters are all reset as well as their double-output buffers. See serial timing for minimum pulse low time in **Section 1.0 "Electrical Characteristics"**.

During a Hard Reset, no communication with the part is possible. The digital interface is maintained in a Reset state.

In this state, to properly bias the input structures of both channels, the MCLK can be applied to the part. If not applied, large analog input leakage currents can be observed for highly negative input signals, and after removing the Reset state, a certain start-up time is necessary to bias the input structure properly. During this delay, the ADC conversions can be inaccurate.

4.21 ADC Shutdown Mode

ADC Shutdown mode is defined as a state where the converters and their biases are off, consuming only leakage current. When the Shutdown bit is reset to '0', the analog biases are enabled, as well as the clock and the digital circuitry. The ADC gives a data ready pulse after the SINC filter settling time has occurred. However, since the analog biases are not completely settled at the beginning of the conversion, the sampling may not be accurate during about 1 ms (corresponding to the settling time of the biasing in worst-case conditions). To ensure the accuracy, the data ready pulse coming within the delay of 1 ms + settling time of the SINC filter should be discarded.

Each converter can be placed in Shutdown mode independently. The CONFIG registers are not modified by the Shutdown mode. This mode is only available through the programming of the SHUTDOWN[1:0] bits in the CONFIG register.

The output data are flushed to all zeros while in ADC Shutdown mode. No data ready pulses are generated by any ADC while in ADC Shutdown mode.

ADC Shutdown mode also affects the modulator output block (i.e., if MDAT of the channel in Shutdown mode is enabled, this pin provides a bit stream corresponding to a zero output; series of '0011' bits continuously repeated).

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When an ADC exits ADC Shutdown mode, any phase delay present before shutdown was entered is still present. If one ADC was not in Shutdown mode, the ADC exiting Shutdown mode automatically resynchronizes the phase delay relative to the other ADC channel, per the Phase Delay register block, and gives data ready pulses accordingly.

If an ADC is placed in Shutdown mode while the other is converting, the internal clock is not shut down. When exiting Shutdown mode, the ADC is automatically resynchronized with the clock that did not stop during Reset.

If both ADCs are in Shutdown mode, the clock is no longer distributed to the input structure or to the digital core for low-power operation. If the input voltage is highly negative (typically below -0.6V, referred to A_{GND}), this can cause potential high analog input leakage currents at the analog inputs. Once any of the ADCs is back to normal operation, the clock is automatically distributed again.

4.22 Full Shutdown Mode

The lowest power consumption can be achieved when SHUTDOWN[1:0] = 11, VREFEXT = CLKEXT = 1. This mode is called Full Shutdown mode and no analog circuitry is enabled. In this mode, both AV_{DD} and DV_{DD} POR monitoring are also disabled. No clock is propagated throughout the chip. Both ADCs are in shutdown, and the internal voltage reference is disabled.

The clock is not distributed to the input structure any longer. This can cause potential high analog input leakage currents at the analog inputs if the input voltage is highly negative (typically below -0.6V, referred to A_{GND}).

The only circuit that remains active is the SPI interface, but this circuit does not induce any static power consumption. If SCK is Idle, the only current consumption comes from the leakage currents induced by the transistors and is less than 1 µA on each power supply.

This mode can be used to power down the chip completely and avoid power consumption when there are no data to convert at the analog inputs. Any SCK or MCLK edge coming while in this mode induces dynamic power consumption.

Once any of the SHUTDOWN, CLKEXT and VREFEXT bits return to '0', the two POR monitoring blocks are back to operation, and AV_{DD} and DV_{DD} monitoring can take place.

When exiting Full Shutdown mode, the device resets to its default configuration state. The Configuration bits all reset to their default value, and the ADCs reset to their initial state, requiring three DRCLK periods for an initial data ready pulse. Exiting Full Shutdown mode is effectively identical to an internal Reset or returning from a POR condition.

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5.0 DEVICE OVERVIEW

5.1 Analog Inputs (CHn+/-)

The MCP3911 analog inputs can be connected directly to current and voltage transducers (such as shunts, current transformers or Rogowski coils). Each input pin is protected by specialized ESD structures that are certified to pass 4.0 kV HBM and 300V MM contact charge. These structures allow bipolar ±2V continuous voltage, with respect to A_{GND}, to be present at their inputs without the risk of permanent damage.

Both channels have fully differential voltage inputs for better noise performance. The absolute voltage at each pin, relative to A_{GND}, should be maintained in the ±1V range during operation to ensure the specified ADC accuracy. The Common-mode signals should be adapted to respect both the previous conditions and the differential input voltage range. For best performance, the Common-mode signals should be maintained to A_{GND}.

Note: If the analog inputs are held to a potential of -0.6 to -1V for extended periods of time, MCLK must be present inside the device to avoid large leakage currents at the analog inputs. This is true even during the Hard or Soft Reset mode of both ADCs. However, during the Shutdown mode of the two ADCs or POR state, the clock is not distributed inside the circuit. During these states, it is recommended to keep the analog input voltages above -0.6V, referred to A_{GND}, to avoid high analog inputs leakage currents.

5.2 Programmable Gain Amplifiers (PGA)

The two Programmable Gain Amplifiers (PGAs) reside at the front end of each Delta-Sigma ADC. They have two functions: translate the Common-mode of the input from A_{GND} to an internal level between A_{GND} and A_{VDD}, and amplify the input differential signal. The translation of the Common-mode does not change the differential signal, but recenters the Common-mode so that the input signal can be properly amplified.

The PGA block can be used to amplify very low signals, but the differential input range of the Delta-Sigma modulator must not be exceeded. The PGA is controlled by the PGA_CHn[2:0] bits in the GAIN register. Table 5-1 represents the gain settings for the PGA.

TABLE 5-1: PGA CONFIGURATION SETTING

GAIN PGA_CHn[2:0]			Gain (V/V)	Gain (dB)	V_{IN} Range (V)
0	0	0	1	0	±0.6
0	0	1	2	6	±0.3
0	1	0	4	12	±0.15
0	1	1	8	18	±0.075
1	0	0	16	24	±0.0375
1	0	1	32	30	±0.01875

Note: This table is defined with V_{REF} = 1.2V. The two undefined settings, '110' and '111' are G = 1.

5.3 Delta-Sigma Modulator

5.3.1 ARCHITECTURE

Both ADCs are identical in the MCP3911 and they include a proprietary second-order modulator with a multibit five-level DAC architecture (see Figure 5-1). The quantizer is a Flash ADC composed of four comparators with equally spaced thresholds and a thermometer output coding. The proprietary five-level architecture ensures minimum quantization noise at the outputs of the modulators without disturbing linearity or inducing additional distortion. The sampling frequency is DMCLK (typically 1 MHz with MCLK = 4 MHz), so the modulator outputs are refreshed at a DMCLK rate. The modulator outputs are available in the MOD register or serially transferred on each MDAT pin.

Figure 5-1 represents a simplified block diagram of the Delta-Sigma ADC present on MCP3911.

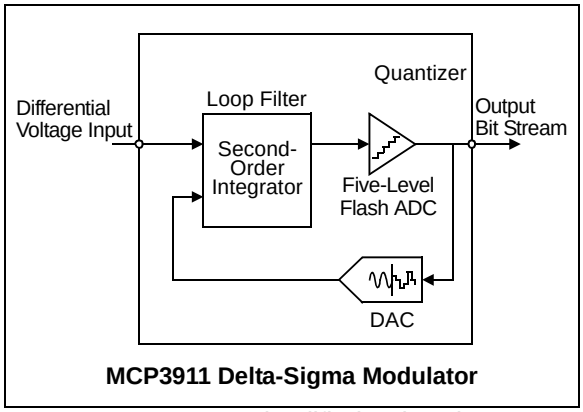


FIGURE 5-1: *Simplified Delta-Sigma ADC Block Diagram.*

5.3.2 MODULATOR INPUT RANGE AND SATURATION POINT

For a specified voltage reference value of 1.2V, the modulator's specified differential input range is ±600 mV. The input range is proportional to V_{REF} and scales according to the V_{REF} voltage. This range is ensuring the stability of the modulator over amplitude and frequency. Outside of this range, the modulator is still functional. However, its stability is no longer ensured and therefore, it is not recommended to exceed this limit. See Figure 2-24 for extended dynamic range performance limitations. The saturation point for the modulator is V_{REF}/1.5, since the transfer function of the ADC includes a gain of 1.5 by default (independent from the PGA setting). See **Section 5.6 "ADC Output Coding"**.

5.3.3 BOOST SETTINGS

The Delta-Sigma modulators include a programmable biasing circuit to further adjust the power consumption to the sampling speed applied through the MCLK. This can be programmed through the BOOST[1:0] bits, which are applied to both channels simultaneously.

The maximum achievable Analog Master Clock (AMCLK) speed and the maximum sampling frequency (DMCLK), and therefore, the maximum achievable data rate (DRCLK), highly depend on BOOST[1:0] and PGA_CHn[2:0] settings. Table 5-2 specifies the maximum AMCLK possible to keep optimal accuracy in function of the BOOST[1:0] and PGA_CHn[2:0] settings.

TABLE 5-2: MAXIMUM AMCLK LIMITS AS A FUNCTION OF BOOST AND PGA GAIN

Conditions		V_{DD} = 3.0V to 3.6V, T_A from -40°C to +125°C		V_{DD} = 2.7V to 3.6V, T_A from -40°C to +125°C	
Boost	Gain	Maximum AMCLK (MHz) (SINAD within -3 dB from its maximum)	Maximum AMCLK (MHz) (SINAD within -5 dB from its maximum)	Maximum AMCLK (MHz) (SINAD within -3 dB from its maximum)	Maximum AMCLK (MHz) (SINAD within -5 dB from its maximum)
0.5x	1	3	3	3	3
0.66x	1	4	4	4	4
1x	1	10	10	10	10
2x	1	16	16	16	16
0.5x	2	2.5	3	3	3
0.66x	2	4	4	4	4
1x	2	10	10	10	10
2x	2	14.5	16	13.3	14.5
0.5x	4	2.5	2.5	2.5	2.5
0.66x	4	4	4	4	4
1x	4	10	10	8	10
2x	4	13.3	16	10.7	11.4
0.5x	8	2.5	2.5	2.5	2.5
0.66x	8	4	4	4	4
1x	8	10	11.4	6.7	8
2x	8	10	14.5	8	8
0.5x	16	2	2	2	2
0.66x	16	4	4	4	4
1x	16	10.6	10.6	8	10
2x	16	12.3	16	8	10.7
0.5x	32	2	2	2	2
0.66x	32	4	4	4	4
1x	32	10	11.4	8	10
2x	32	13.3	16	8	10

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5.3.4 AUTO-ZEROING FREQUENCY SETTING (AZ_FREQ)

The MCP3911 modulators include an auto-zeroing algorithm to improve the offset error performance and greatly diminish 1/f noise in the ADC. This algorithm allows the device to reach very high SNR and flattens the noise spectrum at the output of the ADC (see performance graphs in Figure 2-1, Figure 2-2, Figure 2-3 and Figure 2-4). This auto-zeroing algorithm is performed synchronously with the MCLK coming to the device. Its rate can be adjusted throughout by the AZ_FREQ bit in the CONFIG register.

When AZ_FREQ = 0 (default), the auto-zeroing occurs at the slowest rate, which diminishes the 1/f noise while not impacting the THD performance. This mode is recommended for low values of the PGA gain (GAIN = 1x or 2x).

When AZ_FREQ = 1, the auto-zeroing occurs at the fastest rate, which further diminishes the 1/f noise and further improves the SNR, especially at higher gain settings. The THD may be slightly impacted in this mode (see Figure 2-22). This mode is recommended for higher PGA gain settings to improve SNR (gain superior or equal to 4x).

5.3.5 DITHER SETTINGS

Both modulators also include a dithering algorithm that can be enabled through the DITHER[1:0] bits in the Configuration register. This dithering process improves THD and SFDR (for high OSR settings), while increasing slightly the noise floor of the ADCs. For power metering applications and applications that are distortion-sensitive, it is recommended to keep DITHER at maximum settings for the best THD and SFDR performance. In the case of power metering applications, THD and SFDR are critical specifications. Optimizing SNR (noise floor) is not really problematic due to the large averaging factor at the output of the ADCs. Therefore, even for low OSR settings, the dithering algorithm shows a positive impact on the performance of the application.

5.4 Modulator Output Block

If the user wishes to use the modulator output of the device, the appropriate bits to enable the modulator output must be set in the Configuration register.

When the MODOUT[1:0] bits are enabled, the modulator output of the corresponding channel is present at the corresponding MDAT output pin as soon as the command is placed. Additionally, the corresponding SINC filter is disabled to consume less current. The corresponding $\overline{DR}$ pulse is also not present at the $\overline{DR}$ output pin. When MODOUT[1:0] bits are cleared, the corresponding SINC filters are back to normal operation and the corresponding MDAT outputs are in high-impedance.

Since the Delta-Sigma modulators have a five-level output given by the state of four comparators with thermometer coding, their outputs can be represented on four bits, each bit giving the state of the corresponding comparator (see Table 5-3). These bits are present on the MOD register and are updated at the DMCLK rate.

To output the comparator's result on a separate pin (MDAT0 and MDAT1), these comparator output bits have been arranged to be serially output at the AMCLK rate (see Figure 5-2).

This 1-bit serial bit stream is identical to the one produced by a 1-bit DAC modulator with a sampling frequency of AMCLK. The modulator can either operate as a five-level output at DMCLK rate or a 1-bit output at AMCLK rate. These two representations are interchangeable. The MDAT outputs can therefore be used in any application that requires 1-bit modulator outputs. These applications often integrate and filter the 1-bit output with SINC or more complex decimation filters computed by an MCU or DSP.

TABLE 5-3: DELTA-SIGMA MODULATOR CODING

COMP[3:0] Code	Modulator Output Code	MDAT Serial Stream
1111	+2	1111
0111	+1	0111
0011	0	0011
0001	-1	0001
0000	-2	0000

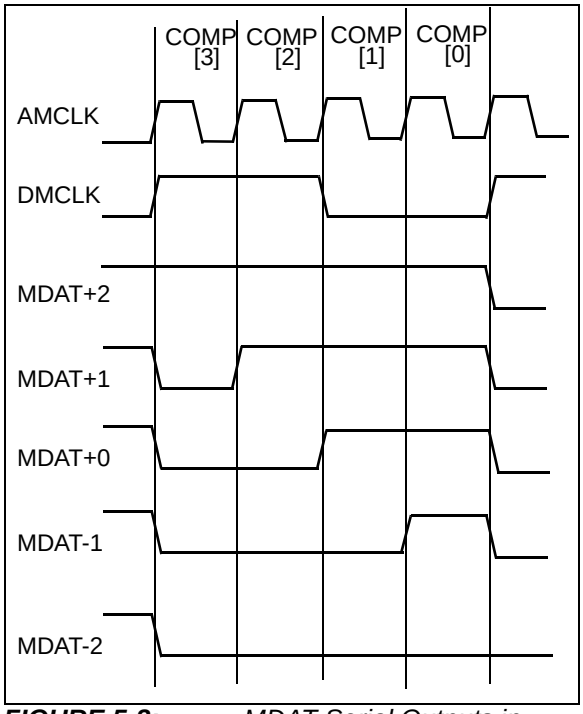


FIGURE 5-2: *MDAT Serial Outputs in Function of the Modulator Output Code.*

Since the Reset and shutdown SPI commands are asynchronous, the MDAT pins are resynchronized with DMCLK after each time the part goes out of Reset and shutdown.

This means that the first output of MDAT, after a Soft Reset or a shutdown, is always '0011' after the first DMCLK rising edge.

The two MDAT output pins are in high-impedance if the $\overline{\text{RESET}}$ pin is low.

5.5 SINC^3 + SINC^1 Filter

The decimation filter present in both channels of the MCP3911 is a cascade of two SINC filters (SINC^3 + SINC^1): a third-order SINC filter with a decimation ratio of OSR_3, followed by a first-order SINC filter with a decimation ratio of OSR_1 (moving average of OSR_1 values). Figure 5-3 represents the decimation filter architecture.

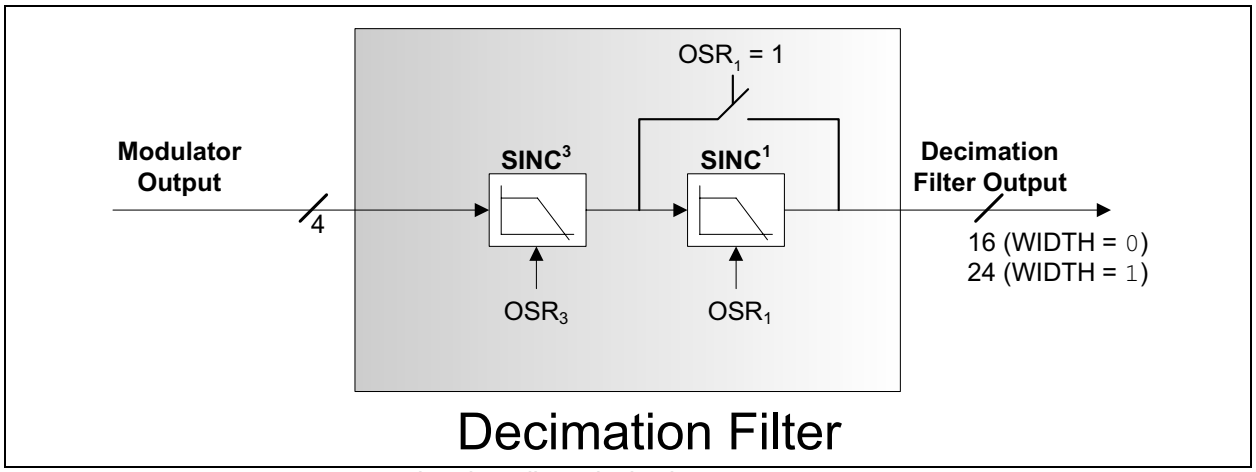


FIGURE 5-3: *MCP3911 Decimation Filter Block Diagram.*

Equation 5-1 contains the formula for calculating the transfer function of the digital decimation filter and settling time of the ADC:

EQUATION 5-1: SINC FILTER TRANSFER FUNCTION

$$H(z) = \frac{\left(1 - z^{-OSR_3}\right)^3}{\left(OSR_3(1 - z^{-1})\right)^3} \times \frac{\left(1 - z^{-OSR_1 \times OSR_3}\right)}{OSR_1 \times \left(1 - z^{-OSR_3}\right)}$$

$$Where \quad z = EXP(2\pi \cdot j \cdot f_{in}/DMCLK)$$

EQUATION 5-2: SETTING TIME OF THE ADC AS A FUNCTION OF DMCLK PERIODS

$$SettlingTime(DMCLKPeriods) = 3 \times OSR_3 + (OSR_1 - 1) \times OSR_3$$

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The SINC^1 filter following the SINC^3 filter is only enabled for the high OSR settings. This SINC^1 filter provides additional rejection at a low cost with little modification to the -3 dB bandwidth. For 24-Bit Output mode (WIDTH = 1), the output of the SINC filter is padded on the right with least significant zeros, up to 24 bits, for any resolution less than 24 bits. For 16-Bit Output modes, the output of the SINC filter is rounded to the closest 16-bit number to conserve only 16-bit words and to minimize truncation error.

The gain of the transfer function of this filter is one at each multiple of DMCLK (typically 1 MHz), so a proper anti-aliasing filter must be placed at the inputs. This attenuates the frequency content around DMCLK and keeps the desired accuracy over the baseband of the converter. This anti-aliasing filter can be a simple, first-order RC network with a sufficiently low time constant to generate high rejection at DMCLK frequency.

Any unsettled data are automatically discarded to avoid data corruption. Each data ready pulse corresponds to fully settled data at the output of the decimation filter. The first data available at the output of the decimation filter are present after the complete settling time of the filter (see Table 5-4). After the first data have been processed, the delay between two data ready pulses is 1/DRCLK. The data stream, from input to output, is delayed by an amount equal to the settling time of the filter (which is the group delay of the filter).

The achievable resolution, the -3 dB bandwidth and the settling time at the output of the decimation filter (the output of the ADC), is dependent on the OSR of each SINC filter and is summarized in Table 5-4:

TABLE 5-4: OVERSAMPLING RATIO AND SINC FILTER SETTLING TIME

OSR[2:0]			OSR_3	OSR_1	Total OSR	Resolution In Bits (No Missing Codes)	Settling Time	-3 dB Bandwidth
0	0	0	32	1	32	17	96/DMCLK	0.26 * DRCLK
0	0	1	64	1	64	20	192/DMCLK	0.26 * DRCLK
0	1	0	128	1	128	23	384/DMCLK	0.26 * DRCLK
0	1	1	256	1	256	24	768/DMCLK	0.26 * DRCLK
1	0	0	512	1	512	24	1536/DMCLK	0.26 * DRCLK
1	0	1	512	2	1024	24	2048/DMCLK	0.37 * DRCLK
1	1	0	512	4	2048	24	3072/DMCLK	0.42 * DRCLK
1	1	1	512	8	4096	24	5120/DMCLK	0.43 * DRCLK

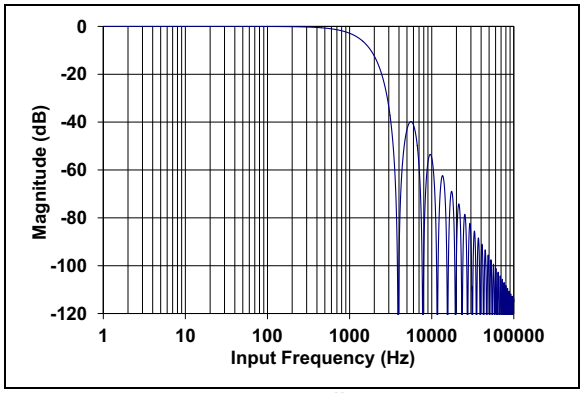


FIGURE 5-4: *SINC Filter Frequency Response, OSR = 256, MCLK = 4 MHz, PRE[1:0] = 00.*

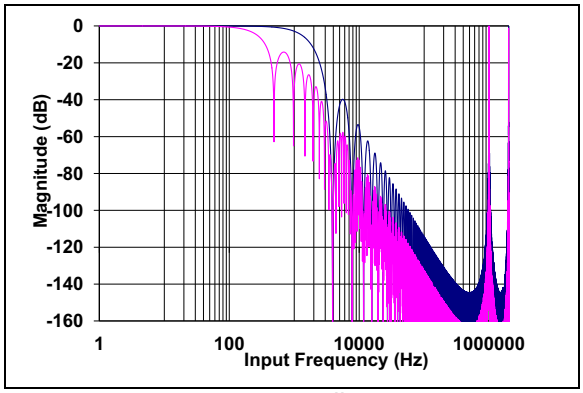


FIGURE 5-5: *SINC Filter Frequency Response, OSR = 4096 (pink), OSR = 512 (blue), MCLK = 4 MHz, PRE[1:0] = 00.*

5.6 ADC Output Coding

The second-order modulator, SINC^3 + SINC^1 filter, PGA, V_{REF} and analog input structure, all work together to produce the device transfer function for the Analog-to-Digital conversion (see Equation 5-3).

The channel data are either a 16-bit or 24-bit word, presented in 23-bit or 15-bit plus sign, two's complement format and are Most Significant Byte (MSB) (left) justified.

The ADC data are two or three bytes wide depending on the WIDTH[1:0] bits. The 16-bit mode includes a round to the closest 16-bit word (instead of truncation) to improve the accuracy of the ADC data.

In case of positive saturation (CHn+ – CHn- > V_{REF}/1.5), the output is locked to 7FFFFF for 24-bit mode (7FFF for 16-bit mode). In case of negative saturation (CHn+ – CHn- < -V_{REF}/1.5), the output code is locked to 800000 for 24-bit mode (8000 for 16-bit mode).

Equation 5-3 is only true for DC inputs. For AC inputs, this transfer function needs to be multiplied by the transfer function of the SINC^3 + SINC^1 filter (see Equation 5-1 and Equation 5-3).

EQUATION 5-3:

$$DATA_CHn = \left(\frac{(CHn+ - CHn-)}{V_{REF}+ - V_{REF}-}\right) \times 8{,}388{,}608 \times G \times 1.5$$

For 24-Bit Mode or WIDTH = 1

$$DATA_CHn = \left(\frac{(CHn+ - CHn-)}{V_{REF}+ - V_{REF}-}\right) \times 32{,}768 \times G \times 1.5$$

For 16-Bit Mode or WIDTH = 0

The ADC resolution is a function of the OSR (**Section 5.5 "SINC^3 + SINC^1 Filter"**). The resolution is the same for both channels. No matter what the resolution is, the ADC output data are always presented in 24-bit words, with added zeros at the end, if the OSR is not large enough to produce 24-bit resolution (left justification).

TABLE 5-5: OSR = 256 (AND HIGHER) OUTPUT CODE EXAMPLES

ADC Output Code (MSB First)	Hexadecimal	Decimal 24-Bit Resolution
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0x7FFFFF	+ 8,388,607
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	0x7FFFFE	+ 8,388,606
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x000000	0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0xFFFFFF	– 1
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	0x800001	– 8,388,607
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x800000	– 8,388,608

TABLE 5-6: OSR = 128 OUTPUT CODE EXAMPLES

ADC Output Code (MSB First)	Hexadecimal	Decimal 23-Bit Resolution
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	0x7FFFFE	+ 4,194,303
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0	0x7FFFFC	+ 4,194,302
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x000000	0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	0xFFFFFE	– 1
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0	0x800002	– 4,194,303
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x800000	– 4,194,304

TABLE 5-7: OSR = 64 OUTPUT CODE EXAMPLES

ADC Output Code (MSB First)	Hexadecimal	Decimal 20-Bit Resolution
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0	0x7FFFF0	+ 524, 287
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0	0x7FFFE0	+ 524, 286
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x000000	0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0	0xFFFFF0	– 1
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0	0x800010	– 524, 287
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x800000	– 524, 288

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TABLE 5-8: OSR = 32 OUTPUT CODE EXAMPLES

ADC Output Code (MSB First)	Hexadecimal	Decimal 17-Bit Resolution
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0	0x7FFF80	+ 65, 535
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0	0x7FFF00	+ 65, 534
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x000000	0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0	0xFFFF80	– 1
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0	0x800080	– 65, 535
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x800000	– 65, 536

5.7 Voltage Reference

5.7.1 INTERNAL VOLTAGE REFERENCE

The MCP3911 contains an internal voltage reference source specially designed to minimize drift over-temperature. To enable the internal voltage reference, the VREFEXT bit in the Configuration register must be set to '0' (Default mode). This internal V_{REF} supplies reference voltage to both channels. The typical value of this voltage reference is 1.2V ±2%. The internal reference has a very low typical temperature coefficient of ±7 ppm/°C, allowing the output to have minimal variation with respect to temperature, since it is proportional to ($1/V_{REF}$).

The noise of the internal voltage reference is low enough not to significantly degrade the SNR of the ADC if compared to a precision external low noise voltage reference. The output pin for the internal voltage reference is REFIN+/OUT.

If the voltage reference is only used as an internal V_{REF}, adding bypass capacitance on REFIN+/OUT is not necessary for keeping ADC accuracy. A minimal 0.1 µF ceramic capacitance can be connected to avoid EMI/EMC susceptibility issues due to the antenna created by the REFIN+/OUT pin if left floating.

The bypass capacitors also help applications where the voltage reference output is connected to other circuits. In this case, additional buffering may be needed as the output drive capability of this output is low.

Adding too much capacitance on the REFIN+/OUT pin may slightly degrade the THD performance of the ADCs.

5.7.2 DIFFERENTIAL EXTERNAL VOLTAGE INPUTS

When the VREFEXT bit is high, the two reference pins (REFIN+/OUT, REFIN-) become a differential voltage reference input. The internal voltage reference circuit is placed into Shutdown mode and the switch connecting this circuit to the reference voltage input of the ADC is opened. The internal voltage reference circuit is placed into Shutdown mode and the switch connecting this circuit to the reference voltage input of the ADC is opened. The voltage at the REFIN+/OUT is noted $V_{REF}+$ and the voltage at the REFIN- pin is noted $V_{REF}-$. The differential voltage input value is given by the following equation:

EQUATION 5-4:

$$V_{REF} = V_{REF}+ - V_{REF}-$$

The specified V_{REF} range is from 1.1V to 1.3V. The REFIN- pin voltage ($V_{REF}-$) should be limited to ±0.1V, with respect to A_{GND}. Typically, for single-ended reference applications, the REFIN- pin should be directly connected to A_{GND}, with its own separate track, to avoid any spike due to switching noise.

5.7.3 TEMPERATURE COMPENSATION (VREFCAL REGISTER)

The internal voltage reference comprises a proprietary circuit and algorithm to compensate first-order and second-order temperature coefficients. The compensation allows very low temperature coefficients (typically 7 ppm/°C) on the entire range of temperatures, from -40°C to +125°C. This temperature coefficient varies from part to part.

This temperature coefficient can be adjusted on each part through the VREFCAL register (address 0x1A). This register is only for advanced users. This register should not be written unless the user wants to calibrate the temperature coefficient of the whole system or application. The default value of this register is set to 0x42. The typical variation of the temperature coefficient of the internal voltage reference, with respect to VREFCAL register code, is shown in Figure 5-6. Modifying the value stored in the VREFCAL register may also vary the output voltage in addition to the temperature coefficient.

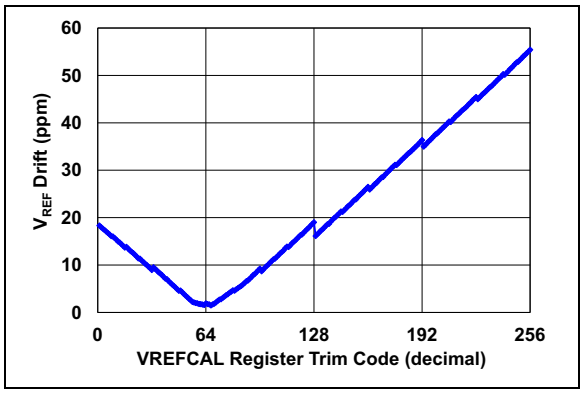


FIGURE 5-6: *V_{REF} Tempco vs. VREFCAL Trim Code Chart.*

5.8 Power-on Reset

The MCP3911 contains an internal POR circuit that monitors both analog and digital supply voltages during operation. The typical threshold for a power-up event detection is 2.1V ±5% and a typical start-up time (t_{POR}) of 50 µs. The POR circuit has a built-in hysteresis for improved transient spike immunity that has a typical value of 200 mV. Proper decoupling capacitors (0.1 µF ceramic and 10 µF in parallel are sufficient in most cases) should be mounted as close as possible to the AV_{DD} and DV_{DD} pins, providing additional transient immunity.

Figure 5-7 illustrates the different conditions at power-up and a power-down event in typical conditions. All internal DC biases are not settled until at least 1 ms, in worst-case conditions, after a system POR. Any data ready pulse that occurs within 1 ms, plus the SINC filter settling time after system Reset, should be ignored to ensure proper accuracy. After POR, data ready pulses are present at the pin with all the default conditions in the Configuration registers.

Both AV_{DD} and DV_{DD} are monitored so either power supply can sequence first.

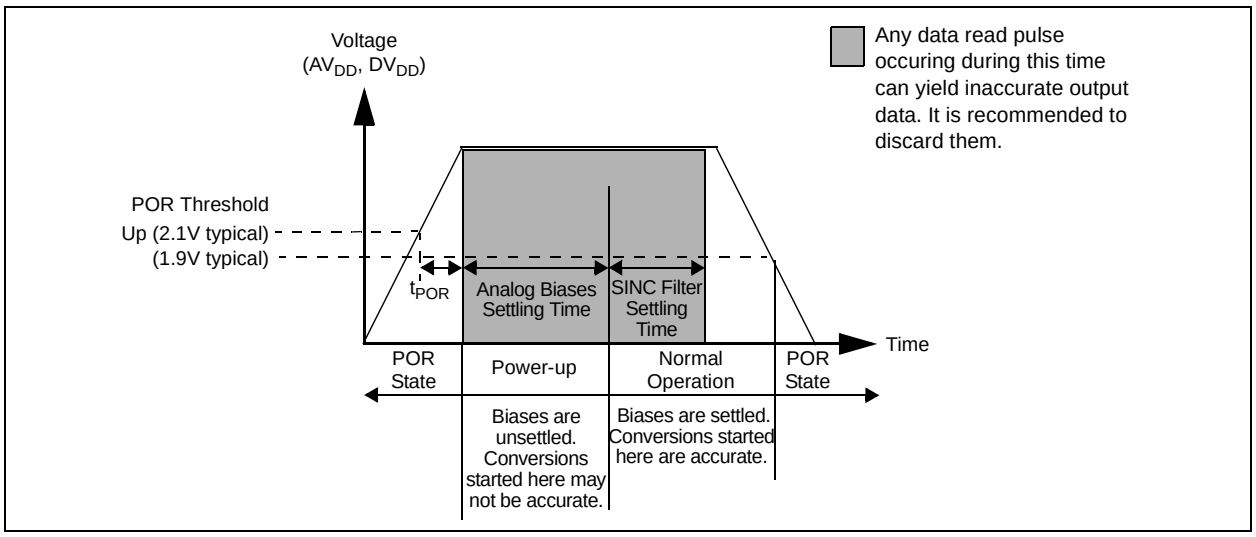


FIGURE 5-7: *Power-on Reset Operation.*

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5.9 $\overline{\text{RESET}}$ Effect On Delta-Sigma Modulator/SINC Filter

When the $\overline{\text{RESET}}$ pin is logic low, both ADCs are in Reset mode and output code 0x0000h. The $\overline{\text{RESET}}$ pin performs a Hard Reset (DC biases still on, part ready to convert) and clears all charges contained in the Delta-Sigma modulators. The comparator's output is '0011' for each ADC.

The SINC filters are all reset, as well as their double-output buffers. This pin is independent of the serial interface. It brings all the registers to the default state. When $\overline{\text{RESET}}$ is logic low, any write with the SPI interface is disabled and has no effect. All output pins (SDO, $\overline{\text{DR}}$, MDAT0/1) are high-impedance.

If MCLK is applied, the input structure is enabled and is properly biasing the substrate of the input transistors. If the analog inputs are between -1V and +1V, the leakage current on the analog inputs is low.

If MCLK is not applied when in Reset mode, the leakage can be high if the analog inputs are below -0.6V, referred to A_{GND}.

5.10 Phase Delay Block

The MCP3911 incorporates a phase delay generator, which ensures that the two ADCs are converting the inputs with a fixed delay between them. The two ADCs are synchronously sampling, but the averaging of modulator outputs is delayed, so that the SINC filter outputs (thus, the ADC outputs) show a fixed phase delay as determined by the PHASE register's setting.

The phase value (PHASE[11:0]) is an 11 bit + sign, MSB first, two's complement code that indicates how much phase delay there is to be between Channel 0 and Channel 1. The four MSBs of the first PHASE register (address 0x07) are undefined and set to '0'. The reference channel for the delay is Channel 1 (typically, the voltage channel for power metering applications). When the PHASE[11:0] bits are positive, Channel 0 is lagging versus Channel 1. When PHASE[11:0] are negative, Channel 0 is leading versus Channel 1. The amount of delay between two ADC conversions is shown in Equation 5-5.

EQUATION 5-5:

$$Delay = \frac{Phase\ Register\ Code}{DMCLK}$$

The timing resolution of the phase delay is 1/DMCLK or 1 µs in the default configuration with MCLK = 4 MHz.

The data ready signals are affected by the phase delay settings. Typically, the time difference between the data ready pulses of Channel 0 and Channel 1 are equal to the phase delay setting.

Note: A detailed explanation of the Data Ready pin ($\overline{\text{DR}}$) with phase delay is shown in Figure 6-9.

5.10.1 PHASE DELAY LIMITS

The phase delay can only go from -OSR/2 to +OSR/2 – 1. This sets the fine phase resolution. The PHASE register is coded with two's complement.

If larger delays between the two channels are needed, they can be implemented externally to the chip with an MCU. A First-In, First-Out algorithm (FIFO) in the MCU can save incoming data from the leading channel for a number N of DRCLK. In this case, DRCLK represents the coarse timing resolution and DMCLK represents the fine timing resolution. The total delay is shown in Equation 5-6.

EQUATION 5-6:

$$Delay = N/DRCLK + PHASE/DMCLK$$

The PHASE register can be programmed once with the OSR = 4096 setting, and adjusts to the OSR automatically afterwards, without the need to change the value of the PHASE register.

Note: Rewriting the PHASE registers with the same value resets and automatically restarts both ADCs.

- **OSR = 4096:** The delay can go from -2048 to +2047. PHASE[11] is the sign bit. Phase[10] is the MSB and PHASE[0] the LSB.
- **OSR = 2048:** The delay can go from -1024 to +1023. PHASE[10] is the sign bit. Phase[9] is the MSB and PHASE[0] the LSB.
- **OSR = 1024:** The delay can go from -512 to +511. PHASE[9] is the sign bit. Phase[8] is the MSB and PHASE[0] the LSB.
- **OSR = 512:** The delay can go from -256 to +255. PHASE[8] is the sign bit. Phase[7] is the MSB and PHASE[0] the LSB.
- **OSR = 256:** The delay can go from -128 to +127. PHASE[7] is the sign bit. Phase[6] is the MSB and PHASE[0] the LSB.
- **OSR = 128:** The delay can go from -64 to +63. PHASE[6] is the sign bit. Phase[5] is the MSB and PHASE[0] the LSB.
- **OSR = 64:** The delay can go from -32 to +31. PHASE[5] is the sign bit. Phase[4] is the MSB and PHASE[0] the LSB.
- **OSR = 32:** The delay can go from -16 to +15. PHASE[4] is the sign bit. Phase[3] is the MSB and PHASE[0] the LSB.

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TABLE 5-9: PHASE VALUES WITH MCLK = 4 MHz, OSR = 4096

Phase Register Value												Hex	Delay (CH0 relative to CH1)
0	1	1	1	1	1	1	1	1	1	1	1	0x7FF	+ 2047 µs
0	1	1	1	1	1	1	1	1	1	1	0	0x7FE	+ 2046 µs
0	0	0	0	0	0	0	0	0	0	0	1	0x001	+ 1 µs
0	0	0	0	0	0	0	0	0	0	0	0	0x000	0 µs
1	1	1	1	1	1	1	1	1	1	1	1	0xFFF	– 1 µs
1	0	0	0	0	0	0	0	0	0	0	1	0x801	– 2047 µs
1	0	0	0	0	0	0	0	0	0	0	0	0x800	– 2048 µs

5.11 Crystal Oscillator

The MCP3911 includes a Pierce-type crystal oscillator with very high stability, and ensures very low tempco and jitter for the clock generation. This oscillator can handle up to 20 MHz crystal frequencies provided that proper load capacitances and quartz quality factor are used.

For a proper start-up, the load capacitors of the crystal should be connected between OSC1 and D_{GND}, and between OSC2 and D_{GND}. They should also respect the following equation:

EQUATION 5-7:

$$R_M < 1.6 \times 10^6 \times \left(\frac{1}{f \bullet C_{LOAD}}\right)^2$$

Where:

f = Crystal frequency in MHz

C_{LOAD} = Load capacitance in pF including parasitics from the PCB

R_M = Motional resistance in ohms of the quartz

When CLKEXT = 1, the crystal oscillator is bypassed by a digital buffer to allow a direct clock input for an external clock (see Figure 4-1).

When CLKEXT = 1, it is recommended to connect the OSC2 pin to D_{GND} directly at all times. The external clock should not be higher than 20 MHz before the prescaler (MCLK < 20 MHz) for proper operation.

Note: In addition to the conditions defining the maximum MCLK input frequency range, the AMCLK frequency should be maintained inferior to the maximum limits defined in Table 5-2 to ensure the accuracy of the ADCs. If these limits are exceeded, it is recommended to either choose a larger OSR or a large prescaler value, so that AMCLK can respect these limits.

5.12 Digital System Offset and Gain Errors

The MCP3911 incorporates two sets of additional registers per channel to perform system digital offset and gain error calibration. If the calibration is enabled, each channel has its own set of associated registers that will modify the output result of the channel. The gain and offset calibrations can be enabled or disabled through two Configuration bits (EN_OFFCAL and EN_GAINCAL). These two bits enable or disable system calibration on both channels at the same time. When both calibrations are enabled, the output of the ADC is modified as in Equation 5-8.

EQUATION 5-8: DIGITAL OFFSET AND GAIN ERROR CALIBRATION REGISTERS CALCULATIONS

$$DATA_CHn(post-cal) = (DATA_CHn(pre-cal) + OFFCAL_CHn) \times (1 + GAINCAL_CHn)$$

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5.12.1 DIGITAL OFFSET ERROR CALIBRATION

The OFFCAL_CHn registers are 23-bit plus sign two's complement register, whose LSB value is the same as the channel ADC data. These two registers are then added bit-by-bit to the ADC output codes if the EN_OFFCAL bit is enabled. Enabling the EN_OFFCAL bit does not create any pipeline delay; the offset addition is instantaneous. For low OSR values, only the significant digits are added to the output (up to the resolution of the ADC). For example, at OSR = 32, only the 17 first bits are added).

The offset is not added when the corresponding channel is in Reset or Shutdown mode. The corresponding input voltage offset value added by each LSB in these 24-bit registers is shown in Equation 5-9.

EQUATION 5-9:

$$OFFSET(1LSB) = V_{REF}/(PGA_CHn \times 1.5 \times 8388608)$$

This register is a "Don't Care" if EN_OFFCAL = 0 (offset calibration disabled), but its value is not cleared by the EN_OFFCAL bit.

5.12.2 DIGITAL GAIN ERROR CALIBRATION

This register is 24-bit signed MSB first coding with a range of -1x to +0.9999999x (from 0x80000 to 0x7FFFFF). The gain calibration adds 1x to this register and multiplies it to the output code of the channel, bit-by-bit, after offset calibration. The range of the gain calibration is thus from 0x to 1.9999999x (from 0x80000 to 0x7FFFFF). The LSB corresponds to a 2^{-23} increment in the multiplier.

Enabling EN_GAINCAL creates a pipeline delay of 24 DMCLK periods on both channels. All data ready pulses are delayed by 24 DMCLK periods, starting from the data ready, following the command enabling the EN_GAINCAL bit. The gain calibration is effective on the next data ready, following the command enabling the EN_GAINCAL bit.

The digital gain calibration does not function when the corresponding channel is in Reset or Shutdown mode. The gain multiplier value for an LSB in these 24-bit registers is shown in Equation 5-10.

EQUATION 5-10:

$$GAIN\ (1LSB) = 1/8388608$$

This register is a "Don't Care" if EN_GAINCAL = 0 (offset calibration disabled), but its value is not cleared by the EN_GAINCAL bit.

If the output result is out of bounds after all calibrations are performed, the output data on the channel are kept to either 7FFF or 8000 in 16-bit mode, or 7FFFFF or 8000 in 24-bit mode.

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NOTES:

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6.0 SERIAL INTERFACE DESCRIPTION

6.1 Overview

The MCP3911 device is compatible with SPI Modes 0,0 and 1,1. Data are clocked out of the MCP3911 on the falling edge of SCK and data are clocked into the MCP3911 on the rising edge of SCK. In these modes, SCK can Idle either high or low.

Each SPI communication starts with a $\overline{CS}$ falling edge and stops with the $\overline{CS}$ rising edge. Each SPI communication is independent. When $\overline{CS}$ is high, SDO is in high-impedance, and transitions on SCK and SDI have no effect. Additional control pins, $\overline{RESET}$, $\overline{DR}$ and MDAT0/1, are also provided on separate pins for advanced communication.

The MCP3911 interface has a simple command structure. The first byte transmitted is always the control byte and is followed by data bytes that are eight bits wide. Both ADCs are continuously converting data by default and can be reset or shut down through a CONFIG register setting.

Since each ADC data are either 16 or 24 bits (depending on the WIDTH bits), the internal registers can be grouped together with various configurations (through the READ bits) to allow easy data retrieval within only one communication. For device reads, the internal address counter can be automatically incremented to loop through groups of data within the register map. The SDO then outputs the data located at the ADDRESS (A[4:0]) defined in the control byte and then ADDRESS + 1, depending on the READ[1:0] bits, which select the groups of registers. These groups are defined in **Section 7.1 "CHANNEL Registers – ADC Channel Data Output Registers"** (Register Map).

The Data Ready pin ($\overline{DR}$) can be used as an interrupt for an MCU and outputs pulses when new ADC channel data are available. The $\overline{RESET}$ pin acts like a Hard Reset and can reset the part to its default power-up configuration. The MDAT0/1 pins give the modulator outputs (see **Section 5.4 "Modulator Output Block"**).

6.2 Control Byte

The control byte of the MCP3911 contains two device Address bits (A[6:5]), five register Address bits (A[4:0]) and a Read/Write bit (R/$\overline{W}$). The first byte transmitted to the MCP3911 is always the control byte.

The MCP3911 interface is device-addressable (through A[6:5]), so that multiple MCP3911 chips can be present on the same SPI bus with no data bus contention. This functionality enables three-phase power metering systems, containing three MCP3911 chips, controlled by a single SPI bus (single $\overline{CS}$, SCK, SDI and SDO pins).

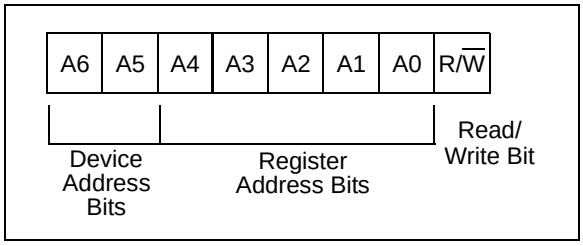


FIGURE 6-1: *Control Byte.*

The default device address bits are '00'. Contact the Microchip factory for additional device address bits. For more information, please see the **Product Identification System** section.

A read on undefined addresses gives an all zeros output on the first and all subsequent transmitted bytes. A write on an undefined address has no effect and does not increment the address counter.

The register map is defined in Table 7-1.

6.3 Reading from the Device

The first data byte read is the one defined by the address given in the control byte. If the CS pin is maintained low after this first byte is transmitted, the communication continues and the address of the next transmitted byte is determined by the status of the READ[1:0] bits in the STATUSCOM register. Multiple looping configurations can be defined through the READ[1:0] bits for the address increment (see **Section 6.7 "Continuous Communication, Looping on Address Sets"**).

6.4 Writing to the Device

The first data byte written is the one defined by the address given in the control byte. Two Write mode configurations for the address increment can be defined through the WRITE bit in the STATUSCOM register. When WRITE = 1, the write communication automatically increments the address for subsequent bytes. The address of the next transmitted byte within the same communication ($\overline{CS}$ stays logic low) is the next address defined on the register map. At the end of the register map, the address loops to the beginning of the writable part of the register map (address 0x06). Writing a non-writable register has no effect. When WRITE = 0, the address is not incremented on the subsequent writes.

The SDO pin stays in high-impedance during a write communication.

6.5 SPI MODE 1,1 – Clock Idle High, Read/Write Examples

In this SPI mode, SCK Idles high. For the MCP3911, this means that there is a falling edge on SCK before there is a rising edge.

Note:	Changing from an SPI Mode 1,1 to an SPI Mode 0,0 is possible and can be done while the $\overline{CS}$ pin is logic high.

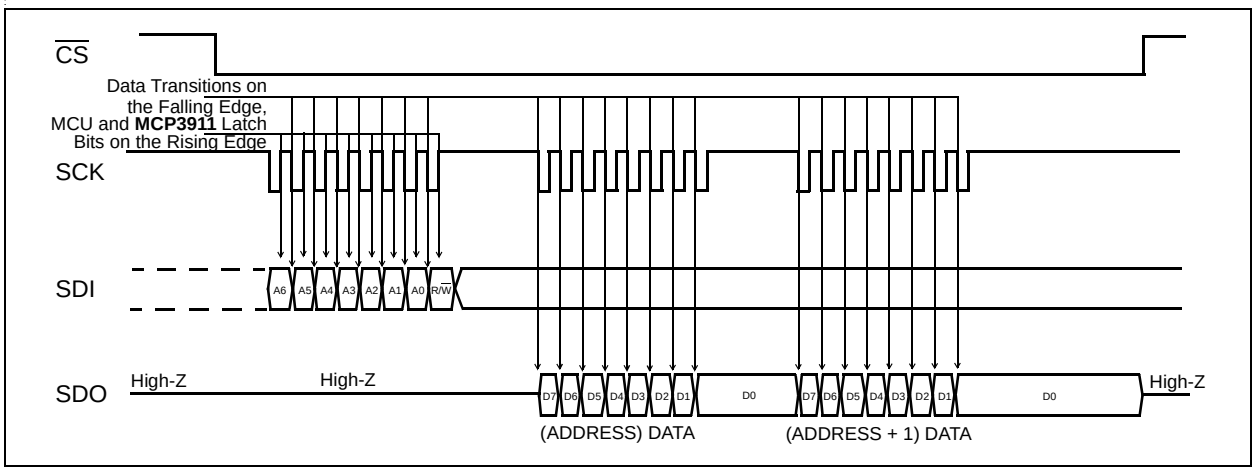


FIGURE 6-2: *Device Read (SPI Mode 1,1 – SCK Idles High).*

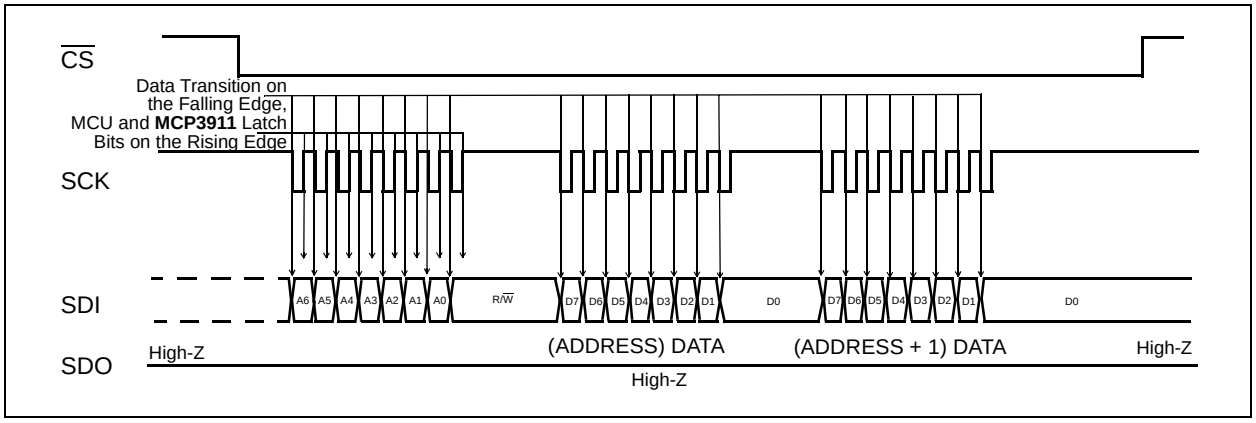


FIGURE 6-3: *Device Write (SPI Mode 1,1 – SCK Idles High).*

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6.6 SPI MODE 0,0 – Clock Idle Low, Read/Write Examples

In this SPI mode, SCK Idles low. For the MCP3911, this means that there is a rising edge on SCK before there is a falling edge.

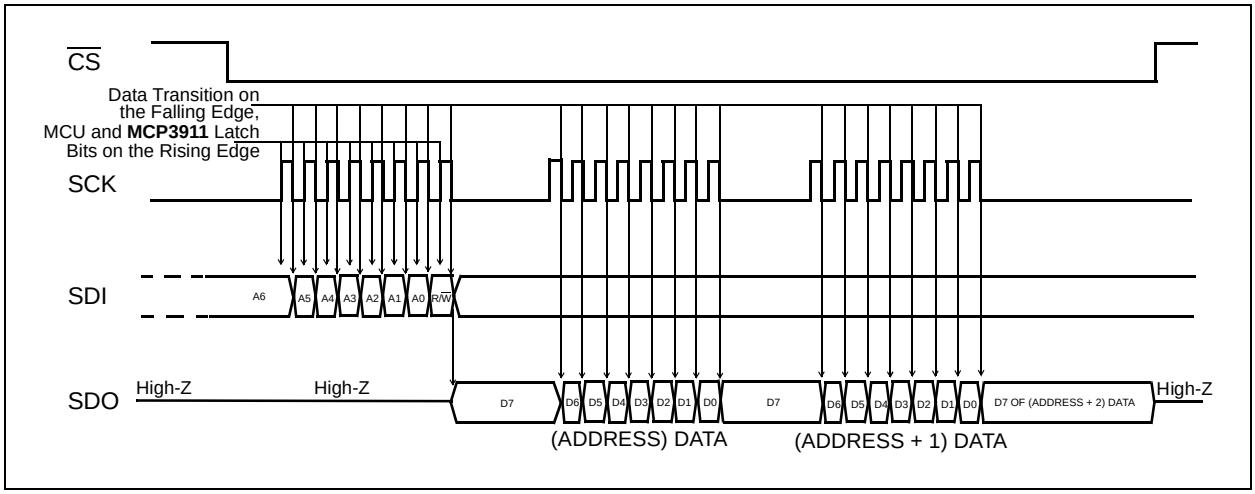


FIGURE 6-4: *Device Read (SPI Mode 0,0 – SCK Idles Low).*

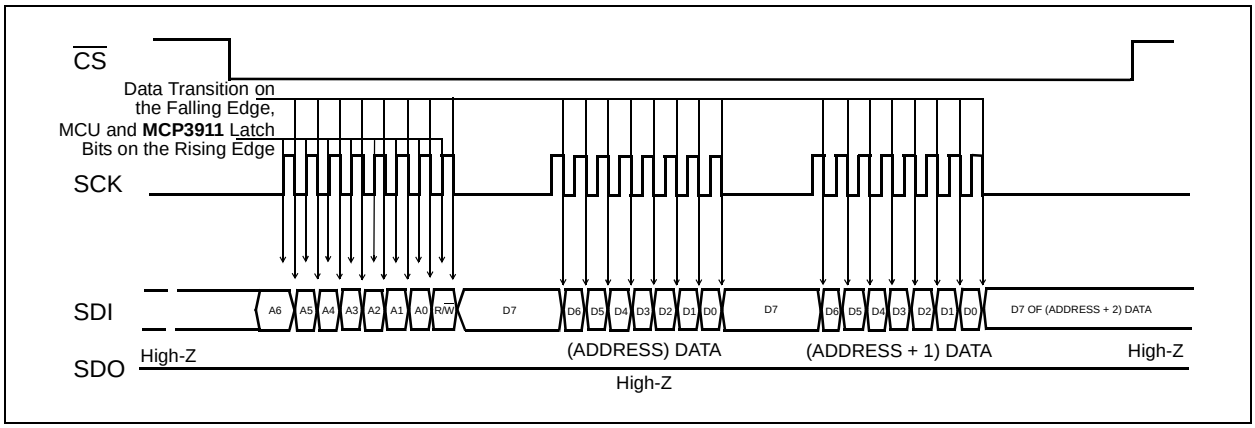


FIGURE 6-5: *Device Write (SPI Mode 0,0 – SCK Idles Low).*

6.7 Continuous Communication, Looping on Address Sets

If the user wishes to read back one or both ADC channels continuously, the internal address counter of the MCP3911 can be set to loop on specific register sets. In this case, there is only one control byte on SDI to start the communication. The part stays within the same loop until the $\overline{CS}$ pin returns logic high.

This internal address counter allows the following functionality:

- Read one ADC channel data continuously
- Read both ADC channels data continuously (both ADC data can be independent or linked with DRMODE settings)
- Continuously read/write the entire register map
- Continuously read/write each separate register
- Continuously read all Configuration registers
- Write all Configuration registers in one communication (see Figure 6-8)

6.7.1 CONTINUOUS READ

The STATUSCOM register contains the loop settings for the internal address counter (READ[1:0] bits and WRITE bit). The internal address counter can either stay constant (READ[1:0] = 00) and continuously read the same byte or it can auto-increment and loop through the register groups defined below (READ[1:0] = 01), register types (READ[1:0] = 10) or the entire register map (READ[1:0] = 11).

The WIDTH[1:0] bits determine three possible configurations for the channel output format:

- WIDTH[1:0] = 11 – Both channels have 24-bit format
- WIDTH[1:0] = 01 or 10 – CH1 has 16-bit format (typically voltage channel), CH0 has 24-bit format (typically current channel)
- WIDTH[0:0] = 00 – Both channels have 16-bit format

In the case of WIDTH = 0 (16-bit), the lower byte of the ADC data is not accessed and the part jumps automatically to the following address (the user does not have to clock out the lower byte since it becomes undefined for WIDTH = 0).

Figure 6-6 and Figure 6-7 represent a typical, continuous read communication with the default settings (DRMODE[1:0] = 00, READ[1:0] = 10) for both WIDTH settings in the case of the SPI Mode 0,0 (see Figure 6-6) and SPI Mode 1,1 (see Figure 6-7). This configuration is typically used for power metering applications.

Note: For continuous reading of ADC data in SPI Mode 0,0 (see Figure 6-6), once the data have been completely read after a data ready, the SDO pin takes the MSB value of the previous data at the end of the reading (falling edge of the last SCK clock). If SCK stays Idle at logic low (by definition of Mode 0,0), the SDO pin is updated at the falling edge of the next data ready pulse (synchronously with the $\overline{DR}$ pin falling edge with an output timing of t_{DODR}) with the new MSB of the data corresponding to the data ready pulse. This mechanism allows the MCP3911 to continuously use Read mode seamlessly in SPI Mode 0,0. In SPI Mode 1,1, the SDO stays in the last state (LSB of previous data) after a complete reading, which also allows seamless continuous Read mode (see Figure 6-7).

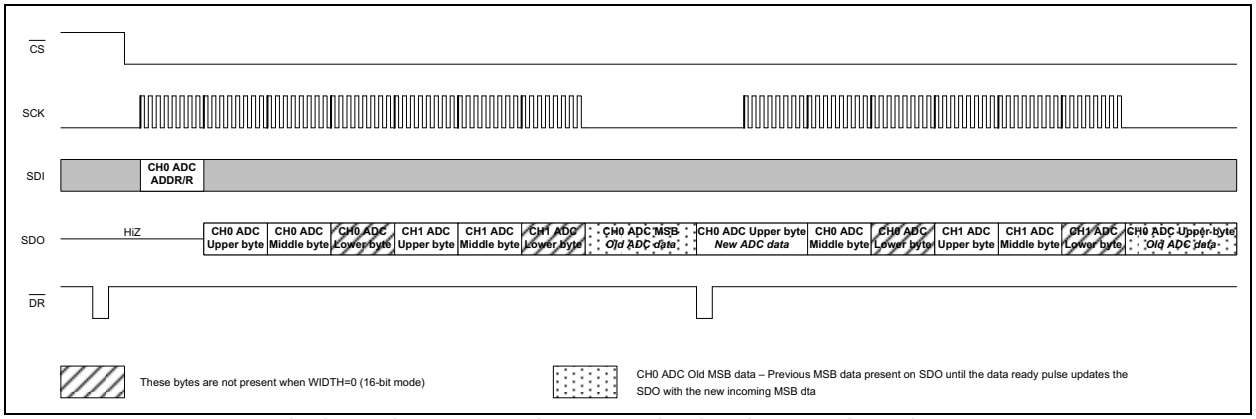


FIGURE 6-6: *Typical Continuous Read Communication (SPI Mode 0,0).*

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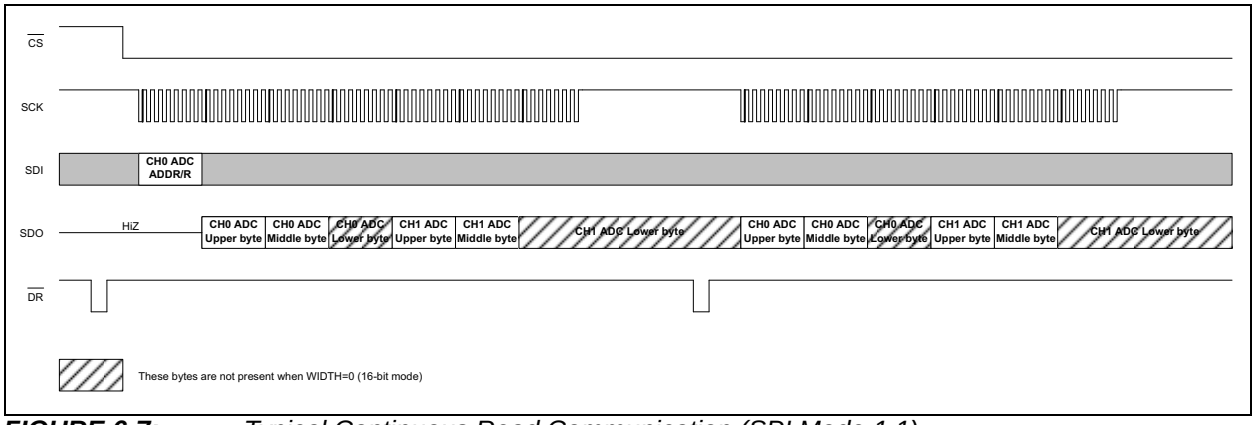


FIGURE 6-7: *Typical Continuous Read Communication (SPI Mode 1,1).*

6.7.2 CONTINUOUS WRITE

Both ADCs are powered up with their default configurations and begin to output data ready pulses immediately (RESET[1:0] and SHUTDOWN[1:0] bits are off by default).

The default output codes for both ADCs are all zeros. The default modulator output for both ADCs is '0011' (corresponding to a theoretical zero voltage at the inputs). The default phase is zero between the two channels.

It is recommended to enter into ADC Reset mode for both ADCs, just after power-up; this is because the desired MCP3911 register configuration may not be the default one. In this case, the ADC outputs undesired data. Within the ADC Reset mode (RESET[1:0] = 11), the user can configure the whole part with a single communication. The write commands automatically increment the address so that the user can start writing the PHASE register and finish with the CONFIG register in only one communication (see Figure 6-8). The RESET[1:0] bits are in the last byte of the CONFIG register to allow exiting the Soft Reset mode, and have the whole part configured and ready to run in only one command.

6.7.3 REGISTER GROUPS AND TYPES

The following register sets are defined as groups:

TABLE 6-1: REGISTER GROUPS

Group	Addresses
ADC DATA CH0	0x00-0x02
ADC DATA CH1	0x03-0x05
MOD, PHASE, GAIN	0x06-0x09
CONFIG, STATUSCOM	0x0A-0x0D
OFFCAL_CH0, GAINCAL_CH0	0x0E-0x13
OFFCAL_CH1, GAINCAL_CH1	0x14-0x19
VREFCAL	0x1A

The following register sets are defined as types:

TABLE 6-2: REGISTER TYPES

Type	Addresses
ADC DATA (both channels)	0x00-0x05
CONFIGURATION	0x06-0x1A

6.8 Situations that Reset ADC Data

Immediately after the following actions, the ADCs are reset and automatically restarted to provide proper operation:

1. Change in PHASE register.
2. Change in the OSR setting.
3. Change in the PRESCALE setting.
4. Overwrite of the same PHASE register value.
5. Change in the CLKEXT setting.
6. Change in the VREFEXT setting.
7. Change in the MODOUT setting.

After these temporary Resets, the ADCs go back to normal operation without the need for an additional command. If the same value is written in the PHASE register, it can be used to serially Soft Reset the ADCs, without using the RESET bits in the Configuration register.

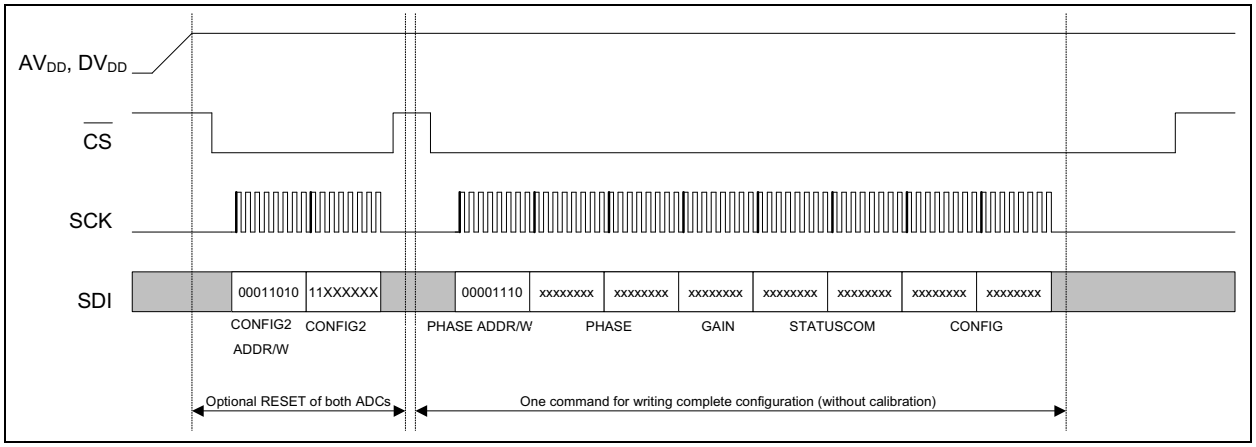


FIGURE 6-8: *Recommended Configuration Sequence at Power-up.*

6.9 Data Ready Pin ($\overline{DR}$)

To signify when channel data are ready for transmission, the data ready signal is available on the Data Ready pin ($\overline{DR}$) through an active-low pulse at the end of a channel conversion.

The Data Ready pin outputs an active-low pulse with a period that is equal to the DRCLK period and a width equal to one DMCLK period.

When not active-low, this pin can either be in high-impedance (when $\overline{DR_HIZ}$ = 0) or in a defined logic high state (when $\overline{DR_HIZ}$ = 1). This is controlled through the STATUSCOM register. This allows multiple devices to share the same Data Ready pin (with a pull-up resistor connected between $\overline{DR}$ and DV_{DD}) in 3-phase energy meter designs to reduce pin count. A single device on the bus does not require a pull-up resistor and therefore, it is recommended to use $\overline{DR_HIZ}$ = 1 configuration for such applications.

After a data ready pulse has occurred, the ADC output data can be read through SPI communication. Two sets of latches at the output of the ADC prevent the communication from outputting corrupted data (see **Section 6.10 "ADC Data Latches and Data Ready Modes (DRMODE[1:0])"**).

The $\overline{CS}$ pin has no effect on the $\overline{DR}$ pin, which means even if $\overline{CS}$ is logic high, data ready pulses will be provided (except when the configuration prevents them from outputting data ready pulses). The $\overline{DR}$ pin can be used as an interrupt when connected to an MCU or a DSP. While the $\overline{RESET}$ pin is logic low, the $\overline{DR}$ pin is not active.

6.10 ADC Data Latches and Data Ready Modes (DRMODE[1:0])

To ensure that both channels' ADC data are present at the same time for SPI read, regardless of phase delay settings for either or both channels, there are two sets of ADC data latches in series with both the data ready and the 'read start' triggers.

The first set of latches holds each output when the data are ready and latches both outputs together when DRMODE[1:0] = 00. When this mode is on, both ADCs work together and produce one set of available data after each data ready pulse (that corresponds to the lagging ADC data ready). The second set of latches ensures that when reading starts on an ADC output, the corresponding data are latched so that no data corruption can occur.

If an ADC read has started, to read the following ADC output, the current reading needs to be completed (all bits must be read from the ADC Output Data registers).

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6.10.1 DATA READY PIN ($\overline{DR}$) CONTROL USING DRMODE BITS

There are four modes that control the data ready pulses and these modes are set with the DRMODE[1:0] bits in the STATUSCOM register. For power metering applications, DRMODE[1:0] = 00 is recommended (Default mode).

The position of the data ready pulses vary, with respect to this mode, to the OSR and to the PHASE settings:

- **DRMODE[1:0] = 11:** Both data ready pulses from ADC Channel 0 and ADC Channel 1 are output on the $\overline{DR}$ pin.
- **DRMODE[1:0] = 10:** Data ready pulses from ADC Channel 1 are output on the $\overline{DR}$ pin. The data ready pulse from ADC Channel 0 is not present on the pin.
- **DRMODE[1:0] = 01:** Data ready pulses from ADC Channel 0 are output on the $\overline{DR}$ pin. The data ready pulse from ADC Channel 1 is not present on the pin.
- **DRMODE[1:0] = 00 (Recommended and Default mode):** Data ready pulses from the lagging ADC between the two are output on the $\overline{DR}$ pin. The lagging ADC depends on the PHASE register and on the OSR. In this mode, the two ADCs are linked so their data are latched together when the lagging ADC output is ready.

6.10.2 ADC CHANNELS LATCHING AND SYNCHRONIZATION

The ADC Channel Data Output registers (addresses 0x00 to 0x05) have a double-buffer output structure. The two sets of latches in series are triggered by the data ready signal and an internal signal indicating the beginning of a read communication sequence (read start).

The first set of latches holds each ADC Channel Data Output register when the data are ready and latches both outputs together when DRMODE[1:0] = 00. This behavior is synchronous with the MCLK.

The second set of latches ensures that when reading starts on an ADC output, the corresponding data are latched so that no data corruption can occur within a read. This behavior is synchronous with the SCK clock. If an ADC read has started, to read the following ADC output, the current reading needs to be fully completed (all bits must be read on the SDO pin from the ADC Output Data registers).

Since the double-output buffer structure is triggered with two events that depend on two asynchronous clocks (data ready with MCLK and read start with SCK), it is recommended to synchronize the reading of the channels with the MCU or processor using one of the following methods:

1. **Use the Data Ready pin pulses as an interrupt** – Once a falling edge occurs on the $\overline{DR}$ pin, the data are available for reading on the ADC Output registers after the t_{DODR} timing. If this timing is not respected, data corruption can occur.
2. **Use a timer clocked with MCLK as a synchronization event** – Since the data ready is synchronous with MCLK, the user can calculate the position of the data ready depending on the PHASE[11:0], OSR[2:0] and PRE[1:0] bits settings for each channel. Here, the t_{DODR} timing needs to be added to this calculation to avoid data corruption.
3. **Poll the DRSTATUS[1:0] bits in the STATUSCOM register** – This method consists of continuously reading the STATUSCOM register and waits for the DRSTATUS bits to be equal to '0'. When this event happens, the user can start a new communication to read the desired ADC data. In this case, no additional timing is required.

The first method is the preferred method as it can be used without adding additional MCU code space, but it requires connecting the $\overline{DR}$ pin to an I/O pin of the microcontroller. The other two methods require more MCU code space and execution time, but they allow synchronizing the reading of the channels without connecting the $\overline{DR}$ pin, which saves one I/O pin on the MCU.

6.10.3 DATA READY PULSES WITH SHUTDOWN OR RESET CONDITIONS

There are no data ready pulses if DRMODE[1:0] = 00 when either one or both of the ADCs are in Reset or Shutdown mode. In Mode 0,0, a data ready pulse only happens when both ADCs are ready. Any data ready pulse corresponds to one data on both ADCs. The two ADCs are linked together and act as if there was only one channel with the combined data of both ADCs. This mode is very practical when both ADC channels' data retrieval and processing need to be synchronized, as in power metering applications.

Note:	If DRMODE[1:0] = 11, the user is still able to retrieve the data ready pulse for the ADC not in Shutdown or Reset mode (i.e., only 1 ADC channel needs to be awake).

Figure 6-9 represents the behavior of the Data Ready pin with the different DRMODE configurations while shutdown or Reset is applied.

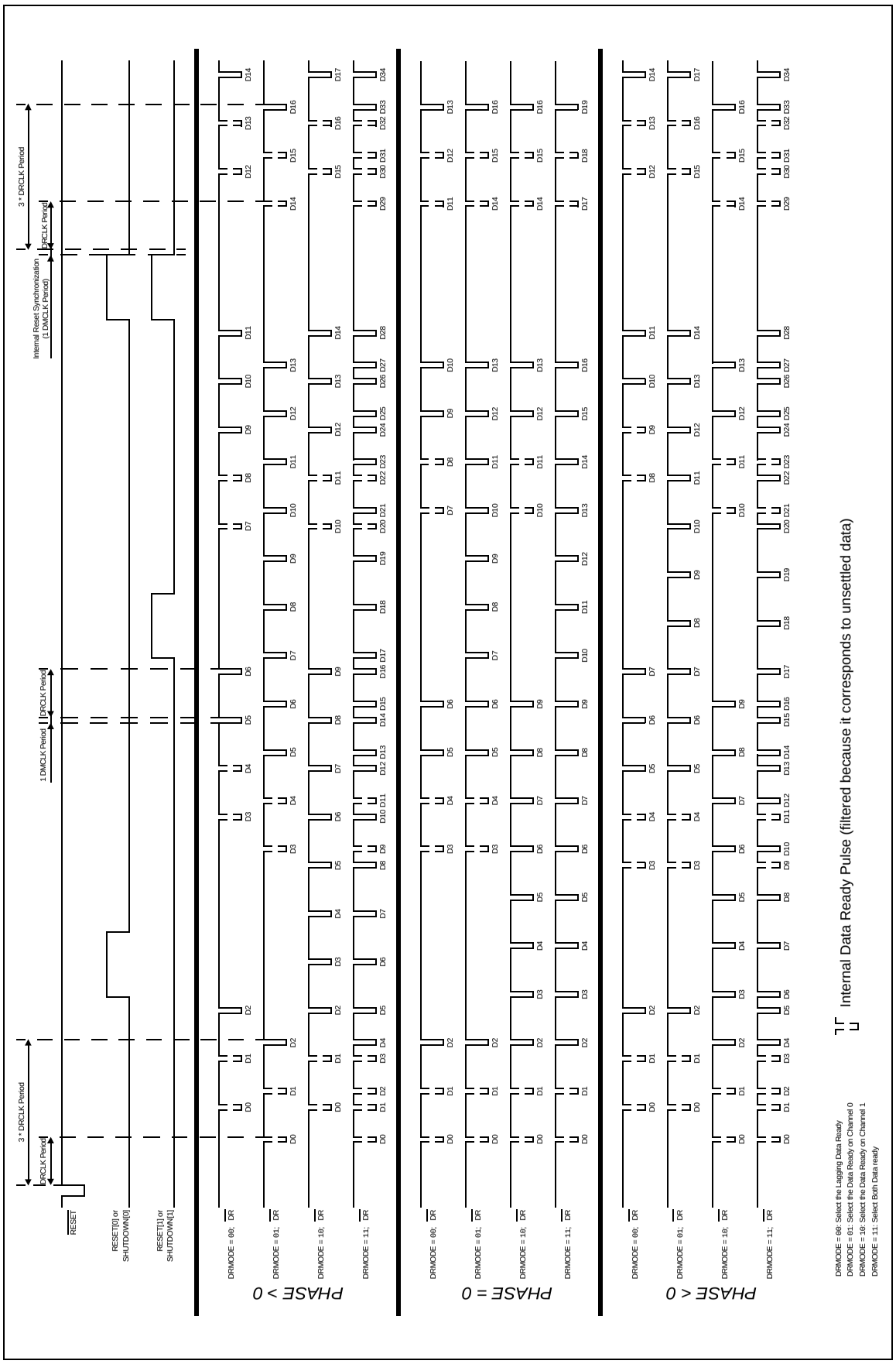


FIGURE 6-9: *Data Ready Behavior.*

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7.0 INTERNAL REGISTERS

The addresses associated with the internal registers are listed below, followed by a detailed description of the registers. All registers are split into 8-bit long registers which can be addressed and read separately. Read and Write modes define the groups and types of registers for continuous read/write communication or looping on address sets, as shown in Table 7-2.

TABLE 7-1: REGISTER MAP

Address	Name	Bits	R/W	Description
0x00	CHANNEL0	24	R	Channel 0 ADC 24-Bit Data [23:0], MSB First
0x03	CHANNEL1	24	R	Channel 1 ADC 24-Bit Data [23:0], MSB First
0x06	MOD	8	R/W	Modulator Output Register for Both ADC Channels
0x07	PHASE	16	R/W	Phase Delay Configuration Register
0x09	GAIN	8	R/W	Gain and Boost Configuration Register
0x0A	STATUSCOM	16	R/W	Status and Communication Register
0x0C	CONFIG	16	R/W	Configuration Register
0x0E	OFFCAL_CH0	24	R/W	Offset Correction Register – Channel 0
0x11	GAINCAL_CH0	24	R/W	Gain Correction Register – Channel 0
0x14	OFFCAL_CH1	24	R/W	Offset Correction Register – Channel 1
0x17	GAINCAL_CH1	24	R/W	Gain Correction Register – Channel 1
0x1A	VREFCAL	8	R/W	Internal Voltage Reference Temperature Coefficient Adjustment Register

TABLE 7-2: REGISTER MAP GROUPING FOR ALL CONTINUOUS READ/WRITE MODES

Function	Address	READ[1:0]				WRITE	
		= 11	= 10	= 01	= 00	= 1	= 0
CHANNEL 0	0x00	LOOP ENTIRE REGISTER MAP	TYPE	GROUP	Static	NOT WRITABLE	
	0x01				Static		
	0x02				Static		
CHANNEL 1	0x03			GROUP	Static		
	0x04				Static		
	0x05				Static		
MOD	0x06		TYPE	GROUP	Static	TYPE	Static
PHASE	0x07				Static		Static
	0x08				Static		Static
GAIN	0x09				Static		Static
STATUSCOM	0x0A			GROUP	Static		Static
	0x0B				Static		Static
CONFIG	0x0C				Static		Static
	0x0D				Static		Static
OFFCAL_CH0	0x0E			GROUP	Static		Static
	0x0F				Static		Static
	0x10				Static		Static
GAINCAL_CH0	0x11				Static		Static
	0x12				Static		Static
	0x13				Static		Static
OFFCAL_CH1	0x14			GROUP	Static		Static
	0x15				Static		Static
	0x16				Static		Static
GAINCAL_CH1	0x17				Static		Static
	0x18				Static		Static
	0x19				Static		Static
VREFCAL	0x1A			GROUP	Static		Static

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7.1 CHANNEL Registers – ADC Channel Data Output Registers

The ADC Channel Data Output registers always contain the most recent A/D conversion data for each channel. These registers are read-only and can be accessed independently or linked together (with the READ[1:0] bits). These registers are latched when an ADC read communication occurs. When a data ready event occurs during a read communication, the most current ADC data are also latched to avoid data corruption issues. The three bytes of each channel are updated synchronously at a DRCLK rate. The three bytes can be accessed separately if needed, but are refreshed synchronously.

Name	Bits	Address	R/W
CHANNEL0	24	0x00	R
CHANNEL1	24	0x03	R

REGISTER 7-1: CHANNEL: ADC CHANNEL DATA OUTPUT REGISTER

R-0 (MSB)	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DATA_CHn[23:16]							
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DATA_CHn[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DATA_CHn[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-0 **DATA_CHn[23:0]:** Output Code from ADC Channel n
These data are post-calibration if the EN_OFFCAL or EN_GAINCAL bits are enabled.

7.2 MOD Register – Modulators Output Register

The MOD register contains the most recent modulator data output. The default value corresponds to an equivalent input of 0V on both ADCs. Each bit in this register corresponds to one comparator output on one of the channels.

Name	Bits	Address	Cof
MOD	8	0x06	R/W

Note: This register should not be written to maintain ADC accuracy.

REGISTER 7-2: MOD: MODULATORS OUTPUT REGISTER

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1
Comparator3 Channel 1	Comparator2 Channel 1	Comparator1 Channel 1	Comparator0 Channel 1	Comparator3 Channel 0	Comparator2 Channel 0	Comparator1 Channel 0	Comparator0 Channel 0
COMP3_CH1	COMP2_CH1	COMP1_CH1	COMP0_CH1	COMP3_CH0	COMP2_CH0	COMP1_CH0	COMP0_CH0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4 **COMPn_CH1:** Comparator Outputs from ADC Channel 1

bit 3-0 **COMPn_CH0:** Comparator Outputs from ADC Channel 0

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7.3 PHASE Register – Phase Configuration Register

Any write to one of these two addresses (0x07 and 0x08) creates an internal reset and restart sequence.

Name	Bits	Address	Cof
PHASE	16	0x07	R/W

REGISTER 7-3: PHASE: PHASE CONFIGURATION REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	PHASE[11]	PHASE[10]	PHASE[9]	PHASE[8]
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASE[7]	PHASE[6]	PHASE[5]	PHASE[4]	PHASE[3]	PHASE[2]	PHASE[1]	PHASE[0]
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11-0 **PHASE[11:0]: CH0 Relative to CH1 Phase Delay**

Delay = PHASE register’s two’s complement code/DMCLK (Default PHASE = 0).

7.4 GAIN – Gain and Boost Configuration Register

Name	Bits	Address	Cof
GAIN	8	0x09	R/W

REGISTER 7-4: GAIN: GAIN AND BOOST CONFIGURATION REGISTER

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BOOST[1]	BOOST[0]	PGA_CH1[2]	PGA_CH1[1]	PGA_CH1[0]	PGA_CH0[2]	PGA_CH0[1]	PGA_CH0[0]
bit 15							bit 8

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **BOOST[1:0]:** Bias Current Selection

11 = Both channels have current x 2
10 = Both channels have current x 1 (default)
01 = Both channels have current x 0.66
00 = Both channels have current x 0.5

bit 5-3 **PGA_CH1[2:0]:** PGA Setting for Channel 1

111 = Reserved (Gain = 1)
110 = Reserved (Gain = 1)
101 = Gain is 32
100 = Gain is 16
011 = Gain is 8
010 = Gain is 4
001 = Gain is 2
000 = Gain is 1 (default)

bit 2-0 **PGA_CH0[2:0]:** PGA Setting for Channel 0

111 = Reserved (Gain = 1)
110 = Reserved (Gain = 1)
101 = Gain is 32
100 = Gain is 16
011 = Gain is 8
010 = Gain is 4
001 = Gain is 2
000 = Gain is 1 (default)

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7.5 STATUSCOM Register – Status and Communication Register

Name	Bits	Address	Cof
STATUSCOM	16	0x0A	R/W

REGISTER 7-5: STATUSCOM: STATUS AND COMMUNICATION REGISTER

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
MODOUT[1]	MODOUT[0]	—	$\overline{\text{DR_HIZ}}$	DRMODE[1]	DRMODE[0]	DRSTATUS[1]	DRSTATUS[0]
bit 15							bit 8

R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	U-0
READ[1]	READ[0]	WRITE	WIDTH[1]	WIDTH[0]	EN_OFFCAL	EN_GAINCAL	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **MODOUT[1:0]:** Modulator Output Setting for MDAT Pins
- 11 = Both CH0 and CH1 modulator outputs are present on the MDAT1 and MDAT0 pins; both SINC filters are off and no data ready pulse is present
- 10 = CH1 ADC modulator output present on the MDAT1 pin; SINC filter on Channel 1 is off and data ready pulse from Channel 1 is not present on the $\overline{\text{DR}}$ pin
- 01 = CH0 ADC modulator output present on the MDAT0 pin; SINC filter on Channel 0 is off and data ready pulse from Channel 0 is not present on $\overline{\text{DR}}$ pin
- 00 = No modulator output is enabled; SINC filters are on and data ready pulses are present on the $\overline{\text{DR}}$ pin for both channels (default)

bit 13 **Unimplemented**: Read as ‘0’.

bit 12 **$\overline{\text{DR_HIZ}}$:** Data Ready Pin Inactive State Control
- 1 = The $\overline{\text{DR}}$ pin state is a logic high when data are NOT ready
- 0 = The $\overline{\text{DR}}$ pin state is high-impedance when data are NOT ready (default)

bit 11-10 **DRMODE[1:0]:** Data Ready Pin ($\overline{\text{DR}}$) Mode Configuration
- 11 = Both data ready pulses from CH0 and CH1 are output on the $\overline{\text{DR}}$ pin
- 10 = Data ready pulses from CH1 ADC are output on the $\overline{\text{DR}}$ pin; data ready pulses from CH0 are not present on the $\overline{\text{DR}}$ pin
- 01 = Data ready pulses from CH0 ADC are output on the $\overline{\text{DR}}$ pin; data ready pulses from CH1 are not present on the $\overline{\text{DR}}$ pin
- 00 = Data ready pulses from the lagging ADC between the two are output on the $\overline{\text{DR}}$ pin. The lagging ADC depends on the PHASE register and on the OSR (default).

bit 9-8 **DRSTATUS[1:0]:** Data Ready Status
- 11 = ADC Channel 1 and Channel 0 data are not ready (default)
- 10 = ADC Channel 1 data are not ready, ADC Channel 0 data are ready
- 01 = ADC Channel 0 data are not ready, ADC Channel 1 data are ready
- 00 = ADC Channel 1 and Channel 0 data are ready

bit 7-6 **READ[1:0]:** Address Loop Setting
- 11 = Address counter incremented, cycle through entire register set
- 10 = Address counter loops on register types (default)
- 01 = Address counter loops on register groups
- 00 = Address not incremented, continually reads single register

REGISTER 7-5: STATUSCOM: STATUS AND COMMUNICATION REGISTER (CONTINUED)

bit 5 **WRITE:** Address Loop Setting for Write Mode
1 = Address counter loops on entire register map (default)
0 = Address not incremented, continually writes same single register

bit 4-3 **WIDTH[1:0]** ADC Channel Output Data Word Width
11 = Both channels are in 24-bit mode(default)
10 = Channel 1 in 16-bit mode, Channel 0 in 24-bit mode
01 = Channel 1 in 16-bit mode, Channel 0 in 24-bit mode
00 = Both channels are in 16-bit mode

bit 2 **EN_OFFCAL** Enables or Disables 24-Bit Digital Offset Calibration on Both Channels
1 = Enabled; this mode does not add any group delay
0 = Disabled (default)

bit 1 **EN_GAINCAL** Enables or Disables 24-Bit Digital Offset Calibration on Both Channels
1 = Enabled; this mode adds a group delay on both channels of 24 DMCLK periods, all data ready pulses are delayed by 24 clock periods compared to the mode with EN_GAINCAL = 0
0 = Disabled (default)

bit 0 **Unimplemented:** Read as '0'

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7.6 CONFIG Register – Configuration Register

Name	Bits	Address	Cof
CONFIG	16	0x0C	R/W

REGISTER 7-6: CONFIG: CONFIGURATION REGISTER

R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0
PRE[1]	PRE[0]	OSR[2]	OSR[1]	OSR[0]	DITHER[1]	DITHER[0]	AZ_FREQ
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-1	U-0
RESET[1]	RESET[0]	SHUTDOWN[1]	SHUTDOWN[0]	—	VREFEXT	CLKEXT	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **PRE[1:0]:** Analog Master Clock (AMCLK) Prescaler Value
11 = AMCLK = MCLK/8
10 = AMCLK = MCLK/4
01 = AMCLK = MCLK/2
00 = AMCLK = MCLK (default)

bit 13-11 **OSR[2:0]:** Oversampling Ratio for Delta-Sigma A/D Conversion (All Channels, f_d/f_S)
111 = 4096 (f_d = 244 sps for MCLK = 4 MHz, f_S = AMCLK = 1 MHz)
110 = 2048 (f_d = 488 sps for MCLK = 4 MHz, f_S = AMCLK = 1 MHz)
101 = 1024 (f_d = 976 sps for MCLK = 4 MHz, f_S = AMCLK = 1 MHz)
100 = 512 (f_d = 1.953 ksps for MCLK = 4 MHz, f_S = AMCLK = 1 MHz)
011 = 256 (f_d = 3.90625 ksps for MCLK = 4 MHz, f_S = AMCLK = 1 MHz) (default)
010 = 128 (f_d = 7.8125 ksps for MCLK = 4 MHz, f_S = AMCLK = 1 MHz)
001 = 64 (f_d = 15.625 ksps for MCLK = 4 MHz, f_S = AMCLK = 1 MHz)
000 = 32 (f_d = 31.25 ksps for MCLK = 4 MHz, f_S = AMCLK = 1 MHz)

bit 10-9 **DITHER[1:0]:** Control for dithering circuit for idle tones cancellation and improved THD
11 = Dithering on, both channels, Strength = Maximum(MCP3901 equivalent) – (default)
10 = Dithering on, both channels, Strength = Medium
01 = Dithering on, both channels, Strength = Minimum
00 = Dithering turned off

bit 8 **AZ_FREQ:** Auto-Zero Frequency Setting
1 = Auto-zeroing algorithm running at higher speed
0 = Auto-zeroing algorithm running at lower speed (default)

bit 7-6 **RESET[1:0]:** Reset Mode Setting for ADCs
11 = Both CH0 and CH1 ADC are in Reset mode
10 = CH1 ADC is in Reset mode
01 = CH0 ADC is in Reset mode
00 = Neither ADC is in Reset mode (default)

bit 5-4 **SHUTDOWN[1:0]:** Shutdown mode setting for ADCs
11 = Both CH0 and CH1 ADC are in shutdown
10 = CH1 ADC is in shutdown
01 = CH0 ADC is in shutdown
00 = Neither channel is in shutdown (default)

bit 3 **Unimplemented:** Read as ‘0’

REGISTER 7-6: CONFIG: CONFIGURATION REGISTER (CONTINUED)

bit 2 **VREFEXT** Internal Voltage Reference Shutdown Control
1 = Internal voltage reference disabled
0 = Internal voltage reference enabled (default)

bit 1 **CLKEXT** Internal Clock Selection
1 = External clock drive by MCU on OSC1 pin (crystal oscillator disabled, no internal power consumption) (default)
0 = Crystal oscillator is enabled; a crystal must be placed between the OSC1 and OSC2 pins

bit 0 **Not implemented:** Read as '0'

7.7 OFFCAL_CHn Registers – Digital Offset Error Calibration Registers

Name	Bits	Address	Cof
OFFCAL_CH0	24	0x0E	R/W
OFFCAL_CH1	24	0x14	R/W

REGISTER 7-7: OFFCAL_CHn: DIGITAL OFFSET ERROR CALIBRATION REGISTER

R/W-0	R/W-0	R/W-0	...	R/W-0	R/W-0	R/W-0	R/W-0
OFFCAL_CHn[23:21]			...	OFFCAL_CHn[3:0]			
bit 23							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-0 **OFFCAL_CHn[23:0]:** Corresponding Channel CHn Digital Offset Calibration Value
This register is simply added to the output code of the channel, bit-by-bit. This register is 24-bit two's complement MSB first coding.
CHn Output Code = OFFCAL_CHn + ADC CHn Output Code. This register is a "Don't Care" if EN_OFFCAL = 0 (offset calibration disabled), but its value is not cleared by the EN_OFFCAL bit.

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7.8 GAINCAL_CHn Registers – Digital Gain Error Calibration Registers

Name	Bits	Address	Cof
GAINCAL_CH0	24	0x11	R/W
GAINCAL_CH1	24	0x17	R/W

REGISTER 7-8: GAINCAL_CHn: DIGITAL GAIN ERROR CALIBRATION REGISTER

R/W-0	R/W-0	R/W-0	...	R/W-0	R/W-0	R/W-0	R/W-0
GAINCAL_CHn[23:21]			...	GAINCAL_CHn[3:0]			
bit 23							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-0 **GAINCAL_CHn:** Corresponding Channel CHn Digital Gain Error Calibration Value

This register is 24-bit signed MSB first coding with a range of -1x to +0.9999999x (from 0x80000 to 0x7FFFFF). The gain calibration adds 1x to this register and multiplies it to the output code of the channel, bit-by-bit, after the offset calibration. Thus, the range of the gain calibration is from 0x to 1.9999999x (from 0x80000 to 0x7FFFFF). The LSB corresponds to a 2^{-23} increment in the multiplier.

CHn Output Code = (GAINCAL_CHn+1) x ADC CHn Output Code. This register is a "Don't Care" if EN_GAINCAL = 0 (offset calibration disabled), but its value is not cleared by the EN_GAINCAL bit.

7.9 VREFCAL Register – Internal Voltage Reference Temperature Coefficient Adjustment Register

This register is only for advanced users. This register should not be written unless the user wants to calibrate the temperature coefficient of the whole system or application. The default value of this register is set to 0x42.

Name	Bits	Address	Cof
VREFCAL	8	0x1A	R/W

REGISTER 7-9: VREFCAL REGISTER

R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0
VREFCAL[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **VREFCAL[7:0]:** Internal Voltage Temperature Coefficient Value

See **Section 5.7.3 "Temperature Compensation (VREFCAL Register)"** for complete description.

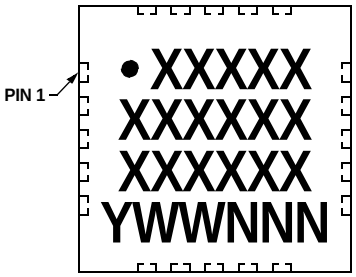
NOTES:

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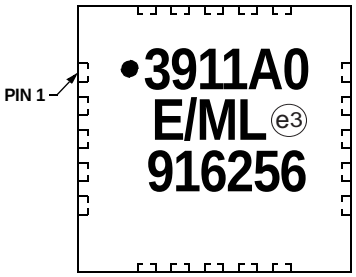
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

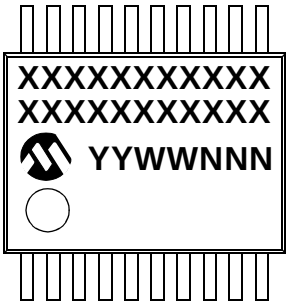
20-Lead QFN (4x4x0.9 mm)



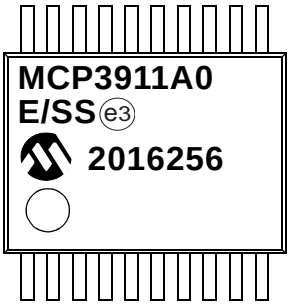
Example



20-Lead SSOP



Example

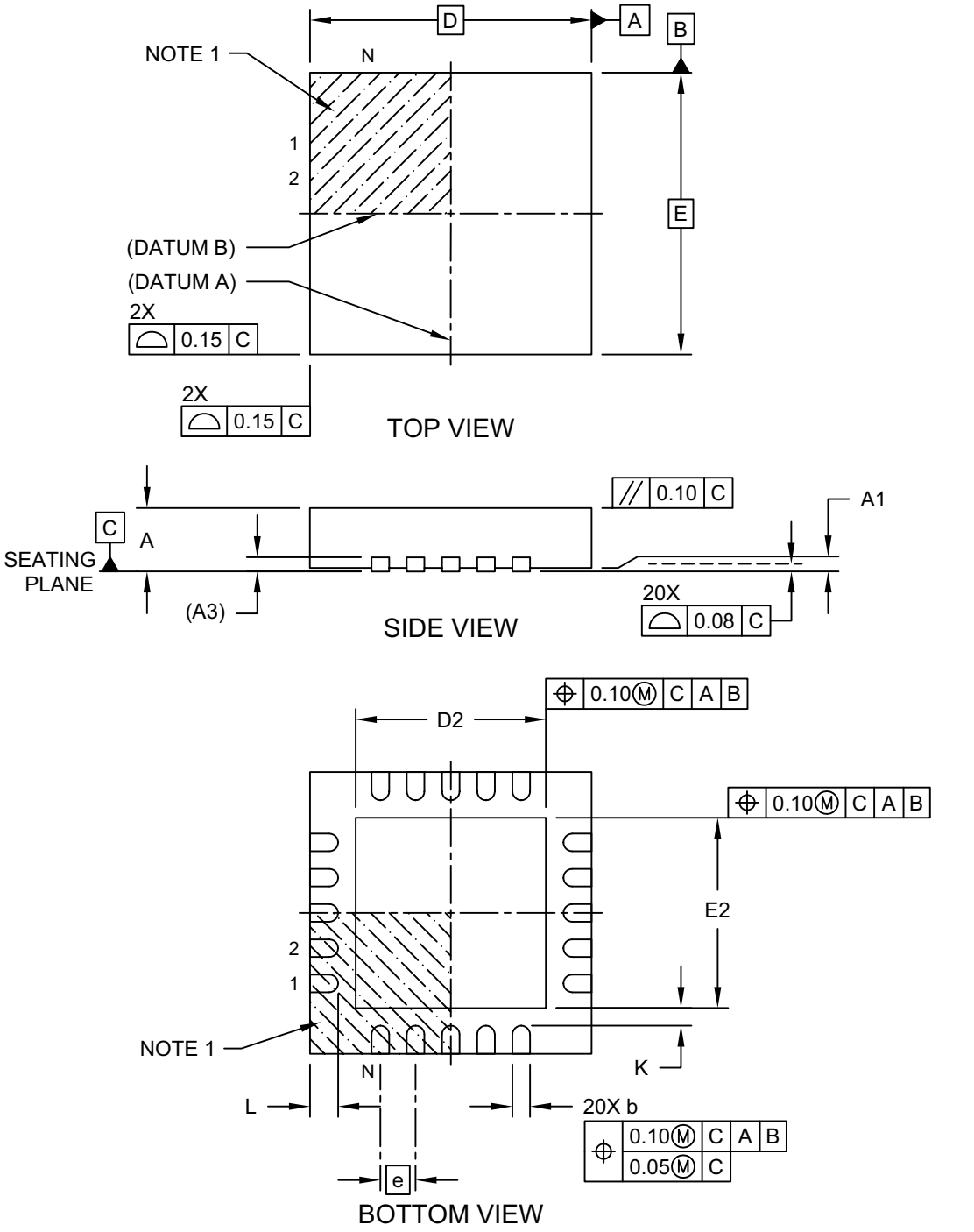


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free Compliant JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free Compliant. The Pb-free Compliant JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

20-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4 mm Body [QFN]
Also called VQFN

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

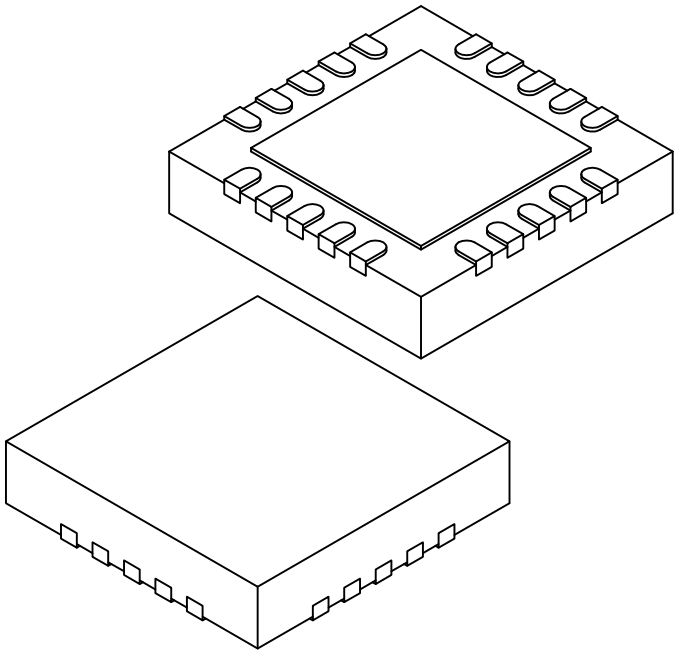


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Also called VQFN

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.60	2.70	2.80
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

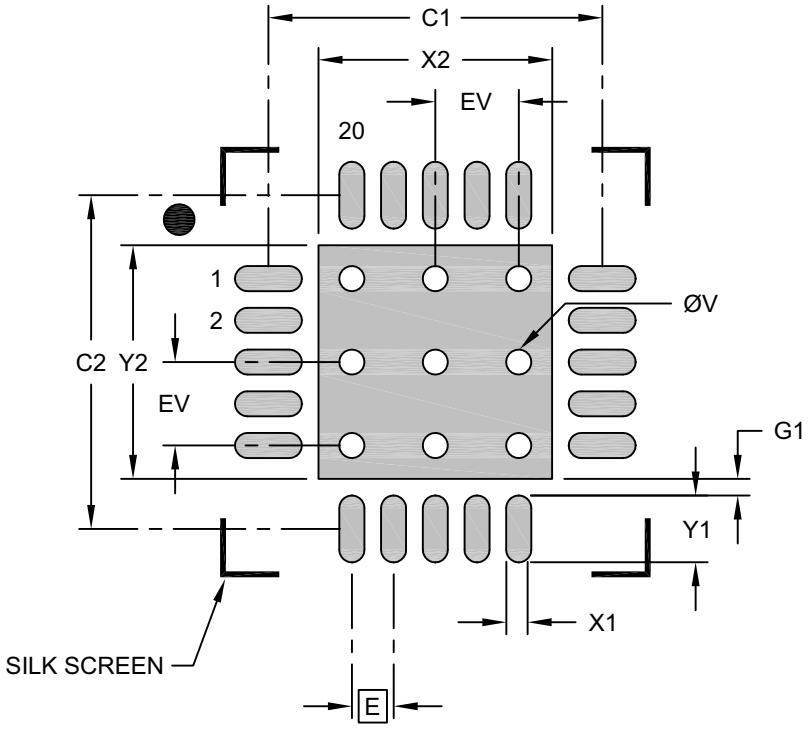
REF: Reference Dimension, usually without tolerance, for information purposes only.

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20-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4 mm Body [QFN]
Also called VQFN

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			2.80
Optional Center Pad Length	Y2			2.80
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X20)	X1			0.30
Contact Pad Length (X20)	Y1			0.80
Contact Pad to Center Pad (X16)	G1	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

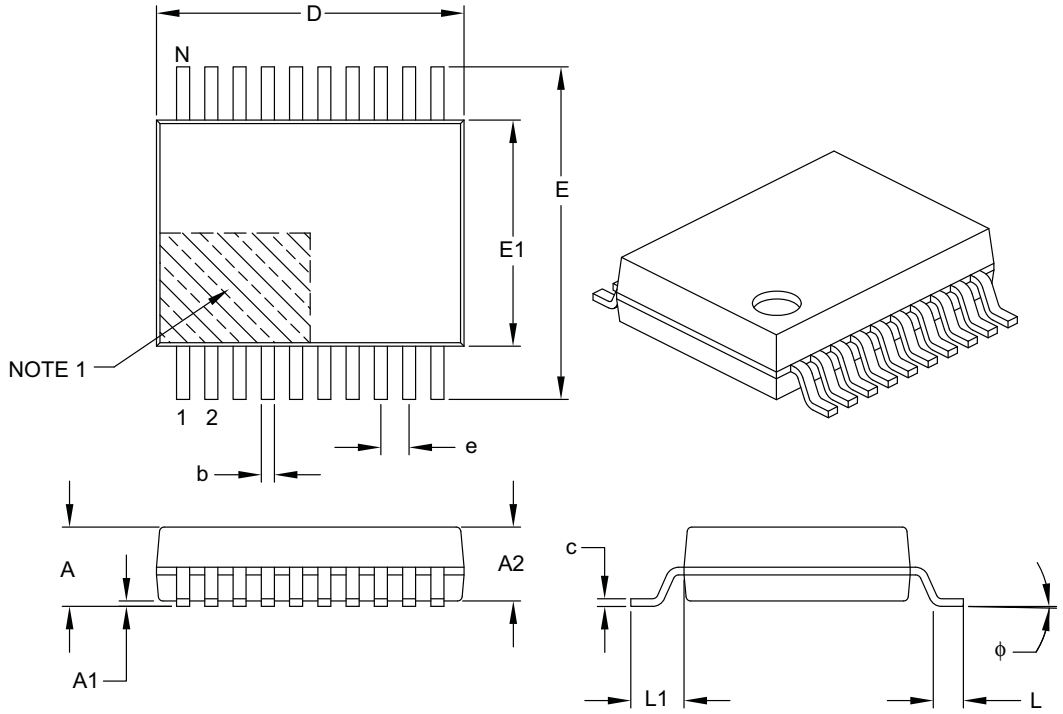
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2126 Rev B

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20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

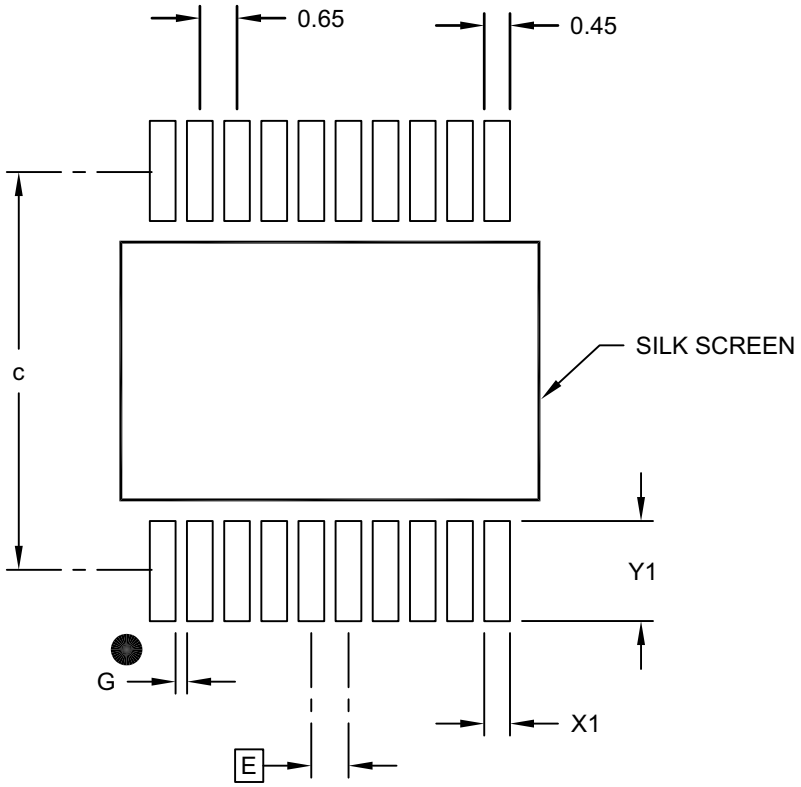
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072B

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APPENDIX A: REVISION HISTORY

Revision D (January 2020)

The following is the list of modifications:

1. Updated Offset Error and Gain Error in Table 1-1.

Revision C (October 2013)

The following is the list of modifications:

1. Changed units from kW to kΩ in Table 1-1.

Revision B (October 2013)

The following is the list of modifications:

1. Corrected ESD values in Absolute Maximum Ratings† section and throughout the document.
2. Updated Section 3.0, Pin Description.
3. Added new Section 6.10.2, ADC Channels Latching and Synchronization.
4. Updated Table 7-2.
5. Added note to Section 7.2, MOD Register – Modulators Output Register.
6. Minor grammatical and spelling corrections.

Revision A (March 2012)

- Original release of this document.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	X	X	/XX
Device	Address Options	Tape and Reel	Temperature Range	Package

Device: MCP3911A0: Two-Channel Analog Font-End Converter

Address Options:

XX		A6	A5
A0*	=	0	0
A1	=	0	1
A2	=	1	0
A3	=	1	1

* Default option. Contact Microchip factory for other address options.

Tape and Reel: T = Tape and Reel

Temperature Range: E = -40°C to +125°C

Package: ML = Plastic Quad Flat No Lead Package (QFN)
SS = Small Shrink Output Package (20-Lead SSOP)

Examples:

a) MCP3911A0-E/ML: Extended Temperature, Two-Channel Analog Front-End Converter, 20-Lead QFN Package.

b) MCP3911A0T-E/ML: Tape and Reel, Extended Temperature, Two-Channel Analog Front-End Converter, 20-Lead QFN Package.

c) MCP3911A0-E/SS: Extended Temperature, Two-Channel Analog Front-End Converter, 20-Lead SSOP Package.

d) MCP3911A0T-E/SS: Tape and Reel, Extended Temperature, Two-Channel Analog Front-End Converter, 20-Lead SSOP Package.

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NOTES:

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