MCP4725

12-Bit Digital-to-Analog Converter with EEPROM Memory

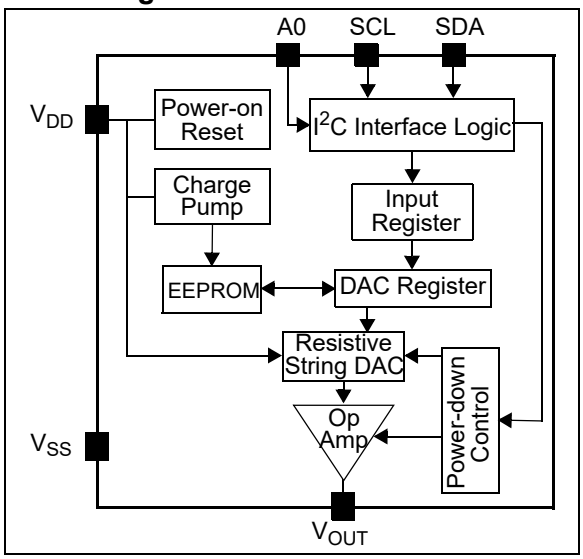
Features

- 12-Bit Resolution
- On-Board Nonvolatile Memory (EEPROM)
- ±0.2 LSB DNL (typical)
- External A0 Address Pin
- Normal or Power-Down Mode
- Fast Settling Time: 6 µs (typical)
- External Voltage Reference (V_{DD})
- Rail-to-Rail Output
- Low Power Consumption
- Single-Supply Operation: 2.7V to 5.5V
- I^2C Interface:
  - Eight Available Addresses
  - Standard (100 kbps), Fast (400 kbps), and High-Speed (3.4 Mbps) Modes
- Small 6-Lead SOT-23 and DFN Package Options
- Extended Temperature Range: -40°C to +125°C

Applications

- Set Point or Offset Trimming
- Sensor Calibration
- Closed-Loop Servo Control
- Low Power Portable Instrumentation
- PC Peripherals
- Data Acquisition Systems

Block Diagram



General Description

The MCP4725 is a low-power, high accuracy, single channel, 12-bit buffered voltage output Digital-to-Analog Converter (DAC) with nonvolatile memory (EEPROM). Its on-board precision output amplifier allows it to achieve rail-to-rail analog output swing.

The DAC input and configuration data can be programmed to the nonvolatile memory (EEPROM) by the user using I^2C interface command. The nonvolatile memory feature enables the DAC device to hold the DAC input code during power-off time, and the DAC output is available immediately after power-up. This feature is very useful when the DAC device is used as a supporting device for other devices in the network.

The device includes a Power-on-Reset (POR) circuit to ensure reliable power-up and an on-board charge pump for the EEPROM programming voltage. The DAC reference is driven from V_{DD} directly. In power-down mode, the output amplifier can be configured to present a known low, medium, or high resistance output load.

The MCP4725 has an external A0 address bit selection pin. This A0 pin can be tied to V_{DD} or V_{SS} of the user's application board.

The MCP4725 has a two-wire I^2C compatible serial interface for standard (100 kHz), fast (400 kHz), or high speed (3.4 MHz) mode.

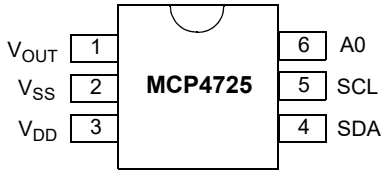
The MCP4725 is an ideal DAC device where design simplicity and small footprint is desired, and for applications requiring the DAC device settings to be saved during power-off time.

The device is available in a small 6-pin SOT-23 and DFN package.

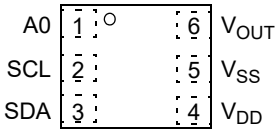
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Package Types

SOT-23-6



6-Lead DFN



Note: The DFN package features an Exposed Pad on the bottom of the package.
See Table 3-1 for pin descriptions.

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{DD}.....6.5V
All inputs and outputs w.r.t V_{SS} .....–0.3V to V_{DD}+0.3V
Current at Input Pins .....±2 mA
Current at Supply Pins .....±50 mA
Current at Output Pins .....±25 mA
Storage Temperature .....-65°C to +150°C
Ambient Temp. with Power Applied .....-55°C to +125°C
ESD protection on all pins ..... ≥ 6 kV HBM, ≥ 400V MM
Maximum Junction Temperature (T_J) .....+150°C

† Notice: Stresses above those listed under "Absolute Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at V_{DD} = + 2.7V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ from V_{OUT} to V_{SS}, C_L = 100 pF, T_A = -40°C to +125°C. Typical values are at +25°C.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Requirements						
Operating Voltage	V_{DD}	2.7	—	5.5	V	
Supply Current	I_{DD}	—	210	400	µA	Digital input pins are grounded, Output pin (V_{OUT}) is not connected (unloaded), Code = 000h
Power-Down Current	I_{DDP}	—	0.06	2.0	µA	V_{DD} = 5.5V
Power-On-Reset Threshold Voltage	V_{POR}	—	2	—	V	
DC Accuracy						
Resolution	n	12	—	—	Bits	Code Range = 000h to FFFh
INL Error	INL	—	±2	±14.5	LSB	**Note 1**
DNL	DNL	-0.75	±0.2	±0.75	LSB	**Note 1**
Offset Error	V_{OS}		0.02	0.75	% of FSR	Code = 000h
Offset Error Drift	ΔV_{OS}/°C	—	±1	—	ppm/°C	-45°C to +25°C
		—	±2	—	ppm/°C	+25°C to +85°C
Gain Error	G_E	-2	-0.1	2	% of FSR	Code = FFFh, Offset error is not included.
Gain Error Drift	ΔG_E/°C	—	-3	—	ppm/°C	
Output Amplifier						
Phase Margin	p_M	—	66	—	Degree(°)	C_L = 400 pF, R_L = ∞
Capacitive Load Stability	C_L	—	—	1000	pF	R_L = 5 kΩ, **Note 2**
Slew Rate	SR	—	0.55	—	V/µs	
Short Circuit Current	I_{SC}	—	15	24	mA	V_{DD} = 5V, V_{OUT} = Grounded
Output Voltage Settling Time	T_S	—	6	—	µs	**Note 3**

Note 1: Test Code Range: 100 to 4000.
2: This parameter is ensured by design and not 100% tested.
3: Within 1/2 LSB of the final value when code changes from 1/4 to 3/4 (400h to C00h) of full scale range.
4: Logic state of external address selection pin (A0 pin).

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at V_{DD} = + 2.7V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ from V_{OUT} to V_{SS}, C_L = 100 pF, T_A = -40°C to +125°C. Typical values are at +25°C.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Up Time	T_{PU}	—	2.5	—	µs	V_{DD} = 5V
		—	5	—	µs	V_{DD} = 3V Exit Power-down Mode, (Started from falling edge of ACK pulse)
DC Output Impedance	R_{OUT}	—	1	—	Ω	Normal mode (V_{OUT} to V_{SS})
		—	1	—	kΩ	Power-Down Mode 1 (V_{OUT} to V_{SS})
		—	100	—	kΩ	Power-Down Mode 2 (V_{OUT} to V_{SS})
		—	500	—	kΩ	Power-Down Mode 3 (V_{OUT} to V_{SS})
Supply Voltage Power-up Ramp Rate for EEPROM loading	V_{DD_RAMP}	1	—	—	V/ms	Validation only.
Dynamic Performance						
Major Code Transition Glitch		—	45	—	nV-s	1 LSB change around major carry (from 800h to 7FFh) (**Note 2**)
Digital Feedthrough		—	<10	—	nV-s	**Note 2**
Digital Interface						
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 3 mA
Input High Voltage (SDA and SCL Pins)	V_{IH}	$0.7V_{DD}$	—	—	V	
Input Low Voltage (SDA and SCL Pins)	V_{IL}	—	—	$0.3V_{DD}$	V	
Input High Voltage (A0 Pin)	$V_{A0\text{-}Hi}$	$0.8V_{DD}$	—	—		**Note 4**
Input Low Voltage (A0 Pin)	$V_{A0\text{-}IL}$	—	—	$0.2V_{DD}$		**Note 4**
Input Leakage	I_{LI}	—	—	±1	µA	SCL = SDA = A0 = V_{SS} or SCL = SDA = A0 = V_{DD}
Pin Capacitance	C_{PIN}	—	—	3	pF	**Note 2**
EEPROM						
EEPROM Write Time	TWRITE	—	25	50	ms	
Data Retention		—	200	—	Years	At +25°C, (**Note 2**)
Endurance		1	—	—	Million Cycles	At +25°C, (**Note 2**)

Note 1: Test Code Range: 100 to 4000.

2: This parameter is ensured by design and not 100% tested.

3: Within 1/2 LSB of the final value when code changes from 1/4 to 3/4 (400h to C00h) of full scale range.

4: Logic state of external address selection pin (A0 pin).

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TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 6L-SOT-23	θ_{JA}	—	190.5	—	°C/W	
Thermal Resistance, 6L-DFN	θ_{JA}	—	60.5	—	°C/W	

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NOTES:

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ to V_{SS}, C_L = 100 pF.

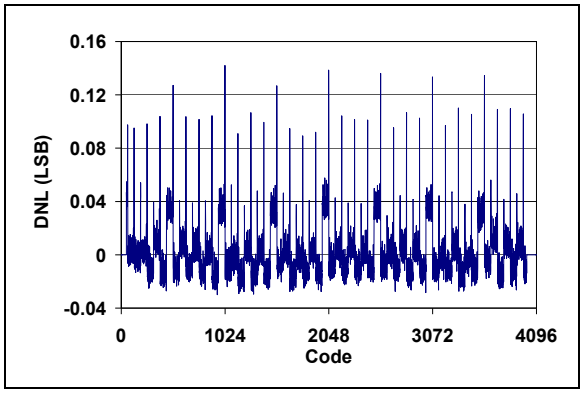


FIGURE 2-1: *DNL vs. Code (V_{DD} = 5.5V).*

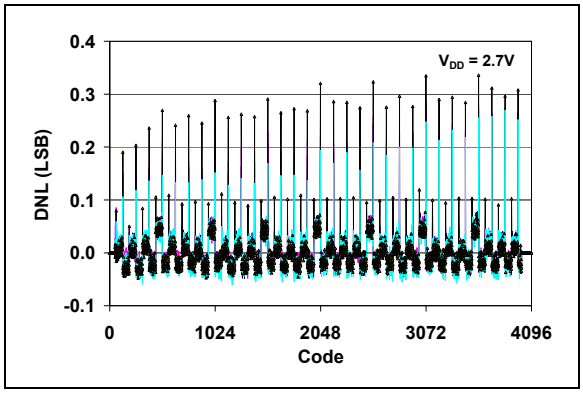


FIGURE 2-4: *DNL vs. Code and Temperature (T_A = -40°C to +125°C).*

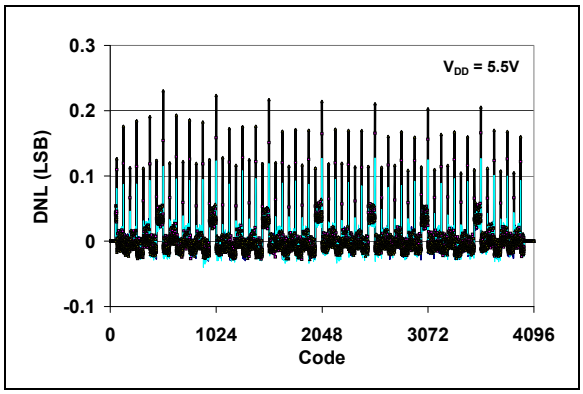


FIGURE 2-2: *DNL vs. Code and Temperature (T_A = -40°C to +125°C).*

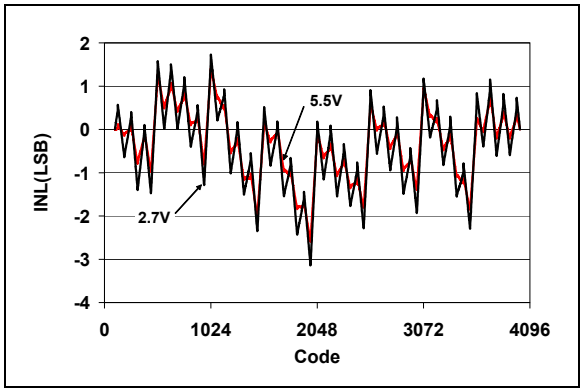


FIGURE 2-5: *INL vs. Code.*

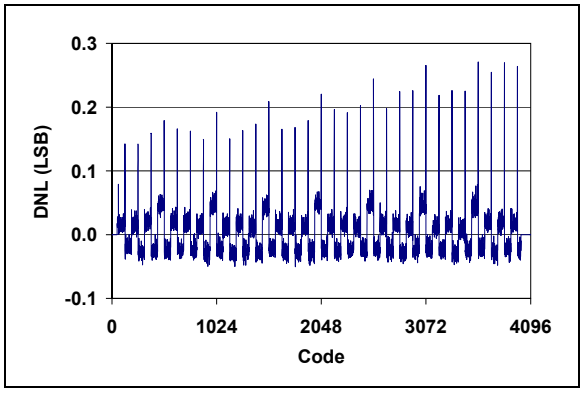


FIGURE 2-3: *DNL vs. Code (V_{DD} = 2.7V).*

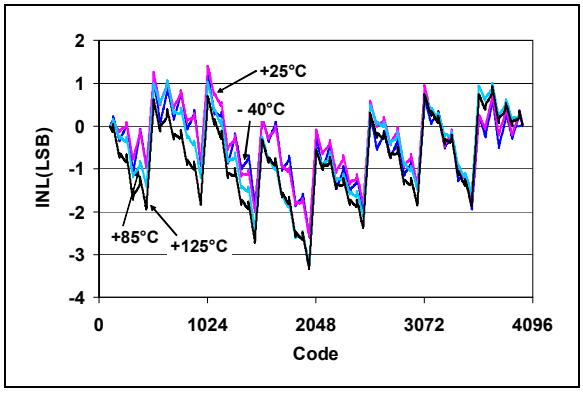


FIGURE 2-6: *INL vs. Code and Temperature (V_{DD} = 5.5V).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ to V_{SS}, C_L = 100 pF.

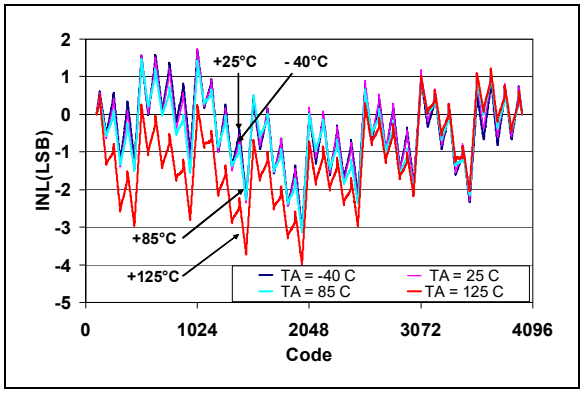


FIGURE 2-7: *INL vs. Code and Temperature (V_{DD} = 2.7V).*

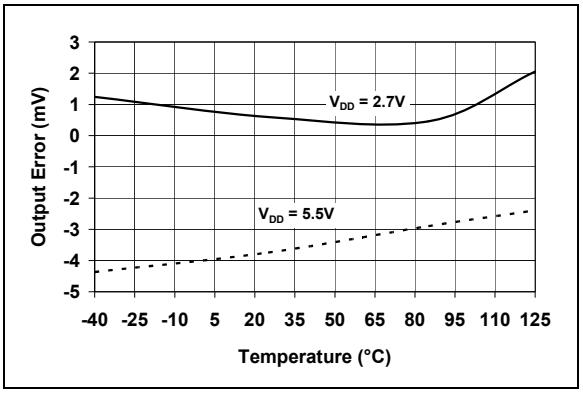


FIGURE 2-10: *Output Error vs. Temperature (Code = 4000d).*

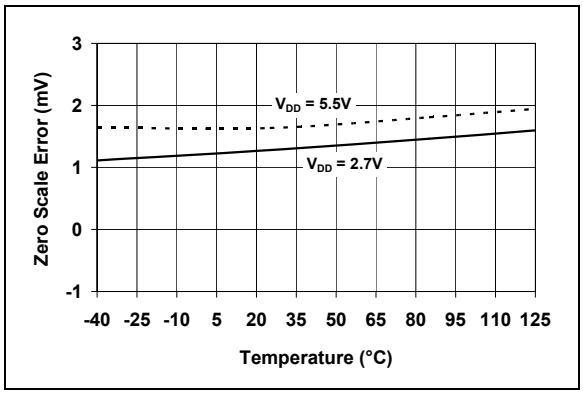


FIGURE 2-8: *Zero Scale Error vs. Temperature (Code = 000d).*

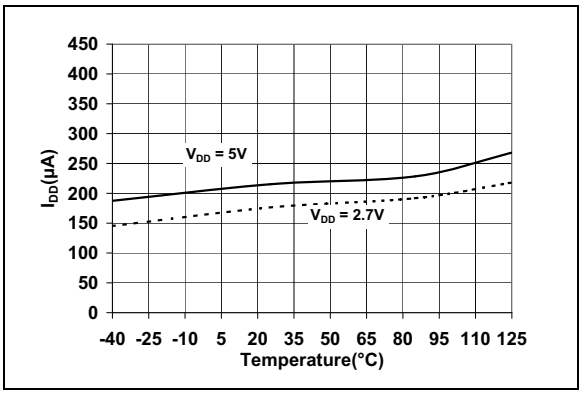


FIGURE 2-11: *I_{DD} vs. Temperature.*

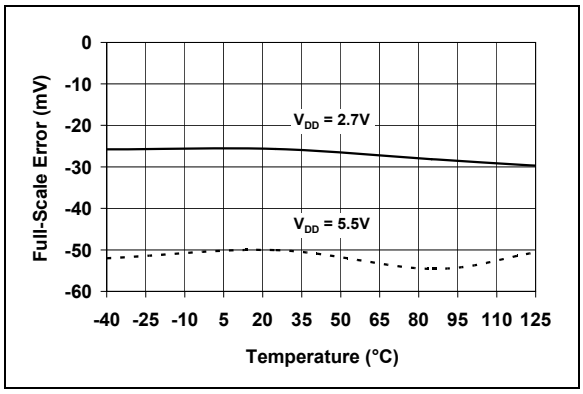


FIGURE 2-9: *Full Scale Error vs. Temperature (Code = 4095d).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ to V_{SS}, C_L = 100 pF.

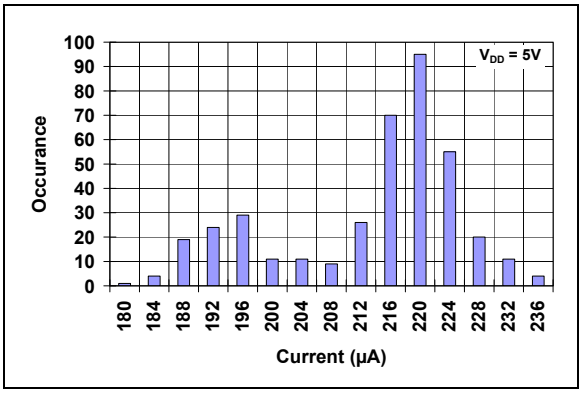


FIGURE 2-12: *I_{DD} Histogram.*

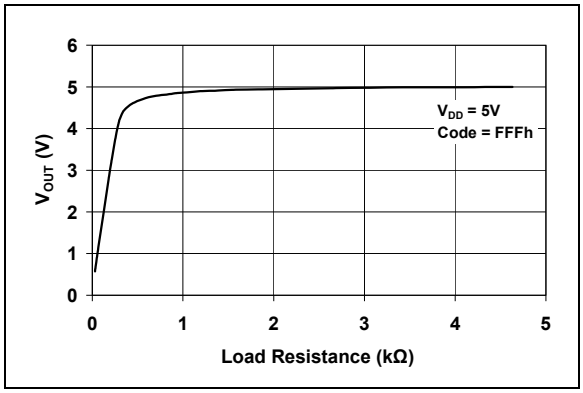


FIGURE 2-15: *V_{OUT} vs. Resistive Load.*

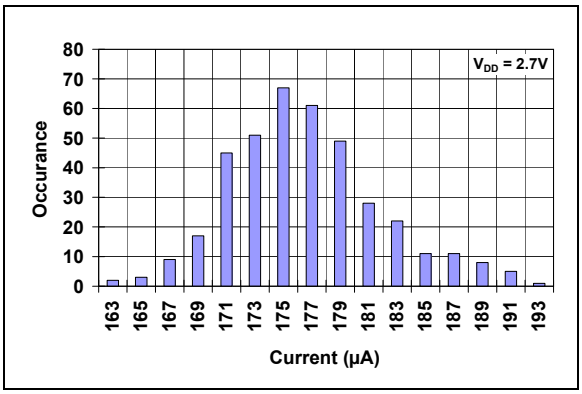


FIGURE 2-13: *I_{DD} Histogram.*

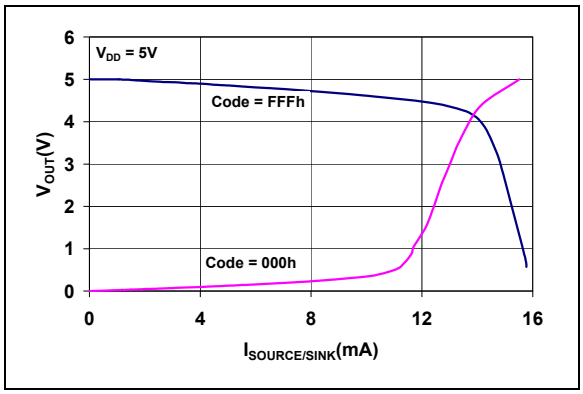


FIGURE 2-16: *Source and Sink Current Capability.*

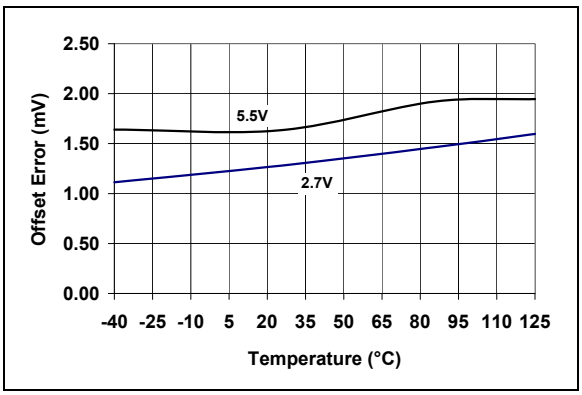


FIGURE 2-14: *Offset Error vs. Temperature and V_{DD}.*

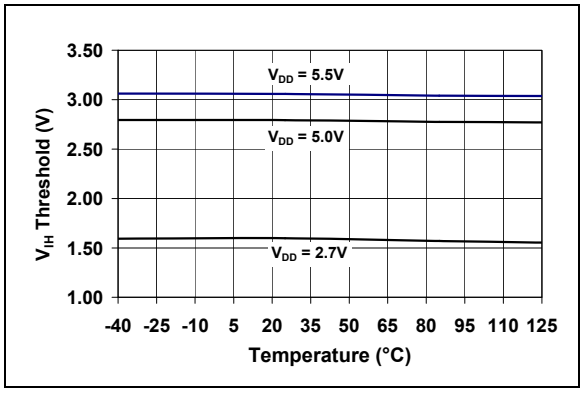


FIGURE 2-17: *V_{IN} High Threshold vs. Temperature and V_{DD}.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ to V_{SS}, C_L = 100 pF.

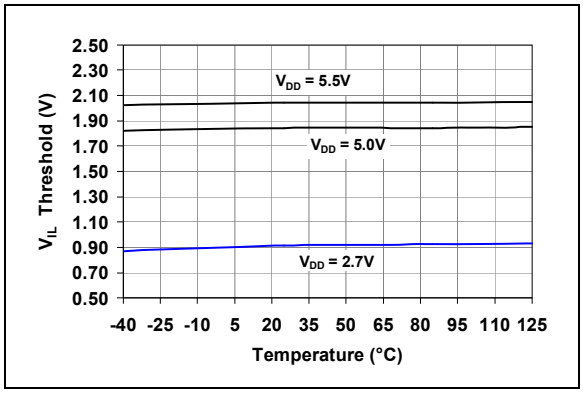


FIGURE 2-18: *V_{IN} Low Threshold vs. Temperature and V_{DD}.*

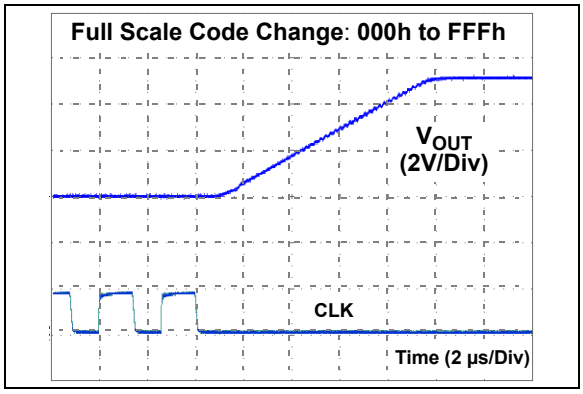


FIGURE 2-19: *Full Scale Settling Time.*

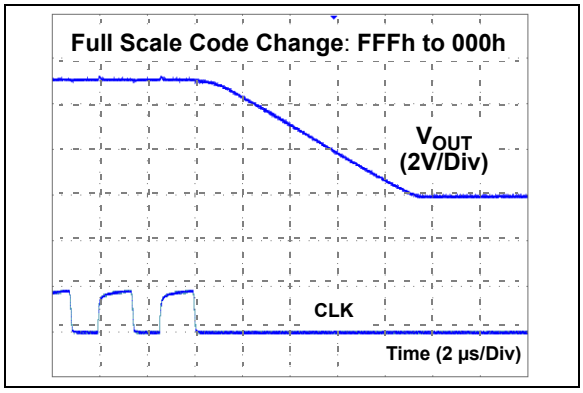


FIGURE 2-20: *Full Scale Settling Time.*

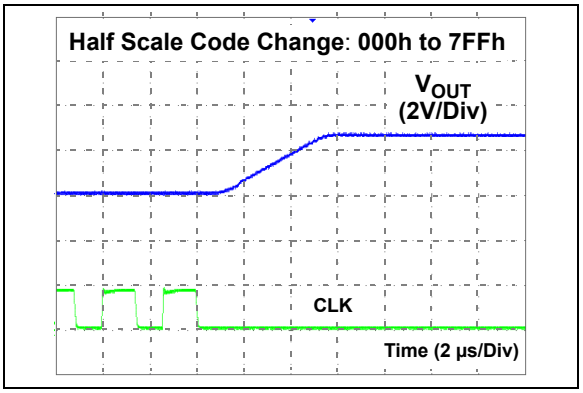


FIGURE 2-21: *Half Scale Settling Time.*

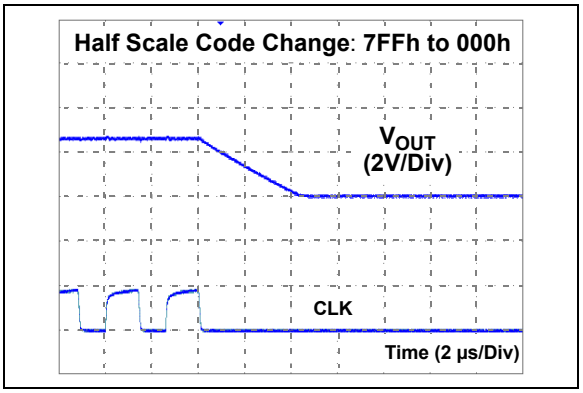


FIGURE 2-22: *Half Scale Settling Time.*

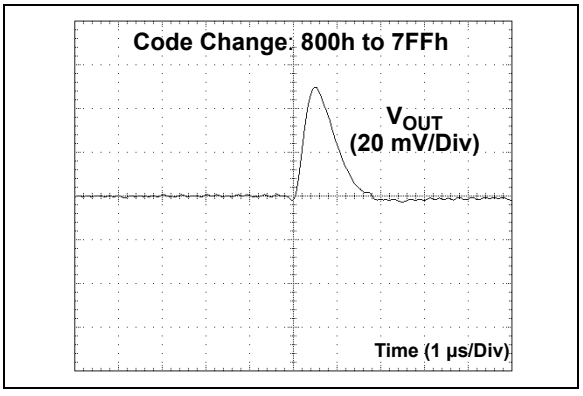


FIGURE 2-23: *Code Change Glitch.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ to V_{SS}, C_L = 100 pF.

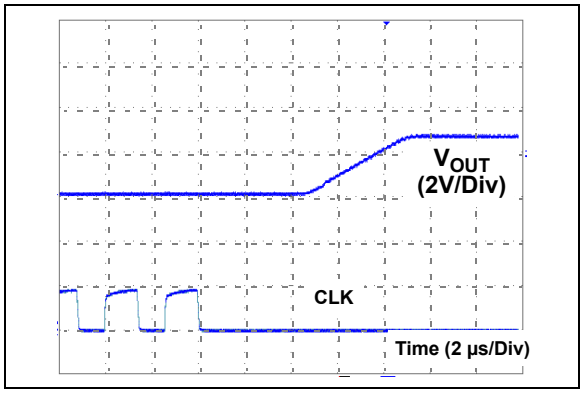


FIGURE 2-24: *Exiting Power Down Mode.*

NOTES:.

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP4725		Name	Description
SOT-23	DFN		
1	6	V_{OUT}	Analog Output Voltage
2	5	V_{SS}	Ground Reference
3	4	V_{DD}	Supply Voltage
4	3	SDA	I^2C Serial Data
5	2	SCL	I^2C Serial Clock Input
6	1	A0	I^2C Address Bit Selection pin (A0 bit). This pin can be tied to V_{SS} or V_{DD}, or can be actively driven by the digital logic levels. The logic state of this pin determines what the A0 bit of the I^2C address bits should be.
—	7	EP	Exposed Pad (**Note 1**)

Note 1: The DFN package has a contact on the bottom of the package. This contact is conductively connected to the die substrate, and therefore should be unconnected or connected to the same ground as the device's V_{SS} pin.

3.1 Analog Output Voltage (V_{OUT})

V_{OUT} is an analog output voltage from the DAC device. The DAC output amplifier drives this pin with a range of V_{SS} to V_{DD}.

3.2 Supply Voltage (V_{DD} or V_{SS})

V_{DD} is the power supply pin for the device. The voltage at the V_{DD} pin is used as the supply input as well as the DAC reference input. The power supply at the V_{DD} pin should be as clean as possible for good DAC performance.

This pin requires an appropriate bypass capacitor of about 0.1 µF (ceramic) to ground. An additional 10 µF capacitor (tantalum) in parallel is also recommended to further attenuate high frequency noise present in application boards. The supply voltage (V_{DD}) must be maintained in the 2.7V to 5.5V range for specified operation.

V_{SS} is the ground pin and the current return path of the device. The V_{SS} pin must be connected to a ground plane through a low impedance connection. If an analog ground path is available in the application PCB (printed circuit board), it is highly recommended that the V_{SS} pin be tied to the analog ground path or isolated within an analog ground plane of the circuit board.

3.3 Serial Data Pin (SDA)

SDA is the serial data pin of the I^2C interface. The SDA pin is used to write or read the DAC register and EEPROM data. The SDA pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor from the V_{DD} line to the SDA pin. Except for START and STOP conditions, the data on the SDA pin must be stable during the high period of the clock. The high or low state of the SDA pin can only change when the clock signal on the SCL pin is low. Refer to **Section 7.0 "I^2C Serial Interface Communication"** for more details of I^2C Serial Interface communication.

3.4 Serial Clock Pin (SCL)

SCL is the serial clock pin of the I^2C interface. The MCP4725 acts only as a slave and the SCL pin accepts only external serial clocks. The input data from the Master device is shifted into the SDA pin on the rising edges of the SCL clock and output from the MCP4725 occurs at the falling edges of the SCL clock. The SCL pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor from the V_{DD} line to the SCL pin. Refer to **Section 7.0 "I^2C Serial Interface Communication"** for more details of I^2C Serial Interface communication.

3.5 Device Address Selection Pin (A0)

This pin is used to select the A0 address bit by the user. The user can tie this pin to V_{SS} (logic '0'), or V_{DD} (logic '1'), or can be actively driven by the digital logic levels, such as the I^2C Master Output. See **Section 7.2 "Device Addressing"** for more details of the address bits.

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4.0 TERMINOLOGY

4.1 Resolution

The resolution is the number of DAC output states that divide the full scale range. For the 12-bit DAC, the resolution is 2^{12} or the DAC code ranges from 0 to 4095.

4.2 LSB

The least significant bit or the ideal voltage difference between two successive codes.

EQUATION 4-1:

$$LSB_{Ideal} = \frac{V_{REF}}{2^n} = \frac{(V_{Full\ Scale} - V_{Zero\ Scale})}{2^n - 1}$$

Where:

V_{REF}	=	The reference voltage = V_{DD} in the MCP4725. This V_{REF} is the ideal full scale voltage range
n	=	The number of digital input bits. (n = 12 for MCP4725)

4.3 Integral Nonlinearity (INL) or Relative Accuracy

INL error is the maximum deviation between an actual code transition point and its corresponding ideal transition point (straight line). Figure 2-5 shows the INL curve of the MCP4725. The end-point method is used for the calculation. The INL error at a given input DAC code is calculated as:

EQUATION 4-2:

$$INL = \frac{(V_{OUT} - V_{Ideal})}{LSB}$$

Where:

V_{Ideal}	=	Code*LSB
V_{OUT}	=	The output voltage measured at the given input code

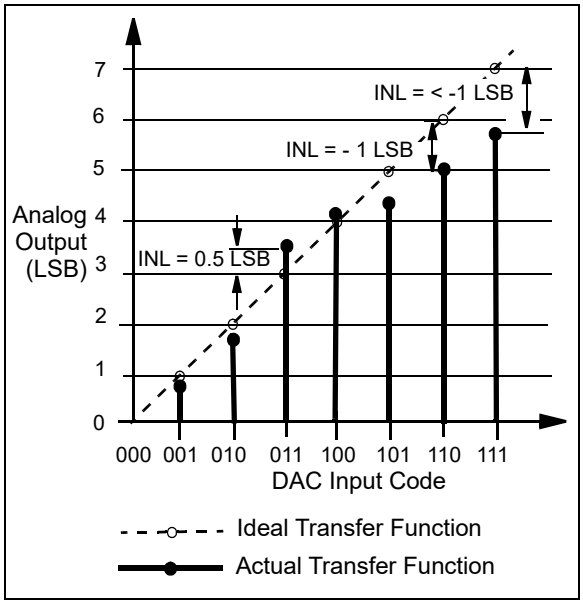


FIGURE 4-1: *INL Accuracy.*

4.4 Differential Nonlinearity (DNL)

Differential nonlinearity error (Figure 4-2) is the measure of step size between codes in actual transfer function. The ideal step size between codes is 1 LSB. A DNL error of zero would imply that every code is exactly 1 LSB wide. If the DNL error is less than 1 LSB, the DAC guarantees monotonic output and no missing codes. The DNL error between any two adjacent codes is calculated as follows:

EQUATION 4-3:

$$DNL = \frac{\Delta V_{OUT} - LSB}{LSB}$$

Where:

ΔV_{OUT}	=	The measured DAC output voltage difference between two adjacent input codes.

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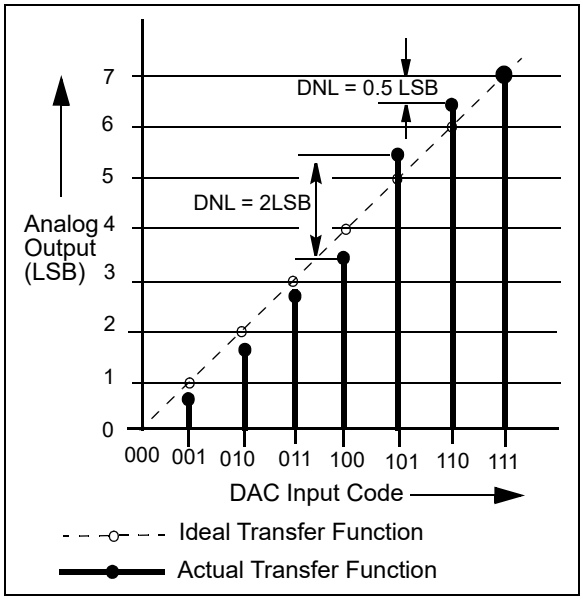


FIGURE 4-2: *DNL Accuracy.*

4.5 Offset Error

Offset error (Figure 4-3) is the deviation from zero voltage output when the digital input code is zero. This error affects all codes by the same amount. In the MCP4725, the offset error is not trimmed at the factory. However, it can be calibrated by software in application circuits.

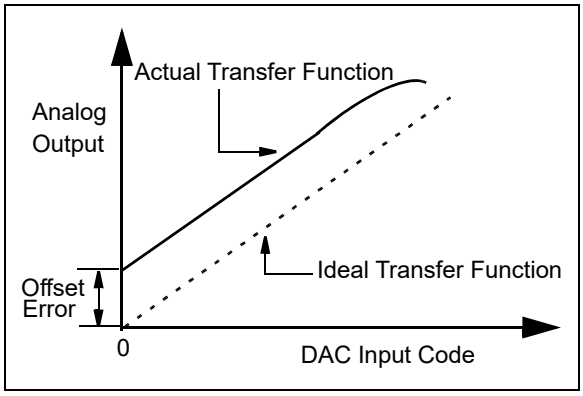


FIGURE 4-3: *Offset Error.*

4.6 Gain Error

Gain error (see Figure 4-4) is the difference between the actual full scale output voltage from the ideal output voltage on the transfer curve. The gain error is calculated after nullifying the offset error, or full scale error minus the offset error.

The gain error indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. The gain error is usually expressed as percent of full scale range (% of FSR) or in LSB.

In the MCP4725, the gain error is not calibrated at the factory and most of the gain error is contributed by the output op amp saturation near the code range beyond 4000. For the applications which need the gain error specification less than 1% maximum, the user may consider using the DAC code range between 100 and 4000 instead of using full code range (code 0 to 4095). The DAC output of the code range between 100 and 4000 is much linear than full scale range (0 to 4095). The gain error can be calibrated by software in applications.

4.7 Full Scale Error (FSE)

Full scale error (Figure 4-4) is the sum of offset error plus gain error. It is the difference between the ideal and measured DAC output voltage with all bits set to one (DAC input code = FFFh).

EQUATION 4-4:

$$FSE = \frac{(V_{OUT} - V_{Ideal})}{LSB}$$

Where:

V_{Ideal} = $(V_{REF})\ (1 - 2^{-n}) - V_{OFFSET}$

V_{REF} = The reference voltage.
$V_{REF} = V_{DD}$ in the MCP4725

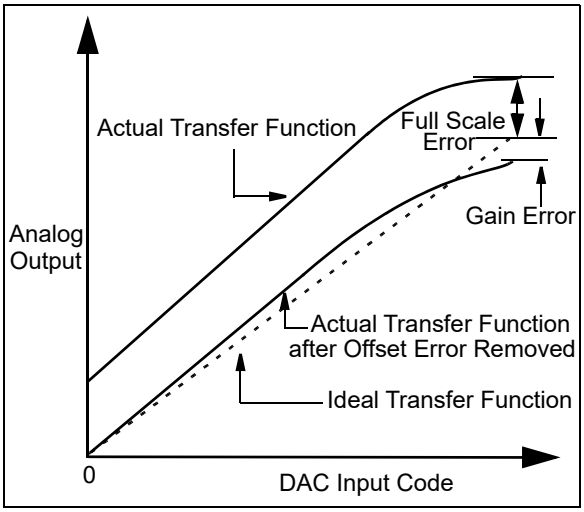


FIGURE 4-4: *Gain Error and Full Scale Error.*

4.8 Gain Error Drift

Gain error drift is the variation in gain error due to a change in ambient temperature. The gain error drift is typically expressed in ppm/°C.

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4.9 Offset Error Drift

Offset error drift is the variation in offset error due to a change in ambient temperature. The offset error drift is typically expressed in ppm/^{o}C.

4.10 Settling Time

The Settling time is the time delay required for the DAC output to settle to its new output value from the start of code transition, within specified accuracy. In the MCP4725, the settling time is a measure of the time delay until the DAC output reaches its final value (within 0.5 LSB) when the DAC code changes from 400h to C00h.

4.11 Major-Code Transition Glitch

Major-code transition glitch is the impulse energy injected into the DAC analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-Sec. and is measured when the digital code is changed by 1 LSB at the major carry transition (Example: 011...111 to 100... 000, or 100... 000 to 011 ... 111).

4.12 Digital Feedthrough

Digital feedthrough is the glitch that appears at the analog output caused by coupling from the digital input pins of the device. It is specified in nV-Sec. and is measured with a full scale change on the digital input pins (Example: 000... 000 to 111... 111, or 111... 111 to 000... 000). The digital feedthrough is measured when the DAC is not being written to the register.

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5.0 GENERAL DESCRIPTION

The MCP4725 is a single channel buffered voltage output 12-bit DAC with nonvolatile memory (EEPROM). The user can store configuration register bits (2 bits) and DAC input data (12 bits) in nonvolatile EEPROM (14 bits) memory.

When the device is powered on first, it loads the DAC code from the EEPROM and outputs the analog output accordingly with the programmed settings. The user can reprogram the EEPROM or DAC register any time.

The device uses a resistor string architecture. DAC's output is buffered with a low power precision amplifier. This output amplifier provides low offset voltage and low noise, as well as rail-to-rail output. The amplifier can also provide high source currents (V_{OUT} pin to V_{SS}).

The DAC can be configured to normal or power saving power-down mode by setting the configuration register bits.

The device uses a two-wire I^2C compatible serial interface and operates from a single power supply ranging from 2.7V to 5.5V.

5.1 Output Voltage

The input coding to the MCP4725 device is unsigned binary. The output voltage range is from 0V to V_{DD}. The output voltage is given in Equation 5-1:

EQUATION 5-1:

$$V_{OUT} = \frac{(V_{REF} \times D_n)}{4096}$$

Where:

V_{REF} = V_{DD}
D_n = Input code

5.1.1 OUTPUT AMPLIFIER

The DAC output is buffered with a low-power, precision CMOS amplifier. This amplifier provides low offset voltage and low noise. The output stage enables the device to operate with output voltages close to the power supply rails. Refer to **Section 1.0 "Electrical Characteristics"** for range and load conditions.

The output amplifier can drive the resistive and high capacitive loads without oscillation. The amplifier can provide maximum load current as high as 25 mA which is enough for most of a programmable voltage reference applications.

5.1.2 DRIVING RESISTIVE AND CAPACITIVE LOADS

The MCP4725 output stage is capable of driving loads up to 1000 pF in parallel with 5 kΩ load resistance. Figure 2-15 shows the V_{OUT} vs. Resistive Load. V_{OUT} drops slowly as the load resistance decreases after about 3.5 kΩ.

5.2 LSB SIZE

One LSB is defined as the ideal voltage difference between two successive codes. (see Equation 4-1). Table 5-1 shows an example of the LSB size over full scale range (V_{DD}).

TABLE 5-1: LSB SIZES FOR MCP4725 (EXAMPLE)

Full Scale Range (V_{DD})	LSB Size	Condition
3.0V	0.73 mV	3V / 4096
5.0V	1.22 mV	5V / 4096

5.3 Voltage Reference

The MCP4725 device uses the V_{DD} as its voltage reference. Any variation or noises on the V_{DD} line can affect directly on the DAC output. The V_{DD} needs to be as clean as possible for accurate DAC performance.

5.4 Reset Conditions

In the Reset conditions, the device uploads the EEPROM data into the DAC register. The device can be reset by two independent events: (a) by POR or (b) by I^2C General Call Reset Command.

The factory default settings for the EEPROM prior to shipment are shown in Table 5-3 (set for a middle scale output). The user can rewrite or read the DAC register or EEPROM anytime after the Power-On-Reset event.

5.4.1 POWER-ON-RESET

The device's internal Power-On-Reset (POR) circuit ensures that the device powers up in a defined state.

If the power supply voltage is less than the POR threshold (V_{POR} = 2V, typical), all circuits are disabled and there will be no DAC output. When the V_{DD} increases above the V_{POR}, the device takes a reset state. During the reset period, the device uploads all configuration and DAC input codes from EEPROM. The DAC output will be the same as for the value last stored in the EEPROM. This enables the device returns to the same state that it was at the last write to the EEPROM before it was powered off.

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5.4.2 V_{DD} RAMP RATE AND EEPROM

The MCP4725 uploads the EEPROM data to the DAC register during power-up sequence. However, if the V_{DD} ramp rate is too slow (<1 V/ms), the device may not be able to load the EEPROM data to the DAC register. Therefore, the DAC output that is corresponding to the current EEPROM data may not available to the output pin. It is highly recommended to send a General Call Reset Command (see **Section 7.3.1 "General call reset"**) after power-up. This command will reset the device at a stable V_{DD} and make the DAC output available immediately using the EEPROM data.

5.5 Normal and Power-Down Modes

The device has two modes of operation: Normal mode and power-down mode. The mode is selected by programming the power-down bits (PD1 and PD0) in the Configuration register. The user can also program the two power-down bits in nonvolatile EEPROM memory.

When the normal mode is selected, the device operates a normal digital-to-analog conversion. If the power-down mode is selected, the device enters a power saving condition by shutting down most of the internal circuits. During the power-down mode, all internal circuits except the I^2C interface are disabled and there is no data conversion event, and no V_{OUT} is available. The device also switches the output stage from the output of the amplifier to a known resistive load. The value of the resistive load is determined by the state of the power-down bits (PD1 and PD0). Table 5-2 shows the outcome of the power-down bit and the resistive load.

During the power-down mode, the device draws about 60 nA (typical). Although most of internal circuits are shutdown, the serial interface remains active in order to receive the I^2C command.

The device exits the power-down mode immediately when (a) it receives a new write command for normal mode or (b) it receives an I^2C General Call Wake-Up Command.

When the DAC operation mode is changed from power-down to normal mode, the output settling time takes less than 10 µs, but greater than the standard Active mode settling time (6 µs, typical).

TABLE 5-2: POWER-DOWN BITS

PD1	PD0	Function
0	0	Normal Mode
0	1	1 kΩ resistor to ground (1)
1	0	100 kΩ resistor to ground (1)
1	1	500 kΩ resistor to ground (1)

Note 1: In the power-down mode: V_{OUT} is off and most of internal circuits are disabled.

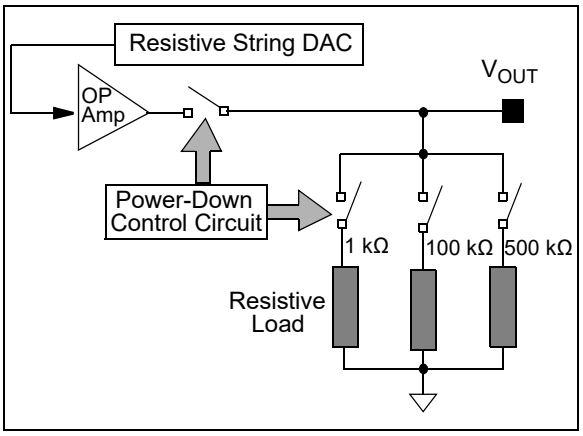


FIGURE 5-1: *Output Stage for Power-Down Mode.*

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5.6 Nonvolatile EEPROM Memory

The MCP4725 device has a 14-bit wide EEPROM memory to store configuration bit (2 bits) and DAC input data (12 bits). These bits are readable and re-writable with I^2C interface commands. The device has an on-chip charge pump circuit to write the EEPROM memory bits without using an external program voltage.

The EEPROM writing operation is initiated when the device receives an EEPROM write command (C2 = 0, C1 = 1, C0 = 1). The configuration and writing data bits are transferred to the EEPROM memory block. A status bit, RDY/$\overline{BSY}$, stays low during the EEPROM writing and goes high as the write operation is completed. While the RDY/$\overline{BSY}$ bit is low (during the EEPROM writing), any new write command is ignored (for EEPROM or DAC register). Table 5-3 shows the EEPROM bits and factory default settings. Table 5-4 shows the DAC input register bits of the MCP4725.

TABLE 5-3: EEPROM MEMORY AND FACTORY DEFAULT SETTINGS (TOTAL NUMBER OF BITS: 14 BITS)

Bit Name	PD1	PD0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Function	Power-Down Select (2 bits)		DAC Input Data (12 bits)											
Factory Default Value	0	0 (1)	1 (2)	0	0	0	0	0	0	0	0	0	0	0

Note 1: See Table 5-2 for details.

2: Bit D11 = '1' (while all other bits are "0") enables the device to output 0.5 * V_{DD} (= middle scale output).

TABLE 5-4: DAC REGISTER

Bit Name	C2	C1	C0	RDY/$\overline{BSY}$	POR	PD1	PD0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Function	Command Type			(1)		Power-Down Select		Data (12 bits)											

Note 1: Write EEPROM status indication bit (0:EEPROM write is not completed. 1:EEPROM write is complete.)

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6.0 THEORY OF OPERATION

When the device is connected to the I^2C bus line, the device is working as a slave device. The Master (MCU) can write/read the DAC input register or EEPROM using the I^2C interface command. The MCP4725 device address contains four fixed bits (1100 = device code) and three address bits (A2, A1, A0). The A2 and A1 bits are hard-wired during manufacturing, and A0 bit is determined by the logic state of A0 pin. The A0 pin can be connected to V_{DD} or V_{SS}, or actively driven by digital logic levels.

The following sections describe the communication protocol to send or read the data code and write/read the EEPROM using the I^2C interface. See **Section 7.0 "I2C Serial Interface Communication"**.

6.1 Write Commands

The write commands are used to load the configuration bits and DAC input code to the DAC register, or to write to the EEPROM of the device. The write command types are defined by using three write command type bits (C2, C1, C0). Table 6-2 shows the write command types and their functions. There are three command types for the MCP4725. The four "reserved" commands in Table 6-2 are for future use. The MCP4725 ignores the "reserved" commands. Write command protocol examples are shown in Figure 6-1 and Figure 6-2.

The input data code is coded as shown in Table 6-1. The MSB of the data is always transmitted first and the format is unipolar binary.

TABLE 6-1: INPUT DATA CODING

Input Code	Nominal Output Voltage (V)
111111111111 (FFFh)	V_{DD} - 1 LSB
111111111110 (FFEh)	V_{DD} - 2 LSB
000000000010 (002h)	2 LSB
000000000001 (001h)	1 LSB
000000000000 (000h)	0

6.1.1 WRITE COMMAND FOR FAST MODE (C2 = 0, C1 = 0, C0 = X, X = DON'T CARE)

The fast write command is used to update the DAC register. The data in the EEPROM of the device is not affected by this command. This command updates Power-Down mode selection bits (PD1 and PD0) and 12 bits of the DAC input code in the DAC register. Figure 6-1 shows an example of the fast write command for the MCP4725 device.

6.1.2 WRITE COMMAND FOR DAC INPUT REGISTER (C2 = 0, C1 = 1, C0 = 0)

In MCP4725, this command performs the same function as the Fast Mode command in **Section 6.1.1 "Write Command for Fast mode (C2 = 0, C1 = 0, C0 = X, X = Don't Care)"**. Figure 6-2 shows the write command protocol for the MCP4725.

As shown in Figure 6-2, the D11 - D0 bits in the third and fourth bytes are DAC input data. The last 4 bits (X, X, X, X) in the fourth byte are don't care bits.

The device executes the Master's write command after receiving the last byte (4th byte). The Master can send a STOP bit to terminate the current sequence, or send a Repeated START bit followed by an address byte. If the device receives three data bytes continuously after the 4th byte, it updates from the 2nd to the 4th data bytes with the last three input data bytes.

The contents of the register are updated at the end of the 4th byte. The device ignores any partially received data bytes if the I^2C communication with the Master ends before completing the 4th byte.

6.1.3 WRITE COMMAND FOR DAC INPUT REGISTER AND EEPROM (C2 = 0, C1 = 1, C0 = 1)

When the device receives this command, it (a) loads the configuration and data bits to the DAC register, and (b) also writes the EEPROM. When the device is writing the EEPROM, the RDY/$\overline{BSY}$ bit goes low and stays low until the EEPROM write operation is completed. The state of the RDY/$\overline{BSY}$ bit can be monitored by a read command. Figure 6-2 shows the details of the this write command protocol and Figure 6-3 shows the details of the read command.

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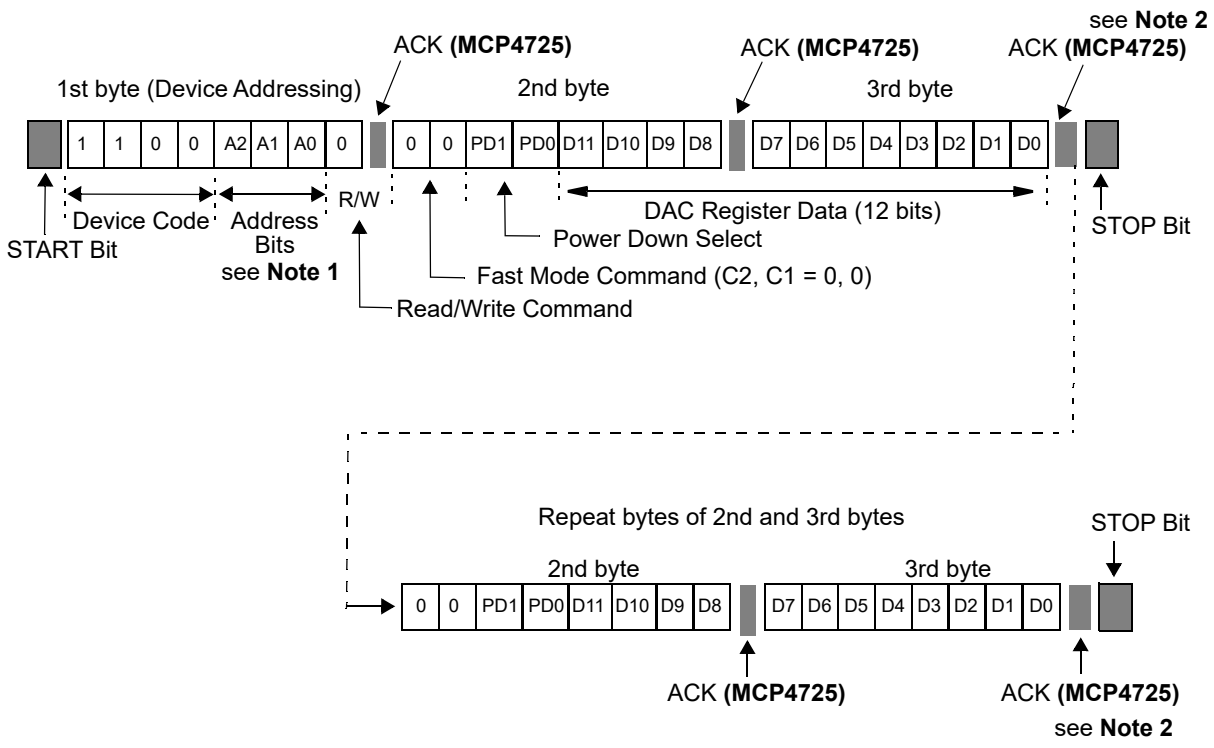
TABLE 6-2: WRITE COMMAND TYPE

C2	C1	C0	Command Name	Function
0	0	X	Fast Mode	This command is used to change the DAC register. EEPROM is not affected
0	0	X	“	“
0	1	0	Write DAC Register	Load configuration bits and data code to the DAC Register
0	1	1	Write DAC Register and EEPROM	(a) Load configuration bits and data code to the DAC Register and (b) also write the EEPROM
1	0	0	Reserved	Reserved for future use
1	0	1	Reserved	Reserved for future use
1	1	0	Reserved	Reserved for future use
1	1	1	Reserved	Reserved for future use

Note 1: X = Don’t Care. Fast Mode does not use C0 bit.

2: The MCP4725 ignores the “Reserved” commands.

Write DAC Register using Fast Mode Write Command: (C2, C1) = (0, 0)



Note 1: A2 and A1 bits are programmed at the factory by hard-wired, and A0 bit is determined by the logic state of A0 pin.

2: The device updates V_{OUT} at the falling edge of the ACK pulse of the 3rd byte.

FIGURE 6-1: *Fast Mode Write Command.*

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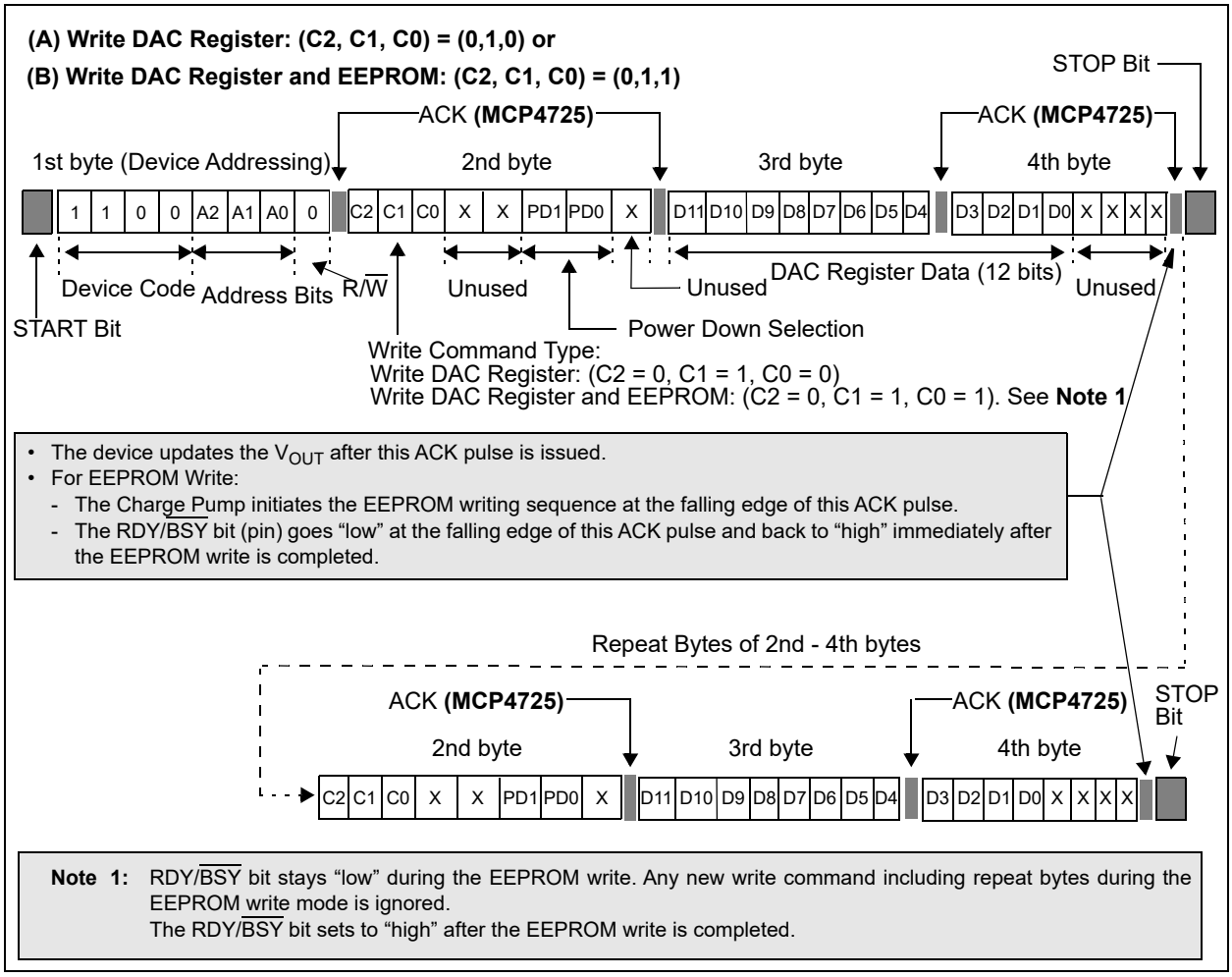
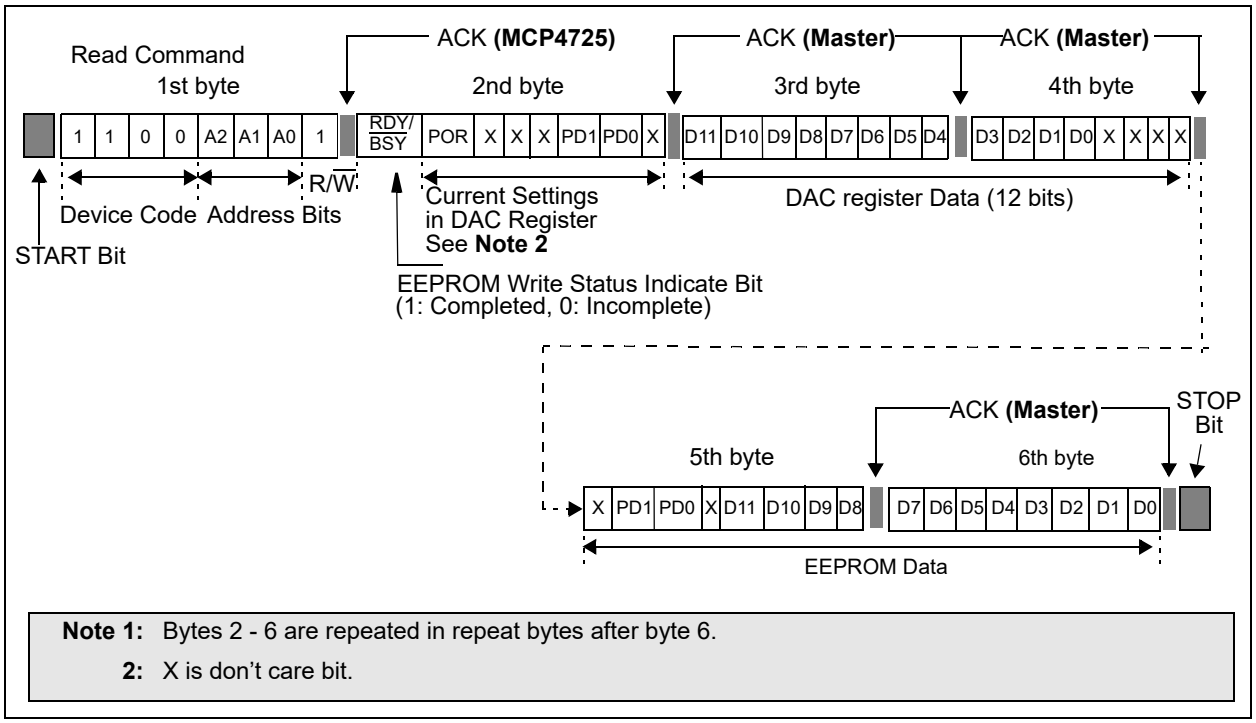


FIGURE 6-2: *Write Commands for DAC Input Register and EEPROM.*

6.2 READ COMMAND

If the R/$\overline{W}$ bit is set to a logic “high”, then the device outputs on SDA pin, the DAC register and EEPROM data. Figure 6-3 shows an example of reading the register and EEPROM data. The 2nd byte in Figure 6-3 indicates the current condition of the device operation. The RDY/$\overline{BSY}$ bit indicates EEPROM writing status. The RDY/$\overline{BSY}$ bit stays low during EEPROM writing and high when the writing is completed.



Note 1: Bytes 2 - 6 are repeated in repeat bytes after byte 6.

2: X is don’t care bit.

FIGURE 6-3: *Read Command and Output Data Format.*

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7.0 I²C SERIAL INTERFACE COMMUNICATION

7.1 OVERVIEW

The MCP4725 device uses a two-wire I²C serial interface that can operate on a standard, fast or high speed mode. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access and generates the START and STOP conditions. The MCP4725 device works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated. An example of hardware connection diagram is shown in Figure 8-1. Communication is initiated by the master (microcontroller) which sends the START bit, followed by the slave address byte. The first byte transmitted is always the slave address byte, which contains the device code, the address bits, and the R/$\overline{W}$ bit. The device code for the MCP4725 device is `1100`.

When the device receives a read command (R/W = `1`), it transmits the contents of the DAC input register and EEPROM. A non-acknowledge (NAK) or repeated START bit can be transmitted at any time. See Figure 6-3 for the read operation example. If writing to the device (R/W = `0`), the device will expect write command type bits in the following byte. See Figure 6-1 and Figure 6-2 for the write operation examples.

The MCP4725 supports all three I²C operating modes:

- Standard Mode: bit rates up to 100 kbit/s
- Fast Mode: bit rates up to 400 kbit/s
- High Speed Mode (HS mode): bit rates up to 3.4 Mbit/s

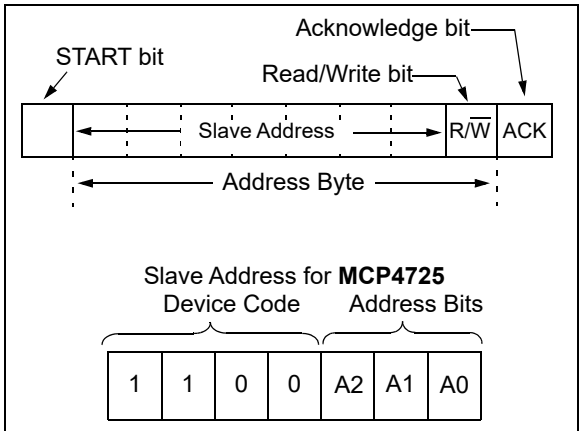
Refer to the NXP I²C document, located here https://www.nxp.com/docs/en/user-guide/UM10204.pdf for more details of the I²C specifications.

7.2 Device Addressing

The address byte is the first byte received following the START condition from the master device. The first part of the address byte consists of a 4-bit device code which is set to `1100` for the MCP4725. The device code is followed by three address bits (A2, A1, A0) which are programmed as follows:

- The choice of A2 and A1 bits are provided by the customer as part of the ordering process. These bits are then programmed (hard-wired) during manufacturing
- The A2 and A1 are programmed to '`00`' (default), if not requested by customer
- A0 bit is determined by the logic state of A0 pin. The A0 pin can be tied to V_{DD} or V_{SS}, or can be actively driven by digital logic levels. The advantage of using the A0 pin is that the users can control the A0 bit on their application PCB circuit and also two identical MCP4725 devices can be used on the same bus line.

When the device receives an address byte, it compares the logic state of the A0 pin with the A0 address bit received before responding with the acknowledge bit. The logic state of the A0 pin needs to be set prior to the interface communication.



Note: A2 and A1: Programmed (hard-wired) at the factory. Please Contact Microchip Technology Inc. for A2 and A1 programming options.
A0: Use the logic level state of A0 pin.

FIGURE 7-1: *Device Addressing.*

7.3 General Call

The MCP4725 device acknowledges the general call address (0x00 in the first byte). The meaning of the general call address is always specified in the second byte (see Figure 7-2). The I²C specification does not allow to use "00000000" (00h) in the second byte. Please refer to the NXP I²C document for more details of the General Call specifications. The MCP4725 supports the following general calls:

7.3.1 GENERAL CALL RESET

The general reset occurs if the second byte is "00000110" (06h). At the acknowledgment of this byte, the device will abort current conversion and perform an internal reset similar to a power-on-reset (POR). Immediately after this reset event, the device uploads the contents of the EEPROM into the DAC register.

7.3.2 GENERAL CALL WAKE-UP

If the second byte is "00001001" (09h), the device will reset the power-down bits. After receiving this command, the power-down bits of the DAC register are set to a normal operation (PD1, PD2 = 0,0). The power-down bit settings in EEPROM are not affected.

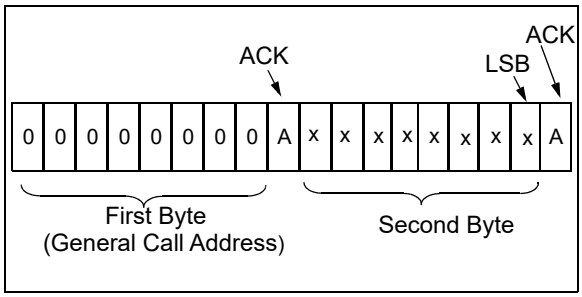


FIGURE 7-2: *General Call Address Format.*

7.4 High-Speed (HS) Mode

The I²C specification requires that a high-speed mode device must be 'activated' to operate in high-speed (3.4 Mbit/s) mode. This is done by sending a special address byte of 00001XXX following the START bit. The XXX bits are unique to the high-speed (HS) mode Master. This byte is referred to as the high-speed (HS) Master Mode Code (HSMMC). The MCP4725 device does not acknowledge this byte. However, upon receiving this command, the device switches to HS mode and can communicate at up to 3.4 Mbit/s on SDA and SCL lines. The device will switch out of the HS mode on the next STOP condition.

For more information on the HS mode, or other I²C modes, please refer to the NXP I²C specification.

7.5 I²C BUS CHARACTERISTICS

The I²C specification defines the following bus protocol:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined using Figure 7-3.

7.5.1 BUS NOT BUSY (A)

Both data and clock lines remain HIGH.

7.5.2 START DATA TRANSFER (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition.

All commands must be preceded by a START condition.

7.5.3 STOP DATA TRANSFER (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

7.5.4 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition.

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7.5.5 ACKNOWLEDGE

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must send an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave.

In this case, the slave (MCP4725) will leave the data line HIGH to enable the master to generate the STOP condition.

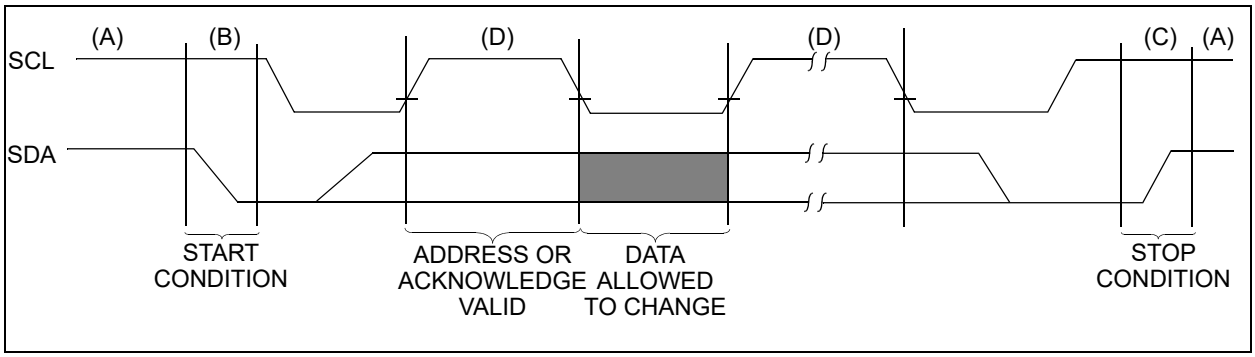


FIGURE 7-3: *Data Transfer Sequence On The Serial Bus.*

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TABLE 7-1: I^2C SERIAL TIMING SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, all limits are specified for T_A = -40 to +85°C, V_{DD} = +2.7V to +5.0V, V_{SS} = 0V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Standard Mode						
Clock frequency	f_{SCL}	0	—	100	kHz	
Clock high time	T_{HIGH}	4000	—	—	ns	
Clock low time	T_{LOW}	4700	—	—	ns	
SDA and SCL rise time	T_R	—	—	1000	ns	From V_{IL} to V_{IH} **(Note 1)**
SDA and SCL fall time	T_F	—	—	300	ns	From V_{IH} to V_{IL} **(Note 1)**
START condition hold time	$T_{HD:STA}$	4000	—	—	ns	After this period, the first clock pulse is generated.
(Repeated) START condition setup time	$T_{SU:STA}$	4700	—	—	ns	
Data hold time	$T_{HD:DAT}$	0	—	3450	ns	**Note 3**
Data input setup time	$T_{SU:DAT}$	250	—	—	ns	
STOP condition setup time	$T_{SU:STO}$	4000	—	—	ns	
Output valid from clock	T_{AA}	0	—	3750	ns	**Notes 2 and 3**
Bus free time	T_{BUF}	4700	—	—	ns	Time between START and STOP conditions.
Fast Mode						
Clock frequency	T_{SCL}	0	—	400	kHz	
Clock high time	T_{HIGH}	600	—	—	ns	
Clock low time	T_{LOW}	1300	—	—	ns	
SDA and SCL rise time	T_R	20 + 0.1Cb	—	300	ns	From V_{IL} to V_{IH} **(Note 1)**
SDA and SCL fall time	T_F	20 + 0.1Cb	—	300	ns	From V_{IH} to V_{IL} **(Note 1)**
START condition hold time	$T_{HD:STA}$	600	—	—	ns	After this period, the first clock pulse is generated
(Repeated) START condition setup time	$T_{SU:STA}$	600	—	—	ns	
Data hold time	$T_{HD:DAT}$	0	—	900	ns	**Note 4**
Data input setup time	$T_{SU:DAT}$	100	—	—	ns	
STOP condition setup time	$T_{SU:STO}$	600	—	—	ns	
Output valid from clock	T_{AA}	0	—	1200	ns	**Notes 2 and 3**
Bus free time	T_{BUF}	1300	—	—	ns	Time between START and STOP conditions.

Note 1: This parameter is ensured by characterization and not 100% tested.

2: This specification is not a part of the I2C specification. This specification is equivalent to the Data Hold Time ($T_{HD:DAT}$) plus SDA Fall (or rise) time: $T_{AA} = T_{HD:DAT} + T_F$ (OR T_R).

3: If this parameter is too short, it can create an unintended START or STOP condition to other devices on the same bus line. If this parameter is too long, Clock Low time (T_{LOW}) can be affected.

4: For Data Input: This parameter must be longer than t_{SP}. If this parameter is too long, the Data Input Setup ($T_{SU:DAT}$) or Clock Low time (T_{LOW}) can be affected.
For Data Output: This parameter is characterized, and tested indirectly by testing T_{AA} parameter.

5: All timing parameters in high-speed modes are tested at V_{DD} = 5V.

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TABLE 7-1: I^2C SERIAL TIMING SPECIFICATIONS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all limits are specified for T_A = -40 to +85°C, V_{DD} = +2.7V to +5.0V, V_{SS} = 0V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
High Speed Mode (Note 5)						
Clock frequency	f_{SCL}	0	—	3.4	MHz	C_b = 100 pF
		0	—	1.7	MHz	C_b = 400 pF
Clock high time	T_{HIGH}	60	—	—	ns	C_b = 100 pF, f_{SCL} = 3.4 MHz
		120	—	—	ns	C_b = 400 pF, f_{SCL} = 1.7 MHz
Clock low time	T_{LOW}	160	—	—	ns	C_b = 100 pF, f_{SCL} = 3.4 MHz
		320	—	—	ns	C_b = 400 pF, f_{SCL} = 1.7 MHz
SCL rise time (Note 1)	$T_{R:SCL}$	—	—	40	ns	From V_{IL} to V_{IH}, C_b = 100 pF, f_{SCL} = 3.4 MHz
		—	—	80	ns	From V_{IL} to V_{IH}, C_b = 400 pF, f_{SCL} = 1.7 MHz
SCL fall time (Note 1)	$T_{F:SCL}$	—	—	40	ns	From V_{IH} to V_{IL}, C_b = 100 pF, f_{SCL} = 3.4 MHz
		—	—	80	ns	From V_{IH} to V_{IL}, C_b = 400 pF, f_{SCL} = 1.7 MHz
SDA rise time (Note 1)	$T_{R:DAT}$	—	—	80	ns	From V_{IL} to V_{IH}, C_b = 100 pF, f_{SCL} = 3.4 MHz
		—	—	160	ns	From V_{IL} to V_{IH}, C_b = 400 pF, f_{SCL} = 1.7 MHz
SDA fall time (Note 1)	$T_{F:DAT}$	—	—	80	ns	From V_{IH} to V_{IL}, C_b = 100 pF, f_{SCL} = 3.4 MHz
		—	—	160	ns	From V_{IH} to V_{IL}, C_b = 400 pF, f_{SCL} = 1.7 MHz
Data hold time (Note 4)	$T_{HD:DAT}$	0	—	70	ns	C_b = 100 pF, f_{SCL} = 3.4 MHz
		0	—	150	ns	C_b = 400 pF, f_{SCL} = 1.7 MHz
Output valid from clock (Notes 2 and 3)	T_{AA}	—	—	150	ns	C_b = 100 pF, f_{SCL} = 3.4 MHz
		—	—	310	ns	C_b = 400 pF, f_{SCL} = 1.7 MHz
START condition hold time	$T_{HD:STA}$	160	—	—	ns	After this period, the first clock pulse is generated
START (Repeated) condition setup time	$T_{SU:STA}$	160	—	—	ns	
Data input setup time	$T_{SU:DAT}$	10	—	—	ns	
STOP condition setup time	$T_{SU:STO}$	160	—	—	ns	

Note 1: This parameter is ensured by characterization and not 100% tested.

2: This specification is not a part of the I2C specification. This specification is equivalent to the Data Hold Time ($T_{HD:DAT}$) plus SDA Fall (or rise) time: $T_{AA} = T_{HD:DAT} + T_F$ (OR T_R).

3: If this parameter is too short, it can create an unintended START or STOP condition to other devices on the same bus line. If this parameter is too long, Clock Low time (T_{LOW}) can be affected.

4: For Data Input: This parameter must be longer than t_{SP}. If this parameter is too long, the Data Input Setup ($T_{SU:DAT}$) or Clock Low time (T_{LOW}) can be affected.
For Data Output: This parameter is characterized, and tested indirectly by testing T_{AA} parameter.

5: All timing parameters in high-speed modes are tested at V_{DD} = 5V.

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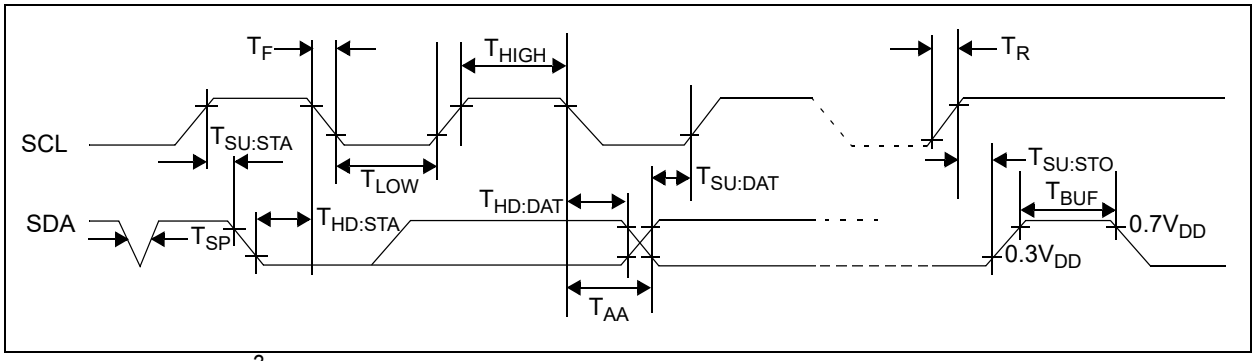


FIGURE 7-4: *I^2C Bus Timing Data.*

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8.0 TYPICAL APPLICATIONS

The MCP4725 device is one of Microchip's latest DAC device family with nonvolatile EEPROM memory. The device is a general purpose resistive string DAC intended to be used in applications where a precision, and low power DAC with moderate bandwidth is required.

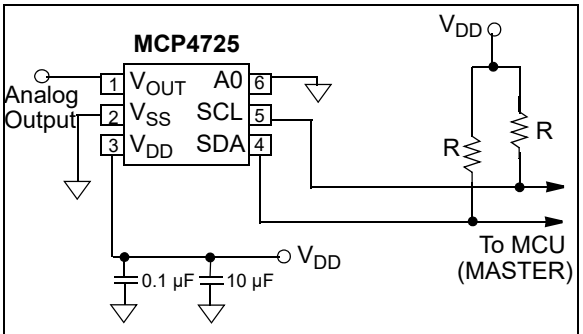
Since the device includes nonvolatile EEPROM memory, the user can use this device for applications that require the output to return to the previous set-up value on subsequent power-ups.

Applications generally suited for the MCP4725 device family include:

- Set Point or Offset Trimming
- Sensor Calibration
- Portable Instrumentation (Battery Powered)
- Motor Speed Control

8.1 Connecting to I²C BUS using Pull-Up Resistors

The SCL and SDA pins of the MCP4725 are open-drain configurations. These pins require a pull-up resistor as shown in Figure 8-1. The value of these pull-up resistors depends on the operating speed (standard, fast, and high speed) and loading capacitance of the I^2C bus line. Higher value of pull-up resistor consumes less power, but increases the signal transition time (higher RC time constant) on the bus. Therefore, it can limit the bus operating speed. The lower resistor value, on the other hand, consumes higher power, but allows higher operating speed. If the bus line has higher capacitance due to long bus line or high number of devices connected to the bus, a smaller pull-up resistor is needed to compensate the long RC time constant. The pull-up resistor is typically chosen between 1 kΩ and 10 kΩ ranges for standard and fast modes, and less than 1 kΩ for high speed mode.



Note 1: R is the pull-up resistor. Typically 1 ~ 10 kΩ

2: A0 can be tied to V_{SS}, V_{DD} or driven by MCU

FIGURE 8-1: *I^2C Bus Interface Connection with A0 pin tied to V_{SS}.*

Two devices with the same A2 and A1 address bits can be connected to the same I^2C bus by utilizing the A0 address pin (Example: A0 pin of device A is tied to V_{DD}, and the other device's pin is tied to V_{SS}).

8.1.1 DEVICE CONNECTION TEST

The user can test the presence of the MCP4725 on the I^2C bus line without performing the data conversion. This test can be achieved by checking an acknowledge response from the MCP4725 after sending a read or write command. Here is an example using Figure 8-2:

(a) Set the R/$\overline{W}$ bit "HIGH" in the address byte.

(b) If the MCP4725 is connected to the I^2C bus line, it will then acknowledge by pulling SDA bus LOW during the ACK clock and then release the bus back to the I^2C Master.

(c) A STOP or repeated START bit can then be issued from the Master and I^2C communication can continue.

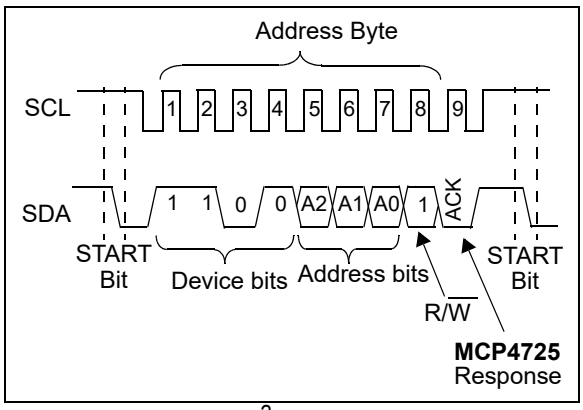


FIGURE 8-2: *I^2C Bus Connection Test.*

8.2 Using Nonvolatile EEPROM Memory

The user can store the DAC input code (12 bits) and power-down configuration bits (2 bits) in the internal nonvolatile EEPROM memory using the I^2C write command. The user can also read the EEPROM data using the I^2C read command. When the device is first powered after power is shut down, the device uploads the EEPROM contents to the DAC register automatically and provides the DAC output immediately. This feature is very useful in applications where the DAC device is used to provide set point or calibration data for other devices in the application system. The DAC will not lose the important system operational parameters due to the system power failure incidents. See **Section 5.6 "Nonvolatile EEPROM Memory"** for more details of the nonvolatile EEPROM memory.

8.3 Power Supply Considerations

The power supply to the device is used for both V_{DD} and DAC reference voltage. Any noise induced on the V_{DD} line can affect on the DAC performance. Typical application will require a bypass capacitor in order to filter out high frequency noise on the V_{DD} line. The noise can be induced onto the power supply's traces or as a result of changes on the DAC output. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 8-1 shows an example of using two bypass capacitors (a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor) in parallel on the V_{DD} line. These capacitors should be placed as close to the V_{DD} pin as possible (within 4 mm).

The power source should be as clean as possible. If the application circuit has separate digital and analog power supplies, the V_{DD} and V_{SS} pins of the MCP4725 should reside on the analog plane.

8.4 Layout Considerations

Inductively-coupled AC transients and digital switching noise from other devices can affect on DAC performance and DAC output signal integrity. Careful board layout will minimize these effects. Bench testing has shown that a multi-layer board utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving the performance that the MCP4725 is capable of providing. Particularly harsh environments may require shielding of critical signals. Separate digital and analog ground planes are recommended. In this case, the V_{SS} pin and the ground pins of the V_{DD} capacitors of the MCP4725 should be terminated to the analog ground plane.

8.5 Application Examples

The MCP4725 is a rail-to-rail output DAC designed to operate with a V_{DD} range of 2.7V to 5.5V. Its output amplifier is robust enough to drive common, small-signal loads directly, thus eliminating the cost and size of an external buffer for most applications.

8.5.1 DC SET POINT OR CALIBRATION

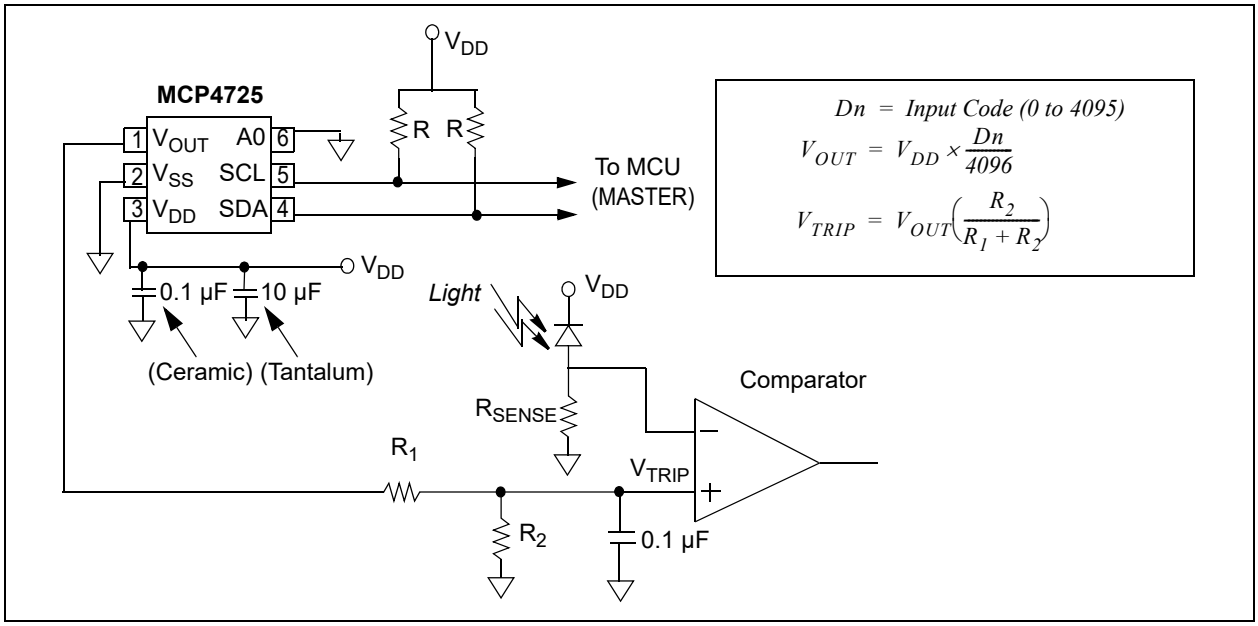
A common application for the MCP4725 is a digitally-controlled set point or a calibration of variable parameters such as sensor offset or bias point. Example 8-1 shows an example of the set point setting. Since the MCP4725 is a 12-bit DAC and uses the V_{DD} supply as a reference source, it provides a $V_{DD}/4096$ of resolution per step.

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8.5.2 DECREASING THE OUTPUT STEP SIZE

Calibrating the threshold of a diode, transistor or resistor may require a very small step size in the DAC output voltage. These applications may require about 200 µV of step resolution within 0.8V of range.

One method of achieving this small step resolution is using a voltage divider at the DAC output. An example is shown in Example 8-1. The step size of the DAC output is scaled down by the factor of the ratio of the voltage divider. Note that the bypass capacitor on the output of the voltage divider plays a critical function in attenuating the output noise of the DAC and the induced noise from the environment.

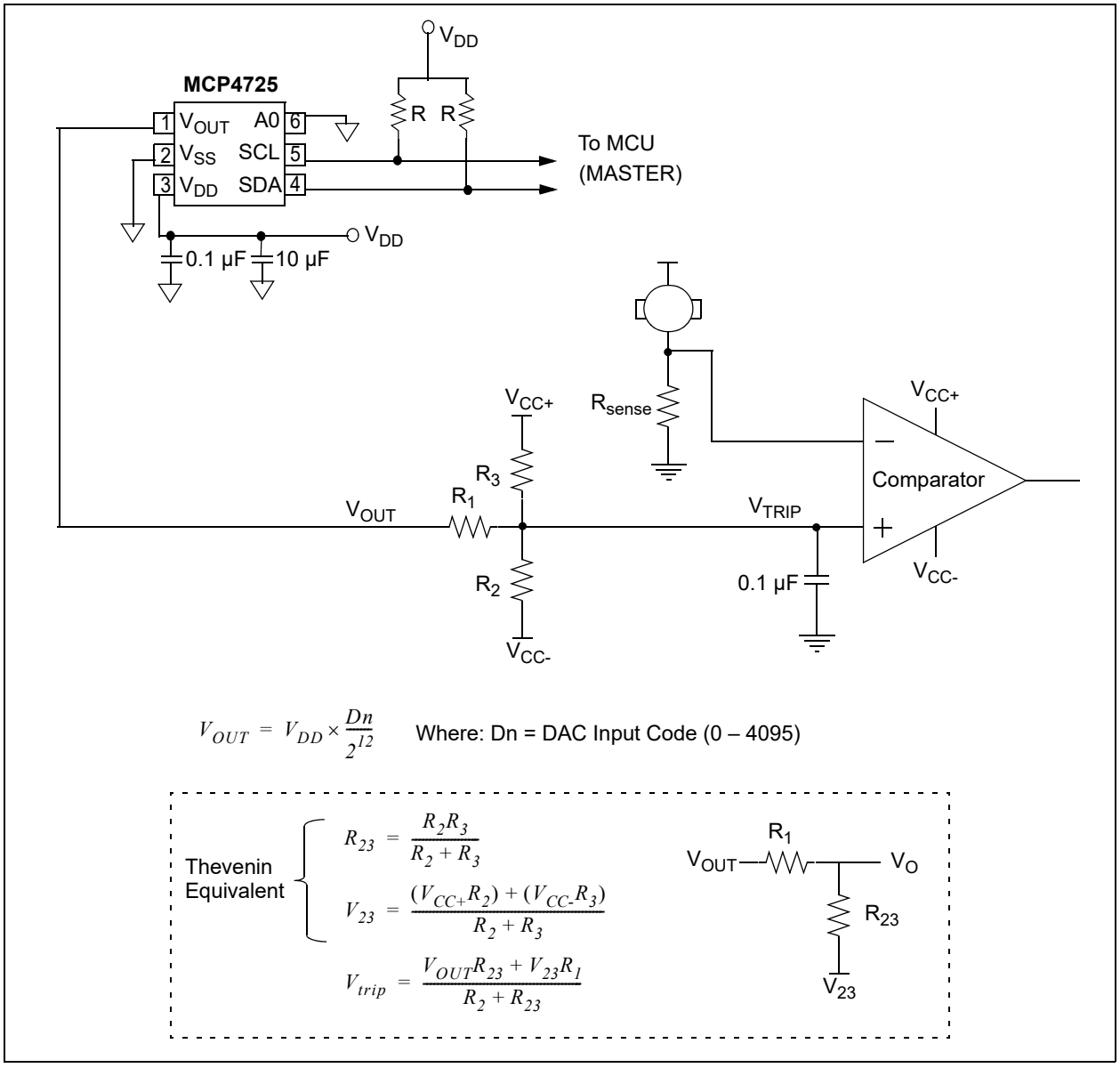


EXAMPLE 8-1: *Set Point Or Threshold Calibration.*

8.5.3 BUILDING A “WINDOW” DAC

Some sensor applications require very high resolution around the set point or threshold voltage.

Example 8-2 shows an example of creating a “window” around the threshold using a voltage divider network with a pull-up and pull-down resistor. In the circuit, the output voltage range is scaled down, but its step resolution is increased greatly.



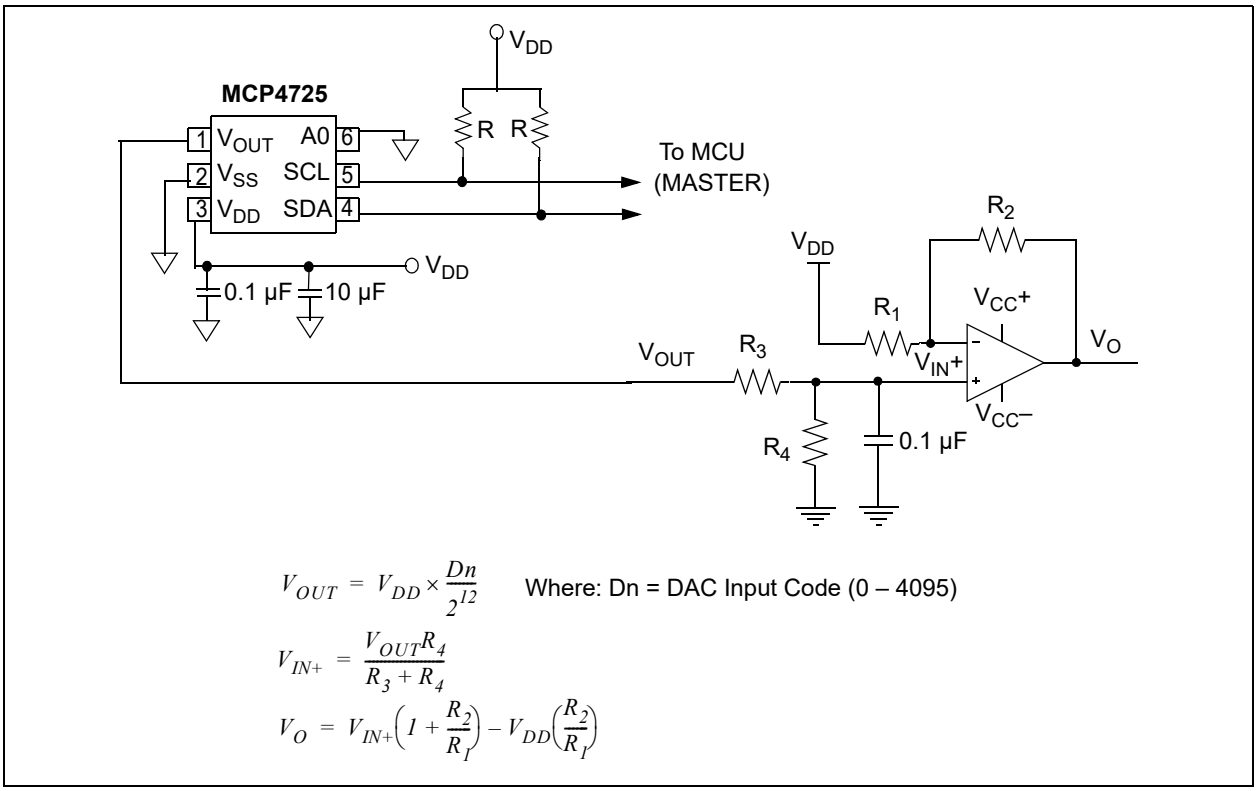
EXAMPLE 8-2: *Single-Supply “Window” DAC.*

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8.5.4 BIPOLAR OPERATION

Bipolar operation is achievable using the MCP4725 by using an external operational amplifier (op amp). This allows a general purpose DAC, with its cost and availability advantages, to meet almost any desired output voltage range, power and noise performance.

Example 8-3 illustrates a simple bipolar voltage source configuration. R_1 and R_2 allow the gain to be selected, while R_3 and R_4 shift the DAC's output to a selected offset. Note that R_4 can be tied to V_{DD} (= V_{REF}) instead of V_{SS}, if a higher offset is desired. Note that a pull-up to V_{DD} could be used, instead of R_4, if a higher offset is desired.



$$V_{OUT} = V_{DD} \times \frac{Dn}{2^{12}}$$ Where: Dn = DAC Input Code (0 – 4095)

$$V_{IN+} = \frac{V_{OUT} R_4}{R_3 + R_4}$$

$$V_O = V_{IN+}\left(1 + \frac{R_2}{R_1}\right) - V_{DD}\left(\frac{R_2}{R_1}\right)$$

EXAMPLE 8-3: *Digitally-Controlled Bipolar Voltage Source.*

8.5.4.1 Design a Bipolar DAC using Example 8-3

Some applications desires an output step magnitude of 1 mV with an output range of ±2.05V. The following steps explain the design solution:

1. Calculate the range: +2.05V – (-2.05V) = 4.1V.
2. Calculate the resolution needed:
   4.1V/1 mV = 4100 steps

   Note that 2^{12} = 4096 for 12-bit resolution.
3. The amplifier gain (R_2/R_1), multiplied by V_{DD}, must be equal to the desired minimum output to achieve bipolar operation. Since any gain can be realized by choosing resistor values (R_1+R_2), the V_{DD} value must be selected first. If a V_{DD} of 4.1V is used, solve for the amplifier's gain by setting the DAC code to 0, knowing that the output needs to be -2.05V. The equation can be simplified to

$$\frac{-R_2}{R_1} = \frac{-2.05}{V_{DD}} = \frac{-2.05}{4.1} \rightarrow \frac{R_2}{R_1} = \frac{1}{2}$$

If R_1 = 20 kΩ and R_2 = 10 kΩ, the gain will be 0.5.

4. Next, solve for R_3 and R_4 by setting the DAC to 4096, knowing that the output needs to be +2.05V.

$$\frac{R_4}{(R_3 + R_4)} = \frac{2.05V + (0.5 \cdot V_{DD})}{1.5 \cdot V_{DD}} = \frac{2}{3}$$

If R_4 = 20 kΩ, then R_3 = 10 kΩ

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8.5.5 PROGRAMMABLE CURRENT SOURCE

Example 8-3 illustrates an example how to convert the DAC voltage output to a digitally selectable current source by adding a voltage follower and a sensor register.

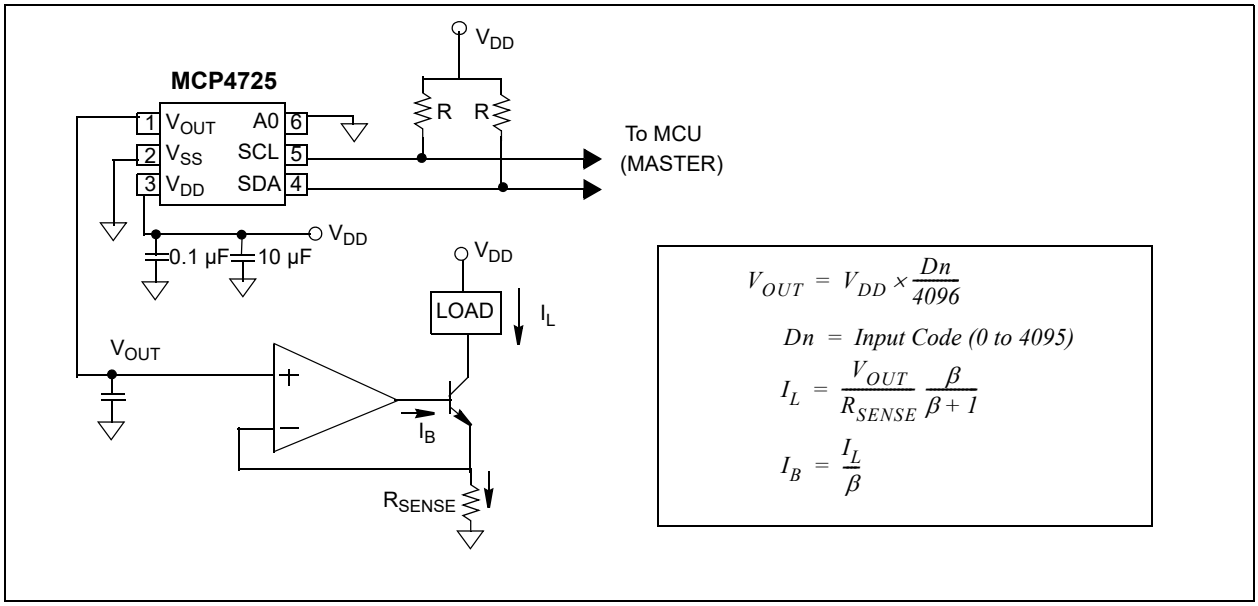


FIGURE 8-3: *Digitally Controllable Current Source.*

NOTES:

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9.0 DEVELOPMENT SUPPORT

9.1 Evaluation & Demonstration Boards

The MCP4725 SOT-23-6 Evaluation Board is available from Microchip Technology Inc. This board works with Microchip's PICkit™ Serial Analyzer. The user can program the DAC input codes and EEPROM data, or read the programmed data using the easy to use PICkit Serial Analyzer with the Graphic User Interface software. Refer to www.microchip.com for further information on this product's capabilities and availability.

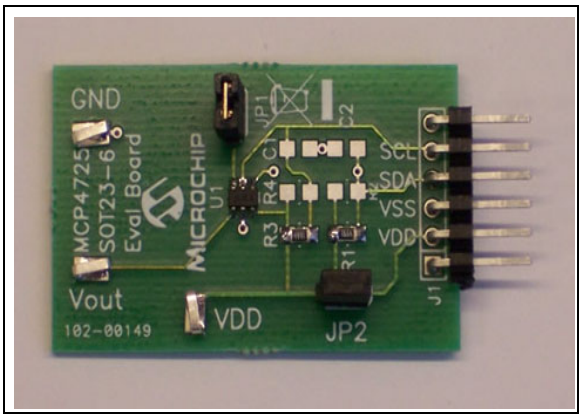


FIGURE 9-1: *MCP4725 SOT-23-6 Evaluation Board.*

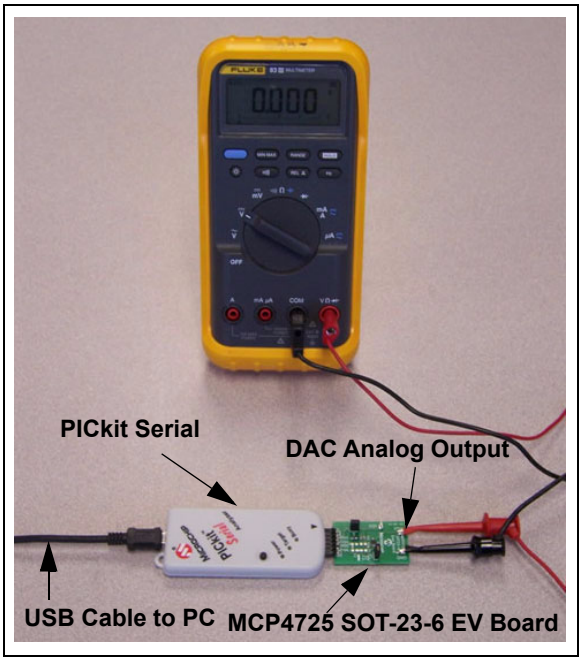


FIGURE 9-2: *Setup for the MCP4725 SOT-23-6 Evaluation Board with PICkit™ Serial Analyzer.*

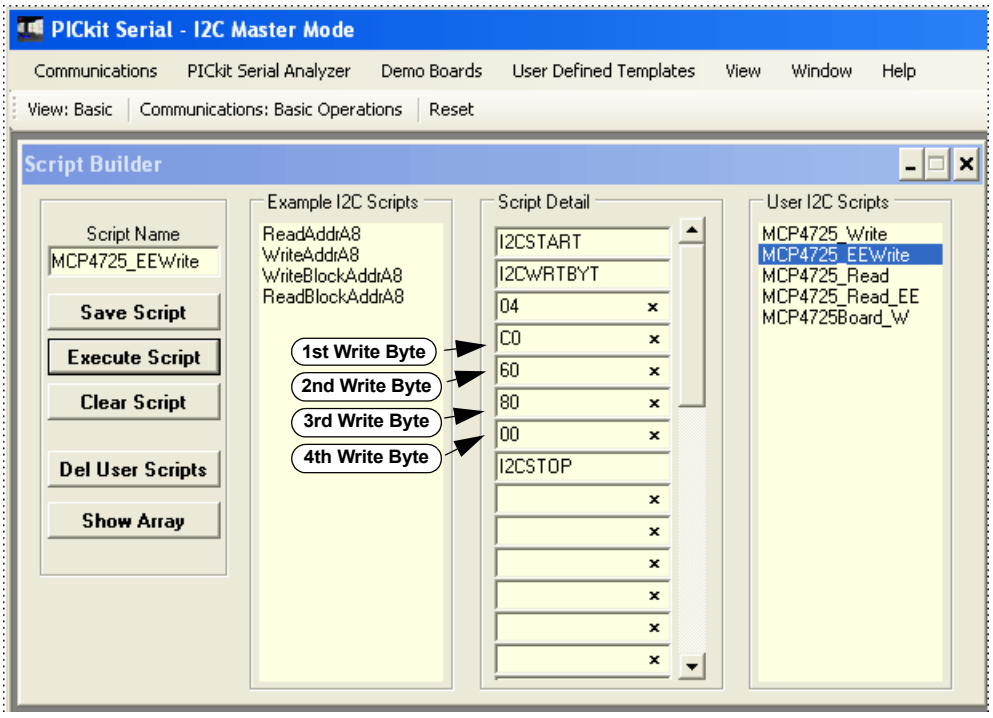


FIGURE 9-3: *Example of PICkit™ Serial User Interface.*

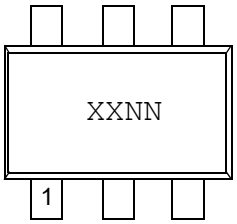
NOTES:

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10.0 PACKAGING INFORMATION

10.1 Package Marking Information

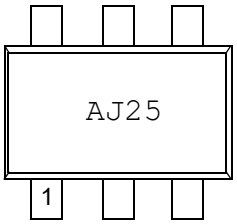
6-Lead SOT-23



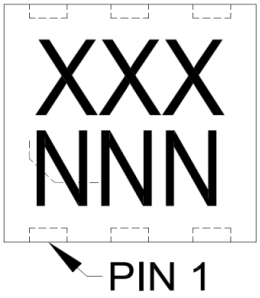
Part Number	Address Option	Code
MCP4725A0T-E/CH	A0 (00)	AJNN
MCP4725A1T-E/CH	A1 (01)	APNN
MCP4725A2T-E/CH	A2 (10)	AQNN
MCP4725A3T-E/CH	A3 (11)	ARNN

Note 1: This table applies to SOT-23 package only.

Example



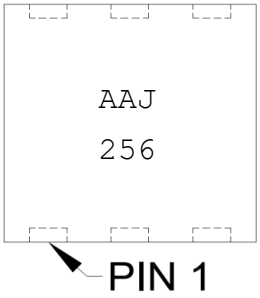
6-Lead DFN



Part Number	Address Option	Code
MCP4725A0T-E/MAY	A0	AAJ
MCP4725A1T-E/MAY	A1	AAK
MCP4725A2T-E/MAY	A2	AAL
MCP4725A3T-E/MAY	A3	AAM

Note 1: This table applies to DFN package only.

Example

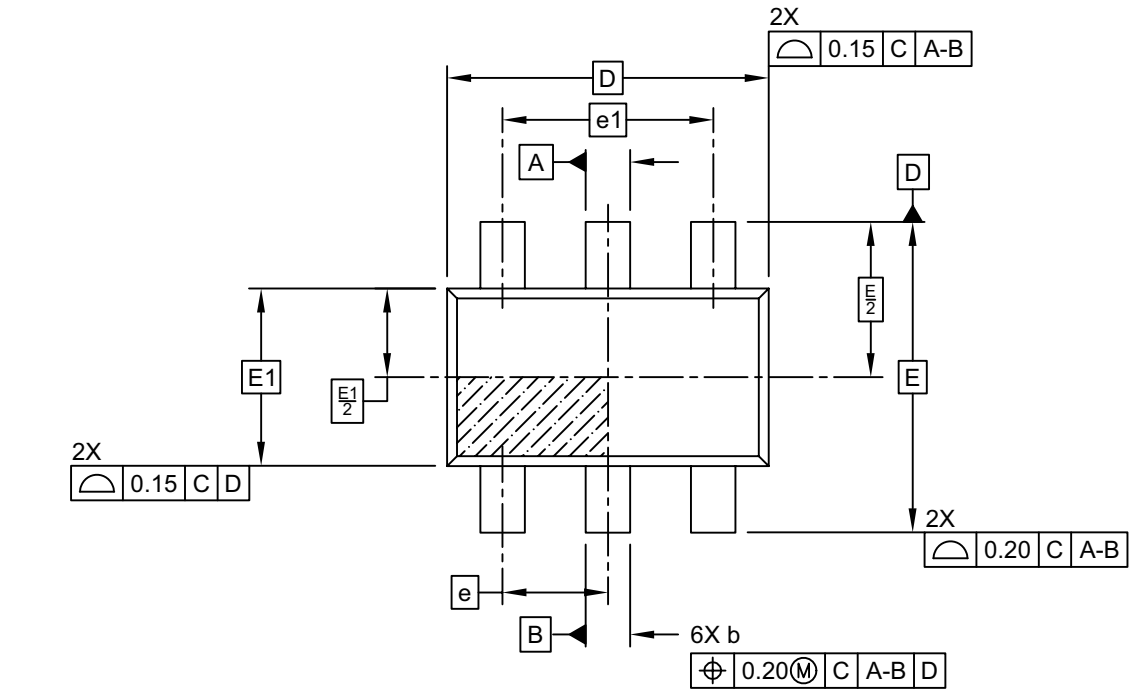


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

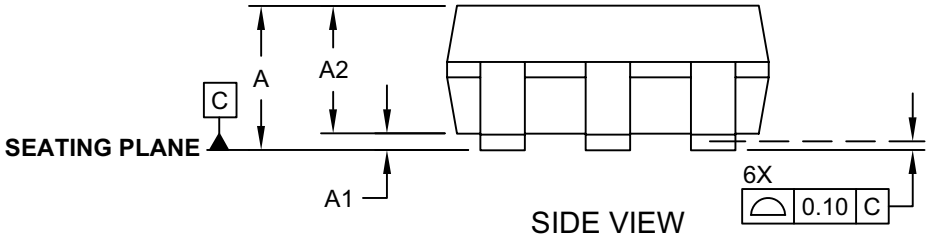
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

6-Lead Plastic Small Outline Transistor (CH, CHY) [SOT-23]

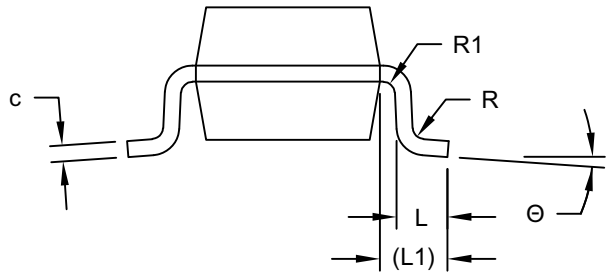
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



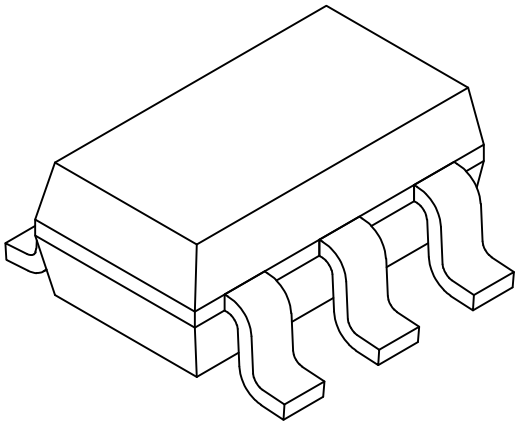
END VIEW

Microchip Technology Drawing C04-028D (CH) Sheet 1 of 2

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6-Lead Plastic Small Outline Transistor (CH, CHY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		6	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	1.15	1.30
Standoff	A1	0.00	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	0.45	0.60
Footprint	L1		0.60 REF	
Foot Angle	ϕ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

Notes:

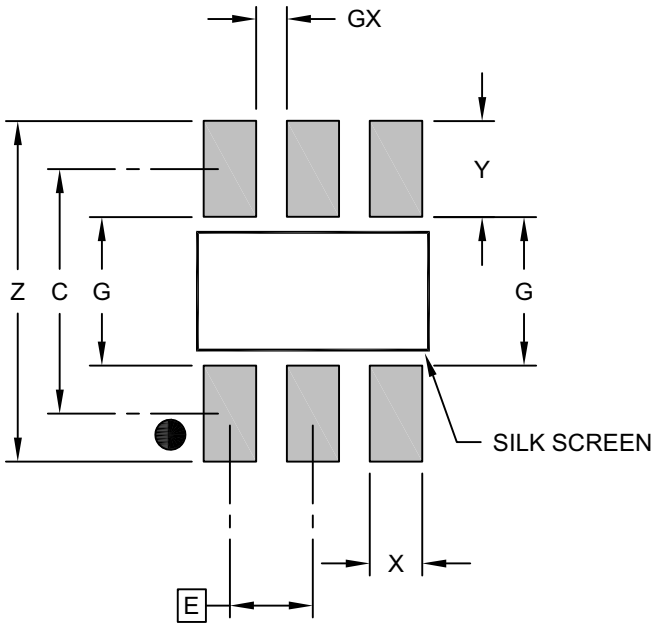
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-028D (CH) Sheet 2 of 2

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6-Lead Plastic Small Outline Transistor (CH, CHY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X3)	X			0.60
Contact Pad Length (X3)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

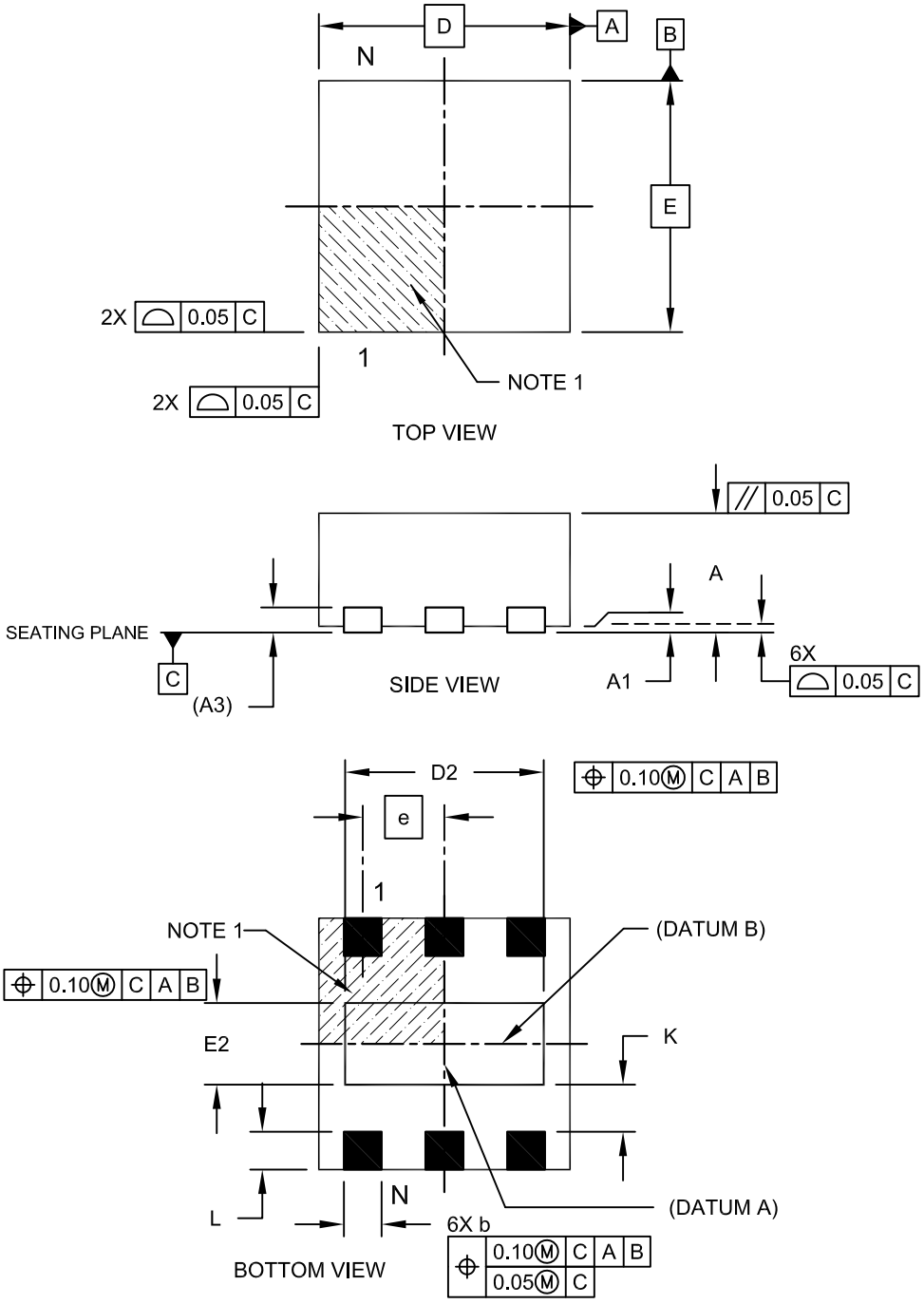
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028D (CH)

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6-Lead Plastic Dual Flat, No Lead Package (MA[Y]) - 2x2x0.9mm Body [DFN]

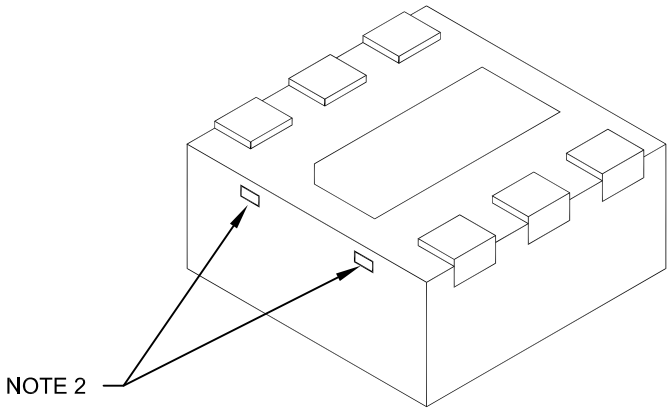
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-120C Sheet 1 of 2

6-Lead Plastic Dual Flat, No Lead Package (MA[Y]) - 2x2x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		2.00 BSC	
Exposed Pad Length	D2	1.50	1.60	1.70
Exposed Pad Width	E2	0.90	1.00	1.10
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

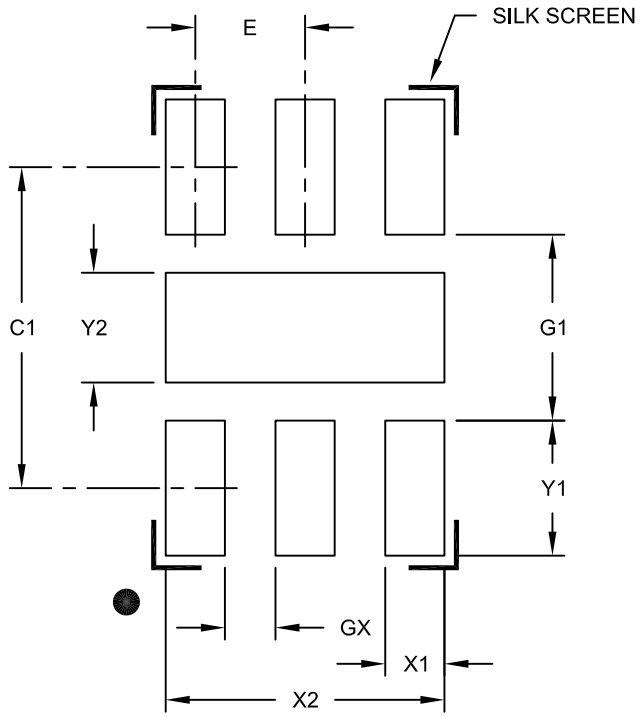
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-120C Sheet 2 of 2

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6-Lead Plastic Dual Flat, No Lead Package (MA) - 2x2x0.9mm Body [DFN]



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	Y2			1.00
Optional Center Pad Length	X2			1.70
Contact Pad Spacing	C1		2.10	
Contact Pad Width (X6)	X1			0.35
Contact Pad Length (X6)	Y1			0.65
Distance Between Pads	GX	0.20		
Distance Between Pads	G1	1.10		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2120A

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APPENDIX A: REVISION HISTORY

Revision E (February 2022)

The following is the list of modifications:

- Added information related to **6-Lead, 2 x 2 mm DFN** package option throughout the document.
- Updated Features
- Updated General Description
- Updated Package Types
- Updated Temperature Characteristics
- Updated **Section 3.0 "Pin Descriptions"** and Table 3-1.
- Updated **Section 10.0 "Packaging Information"**.
- Updated **Product Identification System**.
- Various typographical and style updates throughout the document.
- Updated literature number to the current Microchip format. The new unique literature number used to identify this document is **DS20002039**.

Revision D (June 2009)

The following is the list of modifications:

- Added V_{DD_RAMP} parameter in **Section "ELECTRICAL CHARACTERISTICS"** and description in **Section 5.4.2 "V_{DD} Ramp Rate and EEPROM"**.

Revision C (November 2007)

The following is the list of modifications:

- Corrected Address Options on Product Identification System page.

Revision B (October 2007)

The following is the list of modifications:

- Added characterization graphs to document.
- Numerous edits throughout.
- Add new package marking address options. Updated package marking information and package outline drawings.
- Added address options to Product Identification System page.

Revision A (April 2007)

- Original release of this document.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	X	X	/XX
Device	Address Options	Tape and Reel	Temperature Range	Package

Device: MCP4725: Single Channel 12-Bit DAC w/EEPROM Memory

Address Options:

XX		A2	A1	A0
A0 *	=	0	0	External
A1	=	0	1	External
A2	=	1	0	External
A3	=	1	1	External

* Default option. Contact Microchip factory for other address options

Tape and Reel: T = Tape and Reel

Temperature Range: E = -40°C to +125°C

Package: CH = Plastic Small Outline Transistor (SOT-23-6), 6-Lead

MAY = Plastic Dual Flat, No Lead Package (2x2 DFN), 6-lead

Examples:

a) MCP4725A0T-E/CH: Tape and Reel, Extended Temperature, 6LD SOT-23 package, Address Option = A0

b) MCP4725A1T-E/CH: Tape and Reel, Extended Temperature, 6LD SOT-23 package, Address Option = A1

c) MCP4725A2T-E/CH: Tape and Reel, Extended Temperature, 6LD SOT-23 package, Address Option = A2

d) MCP4725A3T-E/CH: Tape and Reel, Extended Temperature, 6LD SOT-23 package, Address Option = A3

a) MCP4725A0T-E/MAY: Tape and Reel, Extended Temperature, 6LD DFN package, Address Option = A0

b) MCP4725A1T-E/MAY: Tape and Reel, Extended Temperature, 6LD DFN package, Address Option = A1

c) MCP4725A2T-E/MAY: Tape and Reel, Extended Temperature, 6LD DFN package. Address Option = A2

d) MCP4725A3T-E/MAY: Tape and Reel, Extended Temperature, 6LD DFN package, Address Option = A3

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