# MCP47CXBXX

## 8/10/12-Bit Digital-to-Analog Converters, 1 LSb INL Single/Dual Voltage Outputs with I²C Interface

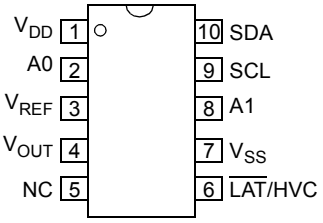
### Features

- Memory Options:
  - Volatile Memory: MCP47CVBXX
  - Nonvolatile Memory: MCP47CMBXX
- Operating Voltage Range:
  - 2.7V to 5.5V – Full specifications
  - 1.8V to 2.7V – Reduced device specifications
- Output Voltage Resolutions:
  - 8-bit: MCP47CXB0X (256 steps)
  - 10-bit: MCP47CXB1X (1024 steps)
  - 12-bit: MCP47CXB2X (4096 steps)
- Nonvolatile Memory (MTP) Size: 32 Locations
- 1 LSb Integral Nonlinearity (INL) Specification
- DAC Voltage Reference Source Options:
  - Device $V_{DD}$
  - External $V_{REF}$ pin (buffered or unbuffered)
  - Internal band gap (1.214V typical)
- Output Gain Options:
  - 1x (Unity)
  - 2x (available when not using internal $V_{DD}$ as voltage source)
- Power-on/Brown-out Reset (POR/BOR) Protection
- Power-Down Modes:
  - Disconnects output buffer (high-impedance)
  - Selection of $V_{OUT}$ pull-down resistors (100 kΩ or 1 kΩ)
- I²C Interface:
  - Slave address options: register-defined address with two physical address select pins (package dependent)
  - Standard (100 kbps), Fast (400 kbps) and High-Speed (up to 3.4 Mbps) modes
- Package Types:
  - Dual: 16-lead 3 x 3 QFN, 10-lead MSOP, 10-lead 3 x 3 DFN
  - Single: 16-lead 3 x 3 QFN, 10-lead MSOP, 10-lead 3 x 3 DFN
- Extended Temperature Range: -40°C to +125°C

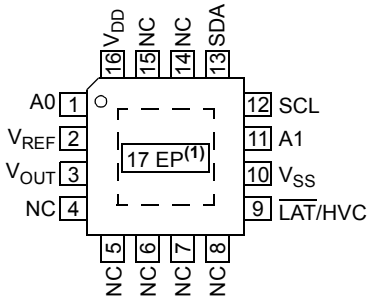
### Package Types

**MCP47CXBX1 (Single)**

**MSOP-10, DFN-10 (3x3)**

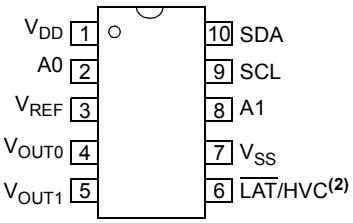



**QFN-16 (3x3)**

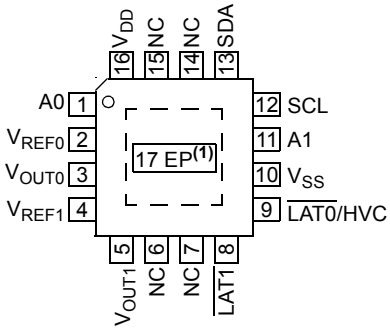



**MCP47CXBX2 (Dual)**

**MSOP-10, DFN-10 (3x3)**




**QFN-16 (3x3)**




**Note 1:** Exposed pad (substrate paddle).
**2:** This pin's signal can be connected to DAC0 and/or DAC1.

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## General Description

The MCP47CXBXX devices are single and dual channel 8-bit, 10-bit and 12-bit buffered voltage output Digital-to-Analog Converters (DAC) with volatile or MTP memory, and an $I^2C$ serial interface.

The MTP memory can be written by the user up to 32 times for each specific register. It requires a high-voltage level on the HVC pin, typically 7.5V, in order to successfully program the desired memory location. The nonvolatile memory includes power-up output values, device Configuration registers and general purpose memory.

The $V_{REF}$ pin, the device $V_{DD}$ or the internal band gap voltage can be selected as the DAC's reference voltage. When $V_{DD}$ is selected, $V_{DD}$ is internally connected to the DAC reference circuit.

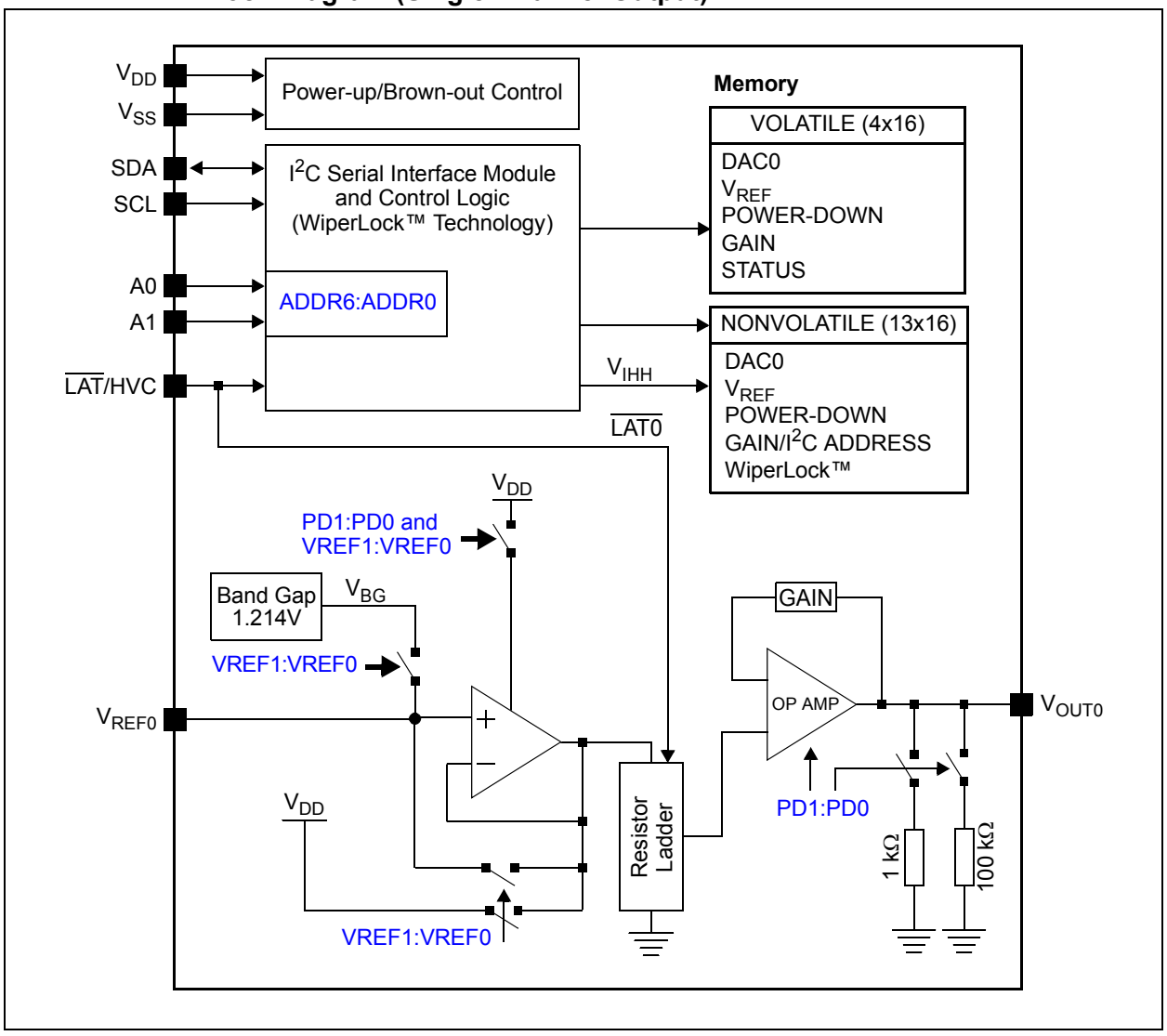
When the $V_{REF}$ pin is used with an external voltage reference, the user can select between a gain of 1 or 2 and can have the reference buffer enabled or disabled. When the gain is 2, the $V_{REF}$ pin voltage should be limited to a maximum of $V_{DD}/2$.

These devices have a two-wire $I^2C$ compatible serial interface for Standard (100 kHz), Fast (400 kHz) or High-Speed (1.7 MHz and 3.4 MHz) modes.

## Applications

- Set Point or Offset Trimming
- Sensor Calibration
- Low-Power Portable Instrumentation
- PC Peripherals
- Data Acquisition Systems

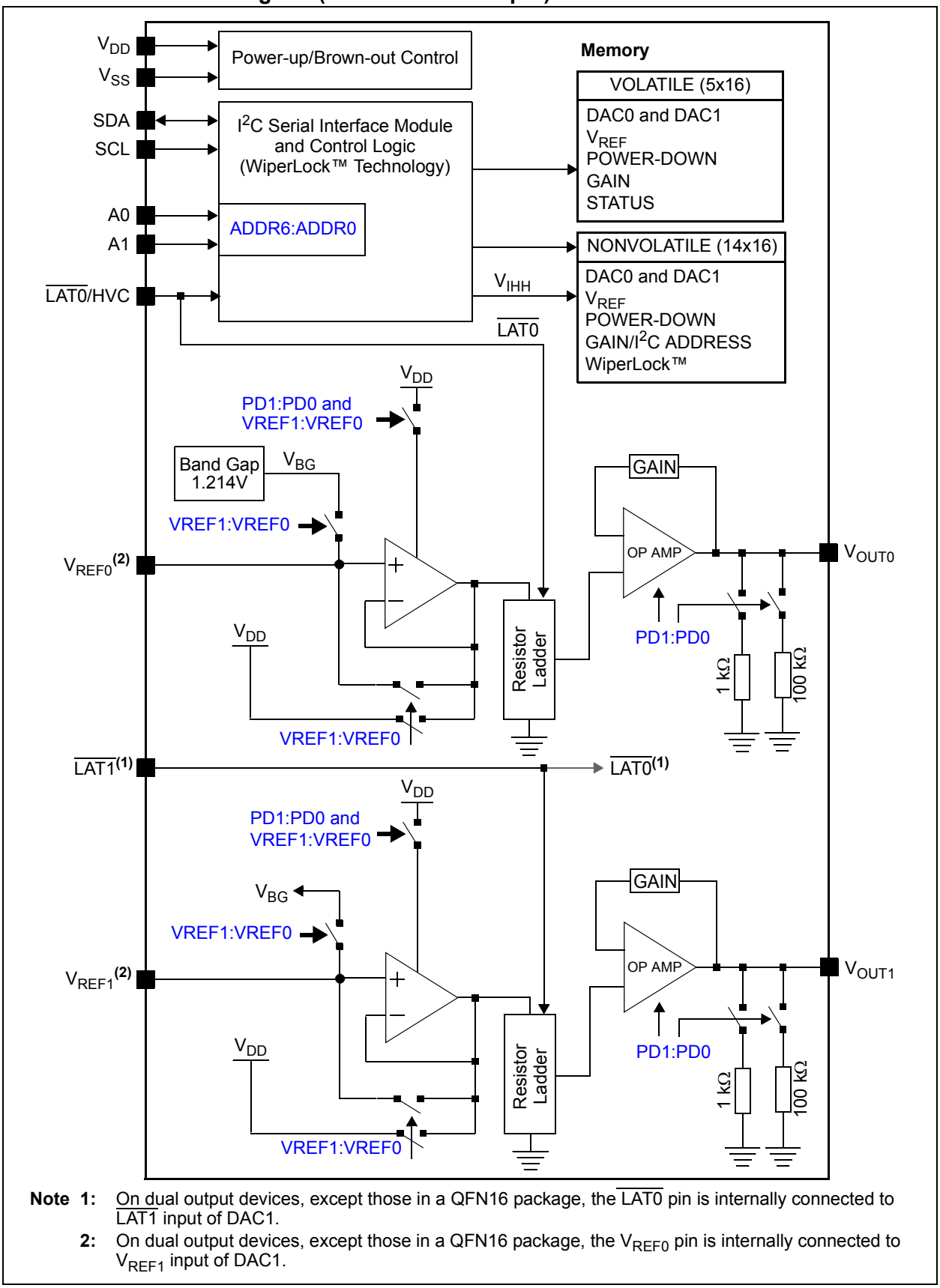
### MCP47CMBX1 Block Diagram (Single-Channel Output)





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## MCP47CMBX2 Block Diagram (Dual Channel Output)




**Note 1:** On dual output devices, except those in a QFN16 package, the $\overline{LAT0}$ pin is internally connected to $\overline{LAT1}$ input of DAC1.

**2:** On dual output devices, except those in a QFN16 package, the $V_{REF0}$ pin is internally connected to $V_{REF1}$ input of DAC1.

## Family Device Features

| Device | Package Type | # of Channels | Resolution (bits) | DAC Output POR/BOR Setting(1) | # of $V_{REF}$ Inputs | # of LAT Inputs(3) | # of Address Pins | Memory(2) | GP MTP Locations |
|---|---|---|---|---|---|---|---|---|---|
| MCP47CVB01 | MSOP, QFN, DFN | 1 | 8 | 7Fh | 1 | 1 | 2 | RAM | — |
| MCP47CVB11 | MSOP, QFN, DFN | 1 | 10 | 1FFh | 1 | 1 | 2 | RAM | — |
| MCP47CVB21 | MSOP, QFN, DFN | 1 | 12 | 7FFh | 1 | 1 | 2 | RAM | — |
| MCP47CVB02 | QFN | 2 | 8 | 7Fh | 2 | 2 | 2 | RAM | — |
| | MSOP, DFN | 2 | 8 | 7Fh | 1 | 1 | 2 | RAM | — |
| MCP47CVB12 | QFN | 2 | 10 | 1FFh | 2 | 2 | 2 | RAM | — |
| | MSOP, DFN | 2 | 10 | 1FFh | 1 | 1 | 2 | RAM | — |
| MCP47CVB22 | QFN | 2 | 12 | 7FFh | 2 | 2 | 2 | RAM | — |
| | MSOP, DFN | 2 | 12 | 7FFh | 1 | 1 | 2 | RAM | — |
| MCP47CMB01 | MSOP, QFN, DFN | 1 | 8 | 7Fh | 1 | 1 | 2 | MTP | 8 |
| MCP47CMB11 | MSOP, QFN, DFN | 1 | 10 | 1FFh | 1 | 1 | 2 | MTP | 8 |
| MCP47CMB21 | MSOP, QFN, DFN | 1 | 12 | 7FFh | 1 | 1 | 2 | MTP | 8 |
| MCP47CMB02 | QFN | 2 | 8 | 7Fh | 2 | 2 | 2 | MTP | 8 |
| | MSOP, DFN | 2 | 8 | 7Fh | 1 | 1 | 2 | MTP | 8 |
| MCP47CMB12 | QFN | 2 | 10 | 1FFh | 2 | 2 | 2 | MTP | 8 |
| | MSOP, DFN | 2 | 10 | 1FFh | 1 | 1 | 2 | MTP | 8 |
| MCP47CMB22 | QFN | 2 | 12 | 7FFh | 2 | 2 | 2 | MTP | 8 |
| | MSOP, DFN | 2 | 12 | 7FFh | 1 | 1 | 2 | MTP | 8 |

**Note 1:** The factory default value.

**2:** Each nonvolatile memory location can be written 32 times. For subsequent writes to the MTP, the device will ignore the commands and the memory will not be modified.

**3:** If the product is a dual device and the package has only one $\overline{LAT}$ pin, it is associated with both DAC0 and DAC1.


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# 1.0 ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings(†)

Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... -0.6V to +6.5V
Voltage on all pins with respect to $V_{SS}$ ..... -0.6V to $V_{DD}$ + 0.3V
Input clamp current, $I_{IK}$ ($V_I < 0$, $V_I > V_{DD}$, $V_I > V_{PP}$ on HV pins) ..... ±20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{DD}$) ..... ±20 mA
Maximum current out of $V_{SS}$ pin (Single) ..... 50 mA
(Dual) ..... 100 mA
Maximum current into $V_{DD}$ pin (Single) ..... 50 mA
(Dual) ..... 100 mA
Maximum current sourced by the $V_{OUT}$ pin ..... 20 mA
Maximum current sunk by the $V_{OUT}$ pin ..... 20 mA
Maximum current source/sunk by the $V_{REF(0)}$ pin (in Band Gap mode) ..... 20 mA
Maximum current sunk by the $V_{REFx}$ pin (when $V_{REF}$ is in Unbuffered mode) ..... 175 µA
Maximum current sourced by the $V_{REFx}$ pin ..... 20 µA
Maximum current sunk by the $V_{REF}$ pin ..... 125 µA
Maximum input current source/sunk by SDA, SCL pins ..... 2 mA
Maximum output current sunk by SDA output pin ..... 25 mA
Total power dissipation(1) ..... 400 mW
ESD protection on all pins ..... ≥ ±6 kV (HBM)
..... ≥ ±400V (MM)
..... ≥ ±2 kV (CDM)
Latch-up (per JEDEC JESD78A) at +125°C ..... ±100 mA
Storage temperature ..... -65°C to +150°C
Ambient temperature with power applied ..... -55°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
Maximum Junction Temperature ($T_J$) ..... +150°C

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Note 1:** Power dissipation is calculated as follows:
$P_{DIS} = V_{DD} \times \{I_{DD} - \Sigma I_{OH}\} + \Sigma \{(V_{DD} - V_{OH}) \times I_{OH}\} + \Sigma(V_{OL} \times I_{OL})$

## DC CHARACTERISTICS

**Standard Operating Conditions (unless otherwise specified)**:
Operating Temperature: -40°C ≤ $T_A$ ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
$V_{DD}$ = +2.7V to 5.5V, $V_{REF}$ = +1.000V to $V_{DD}$, $V_{SS}$ = 0V, $R_L$ = 2 kΩ from $V_{OUT}$ to GND, $C_L$ = 100 pF.
Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 2.7 | — | 5.5 | V | |
| | | 1.8 | — | 2.7 | V | DAC operation (reduced analog specifications) and serial interface |
| $V_{DD}$ Voltage (rising) to Ensure Device Power-on Reset | $V_{POR}$ | — | — | 1.75 | V | RAM retention voltage: ($V_{RAM}$) < $V_{POR}$, $V_{DD}$ voltages greater than the $V_{POR}$ limit ensure that the device is out of Reset |
| $V_{DD}$ Voltage (falling) to Ensure Device Brown-out Reset | $V_{BOR}$ | $V_{RAM}$ | — | 1.61 | V | RAM retention voltage: ($V_{RAM}$) < $V_{BOR}$ |
| $V_{DD}$ Rise Rate to Ensure Power-on Reset | $V_{DDRR}$ | **Note 3** | | | V/ms | |
| Power-on Reset to Output-Driven Delay(2) | $T_{POR2OD}$ | — | — | 130 | µs | $V_{DD}$ rising, $V_{DD}$ > $V_{POR}$, single output |
| | | — | — | 145 | µs | $V_{DD}$ rising, $V_{DD}$ > $V_{POR}$, dual output |

**Note 2** This parameter is ensured by characterization.

**Note 3** POR/BOR voltage trip point is not slope-dependent. Hysteresis implemented with time delay.


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## DC CHARACTERISTICS (CONTINUED)

**Standard Operating Conditions (unless otherwise specified)**:
Operating Temperature: -40°C ≤ $T_A$ ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
$V_{DD}$ = +2.7V to 5.5V, $V_{REF}$ = +1.000V to $V_{DD}$, $V_{SS}$ = 0V, $R_L$ = 2 kΩ from $V_{OUT}$ to GND, $C_L$ = 100 pF.
Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions | | |
|---|---|---|---|---|---|---|---|---|
| Supply Current | $I_{DD}$ | — | — | 230 | µA | Single | 100 kHz[2] | Serial interface active, VRxB:VRxA = 10[4], $V_{OUT}$ is unloaded, $V_{REF}$ = $V_{DD}$ = 5.5V, Volatile DAC register = Mid-Scale |
| | | — | — | 310 | | | 400 kHz | |
| | | — | — | 460 | | | 1.7 MHz[2] | |
| | | — | — | 620 | | | 3.4 MHz[2] | |
| | | — | — | 330 | | Dual | 100 kHz[2] | |
| | | — | — | 410 | | | 400 kHz | |
| | | — | — | 560 | | | 1.7 MHz[2] | |
| | | — | — | 720 | | | 3.4 MHz[2] | |
| | | — | — | 160 | | Single | Serial interface inactive, VRxB:VRxA = 10, $V_{OUT}$ is unloaded, $V_{REF}$ = $V_{DD}$ = 5.5V, Volatile DAC register = Mid-Scale | |
| | | — | — | 280 | | Dual | | |
| $\overline{LAT}$/HVC Pin Write Current[2] | $I_{DD(MTP_WR)}$ | — | — | 6.40 | mA | — | Serial interface inactive (MTP write active), VRxB:VRxA = 10 (valid for all modes), $V_{DD}$ = 5.5V, $\overline{LAT}$/HVC = $V_{IHH}$, write all '1's to nonvolatile DAC0, $V_{OUT}$ pins are unloaded | |
| Power-Down Current | $I_{DDP}$ | — | 0.65 | 3.80 | µA | — | PDxB:PDxA = 01[5], VRxB:VRxA = 10, $V_{OUT}$ not connected | |

**Note 2** This parameter is ensured by characterization.

**Note 4** Supply current is independent of current through the resistor ladder in mode VRxB:VRxA = 10.

**Note 5** The PDxB:PDxA = 01, 10 and 11 configurations should have the same current.

## DC CHARACTERISTICS (CONTINUED)

**Standard Operating Conditions (unless otherwise specified)**:
Operating Temperature: -40°C ≤ $T_A$ ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
$V_{DD}$ = +2.7V to 5.5V, $V_{REF}$ = +1.000V to $V_{DD}$, $V_{SS}$ = 0V, $R_L$ = 2 kΩ from $V_{OUT}$ to GND, $C_L$ = 100 pF.
Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions | |
|---|---|---|---|---|---|---|---|
| Resistor Ladder Resistance(6) | $R_L$ | 63.9 | 71 | 78.1 | kΩ | VRxB:VRxA = 10, $V_{REF}$ = $V_{DD}$ | |
| Resolution (# of resistors and # of taps), (see C.1 "Resolution") | N | 256 | | | Taps | 8-bit | No missing codes |
| | | 1024 | | | Taps | 10-bit | No missing codes |
| | | 4096 | | | Taps | 12-bit | No missing codes |
| Nominal $V_{OUT}$ Match(10) | $\lvert V_{OUT} - V_{OUTMEAN} \rvert / V_{OUTMEAN}$ | — | 0.016 | 0.300 | % | 1.8V ≤ $V_{DD}$ ≤ 5.5V(2) | |
| $V_{OUT}$ Tempco(2) (see C.19 "$V_{OUT}$ Temperature Coefficient") | $\Delta V_{OUT}/\Delta T$ | — | 3 | — | ppm/°C | Code = Mid-Scale, VRxB:VRxA = 00, 10 and 11 | |
| $V_{REF}$ Pin Input Voltage Range(1) | $V_{REF}$ | $V_{SS}$ | — | $V_{DD}$ | V | 1.8V ≤ $V_{DD}$ ≤ 5.5V | |

**Note 1** This parameter is ensured by design.

**Note 2** This parameter is ensured by characterization.

**Note 6** Resistance is defined as the resistance between the $V_{REF}$ pin (mode VRxB:VRxA = 10) to the $V_{SS}$ pin. For dual channel devices (MCP47CXBX2), this is the effective resistance of each resistor ladder. The resistance measurement is one of the two resistor ladders measured in parallel.

**Note 10** Variation of one output voltage to mean output voltage for dual devices only.


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## DC CHARACTERISTICS (CONTINUED)

**Standard Operating Conditions (unless otherwise specified)**:
Operating Temperature: -40°C ≤ $T_A$ ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
$V_{DD}$ = +2.7V to 5.5V, $V_{REF}$ = +1.000V to $V_{DD}$, $V_{SS}$ = 0V, $R_L$ = 2 kΩ from $V_{OUT}$ to GND, $C_L$ = 100 pF.
Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions | |
|---|---|---|---|---|---|---|---|
| Zero-Scale Error (Code = 000h) (see **C.5 "Zero-Scale Error ($E_{ZS}$)"**) | $E_{ZS}$ | — | — | 0.375 | LSb | 8-bit | VRxB:VRxA = 10, G = 0, $V_{REF}$ = $V_{DD}$, no load |
| | | — | — | 1.5 | LSb | 10-bit | VRxB:VRxA = 10, G = 0, $V_{REF}$ = $V_{DD}$, no load |
| | | — | — | 6 | LSb | 12-bit | VRxB:VRxA = 10, G = 0, $V_{REF}$ = $V_{DD}$, no load |
| | | See **Section 2.0 "Typical Performance Curves"**(2) | | | LSb | | VRxB:VRxA = 10, G = 1, $V_{REF}$ = 0.5 x $V_{DD}$, no load |
| | | See **Section 2.0 "Typical Performance Curves"**(2) | | | LSb | | VRxB:VRxA = 01, G = 0, G = 1, $V_{DD}$ = 1.8V-5.5V, no load |
| Offset Error (see **C.7 "Offset Error ($E_{OS}$)"**) | $E_{OS}$ | -6 | ±0.4 | +6 | mV | VRxB:VRxA = 10, Gx = 0, no load, 8-bit: Code = 4; 10-bit: Code = 16; 12-bit: Code = 64 | |
| Offset Voltage Temperature Coefficient(2,9) | $V_{OSTC}$ | — | ±5 | — | µV/°C | | |
| Full-Scale Error (see **C.4 "Full-Scale Error ($E_{FS}$)"**) | $E_{FS}$ | — | — | 2.5 | LSb | 8-bit | VRxB:VRxA = 10, G = 0, $V_{REF}$ = $V_{DD}$, no load |
| | | — | — | 9 | LSb | 10-bit | VRxB:VRxA = 10, G = 0, $V_{REF}$ = $V_{DD}$, no load |
| | | — | — | 35 | LSb | 12-bit | VRxB:VRxA = 10, G = 0, $V_{REF}$ = $V_{DD}$, no load |
| | | See **Section 2.0 "Typical Performance Curves"**(2) | | | LSb | | VRxB:VRxA = 10, G = 1, $V_{REF}$ = 0.5 x $V_{DD}$, no load |
| | | See **Section 2.0 "Typical Performance Curves"**(2) | | | LSb | | VRxB:VRxA = 01, G = 0, G = 1, $V_{DD}$ = 1.8V-5.5V, no load |
| Gain Error (see **C.9 "Gain Error ($E_G$)"**)(7) | $E_G$ | -1 | ±0.1 | +1 | % of FSR | 8-bit | VRxB:VRxA = 10, G = 0, Code = 252, $V_{REF}$ = $V_{DD}$, no load |
| | | -1 | ±0.1 | +1 | % of FSR | 10-bit | VRxB:VRxA = 10, G = 0, Code = 1008, $V_{REF}$ = $V_{DD}$, no load |
| | | -1 | ±0.1 | +1 | % of FSR | 12-bit | VRxB:VRxA = 10, G = 0, Code = 4032, $V_{REF}$ = $V_{DD}$, no load |
| Gain Error Drift(2,9) (see **C.10 "Gain Error Drift ($EG_D$)"**) | ΔG/°C | — | -6 | — | ppm/°C | | |

**Note 2** This parameter is ensured by characterization.

**Note 7** This gain error does not include the offset error.

**Note 9** Code range dependent on resolution: 8-bit, codes 4 to 252; 10-bit, codes 16 to 1008; 12-bit, codes 64 to 4032.

## DC CHARACTERISTICS (CONTINUED)

**Standard Operating Conditions (unless otherwise specified)**:
Operating Temperature: -40°C ≤ $T_A$ ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
$V_{DD}$ = +2.7V to 5.5V, $V_{REF}$ = +1.000V to $V_{DD}$, $V_{SS}$ = 0V, $R_L$ = 2 kΩ from $V_{OUT}$ to GND, $C_L$ = 100 pF.
Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions | |
|---|---|---|---|---|---|---|---|
| Total Unadjusted Error[2,9] (see **C.6 "Total Unadjusted Error ($E_T$)"**) | $E_T$ | -2.5 | — | 0.75 | LSb | 8-bit | VRxB:VRxA = 10, G = 0, $V_{REF}$ = $V_{DD}$, no load |
| | | -9 | — | 3 | LSb | 10-bit | VRxB:VRxA = 10, G = 0, $V_{REF}$ = $V_{DD}$, no load |
| | | -35 | — | 12 | LSb | 12-bit | VRxB:VRxA = 10, G = 0, $V_{REF}$ = $V_{DD}$, no load |
| | | See **Section 2.0 "Typical Performance Curves"**[2] | | | LSb | | VRxB:VRxA = 10, G = 1, $V_{REF}$ = 0.5 x $V_{DD}$, no load |
| | | See **Section 2.0 "Typical Performance Curves"**[2] | | | LSb | | VRxB:VRxA = 01, G = 0, G = 1, $V_{DD}$ = 1.8V-5.5V, no load |
| Integral Nonlinearity (see **C.11 "Integral Nonlinearity (INL)"**)[9] | INL | -0.1 | — | +0.1 | LSb | 8-bit | VRxB:VRxA = 10, G = 0, $V_{REF}$ = $V_{DD}$, no load |
| | | -0.25 | — | +0.25 | LSb | 10-bit | VRxB:VRxA = 10, G = 0, $V_{REF}$ = $V_{DD}$, no load |
| | | -1 | — | +1 | LSb | 12-bit | VRxB:VRxA = 10, G = 0, $V_{REF}$ = $V_{DD}$, no load |
| | | See **Section 2.0 "Typical Performance Curves"**[2] | | | LSb | | VRxB:VRxA = 10, G = 1, $V_{REF}$ = 0.5 x $V_{DD}$, no load |
| | | See **Section 2.0 "Typical Performance Curves"**[2] | | | LSb | | VRxB:VRxA = 01, G = 0, G = 1, $V_{DD}$ = 1.8V-5.5V, no load |
| Differential Nonlinearity (see **C.12 "Differential Nonlinearity (DNL)"**)[9] | DNL | -0.1 | — | +0.1 | LSb | 8-bit | VRxB:VRxA = 10, G = 0, $V_{REF}$ = $V_{DD}$, no load |
| | | -0.25 | — | +0.25 | LSb | 10-bit | VRxB:VRxA = 10, G = 0, $V_{REF}$ = $V_{DD}$, no load |
| | | -1.0 | — | +1.0 | LSb | 12-bit | VRxB:VRxA = 10, G = 0, $V_{REF}$ = $V_{DD}$, no load |
| | | See **Section 2.0 "Typical Performance Curves"**[2] | | | LSb | | VRxB:VRxA = 10, G = 1, $V_{REF}$ = 0.5 x $V_{DD}$, no load |
| | | See **Section 2.0 "Typical Performance Curves"**[2] | | | LSb | | VRxB:VRxA = 01, G = 0, G = 1, $V_{DD}$ = 1.8V-5.5V, no load |

**Note 2** This parameter is ensured by characterization.

**Note 9** Code range dependent on resolution: 8-bit, codes 4 to 252; 10-bit, codes 16 to 1008; 12-bit, codes 64 to 4032.


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## DC CHARACTERISTICS (CONTINUED)

**Standard Operating Conditions (unless otherwise specified)**:
Operating Temperature: -40°C ≤ $T_A$ ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
$V_{DD}$ = +2.7V to 5.5V, $V_{REF}$ = +1.000V to $V_{DD}$, $V_{SS}$ = 0V, $R_L$ = 2 kΩ from $V_{OUT}$ to GND, $C_L$ = 100 pF.
Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions | |
|---|---|---|---|---|---|---|---|
| -3 dB Bandwidth (see **C.16 "-3 dB Bandwidth"**) | BW | — | 60 | — | kHz | $V_{REF}$ = 3.00V ± 2V, VRxB:VRxA = 10, Gx = 0 | |
| | | — | 35 | — | | $V_{REF}$ = 3.50V ± 1.5V, VRxB:VRxA = 10, Gx = 1 | |
| **Output Amplifier (Op Amp)** | | | | | | | |
| Phase Margin[1] | PM | — | 58 | — | °C | $R_L$ = ∞ | |
| Slew Rate | SR | — | 0.15 | — | V/µs | $R_L$ = 2 kΩ | |
| Load Regulation | — | — | 130 | — | µV/mA | 1 mA ≤ I ≤ 6 mA | $V_{DD}$ = 5.5V, DAC code = Mid-Scale |
| | | — | 320 | — | µV/mA | -6 mA ≤ I ≤ -1 mA | |
| Short-Circuit Current | $I_{SC_OA}$ | 6 | 10 | 14 | mA | Short to $V_{SS}$ | DAC code = Full Scale |
| | | 6 | 10 | 14 | mA | Short to $V_{DD}$ | DAC code = Zero Scale |
| Settling Time[8] | $t_{SETTLING}$ | — | 16 | — | µs | $R_L$ = 2 kΩ | |
| **Internal Band Gap** | | | | | | | |
| Band Gap Voltage | $V_{BG}$ | 1.180 | 1.214 | 1.260 | V | 1.8V ≤ $V_{DD}$ ≤ 5.5V | |
| Short-Circuit Current | $I_{SC_BG}$ | 6 | 10 | 14 | mA | Short to $V_{SS}$ | |
| | | 6 | 10 | 14 | mA | Short to $V_{DD}$ | |
| Band Gap Voltage Temperature Coefficient | $V_{BGTC}$ | — | 16 | — | ppm/°C | 1.8V ≤ $V_{DD}$ ≤ 5.5V | |
| Band Gap mode, $V_{REF}$ Pin Load Regulation | $I_{BG}$ | — | 30 | — | µV/mA | 1 mA ≤ I ≤ 6 mA | $V_{DD}$ = 5.5V |
| | | — | 390 | — | µV/mA | -6 mA ≤ I ≤ -1 mA | |

**Note 1** This parameter is ensured by design.

**Note 8** Within 1/2 LSb of the final value, when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device.)

## DC CHARACTERISTICS (CONTINUED)

**Standard Operating Conditions (unless otherwise specified)**:
Operating Temperature: -40°C ≤ $T_A$ ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
$V_{DD}$ = +2.7V to 5.5V, $V_{REF}$ = +1.000V to $V_{DD}$, $V_{SS}$ = 0V, $R_L$ = 2 kΩ from $V_{OUT}$ to GND, $C_L$ = 100 pF.
Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **External Reference ($V_{REF}$)** | | | | | | |
| Input Range(1) | $V_{REF}$ | $V_{SS}$ | — | $V_{DD}$ | V | VRxB:VRxA = 10 (Unbuffered mode) |
| Input Capacitance | $C_{REF}$ | — | 29 | — | pF | VRxB:VRxA = 10 (Unbuffered mode) |
| Input Impedance | $R_L$ | See **Resistor Ladder Resistance(6)** | | | kΩ | 2.7V ≤ $V_{DD}$ ≤ 5.5V, VRxB:VRxA = 10, $V_{REF}$ = $V_{DD}$ |
| Current through $V_{REF}$(1) | $I_{VREF}$ | — | — | 172.15 | µA | Mathematically from $R_{VREF(min)}$ spec (at 5.5V) |
| Total Harmonic Distortion(1) | THD | — | -76 | — | dB | $V_{REF}$ = 2.048V ± 0.1V, VRxB:VRxA = 10, Gx = 0, Frequency = 1 kHz |
| **Dynamic Performance** | | | | | | |
| Major Code Transition Glitch (see **C.14 "Major Code Transition Glitch"**) | — | — | 10 | — | nV-s | 1 LSb change around major carry (7FFh to 800h) |
| Digital Feedthrough (see **C.15 "Digital Feedthrough"**) | — | — | <2 | — | nV-s | |

**Note 1** This parameter is ensured by design.

**Note 6** Resistance is defined as the resistance between the $V_{REF}$ pin (mode VRxB:VRxA = 10) to the $V_{SS}$ pin. For dual channel devices (MCP47CXBX2), this is the effective resistance of each resistor ladder. The resistance measurement is one of the two resistor ladders measured in parallel.


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## DC CHARACTERISTICS (CONTINUED)

**Standard Operating Conditions (unless otherwise specified)**:
Operating Temperature: -40°C ≤ $T_A$ ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
$V_{DD}$ = +2.7V to 5.5V, $V_{REF}$ = +1.000V to $V_{DD}$, $V_{SS}$ = 0V, $R_L$ = 2 kΩ from $V_{OUT}$ to GND, $C_L$ = 100 pF.
Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions | |
|---|---|---|---|---|---|---|---|
| **Digital Inputs/Outputs ($\overline{LAT0}$/HVC, LAT1, A0, A1)** | | | | | | | |
| Schmitt Trigger High Input Threshold | $V_{IH}$ | 0.45 $V_{DD}$ | — | — | V | 1.8V ≤ $V_{DD}$ ≤ 5.5V (allows 2.7V digital $V_{DD}$ with 5.5V analog $V_{DD}$ or 1.8V digital $V_{DD}$ with 3.0V analog $V_{DD}$) | |
| Schmitt Trigger Low Input Threshold | $V_{IL}$ | — | — | 0.2 $V_{DD}$ | V | | |
| Hysteresis of Schmitt Trigger Inputs | $V_{HYS}$ | — | 0.1 $V_{DD}$ | — | V | | |
| Input Leakage Current | $I_{IL}$ | -1 | — | 1 | µA | $V_{IN}$ = $V_{DD}$ and $V_{IN}$ = $V_{SS}$ | |
| Pin Capacitance | $C_{IN}$, $C_{OUT}$ | — | 10 | — | pF | | |
| **Digital Interface (SDA, SCL)** | | | | | | | |
| Output Low Voltage | $V_{OL}$ | — | — | 0.4 | V | $V_{DD}$ ≥ 2.0V, $I_{OL}$ = 3 mA | |
| | | — | — | 0.2 $V_{DD}$ | V | $V_{DD}$ < 2.0V, $I_{OL}$ = 1 mA | |
| Input High Voltage (SDA and SCL pins) | $V_{IH}$ | 0.7 $V_{DD}$ | — | — | V | 1.8V ≤ $V_{DD}$ ≤ 5.5V | |
| Input Low Voltage (SDA and SCL pins) | $V_{IL}$ | — | — | 0.3 $V_{DD}$ | V | 1.8V ≤ $V_{DD}$ ≤ 5.5V | |
| Input Leakage | $I_L$ | -1 | — | 1 | µA | SCL = SDA = $V_{SS}$ or SCL = SDA = $V_{DD}$ | |
| Pin Capacitance | $C_{PIN}$ | — | 10 | — | pF | | |
| **RAM Value** | | | | | | | |
| Value Range | N | 0h | — | FFh | Hex | 8-bit | |
| | | | — | 3FFh | | 10-bit | |
| | | | — | FFFh | | 12-bit | |
| DAC Register POR/BOR Value | N | See Table 4-2 | | | Hex | 8-bit | |
| | | | | | | 10-bit | |
| | | | | | | 12-bit | |
| PDCON Initial Factory Setting | — | See Table 4-2 | | | Hex | | |
| **Power Requirements** | | | | | | | |
| Power Supply Sensitivity (**C.17 "Power Supply Sensitivity (PSS)"**) | PSS | — | 0.0010 | 0.0035 | %/% | 8-bit | Code = Mid-Scale |
| | | — | | | | 10-bit | |
| | | — | | | | 12-bit | |

## DC CHARACTERISTICS (CONTINUED)

**Standard Operating Conditions (unless otherwise specified)**:
Operating Temperature: -40°C ≤ $T_A$ ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
$V_{DD}$ = +2.7V to 5.5V, $V_{REF}$ = +1.000V to $V_{DD}$, $V_{SS}$ = 0V, $R_L$ = 2 kΩ from $V_{OUT}$ to GND, $C_L$ = 100 pF.
Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Multi-Time Programming Memory (MTP)** | | | | | | |
| MTP Programming Voltage(1) | $V_{PG_MTP}$ | 2.0 | — | 5.5 | V | HVC = $V_{IHH}$, -20°C ≤ $T_A$ ≤ +125°C |
| $\overline{LAT}$/HVC Pin Voltage for MTP Programming (high-voltage commands) | $V_{IHH}$ | 7.25 | 7.5 | 7.75V | V | The $\overline{LAT}$/HVC pin will be at one of the three input levels ($V_{IL}$, $V_{IH}$ or $V_{IHH}$)(1,11), the $\overline{LAT}$/HVC pin must supply the required MTP programming current (up to 6.4 mA) |
| Writes Cycles | — | — | — | 32(12) | Cycles | **Note 1** |
| Data Retention | $DR_{MTP}$ | 10 | — | — | Years | At +85°C(1) |
| MTP Range | N | 0h | — | FFh | Hex | 8-bit |
| | | 0h | — | 3FFh | Hex | 10-bit |
| | | 0h | — | FFFh | Hex | 12-bit |
| | | 0000h | | 7FFFh | Hex | All general purpose memory |
| Initial Factory Setting | N | See Table 4-2 | | | — | |
| MTP Programming Write Cycle Time(1) | $t_{WC(MTP)}$ | — | — | 250 | µs | $V_{DD}$ = +2.0V to 5.5V, -20°C ≤ $T_A$ ≤ +125°C |

**Note 1** This parameter is ensured by design.

**Note 11** High-voltage on the LAT/HVC pin must be limited to the command + programming time. After the programming cycle, the LAT/HVC pin voltage must be returned to 5.5V or lower.

**Note 12** After 32 MTP write cycles, writes are inhibited and the 32nd write value is retained (not corrupted).


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### DC Notes:

1. This parameter is ensured by design.
2. This parameter is ensured by characterization.
3. POR/BOR voltage trip point is not slope-dependent. Hysteresis implemented with time delay.
4. Supply current is independent of current through the resistor ladder in mode VRxB:VRxA = `10`.
5. The PDxB:PDxA = `01`, `10` and `11` configurations should have the same current.
6. Resistance is defined as the resistance between the $V_{REF}$ pin (mode VRxB:VRxA = `10`) to the $V_{SS}$ pin. For dual channel devices (MCP47CXBX2), this is the effective resistance of each resistor ladder. The resistance measurement is one of the two resistor ladders measured in parallel.
7. This gain error does not include the offset error.
8. Within 1/2 LSb of the final value, when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device.)
9. Code range dependent on resolution: 8-bit, codes 4 to 252; 10-bit, codes 16 to 1008; 12-bit, codes 64 to 4032.
10. Variation of one output voltage to mean output voltage for dual devices only.
11. High-voltage on the $\overline{LAT}$/HVC pin must be limited to the command + programming time. After the programming cycle, the $\overline{LAT}$/HVC pin voltage must be returned to 5.5V or lower.
12. After 32 MTP write cycles, writes are inhibited and the 32nd write value is retained (not corrupted).

## 1.1 Timing Waveforms and Requirements

### 1.1.1 WIPER SETTLING TIME

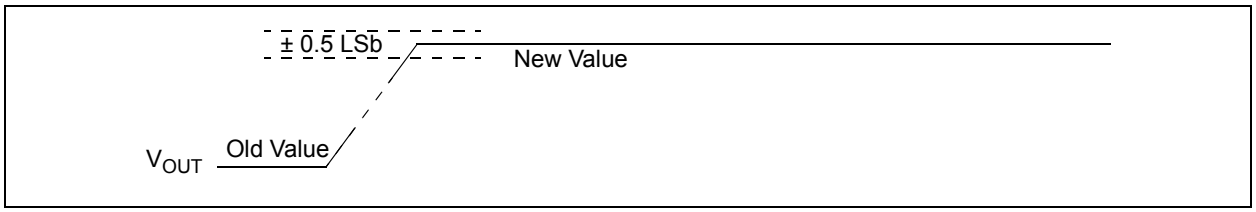



***FIGURE 1-1:*** *$V_{OUT}$ Settling Time Waveforms.*

**TABLE 1-1: WIPER SETTLING TIMING**

| **Timing Characteristics** | | **Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ $T_A$ ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. $V_{DD}$ = +2.7V to 5.5V, $V_{SS}$ = 0V, $R_L$ = 2 kΩ from $V_{OUT}$ to GND, $C_L$ = 100 pF. Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C. | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameters** | **Sym.** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** | |
| $V_{OUT}$ Settling Time (see C.13 "Settling Time") | $t_S$ | — | 16 | — | µs | 12-bit | Code = 400h → C00h; C00h → 400h(2) |

**Note 2** Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR.

### 1.1.2 LATCH PIN ($\overline{LAT}$) TIMING

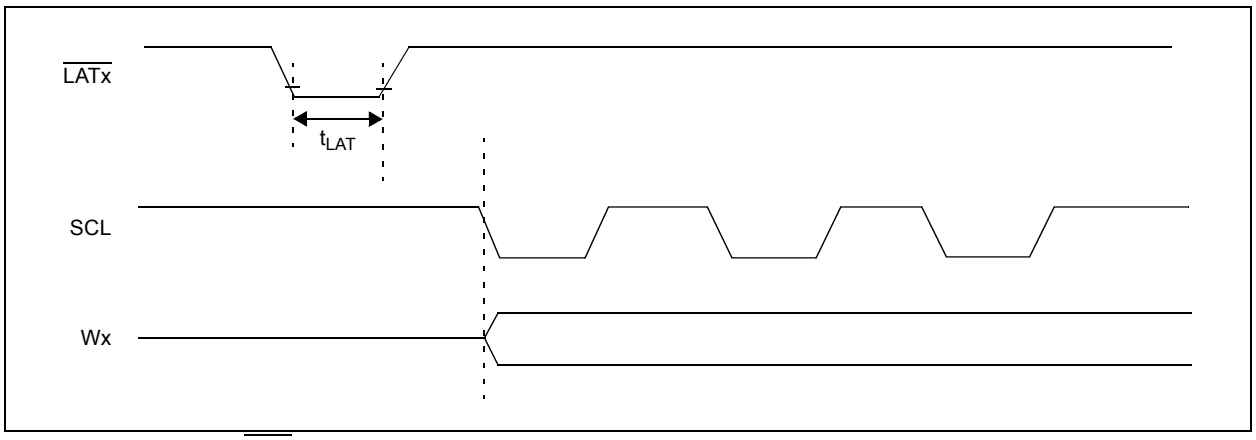



***FIGURE 1-2:*** *$\overline{LAT}$ Pin Waveforms.*

**TABLE 1-2: $\overline{LAT}$ PIN TIMING**

| **Timing Characteristics** | | **Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ $T_A$ ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. $V_{DD}$ = +2.7V to 5.5V, $V_{SS}$ = 0V, RL = 2 kΩ from $V_{OUT}$ to GND, $C_L$ = 100 pF. Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C. | | | | |
|---|---|---|---|---|---|---|
| **Parameters** | **Sym.** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| $\overline{LATx}$ pin pulse width | $t_{LAT}$ | 20 | — | — | ns | |


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## 1.2 I²C Mode Timing Waveforms and Requirements

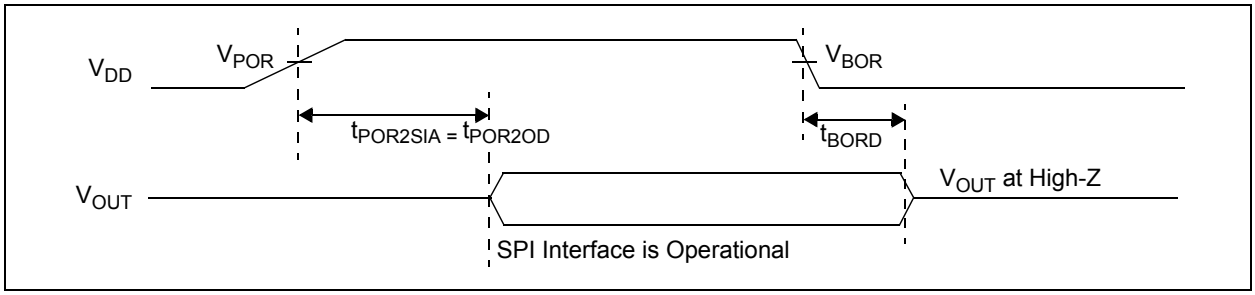



***FIGURE 1-3:*** *Power-on and Brown-out Reset Waveforms.*

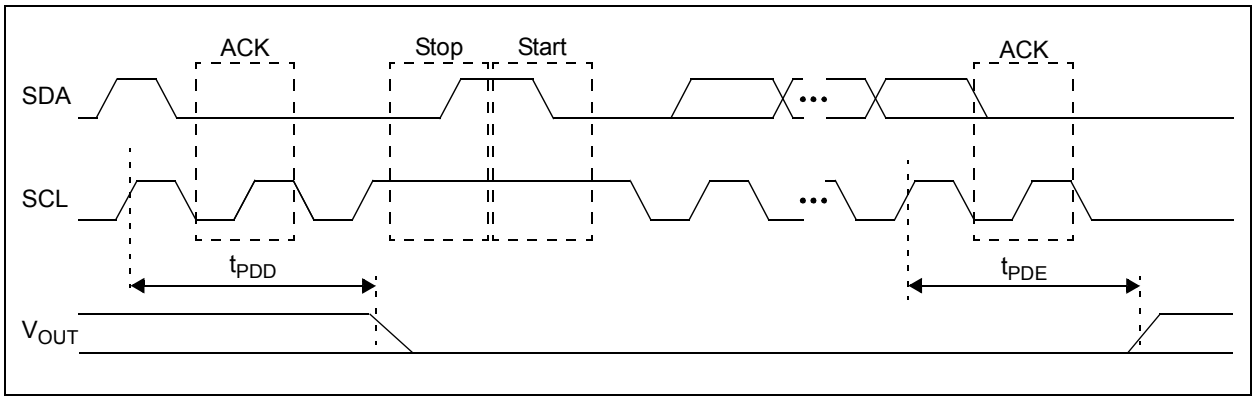
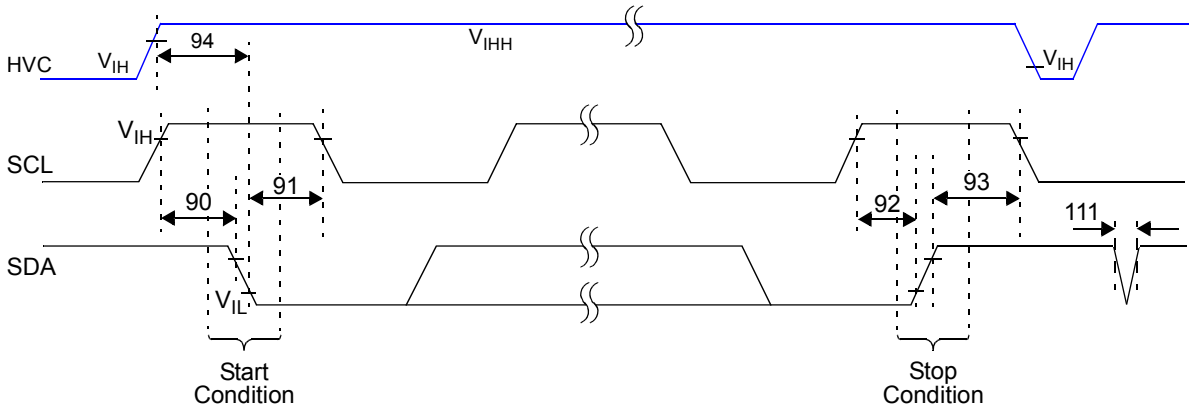



***FIGURE 1-4:*** *I²C Power-Down Command Timing.*

**TABLE 1-3: RESET TIMING**

| **Timing Characteristics** | | **Standard Operating Conditions (unless otherwise specified)**: Operating Temperature: -40°C ≤ $T_A$ ≤ +125°C (Extended)<br>All parameters apply across the specified operating ranges unless noted. $V_{DD}$ = +2.7V to 5.5V, $V_{SS}$ = 0V, $R_L$ = 2 kΩ from $V_{OUT}$ to GND, $C_L$ = 100 pF. Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C. | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameters** | **Sym.** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** | |
| Power-on Reset Delay(1) | $t_{POR2SIA}$ | — | — | 130 | µs | Single | Monitor ACK bit response to ensure the device responds to command |
| | | — | — | 145 | | Dual | |
| Brown-out Reset Delay | $t_{BORD}$ | — | 30 | — | µs | $V_{DD}$ transitions from $V_{DD(MIN)} \rightarrow > V_{POR}$, $V_{OUT}$ driven to $V_{OUT}$ disabled | |
| Power-Down Output Enable Time Delay | $T_{PDE}$ | — | 1.5 | — | µs | PDxB:PDxA = `11`, `10`, or `01` ≥ `00` started from the rising edge of the SCL at the end of the 8th clock cycle, Volatile DAC register = FFFh, $V_{OUT}$ = 10 mV, $V_{OUT}$ not connected | |
| Power-Down Output Disable Time Delay | $T_{PDD}$ | — | 0.025 | — | µs | PDxB:PDxA = `00` → `11`, `10` or `01` started from the rising edge of the SCL at the end of the 8th clock cycle, $V_{OUT}$ = $V_{OUT}$ – 10 mV, $V_{OUT}$ not connected | |

**Note 1** Not tested. This parameter is ensured by characterization.




**Note 1:** The HVC pin must be at $V_{IHH}$ until the MTP write cycle is complete.

***FIGURE 1-5:*** *$I^2C$ Bus Start/Stop Bits and HVC Timing Waveforms.*


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**TABLE 1-4: I²C BUS START/STOP BITS AND $\overline{LAT}$ REQUIREMENTS**

| **I²C AC Characteristics** | | | | **Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ $T_A$ ≤ +125°C (Extended). The operating voltage range is described in **DC Characteristics**. | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym.** | **Characteristic** | | **Min.** | **Max.** | **Units** | **Conditions** |
| — | $F_{SCL}$ | SCL Pin Frequency | Standard mode | 0 | 100 | kHz | $C_b$ = 400 pF, 1.8V-5.5V(1) |
| | | | Fast mode | 0 | 400 | kHz | $C_b$ = 400 pF, 2.7V-5.5V |
| | | | High Speed 1.7 | 0 | 1.7 | MHz | $C_b$ = 400 pF, 4.5V-5.5V(1) |
| | | | High Speed 3.4 | 0 | 3.4 | MHz | $C_b$ = 100 pF, 4.5V-5.5V(1) |
| 90 | $T_{SU:STA}$ | Start Condition Setup Time (only relevant for Repeated Start condition) | 100 kHz mode | 4700 | — | ns | **Note 1** |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1.7 MHz mode | 160 | — | ns | **Note 1** |
| | | | 3.4 MHz mode | 160 | — | ns | |
| 91 | $T_{HD:STA}$ | Start Condition Hold Time (after this period, the first clock pulse is generated) | 100 kHz mode | 4000 | — | ns | **Note 1** |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1.7 MHz mode | 160 | — | ns | **Note 1** |
| | | | 3.4 MHz mode | 160 | — | ns | |
| 92 | $T_{SU:STO}$ | Stop Condition Setup Time | 100 kHz mode | 4000 | — | ns | **Note 1** |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1.7 MHz mode | 160 | — | ns | **Note 1** |
| | | | 3.4 MHz mode | 160 | — | ns | |
| 93 | $T_{HD:STO}$ | Stop Condition Hold Time | 100 kHz mode | 4000 | — | ns | **Note 1** |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1.7 MHz mode | 160 | — | ns | **Note 1** |
| | | | 3.4 MHz mode | 160 | — | ns | |
| 94 | $T_{HVCSU}$ | HVC High to Start Condition (setup time) | | 0 | — | µs | Not tested, specification ensured by Master |

**Note 1** Not tested. This parameter is ensured by characterization.

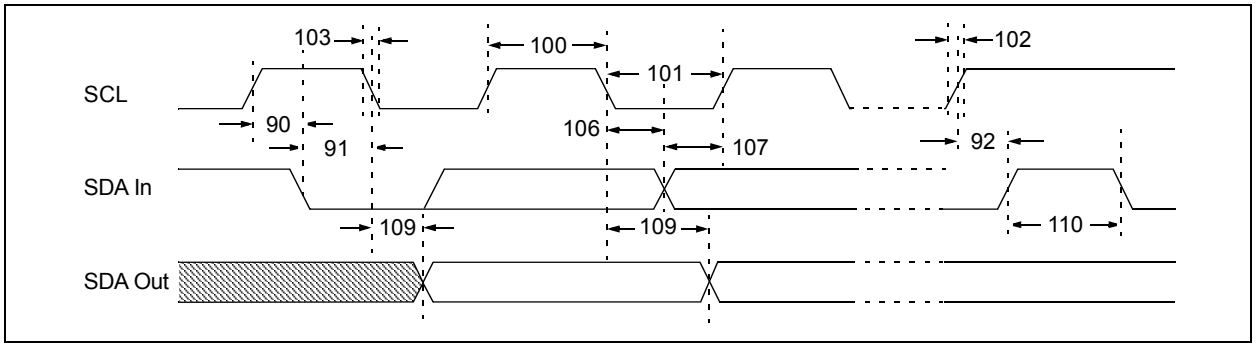



***FIGURE 1-6:*** *$I^2C$ Bus Data Timing Waveforms.*

**TABLE 1-5: $I^2C$ BUS REQUIREMENTS (SLAVE MODE)**

| **$I^2C$ AC Characteristics** | | | **Standard Operating Conditions (unless otherwise specified)**: Operating Temperature: -40°C ≤ $T_A$ ≤ +125°C (Extended). The operating voltage range is described in **DC Characteristics**. | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym.** | **Characteristic** | | **Min.** | **Max.** | **Units** | **Conditions** |
| 100 | $T_{HIGH}$ | Clock High Time | 100 kHz mode | 4000 | — | ns | 1.8V-5.5V(1) |
| | | | 400 kHz mode | 600 | — | ns | 2.7V-5.5V |
| | | | 1.7 MHz mode | 120 | — | ns | 4.5V-5.5V(1) |
| | | | 3.4 MHz mode | 60 | — | ns | 4.5V-5.5V(1) |
| 101 | $T_{LOW}$ | Clock Low Time | 100 kHz mode | 4700 | — | ns | 1.8V-5.5V(1) |
| | | | 400 kHz mode | 1300 | — | ns | 2.7V-5.5V |
| | | | 1.7 MHz mode | 320 | — | ns | 4.5V-5.5V(1) |
| | | | 3.4 MHz mode | 160 | — | ns | 4.5V-5.5V(1) |
| 102A(10) | $T_{RSCL}$ | SCL Rise Time | 100 kHz mode | — | 1000 | ns | $C_b$ is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode) |
| | | | 400 kHz mode | 20 + 0.1$C_b$(4) | 300 | ns | |
| | | | 1.7 MHz mode | 20 | 80 | ns | |
| | | | 1.7 MHz mode | 20 | 160 | ns | After a Repeated Start condition or an Acknowledge bit |
| | | | 3.4 MHz mode | 10 | 40 | ns | |
| | | | 3.4 MHz mode | 10 | 80 | ns | After a Repeated Start condition or an Acknowledge bit |
| 102B(10) | $T_{RSDA}$ | SDA Rise Time | 100 kHz mode | — | 1000 | ns | Cb is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode) |
| | | | 400 kHz mode | 20 + 0.1$C_b$ | 300 | ns | |
| | | | 1.7 MHz mode | 20 | 160 | ns | |
| | | | 3.4 MHz mode | 10 | 80 | ns | |
| 103A(10) | $T_{FSCL}$ | SCL Fall Time | 100 kHz mode | — | 300 | ns | $C_b$ is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)(4) |
| | | | 400 kHz mode | 20 + 0.1$C_b$ | 300 | ns | |
| | | | 1.7 MHz mode | 20 | 80 | ns | |
| | | | 3.4 MHz mode | 10 | 40 | ns | |

**Note 1** Not tested. This parameter is ensured by characterization.

**Note 4** Use Cb in pF for the calculations.

**Note 10** Not tested. This parameter is ensured by design.


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**TABLE 1-5: I²C BUS REQUIREMENTS (SLAVE MODE) (CONTINUED)**

| I²C AC Characteristics | | | | Standard Operating Conditions (unless otherwise specified): Operating Temperature: -40°C ≤ $T_A$ ≤ +125°C (Extended). The operating voltage range is described in DC Characteristics. | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym.** | **Characteristic** | | **Min.** | **Max.** | **Units** | **Conditions** |
| 103B(10) | $T_{FSDA}$ | SDA Fall Time | 100 kHz mode | — | 300 | ns | $C_b$ is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)(4) |
| | | | 400 kHz mode | 20 + 0.1$C_b$ | 300 | ns | |
| | | | 1.7 MHz mode | 20 | 160 | ns | |
| | | | 3.4 MHz mode | 10 | 80 | ns | |
| 106 | $T_{HD:DAT}$ | Data Input Hold Time | 100 kHz mode | 0 | — | ns | 1.8V-5.5V(1,5) |
| | | | 400 kHz mode | 0 | — | ns | 2.7V-5.5V(5) |
| | | | 1.7 MHz mode | 0 | — | ns | 4.5V-5.5V(1,5) |
| | | | 3.4 MHz mode | 0 | — | ns | 4.5V-5.5V(1,5) |
| 107 | $T_{SU:DAT}$ | Data Input Setup Time | 100 kHz mode | 250 | — | ns | Notes 1, 6 |
| | | | 400 kHz mode | 100 | — | ns | Note 6 |
| | | | 1.7 MHz mode | 10 | — | ns | Notes 1, 6 |
| | | | 3.4 MHz mode | 10 | — | ns | Notes 1, 6 |
| 109 | $T_{AA}$ | Output Valid from Clock | 100 kHz mode | — | 3450 | ns | Notes 1, 5, 7, 9 |
| | | | 400 kHz mode | — | 900 | ns | Notes 5, 7, 9 |
| | | | 1.7 MHz mode | — | 310 | ns | $C_b$ = 400 pF(1,9) |
| | | | 3.4 MHz mode | — | 150 | ns | $C_b$ = 100 pF(1,9) |
| 110 | $T_{BUF}$ | Bus Free Time | 100 kHz mode | 4700 | — | ns | Time the bus must be free before a new transmission can start(1) |
| | | | 400 kHz mode | 1300 | — | ns | |
| | | | 1.7 MHz mode | N.A. | — | ns | |
| | | | 3.4 MHz mode | N.A. | — | ns | |
| 111 | $T_{SP}$ | Input Filter Spike Suppression (SDA and SCL) | 100 kHz mode | — | 50 | ns | NXP Spec states N.A.(1) |
| | | | 400 kHz mode | — | 50 | ns | NXP Spec states N.A. |
| | | | 1.7 MHz mode | — | 10 | ns | NXP Spec states N.A.(1) |
| | | | 3.4 MHz mode | — | 10 | ns | NXP Spec states N.A.(1) |

**Note 1** Not tested. This parameter is ensured by characterization.

**Note 4** Use Cb in pF for the calculations.

**Note 5** A Master transmitter must provide a delay to ensure that the difference between SDA and SCL fall times does not unintentionally create a Start or Stop condition.

**Note 6** A Fast mode (400 kHz) I²C bus device can be used in a Standard mode (100 kHz) I²C bus system, but the requirement, $t_{SU:DAT} \geq 250$ ns, must then be met. This will automatically be the case if the device does not stretch the Low period of the SCL signal. If such a device does stretch the Low period of the SCL signal, it must output the next data bit to the SDA line, $T_R$ max.+ $t_{SU:DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification) before the SCL line is released.

**Note 7** As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

**Note 8** Ensured by the $T_{AA}$ 3.4 MHz specification test.

**Note 9** The specification is not part of the I²C specification. $T_{AA} = T_{HD:DAT} + T_{FSDA}$ (or $T_{RSDA}$).

**Note 10** Not tested. This parameter is ensured by design.

### Timing Notes:

1. Not tested. This parameter is ensured by characterization.
2. Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR.
3. The transition of the $\overline{LAT}$ signal, between 10 ns before the rising edge (Spec 94) and 250 ns after the rising edge (Spec 95) of the SCL signal, is indeterminate whether the change in $V_{OUT}$ is delayed or not.
4. Use $C_b$ in pF for the calculations.
5. A Master transmitter must provide a delay to ensure that the difference between SDA and SCL fall times does not unintentionally create a Start or Stop condition.
6. A Fast mode (400 kHz) $I^2C$ bus device can be used in a Standard mode (100 kHz) $I^2C$ bus system, but the requirement, $t_{SU:DAT} \geq 250$ ns, must then be met. This will automatically be the case if the device does not stretch the Low period of the SCL signal. If such a device does stretch the Low period of the SCL signal, it must output the next data bit to the SDA line, $T_R$ max.+ $t_{SU:DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode $I^2C$ bus specification) before the SCL line is released.
7. As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.
8. Ensured by the $T_{AA}$ 3.4 MHz specification test.
9. The specification is not part of the $I^2C$ specification. $T_{AA} = T_{HD:DAT} + T_{FSDA}$ (or $T_{RSDA}$).
10. Not tested. This parameter is ensured by design.


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## TEMPERATURE SPECIFICATIONS

| **Electrical Specifications:** Unless otherwise indicated, $V_{DD}$ = +2.7V to +5.5V, $V_{SS}$ = GND. | | | | | | |
|---|---|---|---|---|---|---|
| **Parameters** | **Sym.** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| **Temperature Ranges** | | | | | | |
| Specified Temperature Range | $T_A$ | -40 | — | +125 | °C | |
| Operating Temperature Range | $T_A$ | -40 | — | +125 | °C | |
| Storage Temperature Range | $T_A$ | -65 | — | +150 | °C | |
| **Thermal Package Resistances** | | | | | | |
| Thermal Resistance, 10L-MSOP | $\theta_{JA}$ | — | 206 | — | °C/W | |
| Thermal Resistance, 10L-DFN (3x3) | $\theta_{JA}$ | — | 91 | — | °C/W | |
| Thermal Resistance, 16L-QFN (3x3) | $\theta_{JA}$ | — | 58 | — | °C/W | |

**NOTES:**


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## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range), and therefore, outside the warranted range.

### 2.1 Electrical Data

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5.5V.

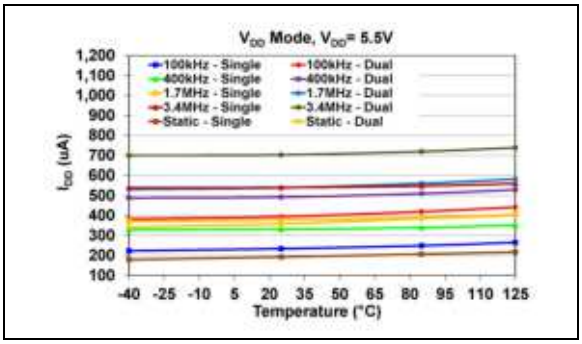



***FIGURE 2-1:*** *Average Device Supply Current vs. $F_{SCL}$ Frequency, Voltage and Temperature – Active Interface, VRxB:VRxA = 00, ($V_{DD}$ Mode).*

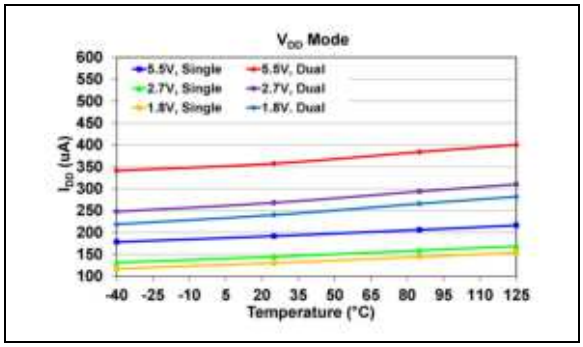



***FIGURE 2-4:*** *Average Device Supply Current – Inactive Interface (SCL = $V_{IH}$ or $V_{IL}$) vs. Voltage and Temperature, VRxB:VRxA = 00 ($V_{DD}$ Mode).*

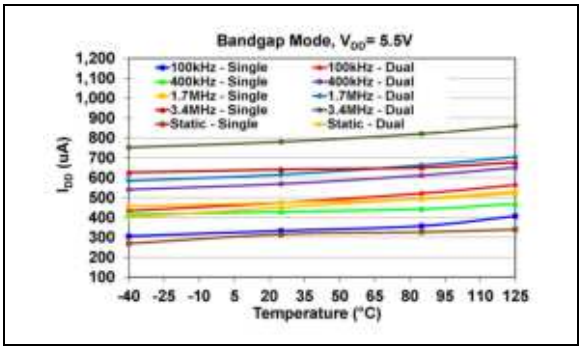



***FIGURE 2-2:*** *Average Device Supply Current vs. $F_{SCL}$ Frequency, Voltage and Temperature – Active Interface, VRxB:VRxA = 01 (Band Gap Mode).*

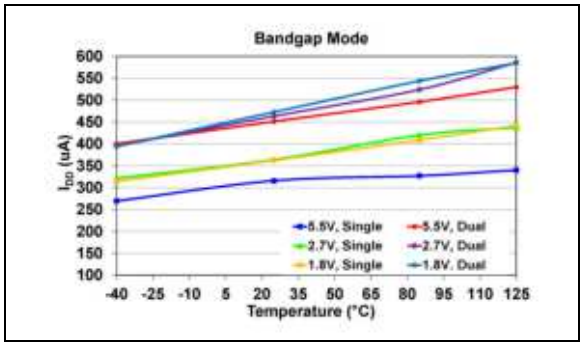



***FIGURE 2-5:*** *Average Device Supply Current – Inactive Interface (SCL = $V_{IH}$ or $V_{IL}$) vs. Voltage and Temperature, VRxB:VRxA = 01 (Band Gap Mode).*

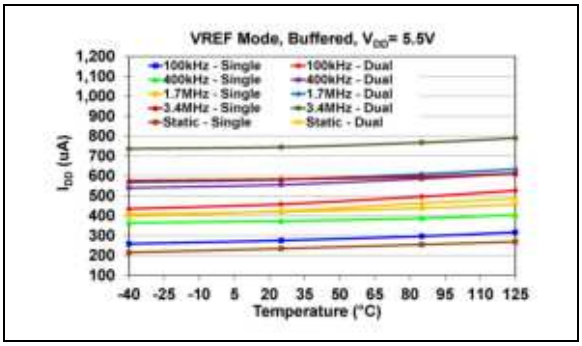



***FIGURE 2-3:*** *Average Device Supply Current vs. $F_{SCL}$ Frequency, Voltage and Temperature – Active Interface, VRxB:VRxA = 11 ($V_{REF}$ Buffered Mode).*

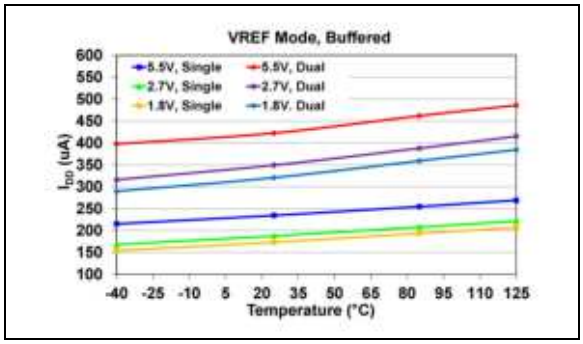



***FIGURE 2-6:*** *Average Device Supply Current – Inactive Interface (SCL = $V_{IH}$ or $V_{IL}$) vs. Voltage and Temperature, VRxB:VRxA = 11 ($V_{REF}$ Buffered Mode).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5.5V.

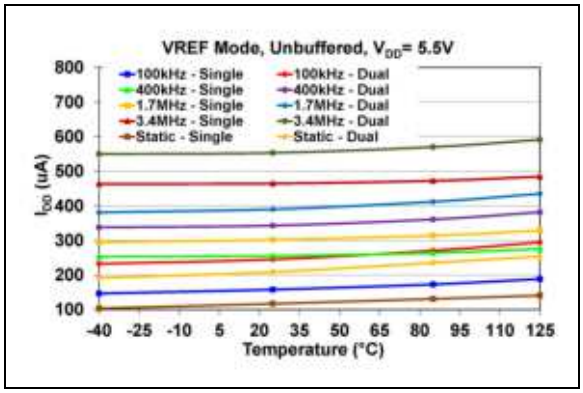



***FIGURE 2-7:*** *Average Device Supply Current vs. $F_{SCL}$ Frequency, Voltage and Temperature – Active Interface, VRxB:VRxA = 10 ($V_{REF}$ Unbuffered Mode).*

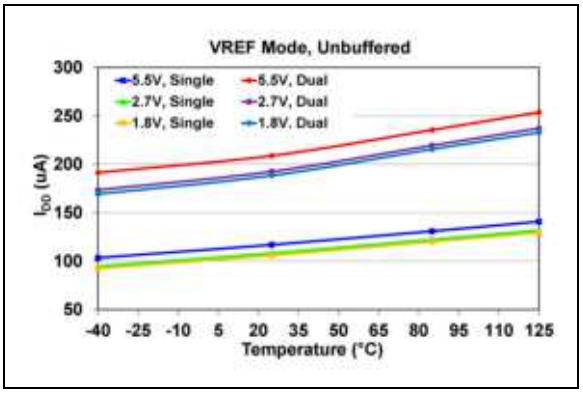



***FIGURE 2-9:*** *Average Device Supply Current – Inactive Interface (SCL = $V_{IH}$ or $V_{IL}$) vs. Voltage and Temperature, VRxB:VRxA = 10 ($V_{REF}$ Unbuffered Mode).*

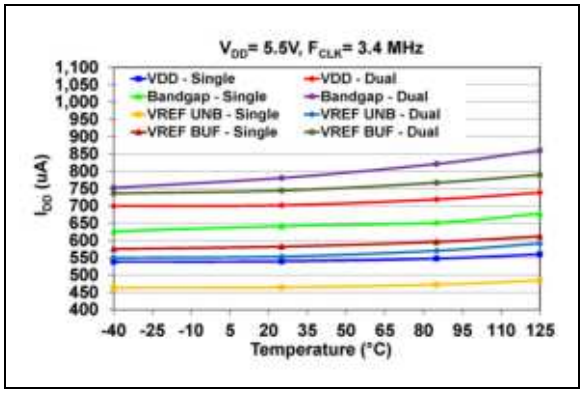



***FIGURE 2-8:*** *Average Device Supply Active Current ($I_{DDA}$) (at 5.5V and $F_{SCL}$ = 3.4 MHz) vs. Temperature and DAC Reference Voltage Mode.*


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## 2.2 Linearity Data

### 2.2.1 TOTAL UNADJUSTED ERROR (TUE) – MCP47CXB2X (12-BIT), $V_{REF} = V_{DD}$ (VRXB:VRXA = 10), GAIN = 1x, CODE 64-4032

**Note:** Unless otherwise indicated: $T_A$ = +25°C, $V_{DD}$ = 5.5V.

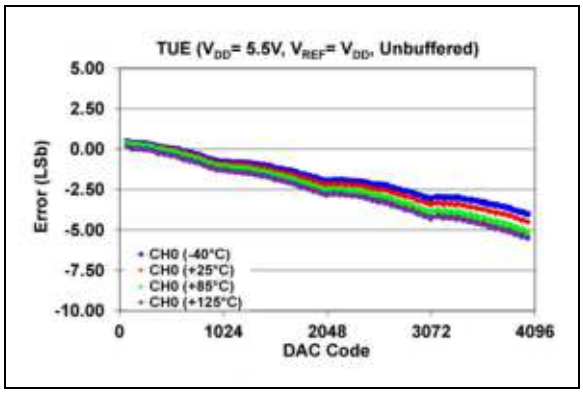



***FIGURE 2-10:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 5.5V.*

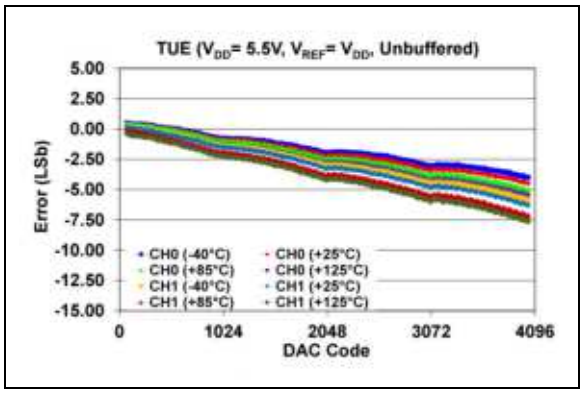



***FIGURE 2-13:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 5.5V.*

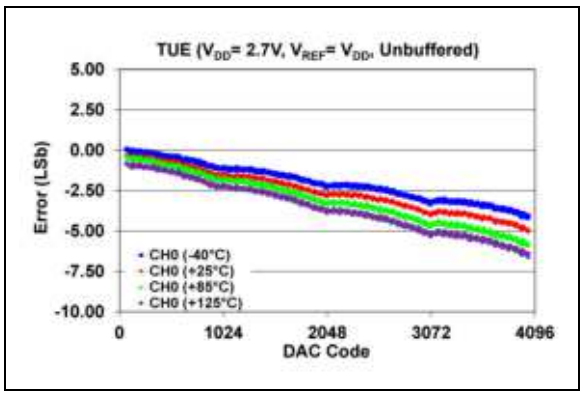



***FIGURE 2-11:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 2.7V.*

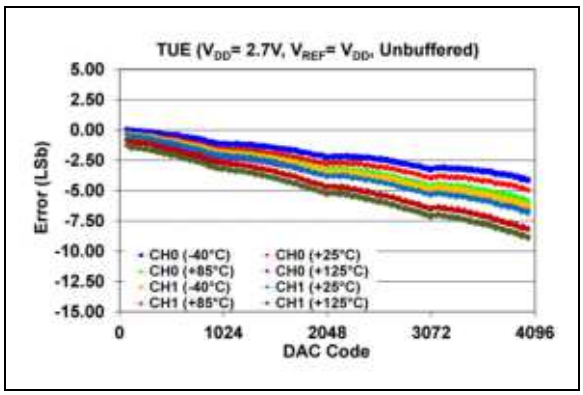



***FIGURE 2-14:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 2.7V.*

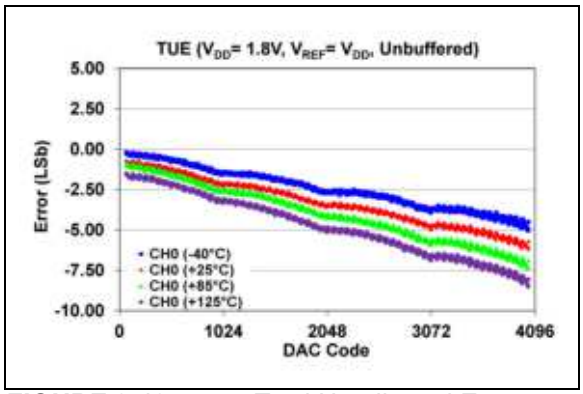



***FIGURE 2-12:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 1.8V.*

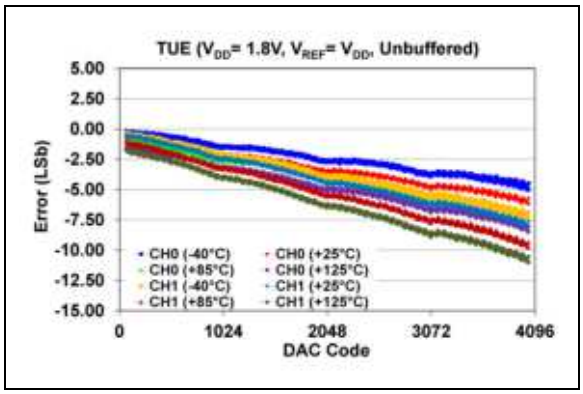



***FIGURE 2-15:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 1.8V.*

### 2.2.2 INTEGRAL NONLINEARITY (INL) – MCP47CXB2X (12-BIT), $V_{REF} = V_{DD}$ (VRXB:VRXA = 10), GAIN = 1x, CODE 64-4032

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5.5V.

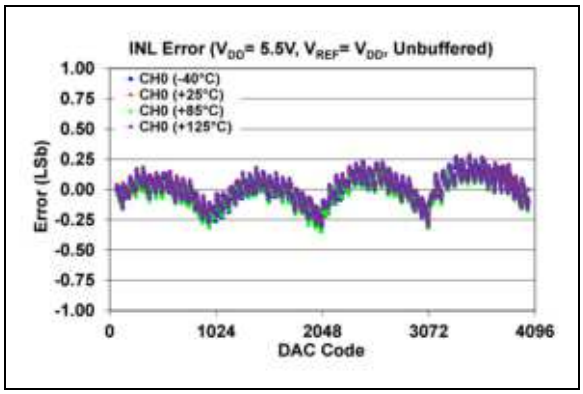



***FIGURE 2-16:*** *INL Error vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 5.5V.*

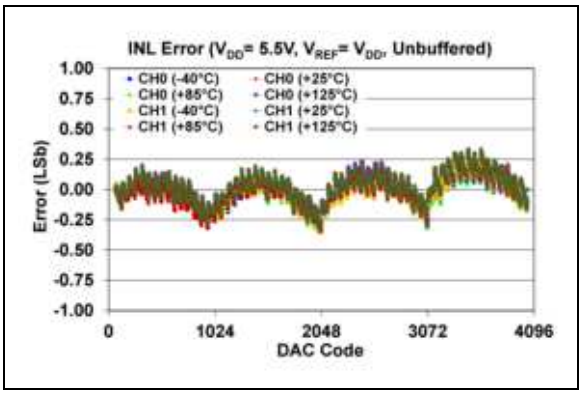



***FIGURE 2-19:*** *INL Error vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 5.5V.*

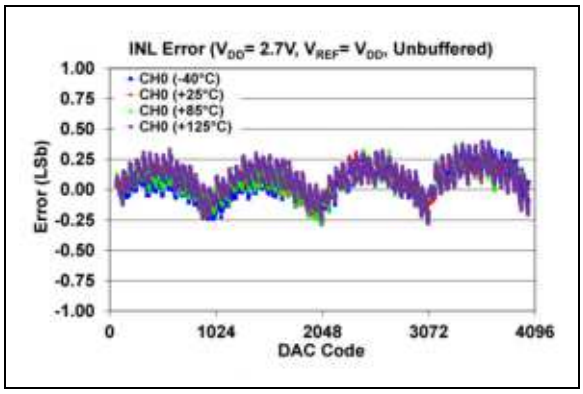



***FIGURE 2-17:*** *INL Error vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 2.7V.*

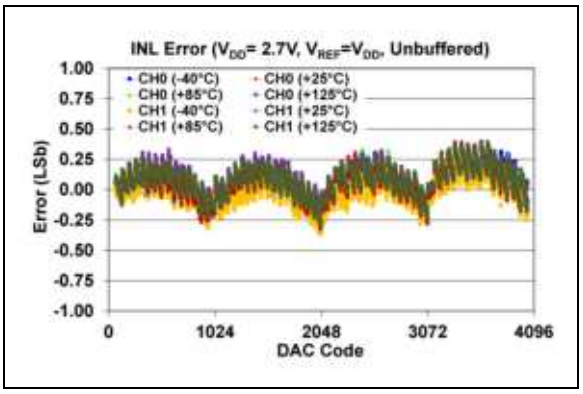



***FIGURE 2-20:*** *INL Error vs. DAC Code and Temperature (Code 100-4000) (Dual Channel – MCP47CXB22), $V_{DD}$ = 2.7V.*

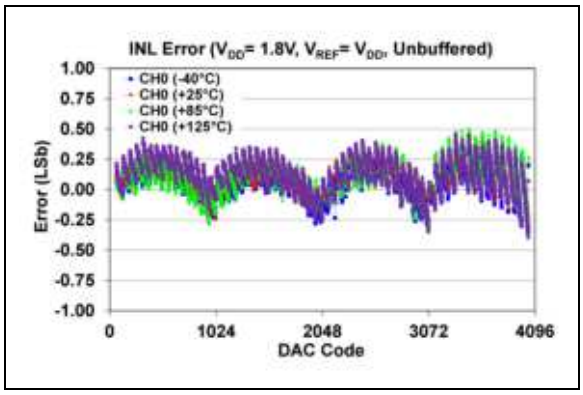



***FIGURE 2-18:*** *INL Error vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 1.8V.*

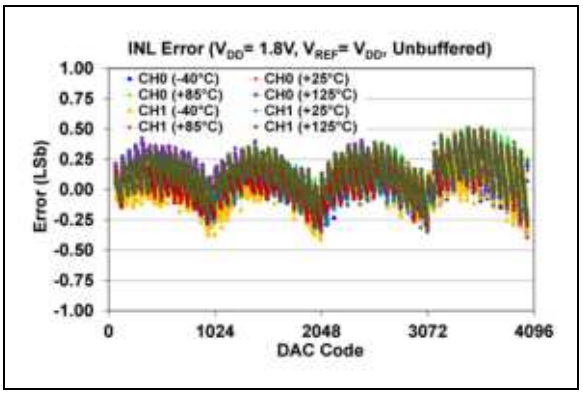



***FIGURE 2-21:*** *INL Error vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 1.8V.*


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### 2.2.3 DIFFERENTIAL NONLINEARITY (DNL) – MCP47CXB2X (12-BIT), $V_{REF} = V_{DD}$ (VRXB:VRXA = 10), GAIN = 1x, CODE 64-4032

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5.5V.

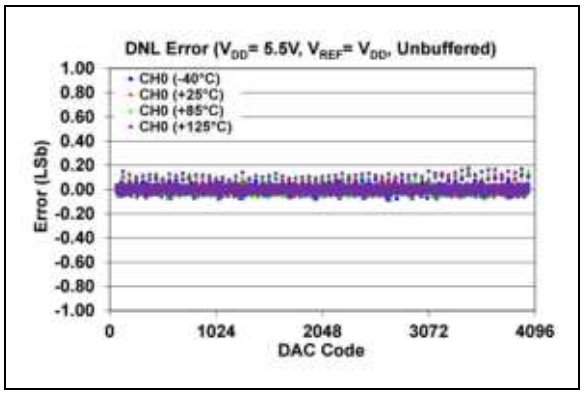



***FIGURE 2-22:*** *DNL Error vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 5.5V.*

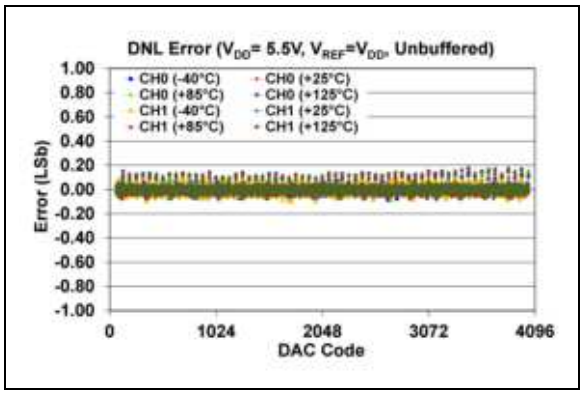



***FIGURE 2-25:*** *DNL Error vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 5.5V.*

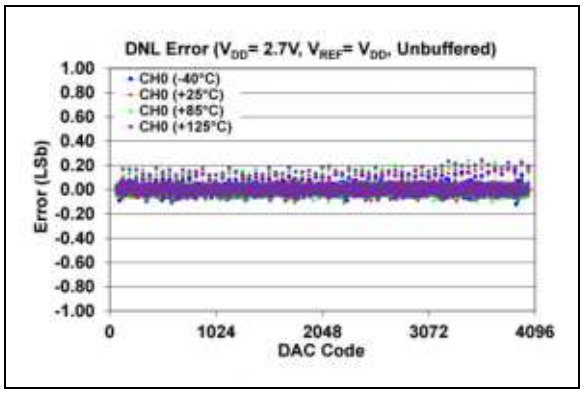



***FIGURE 2-23:*** *DNL Error vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 2.7V.*

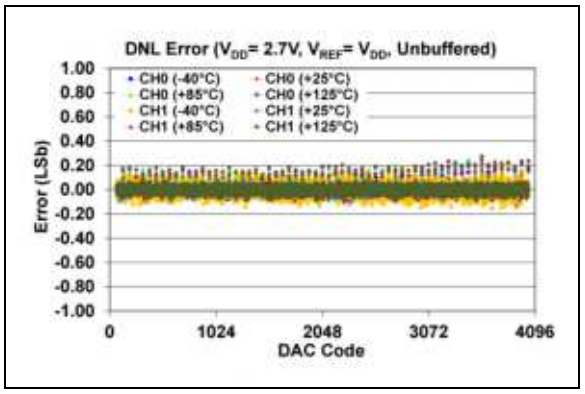



***FIGURE 2-26:*** *DNL Error vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 2.7V.*

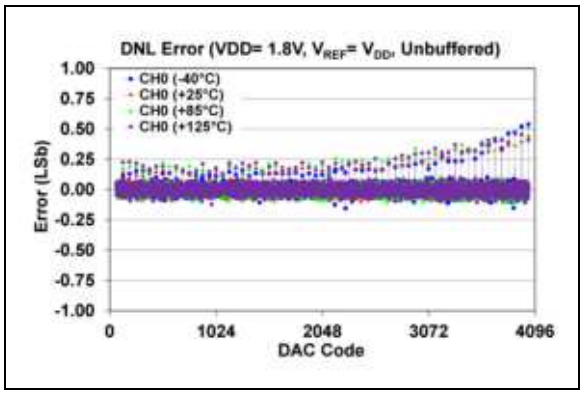



***FIGURE 2-24:*** *DNL Error vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 1.8V.*

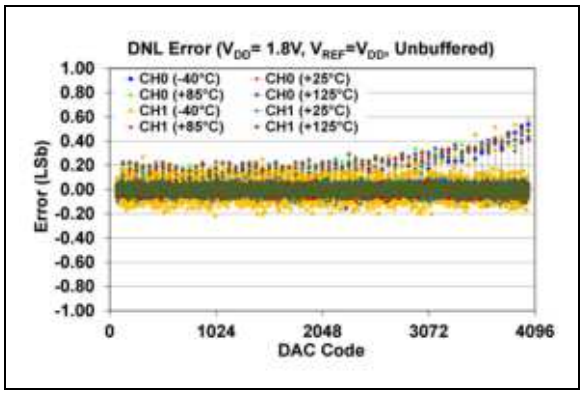



***FIGURE 2-27:*** *DNL Error vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 1.8V.*

### 2.2.4 TOTAL UNADJUSTED ERROR (TUE) – MCP47CXB2X (12-BIT), EXTERNAL $V_{REF}$ = 0.5 $V_{DD}$ (VRXB:VRXA = 10), UNBUFFERED, CODE 64-4032

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5.5V.

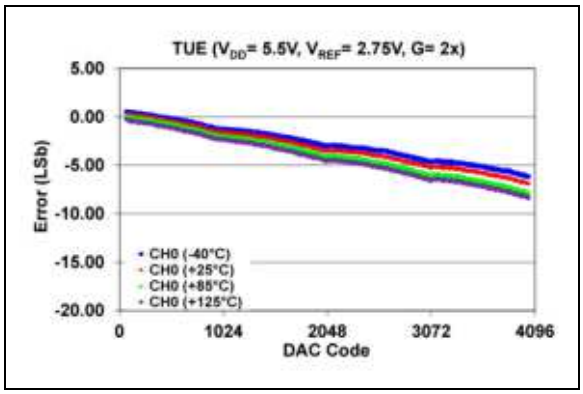



***FIGURE 2-28:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{REF}$ = 0.5 x $V_{DD}$ = 2.75V, Gain = 2x.*

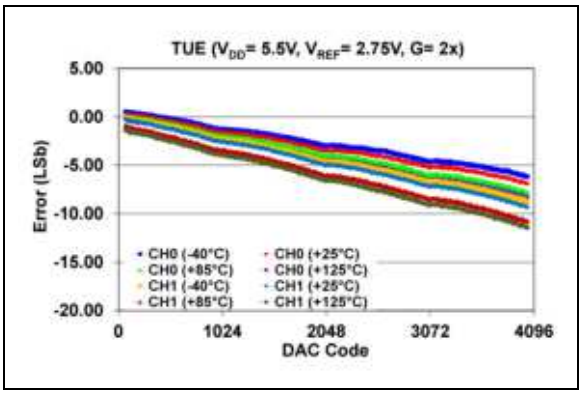



***FIGURE 2-30:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code, and Temperature (Dual Channel – MCP47CXB22), $V_{REF}$ = 0.5 x $V_{DD}$ = 2.75V, Gain = 2x.*

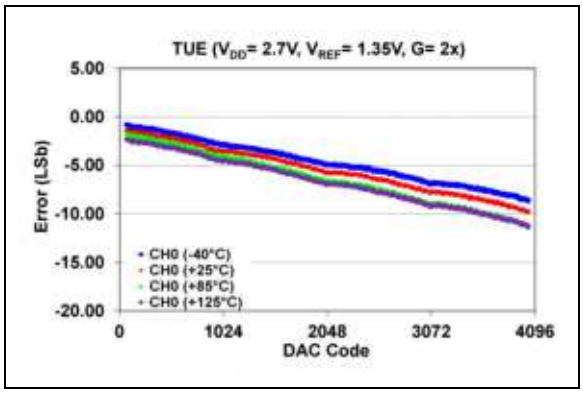



***FIGURE 2-29:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{REF}$ = 0.5 x $V_{DD}$ = 1.35V, Gain = 2x.*

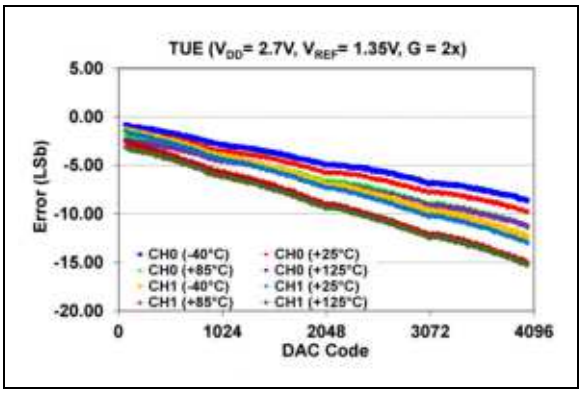



***FIGURE 2-31:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{REF}$ = 0.5 x $V_{DD}$ = 1.35V, Gain = 2x.*


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### 2.2.5 INTEGRAL NONLINEARITY (INL) – MCP47CXB2X (12-BIT), EXTERNAL $V_{REF}$ = 0.5 $V_{DD}$ (VRXB:VRXA = 10), UNBUFFERED, CODE 64-4032

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5.5V.

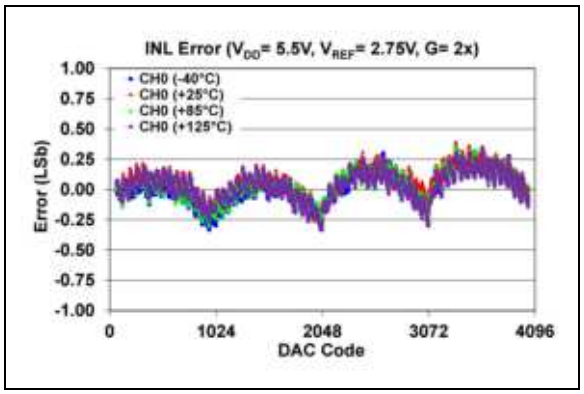



***FIGURE 2-32:*** *INL Error vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{REF}$ = 0.5 x $V_{DD}$ = 2.75V, Gain = 2x.*

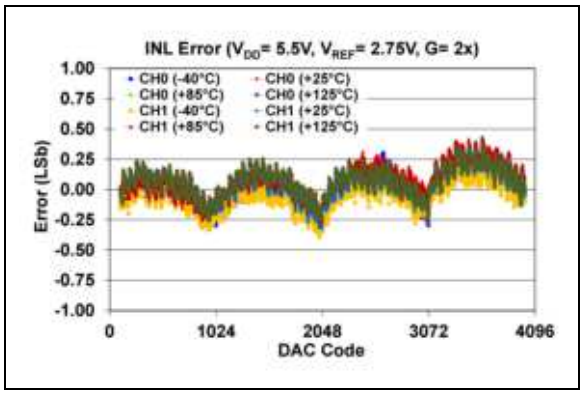



***FIGURE 2-34:*** *INL Error vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{REF}$ = 0.5 x $V_{DD}$ = 2.75V, Gain = 2x.*

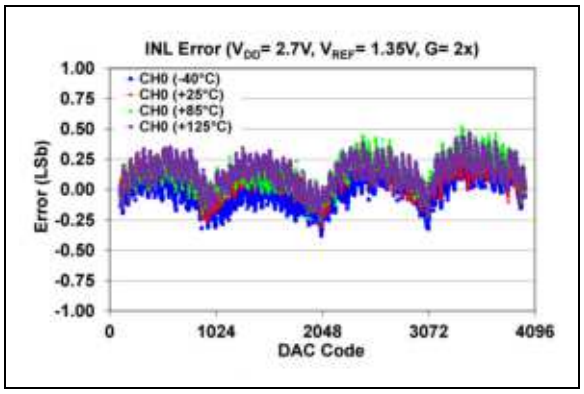



***FIGURE 2-33:*** *INL Error vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{REF}$ = 0.5 x $V_{DD}$ = 1.35V, Gain = 2x.*

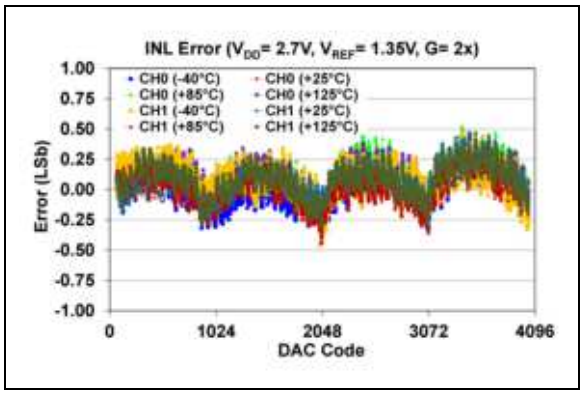



***FIGURE 2-35:*** *INL Error vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{REF}$ = 0.5 x $V_{DD}$ = 1.35V, Gain = 2x.*

### 2.2.6 DIFFERENTIAL NONLINEARITY ERROR (DNL) – MCP47CXB2X (12-BIT), EXTERNAL $V_{REF}$ = 0.5 $V_{DD}$ (VRXB:VRXA = 10), UNBUFFERED, CODE 64-4032

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5.5V.

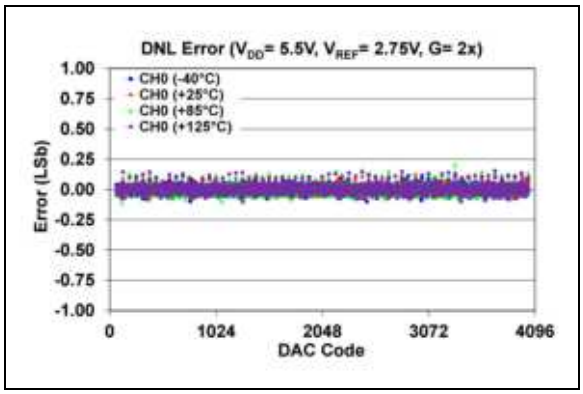



***FIGURE 2-36:*** *DNL Error vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 5.5V, $V_{REF}$ = 0.5 x $V_{DD}$ = 2.75V.*

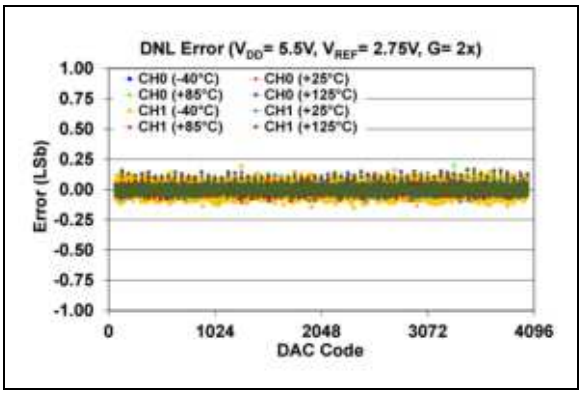



***FIGURE 2-38:*** *DNL Error vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 5.5V, $V_{REF}$ = 0.5 x $V_{DD}$ = 2.75V.*

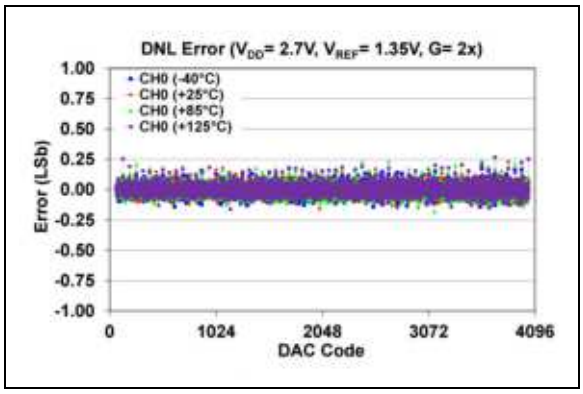



***FIGURE 2-37:*** *DNL Error vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 5.5V, $V_{REF}$ = 0.5 x $V_{DD}$ = 1.35V.*

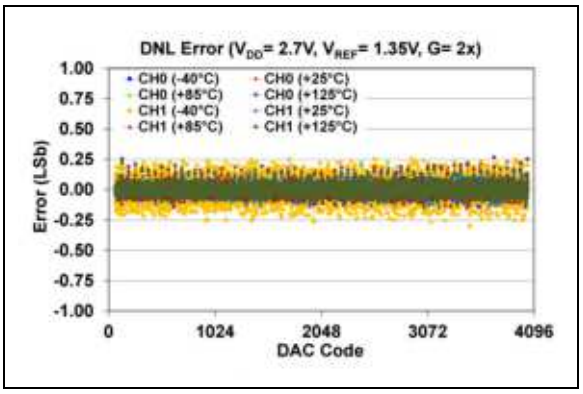



***FIGURE 2-39:*** *DNL Error vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 5.5V, $V_{REF}$ = 0.5 x $V_{DD}$ = 1.35V.*


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### 2.2.7 TOTAL UNADJUSTED ERROR (TUE) – MCP47CXB2X (12-BIT), $V_{REF}$ = INTERNAL BAND GAP (VRXB:VRXA = 01), CODE 64-4032

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5.5V.

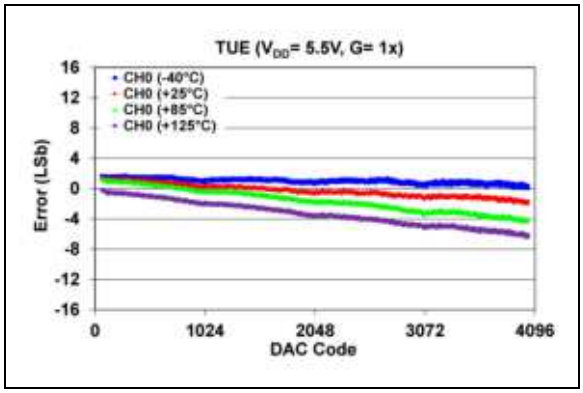



***FIGURE 2-40:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 5.5V, Gain = 1x.*

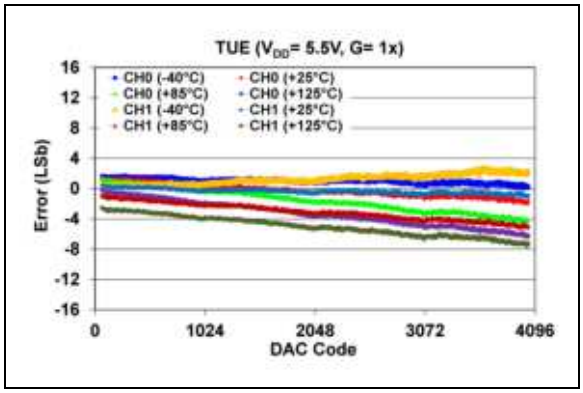



***FIGURE 2-43:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 5.5V, Gain = 1x.*

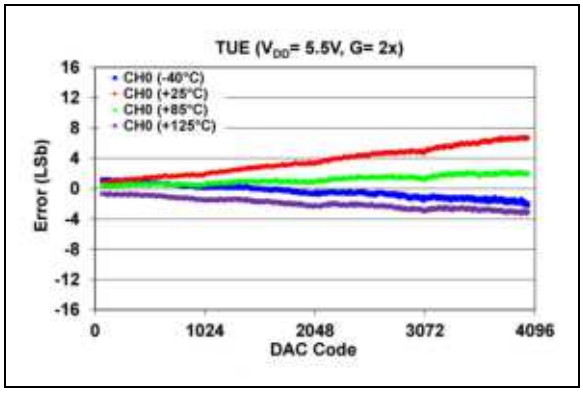



***FIGURE 2-41:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 5.5V, Gain = 2x.*

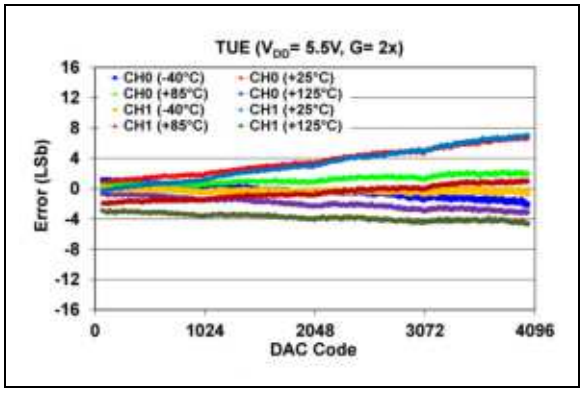



***FIGURE 2-44:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 5.5V, Gain = 2x.*

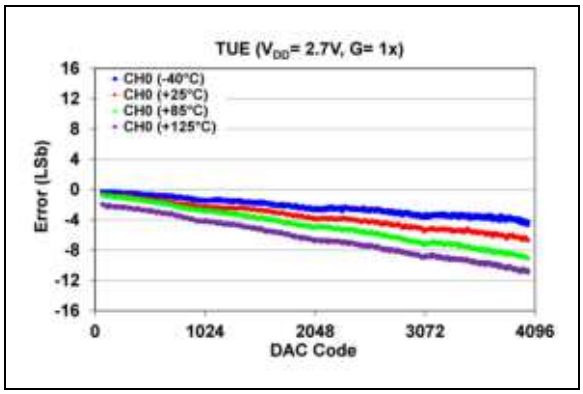



***FIGURE 2-42:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 2.7V, Gain = 1x.*

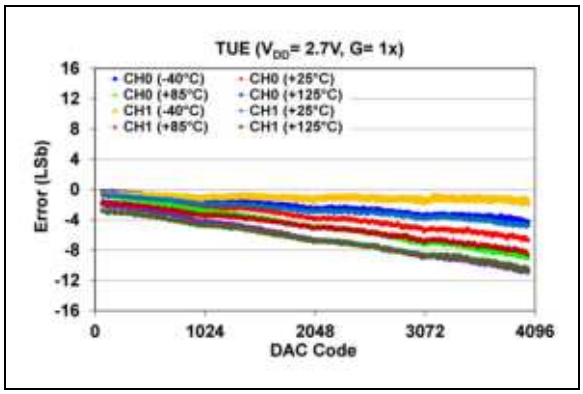



***FIGURE 2-45:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 2.7V, Gain = 1x.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5.5V.

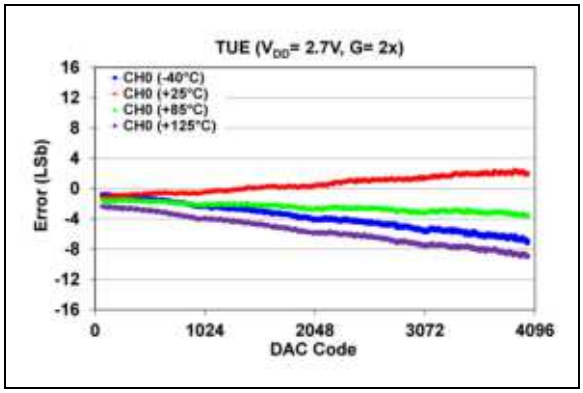



***FIGURE 2-46:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 2.7V, Gain = 2x.*

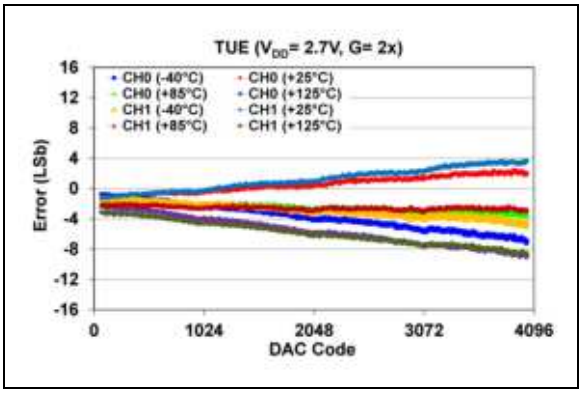



***FIGURE 2-49:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 2.7V, Gain = 2x.*

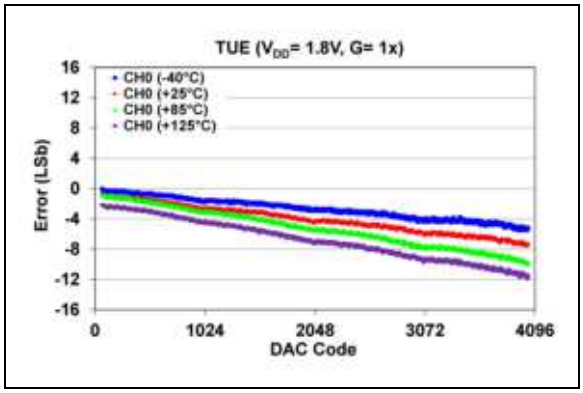



***FIGURE 2-47:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 1.8V, Gain = 1x.*

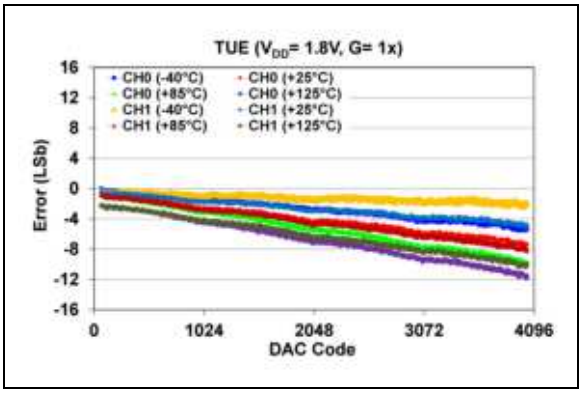



***FIGURE 2-50:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 1.8V, Gain = 1x.*

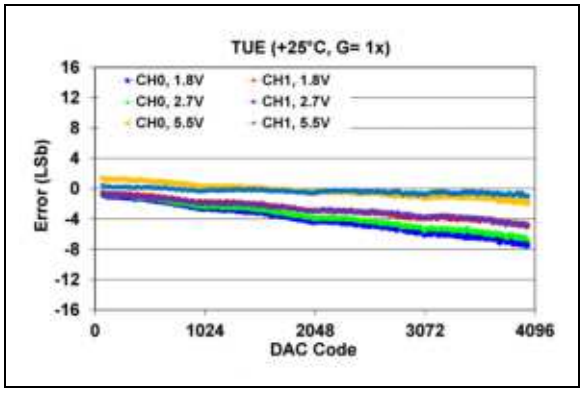



***FIGURE 2-48:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code, 25°C, Gain = 1x.*

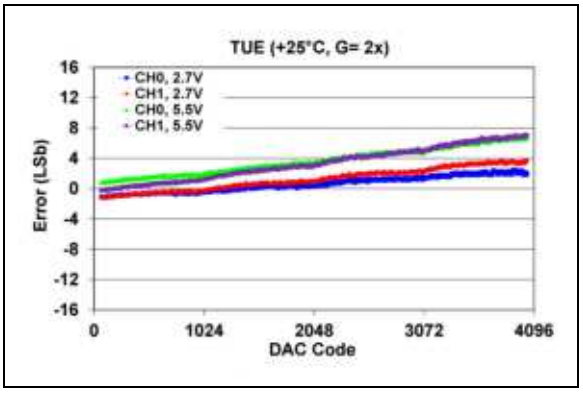



***FIGURE 2-51:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code, 25°C, Gain = 2x.*


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**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5.5V.

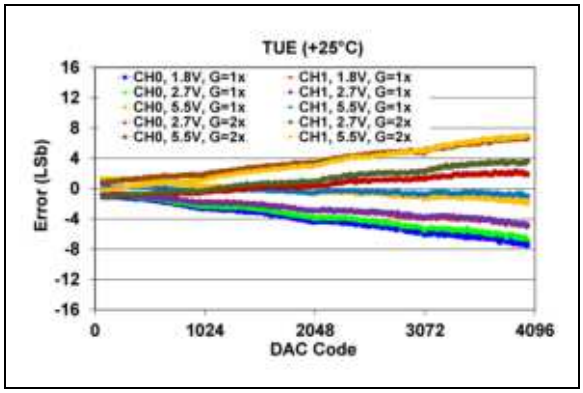



***FIGURE 2-52:*** *Total Unadjusted Error ($V_{OUT}$) vs. DAC Code, +25°C, Gain = 1x and 2x.*

### 2.2.8 INTEGRAL NONLINEARITY ERROR (INL) – MCP47CXB2X (12-BIT), $V_{REF}$ = INTERNAL BAND GAP (VRXB:VRXA = 01), CODE 64-4032

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5.5V.

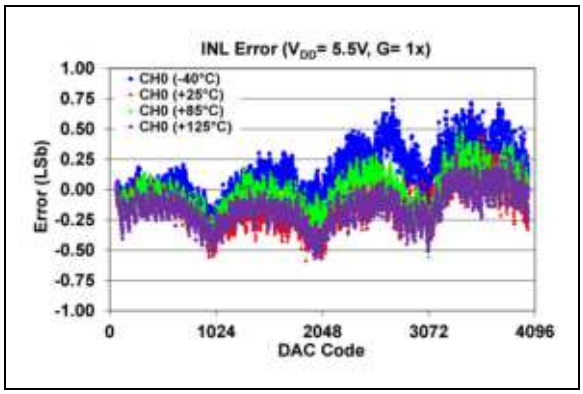



***FIGURE 2-53:*** *INL Error vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 5.5V, Gain = 1x.*

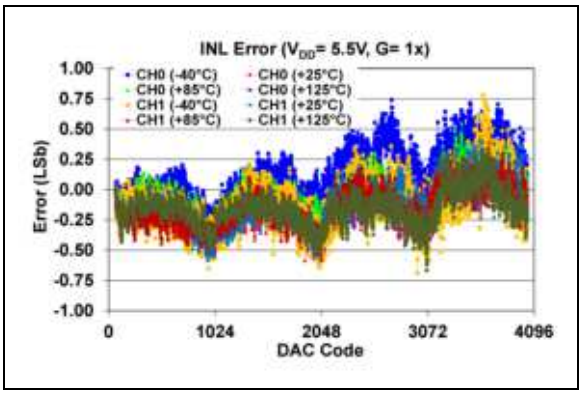



***FIGURE 2-56:*** *INL Error vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 5.5V, Gain = 1x.*

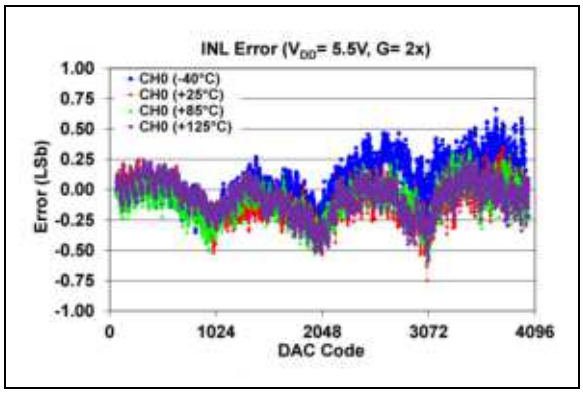



***FIGURE 2-54:*** *INL Error vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 5.5V, Gain = 2x.*

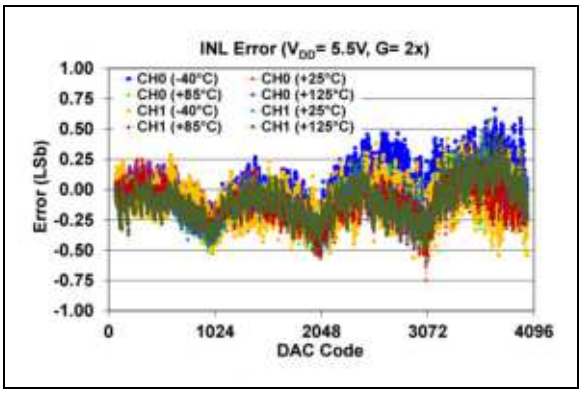



***FIGURE 2-57:*** *INL Error vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 5.5V, Gain = 2x.*

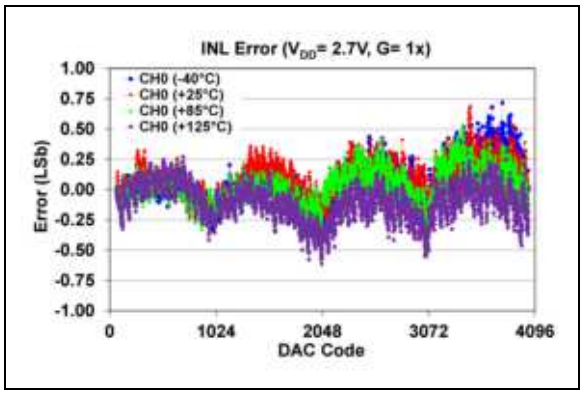



***FIGURE 2-55:*** *INL Error vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 2.7V, Gain = 1x.*

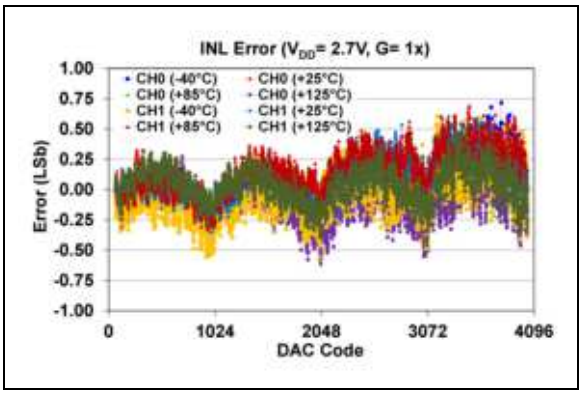



***FIGURE 2-58:*** *INL Error vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 2.7V, Gain = 1x.*


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**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5.5V.

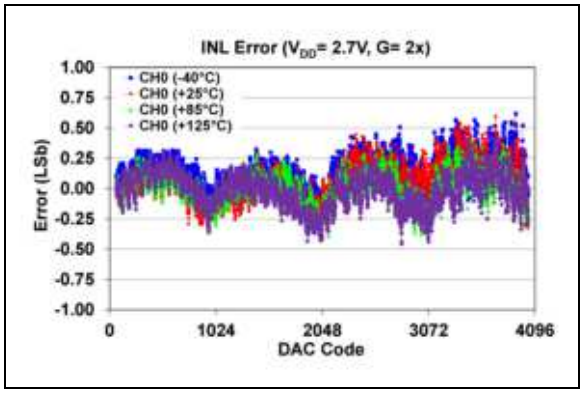



***FIGURE 2-59:*** *INL Error vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 2.7V, Gain = 2x.*

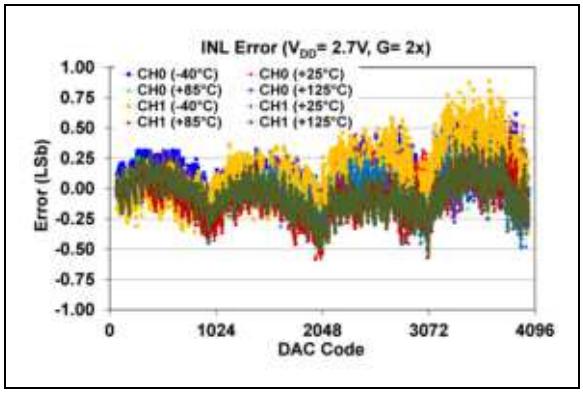



***FIGURE 2-62:*** *INL Error vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 2.7V, Gain = 2x.*

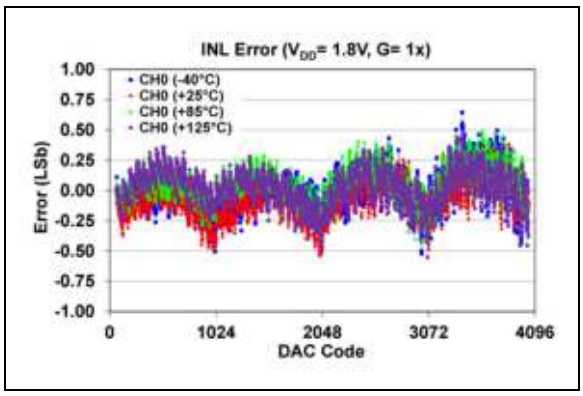



***FIGURE 2-60:*** *INL Error vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 1.8V, Gain = 1x.*

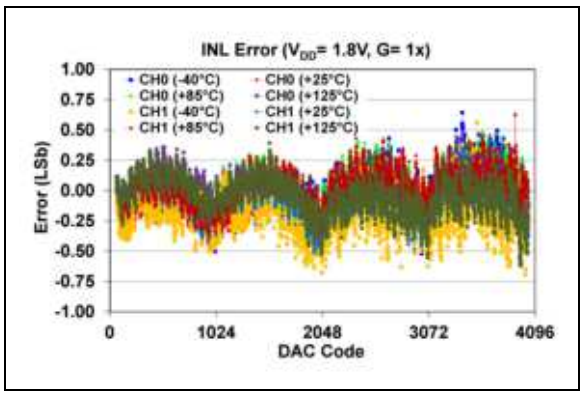



***FIGURE 2-63:*** *INL Error vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 1.8V, Gain = 1x.*

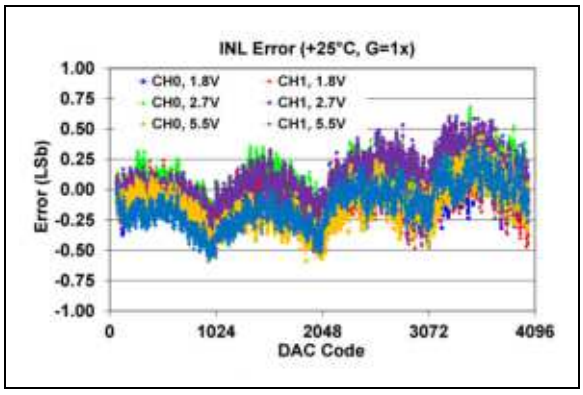



***FIGURE 2-61:*** *INL Error vs. DAC Code, +25°C, Gain = 1x.*

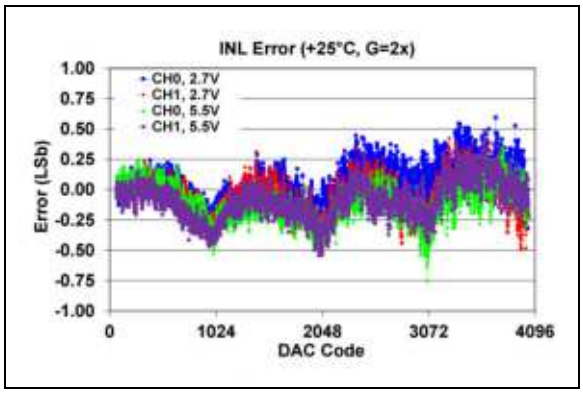



***FIGURE 2-64:*** *INL Error vs. DAC Code, +25°C, Gain = 2x.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5.5V.

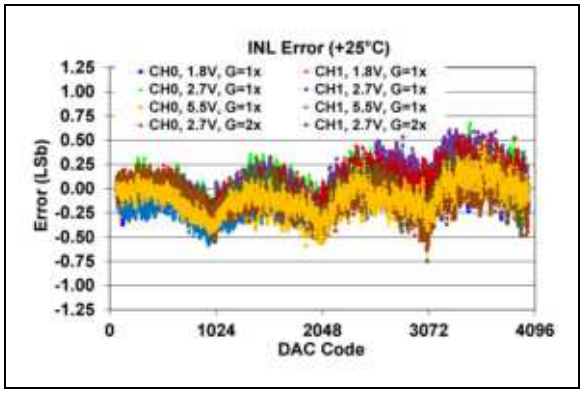



***FIGURE 2-65:*** *INL Error vs. DAC Code, +25°C, Gain = 1x and 2x.*


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### 2.2.9 DIFFERENTIAL NONLINEARITY ERROR (DNL) – MCP47CXB2X (12-BIT), $V_{REF}$ = INTERNAL BAND GAP (VRXB:VRXA = 01), CODE 64-4032

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5.5V.

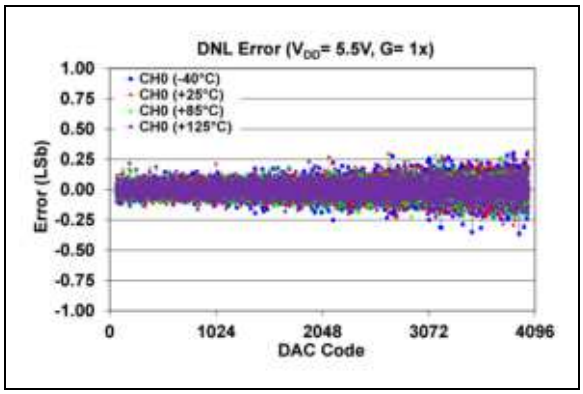



***FIGURE 2-66:*** *DNL Error vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 5.5V, Gain = 1x.*

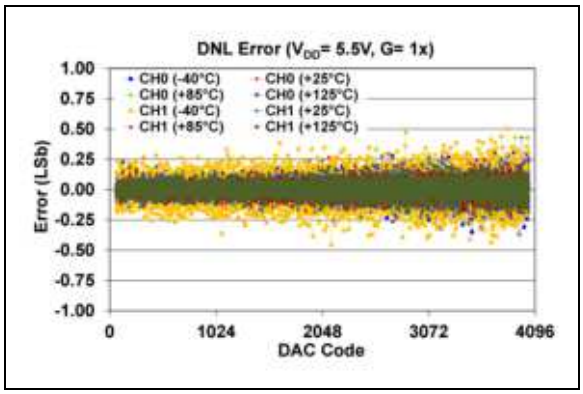



***FIGURE 2-69:*** *DNL Error vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 5.5V, Gain = 1x.*

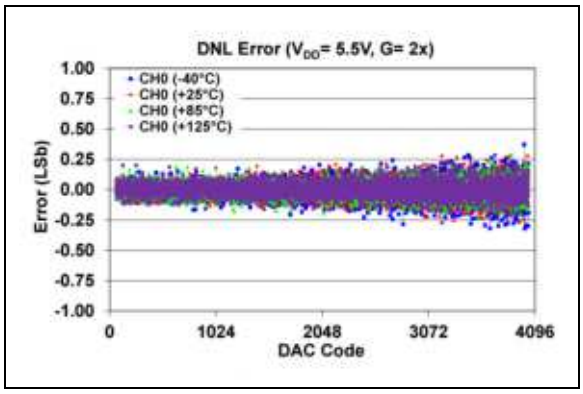



***FIGURE 2-67:*** *DNL Error vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 5.5V, Gain = 2x.*

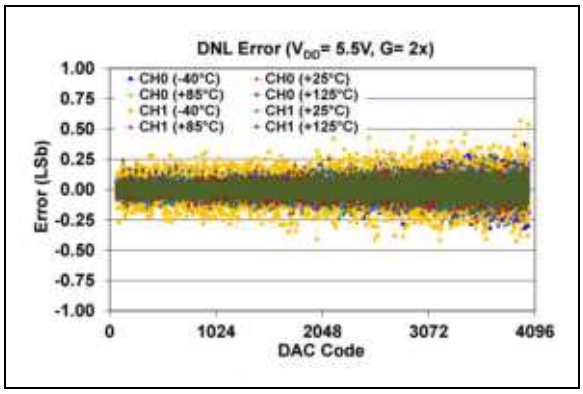



***FIGURE 2-70:*** *DNL Error vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 5.5V, Gain = 2x.*

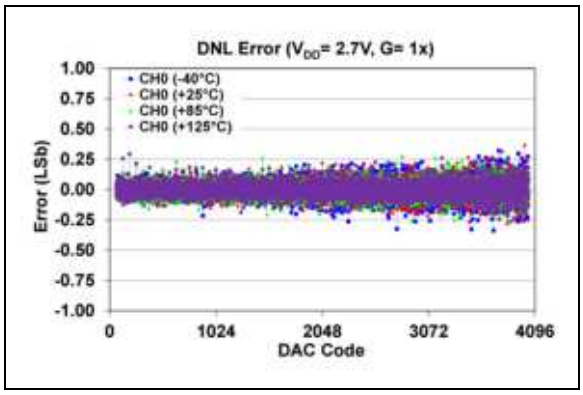



***FIGURE 2-68:*** *DNL Error vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 2.7V, Gain = 1x.*

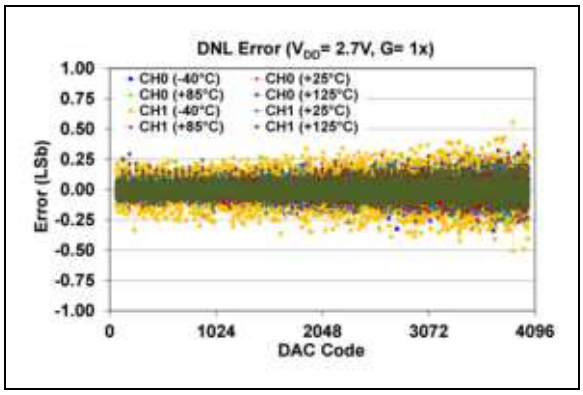



***FIGURE 2-71:*** *DNL Error vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 2.7V, Gain = 1x.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5.5V.

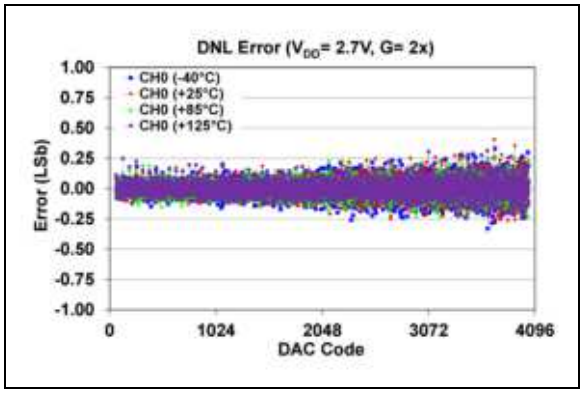



***FIGURE 2-72:*** *DNL Error vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 2.7V, Gain = 2x.*

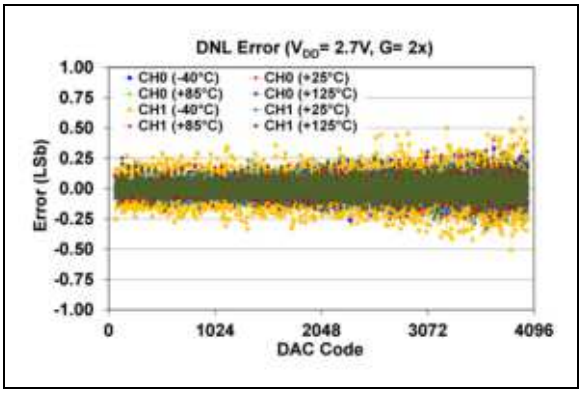



***FIGURE 2-75:*** *DNL Error vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 2.7V, Gain = 2x.*

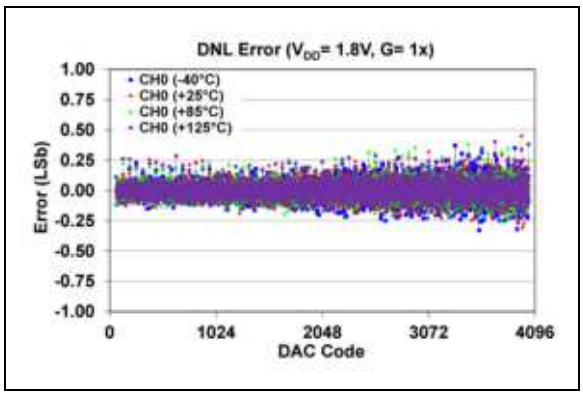



***FIGURE 2-73:*** *DNL Error vs. DAC Code and Temperature (Single Channel – MCP47CXB21), $V_{DD}$ = 1.8V, Gain = 1x.*

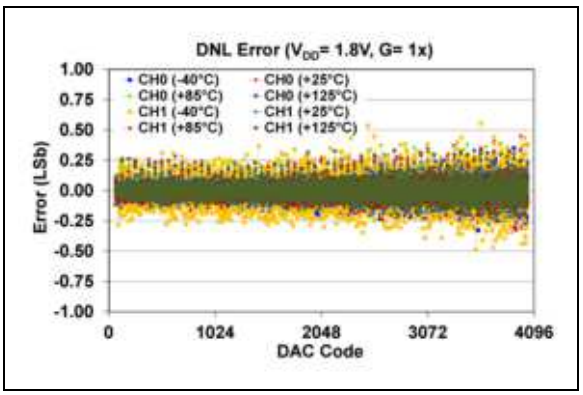



***FIGURE 2-76:*** *DNL Error vs. DAC Code and Temperature (Dual Channel – MCP47CXB22), $V_{DD}$ = 1.8V, Gain = 1x.*

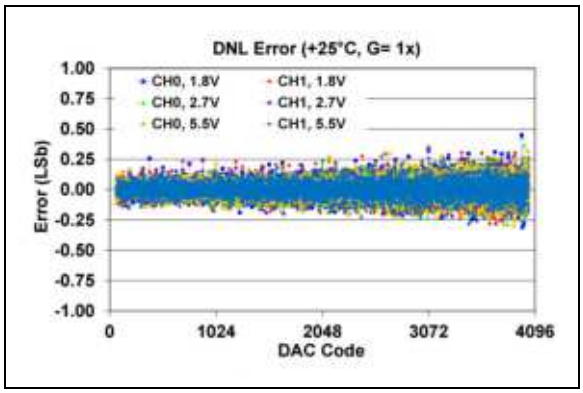



***FIGURE 2-74:*** *DNL Error vs. DAC Code, +25°C, Gain = 1x.*

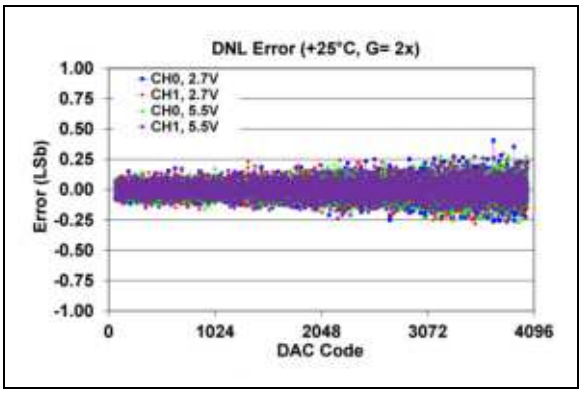



***FIGURE 2-77:*** *DNL Error vs. DAC Code, +25°C, Gain = 2x.*


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**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5.5V.

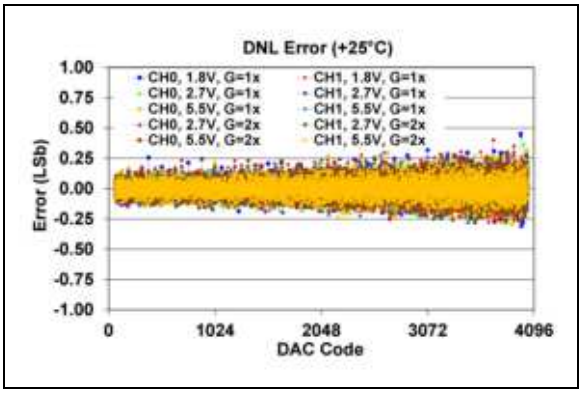



***FIGURE 2-78:*** *DNL Error vs. DAC Code, +25°C, Gain = 1x and 2x.*

**NOTES:**


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## 3.0 PIN DESCRIPTIONS

Overviews of the pin functions are provided in **Section 3.1 "Positive Power Supply Input ($V_{DD}$)"** through **Section 3.9 "No Connect (NC)"**.

The descriptions of the pins for the single DAC output device are listed in Table 3-1 and descriptions for the dual DAC output device are listed in Table 3-2.

**TABLE 3-1: MCP47CXBX1 (SINGLE DAC) PIN FUNCTION TABLE**

| Pin | | | Symbol | I/O | Buffer Type | Description |
|---|---|---|---|---|---|---|
| MSOP 10L | DFN 10L | QFN 16L | | | | |
| 1 | 1 | 16 | $V_{DD}$ | — | P | Supply Voltage Pin |
| 2 | 2 | 1 | A0 | I | ST | $I^2C$ Slave Address Bit 0 Pin |
| 3 | 3 | 2 | $V_{REF}$ | A | Analog | Voltage Reference Input/Output Pin |
| 4 | 4 | 3 | $V_{OUT}$ | A | Analog | Buffered Analog Voltage Output Pin |
| 5 | 5 | 4,5,6,7, 8,14,15 | NC | — | — | Not Internally Connected |
| 6 | 6 | 9 | $\overline{LAT}$/HVC | I | ST | DAC Wiper Register Latch/High-Voltage Command Pin.<br>The Latch pin allows the value in the Volatile DAC registers (Wiper and Configuration bits) to be transferred to the DAC output ($V_{OUT}$).<br>High-voltage commands allow the user MTP Configuration bits to be written. |
| 7 | 7 | 10 | $V_{SS}$ | — | P | Ground Reference Pin for all circuitries on the device |
| 8 | 8 | 11 | A1 | I | ST | $I^2C$ Slave Address Bit 1 Pin |
| 9 | 9 | 12 | SCL | I | ST | $I^2C$ Serial Clock Pin |
| 10 | 10 | 13 | SDA | I/O | ST | $I^2C$ Serial Data Pin |
| — | — | 17 | EP | — | P | Exposed Thermal Pad Pin, must be connected to $V_{SS}$ |

**Note 1:** A = Analog, I = Input, ST = Schmitt Trigger, O = Output, I/O = Input/Output, P = Power

**TABLE 3-2: MCP47CXBX2 (DUAL DAC) PIN FUNCTION TABLE**

| Pin | | | Symbol | I/O | Buffer Type | Description |
|---|---|---|---|---|---|---|
| MSOP 10L | DFN 10L | QFN 16L | | | | |
| 1 | 1 | 16 | $V_{DD}$ | — | P | Supply Voltage Pin |
| 2 | 2 | 1 | A0 | I | ST | $I^2C$ Slave Address Bit 0 Pin |
| 3 | 3 | — | $V_{REF}$ | A | Analog | Voltage Reference Input/Output Pin |
| — | — | 2 | $V_{REF0}$ | A | Analog | Voltage Reference Input/Output Pin for DAC0 |
| — | — | 4 | $V_{REF1}$ | A | Analog | Voltage Reference Input/Output Pin for DAC1 |
| 4 | 4 | 3 | $V_{OUT0}$ | A | Analog | Buffered Analog Voltage Output 0 Pin |
| 5 | 5 | 5 | $V_{OUT1}$ | A | Analog | Buffered Analog Voltage Output 1 Pin |
| — | — | 6,7,14, 15 | NC | — | — | Not Internally Connected |
| 6 | 6 | — | $\overline{LAT}$/HVC | I | ST | DAC Wiper Register Latch/High-Voltage Command Pin.<br>The Latch pin allows the value in the Volatile DAC registers (Wiper and Configuration bits) to be transferred to the DAC output ($V_{OUT}$).<br>High-voltage commands allow the user MTP Configuration bits to be written. |
| — | — | 9 | $\overline{LAT0}$/HVC | I | ST | DAC0 Wiper Register Latch/High-Voltage Command Pin.<br>The Latch pin allows the value in the Volatile DAC0 registers (Wiper and Configuration bits) to be transferred to the DAC0 output ($V_{OUT0}$).<br>High-voltage commands allow the user MTP Configuration bits to be written. |
| — | — | 8 | $\overline{LAT1}$ | I | ST | DAC1 Wiper Register Latch Pin.<br>The Latch pin allows the value in the Volatile DAC1 registers (Wiper and Configuration bits) to be transferred to the DAC1 output ($V_{OUT1}$). |
| 7 | 7 | 10 | $V_{SS}$ | — | P | Ground Reference Pin for all circuitries on the device |
| 8 | 8 | 11 | A1 | I | ST | $I^2C$ Slave Address Bit 1 Pin |
| 9 | 9 | 12 | SCL | I | ST | $I^2C$ Serial Clock Pin |
| 10 | 10 | 13 | SDA | I/O | ST | $I^2C$ Serial Data Pin |

**Note 1:** A = Analog, I = Input, ST = Schmitt Trigger, O = Output, I/O = Input/Output, P = Power


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## 3.1 Positive Power Supply Input ($V_{DD}$)

$V_{DD}$ is the positive supply voltage input pin. The input supply voltage is relative to $V_{SS}$.

The power supply at the $V_{DD}$ pin should be as clean as possible for good DAC performance. It is recommended to use an appropriate bypass capacitor of about 0.1 µF (ceramic) to ground as close as possible to the pin. An additional 10 µF capacitor (tantalum) in parallel is also recommended to further attenuate noise present in application boards.

## 3.2 Ground ($V_{SS}$)

The $V_{SS}$ pin is the device ground reference.

The user must connect the $V_{SS}$ pin to a ground plane through a low-impedance connection. If an analog ground path is available in the application PCB (Printed Circuit Board), it is highly recommended that the $V_{SS}$ pin be tied to the analog ground path or isolated within an analog ground plane of the circuit board.

## 3.3 Voltage Reference Pin ($V_{REF}$)

The $V_{REF}$ pin is either an input or an output. When the DAC's voltage reference is configured as the $V_{REF}$ pin, the pin is an input. When the DAC's voltage reference is configured as the internal band gap, the pin is an output.

When the DAC's voltage reference is configured as the $V_{REF}$ pin, there are two options for this voltage input: $V_{REF}$ pin voltage is buffered or unbuffered. The buffered option is offered in cases where the external reference voltage does not have sufficient current capability to not drop its voltage when connected to the internal resistor ladder circuit.

When the DAC's voltage reference is configured as the device $V_{DD}$, the $V_{REF}$ pin is disconnected from the internal circuit.

When the DAC's voltage reference is configured as the internal band gap, the $V_{REF}$ pin's drive capability is minimal, so the output signal should be buffered.

See **Section 5.2 "Voltage Reference Selection"** and Register 4-2 for more details on the Configuration bits.

## 3.4 Analog Output Voltage Pins ($V_{OUT0}$, $V_{OUT1}$)

$V_{OUT0}$ and $V_{OUT1}$ are the DAC analog voltage output pins. Each DAC output has an output amplifier. The DAC output range is dependent on the selection of the voltage reference source (and potential output gain selection). These are:

- Device $V_{DD}$ – The Full-Scale Range (FSR) of the DAC output is from $V_{SS}$ to approximately $V_{DD}$.
- $V_{REF}$ pin – The Full-Scale Range of the DAC output is from $V_{SS}$ to G x $V_{RL}$, where G is the gain selection option (1x or 2x).
- Internal Band Gap – The Full-Scale Range of the DAC output is from $V_{SS}$ to G x $V_{BG}$, where G is the gain selection option (1x or 2x).

In Normal mode, the DC impedance of the output pin is about 1Ω. In Power-Down mode, the output pin is internally connected to a known pull-down resistor of 1 kΩ, 100 kΩ or open. The power-down selection bits settings are shown in Register 4-3 (Table 5-5).

## 3.5 Latch/High-Voltage Command Pin (LAT/HVC)

The DAC output value update event can be controlled and synchronized using the $\overline{LAT}$ pin, for one or both channels, on single or different devices.

The $\overline{LAT}$ pin controls the effect of the Volatile Wiper registers, VRxB:VRxA and PDxB:PDxA, and the Gx bits on the DAC output. If the $\overline{LAT}$ pin is held at $V_{IH}$, the values sent to the Volatile Wiper registers and Configuration bits have no effect on the DAC outputs. After the Volatile Wiper registers and Configuration bits have been loaded with the desired data, once the voltage on the pin transitions to $V_{IL}$, the values in the Volatile Wiper registers and Configuration bits are transferred to the DAC outputs. Pulsing $\overline{LAT}$ low during writes to the registers could lead to unpredictable DAC output voltage values until the next pulse is issued and should be avoided. The pin is level-sensitive, so writing to the Volatile Wiper registers and Configuration bits while it is being held at $V_{IL}$, will trigger an immediate change in the outputs.

For dual output devices in MSOP and DFN packages, the $\overline{LAT}$ pin controls both channels at the same time. The HVC pin allows the device's MTP memory to be programmed for the MCP47CMBXX devices. The programming voltage supply should provide 7.5V and at least 6.4 mA.

| | |
|---|---|
| **Note:** | The HVC pin should have voltages greater than 5.5V present only during the MTP programming operation. Using voltages greater than 5.5V for an extended time on the pin may cause device reliability issues. |

### 3.6 I²C – Serial Clock Pin (SCL)

The SCL pin is the serial clock pin of the I²C interface. The MCP47CXBXX I²C interface only acts as a Slave and the SCL pin accepts only external serial clocks. The input data from the Master device are shifted into the SDA pin on the rising edges of the SCL clock and output from the device occurs at the falling edges of the SCL clock. The SCL pin is an open-drain N-channel driver. Therefore, it needs an external pull-up resistor from the $V_{DD}$ line to the SCL pin. Refer to **Section 6.0 "I²C Serial Interface Module"** for more details on the I²C serial interface communication.

### 3.7 I²C – Serial Data Pin (SDA)

The SDA pin is the serial data pin of the I²C interface. The SDA pin is used to write or read the DAC registers and Configuration bits. The SDA pin is an open-drain N-channel driver. Therefore, it needs an external pull-up resistor from the $V_{DD}$ line to the SDA pin. Except for Start and Stop conditions, the data on the SDA pin must be stable during the high period of the clock. The high or low state of the SDA pin can only change when the clock signal on the SCL pin is low. See **Section 6.0 "I²C Serial Interface Module"**.

### 3.8 I²C Slave Address Pins (A0,A1)

The state of these pins will determine the device's I²C Slave Address bit 0 value (overriding the ADD0 bit and the ADD1 bit in Register 4-5).

### 3.9 No Connect (NC)

The NC pin is not internally connected to the device.


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## 4.0 GENERAL DESCRIPTION

The MCP47CXBX1 (MCP47CXB01, MCP47CXB11 and MCP47CXB21) devices are single-channel voltage output devices.

MCP47CXBX2 (MCP47CXB02, MCP47CXB12 and MCP47CXB22) are dual channel voltage output devices.

These devices are offered with 8-bit (MCP47CXB0X), 10-bit (MCP47CXB1X) and 12-bit (MCP47CXB2X) resolutions.

The family offers two memory options: the MCP47CVBXX devices have volatile memory, while the MCP47CMBXX have 32-times programmable nonvolatile memory (MTP).

All devices include an $I^2C$ serial interface and a write latch ($\overline{LAT}$) pin to control the update of the analog output voltage value from the value written in the Volatile DAC Output register.

The devices use a resistor ladder architecture. The resistor ladder DAC is driven from a software-selectable voltage reference source. The source can be either the device's internal $V_{DD}$, an external $V_{REF}$ pin voltage (buffered or unbuffered) or an internal band gap voltage source.

The DAC output is buffered with a low-power and precision output amplifier. This output amplifier provides a rail-to-rail output with low offset voltage and low noise. The gain (1x or 2x) of the output buffer is software configurable.

The devices operate from a single supply voltage. This voltage is specified from 2.7V to 5.5V for full specified operation, and from 1.8V to 5.5V for digital operation. The device operates between 1.8V and 2.7V, but some device parameters are not specified.

The MCP47CMBXX devices also have user-programmable nonvolatile configuration memory (MTP). This allows the device's desired POR values to be saved or the $I^2C$ address to be changed. The device also has general purpose MTP memory locations for storing system-specific information (calibration data, serial numbers, system ID information). A high-voltage requirement for programming on the HVC pin ensures that these device settings are not accidentally modified during normal system operation. Therefore, it is recommended that the MTP memory should only be programmed at the user's factory.

The main functional blocks are:

- Power-on Reset/Brown-out Reset (POR/BOR)
- Device Memory
- Resistor Ladder
- Output Buffer/$V_{OUT}$ Operation
- $I^2C$ Serial Interface Module

### 4.1 Power-on Reset/Brown-out Reset (POR/BOR)

The internal Power-on Reset (POR)/Brown-out Reset (BOR) circuit monitors the power supply voltage ($V_{DD}$) during operation. This circuit ensures correct device start-up at system power-up and power-down events.

The device's RAM Retention Voltage ($V_{RAM}$) is lower than the POR/BOR Voltage Trip Point ($V_{POR}/V_{BOR}$). The maximum $V_{POR}/V_{BOR}$ voltage is less than 1.8V.

The POR and BOR trip points are at the same voltage, and the condition is determined by whether the $V_{DD}$ voltage is rising or falling (see Figure 4-1). What occurs is different depending on whether the Reset is a POR or BOR Reset.

POR occurs as the voltage rises (typically from 0V), while BOR occurs as the voltage falls (typically from $V_{DD(MIN)}$ or higher).

When $V_{POR}/V_{BOR} < V_{DD} < 2.7V$, the electrical performance may not meet the data sheet specifications. In this region, the device is capable of reading and writing to its volatile memory if the proper serial command is executed.

#### 4.1.1 POWER-ON RESET

The Power-on Reset is the case where the device's $V_{DD}$ has power applied to it from the $V_{SS}$ voltage level. As the device powers up, the $V_{OUT}$ pin floats to an unknown value. When the device's $V_{DD}$ is above the transistor threshold voltage of the device, the output starts to be pulled low.

After the $V_{DD}$ is above the POR/BOR trip point ($V_{BOR}/V_{POR}$), the resistor network's wiper is loaded with the POR value. The POR value is either mid-scale (MCP47CVBXX) or the user's MTP programmed value (MCP47CMBXX).

| | |
|---|---|
| **Note:** | In order to have the MCP47CMBXX devices load the values from nonvolatile memory locations at POR, they have to be programmed at least once by the user; otherwise, the loaded values will be the default ones. After MTP programming, a POR event is required to load the written values from the nonvolatile memory. |

Volatile memory determines the Analog Output ($V_{OUT}$) pin voltage. After the device is powered up, the user can update the device memory.

When the rising $V_{DD}$ voltage crosses the $V_{POR}$ trip point, the following occur:

- The default DAC POR value is latched into the Volatile DAC register.
- The default DAC POR Configuration bit values are latched into the Volatile Configuration bits.
- POR status bit is set ('1').
- The Reset Delay Timer ($t_{PORD}$) starts; when the Reset Delay Timer ($t_{PORD}$) times out, the $I^2C$ serial interface is operational. During this delay time, the $I^2C$ interface will not accept commands.
- The Device Memory Address Pointer is forced to 00h.

The Analog Output ($V_{OUT}$) state is determined by the state of the Volatile Configuration bits and the DAC register. This is called a Power-on Reset (event).

Figure 4-1 illustrates the conditions for power-up and power-down events under typical conditions.

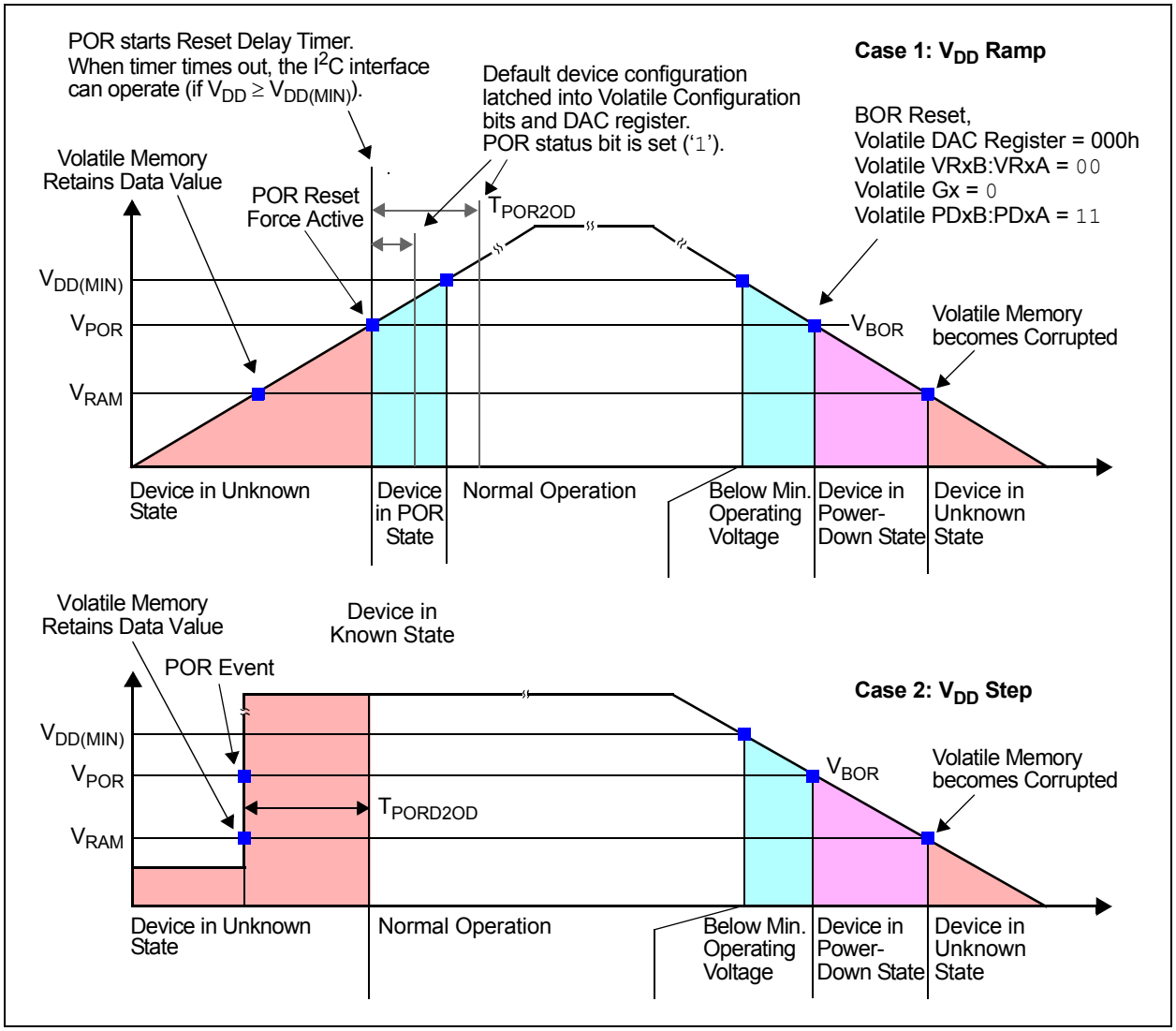



***FIGURE 4-1:*** *Power-on Reset Operation.*


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### 4.1.2 BROWN-OUT RESET

A Brown-out Reset occurs when a device had power applied to it and that power (voltage) drops below the specified range.

When the falling $V_{DD}$ voltage crosses the $V_{POR}$ trip point (BOR event), the following occurs:

- Serial interface is disabled.
- MTP writes are disabled.
- Device is forced into a power-down state (PDxB:PDxA = 11). Analog circuitry is turned off.
- Volatile DAC register is forced to 000h.

Volatile Configuration bits, VRxB:VRxA and Gx, are forced to '0'.

If the $V_{DD}$ voltage decreases below the $V_{RAM}$ voltage, all volatile memory may become corrupted.

As the voltage recovers above the $V_{POR}/V_{BOR}$ voltage, see **Section 4.1.1 "Power-on Reset"** for further details.

Serial commands not completed due to a brown-out condition may cause the memory location to become corrupted.

Figure 4-1 illustrates the conditions for power-up and power-down events under typical conditions.

## 4.2 Device Memory

User memory includes the following types:

- Volatile Register Memory (RAM)
- **Nonvolatile Register Memory (MTP)**

MTP memory is present just for the MCP47CMBXX devices and has three groupings:

- NV DAC Output Values (loaded on POR event)
- Device Configuration Memory
- General Purpose NV Memory

Each memory location is up to 16 bits wide. The memory-mapped register space is shown in Table 4-1.

The $I^2C$ interface depends on how this memory is read and written. Refer to **Section 6.0 "$I^2C$ Serial Interface Module"** and **Section 7.0 "Device Commands"** for more details on reading and writing the device's memory.

### 4.2.1 VOLATILE REGISTER MEMORY (RAM)

The MCP47CXBXX devices have volatile memory to directly control the operation of the DACs. There are up to five volatile memory locations:

- DAC0 and DAC1 Output Value registers
- VREF Select register
- Power-Down Configuration register
- Gain and Status register

The volatile memory starts functioning when the device $V_{DD}$ is at (or above) the RAM retention voltage ($V_{RAM}$). The volatile memory will be loaded with the default device values when the $V_{DD}$ rises across the $V_{POR}/V_{BOR}$ voltage trip point.

After the device is powered-up, the user can update the device memory. Table 4-2 shows the volatile memory locations and their interaction due to a POR event.

**TABLE 4-1: MCP47CXBXX MEMORY MAP (16-BIT)**

| Address | Function | Single | Dual |
|---|---|---|---|
| 00h | Volatile DAC Wiper Register 0 | Y | Y |
| 01h | Volatile DAC Wiper Register 1 | — | Y |
| 02h | Reserved | — | — |
| 03h | Reserved | — | — |
| 04h | Reserved | — | — |
| 05h | Reserved | — | — |
| 06h | Reserved | — | — |
| 07h | Reserved | — | — |
| 08h | Volatile VREF Register | Y | Y |
| 09h | Volatile Power-Down Register | Y | Y |
| 0Ah | Volatile Gain and Status Register | Y | Y |
| 0Bh | Reserved | — | — |
| 0Ch | General Purpose MTP | (1) | |
| 0Dh | General Purpose MTP | (1) | |
| 0Eh | General Purpose MTP | (1) | |
| 0Fh | General Purpose MTP | (1) | |

| Address | Function | Single(1) | Dual(1) |
|---|---|---|---|
| 10h | Nonvolatile DAC Wiper Register 0 | Y | Y |
| 11h | Nonvolatile DAC Wiper Register 1 | — | Y |
| 12h | Reserved | — | — |
| 13h | Reserved | — | — |
| 14h | Reserved | — | — |
| 15h | Reserved | — | — |
| 16h | Reserved | — | — |
| 17h | Reserved | — | — |
| 18h | Nonvolatile VREF Register | Y | Y |
| 19h | Nonvolatile Power-Down Register | Y | Y |
| 1Ah | NV Gain and $I^2C$ 7-Bit Slave Address | Y | Y |
| 1Bh | NV WiperLock™ Technology Register | Y | Y |
| 1Ch | General Purpose MTP | (1) | |
| 1Dh | General Purpose MTP | (1) | |
| 1Eh | General Purpose MTP | (1) | |
| 1Fh | General Purpose MTP | (1) | |

**Legend:**

| | |
|---|---|
| | Volatile Memory Addresses |
| | MTP Memory Addresses |
| | Memory Locations Not Implemented on this Device Family |

**Note 1:** On nonvolatile memory devices only (MCP47CMBXX).


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### 4.2.2 NONVOLATILE REGISTER MEMORY (MTP)

This memory option is available only for the MCP47CMBXX devices.

MTP memory starts functioning below the device's $V_{POR}/V_{BOR}$ trip point, and once the $V_{POR}$ event occurs, the Volatile Memory registers are loaded with the corresponding MTP register memory values.

Memory addresses, 0Ch through 1Fh, are nonvolatile memory locations. These registers contain the DAC POR/BOR wiper values, the DAC POR/BOR Configuration bits, the $I^2C$ Slave address and eight general purpose memory addresses for storing user-defined data as calibration constants or identification numbers. The Nonvolatile DAC Wiper registers and Configuration bits contain the user's DAC Output and configuration values for the POR event.

The Nonvolatile DAC Wiper registers contain the user's DAC output and configuration values for the POR event. These nonvolatile values will overwrite the factory default values. If these MTP addresses are unprogrammed, the factory default values define the output state.

The Nonvolatile DAC registers enable the stand-alone operation of the device (without microcontroller control) after being programmed to the desired values.

To program nonvolatile memory locations, a high-voltage source on the $\overline{LAT}$/HVC pin is required. Each register/MTP location can be programmed 32 times. After 32 writes, a new write operation will not be possible and the last successful value written will remain associated with the memory location.

The device starts writing the MTP memory cells at the completion of the serial interface command at the rising edge of the last data bit. The high voltage should remain present on the $\overline{LAT}$/HVC pin until the write cycle is complete; otherwise, the write is unsuccessful and the location is compromised (cannot be used again and the number of available writes decreases by one).

To recover from an aborted MTP write operation, the following procedure must be used:

- Write again any valid value to the same address
- Force a POR condition
- Write again the desired value to the MTP location

It is recommended to keep high voltage on only during the MTP write command and programming cycle; otherwise, the reliability of the device could be affected.

### 4.2.3 POR/BOR OPERATION WITH WIPERLOCK TECHNOLOGY ENABLED

Regardless of the WiperLock technology state, a POR event will load the Volatile DACx Wiper register value with the Nonvolatile DACx Wiper register value. Refer to **Section 4.1 "Power-on Reset/Brown-out Reset (POR/BOR)"** for further information.

### 4.2.4 UNIMPLEMENTED LOCATIONS

#### 4.2.4.1 Unimplemented Register Bits

When issuing read commands to a valid memory location with unimplemented bits, the unimplemented bits will be read as '0'.

#### 4.2.4.2 Unimplemented (RESERVED) Locations

There are a number of unimplemented memory locations that are reserved for future use. Normal (voltage) commands (read or write) to any unimplemented memory address will result in a command error condition ($I^2C$ NACK).

High-voltage commands to any unimplemented Configuration bit(s) will also result in a command error condition.

**TABLE 4-2: FACTORY DEFAULT POR/BOR VALUES (MTP MEMORY UNPROGRAMMED)**

| Address | Function | POR/BOR Value | | |
|---|---|---|---|---|
| | | 8-Bit | 10-Bit | 12-Bit |
| 00h | Volatile DAC0 Register | 7Fh | 1FFh | 7FFh |
| 01h | Volatile DAC1 Register | 7Fh | 1FFh | 7FFh |
| 02h | Reserved(3) | — | — | — |
| 03h | Reserved(3) | — | — | — |
| 04h | Reserved(3) | — | — | — |
| 05h | Reserved(3) | — | — | — |
| 06h | Reserved(3) | — | — | — |
| 07h | Reserved(3) | — | — | — |
| 08h | Volatile VREF Register | 0000h | 0000h | 0000h |
| 09h | Volatile Power-Down Register | 0000h | 0000h | 0000h |
| 0Ah | Volatile Gain and Status Register(4) | 0080h | 0080h | 0080h |
| 0Bh | Reserved(3) | 0000h | 0000h | 0000h |
| 0Ch | General Purpose MTP(1) | 0000h | 0000h | 0000h |
| 0Dh | General Purpose MTP(1) | 0000h | 0000h | 0000h |
| 0Eh | General Purpose MTP(1) | 0000h | 0000h | 0000h |
| 0Fh | General Purpose MTP(1) | 0000h | 0000h | 0000h |
| 10h | Nonvolatile DAC0 Wiper Register(1) | 7Fh | 1FFh | 7FFh |
| 11h | Nonvolatile DAC1 Wiper Register(1) | 7Fh | 1FFh | 7FFh |
| 12h | Reserved(3) | — | — | — |
| 13h | Reserved(3) | — | — | — |
| 14h | Reserved(3) | — | — | — |
| 15h | Reserved(3) | — | — | — |
| 16h | Reserved(3) | — | — | — |
| 17h | Reserved(3) | — | — | — |
| 18h | Nonvolatile VREF Register(1) | 0000h | 0000h | 0000h |
| 19h | Nonvolatile Power-Down Register(1) | 0000h | 0000h | 0000h |
| 1Ah | NV Gain and $I^2C$ 7-Bit Slave Address(1,2) | 0060h | 0060h | 0060h |
| 1Bh | NV WiperLock™ Technology Register(1) | 0000h | 0000h | 0000h |
| 1Ch | General Purpose MTP(1) | 0000h | 0000h | 0000h |
| 1Dh | General Purpose MTP(1) | 0000h | 0000h | 0000h |
| 1Eh | General Purpose MTP(1) | 0000h | 0000h | 0000h |
| 1Fh | General Purpose MTP(1) | 0000h | 0000h | 0000h |

**Legend:**

- Volatile Memory Address Range
- Nonvolatile Memory Address Range
- Not Implemented

**Note 1:** On nonvolatile devices only (MCP47CMBXX).

**2:** Default $I^2C$ 7-bit Slave address is '110 0000' ('110 00xx' when A1:A0 bits are determined from the A1 and A0 pins).

**3:** Reading a reserved memory location will result in the $I^2C$ command to Not ACK the command byte. The device data bits will output all '1's. A Start condition will reset the $I^2C$ interface.

**4:** The '1' bit is the POR status bit, which is set after the POR event and cleared after address 0Ah is read.


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### 4.2.5 DEVICE REGISTERS

Register 4-1 shows the format of the DAC Output Value registers for the volatile memory locations. These registers will be either 8 bits, 10 bits or 12 bits wide. The values are right justified.

**REGISTER 4-1: DAC0 (00h/10h) AND DAC1 (01h/11h) OUTPUT VALUE REGISTERS (VOLATILE/NONVOLATILE)**

| | U-0 | U-0 | U-0 | U-0 | R/W-n | R/W-n | R/W-n | R/W-n | R/W-n | R/W-n | R/W-n | R/W-n | R/W-n | R/W-n | R/W-n | R/W-n |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 12-bit | — | — | — | — | D11 | D10 | D09 | D08 | D07 | D06 | D05 | D04 | D03 | D02 | D01 | D00 |
| 10-bit | — | — | — | — | — | — | D09 | D08 | D07 | D06 | D05 | D04 | D03 | D02 | D01 | D00 |
| 8-bit | — | — | — | — | — | — | — | — | D07 | D06 | D05 | D04 | D03 | D02 | D01 | D00 |
| | bit 15 | | | | | | | | | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |
| = 12-bit device | = 10-bit device | = 8-bit device | |

| **12-bit** | **10-bit** | **8-bit** | |
|---|---|---|---|
| bit 15-12 | bit 15-10 | bit 15-8 | **Unimplemented:** Read as '0' |
| bit 11-0 | — | — | **D11:D00:** DAC Output Value bits – 12-bit devices<br>FFFh = Full-scale output value<br>7FFh = Mid-scale output value<br>000h = Zero scale output value |
| — | bit 9-0 | — | **D09:D00:** DAC Output Value bits – 10-bit devices<br>3FFh = Full-scale output value<br>1FFh = Mid-scale output value<br>000h = Zero scale output value |
| — | — | bit 7-0 | **D07:D00:** DAC Output Value bits – 8-bit devices<br>FFh = Full-scale output value<br>7Fh = Mid-scale output value<br>00h = Zero scale output value |

Register 4-2 shows the format of the Voltage Reference Control register. Each DAC has two bits to control the source of the voltage reference of the DAC. This register is for the volatile memory locations. The width of this register is two times the number of DACs for the device.

**REGISTER 4-2: VOLTAGE REFERENCE (VREF) CONTROL REGISTERS (08h/18h) (VOLATILE/NONVOLATILE)**

| | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-n | R/W-n | R/W-n | R/W-n |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Single | — | — | — | — | — | — | — | — | — | — | — | — | —(1) | —(1) | VR0B | VR0A |
| Dual | — | — | — | — | — | — | — | — | — | — | — | — | VR1B | VR1A | VR0B | VR0A |
| | bit 15 | | | | | | | | | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |
| = Single channel device | = Dual channel device | | |

| Single | Dual | |
|---|---|---|
| bit 15-2 | bit 15-4 | **Unimplemented:** Read as '0' |
| bit 1-0 | bit 3-0 | **VRxB:VRxA:** DAC Voltage Reference Control bits<br>11 = $V_{REF}$ pin (buffered); $V_{REF}$ buffer enabled<br>10 = $V_{REF}$ pin (unbuffered); $V_{REF}$ buffer disabled<br>01 = Internal band gap (1.214V typical); $V_{REF}$ buffer enabled, $V_{REF}$ voltage driven when powered down(2)<br>00 = $V_{DD}$ (unbuffered); $V_{REF}$ buffer disabled, use this state with power-down bits for lowest current |

**Note 1:** Unimplemented bit, read as '0'.

**2:** When the internal band gap is selected, the band gap voltage source will continue to output the voltage on the $V_{REF}$ pin in any of the Power-Down modes. To reduce the power consumption to its lowest level (band gap disabled), after selecting the desired Power-Down mode, the voltage reference should be changed to $V_{DD}$ or the $V_{REF}$ pin unbuffered ('00' or '10'), which turns off the Internal band gap circuitry. After wake-up, the user needs to reselect the internal band gap ('01') for the voltage reference source.


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Register 4-3 shows the format of the Power-Down Control register. Each DAC has two bits to control the power-down state of the DAC. This register is for the volatile memory locations and the nonvolatile memory locations. The width of this register is two times the number of DACs for the device.

**REGISTER 4-3: POWER-DOWN CONTROL REGISTERS (09h/19h) (VOLATILE/NONVOLATILE)**

| | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-n | R/W-n | R/W-n | R/W-n |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Single | — | — | — | — | — | — | — | — | — | — | — | — | —(1) | —(1) | PD0B | PD0A |
| Dual | — | — | — | — | — | — | — | — | — | — | — | — | PD1B | PD1A | PD0B | PD0A |
| | bit 15 | | | | | | | | | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |
| = Single channel device | = Dual channel device | | |

| Single | Dual | |
|---|---|---|
| bit 15-2 | bit 15-4 | **Unimplemented:** Read as '0' |
| bit 1-0 | bit 3-0 | **PDxB:PDxA:** DAC Power-Down Control bits(2)<br>11 = Powered down – $V_{OUT}$ is open circuit<br>10 = Powered down – $V_{OUT}$ is loaded with a 100 kΩ resistor to ground<br>01 = Powered down – $V_{OUT}$ is loaded with a 1 kΩ resistor to ground<br>00 = Normal operation (not powered down) |

**Note 1:** Unimplemented bit, read as '0'.

**2:** See Table 5-5 for more details.

Register 4-4 shows the format of the Gain Control and System Status register. Each DAC has one bit to control the gain of the DAC and two Status bits.

**REGISTER 4-4: GAIN CONTROL AND SYSTEM STATUS REGISTER (0Ah) (VOLATILE)**

| | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-n | R/W-n | R/C-1 | R | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Single | — | — | — | — | — | — | —(1) | G0 | POR | MTPMA | — | — | — | — | — | — |
| Dual | — | — | — | — | — | — | G1 | G0 | POR | MTPMA | — | — | — | — | — | — |
| | bit 15 | | | | | | | | | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | C = Clearable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |
| = Single channel device | = Dual channel device | | |

| Single | Dual | |
|---|---|---|
| bit 15-9 | bit 15-10 | **Unimplemented:** Read as '0' |
| — | bit 9 | **G1:** DAC1 Output Driver Gain Control bit<br>1 = 2x gain; not applicable when $V_{DD}$ is used as $V_{RL}$(2)<br>0 = 1x gain |
| bit 8 | bit 8 | **G0:** DAC0 Output Driver Gain Control bit<br>1 = 2x gain; not applicable when $V_{DD}$ is used as $V_{RL}$(2)<br>0 = 1x gain |
| bit 7 | bit 7 | **POR:** Power-on Reset (Brown-out Reset) Status bit<br>This bit indicates if a POR or BOR event has occurred since the last read command of this register. Reading this register clears the state of the POR Status bit.<br>1 = A POR (BOR) event occurred since the last read of this register; reading this register clears this bit<br>0 = A POR (BOR) event has not occurred since the last read of this register |
| bit 6 | bit 6 | **MTPMA:** MTP Memory Access Status bit(3)<br>This bit indicates if the MTP memory access is occurring.<br>1 = An MTP memory access is currently occurring (during the POR MTP read cycle or an MTP write cycle is occurring); only serial commands addressing the volatile memory are allowed<br>0 = An MTP memory access is NOT currently occurring |
| bit 5-0 | bit 5-0 | **Unimplemented:** Read as '0' |

**Note 1:** Unimplemented bit, read as '0'.

**2:** The DAC's Gain bit is ignored and the gain is forced to 1x (Gx = 0) when the DAC voltage reference is selected as $V_{DD}$ (VRxB:VRxA = 00).

**3:** For devices configured as volatile memory, this bit is read as '0'.


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Register 4-5 shows the format of the Nonvolatile Gain Control and Slave Address register. Each DAC has one bit to control the gain of the DAC. $I^2C$ devices also have seven bits that are the $I^2C$ Slave address.

**REGISTER 4-5: GAIN CONTROL AND SLAVE ADDRESS REGISTER (1Ah) (NONVOLATILE)**

| | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-n | R/W-n | U-0 | R/W-n | R/W-n | R/W-n | R/W-n | R/W-n | R/W-n | R/W-n |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Single | — | — | — | — | — | — | G1 | G0 | — | ADD6 | ADD5 | ADD4 | ADD3 | ADD2 | ADD1 | ADD0 |
| Dual | — | — | — | — | — | — | G1 | G0 | — | ADD6 | ADD5 | ADD4 | ADD3 | ADD2 | ADD1 | ADD0 |
| | bit 15 | | | | | | | | | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | C = Clearable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |
| = Single-channel device | = Dual-channel device | | |

| **Single** | **Dual** | |
|---|---|---|
| bit 15-10 | bit 15-10 | **Unimplemented:** Read as '0' |
| bit 9-8 | bit 9-8 | **Gx**: DAC Output Driver Gain Control bits(1)<br>1 = 2x gain<br>0 = 1x gain |
| bit 7 | bit 7 | **Unimplemented:** Read as '0' |
| bit 6-0 | bit 6-0 | **ADD6:ADD0**: $I^2C$ 7-Bit Slave Address bits(2) |

**Note 1:** When the DAC voltage reference is selected as $V_{DD}$ (VRxB:VRxA = 00), the DAC's Gain bit is ignored and the gain is forced to 1x (Gx = 0).

**2:** For $I^2C$ devices that have the A1 and A0 pins, the 7-bit Slave address is ADD6:ADD2 + A1:A0. For devices without the A1 and A0 pins, the 7-bit Slave address is ADD6:ADD0.

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Register 4-6 shows the format of the DAC WiperLock Technology Status register. The width of this register is two times the number of DACs for the device.

WiperLock technology bits only control access to volatile memory. Nonvolatile memory write access is controlled by the requirement of high voltage on the HVC pin, which is recommended to not be available during normal device operation.

**REGISTER 4-6: WiperLock™ TECHNOLOGY CONTROL REGISTER (1Bh) (NONVOLATILE)**

| | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-n | R/W-n | R/W-n | R/W-n |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Single | — | — | — | — | — | — | — | — | — | — | — | — | —(1) | —(1) | WL0B | WL0A |
| Dual | — | — | — | — | — | — | — | — | — | — | — | — | WL1B | WL1A | WL0B | WL0A |
| | bit 15 | | | | | | | | | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | C = Clearable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |
| = Single channel device | = Dual channel device | | |

| **Single** | **Dual** | |
|---|---|---|
| bit 15-2 | bit 15-4 | **Unimplemented:** Read as '0' |
| bit 1-0 | bit 3-1 | **WLxB:WLxA:** WiperLock™ Technology Status bits(2)<br>11 = Volatile DAC Wiper register and Volatile DAC Configuration bits are locked<br>10 = Volatile DAC Wiper register is locked and Volatile DAC Configuration bits are unlocked<br>01 = Volatile DAC Wiper register is unlocked and Volatile DAC Configuration bits are locked<br>00 = Volatile DAC Wiper register and Volatile DAC Configuration bits are unlocked |

**Note 1:** Unimplemented bit, read as '0'.

**2:** The Volatile PDxB:PDxA bits are NOT locked due to the requirement of being able to exit Power-Down mode.


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## 5.0 DAC CIRCUITRY

The Digital-to-Analog Converter circuitry converts a digital value into its analog representation. This description describes the functional operation of the device.

The DAC circuit uses a resistor ladder implementation. Devices have up to two DACs. Figure 5-1 shows the functional block diagram for the MCP47CXBXX DAC circuitry.

The functional blocks of the DAC include:

- Resistor Ladder
- Voltage Reference Selection
- Output Buffer/$V_{OUT}$ Operation
- Latch Pin (LAT)
- Power-Down Operation

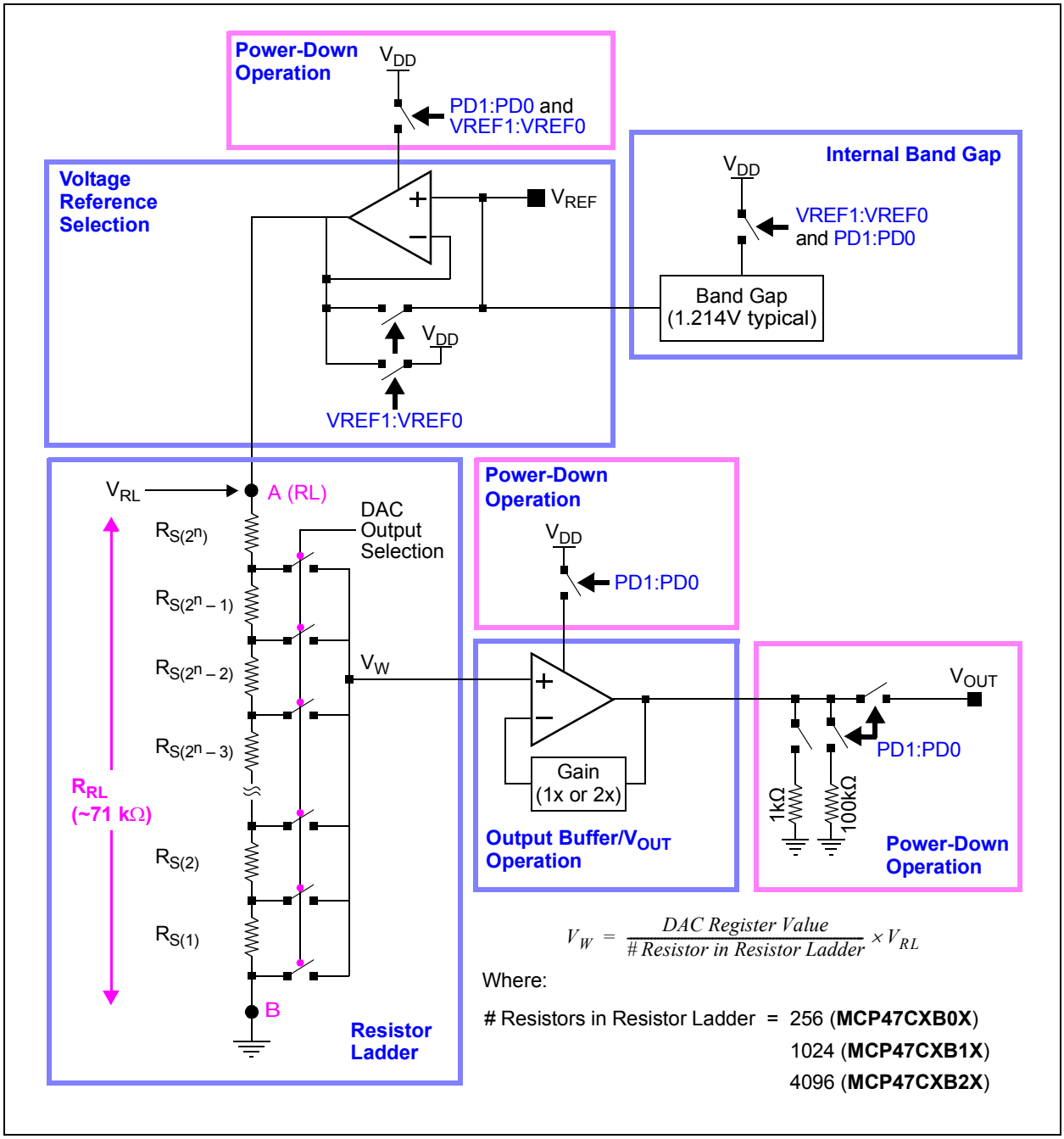



***FIGURE 5-1:*** *MCP47CXBXX DAC Module Block Diagram.*

## 5.1 Resistor Ladder

The resistor ladder is a digital potentiometer with the A Terminal connected to the selected reference voltage and the B Terminal internally grounded (see Figure 5-2). The Volatile DAC register controls the wiper position. The Wiper Voltage ($V_W$) is proportional to the DAC register value divided by the number of Resistor Elements ($R_S$) in the ladder (256, 1024 or 4096) related to the $V_{RL}$ voltage.

The output of the resistor network will drive the input of an output buffer.

The resistor network is made up of three parts:

- Resistor Ladder (string of $R_S$ elements)
- Wiper Switches
- DAC Register Decode

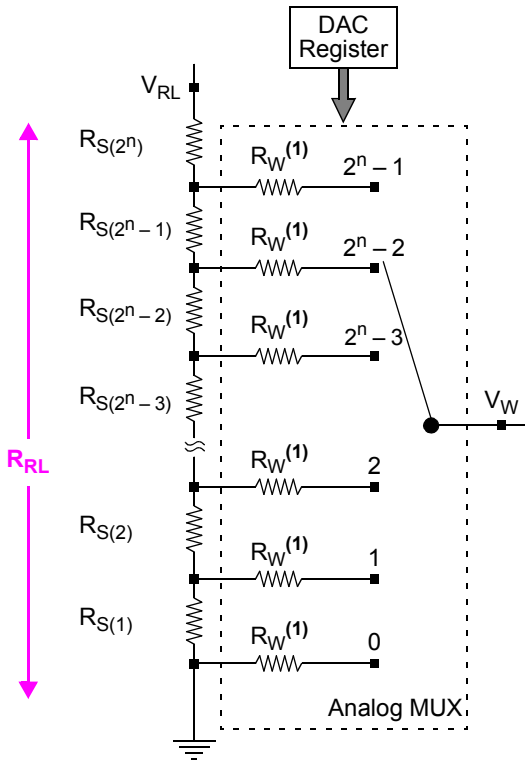
The resistor ladder has a typical impedance ($R_{RL}$) of approximately 71 kΩ. This Resistor Ladder Resistance ($R_{RL}$) may vary from device to device, up to ±10%. Since this is a voltage divider configuration, the actual $R_{RL}$ resistance does not affect the output, given a fixed voltage at $V_{RL}$.

Equation 5-1 shows the calculation for the step resistance.

| | |
|---|---|
| **Note:** | The maximum wiper position is $2^n - 1$, while the number of resistors in the resistor ladder is $2^n$. This means that when the DAC register is at full scale, there is one Resistor Element ($R_S$) between the wiper and the $V_{RL}$ voltage. |

If the unbuffered $V_{REF}$ pin is used as the $V_{RL}$ voltage source, the external voltage source should have a low output impedance.

When the DAC is powered down, the resistor ladder is disconnected from the selected reference voltage.




**Note 1:** The analog Switch Resistance ($R_W$) does not affect performance due to the voltage divider configuration.

***FIGURE 5-2:*** *Resistor Ladder Model Block Diagram.*

**EQUATION 5-1: $R_S$ CALCULATION**

$$R_S = \frac{R_{RL}}{(256)} \quad \textit{8-Bit Device}$$

$$R_S = \frac{R_{RL}}{(1024)} \quad \textit{10-Bit Device}$$

$$R_S = \frac{R_{RL}}{(4096)} \quad \textit{12-Bit Device}$$


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## 5.2 Voltage Reference Selection

The resistor ladder has up to four sources for the reference voltage. The selection of the voltage reference source is specified with the Volatile VREF1:VREF0 Configuration bits (see Register 4-2). The selected voltage source is connected to the $V_{RL}$ node (see Figure 5-3 and Figure 5-4).

The four voltage source options for the Resistor Ladder are:

1. $V_{DD}$ pin voltage.
2. Internal Band Gap Voltage Reference ($V_{BG}$).
3. $V_{REF}$ pin voltage – unbuffered.
4. $V_{REF}$ pin voltage – internally buffered.

On a POR/BOR event, the default configuration state or the value written in the Nonvolatile register is latched into the Volatile VREF1:VREF0 Configuration bits.

If the $V_{REF}$ pin is used with an external voltage source, then the user must select between Buffered or Unbuffered mode.

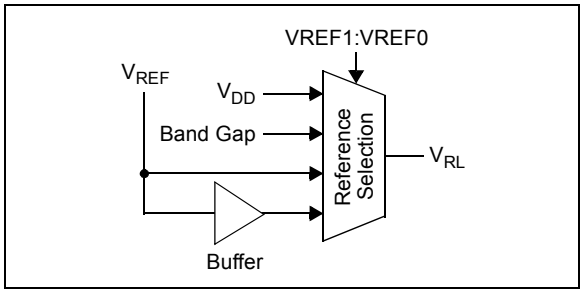
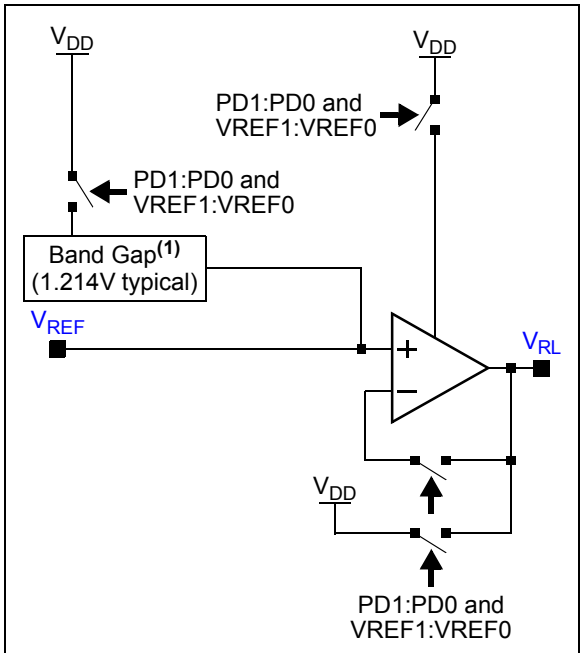



***FIGURE 5-3:*** *Resistor Ladder Reference Voltage Selection Block Diagram.*




**Note 1:** The Band Gap Voltage ($V_{BG}$) is 1.214V typical. The band gap output goes through the buffer with a 2x gain to create the $V_{RL}$ voltage. See Table 5-1 for additional information on the band gap circuit.

***FIGURE 5-4:*** *Reference Voltage Selection Implementation Block Diagram.*

### 5.2.1 USING $V_{DD}$ AS $V_{REF}$

When the user selects the $V_{DD}$ as reference, the $V_{REF}$ pin voltage is not connected to the resistor ladder. The $V_{DD}$ voltage is internally connected to the resistor ladder.

### 5.2.2 USING AN EXTERNAL $V_{REF}$ SOURCE IN UNBUFFERED MODE

In this case, the $V_{REF}$ pin voltage may vary from $V_{SS}$ to $V_{DD}$. The voltage source should have a low output impedance. If the voltage source has a high output impedance, then the voltage on the $V_{REF}$ pin could be lower than expected. The resistor ladder has a typical impedance of 71 kΩ and a typical capacitance of 29 pF.

If a single $V_{REF}$ pin is supplying multiple DACs, the $V_{REF}$ pin source must have adequate current capability to support the number of DACs. It must be assumed that the Resistor Ladder Resistance ($R_{RL}$) of each DAC is at the minimum specified resistance and these resistances are in parallel.

If the $V_{REF}$ pin is tied to the $V_{DD}$ voltage, selecting the $V_{DD}$ Reference mode (VREF1:VREF0 = 00) is recommended.

### 5.2.3 USING AN EXTERNAL $V_{REF}$ SOURCE IN BUFFERED MODE

The $V_{REF}$ pin voltage may be from 0V to $V_{DD}$. The input buffer (amplifier) provides low offset voltage, low noise, and a very high input impedance, with only minor limitations on the input range and frequency response.

Any variation or noises on the reference source can directly affect the DAC output. The reference voltage needs to be as clean as possible for accurate DAC performance.

### 5.2.4 USING THE INTERNAL BAND GAP AS VOLTAGE REFERENCE

The internal band gap is designed to drive the resistor ladder buffer.

If the internal band gap is selected, then the band gap voltage source will drive the external $V_{REF}$ pins. The $V_{REF0}$ pin can source up to 1 mA of current without affecting the DAC output specifications. The $V_{REF1}$ pin must be left unloaded in this mode. The voltage reference source can be independently selected on devices with two DAC channels, but restrictions apply:

- The $V_{DD}$ mode can be used without issues on any channel.
- When the internal band gap is selected as the voltage source, all the $V_{REF}$ pins are connected to its output. The use of the Unbuffered mode is only possible on $V_{REF0}$, because it's the only one that can be loaded.
- When using the Internal Band Gap mode on Channel 0, Channel 1 must be put in Buffered External $V_{REF}$ mode or $V_{DD}$ Reference mode and the $V_{REF1}$ pin must be left unloaded.

The resistance of the Resistor Ladder ($R_{RL}$) is targeted to be 71 kΩ (±10%), which means a minimum resistance of 63.9 kΩ.

The band gap selection can be used across the $V_{DD}$ voltages while maximizing the $V_{OUT}$ voltage ranges. For $V_{DD}$ voltages below the Gain ∗ $V_{BG}$ voltage, the output for the upper codes will be clipped to the $V_{DD}$ voltage. Table 5-1 shows the maximum DAC register code given device $V_{DD}$ and Gain bit setting.

**TABLE 5-1: $V_{OUT}$ USING BAND GAP**

| $V_{DD}$ | DAC Gain | Max DAC Code(1) | | | Comment |
|---|---|---|---|---|---|
| | | 12-Bit | 10-Bit | 8-Bit | |
| 5.5 | 1 | FFFh | 3FFh | FFh | $V_{OUT(max)}$ = 1.214V(3) |
| | 2 | FFFh | 3FFh | FFh | $V_{OUT(max)}$ = 2.428V(3) |
| 2.7 | 1 | FFFh | 3FFh | FFh | $V_{OUT(max)}$ = 1.214V(3) |
| | 2 | FFFh | 3FFh | FFh | $V_{OUT(max)}$ = 2.428V |
| 1.8 | 1 | FFFh | 3FFh | FFh | $V_{OUT(max)}$ = 1.214V |
| | 2(2) | BBCh | 2EFh | BBh | 1.8V |

**Note 1:** Without the $V_{OUT}$ pin voltage being clipped.
**2:** Recommended to use the Gain = 1 setting.
**3:** When $V_{BG}$ = 1.214V typical.

## 5.3 Output Buffer/$V_{OUT}$ Operation

The output driver buffers the Wiper Voltage ($V_W$) of the resistor ladder.

The DAC output is buffered with a low-power, precision output amplifier with selectable gain. This amplifier provides a rail-to-rail output with low offset voltage and low noise. The amplifier's output can drive the resistive and high-capacitive loads without oscillation. The amplifier provides a maximum load current, which is enough for most programmable voltage reference applications. Refer to **Section 1.0 "Electrical Characteristics"** for the specifications of the output amplifier.

| **Note:** | The load resistance must be kept higher than 2 kΩ to maintain stability of the analog output and have it meet electrical specifications. |
|---|---|

Figure 5-5 shows a block diagram of the output driver circuit.

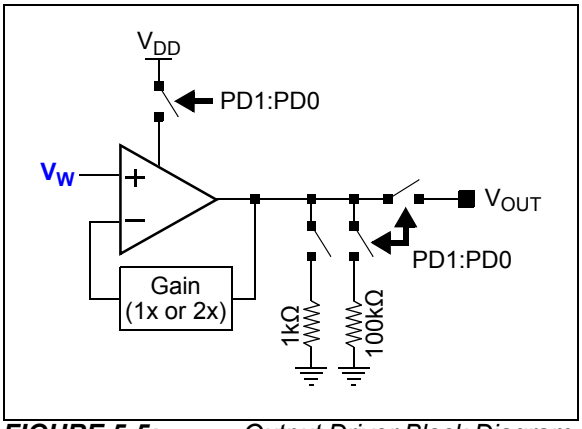



***FIGURE 5-5:*** *Output Driver Block Diagram.*

Power-down logic also controls the output buffer operation (see **Section 5.5 "Power-Down Operation"** for additional information on power-down). In any of the three Power-Down modes, the output amplifier is powered down and its output becomes a high-impedance to the $V_{OUT}$ pin.

### 5.3.1 PROGRAMMABLE GAIN

The amplifier's gain is controlled by the Gain (G) Configuration bit (see Register 4-4) and the $V_{RL}$ reference selection (see Register 4-2).

The Gain options are:

a) Gain of 1, with either the $V_{DD}$ or $V_{REF}$ pin used as the reference voltage.

b) Gain of 2, only when the $V_{REF}$ pin or the internal band gap is used as the reference voltage. The $V_{REF}$ pin voltage should be limited to $V_{DD}/2$. When the Reference Voltage Selection ($V_{RL}$) is the device's $V_{DD}$ voltage, the Gx bit is ignored and a gain of 1 is used.


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Table 5-2 shows the gain bit operation.

**TABLE 5-2: OUTPUT DRIVER GAIN**

| Gain Bit | Gain | Comment |
|---|---|---|
| 0 | 1 | |
| 1 | 2 | Limits $V_{REF}$ pin voltages relative to device $V_{DD}$ voltage. |

The volatile G bit value can be modified by:

- POR Event
- BOR Event
- $I^2C$ Write Commands
- $I^2C$ General Call Reset Command

### 5.3.2 OUTPUT VOLTAGE

The Volatile DAC register values, along with the device's Configuration bits, control the analog $V_{OUT}$ voltage. The Volatile DAC register's value is unsigned binary. The formula for the output voltage is provided in Equation 5-2. Examples of Volatile DAC register values and the corresponding theoretical $V_{OUT}$ voltage for the MCP47CXBXX devices are shown in Table 5-6.

**EQUATION 5-2: CALCULATING OUTPUT VOLTAGE ($V_{OUT}$)**

$$V_{OUT} = \frac{V_{RL} \times DAC\ Register\ Value}{\#\ Resistor\ in\ Resistor\ Ladder} \times Gain$$

Where:

# Resistors in R-Ladder = 4096 (MCP47CXB2X)
1024 (MCP47CXB1X)
256 (MCP47CXB0X)

When Gain = 2 ($V_{RL} = V_{REF}$), if $V_{REF} > V_{DD}/2$, the $V_{OUT}$ voltage is limited to $V_{DD}$. So if $V_{REF} = V_{DD}$, the $V_{OUT}$ voltage does not change for Volatile DAC register values mid-scale and greater, since the output amplifier is at full-scale output.

The following events update the DAC register value, and therefore, the analog Voltage Output ($V_{OUT}$):

- Power-on Reset
- Brown-out Reset
- $I^2C$ write command (to Volatile registers) on the rising edge of the last write command bit
- $I^2C$ General Call Reset command; the output is updated with default POR data or MTP values
- $I^2C$ general call wake-up command; the output is updated with default POR data or MTP values

Next, the $V_{OUT}$ voltage starts driving to the new value after the event has occurred.

### 5.3.3 STEP VOLTAGE ($V_S$)

The step voltage depends on the device resolution and the calculated output voltage range. One LSb is defined as the ideal voltage difference between two successive codes. The step voltage can easily be calculated by using Equation 5-3 (the DAC register value is equal to '1'). Theoretical step voltages are shown in Table 5-3 for several $V_{REF}$ voltages.

**EQUATION 5-3: $V_S$ CALCULATION**

$$V_S = \frac{V_{RL}}{\#\ Resistor\ in\ Resistor\ Ladder} \times Gain$$

Where:

# Resistors in R-Ladder = 4096 (12-bit)
1024 (10-bit)
256 (8-bit)

**TABLE 5-3: THEORETICAL STEP VOLTAGE ($V_S$)(1)**

| Step Voltage | $V_{REF}$ | | | | | |
|---|---|---|---|---|---|---|
| | **5.0** | **2.7** | **1.8** | **1.5** | **1.0** | |
| $V_S$ | 1.22 mV | 659 uV | 439 uV | 366 uV | 244 uV | 12-bit |
| | 4.88 mV | 2.64 mV | 1.76 mV | 1.46 mV | 977 uV | 10-bit |
| | 19.5 mV | 10.5 mV | 7.03 mV | 5.86 mV | 3.91 mV | 8-bit |

**Note 1:** When Gain = 1x, $V_{FS} = V_{RL}$ and $V_{ZS} = 0V$.

### 5.3.4 OUTPUT SLEW RATE

Figure 5-6 shows an example of the slew rate of the $V_{OUT}$ pin. The slew rate can be affected by the characteristics of the circuit connected to the $V_{OUT}$ pin.

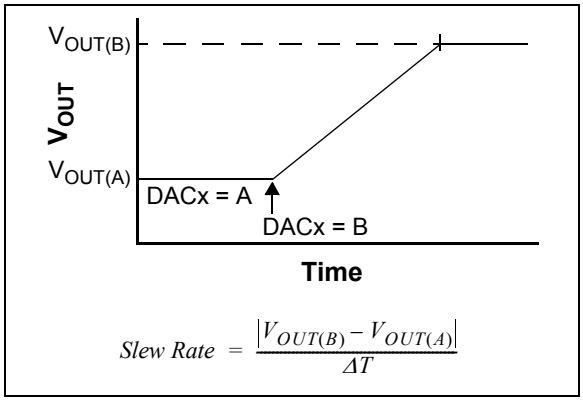



***FIGURE 5-6:*** *$V_{OUT}$ Pin Slew Rate.*

#### 5.3.4.1 Small Capacitive Load

With a small capacitive load, the output buffer's current is not affected by the Capacitive Load ($C_L$). But still, the $V_{OUT}$ pin's voltage is not a step transition from one output value (DAC register value) to the next output value. The change of the $V_{OUT}$ voltage is limited by the output buffer's characteristics, so the $V_{OUT}$ pin voltage will have a slope from the old voltage to the new voltage. This slope is fixed for the output buffer, and is referred to as the Buffer Slew Rate ($SR_{BUF}$).

#### 5.3.4.2 Large Capacitive Load

With a larger capacitive load, the slew rate is determined by two factors:

- The output buffer's Short-Circuit Current ($I_{SC}$)
- The $V_{OUT}$ pin's external load

$I_{OUT}$ cannot exceed the output buffer's Short-Circuit Current ($I_{SC}$), which fixes the output Buffer Slew Rate ($SR_{BUF}$). The voltage on the Capacitive Load ($C_L$), $V_{CL}$, changes at a rate proportional to $I_{OUT}$, which fixes a Capacitive Load Slew Rate ($SR_{CL}$).

The $V_{CL}$ voltage slew rate is limited to the slower of the output buffer's internally Set Slew Rate (SRBUF) and the Capacitive Load Slew Rate ($SR_{CL}$).

### 5.3.5 DRIVING RESISTIVE AND CAPACITIVE LOADS

The $V_{OUT}$ pin can drive up to 100 pF of capacitive load in parallel with a 5 kΩ resistive load (to meet electrical specifications). $V_{OUT}$ drops slowly as the load resistance decreases after about 3.5 kΩ. It is recommended to use a load with $R_L$ greater than 2 kΩ.

Refer to **Section 2.0 "Typical Performance Curves"** for a detailed $V_{OUT}$ vs. Resistive Load characterization graph.

Driving large capacitive loads can cause stability problems for voltage feedback output amplifiers. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response with overshoot and ringing in the step response. That is, since the $V_{OUT}$ pin's voltage does not quickly follow the buffer's input voltage (due to the large capacitive load), the output buffer will overshoot the desired target voltage. Once the driver detects this overshoot, it compensates by forcing it to a voltage below the target. This causes voltage ringing on the $V_{OUT}$ pin.

So, when driving large capacitive loads with the output buffer, a small Series Resistor ($R_{ISO}$) at the output (see Figure 5-7) improves the output buffer's stability (feedback loop's phase margin) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

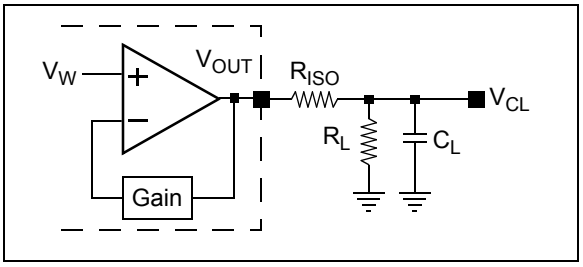



***FIGURE 5-7:*** *Circuit to Stabilize Output Buffer for Large Capacitive Loads ($C_L$).*

The $R_{ISO}$ resistor value for your circuit needs to be selected. The resulting frequency response peaking and step response overshoot for this $R_{ISO}$ resistor value should be verified on the bench. Modify the $R_{ISO}$'s resistance value until the output characteristics meet your requirements.

A method to evaluate the system's performance is to inject a step voltage on the $V_{REF}$ pin and observe the $V_{OUT}$ pin's characteristics.

| **Note:** | Additional insight into circuit design for driving capacitive loads can be found in *AN884, "Driving Capacitive Loads With Op Amps"* (DS00884). |
|---|---|


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## 5.4 Latch Pin ($\overline{LAT}$)

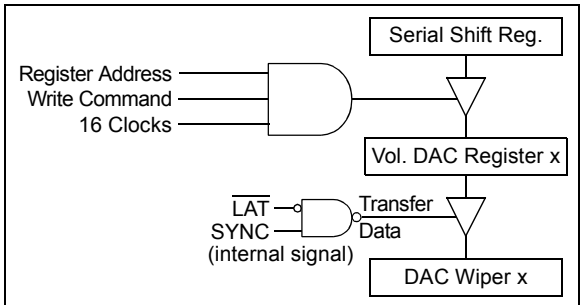
The Latch pin controls when the Volatile DAC register value is transferred to the DAC wiper. This is useful for applications that need to synchronize the wiper(s) updates to an external event, such as zero-crossing or updates to the other wipers on the device. The $\overline{LAT}$ pin is asynchronous to the serial interface operation.

When the $\overline{LAT}$ pin is high, transfers from the Volatile DAC register to the DAC wiper are inhibited. The Volatile DAC register value(s) can continue to be updated.

When the $\overline{LAT}$ pin is low, the Volatile DAC register value is transferred to the DAC wiper.

| **Note:** | This allows both the Volatile DAC0 and DAC1 registers to be updated while the $\overline{LAT}$ pin is high, and to have outputs synchronously updated as the $\overline{LAT}$ pin is driven low. |
|---|---|

Figure 5-8 shows the interaction of the $\overline{LAT}$ pin and the loading of the DAC Wiper x (from the Volatile DAC Register x). The transfers are level-driven. If the $\overline{LAT}$ pin is held low, the corresponding DAC wiper is updated as soon as the Volatile DAC register value is updated.




| $\overline{LAT}$ | SYNC | Transfer Data | Comment |
|---|---|---|---|
| 1 | 1 | 0 | No Transfer |
| 1 | 0 | 0 | No Transfer |
| 0 | 1 | 1 | Vol. DAC Register x → DAC Wiper x |
| 0 | 0 | 0 | No Transfer |

***FIGURE 5-8:*** *$\overline{LAT}$ and DAC Interaction.*

The $\overline{LAT}$ pin allows the DAC wiper to be updated to an external event and to have multiple DAC channels/devices update at a common event.

Since the DAC Wiper x is updated from the Volatile DAC Register x, all DACs that are associated with a given $\overline{LAT}$ pin can be updated synchronously.

If the application does not require synchronization, then this signal should be tied low.

Figure 5-9 shows two cases of using the $\overline{LAT}$ pin to control when the Wiper register is updated relative to the value of a sine wave signal.

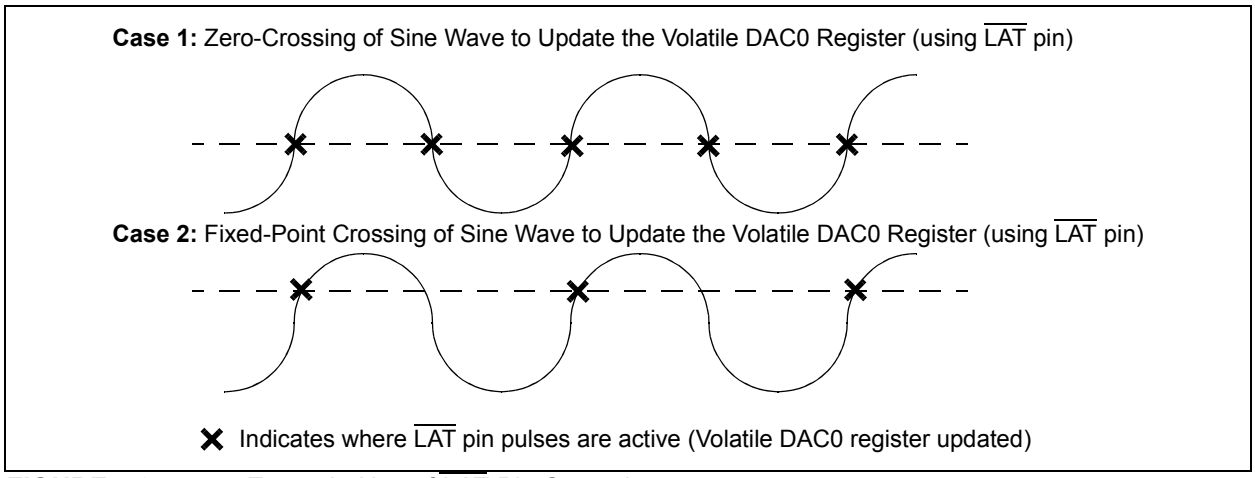



***FIGURE 5-9:*** *Example Use of $\overline{LAT}$ Pin Operation.*

## 5.5 Power-Down Operation

To allow the application to conserve power when DAC operation is not required, three Power-Down modes are available. On devices with multiple DACs, each DAC's Power-Down mode is individually controllable.

All Power-Down modes do the following:

- Turn off most of the DAC module's internal circuits
- Op amp output becomes high-impedance to the $V_{OUT}$ pin
- Retain the value of the Volatile DAC register and Configuration bits

Depending on the selected Power-Down mode, the following will occur:

- $V_{OUT}$ pin is switched to one of the two resistive pull-downs:
  - 100 kΩ (typical)
  - 1 kΩ (typical)
- Op amp is powered down and the $V_{OUT}$ pin becomes high-impedance

The Power-Down Configuration bits (PD1:PD0) control the power-down operation (Table 5-4).

**TABLE 5-4: POWER-DOWN BITS AND OUTPUT RESISTIVE LOAD**

| PD1 | PD0 | Function |
|---|---|---|
| 0 | 0 | Normal operation |
| 0 | 1 | 1 kΩ resistor to ground |
| 1 | 0 | 100 kΩ resistor to ground |
| 1 | 1 | Open circuit |

There is a delay ($T_{PDD}$) between the PD1:PD0 bits changing from '00' to either '01', '10' or '11' and the op amp no longer driving the $V_{OUT}$ output, and the pull-down resistors' sinking current.

In any of the Power-Down modes, where the $V_{OUT}$ pin is not externally connected (sinking or sourcing current), as the number of DACs increases, the device's power-down current will also increase.

Table 5-5 shows the current sources for the DAC based on the selected source of the DAC's reference voltage and if the device is in normal operating mode or one of the Power-Down modes.

**TABLE 5-5: DAC CURRENT SOURCES**

| Device $V_{DD}$ Current Source | PDxB:xA = 00, VREFxB:xA = | | | | PDxB:xA ≠ 00, VREFxB:xA = | | | |
|---|---|---|---|---|---|---|---|---|
| | 00 | 01 | 10 | 11 | 00 | 01 | 10 | 11 |
| Output Op Amp | Y | Y | Y | Y | N | N | N | N |
| Resistor Ladder | Y | Y | N(1) | Y | N | N | N(1) | N |
| $V_{REF}$ Selection Buffer | N | Y | N | Y | N | N | N | N |
| Band Gap | N | Y | N | N | N(2) | Y(2) | N(2) | N(2) |

**Note 1:** The current is sourced from the $V_{REF}$ pin, not the device $V_{DD}$.
**2:** If DAC0 and DAC1 are in one of the Power-Down modes, MTP write operations are not recommended.

The power-down bits are modified by using a write command to the Volatile Power-Down register, or a POR event, which transfers the Nonvolatile Power-Down register to the Volatile Power-Down register.

**Section 7.0 "Device Commands"** describes the $I^2C$ commands for writing the power-down bits. The commands that can update the volatile PD1:PD0 bits are:

- Write
- General Call Reset
- General Call Wake-up

**Note 1:** The $I^2C$ serial interface circuit is not affected by the Power-Down mode. This circuit remains active in order to receive any command that might come from the $I^2C$ Master device.
**2:** A General Call Reset will do the POR event sequence, except that the MTP shadow memory values will be transfered to the Volatile Memory registers.

### 5.5.1 EXITING POWER-DOWN

The following events change the PD1:PD0 bits to '00', and therefore, exit the Power-Down mode. These are:

- Any $I^2C$ Write Command, where the PD1:PD0 bits are '00'
- $I^2C$ General Call Wake-up Command
- $I^2C$ General Call Reset Command

When the device exits Power-Down mode, the following occurs:

- Disabled internal circuits are turned on
- Resistor ladder is connected to the selected Reference Voltage ($V_{RL}$)
- Selected pull-down resistor is disconnected
- The $V_{OUT}$ output is driven to the voltage represented by the Volatile DAC register's value and Configuration bits

The DAC Wiper register and DAC wiper value may be different due to the DAC Wiper register being modified while the $\overline{LAT}$ pin was driven to (and remaining at) $V_{IH}$.

The $V_{OUT}$ output signal requires time as these circuits are powered up and the output voltage is driven to the specified value, as determined by the Volatile DAC register and Configuration bits.

**Note:** Since the op amp and resistor ladder were powered off (0V), the op amp's Input Voltage ($V_W$) can be considered as 0V. There is a delay ($T_{PDE}$) between the PD1:PD0 bits updating to '00' and the op amp driving the $V_{OUT}$ output. The op amp's settling time (from 0V) needs to be taken into account to ensure the $V_{OUT}$ voltage reflects the selected value.


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**TABLE 5-6: DAC INPUT CODE VS. CALCULATED ANALOG OUTPUT ($V_{OUT}$) ($V_{DD}$ = 5.0V)**

| Device | Volatile DAC Register Value | $V_{RL}$ (1) | LSb | | Gain Selection (2) | $V_{OUT}$ (3) | |
|---|---|---|---|---|---|---|---|
| | | | Equation | µV | | Equation | V |
| **MCP47CVB2X** (12-bit) | 1111 1111 1111 | 5.0V | 5.0V/4096 | 1,220.7 | 1x | $V_{RL} * (4095/4096) * 1$ | 4.998779 |
| | | 2.5V | 2.5V/4096 | 610.4 | 1x | $V_{RL} * (4095/4096) * 1$ | 2.499390 |
| | | | | | 2x(2) | $V_{RL} * (4095/4096) * 2$) | 4.998779 |
| | 0111 1111 1111 | 5.0V | 5.0V/4096 | 1,220.7 | 1x | $V_{RL} * (2047/4096) * 1$) | 2.498779 |
| | | 2.5V | 2.5V/4096 | 610.4 | 1x | $V_{RL} * (2047/4096) * 1$) | 1.249390 |
| | | | | | 2x(2) | $V_{RL} * (2047/4096) * 2$) | 2.498779 |
| | 0011 1111 1111 | 5.0V | 5.0V/4096 | 1,220.7 | 1x | $V_{RL} * (1023/4096) * 1$) | 1.248779 |
| | | 2.5V | 2.5V/4096 | 610.4 | 1x | $V_{RL} * (1023/4096) * 1$) | 0.624390 |
| | | | | | 2x(2) | $V_{RL} * (1023/4096) * 2$) | 1.248779 |
| | 0000 0000 0000 | 5.0V | 5.0V/4096 | 1,220.7 | 1x | $V_{RL} * (0/4096) * 1$) | 0 |
| | | 2.5V | 2.5V/4096 | 610.4 | 1x | $V_{RL} * (0/4096) * 1$) | 0 |
| | | | | | 2x(2) | $V_{RL} * (0/4096) * 2$) | 0 |
| **MCP47CVB1X** (10-bit) | 11 1111 1111 | 5.0V | 5.0V/1024 | 4,882.8 | 1x | $V_{RL} * (1023/1024) * 1$ | 4.995117 |
| | | 2.5V | 2.5V/1024 | 2,441.4 | 1x | $V_{RL} * (1023/1024) * 1$ | 2.497559 |
| | | | | | 2x(2) | $V_{RL} * (1023/1024) * 2$ | 4.995117 |
| | 01 1111 1111 | 5.0V | 5.0V/1024 | 4,882.8 | 1x | $V_{RL} * (511/1024) * 1$ | 2.495117 |
| | | 2.5V | 2.5V/1024 | 2,441.4 | 1x | $V_{RL} * (511/1024) * 1$ | 1.247559 |
| | | | | | 2x(2) | $V_{RL} * (511/1024) * 2$ | 2.495117 |
| | 00 1111 1111 | 5.0V | 5.0V/1024 | 4,882.8 | 1x | $V_{RL} * (255/1024) * 1$ | 1.245117 |
| | | 2.5V | 2.5V/1024 | 2,441.4 | 1x | $V_{RL} * (255/1024) * 1$ | 0.622559 |
| | | | | | 2x(2) | $V_{RL} * (255/1024) * 2$ | 1.245117 |
| | 00 0000 0000 | 5.0V | 5.0V/1024 | 4,882.8 | 1x | $V_{RL} * (0/1024) * 1$ | 0 |
| | | 2.5V | 2.5V/1024 | 2,441.4 | 1x | $V_{RL} * (0/1024) * 1$ | 0 |
| | | | | | 2x(2) | $V_{RL} * (0/1024) * 1$ | 0 |
| **MCP47CVB0X** (8-bit) | 1111 1111 | 5.0V | 5.0V/256 | 19,531.3 | 1x | $V_{RL} * (255/256) * 1$ | 4.980469 |
| | | 2.5V | 2.5V/256 | 9,765.6 | 1x | $V_{RL} * (255/256) * 1$ | 2.490234 |
| | | | | | 2x(2) | $V_{RL} * (255/256) * 2$ | 4.980469 |
| | 0111 1111 | 5.0V | 5.0V/256 | 19,531.3 | 1x | $V_{RL} * (127/256) * 1$ | 2.480469 |
| | | 2.5V | 2.5V/256 | 9,765.6 | 1x | $V_{RL} * (127/256) * 1$ | 1.240234 |
| | | | | | 2x(2) | $V_{RL} * (127/256) * 2$ | 2.480469 |
| | 0011 1111 | 5.0V | 5.0V/256 | 19,531.3 | 1x | $V_{RL} * (63/256) * 1$ | 1.230469 |
| | | 2.5V | 2.5V/256 | 9,765.6 | 1x | $V_{RL} * (63/256) * 1$ | 0.615234 |
| | | | | | 2x(2) | $V_{RL} * (63/256) * 2$ | 1.230469 |
| | 0000 0000 | 5.0V | 5.0V/256 | 19,531.3 | 1x | $V_{RL} * (0/256) * 1$ | 0 |
| | | 2.5V | 2.5V/256 | 9,765.6 | 1x | $V_{RL} * (0/256) * 1$ | 0 |
| | | | | | 2x(2) | $V_{RL} * (0/256) * 2$ | 0 |

**Note 1:** $V_{RL}$ is the resistor ladder's reference voltage. It is independent of the VREF1:VREF0 selection.

**2:** Gain selection of 2x (Gx = 1) requires the voltage reference source to come from the $V_{REF}$ pin (VREF1:VREF0 = 10 or 11) and requires $V_{REF}$ pin voltage (or $V_{RL}$) ≤ $V_{DD}/2$ or from the internal band gap (VREF1:VREF0 = 01).

**3:** These theoretical calculations do not take into account the offset, gain and nonlinearity errors.

**NOTES:**


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# 6.0 I²C SERIAL INTERFACE MODULE

The MCP47CXBXX's I²C serial interface module supports the I²C serial protocol specification. This I²C interface is a two-wire interface (clock and data). Figure 6-1 shows a typical I²C interface connection.

The I²C specification only defines the field types, lengths, timings, etc., of a frame. The frame content defines the behavior of the device. The frame content (commands) for the MCP47CXBXX is defined in **Section 7.0 "Device Commands"**.

An overview of the I²C protocol is available in **Appendix B: "I²C Serial Interface"**.

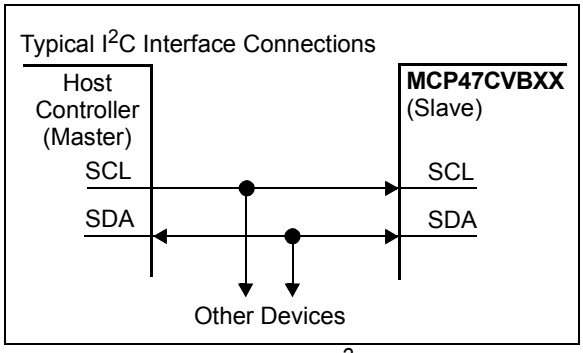



***FIGURE 6-1:*** *Typical I²C Interface.*

## 6.1 Overview

This section discusses some of the specific characteristics of the MCP47CXBXX devices' I²C serial interface module. This is to assist in the development of your application.

The following sections discuss some of these device-specific characteristics.

- Interface Pins (SCL and SDA)
- Communication Data Rates
- POR/BOR
- Device Memory Address
- General Call Commands
- Device I²C Slave Addressing
- Slope Control

### 6.1.1 INTERFACE PINS (SCL AND SDA)

The MCP47CXBXX I²C module SCL pin does not generate the serial clock since the device operates in Slave mode. Also, the MCP47CXBXX will not stretch the clock signal (SCL) since memory read access occurs fast enough.

The MCP47CXBXX I²C module implements slope control on the SDA pin output driver.

## 6.2 Communication Data Rates

The I²C interface specifies different communication bit rates. These are referred to as Standard, Fast or High-Speed modes. The MCP47CXBXX supports these three modes. The clock rates (bit rate) of these modes are:

- Standard mode: Up to 100 kHz (kbit/s)
- Fast mode: Up to 400 kHz (kbit/s)
- High-Speed mode (HS mode): Up to 3.4 MHz (Mbit/s)

A description on how to enter High-Speed mode is described in **Section 6.8 "Slope Control"**.

## 6.3 POR/BOR

On a POR/BOR event, the I²C serial interface module state machine is reset, which includes forcing the device's Memory Address Pointer to 00h.

## 6.4 Device Memory Address

The memory address is the 5-bit value that specifies the location in the device's memory that the specified command will operate on.

On a POR/BOR event, the device's Memory Address Pointer is forced to 00h.

The MCP47CXBXX retains the last received "Device Memory Address". That is, the MCP47CXBXX does not "corrupt" the "device memory address" after Repeated Start or Stop conditions.

## 6.5 General Call Commands

The general call commands utilize the I²C specification reserved general call command address and command codes. The MCP47CXBXX also implements a nonstandard general call command.

The general call commands are:

- General Call Reset
- General Call Wake-up (MCP47CXBXX defined)

The general call wake-up command will cause all the MCP47CXBXX devices to exit their power-down state.

## 6.6 Multi-Master Systems

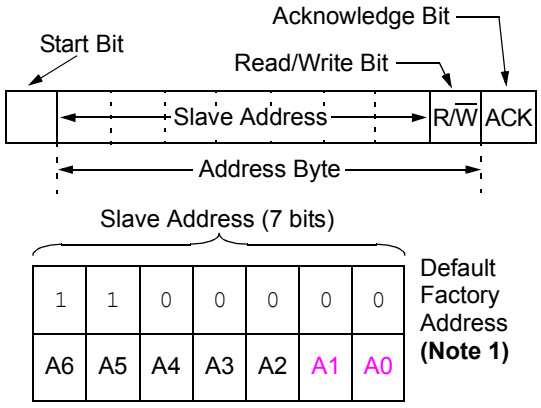
The MCP47CXBXX is not a Master device (generates the interface clock), but it can be used in Multi-Master applications.

## 6.7 Device I²C Slave Addressing

The address byte is the first byte received following the Start (or Repeated Start) condition from the Master device (see Figure 6-2). For nonvolatile devices, the seven bits of the I²C Slave address are user-programmable. The default address is '110 0000'. If the address pins are present on the specific package, the lower two bits of the address are determined by the state of the A1 and A0 pins.

| | |
|---|---|
| **Note:** | Address bits, A6:A0, are MTP and can be programmed during the user's manufacturing flow. |

For volatile devices (MCP47CVBXX), the I²C Slave address bits, A6:A0, are fixed ('110 0000'). The user still has Slave address programmability with the A1:A0 address pins (if available on the package).




**Note 1:** Address bits (A6:A0) can be programmed by the user (MCP47CMBXX devices). Bits A1 and A0 are determined by either the MTP bits or the A0 and A1 pin values if present on the package.

***FIGURE 6-2:*** *Slave Address Bits in the I²C Control Byte.*

Table 6-1 shows the four standard orderable I²C Slave addresses and their respective device order codes.

**TABLE 6-1: I²C ADDRESS/ORDER CODE**

| Default 7-Bit I²C Address | Device Order Code(1) | Memory | | Tape and Reel |
|---|---|---|---|---|
| | | VOL | NV | |
| '1100000' | MCP47CXBXX-E/XX | Y | Y | N |
| | MCP47CXBXXT-E/XX | Y | Y | Y |

**Note 1:** Nonvolatile devices' I²C Slave address can be reprogrammed by the end user.

### 6.7.1 CUSTOM I²C SLAVE ADDRESS OPTIONS

Custom I²C Slave address options can be requested. Users can request the custom I²C Slave address via the Nonstandard Customer Authorization Request (NSCAR) process.

| | |
|---|---|
| **Note:** | Non-Recurring Engineering (NRE) charges and minimum ordering requirements for custom orders. Please contact Microchip sales for additional information.<br><br>A custom device will be assigned custom device marking. |

## 6.8 Slope Control

The slope control on the SDA output is different between the Fast/Standard Speed and the High-Speed Clock modes of the interface.

## 6.9 Pulse Gobbler

The pulse gobbler on the SCL pin is automatically adjusted to suppress spikes <10 ns during HS mode.


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## 6.10 Entering High-Speed (HS) Mode

The $I^2C$ specification requires that a High-Speed mode device be 'activated' to operate in High-Speed (3.4 Mbit/s) mode. This is done by the Master sending a special address byte following the Start bit. This byte is referred to as the High-Speed Master Mode Code (HSMMC).

The device can now communicate at up to 3.4 Mbit/s on SDA and SCL lines. The device will switch out of the HS mode on the next Stop condition.

The Master code is sent as follows:

1. Start condition (S).
2. High-Speed Master Mode Code ('0000 1xxx'); the 'xxx' bits are unique to the High-Speed (HS) Master mode.
3. No Acknowledge ($\overline{A}$).

After switching to High-Speed mode, the next transferred byte is the $I^2C$ control byte, which specifies the device to communicate with and any number of data bytes plus Acknowledgments. The Master device can then either issue a Repeated Start bit to address a different device (at High-Speed mode) or a Stop bit to return to the bus Fast/Standard Speed mode. After the Stop bit, any other Master device (in a Multi-Master system) can arbitrate for the $I^2C$ bus.

The MCP47CXBXX device does not Acknowledge the HS select byte. However, upon receiving this command, the device switches to HS mode.

See Figure 6-3 for an illustration of the HS mode command sequence.

For more information on the HS mode, or other $I^2C$ modes, refer to the *"NXP $I^2C$ Specification"*.

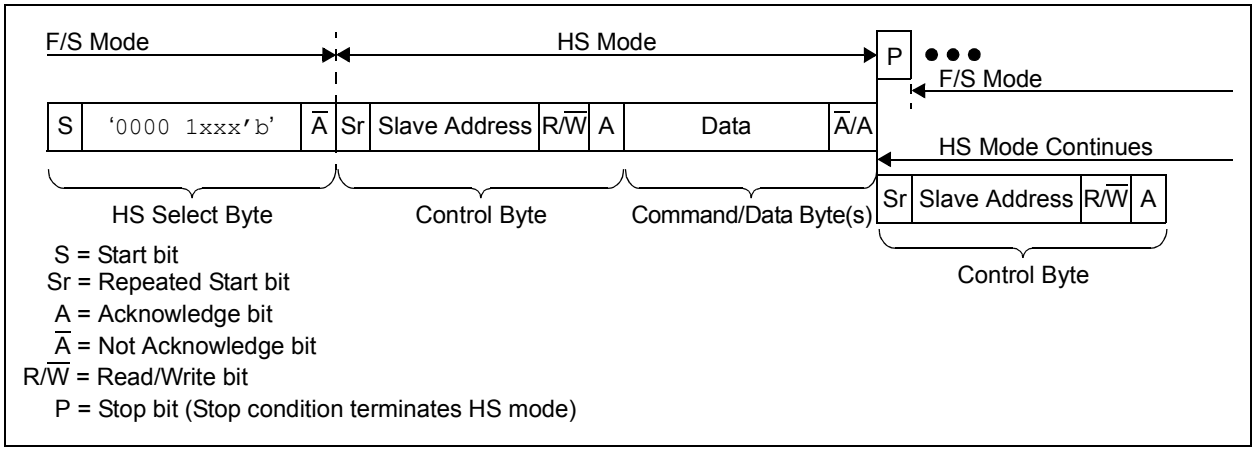



***FIGURE 6-3:*** *HS Mode Sequence.*

**NOTES:**


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## 7.0 DEVICE COMMANDS

The $I^2C$ protocol does not specify how commands are formatted, so this section specifies the MCP47CXBXX device's $I^2C$ command formats and operation.

The commands can be grouped into the following categories:

- Write Commands (C1:C0 = 00)
- Read Commands (C1:C0 = 11)
- General Call Commands

The supported commands are shown in Table 7-1. These commands allow both single data or continuous data operation. Continuous data operation means that the $I^2C$ Master does not generate a Stop bit but repeats the required data/clocks. This allows faster updates since the overhead of the $I^2C$ control byte is removed. Table 7-1 also shows the required number of bit clocks for each command's different mode of operation.

### 7.1 Write Commands

Write commands are used to transfer data to the desired memory location (from the Host controller). The modes are Single or Continuous. The Continuous mode format allows the fastest data update rate for the device's memory locations.

See **Section 7.5 "Write Command"** for a full description of the write commands.

| **Note:** | The 8-bit data devices use the same format as 10-bit and 12-bit devices. This allows code migration compatibility at the cost of nine extra clock cycles per data byte transferred. |
|---|---|

### 7.2 Read Commands

Read commands are used to transfer data from the desired memory location to the Host controller. The read command format writes two bytes (Control byte (R/$\overline{W}$ bit) = 0) and the read command byte (desired memory address and the read command). Then, a Restart condition is followed by a second control byte, but this control byte indicates an $I^2C$ read operation (R/$\overline{W}$ bit = 1). The Master will then supply 16 clocks so the specified address data are transfered. See **Section 7.6 "Read Command"** for full a description of the read commands.

**TABLE 7-1: DEVICE COMMANDS – NUMBER OF CLOCKS**

| Command | | | | # of Bit Clocks(1) | Data Update Rate (8-bit/10-bit/12-bit) (Data Words/Second) | | | Comments |
|---|---|---|---|---|---|---|---|---|
| Operation | Code | | Mode | | 100 kHz | 400 kHz | 3.4 MHz (3) | |
| | C1 | C0 | | | | | | |
| Write Command(4) | 0 | 0 | Single | 38 | 2,632 | 10,526 | 89,474 | |
| | 0 | 0 | Continuous | 27n + 11 | 3,559 | 14,235 | 120,996 | For ten data words |
| Read Command | 1 | 1 | Random | 48 | 2,083 | 8,333 | 70,833 | |
| | 1 | 1 | Continuous | 18n + 11 | 4,762 | 19,048 | 161,905 | For ten data words |
| | 1 | 1 | Last Address | 29 | 3,448 | 13,793 | 117,241 | |
| General Call Reset Command | — | — | Single | 20 | 5,000 | 20,000 | 170,000 | **Note 2** |
| General Call Wake-up Command | — | — | Single | 20 | 5,000 | 20,000 | 170,000 | **Note 2** |

**Note 1:** "n" indicates the number of times the command operation is to be repeated.

**2:** Determined by general call command byte after the $I^2C$ general call address.

**3:** There is a minimal overhead to enter into 3.4 MHz mode.

**4:** This command can be at either normal or high voltage. A high-voltage command requires the HVC pin to be at $V_{IHH}$, for the entire command, until the completion of the MTP cycle.

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## 7.3 General Call Commands

The general call commands utilize the I²C specification reserved general call command address and command codes. The General Call Reset command format is specified by the *"NXP I²C Specification"*. The general call wake-up command is a Microchip-defined format.

I²C devices Acknowledge the general call address command (0x00 in the first byte). The meaning of the general call address is always specified in the second byte. The I²C specification does not allow '00000000' (00h) in the second byte. Also, the '00000100' and '00000110' functionality is defined by the *"NXP I²C Specification"*. Lastly, a data byte with a '1' in the LSb indicates a "Hardware General Call".

Please refer to the *"NXP I²C Specification"* for more details on the general call specifications.

The MCP47CXBXX devices support the following I²C general calls:

- General Call Reset
- General Call Wake-up

See **Section 7.7.1 "General Call Reset"** for a full description of the General Call Reset command and the general call wake-up command.

## 7.4 Aborting a Transmission

A Restart or Stop condition in an expected data bit position will abort the current command sequence, and if the command is a write, that data word will not be written to the MCP47CXBXX. Also, the I²C state machine will be reset.

## 7.5 Write Command

The write command can be issued to both the volatile and nonvolatile memory locations. Write commands can also be structured as either single or continuous. The continuous format allows the fastest data update rate for the device's memory locations.

The format of the command is shown in Figure 7-1. The MCP47CXBXX generates the A/$\overline{A}$ bits. The format of the command is shown in Figure 7-1 (single) and Figure 7-3 (continuous); for example, ACK/NACK behavior (see Figure 7-2).

A write command to a volatile memory location changes that location after a properly formatted write command and the rising edge of the D00 bit (last data bit) clock has been detected.

A write command to a nonvolatile memory location will only start a write cycle after a properly formatted write command has been received and the Stop condition has occurred.

| | |
|---|---|
| **Note 1:** | Writes to volatile memory locations will be dependent on the state of their respective WiperLock Technology bits. |
| **2:** | During device communication, if the device address/command combination is invalid or an unimplemented device address is specified, then the MCP47CXBXX will NACK that byte. To reset the I²C state machine, the I²C communication must detect a Start bit. |
| **3:** | Writes to volatile memory locations will be dependent on the state of their respective WiperLock Technology bits. |

### 7.5.1 SINGLE WRITE TO VOLATILE MEMORY

For volatile memory locations, data are written to the MCP47CXBXX after every data word transfer (16 bits) during the rising edge of the last data bit. If a Stop or Restart condition is generated during a data transfer (before the last data bit is received), the data will not be written to the MCP47CXBXX. After the A bit, the Master can initiate the next sequence with a Stop or Restart condition. (See Figure 7-1 for the write sequence.)

| | |
|---|---|
| **Note:** | Writes to a Volatile DAC register will not transfer to the output register until the $\overline{LAT}$ (HVC) pin is transitioned to the $V_{IL}$ voltage. |

### 7.5.2 SINGLE WRITE TO NONVOLATILE MEMORY (HVC PIN = $V_{IL}$ OR $V_{IH}$)

In normal user mode, the MTP memory address cannot be written. Writing to the MTP address space, while the HVC pin is not at $V_{IHH}$, will not have any effect; the command is Acknowledged but the memory is not modified.


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### 7.5.3 SINGLE WRITE TO NONVOLATILE MEMORY (HVC PIN = $V_{IHH}$)

| | |
|---|---|
| **Note:** | Writes to MTP memory require the HVC pin at 7.5V. This is not the normal operating conditions of the device; it is designed for factory programming of configuration parameters. |

The sequence to write to a single nonvolatile memory location is the same as a single write to volatile memory, with the exception that the MTP Write Cycle ($t_{WC}$) is started after a properly formatted command, including the Stop bit, is received. After the Stop condition occurs, the serial interface may immediately be re-enabled by initiating a Start condition.

The HVC pin must be at $V_{IHH}$ until the completion of the MTP Write Cycle ($t_{WC}$).

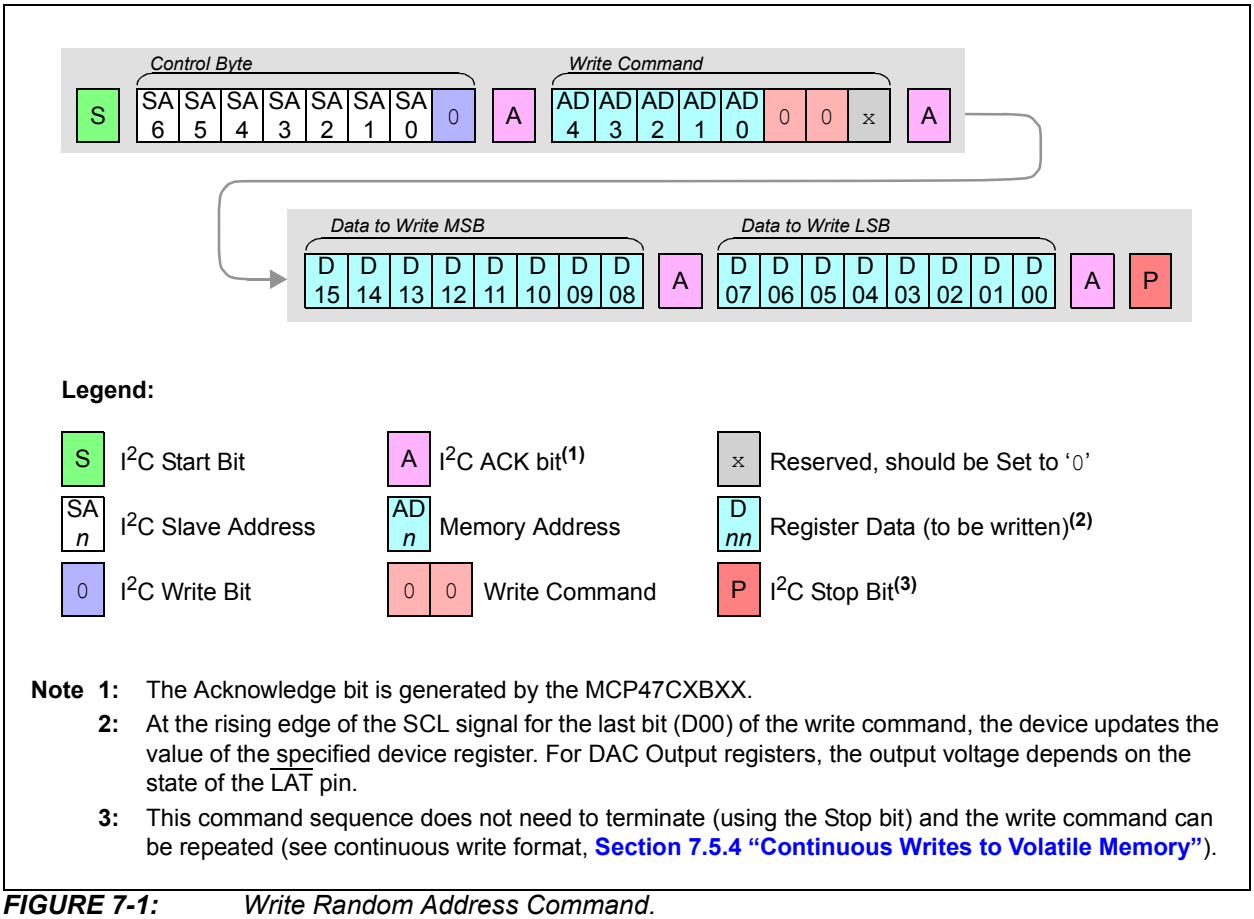
During an MTP write cycle, access to the volatile memory is allowed when using the appropriate command sequence. Commands that address nonvolatile memory are ignored until the MTP Write Cycle ($t_{WC}$) completes. This allows the Host controller to operate on the Volatile DAC registers.

Once a write command to a nonvolatile memory location has been received, no other commands should be received before the Stop condition occurs.

| | |
|---|---|
| **Note:** | If a Stop condition does not occur, then the NV Write does not occur and all following command(s) will have an error condition ($\overline{A}$). A Start bit is required to reset the command state machine. |

Writes to a NV memory location while an MTP write cycle is occurring will force an error condition ($\overline{A}$). A Start bit is required to reset the command state machine.

Figure 7-1 shows the waveform for a single write.




**Note 1:** The Acknowledge bit is generated by the MCP47CXBXX.

**2:** At the rising edge of the SCL signal for the last bit (D00) of the write command, the device updates the value of the specified device register. For DAC Output registers, the output voltage depends on the state of the $\overline{LAT}$ pin.

**3:** This command sequence does not need to terminate (using the Stop bit) and the write command can be repeated (see continuous write format, **Section 7.5.4 "Continuous Writes to Volatile Memory"**).

***FIGURE 7-1:*** *Write Random Address Command.*

### 7.5.4 CONTINUOUS WRITES TO VOLATILE MEMORY

A Continuous Write mode of operation is possible when writing to the device's Volatile Memory registers (see Table 7-2). This Continuous Write mode allows writes without a Stop or Restart condition, or repeated transmissions of the $I^2C$ control byte. Figure 7-3 shows the sequence for three continuous writes. The writes do not need to be to the same volatile memory address. The sequence ends with the Master sending a Stop or Restart condition.

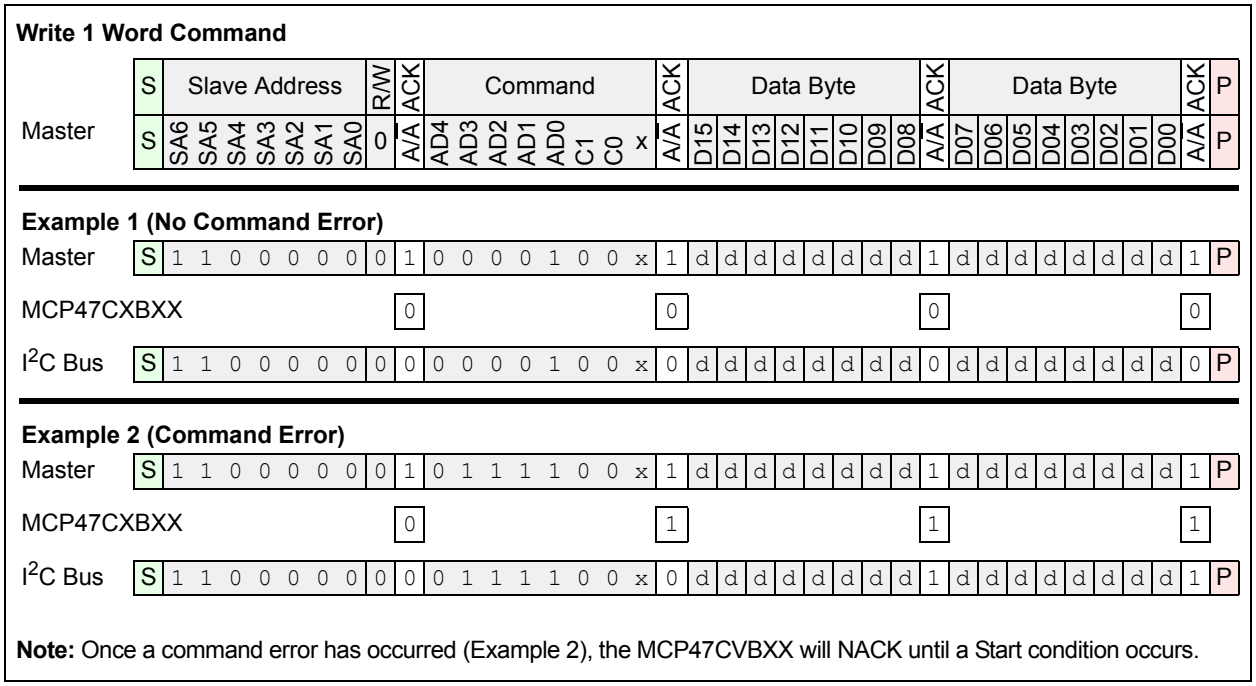
**TABLE 7-2: VOLATILE MEMORY ADDRESSES**

| Address | Single Channel | Dual Channel |
|---|---|---|
| 00h | Yes | Yes |
| 01h | No | Yes |
| 08h | Yes | Yes |
| 09h | Yes | Yes |
| 0Ah | Yes | Yes |

### 7.5.5 CONTINUOUS WRITES TO NONVOLATILE MEMORY

If a continuous write is attempted on nonvolatile memory, the missing Stop condition will cause the command to be an error condition ($\overline{A}$) on all following bytes. A Start bit is required to reset the command state machine.

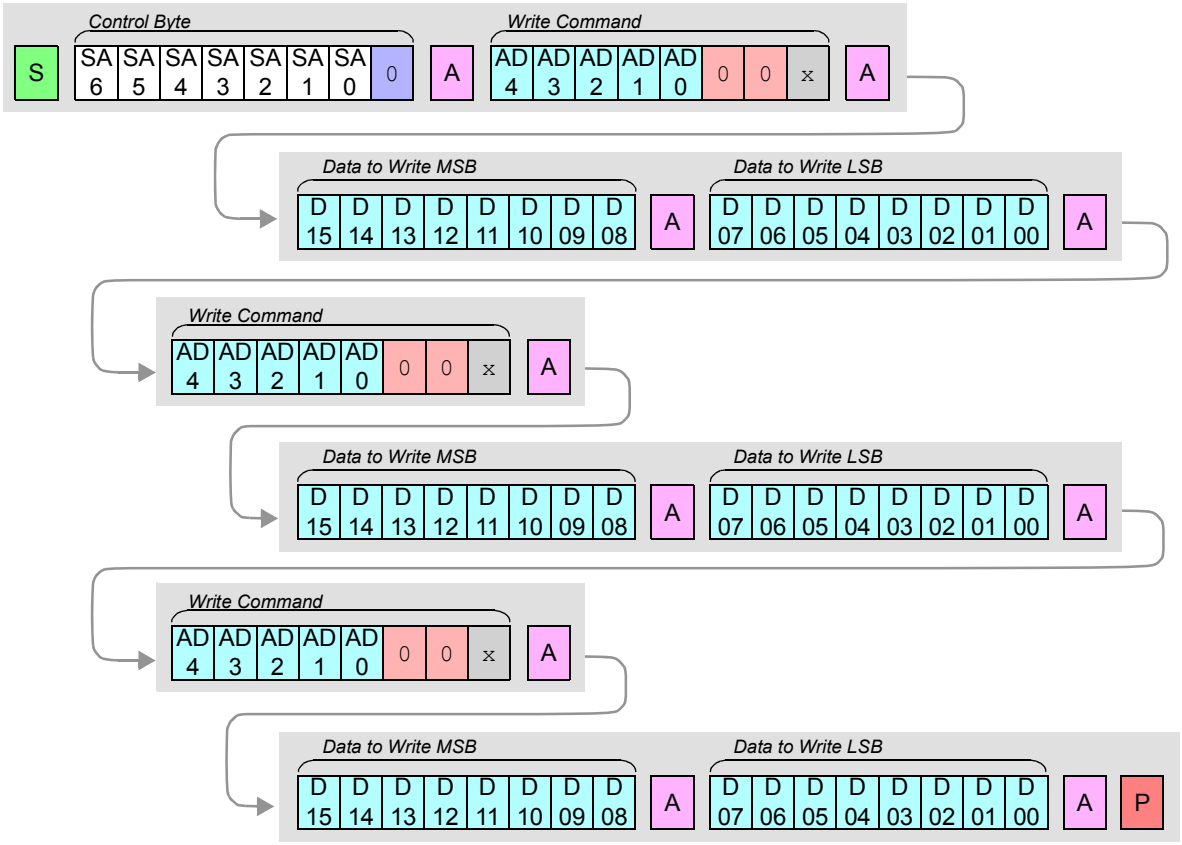
**Note:** All bytes are ignored and not transferred to memory.




**Note:** Once a command error has occurred (Example 2), the MCP47CVBXX will NACK until a Start condition occurs.

***FIGURE 7-2:*** *$I^2C$ ACK/NACK Behavior (Write Command Example).*


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**Legend:**

| | | | | | |
|---|---|---|---|---|---|
| S | $I^2C$ Start Bit | A | $I^2C$ ACK Bit (1) | x | Reserved, should be Set to '0' |
| SA *n* | $I^2C$ Slave Address | AD *n* | Memory Address | D *nn* | Register Data (to be written)(2) |
| 0 | $I^2C$ Write Bit | 0 0 | Write Command | P | $I^2C$ Stop Bit(3) |

**Note 1:** The Acknowledge bit is generated by the MCP47CXBXX.

**2:** At the falling edge of the SCL pin for the write command ACK bit, the MCP47CXBXX device updates the value of the specified device register.

**3:** This command sequence does not need to terminate (using the Stop bit) and the write command can be repeated (see continuous write format, **Section 7.5.4 "Continuous Writes to Volatile Memory"**).

**4:** Only functions when writing to Volatile registers (AD4:AD0 = 00h through 0Ah).

***FIGURE 7-3:*** *Continuous Write Commands (Volatile Memory Only).*

## 7.6 Read Command

Read commands are used to transfer data from the specified memory location to the Host controller.

The read command can be issued to both the volatile and nonvolatile memory locations. During an MTP memory write cycle, the read command can only read the volatile memory locations. By reading the Status Register (0Ah), the Host controller can determine when the Write Cycle ($t_{WC}$) has been completed (via the state of the MTPMA bit).

The read command formats include:

- Single Read
  - Single Memory Address
  - Last Memory Address Accessed
- Continuous Reads

The MCP47CXBXX retains the last received device memory address. This means the MCP47CXBXX does not corrupt the device memory address after Repeated Start or Stop conditions.

| | |
|---|---|
| **Note 1:** | During device communication, if the device address/command combination is invalid or an unimplemented address is specified, the MCP47CXBXX will NACK that byte. To reset the $I^2C$ state machine, the $I^2C$ communication must detect a Start bit. |
| **2:** | If the $\overline{LAT}$ pin is high ($V_{IH}$), reads of the Volatile DAC register return the current output value, not the internal register value. |
| **3:** | The read commands operate the same regardless of the state of the High-Voltage Command (HVC) signal. |

### 7.6.1 SINGLE READ

The read command format writes two bytes, the control byte and the read command byte (desired memory address and the read command), and then has a Restart condition. Then, a second control byte is transmitted, but this control byte indicates an $I^2C$ read operation (R/$\overline{W}$ bit = 1).

#### 7.6.1.1 Single Memory Address

Figure 7-4 shows the sequence for reading a specified memory address.

#### 7.6.1.2 Last Memory Address Accessed

This is useful for checking the status of the MTPMA bit or when writes to other $I^2C$ devices on the bus must occur between these memory reads. The Master must send a Stop or Restart condition after the data word is sent from the Slave. Figure 7-5 shows the waveforms for a single read of the last memory location accessed.

### 7.6.2 CONTINUOUS READS

Continuous reads allow the device's memory to be read quickly and are valid for all memory locations.

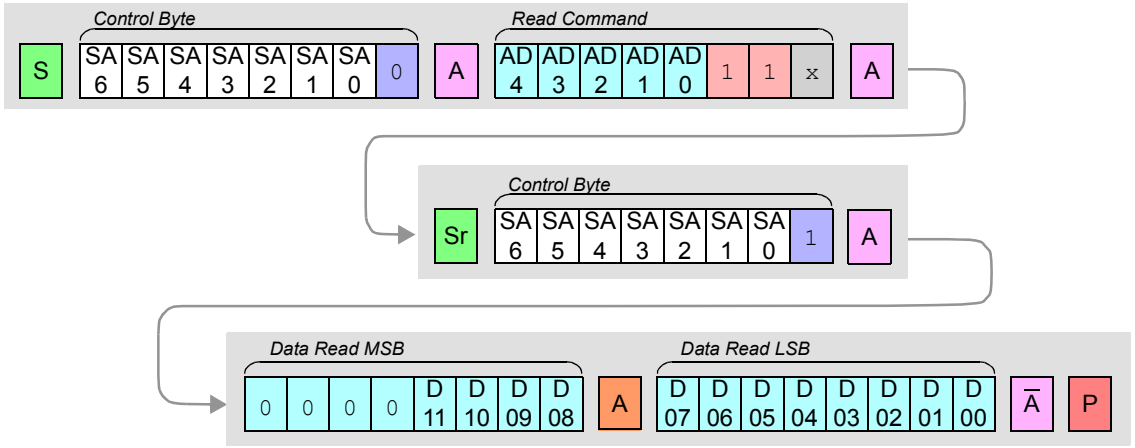
Figure 7-7 shows the sequence for three continuous reads.

For continuous reads, instead of transmitting a Stop or Restart condition after the data transfer, the Master continually reads the data byte. The sequence ends with the Master Not Acknowledging and then sending a Stop or Restart.

### 7.6.3 IGNORING AN $I^2C$ TRANSMISSION AND "FALLING OFF" THE BUS

The MCP47CXBXX expects to receive complete, valid $I^2C$ commands and will assume any command not defined as a valid command is due to a bus corruption, thus entering a passive high condition on the SDA signal. All signals will be ignored until the next valid Start condition and control byte are received.


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**Legend:**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| S | I²C Start Bit | AD *n* | Memory Address(5) | 1 | I²C Read Bit | P | I²C Stop Bit(3) |
| SA *n* | I²C Slave Address | 1 1 | Read Command | D *nn* | Data (read from memory) | | |
| 0 | I²C Write Bit | x | Reserved, Set to '0' | A | I²C ACK Bit(2) | | |
| A | I²C ACK Bit(1) | Sr | I²C Start Bit, Repeated | Ā | I²C NACK Bit(4) | | |

**Note 1:** The Master device is responsible for the A/Ā signal. If an Ā signal occurs, the MCP47CXBXX will abort this transfer and release the bus.

**2:** This Acknowledge bit is generated by the Master device.

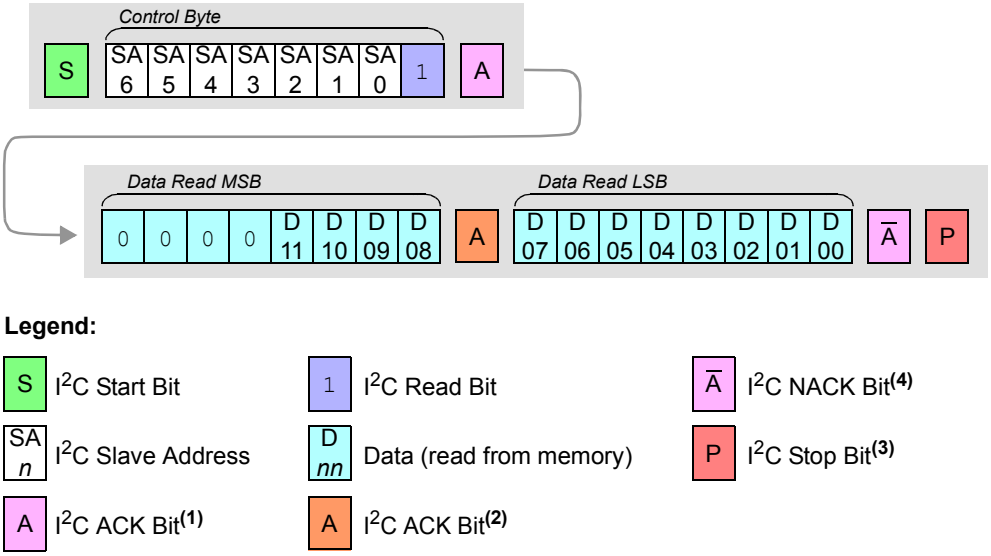
**3:** This command sequence does not need to terminate (using the Stop bit) and the read command can be repeated (see **Section 7.6.2 "Continuous Reads"**).

**4:** The Master device will Not Acknowledge and the MCP47CXBXX will release the bus so the Master device can generate a Stop or Repeated Start condition.

**5:** The MCP47CXBXX retains the last received "device memory address".

**6:** The non-data bits of the Read Data Word will be output as '0's:
for 12-bit devices, bits D15:D12 are '0's
for 10-bit devices, bits D15:D10 are '0's
for 8-bit devices, bits D15:D08 are '0's

***FIGURE 7-4:*** *Read Command – Single Memory Address.*




**Note 1:** The Master device is responsible for the A/$\overline{A}$ signal. If an $\overline{A}$ signal occurs, the MCP47CXBXX will abort this transfer and release the bus.

**2:** This Acknowledge bit is generated by the Master device.

**3:** This command sequence does not need to terminate (using the Stop bit) and the read command can be repeated (see **Section 7.6.2 "Continuous Reads"**).

**4:** The Master device will Not Acknowledge and the MCP47CXBXX will release the bus so the Master device can generate a Stop or Repeated Start condition.

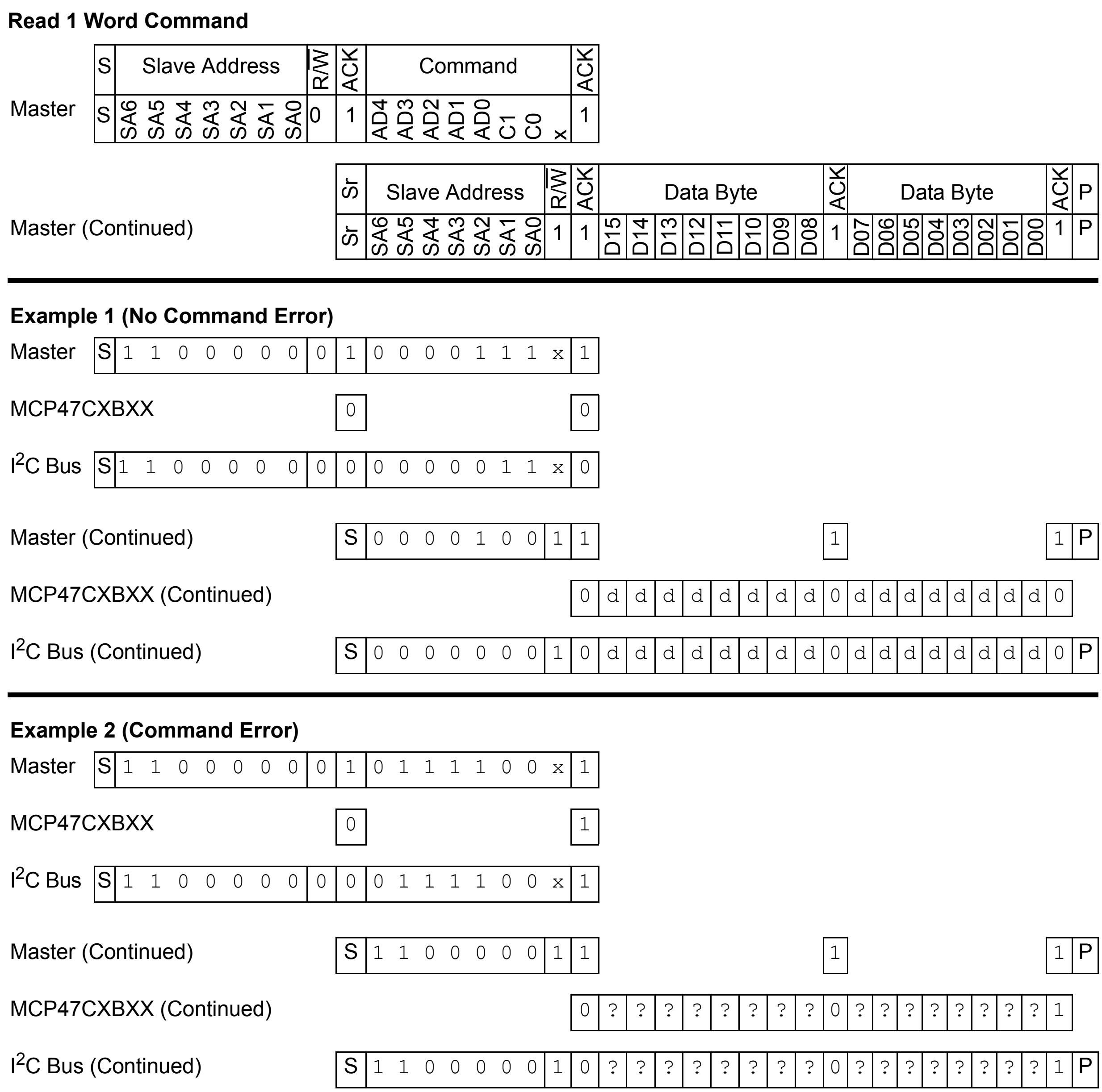
**5:** The MCP47CXBXX retains the last received "Device Memory Address".

**6:** The non-data bits of the Read Data Word will be output as '0's:
for 12-bit devices, bits D15:D12 are '0's
for 10-bit devices, bits D15:D10 are '0's
for 8-bit devices, bits D15:D08 are '0's

**7:** If the last device address written (via the read or write command) is invalid for a read, then the read last memory address command will NACK due to the invalid device memory address.

***FIGURE 7-5:*** *Read Command – Last Memory Address Accessed.*

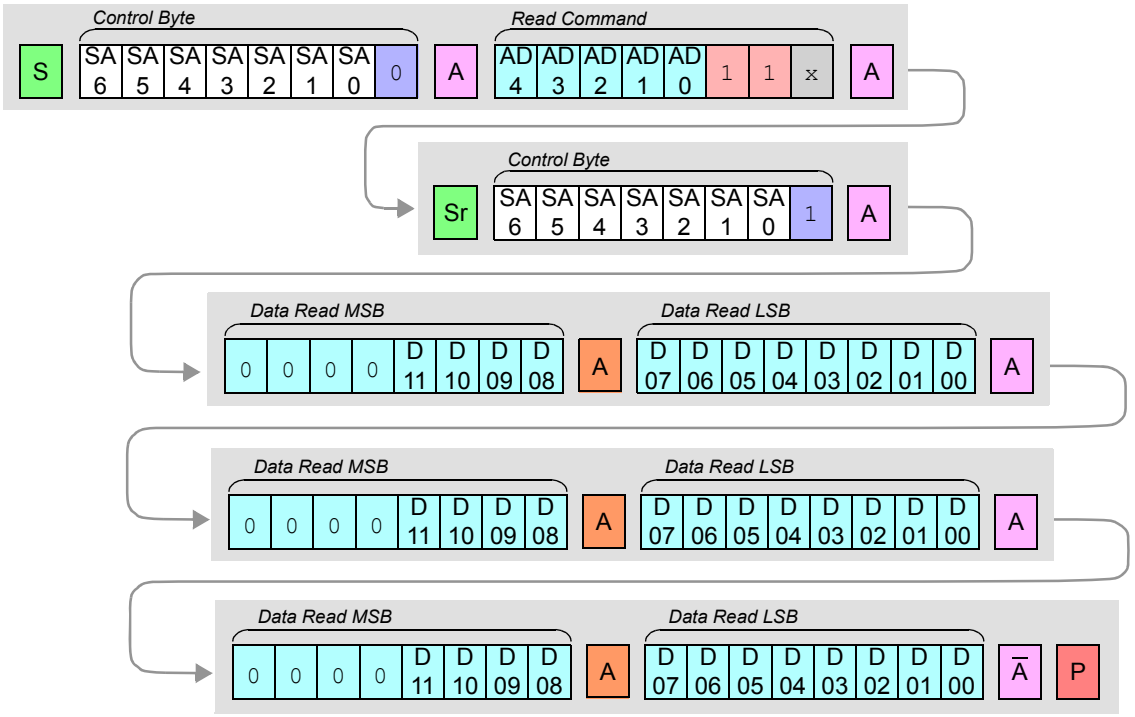

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**Note 1:** Once a command error has occurred (Example 2), the MCP47CXBXX will NACK until a Start condition occurs.

**2:** For command error case (Example 2), the data read is from the register of the last valid address loaded into the device.

***FIGURE 7-6:*** *$I^2C$ ACK/NACK Behavior (Read Command Example).*




**Legend:**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| S | $I^2C$ Start Bit | AD *n* | Memory Address(5) | 1 | $I^2C$ Read Bit | P | $I^2C$ Stop Bit(3) |
| SA *n* | $I^2C$ Slave Address | 1 1 | Read Command | D *nn* | Data (read from memory) | | |
| 0 | $I^2C$ Write Bit | x | Reserved, Set to '0' | A | $I^2C$ ACK Bit(2) | | |
| A | $I^2C$ ACK Bit(1) | Sr | $I^2C$ Start Bit, Repeated | Ā | $I^2C$ NACK Bit(4) | | |

**Note 1:** The Master device is responsible for the A/$\overline{A}$ signal. If an $\overline{A}$ signal occurs, the MCP47CXBXX will abort this transfer and release the bus.

**2:** This Acknowledge bit is generated by the Master device.

**3:** This command sequence does not need to terminate (using the Stop bit) and the read command can be repeated (see **Section 7.6.2 "Continuous Reads"**).

**4:** The Master device will Not Acknowledge and the MCP47CXBXX will release the bus so the Master device can generate a Stop or Repeated Start condition.

**5:** The MCP47CXBXX retains the last received "Device Memory Address".

**6:** The non-data bits of the Read Data Word will be output as '0's:
for 12-bit devices, bits D15:D12 are '0's
for 10-bit devices, bits D15:D10 are '0's
for 8-bit devices, bits D15:D08 are '0's

***FIGURE 7-7:*** *Continuous Read Command of Specified Address.*


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## 7.7 General Call Commands

The MCP47CXBXX Acknowledges the general call address command (00h in the first byte). General call commands can be used to communicate to all devices on the I²C bus (at the same time) that understand the general call command. The meaning of the general call address is always specified in the second byte (see Figure 7-8).

If the second byte has a '1' in the LSb, the specification intends this to indicate a "Hardware General Call". The MCP47CXBXX will ignore this byte and all following bytes (and $\overline{A}$), until a Stop bit (P) is encountered.

The MCP47CXBXX devices support the following I²C general call commands:

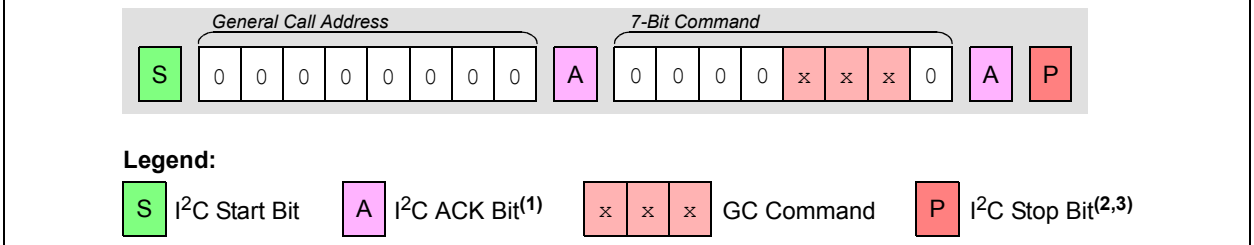
- General Call Reset (06h)
- General Call Wake-up (0Ah)

The General Call Reset command format is specified by the I²C Specification. The general call wake-up command is a Microchip-defined format. The general call wake-up command will have all devices wake-up (that is, exit the Power-Down mode).

The other two I²C specification command codes (04h and 00h) are not supported, and therefore, those commands are Not Acknowledged.

If these 7-bit commands conflict with other I²C devices on the bus, the user will need two I²C buses to ensure that the devices are on the correct bus for their desired application functionality.

**Note:** Refer to the *"NXP Specification"*, #UM10204, Rev. 03 19, June 2007 document for more details on the general call specifications. The I²C specification does not allow '00000000' (00h) in the second byte.




**Note 1:** The Acknowledge bit is generated by the MCP47CXBXX.

**2:** This command sequence does not need to terminate (using the Stop bit) and the general call command can be repeated or another general call command can be sent. Only the first command will be accepted by the MCP47CXBXX.

***FIGURE 7-8:*** *General Call Formats.*

### 7.7.1 GENERAL CALL RESET

The I²C General Call Reset command forces a reset event. This is similar to the Power-On Reset, except that the reset delay timer is not started. This command allows multiple devices to be reset synchronously.

The device performs General Call Reset if the second byte is '00000110' (06h). At the acknowledgment of this byte, the device will perform the following tasks:

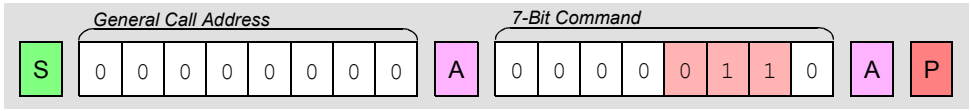
- Internal reset similar to a POR. The contents of the MTP are loaded into the DAC registers
- Analog output ($V_{OUT}$) is available after the POR sequence has been completed.

### 7.7.2 GENERAL CALL WAKE-UP

The I²C General Call Wake-Up command forces the device to exit from its Power-Down state (forces the PDxB:PDxA bits to '00'). This command allows multiple MCP47CXBXX devices to wake up synchronously.

The device performs General Call Wake-Up if the second byte (after the General Call Address) is '00001010' (0Ah). At the acknowledgment of this byte, the device will perform the following task:

- The device's volatile power-down bits (PDxB:PDxA) are forced to '00'.




**Legend:**

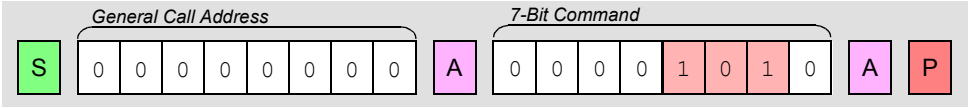
S I²C Start Bit | A I²C ACK Bit(1) | 0 1 1 Reset Command | P I²C Stop Bit(2,3)

**Note 1:** The Acknowledge bit is generated by the MCP47CXBXX.

**2:** At the falling edge of the SCL pin for the General Call Reset command ACK bit, the MCP47CXBXX device is reset.

**3:** This command sequence does not need to terminate (using the Stop bit) and the General Call Reset command can be repeated or the general call wake-up command can be sent. Only the first command will be accepted by the MCP47CXBXX.

***FIGURE 7-9:*** *General Call Reset Command.*




**Legend:**

S I²C Start Bit | A I²C ACK Bit(1) | 1 0 1 Reset Command | P I²C Stop Bit(3)

**Note 1:** The Acknowledge bit is generated by the MCP47CXBXX.

**2:** At the rising edge of the last data bit for the general call wake-up command, the volatile Power-Down bits (PDxB:PDxA) are forced to '00'.

**3:** This command sequence does not need to terminate (using the Stop bit) and the general call wake-up command can be repeated or the General Call Reset command can be sent.

***FIGURE 7-10:*** *General Call Wake-up Command.*


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## 8.0 TYPICAL APPLICATIONS

The MCP47CXBXX devices are general purpose, single/dual channel voltage output DACs for various applications where a precision operation with low power is needed.

Applications generally suited for the devices are:

- Set Point or Offset Trimming
- Sensor Calibration
- Portable Instrumentation (Battery-Powered)
- Motor Control

### 8.1 Connecting to the I²C Bus Using Pull-up Resistors

The SCL and SDA pins of the MCP47CXBXX devices are open-drain configurations. These pins require a pull-up resistor, as shown in Figure 8-2.

The pull-up resistor values ($R_1$ and $R_2$) for SCL and SDA pins depend on the operating speed (standard, fast and high speed) and loading capacitance of the I²C bus line. A higher value of the pull-up resistor consumes less power, but increases the signal transition time (higher RC time constant) on the bus line; therefore, it can limit the bus operating speed. The lower resistor value, on the other hand, consumes higher power, but allows higher operating speed. If the bus line has higher capacitance due to long metal traces or multiple device connections to the bus line, a smaller pull-up resistor is needed to compensate for the long RC time constant. The pull-up resistor is typically chosen between 1 kΩ and 10 kΩ ranges for Standard and Fast modes, and less than 1 kΩ for High-Speed mode.

#### 8.1.1 DEVICE CONNECTION TEST

The user can test the presence of the device on the I²C bus line using a simple I²C command. This test can be achieved by checking an Acknowledge response from the device after sending a read or write command. Figure 8-1 shows an example with a read command. The steps are:

1. Set the R/$\overline{W}$ bit "High" in the device's address byte.
2. Check the ACK bit of the address byte.
   If the device Acknowledges (ACK = 0) the command, then the device is connected; otherwise, it is not connected.
3. Send Stop bit.

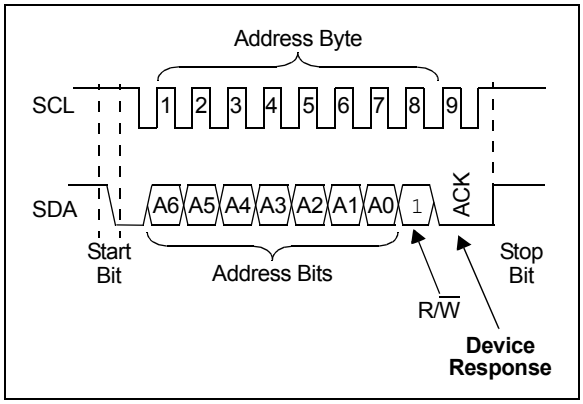
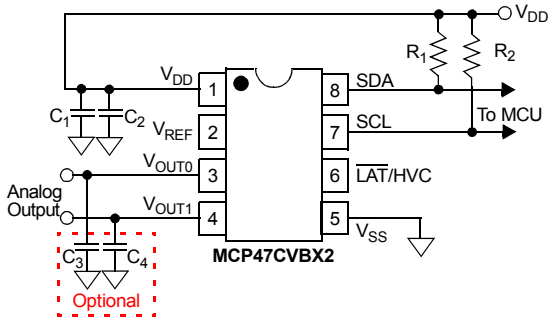



***FIGURE 8-1:*** *I²C Bus Connection Test.*

## 8.2 Power Supply Considerations

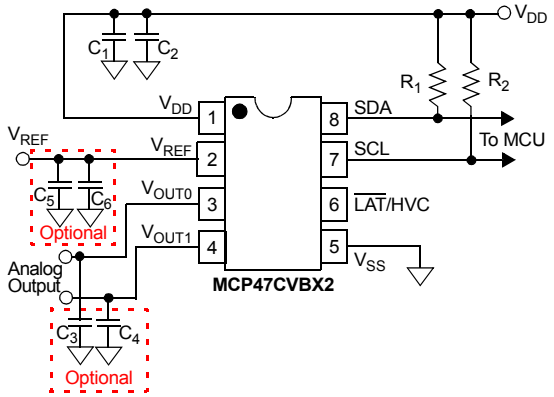
The power source should be as clean as possible. The power supply to the device is also used for the DAC voltage reference internally if the internal $V_{DD}$ is selected as the resistor ladder's reference voltage (VRxB:VRxA = 00).

Any noise induced on the $V_{DD}$ line can affect the DAC performance. Typical applications will require a bypass capacitor in order to filter out high-frequency noise on the $V_{DD}$ line. The noise can be induced onto the power supply's traces or as a result of changes on the DAC output. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 8-2 shows an example of using two bypass capacitors (a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor) in parallel on the $V_{DD}$ line. These capacitors should be placed as close to the $V_{DD}$ pin as possible (within 4 mm). If the application circuit has separate digital and analog power supplies, the $V_{DD}$ and $V_{SS}$ pins of the device should reside on the analog plane.




(a) Circuit when $V_{DD}$ is selected as reference.

**Note:** $V_{DD}$ is connected to the reference circuit internally.




(b) Circuit when external reference is used.

$R_1$ and $R_2$ are $I^2C$ pull-up resistors:

$R_1$ and $R_2$:

5 kΩ-10 kΩ for $f_{SCL}$ = 100 kHz to 400 kHz

~700Ω for $f_{SCL}$ = 3.4 MHz

$C_1$: 0.1 µF capacitor = Ceramic

$C_2$: 10 µF capacitor = Tantalum

$C_3$: ~ 0.1 µF = Optional to reduce noise in $V_{OUT}$ pin

$C_4$: 0.1 µF capacitor = Ceramic

$C_5$: 10 µF capacitor = Tantalum

$C_6$: 0.1 µF capacitor = Ceramic

***FIGURE 8-2:*** *Example Circuit.*


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## 8.3 Application Examples

The MCP47CXBXX devices are rail-to-rail output DACs designed to operate with a $V_{DD}$ range of 2.7V to 5.5V. The internal output amplifier is robust enough to drive common, small signal loads directly, thus eliminating the cost and size of the external buffers for most applications. The user can use the gain of 1 or 2 of the output op amp by setting the Configuration register bits. The internal $V_{DD}$ or an external reference can be used. There are various user options and easy-to-use features that make the devices suitable for various modern DAC applications.

Application examples include:

- Decreasing Output Step-Size
- Building a “Window” DAC
- Bipolar Operation
- Selectable Gain and Offset Bipolar Voltage Output
- Designing a Double Precision DAC
- Building Programmable Current Source
- Serial Interface Communication Times
- Software $I^2C$ Interface Reset Sequence
- Power Supply Considerations
- Layout Considerations

### 8.3.1 DC SET POINT OR CALIBRATION

A common application for the devices is a digitally controlled set point and/or calibration of variable parameters, such as sensor offset or slope. For example, the MCP47CVB2X provides 4096 output steps. If the voltage reference is 4.096V (where Gx = 0), the LSb size is 1 mV. If a smaller output step-size is desired, a lower external voltage reference is needed.

#### 8.3.1.1 Decreasing Output Step-Size

If the application is calibrating the bias voltage of a diode or transistor, a bias voltage range of 0.8V may be desired, with about 200 µV resolution per step. Two common methods to achieve small step-size are to use a lower $V_{REF}$ pin voltage or a voltage divider on the DAC’s output.

Using an external Voltage Reference ($V_{REF}$) is an option if the external reference is available with the desired output voltage range. However, when using a low-voltage reference voltage, occasionally the noise floor causes an SNR error that is intolerable. Using a voltage divider method is another option, and provides some advantages when external voltage reference needs to be very low, or when the desired output voltage is not available. In this case, a larger value reference voltage is used, while two resistors scale the output range down to the precise desired level.

Figure 8-3 illustrates this concept. A bypass capacitor on the output of the voltage divider plays a critical function in attenuating the output noise of the DAC and the induced noise from the environment.

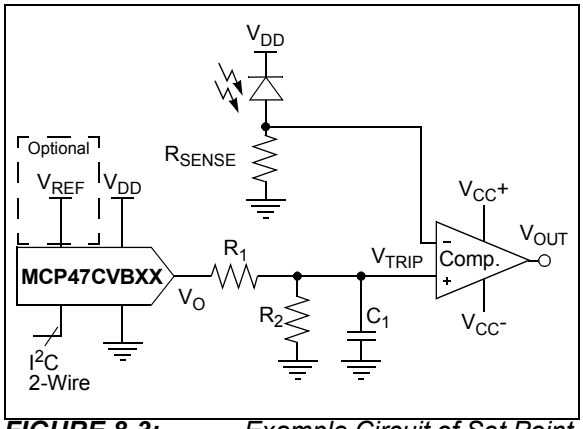



***FIGURE 8-3:*** *Example Circuit of Set Point or Threshold Calibration.*

**EQUATION 8-1: $V_{OUT}$ AND $V_{TRIP}$ CALCULATIONS**

$$V_{OUT} = V_{REF} \bullet G \bullet \frac{DAC\ Register\ Value}{2^N}$$

$$V_{trip} = V_{OUT}\left(\frac{R_2}{R_1 + R_2}\right)$$

### 8.3.1.2 Building a “Window” DAC

When calibrating a set point or threshold of a sensor, typically only a small portion of the DAC output range is utilized. If the LSb size is adequate enough to meet the application’s accuracy needs, the unused range is sacrificed without consequences. If greater accuracy is needed, then the output range will need to be reduced to increase the resolution around the desired threshold.

If the threshold is not near $V_{REF}$, 2 • $V_{REF}$ or $V_{SS}$, then creating a “window” around the threshold has several advantages. One simple method to create this “window” is to use a voltage divider network with a pull-up and pull-down resistor. Figure 8-4 and Figure 8-6 illustrate this concept.

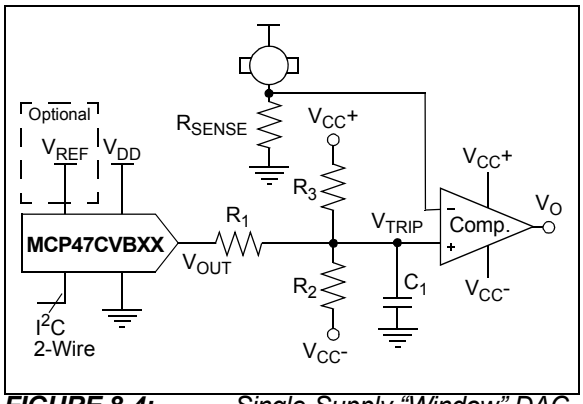



***FIGURE 8-4:*** *Single-Supply “Window” DAC.*

**EQUATION 8-2: $V_{OUT}$ AND $V_{TRIP}$ CALCULATIONS**

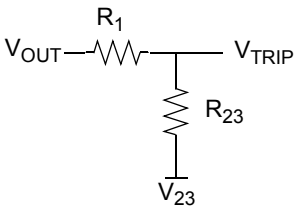
$$V_{OUT} = V_{REF} \bullet G \bullet \frac{DAC\ Register\ Value}{2^N}$$

$$V_{TRIP} = \frac{V_{OUT}R_{23} + V_{23}R_1}{R_1 + R_{23}}$$

Thevenin Equivalent:

$$R_{23} = \frac{R_2R_3}{R_2 + R_3}$$

$$V_{23} = \frac{(V_{CC+}R_2) + (V_{CC-}R_3)}{R_2 + R_3}$$




## 8.4 Bipolar Operation

Bipolar operation is achievable by utilizing an external operational amplifier. This configuration is desirable due to the wide variety and availability of op amps. This allows a general purpose DAC, with its cost and availability advantages, to meet almost any desired output voltage range, power and noise performance.

Figure 8-5 illustrates a simple bipolar voltage source configuration. $R_1$ and $R_2$ allow the gain to be selected, while $R_3$ and $R_4$ shift the DAC's output to a selected offset. Note that R4 can be tied to $V_{DD}$ instead of $V_{SS}$ if a higher offset is desired.

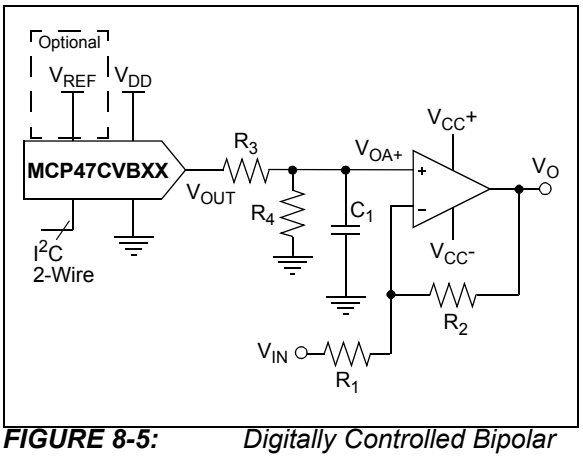



***FIGURE 8-5:*** *Digitally Controlled Bipolar Voltage Source Example Circuit.*

**EQUATION 8-3: $V_{OUT}$, $V_{OA}$+ AND $V_O$ CALCULATIONS**

$$V_{OUT} = V_{REF} \bullet G \bullet \frac{DAC\ Register\ Value}{2^N}$$

$$V_{OA+} = \frac{V_{OUT} \bullet R_4}{R_3 + R_4}$$

$$V_O = V_{OA+} \bullet (1 + \frac{R_2}{R_1}) - V_{DD} \bullet (\frac{R_2}{R_1})$$


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## 8.5 Selectable Gain and Offset Bipolar Voltage Output

In some applications, precision digital control of the output range is desirable. Figure 8-6 illustrates how to use the DAC devices to achieve this in a bipolar or single-supply application.

This circuit is typically used for linearizing a sensor whose slope and offset varies.

The equation to design a bipolar "window" DAC would be utilized if $R_3$, $R_4$ and $R_5$ are populated.

### 8.5.1 BIPOLAR DAC EXAMPLE

An output step-size of 1 mV, with an output range of ±2.05V, is desired for a particular application.

**Step 1:** Calculate the range: +2.05V – (-2.05V) = 4.1V

**Step 2:** Calculate the resolution needed:

4.1V/1 mV = 4100

Since $2^{12}$ = 4096, 12-bit resolution is desired

**Step 3:** The amplifier gain ($R_2/R_1$), multiplied by full-scale $V_{OUT}$ (4.096V), must be equal to the desired minimum output to achieve bipolar operation. Since any gain can be realized by choosing resistor values ($R_1$ + $R_2$), the $V_{REF}$ value must be selected first. If a $V_{REF}$ of 4.096V is used, solve for the amplifier's gain by setting the DAC to 0, knowing that the output needs to be -2.05V.

The equation can be simplified to:

**EQUATION 8-4:**

$$\frac{-R_2}{R_1} = \frac{-2.05}{4.096V} \qquad \frac{R_2}{R_1} = \frac{1}{2}$$

If $R_1$ = 20 kΩ and $R_2$ = 10 kΩ, the gain will be 0.5.

**Step 4:** Next, solve for $R_3$ and $R_4$ by setting the DAC to 4096, knowing that the output needs to be +2.05V.

**EQUATION 8-5:**

$$\frac{R_4}{(R_3 + R_4)} = \frac{2.05V + (0.5 \cdot 4.096V)}{1.5 \cdot 4.096V} = \frac{2}{3}$$

If $R_4$ = 20 kΩ, then $R_3$ = 10 kΩ.

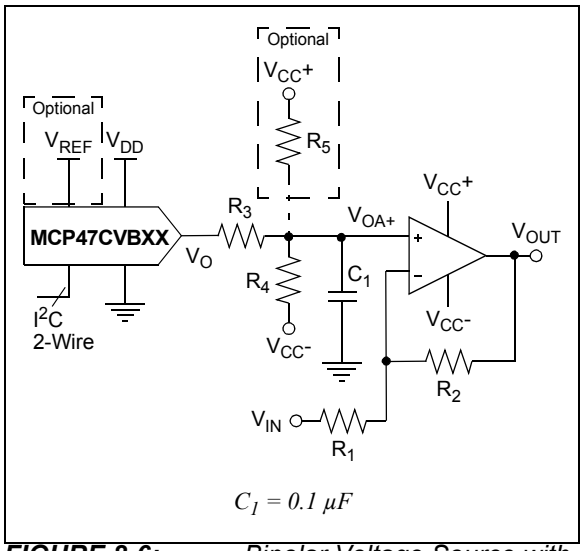



***FIGURE 8-6:*** *Bipolar Voltage Source with Selectable Gain and Offset.*

**EQUATION 8-6: $V_{OUT}$, $V_{OA}$+ AND $V_O$ CALCULATIONS**

$$V_{OUT} = V_{REF} \bullet G \bullet \frac{DAC\ Register\ Value}{2^N}$$

$$V_{OA+} = \frac{V_{OUT} \bullet R_4 + V_{CC-} \bullet R_5}{R_3 + R_4}$$

$$V_O = \underbrace{V_{OA+} \bullet \left(1 + \frac{R_2}{R_1}\right)}_{\text{Offset Adjust}} - \underbrace{V_{IN} \bullet \left(\frac{R_2}{R_1}\right)}_{\text{Gain Adjust}}$$

**EQUATION 8-7: BIPOLAR "WINDOW" DAC USING $R_4$ AND $R_5$**

Thevenin Equivalent

$$V_{45} = \frac{V_{CC+}R_4 + V_{CC-}R_5}{R_4 + R_5}$$

$$V_{IN+} = \frac{V_{OUT}R_{45} + V_{45}R_3}{R_3 + R_{45}}$$

$$R_{45} = \frac{R_4R_5}{R_4 + R_5}$$

$$V_O = \underbrace{V_{IN+}\left(1 + \frac{R_2}{R_1}\right)}_{\text{Offset Adjust}} \underbrace{- V_A\left(\frac{R_2}{R_1}\right)}_{\text{Gain Adjust}}$$

## 8.6 Designing a Double Precision DAC

Figure 8-7 shows an example design of a single-supply voltage output capable of up to 24-bit resolution. This requires two 12-bit DACs. This design is simply a voltage divider with a buffered output.

As an example, if a similar application to the one developed in **Section 8.5.1 "Bipolar DAC Example"** required a resolution of 1 µV instead of 1 mV, and a range of 0V to 4.1V, then 12-bit resolution would not be adequate.

**Step 1:** Calculate the resolution needed:

4.1V/1 µV = 4.1 x $10^6$
Since $2^{22}$ = 4.2 x $10^6$, a 22-bit resolution is desired. Since DNL = ±1.0 LSb, this design can be attempted with the 12-bit DAC.

**Step 2:** Since DAC1's $V_{OUT1}$ has a resolution of 1 mV, its output only needs to be "pulled" 1/1000 to meet the 1 µV target. Dividing $V_{OUT0}$ by 1000 would allow the application to compensate for DAC1's DNL error.

**Step 3:** If $R_2$ is 100Ω, then $R_1$ needs to be 100 kΩ.

**Step 4:** The resulting transfer function is shown in Equation 8-8.

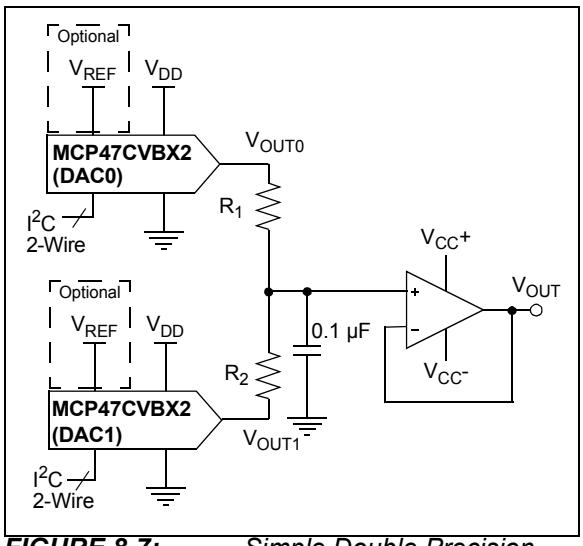



***FIGURE 8-7:*** *Simple Double Precision DAC Using MCP47CVBX2.*

**EQUATION 8-8: $V_{OUT}$ CALCULATION**

$$V_{OUT} = \frac{V_{OUT0} * R_2 + V_{OUT1} * R_1}{R_1 + R_2}$$

Where:
$V_{OUT0}$ = ($V_{REF}$ * Gx * DAC0 Register Value)/4096
$V_{OUT1}$ = ($V_{REF}$ * Gx * DAC1 Register Value)/4096
Gx = Selected Op Amp Gain

## 8.7 Building Programmable Current Source

Figure 8-8 shows an example of building a programmable current source using a voltage follower. The current sensor resistor is used to convert the DAC voltage output into a digitally-selectable current source.

The smaller $R_{SENSE}$ is, the less power is dissipated across it. However, this also reduces the resolution that the current can be controlled at.

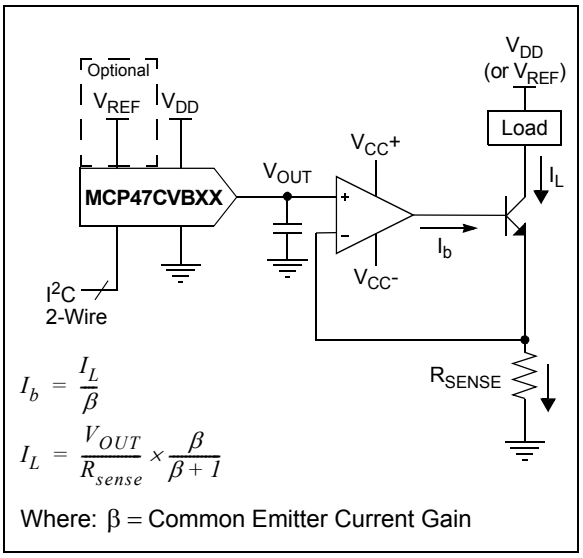



***FIGURE 8-8:*** *Digitally-Controlled Current Source.*

## 8.8 Serial Interface Communication Times

Table 7-1 shows the time/frequency of the supported operations of the $I^2C$ serial interface for the different serial interface operational frequencies. This, along with the $V_{OUT}$ output performance (such as slew rate), would be used to determine your application's Volatile DAC register update rate.


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## 8.9 Software I²C Interface Reset Sequence

**Note:** This technique is documented in *AN1028, "Recommended Usage of Microchip I²C Serial EEPROM Devices"* (DS01028).

At times, it may become necessary to perform a Software Reset sequence to ensure the MCP47CXBXX device is in a correct and known I²C interface state. This technique only resets the I²C state machine.

This is useful if the MCP47CXBXX device powers up in an incorrect state (due to excessive bus noise, etc.), or if the Master device is reset during communication. Figure 8-9 shows the communication sequence to software reset the device.

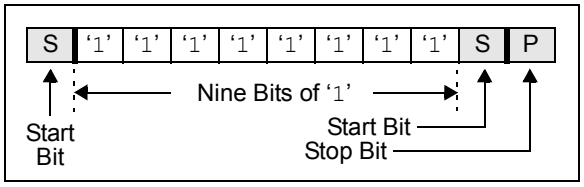



***FIGURE 8-9:*** *Software Reset Sequence Format.*

The first Start bit will cause the device to reset from a state in which it is expecting to receive data from the Master device. In this mode, the device is monitoring the data bus in Receive mode and can detect if the Start bit forces an internal Reset.

The nine bits of '1' are used to force a reset of those devices that could not be reset by the previous Start bit. This occurs only if the MCP47CXBXX is driving an A bit on the I²C bus or is in Output mode (from a read command) and is driving a data bit of '0' onto the I²C bus. In both of these cases, the previous Start bit could not be generated due to the MCP47CXBXX holding the bus low. By sending out nine '1' bits, it is ensured that the device will see an $\overline{A}$ bit (the Master device does not drive the I²C bus low to Acknowledge the data sent by the MCP47CXBXX), which also forces the MCP47CXBXX to reset.

The second Start bit is sent to address the rare possibility of an erroneous write. This could occur if the Master device was reset while sending a write command to the MCP47CXBXX, and then as the Master device returns to normal operation and issues a Start condition, while the MCP47CXBXX is issuing an Acknowledge. In this case, if the second Start bit is not sent (and the Stop bit was sent), the MCP47CXBXX could initiate a write cycle.

**Note:** The potential for this erroneous write ONLY occurs if the Master device is reset while sending a write command to the MCP47CVBXX.

The Stop bit terminates the current I²C bus activity. The MCP47CXBXX waits to detect the next Start condition. This sequence does not affect any other I²C devices which may be on the bus, as they should disregard this as an invalid command.

## 8.10 Design Considerations

In the design of a system with the MCP47CXBXX devices, the following considerations should be taken into account:

- Power Supply Considerations
- Layout Considerations

### 8.10.1 POWER SUPPLY CONSIDERATIONS

The typical application requires a bypass capacitor in order to filter high-frequency noise, which can be induced onto the power supply's traces. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 8-10 illustrates an appropriate bypass strategy.

In this example, the recommended bypass capacitor value is 0.1 µF. This capacitor should be placed as close (within 4 mm) to the device power pin ($V_{DD}$) as possible.

The power source supplying these devices should be as clean as possible. If the application circuit has separate digital and analog power supplies, $V_{DD}$ and $V_{SS}$ should reside on the analog plane.

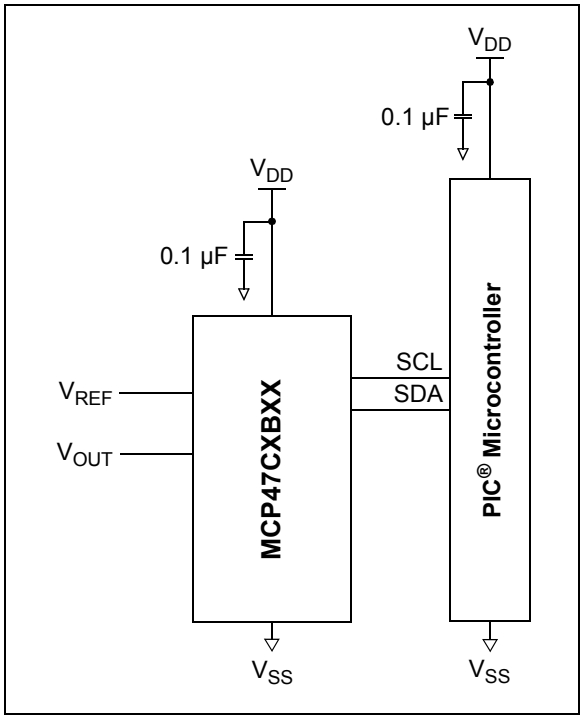



***FIGURE 8-10:*** *Typical Microcontroller Connections.*

### 8.10.2 LAYOUT CONSIDERATIONS

Several layout considerations may be applicable to your application. These may include:

- Noise
- PCB Area Requirements

#### 8.10.2.1 Noise

Inductively coupled AC transients and digital switching noise can degrade the input and output signal integrity, potentially masking the MCP47CXBXX device's performance. Careful board layout minimizes these effects and increases the Signal-to-Noise Ratio (SNR). Multi-layer boards utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving the performance that the silicon is capable of providing. Particularly harsh environments may require shielding of critical signals.

Separate digital and analog ground planes are recommended. In this case, the $V_{SS}$ pin and the ground pins of the $V_{DD}$ capacitors should be terminated to the analog ground plane.

| **Note:** | Breadboards and wire-wrapped boards are not recommended. |
|---|---|

#### 8.10.2.2 PCB Area Requirements

In some applications, PCB area is a criteria for device selection. Table 8-1 shows the typical package dimensions and area for the different package options.

**TABLE 8-1: PACKAGE FOOTPRINT(1)**

| Package | | | Package Footprint | | |
|---|---|---|---|---|---|
| Pins | Type | Code | Dimensions (mm) | | Area ($mm^2$) |
| | | | Length | Width | |
| 10 | MSOP | UN | 3.00 | 4.90 | 14.70 |
| 10 | DFN | MF | 3.00 | 3.00 | 9.00 |
| 16 | QFN | MG | 3.00 | 3.00 | 9.00 |

**Note 1:** Does not include recommended land pattern dimensions. Dimensions are typical values.


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## 9.0 DEVELOPMENT SUPPORT

Development support can be classified into two groups:

- Development Tools
- Technical Documentation

### 9.1 Development Tools

Several development tools are available to assist in your design and evaluation of the MCP47CXBXX devices. The currently available tools are shown in Table 9-1.

Figure 9-1 shows how the ADM00309 bond-out PCB can be populated to easily evaluate the MCP47CXBXX devices. Device evaluation can use the PICkit™ Serial Analyzer to control the DAC Output registers and state of the Configuration, Control and Status registers.

The ADM00309 boards may be purchased directly from the Microchip web site at www.microchip.com.

### 9.2 Technical Documentation

Several additional technical documents are available to assist you in your design and development. These technical documents include Application Notes, Technical Briefs and Design Guides. Table 9-2 lists some of these documents.

**TABLE 9-1: DEVELOPMENT TOOLS(1)**

| Board Name | Part # | Comment |
|---|---|---|
| MSOP-8 and MSOP-10 Evaluation Board | ADM00309 | The MSOP-8 and MSOP-10 Evaluation Board is a bond-out board that allows the system designer to quickly evaluate the operation of Microchip Technology's devices in any of the following packages:<br>• MSOP (8/10-pin)<br>• DIP (10 pin) |

**Note 1:** Supports the PICkit™ Serial Analyzer. See the User's Guide for additional information and requirements.

**TABLE 9-2: TECHNICAL DOCUMENTATION**

| Application Note Number | Title | Literature # |
|---|---|---|
| AN1326 | Using the MCP4728 12-Bit DAC for LDMOS Amplifier Bias Control Applications | DS01326 |
| — | Signal Chain Design Guide | DS21825 |
| — | Analog Solutions for Automotive Applications Design Guide | DS01005 |

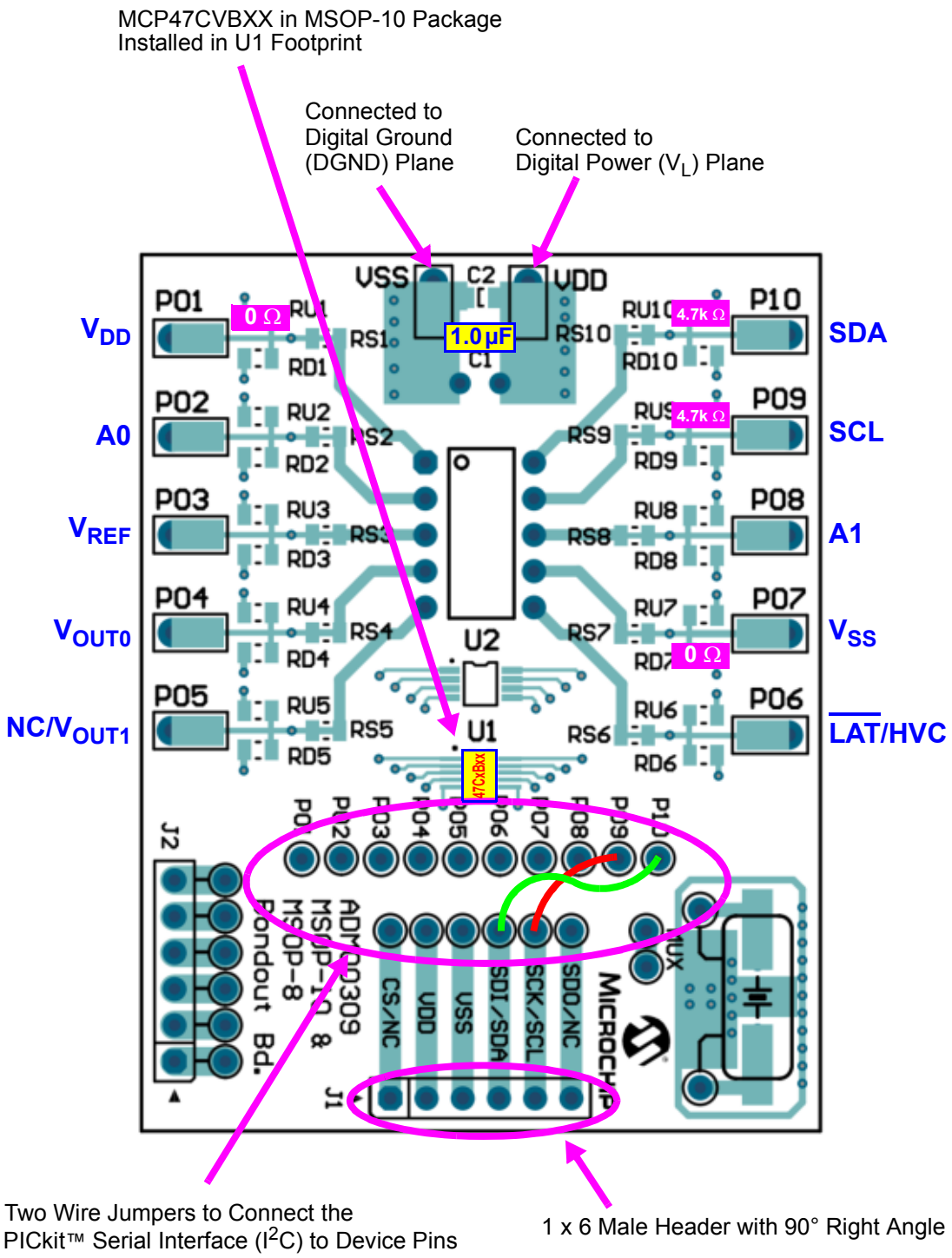


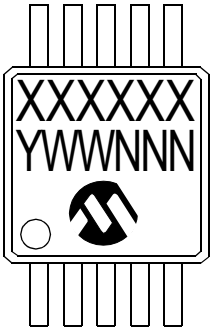

***FIGURE 9-1:*** *MCP47CXBXX Evaluation Board Circuit Using ADM00309.*


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## 10.0 PACKAGING INFORMATION

### 10.1 Package Marking Information

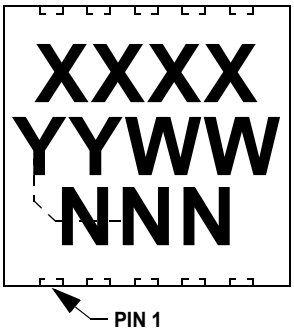
10-Lead MSOP




Example

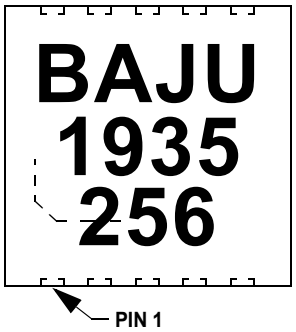



10-Lead DFN (3x3 mm)




| Part Number | Code |
|---|---|
| MCP47CVB01-E/MF | BAJU |
| MCP47CVB11-E/MF | BAJX |
| MCP47CVB21-E/MF | BAJZ |
| MCP47CVB02-E/MF | BAJV |
| MCP47CVB12-E/MF | BAJY |
| MCP47CVB22-E/MF | BAKA |
| MCP47CMB01-E/MF | BAJV |
| MCP47CMB11-E/MF | BAJQ |
| MCP47CMB21-E/MF | BAJS |
| MCP47CMB02-E/MF | BAJP |
| MCP47CMB12-E/MF | BAJR |
| MCP47CMB22-E/MF | BAJT |

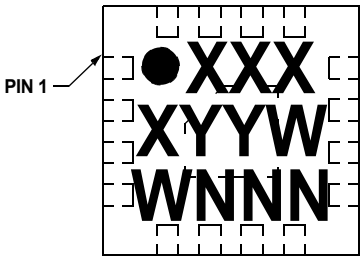
Example




| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

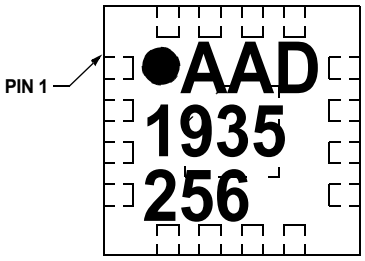
**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

16-Lead QFN (3x3 mm)




| Part Number | Code |
|---|---|
| MCP47CVB02-E/MG | AAD |
| MCP47CVB12-E/MG | AAE |
| MCP47CVB22-E/MG | AAF |
| MCP47CMB02-E/MG | AAA |
| MCP47CMB12-E/MG | AAB |
| MCP47CMB22-E/MG | AAC |

Example

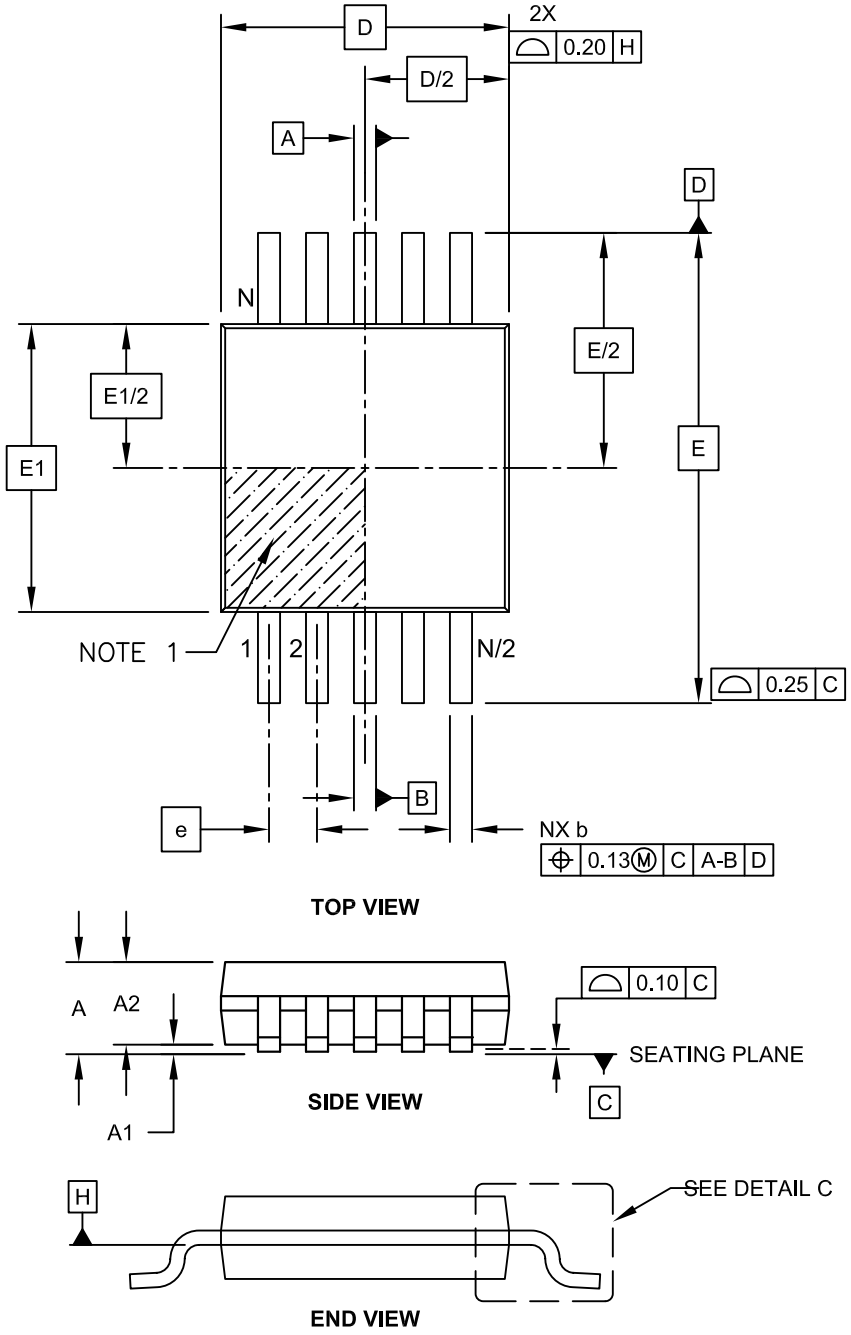



**Note:** For MCP47CVB02, MCP47CVB12, MCP47CVB22, MCP47CMB02, MCP47CMB12 and MCP47CMB22) devices.


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### 10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

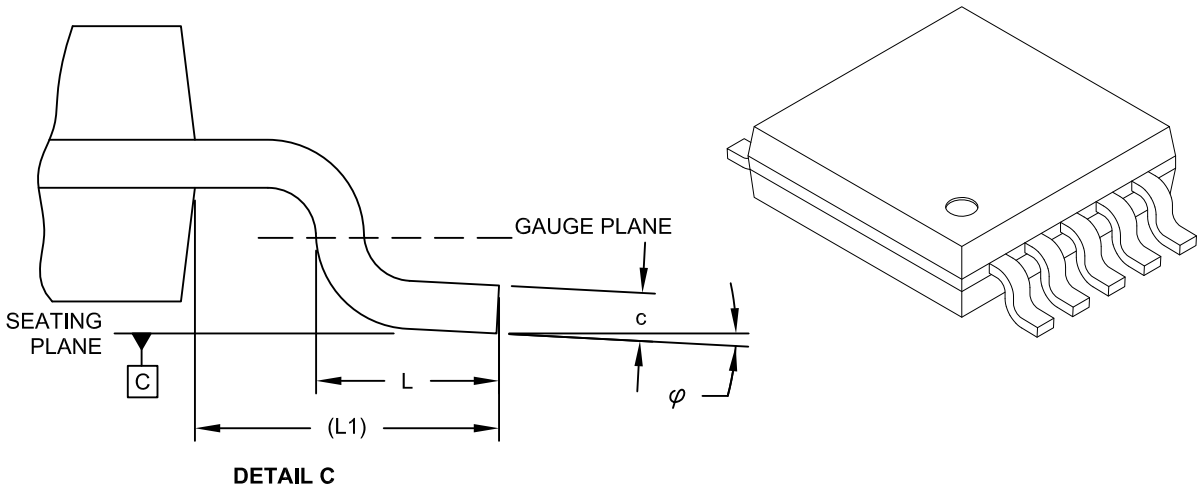
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-021C Sheet 1 of 2

## 10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




**DETAIL C**

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 10 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | - | - | 1.10 |
| Molded Package Thickness | A2 | 0.75 | 0.85 | 0.95 |
| Standoff | A1 | 0.00 | - | 0.15 |
| Overall Width | E | | 4.90 BSC | |
| Molded Package Width | E1 | | 3.00 BSC | |
| Overall Length | D | | 3.00 BSC | |
| Foot Length | L | 0.40 | 0.60 | 0.80 |
| Footprint | L1 | | 0.95 REF | |
| Foot Angle | φ | 0° | - | 8° |
| Lead Thickness | c | 0.08 | - | 0.23 |
| Lead Width | b | 0.15 | - | 0.33 |

**Notes:**

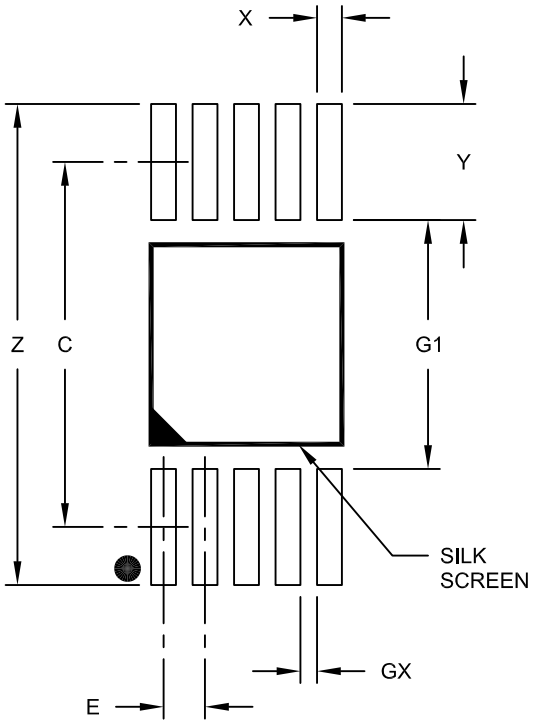
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-021C Sheet 2 of 2


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### 10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Contact Pad Spacing | C | | 4.40 | |
| Overall Width | Z | | | 5.80 |
| Contact Pad Width (X10) | X1 | | | 0.30 |
| Contact Pad Length (X10) | Y1 | | | 1.40 |
| Distance Between Pads | G1 | 3.00 | | |
| Distance Between Pads | GX | 0.20 | | |

Notes:

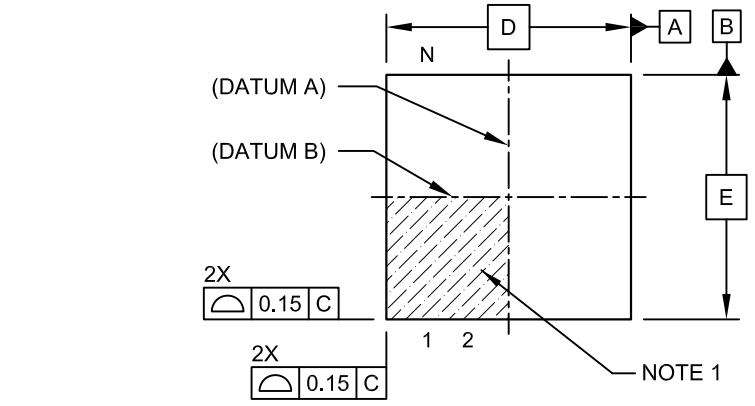
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

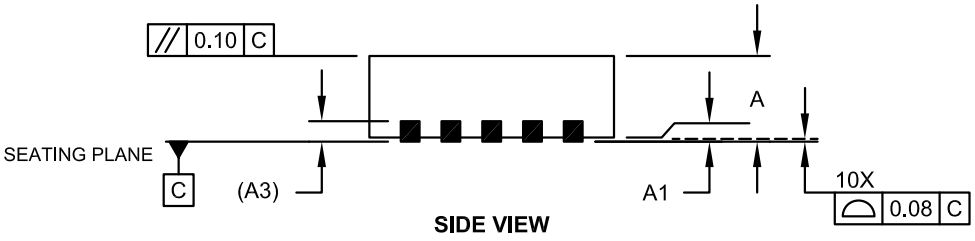
Microchip Technology Drawing No. C04-2021A

### 10-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

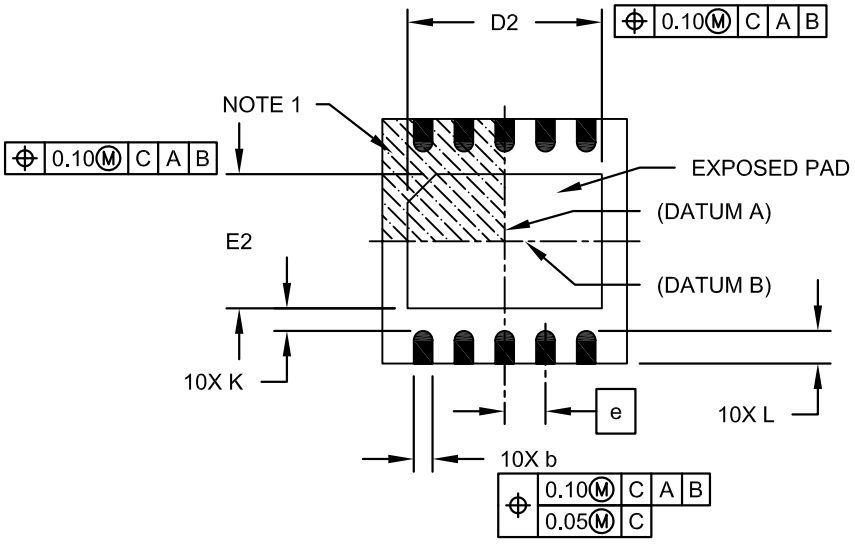
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




**TOP VIEW**




**SIDE VIEW**



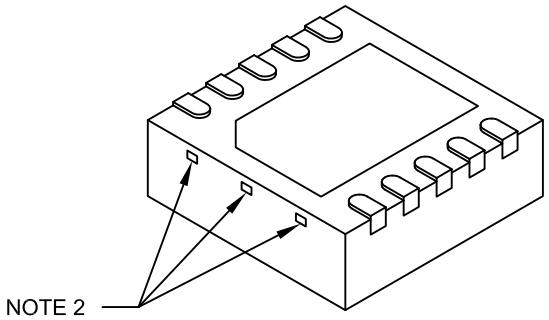

**BOTTOM VIEW**

Microchip Technology Drawing No. C04-063C Sheet 1 of 2


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### 10-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 10 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 3.00 BSC | |
| Exposed Pad Length | D2 | 2.15 | 2.35 | 2.45 |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Width | E2 | 1.40 | 1.50 | 1.75 |
| Contact Width | b | 0.18 | 0.25 | 0.30 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

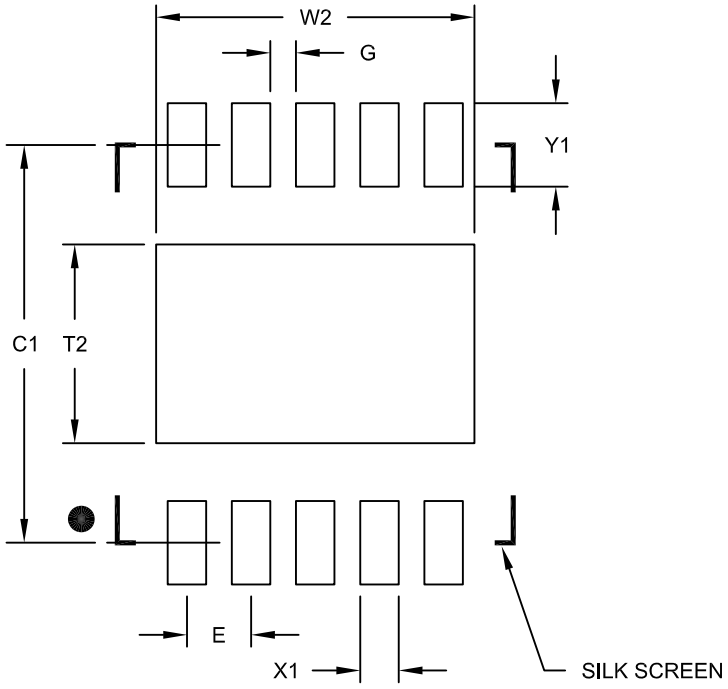
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-063C Sheet 2 of 2

### 10-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | W2 | | | 2.48 |
| Optional Center Pad Length | T2 | | | 1.55 |
| Contact Pad Spacing | C1 | | 3.10 | |
| Contact Pad Width (X10) | X1 | | | 0.30 |
| Contact Pad Length (X10) | Y1 | | | 0.65 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

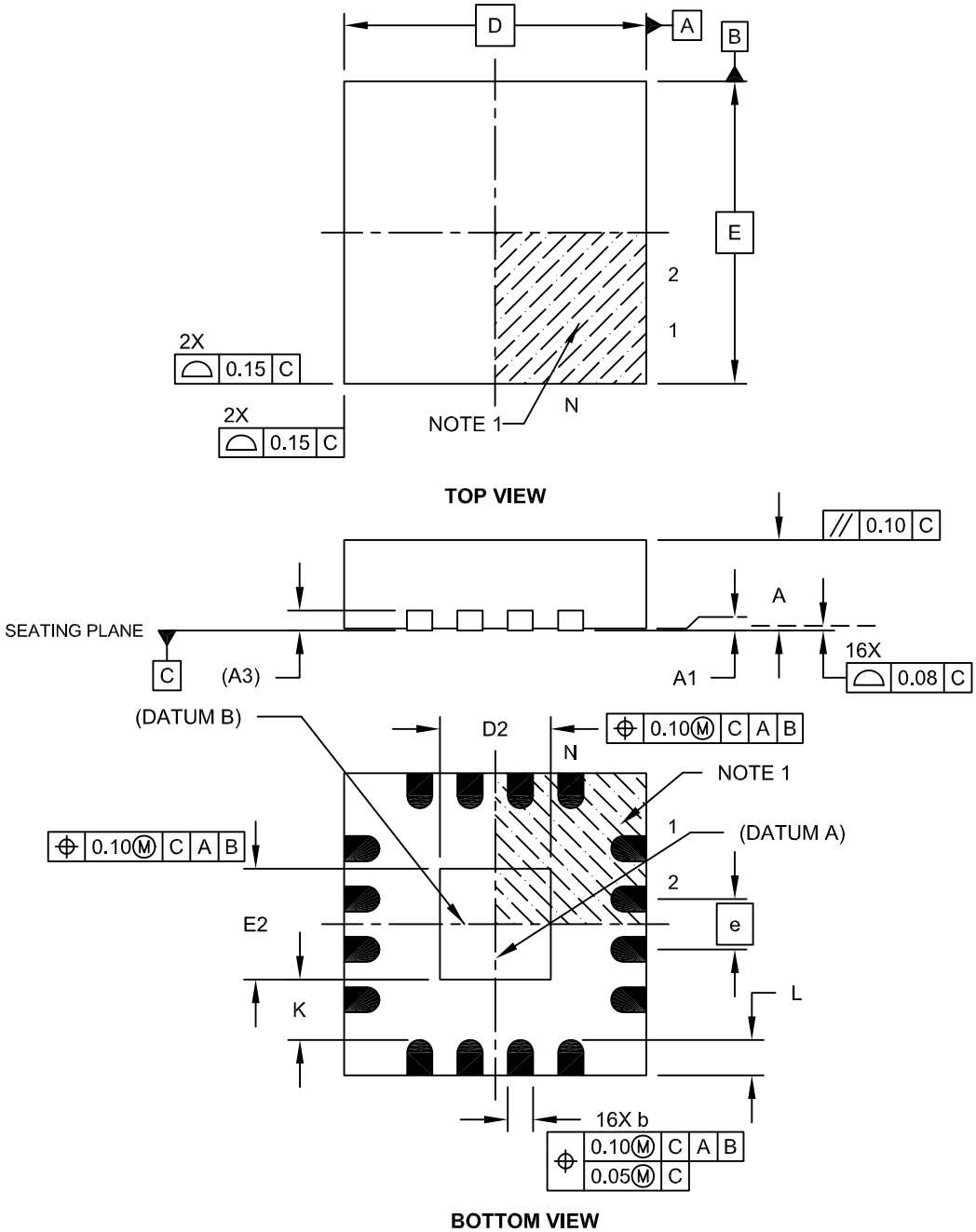
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2063B


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### 16-Lead Plastic Quad Flat, No Lead Package (MG) - 3x3x0.9 mm Body [QFN]

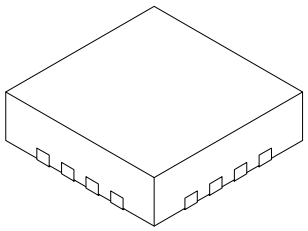
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-142A Sheet 1 of 2

### 16-Lead Plastic Quad Flat, No Lead Package (MG) - 3x3x0.9 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 16 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.85 | 0.90 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Width | E2 | 1.00 | 1.10 | 1.50 |
| Overall Length | D | | 3.00 BSC | |
| Exposed Pad Length | D2 | 1.00 | 1.10 | 1.50 |
| Contact Width | b | 0.18 | 0.25 | 0.30 |
| Contact Length | L | 0.25 | 0.35 | 0.45 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

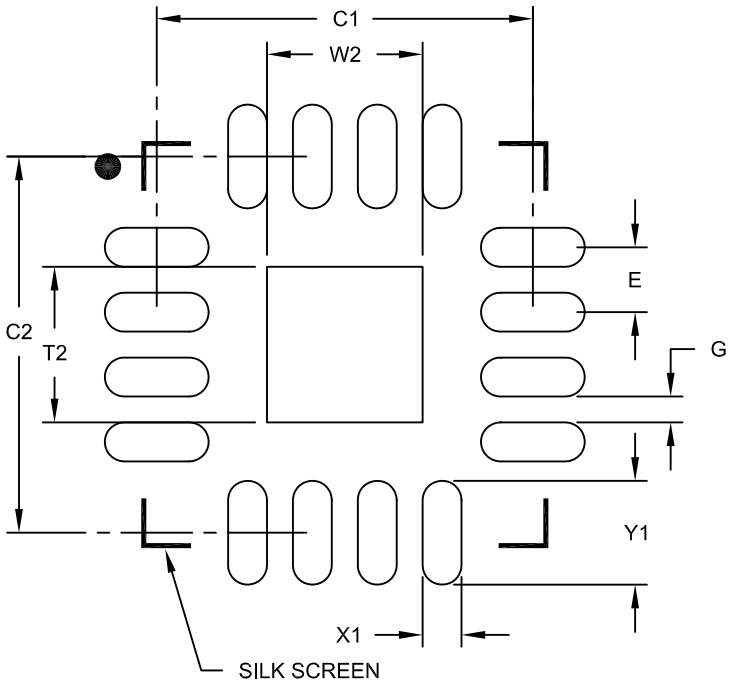
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-142A Sheet 2 of 2


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16-Lead Plastic Quad Flat, No Lead Package (MG) – 3x3x0.9 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | W2 | | | 1.20 |
| Optional Center Pad Length | T2 | | | 1.20 |
| Contact Pad Spacing | C1 | | 2.90 | |
| Contact Pad Spacing | C2 | | 2.90 | |
| Contact Pad Width (X16) | X1 | | | 0.30 |
| Contact Pad Length (X16) | Y1 | | | 0.80 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2142A

**NOTES:**


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# APPENDIX A: REVISION HISTORY

## Revision B (June 2019)

- Corrected the Internal Band Gap voltage throughout the document.
- Updated the Block Diagrams.
- Updated **DC Characteristics** table.
- Added **Section 1.1.2, Latch Pin (LAT) Timing**.
- Updated Figure 1-3, Figure 1-4 and Figure 4-1.
- Updated Table 1-3, Table 1-5, Table 3-2 and Table 4-1.
- Updated **Section 3.5 "Latch/High-Voltage Command Pin (LAT/HVC)"**.
- Updated **Section 4.2.2 "Nonvolatile Register Memory (MTP)"**.
- Updated **Section 5.2.3 "Using an External $V_{REF}$ Source in Buffered Mode"**.
- Updated **Section 5.3.2 "Output Voltage"**.
- Various typographical edits.

## Revision A (September 2018)

- Original release of this document.

**NOTES:**


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# APPENDIX B: I²C SERIAL INTERFACE

This I²C is a two-wire interface that allows multiple devices to be connected to the two-wire bus. Figure B-1 shows a typical I²C interface connection.

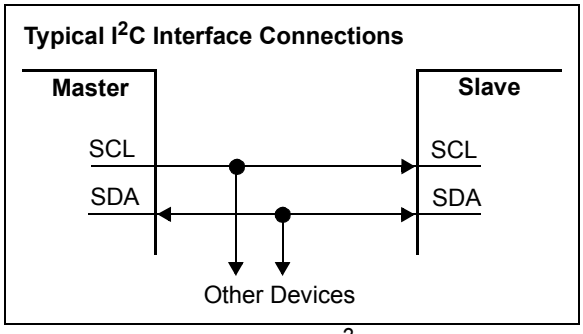



***FIGURE B-1:*** *Typical I²C Interface.*

## B.1 Overview

A device that sends data onto the bus is defined as a transmitter and a device receiving data is defined as a receiver. The bus has to be controlled by a Master device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions. Devices that do not generate a serial clock work as Slave devices. Both Master and Slave can operate as transmitter or receiver, but the Master device determines which mode is activated. Communication is initiated by the Master (microcontroller), which sends the Start bit followed by the Slave address byte. The first byte transmitted is always the Slave address byte, which contains the device code, the address bits and the R/$\overline{W}$ bit.

The I²C interface specifies different communication bit rates. These are referred to as Standard, Fast or High-Speed modes and the MCP47CXBXX supports these three modes. The clock rates (bit rate) of these modes are:

- Standard mode: Up to 100 kHz (kbit/s)
- Fast mode: Up to 400 kHz (kbit/s)
- High-Speed mode (HS mode): Up to 3.4 MHz (Mbit/s)

The I²C protocol supports two addressing modes:

- 7-Bit Slave Addressing
- 10-Bit Slave Addressing (allows more devices on the I²C bus)

Only 7-Bit Slave Addressing will be discussed in this section.

The I²C serial protocol allows multiple Master devices on the I²C bus. This is referred to as “Multi-Master”. For this, all Master devices must support Multi-Master operation. In this configuration, all Master devices monitor their communication. If they detect that they wish to transmit a bit that is a logic high, but is detected as a logic low (some other Master device driving), they “get off” the bus. That is, they stop their communication and continue to listen to determine if the communication is directed towards them.

The I²C serial protocol only defines the field types, field lengths, timings, etc., of a frame. The frame content defines the behavior of the device. For details on the frame content (commands/data), refer to **Section 7.0, Device Commands**.

The I²C serial protocol defines some commands, called “General Call Addressing”, which allow the Master device to communicate to all Slave devices on the I²C bus.

| **Note:** | Refer to the *“NXP Specification #UM10204”*, Rev. 06, 4 April 2014 document for more details on the I²C specifications. |
|---|---|

## B.2 Signal Descriptions

The I²C interface uses two pins (signals). These are:

- SDA (Serial Data)
- SCL (Serial Clock)

### B.2.1 SERIAL DATA (SDA)

The Serial Data (SDA) signal is the data signal of the device. The value on this pin is latched on the rising edge of the SCL signal when the signal is an input.

With the exception of the Start (Restart) and Stop conditions, the high or low state of the SDA pin can only change when the clock signal on the SCL pin is low. During the high period of the clock, the SDA pin's value (high or low) must be stable. Changes in the SDA pin's value while the SCL pin is high will be interpreted as a Start or a Stop condition.

### B.2.2 SERIAL CLOCK (SCL)

The Serial Clock (SCL) signal is the clock signal of the device. The rising edge of the SCL signal latches the value on the SDA pin.

Depending on the Clock Rate mode, the interface will display different characteristics.

## B.3 I²C Operation

### B.3.1 I²C BIT STATES AND SEQUENCE

Figure B-8 shows the I²C transfer sequence, while Figure B-7 shows the bit definitions. The serial clock is generated by the Master. The following definitions are used for the bit states:

- Start Bit (S)
- Data Bit
- Acknowledge (A) Bit (driven low)/
  No Acknowledge ($\overline{A}$) bit (not driven low)
- Repeated Start Bit (Sr)
- Stop Bit (P)

#### B.3.1.1 Start Bit

The Start bit (see Figure B-2) indicates the beginning of a data transfer sequence. The Start bit is defined as the SDA signal falling when the SCL signal is "high".

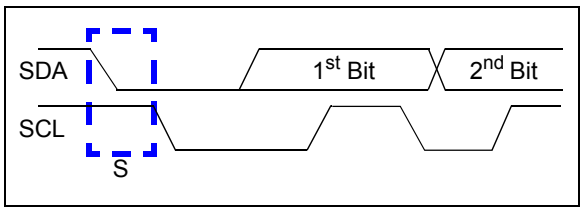



***FIGURE B-2:*** *Start Bit.*

#### B.3.1.2 Data Bit

The SDA signal may change state while the SCL signal is low. While the SCL signal is high, the SDA signal MUST be stable (see Figure B-3).

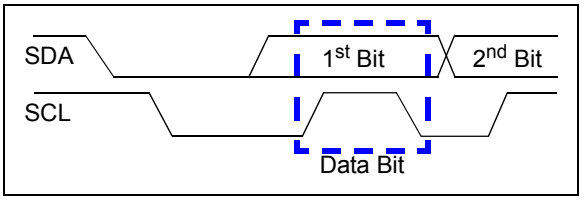



***FIGURE B-3:*** *Data Bit.*

#### B.3.1.3 Acknowledge (A) Bit

The A bit (see Figure B-4) is typically a response from the receiving device to the transmitting device. Depending on the context of the transfer sequence, the A bit may indicate different things. Typically, the Slave device will supply an A response after the Start bit and eight "data" bits have been received. An A bit has the SDA signal low, while the $\overline{A}$ bit has the SDA signal high.

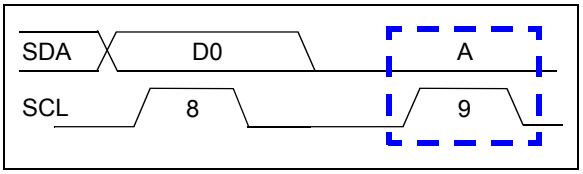



***FIGURE B-4:*** *Acknowledge Waveform.*

Table B-1 shows some of the conditions where the Slave device issues the A or Not A ($\overline{A}$).

If an error condition occurs (such as an $\overline{A}$ instead of A), then a Start bit must be issued to reset the command state machine.

**TABLE B-1: MCP47CXBXX A/$\overline{A}$ RESPONSES**

| Event | Acknowledge Bit Response | Comment |
|---|---|---|
| General Call | A | |
| Slave Address Valid | A | |
| Slave Address Not Valid | $\overline{A}$ | |
| Bus Collision | N/A | I²C module resets or is a "Don't Care" if the collision occurs on the Master's "Start bit" |


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### B.3.1.4 Repeated Start Bit

The Repeated Start bit (see Figure B-5) indicates the current Master device wishes to continue communicating with the current Slave device without releasing the $I^2C$ bus. The Repeated Start condition is the same as the Start condition, except that the Repeated Start bit follows a Start bit (with the Data bits + A bit) and not a Stop bit.

The Start bit is the beginning of a data transfer sequence and is defined as the SDA signal falling when the SCL signal is “high”.

**Note 1:** A bus collision during the Repeated Start condition occurs if:

- SDA is sampled low when SCL goes from low-to-high.
- SCL goes low before SDA is asserted low. This may indicate that another Master is attempting to transmit a data ‘1’.

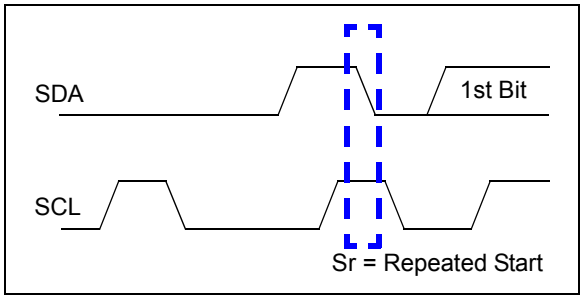



***FIGURE B-5:*** *Repeated Start Condition Waveform.*

### B.3.1.5 Stop Bit

The Stop bit (see Figure B-6) Indicates the end of the $I^2C$ data transfer sequence. The Stop bit is defined as the SDA signal rising when the SCL signal is “high”.

A Stop bit should reset the $I^2C$ interface of the Slave device.

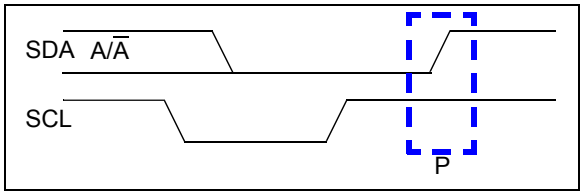



***FIGURE B-6:*** *Stop Condition Receive or Transmit Mode.*

### B.3.2 CLOCK STRETCHING

“Clock Stretching” is something the receiving device can do, to allow additional time to “respond” to the “data” that has been received.

### B.3.3 ABORTING A TRANSMISSION

If any part of the $I^2C$ transmission does not meet the command format, it is aborted. This can be intentionally accomplished with a Start or Stop condition. This is done so that noisy transmissions (usually an extra Start or Stop condition) are aborted before they corrupt the device.

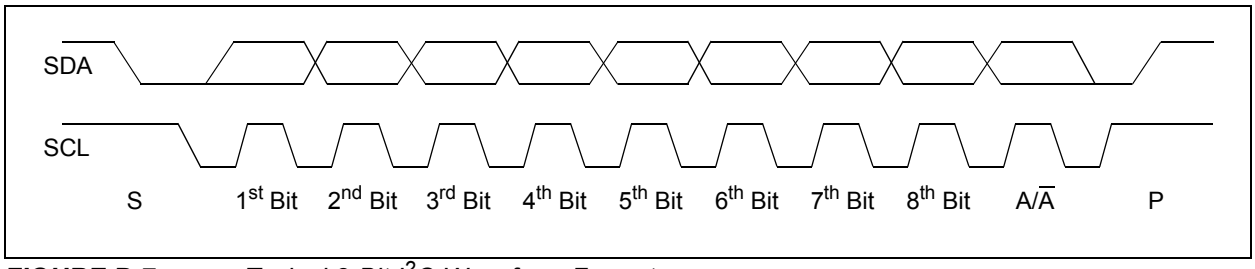



***FIGURE B-7:*** *Typical 8-Bit $I^2C$ Waveform Format.*

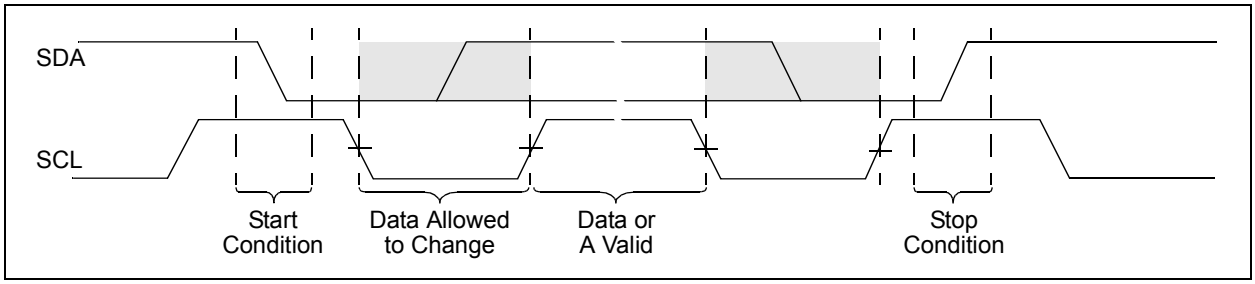



***FIGURE B-8:*** *$I^2C$ Data States and Bit Sequence.*

### B.3.4 SLOPE CONTROL

As the device transitions from High-Speed (HS) mode to Fats (FS) mode, the slope control parameter will change from the HS specification to the FS specification.

For FS and HS modes, the device has a spike suppression and a Schmitt Trigger at SDA and SCL inputs.

### B.3.5 DEVICE ADDRESSING

The I²C Slave address control byte is the first byte received following the Start condition from the Master device. This byte has seven bits to specify the Slave address and the read/write control bit.

Figure B-9 shows the I²C Slave address byte format, which contains the seven address bits and a Read/Write (R/$\overline{W}$) bit.

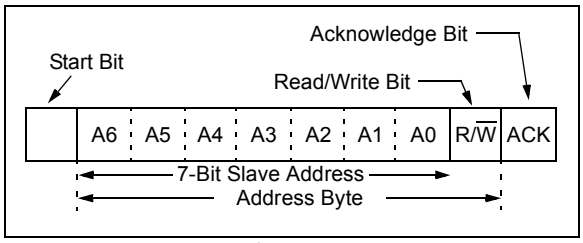



***FIGURE B-9:*** *I²C Slave Address Control Byte.*

### B.3.6 HS MODE

The I²C specification requires that a High-Speed mode device must be 'activated' to operate in High-Speed (3.4 Mbit/s) mode. This is done by the Master sending a special address byte following the Start bit. This byte is referred to as the High-Speed Master Mode Code (HSMMC).

The device can now communicate at up to 3.4 Mbit/s on SDA and SCL lines. The device will switch out of the HS mode on the next Stop condition.

The Master code is sent as follows:

1. Start condition (S).
2. High-Speed Master Mode Code ('`0000 1xxx`'); the '`xxx`' bits are unique to the HS mode Master.
3. No Acknowledge ($\overline{A}$).

After switching to HS mode, the next transferred byte is the I²C control byte, which specifies the device to communicate with, and any number of data bytes plus Acknowledgments. The Master device can then either issue a Repeated Start bit to address a different device (at high speed) or a Stop bit to return to fast/standard bus speed. After the Stop bit, any other Master device (in a Multi-Master system) can arbitrate for the I²C bus.

See Figure B-10 for an illustration of an HS mode command sequence.

For more information on the HS mode, or other I²C modes, refer to the *"NXP I²C Specification"*.

#### B.3.6.1 Slope Control

The slope control on the SDA output is different between the Fast/Standard Speed and the High-Speed Clock modes of the interface.

#### B.3.6.2 Pulse Gobbler

The pulse gobbler on the SCL pin is automatically adjusted to suppress spikes <10 ns during HS mode.

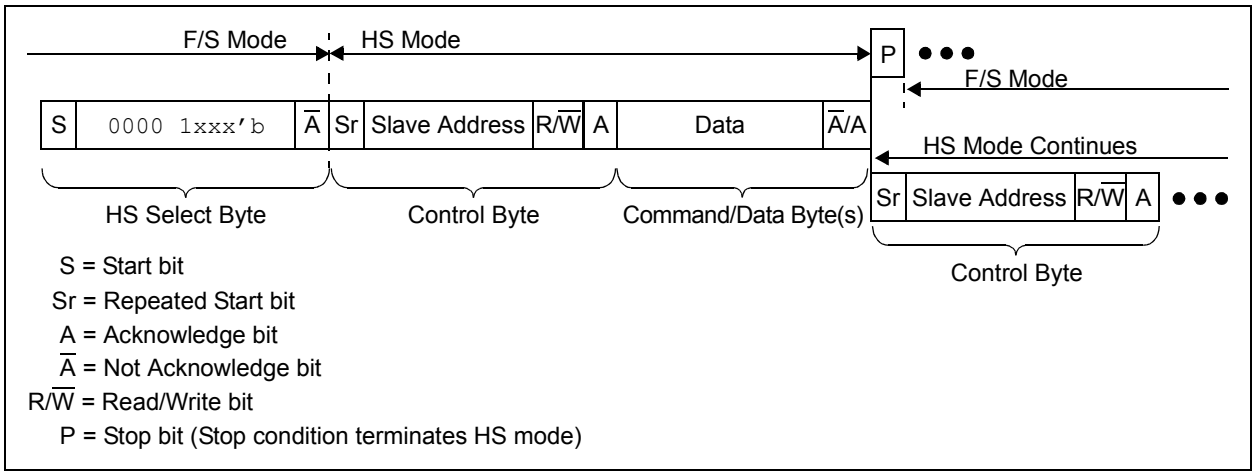



***FIGURE B-10:*** *HS Mode Sequence.*


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### B.3.7 GENERAL CALL

The general call is a method the Master device can use to communicate with all other Slave devices. In a Multi-Master application, the other Master devices are operating in Slave mode. The general call address has two documented formats. These are shown in Figure B-11.

The I²C specification documents three 7-bit command bytes.

The I²C specification does not allow '00000000' (00h) in the second byte. Also, the '00000100' and '00000110' functionalities are defined by the specification. Lastly, a data byte with a '1' in the LSb indicates a "Hardware General Call".

For details on the operation of the MCP47CXBXX device's general call commands, see **Section 7.3 "General Call Commands"**.

| **Note:** | Only one general call command per issue of the general call control byte. Any additional general call commands are ignored and Not Acknowledged. |
|---|---|

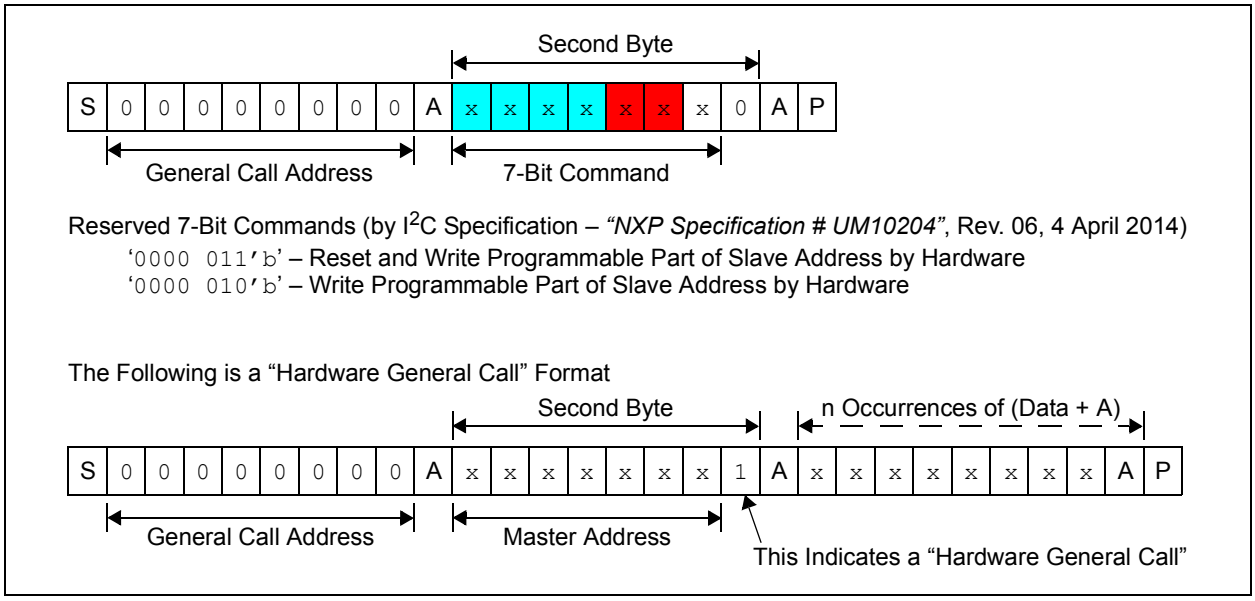



***FIGURE B-11:*** *General Call Formats.*

**NOTES:**


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# APPENDIX C: TERMINOLOGY

## C.1 Resolution

The resolution is the number of DAC output states that divide the Full-Scale Range (FSR). For the 12-bit DAC, the resolution is $2^{12}$, meaning the DAC code ranges from 0 to 4095.

**Note:** When there are $2^N$ resistors in the resistor ladder and $2^N$ tap points, the full-scale DAC register code is the resistor element (1 LSb) from the source reference voltage ($V_{DD}$ or $V_{REF}$).

## C.2 Least Significant Bit (LSb)

This is the voltage difference between two successive codes. For a given output voltage range, it is divided by the resolution of the device (Equation C-1). The range may be $V_{DD}$ (or $V_{REF}$) to $V_{SS}$ (ideal); the DAC register codes across the linear range of the output driver (Measured 1) or full scale to zero scale (Measured 2).

**EQUATION C-1: LSb VOLTAGE CALCULATION**

**Ideal**

$$V_{LSb(IDEAL)} = \frac{V_{DD}}{2^N} \text{ or } \frac{V_{REF}}{2^N}$$

**Measured 1**

$$V_{LSb(Measured)} = \frac{V_{OUT(@4032)} - V_{OUT(@64)}}{(4032 - 64)}$$

**Measured 2**

$$V_{LSb} = \frac{V_{OUT(@FS)} - V_{OUT(@ZS)}}{2^N - 1}$$

$2^N$ = 4096 (MCP47CVB2X)
= 1024 (MCP47CVB1X)
= 256 (MCP47CVB0X)

## C.3 Monotonic Operation

The monotonic operation means that the device's Output Voltage ($V_{OUT}$) increases with every one code step (LSb) increment (from $V_{SS}$ to the DAC's reference voltage ($V_{DD}$ or $V_{REF}$)).

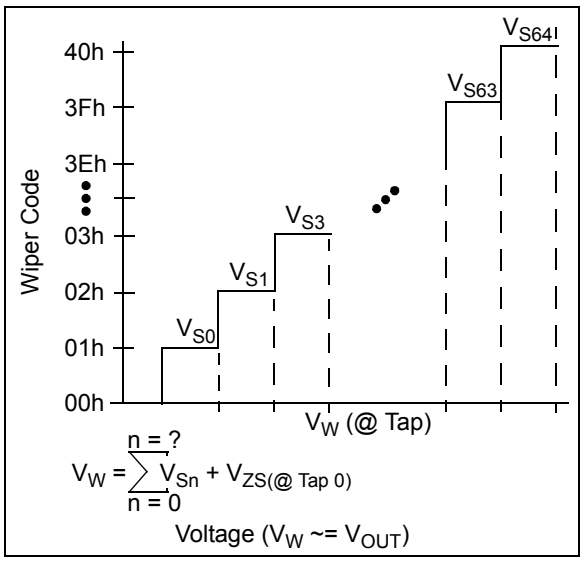



***FIGURE C-1:*** *$V_W$ ($V_{OUT}$).*

## C.4 Full-Scale Error ($E_{FS}$)

The Full-Scale Error, $E_{FS}$ (see Figure C-3), is the error on the $V_{OUT}$ pin relative to the expected $V_{OUT}$ voltage (theoretical) for the maximum device DAC register code (code FFFh for 12-bit, code 3FFh for 10-bit and code FFh for 8-bit); see Equation C-2. The error is dependent on the resistive load on the $V_{OUT}$ pin (and where that load is tied to, such as $V_{SS}$ or $V_{DD}$). For loads (to $V_{SS}$) greater than specified, the full-scale error will be greater.

The error in bits is determined by the theoretical voltage step-size to give an error in LSb.

**EQUATION C-2: FULL-SCALE ERROR**

$$E_{FS} = \frac{V_{OUT(@FS)} - V_{IDEAL(@FS)}}{V_{LSb(IDEAL)}}$$

Where:

$E_{FS}$ is expressed in LSb.

$V_{OUT(@FS)}$ is the $V_{OUT}$ voltage when the DAC register code is at full scale.

$V_{IDEAL(@FS)}$ is the ideal output voltage when the DAC register code is at full scale.

$V_{LSb(IDEAL)}$ is the theoretical voltage step-size.

## C.5 Zero-Scale Error ($E_{ZS}$)

The Zero-Scale Error, $E_{ZS}$ (see Figure C-2), is the difference between the ideal and measured $V_{OUT}$ voltage with the DAC register code equal to 000h (Equation C-3). The error is dependent on the resistive load on the $V_{OUT}$ pin (and where that load is tied to, such as $V_{SS}$ or $V_{DD}$). For loads (to $V_{DD}$) greater than specified, the zero-scale error is greater.

The error in bits is determined by the theoretical voltage step-size to give an error in LSb.

**EQUATION C-3: ZERO-SCALE ERROR**

$$E_{ZS} = \frac{V_{OUT(@ZS)}}{V_{LSb(IDEAL)}}$$

Where:

$E_{FS}$ is expressed in LSb.

$V_{OUT(@ZS)}$ is the $V_{OUT}$ voltage when the DAC register code is at zero scale.

$V_{LSb(IDEAL)}$ is the theoretical voltage step-size.

## C.6 Total Unadjusted Error ($E_T$)

The Total Unadjusted Error ($E_T$) is the difference between the ideal and measured $V_{OUT}$ voltage. Typically, calibration of the output voltage is implemented to improve the system's performance.

The error in bits is determined by the theortical voltage step-size to give an error in LSb.

Equation C-4 shows the total unadjusted error calculation.

**EQUATION C-4: TOTAL UNADJUSTED ERROR CALCULATION**

$$E_T = \frac{(V_{OUT_Actual(@code)} - V_{OUT_Ideal(@code)})}{V_{LSb(Ideal)}}$$

Where:

$E_T$ is expressed in LSb.

$V_{OUT_Actual(@code)}$ = The measured DAC output voltage at the specified code

$V_{OUT_Ideal(@code)}$ = The calculated DAC output voltage at the specified code (*code* * $V_{LSb(Ideal)}$)

$V_{LSb(Ideal)}$ = $V_{REF}$/# Steps
12-bit = $V_{REF}$/4096
10-bit = $V_{REF}$/1024
8-bit = $V_{REF}$/256


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## C.7 Offset Error ($E_{OS}$)

The Offset Error ($E_{OS}$) is the delta voltage of the $V_{OUT}$ voltage from the ideal output voltage at the specified code. This code is specified where the output amplifier is in the linear operating range; for the MCP47CXBXX, we specify code 100 (decimal). Offset error does not include gain error, which is illustrated in Figure C-2.

This error is expressed in mV. Offset error can be negative or positive. The error can be calibrated by software in application circuits.

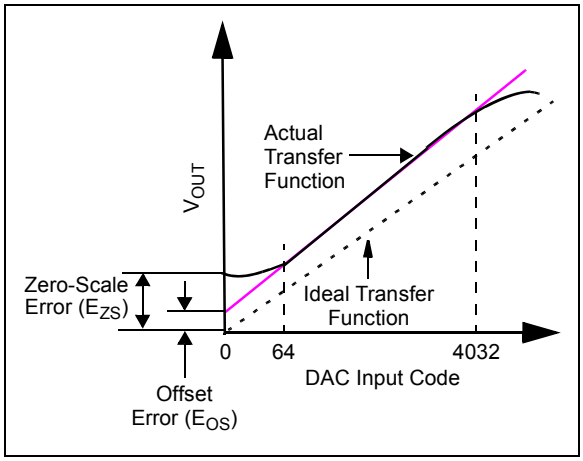



***FIGURE C-2:*** *Offset Error (Zero Gain Error).*

## C.8 Offset Error Drift ($E_{OSD}$)

The Offset Error Drift ($E_{OSD}$) is the variation in offset error due to a change in ambient temperature. The offset error drift is typically expressed in ppm/°C or µV/°C.

## C.9 Gain Error ($E_G$)

Gain Error ($E_G$) is a calculation based on the ideal slope using the voltage boundaries for the linear range of the output driver (e.g., code 100 and code 4000); see Figure C-3). The gain error calculation nullifies the device's offset error.

The gain error indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. The gain error is usually expressed as a percent of Full-Scale Range (% of FSR) or in LSb. FSR is the ideal full-scale voltage of the DAC (see Equation C-5).

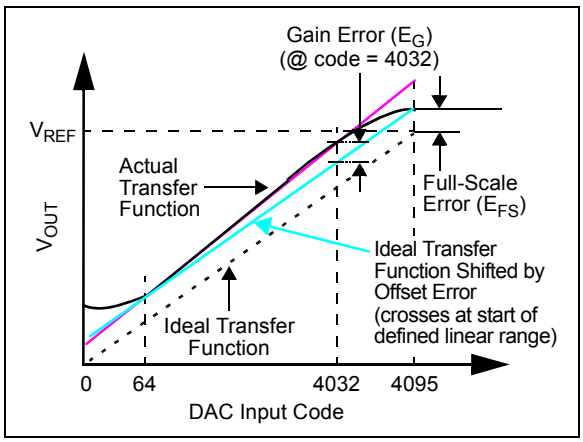



***FIGURE C-3:*** *Gain Error and Full-Scale Error Example.*

**EQUATION C-5: GAIN ERROR EXAMPLE**

$$E_G = \frac{(V_{OUT(@4032)} - V_{OS} - V_{OUT_Ideal(@4032)})}{V_{Full\text{-}Scale\ Range}} * 100$$

Where:

$E_G$ is expressed in % of Full-Scale Range (FSR).

$V_{OUT(@4032)}$ = The measured DAC output voltage at the specified code

$V_{OUT_Ideal(@4032)}$ = The calculated DAC output voltage at the specified code (4032 * $V_{LSb(Ideal)}$)

$V_{OS}$ = Measured offset voltage

$V_{Full\text{-}Scale\ Range}$ = Expected full-scale output value (such as the $V_{REF}$ voltage)

## C.10 Gain Error Drift ($E_{GD}$)

The Gain Error Drift ($E_{GD}$) is the variation in gain error due to a change in ambient temperature. The gain error drift is typically expressed in ppm/°C (of Full-Scale Range).

## C.11 Integral Nonlinearity (INL)

The Integral Nonlinearity (INL) error is the maximum deviation of an actual transfer function, from an ideal transfer function (straight line), passing through the defined end-points of the DAC transfer function (after Offset and Gain Errors have been removed).

For the MCP47CXBXX, INL is calculated using the defined end points, DAC code 64 and code 4032. INL can be expressed as a percentage of Full-Scale Range (FSR) or in LSb. INL is also called relative accuracy. Equation C-6 shows how to calculate the INL error in LSb and Figure C-4 shows an example of INL accuracy.

Positive INL means a $V_{OUT}$ voltage higher than the ideal one. Negative INL means a $V_{OUT}$ voltage lower than the ideal one.

**EQUATION C-6: INL ERROR**

$$E_{INL} = \frac{(V_{OUT} - V_{Calc_Ideal})}{V_{LSb(Measured)}}$$

Where:

INL is expressed in LSb

$V_{Calc_Ideal}$ = Code * $V_{LSb(Measured)}$ + $V_{OS}$

$V_{OUT(Code = n)}$ = The measured DAC output voltage with a given DAC register code

$V_{LSb(Measured)}$ = For Measured: $(V_{OUT(4032)} - V_{OUT(64)})/3968$

$V_{OS}$ = Measured offset voltage

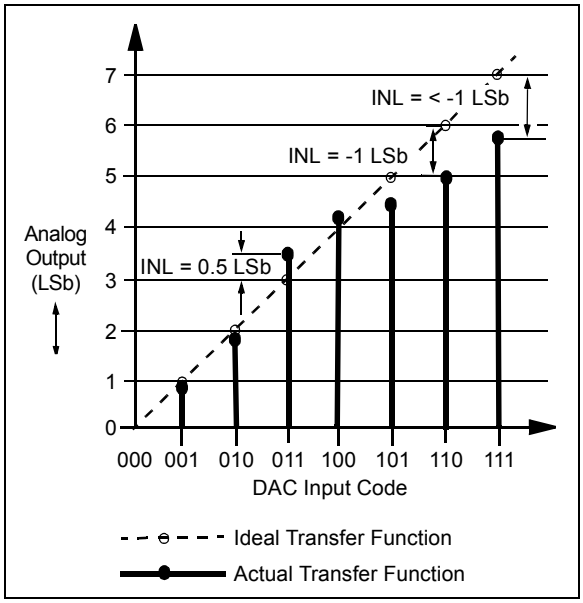



***FIGURE C-4:*** *INL Accuracy.*

## C.12 Differential Nonlinearity (DNL)

The Differential Nonlinearity (DNL) error (see Figure C-5) is the measure of step-size between codes in an actual transfer function. The ideal step-size between codes is 1 LSb. A DNL error of zero would imply that every code is exactly 1 LSb wide. If the DNL error is less than 1 LSb, the DAC ensures monotonic output and no missing codes. Equation C-7 shows how to calculate the DNL error between any two adjacent codes in LSb.

**EQUATION C-7: DNL ERROR**

$$E_{DNL} = \frac{(V_{OUT(code = n+1)} - V_{OUT(code = n)})}{V_{LSb(Measured)}} - 1$$

Where:

DNL is expressed in LSb.

$V_{OUT(Code = n)}$ = The measured DAC output voltage with a given DAC register code

$V_{LSb(Measured)}$ = For Measured: $(V_{OUT(4032)} - V_{OUT(64)})/3968$

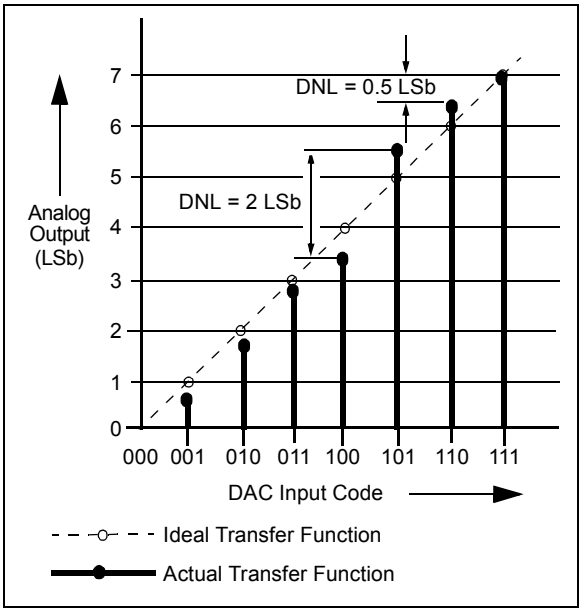



***FIGURE C-5:*** *DNL Accuracy.*


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## C.13 Settling Time

The settling time is the time delay required for the $V_{OUT}$ voltage to settle into its new output value. This time is measured from the start of code transition to when the $V_{OUT}$ voltage is within the specified accuracy.

For the MCP47CXBXX, the settling time is a measure of the time delay until the $V_{OUT}$ voltage reaches within 0.5 LSb of its final value, when the Volatile DAC register changes from 1/4 to 3/4 of the Full-Scale Range (12-bit device: 400h to C00h).

## C.14 Major Code Transition Glitch

Major code transition glitch is the impulse energy injected into the DAC analog output when the code in the DAC register changes the state. It is normally specified as the area of the glitch in nV-Sec and is measured when the digital code is changed by 1 LSb at the major carry transition (Example: `011...111` to `100...000`, or `100...000` to `011...111`).

## C.15 Digital Feedthrough

The digital feedthrough is the glitch that appears at the analog output caused by coupling from the digital input pins of the device. The area of the glitch is expressed in nV-Sec and is measured with a full-scale change (Example: all '`0`'s to all '`1`'s and vice versa) on the digital input pins. The digital feedthrough is measured when the DAC is not being written to the output register.

## C.16 -3 dB Bandwidth

This is the frequency of the signal at the $V_{REF}$ pin that causes the voltage at the $V_{OUT}$ pin to fall to -3 dB from a static value on the $V_{REF}$ pin. The output decreases due to the RC characteristics of the resistor ladder and the characteristics of the output buffer.

## C.17 Power Supply Sensitivity (PSS)

PSS indicates how the output of the DAC is affected by changes in the supply voltage. PSS is the ratio of the change in $V_{OUT}$ to a change in $V_{DD}$ for mid-scale output of the DAC. The $V_{OUT}$ is measured while the $V_{DD}$ is varied from 5.5V to 2.7V as a step ($V_{REF}$ voltage held constant), and expressed in %/%, which is the % change of the DAC output voltage with respect to the % change of the $V_{DD}$ voltage.

**EQUATION C-8: PSS CALCULATION**

$$PSS = \frac{(V_{OUT(@5.5V)} - V_{OUT(@2.7V)}) / V_{OUT(@5.5V)}}{(5.5V - 2.7V) / (5.5V)}$$

Where:

PSS is expressed in %/%.

$V_{OUT(@5.5V)}$ = The measured DAC output voltage with $V_{DD}$ = 5.5V

$V_{OUT(@2.7V)}$ = The measured DAC output voltage with $V_{DD}$ = 2.7V

## C.18 Power Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in $V_{OUT}$ to a change in $V_{DD}$ for full-scale output of the DAC. The $V_{OUT}$ is measured while the $V_{DD}$ is varied ±10% ($V_{REF}$ voltage held constant) and expressed in dB or µV/V.

## C.19 $V_{OUT}$ Temperature Coefficient

The $V_{OUT}$ temperature coefficient quantifies the error in the resistor ladder's resistance ratio (DAC register code value) and output buffer due to temperature drift.

## C.20 Absolute Temperature Coefficient

The absolute temperature coefficient quantifies the error in the end-to-end output voltage (nominal output voltage, $V_{OUT}$) due to temperature drift. For a DAC, this error is typically not an issue due to the ratiometric aspect of the output.

## C.21 Noise Spectral Density

The noise spectral density is a measurement of the device's internally generated random noise and is characterized as a spectral density (voltage per √Hz). It is measured by loading the DAC to the mid-scale value and measuring the noise at the $V_{OUT}$ pin. It is measured in nV/√Hz.

**NOTES:**


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## PRODUCT IDENTIFICATION SYSTEM

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| PART NO. | X(1) | - | X | /XX |
|---|---|---|---|---|
| Device | Tape and Reel | | Temperature Range | Package |

| | | |
|---|---|---|
| **Device:** | MCP47CXBXX: | 1 LSb INL Voltage Output Digital-to-Analog Converters with $I^2C$ Interface, 8/10/12-Bit Resolution, Single/Dual Outputs and Volatile/MTP Memory |
| **Tape and Reel:** | T = | Tape and Reel |
| **Temperature Range:** | E = | -40°C to +125°C (Extended) |
| **Package:** | MF = | Plastic Dual Flat, No Lead Package (DFN), 3x3x0.9 mm, 10-Lead |
| | MG = | Plastic Quad Flat, No Lead Package (QFN), 3x3x0.9 mm, 16-Lead |
| | UN = | Plastic Micro Small Outline Package (MSOP), 10-Lead |

**Examples:**

a) MCP47CVB01-E/MF: 1 LSb INL Voltage Output Digital-to-Analog Converter, 8-Bit Resolution, Extended Temperature, 10LD DFN, with Volatile Memory.

b) MCP47CVB01T-E/MF: 1 LSb INL Voltage Output Digital-to-Analog Converter, 8-Bit Resolution, Tape and Reel, Extended Temperature, 10LD DFN, with Volatile Memory.

a) MCP47CVB12-E/MG: 1 LSb INL Voltage Output Digital-to-Analog Converter, 10-Bit Resolution, Extended Temperature, 16LD QFN, with Volatile Memory.

b) MCP47CVB12T-E/MG: 1 LSb INL Voltage Output Digital-to-Analog Converter, 10-Bit Resolution, Tape and Reel, Extended Temperature, 16LD QFN, with Volatile Memory.

a) MCP47CMB21-E/UN: 1 LSb INL Voltage Output Digital-to-Analog Converter, 12-Bit Resolution, Extended Temperature, 10LD MSOP, with Nonvolatile Memory.

b) MCP47CMB21T-E/UN: 1 LSb INL Voltage Output Digital-to-Analog Converter, 12-Bit Resolution, Tape and Reel, Extended Temperature, 10LD MSOP, with Nonvolatile Memory.

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