MIC2085

Single-Channel Low Voltage Hot Swap Controller

Features

- Pin-for-Pin Functional Equivalent to the LTC1642
- 2.3V to 16.5V Supply Voltage Operation
- Surge Voltage Protection to 33V
- Operating Temperature Range –40°C to +85°C
- Active Current Regulation Limits Inrush Current Independent of Load Capacitance
- Programmable Inrush Current Limiting
- Analog Foldback Current Limiting
- Electronic Circuit Breaker
- Dual-Level Overcurrent Fault Sensing
- Fast Response to Short-Circuit Conditions (<1µs)
- Programmable Output Undervoltage Detection
- Undervoltage Lockout Protection
- Power-On Reset
- /FAULT Status Output
- Driver for SCR Crowbar on Overvoltage

Applications

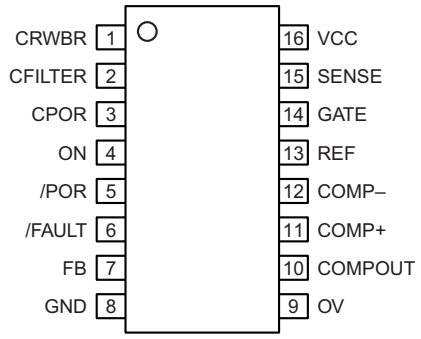
- RAID Systems
- Cellular Base Stations
- LAN Servers
- WAN Servers
- InfiniBand™ Systems
- Industrial High-Side Switching

General Description

The MIC2085 is a single channel, positive voltage, hot swap controller designed to allow the safe insertion of boards into live system backplanes. The MIC2085 is available in a 16-pin QSOP package. Using a few external components and by controlling the gate drive of an external N-Channel MOSFET device, the MIC2085 provides inrush current limiting and output voltage slew rate control in harsh, critical power supply environments. Additionally, a circuit breaker function will latch the output MOSFET off if the current limit threshold is exceeded for a programmed period of time. The device's array of features provide a simplified yet robust solution for many network applications in meeting the power supply regulation requirements and affords protection of critical downstream devices and components.

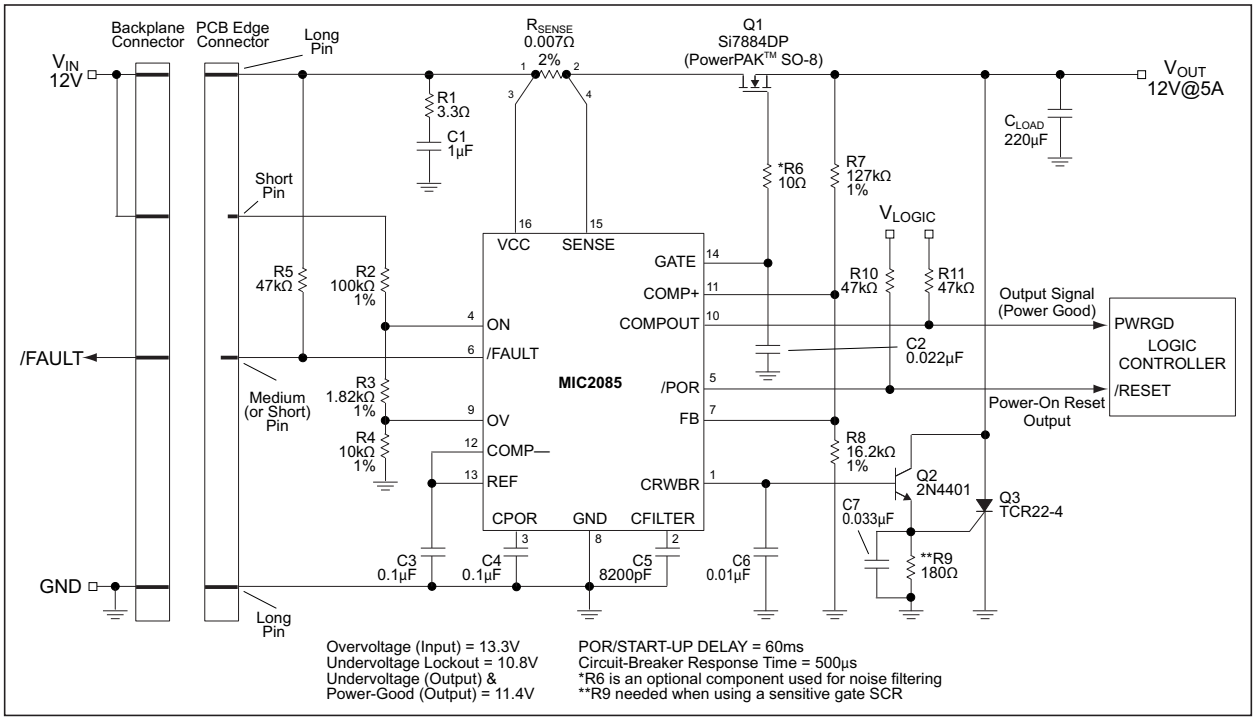
Package Type

MIC2085
16-Lead QSOP (QS)
(Top View)

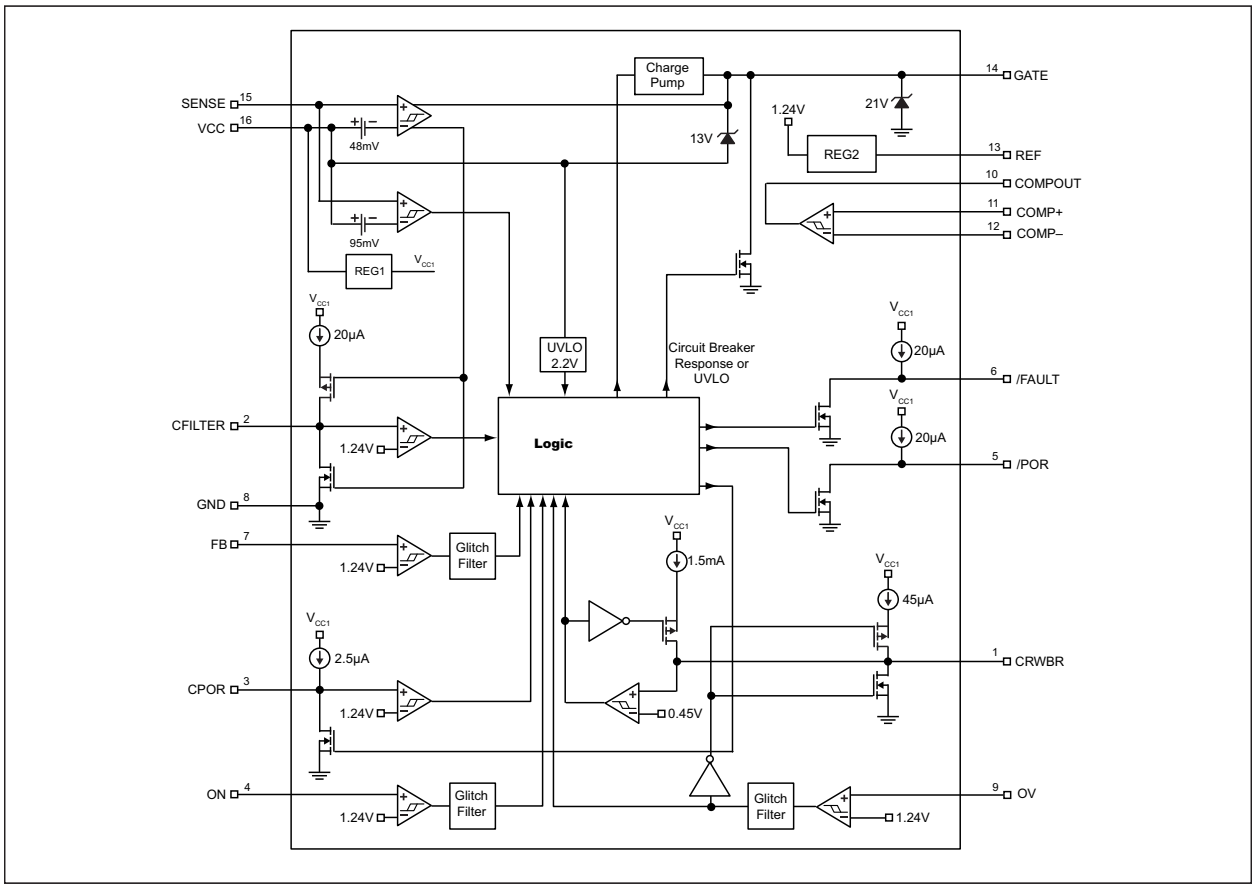


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Typical Application Circuit



Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

(All voltages are referred to GND)

Supply Voltage (V_{CC}) ..... –0.3V to +33V
SENSE Pin ..... –0.3 to V_{CC}+0.3V
GATE Pin ..... –0.3V to +22V
ON, /POR, /FAULT, COMP+, COMP–, COMPOUT ..... –0.3V to +20V
CRWBR, FB, OV, REF ..... –0.3V to +6V
Digital Output Pins (/POR, /FAULT, COMPOUT) ..... 10 mA
ESD Rating (HBM) ..... 2 kV
ESD Rating (MM) 200V

Operating Ratings ††

Supply Voltage (V_{CC}) ..... +2.3V to +16.5V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† Notice: The device is not guaranteed to function outside its operating ratings.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 5.0V; T_A = +25°C, unless otherwise noted. **Bold** indicates specifications over the full operating temperature range of –40°C to +85°C. Note 1

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{CC}	**2.3**	—	**16.5**	V	—
Supply Current	I_{CC}	—	1.6	**2.5**	mA	—
Undervoltage Lockout Threshold	V_{UVLO}	**2.05**	2.18	**2.28**	V	V_{CC} rising
		1.85	2.0	**2.10**		V_{CC} falling
UV Lockout Hysteresis	V_{UVHYST}	—	180	—	mV	—
FB (Power Good) Threshold Voltage	V_{FB}	**1.19**	1.24	**1.29**	V	FB rising
FB Hysteresis	V_{FBHYST}	—	3	—	mV	—
OV Pin Threshold Voltage	V_{OV}	**1.19**	1.24	**1.29**	mV	OV pin rising
OV Pin Threshold Voltage Line Regulation	ΔV_{OV}	—	5	**15**	mV	2.3V < V_{CC} < 16.5V
OV Pin Hysteresis	V_{OVHYST}	—	3	—	mV	—
OV Pin Current	I_{OV}	—	—	**0.2**	µA	—
POR Delay and Overcurrent (CFILTER) Timer Threshold	V_{TH}	**1.19**	1.24	**1.29**	V	V_{CPOR}, $V_{CFILTER}$ rising
Power-On Reset Timer Current	I_{CPOR}	**–2.5**	–2.0	**–1.5**	µA	Timer on
		—	5	—	mA	Timer off
Current Limit /Overcurrent Timer Current (CFILTER)	I_{TIMER}	**–30**	–20	**–15**	µA	Timer on
		—	2.5	—	mA	Timer off

Note 1: Specification for packaged product only.

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{CC} = 5.0V; T_A = +25°C, unless otherwise noted. **Bold** indicates specifications over the full operating temperature range of –40°C to +85°C. Note 1

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
CRWBR Pin Threshold Voltage	V_{CR}	445	470	495	mV	2.3V < V_{CC} < 16.5V
CRWBR Pin Threshold Voltage Line Regulation	ΔV_{CR}	—	4	**15**	µA	2.3V < V_{CC} < 16.5V
CRWBR Pin Current	I_{CR}	**–60**	–45	**–30**	µA	CRWBR On, V_{CRWBR} = 0V
		—	–1.5	–1.0	mA	CRWBR On, V_{CRWBR} = 2.1V
		—	3.3	—	mA	CRWBR Off, V_{CRWBR} = 1.5V
Circuit Breaker Trip Voltage (Current Limit Threshold)	V_{TRIP}	**40**	48	**55**	mV	V_{TRIP} = V_{CC} = V_{SENSE}, $V_{TRIPSLOW}$
		80	95	**110**		2.3V ≤ V_{CC} ≤ 16.5V, $V_{TRIPFAST}$, x = J
		—	150	—		2.3V ≤ V_{CC} ≤ 16.5V, $V_{TRIPFAST}$, x = K
		—	200	—		2.3V ≤ V_{CC} ≤ 16.5V, $V_{TRIPFAST}$, x = L
External Gate Drive	V_{GS}	4	8	9	V	V_{GATE} – V_{CC}, V_{CC} < 3V
		11	12	13		V_{GATE} – V_{CC}, 5V < V_{CC} < 9V
		4.5	21 – V_{CC}	13		V_{GATE} – V_{CC}, 9V < V_{CC} < 15.0V
GATE Pin Pull-Up Current	I_{GATE}	**–22**	–16	**–8**	µA	Start cycle, V_{GATE} > 0V, V_{CC} = 16.5V
		–20	–14	**–8**		Start cycle, V_{GATE} > 0V, V_{CC} = 2.3V
GATE Pin Sink Current	$I_{GATEOFF}$	**25**	50	—	mA	/FAULT = 0, V_{GATE} > 1V, V_{CC} = 16.5V
		12	20	—		/FAULT = 0, V_{GATE} > 1V, V_{CC} = 2.3V
ON Pin Threshold Voltage	V_{ON}	**1.19**	1.24	**1.29**	V	ON rising
		1.09	1.14	1.19		ON falling
ON Pin Hysteresis	V_{ONHYST}	—	100	—	mV	—
ON Pin Input Current	I_{ON}	—	—	**0.5**	µA	V_{ON} = V_{CC}
Undervoltage Start-Up Timer Threshold	V_{START}	**1.19**	1.24	**1.29**	V	V_{CPOR} rising
/FAULT, /POR Output Voltage	V_{OL}	—	—	**0.4**	V	I_{OUT} = 1.6 mA
Output Signal Pull-Up Current /FAULT, /POR, COMPOUT	I_{PULLUP}	—	–20	—	µA	/FAULT, /POR = GND
Reference Output Voltage	V_{REF}	1.21	1.24	1.27	V	I_{LOAD} = 0 mA; C_{REF} = 0.1 µF
Reference Line Regulation	ΔV_{LNR}	—	5	**10**	mV	2.3V < V_{CC} < 16.5V
Reference Load Regulation	ΔV_{LDR}	—	2.5	**7.5**	mV	I_{OUT} = 1 mA
Reference Short-Circuit Current	I_{RSC}	—	3.5	—	mA	V_{REF} = 0V
Comparator Offset Voltage	V_{COS}	**–5**	—	**5**	mV	V_{CM} = V_{REF}
Comparator Hysteresis	V_{CHYST}	—	3	—	mV	V_{CM} = V_{REF}

Note 1: Specification for packaged product only.

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AC ELECTRICAL CHARACTERISTICS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Fast Overcurrent Sense to GATE Low Trip Time	t_{OCFAST}	—	1	—	µs	V_{CC} = 5V $V_{CC} - V_{SENSE}$ = 100 mV C_{GATE} = 10 nF, See Figure 1-1
Slow Overcurrent Sense to GATE Low Trip Time	t_{OCSLOW}	—	5	—	µs	V_{CC} = 5V $V_{CC} - V_{SENSE}$ = 50 mV C_{GATE} = 0 nF, See Figure 1-1
ON Delay Filter	t_{ONDLY}	—	20	—	µs	—
FB Delay Filter	t_{FBDLY}	—	20	—	µs	—

Note 1: Specification for packaged product only.

Timing Diagrams

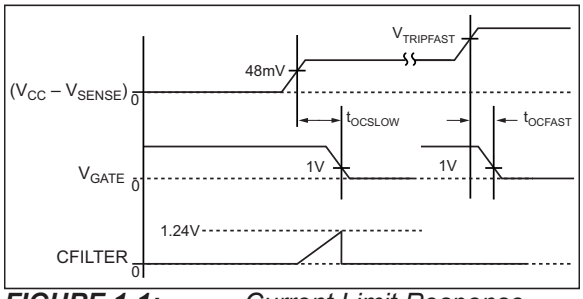


FIGURE 1-1: *Current Limit Response.*

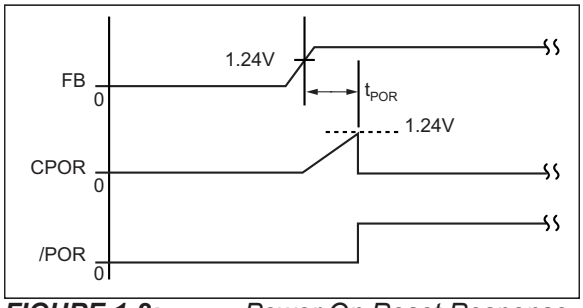


FIGURE 1-2: *Power-On Reset Response.*

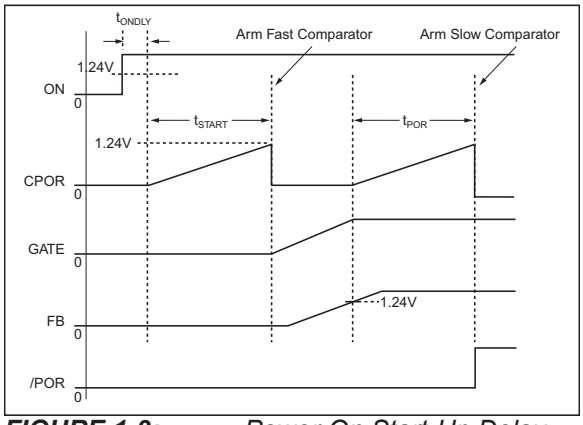


FIGURE 1-3: *Power-On Start-Up Delay Timing.*

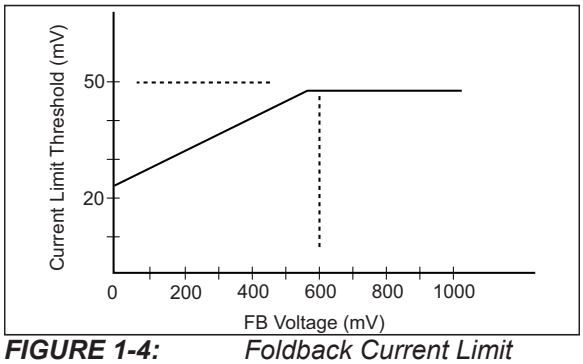


FIGURE 1-4: *Foldback Current Limit Response.*

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	—	–40	—	+85	°C	—
Maximum Junction Temperature	T_J	—	—	+125	°C	—
Package Thermal Resistances						
Thermal Resistance, QSOP 16-Ld	θ_{JA}	—	112	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

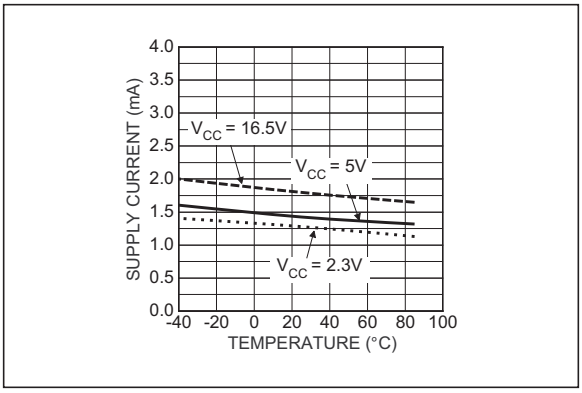


FIGURE 2-1: *Supply Current vs. Temperature.*

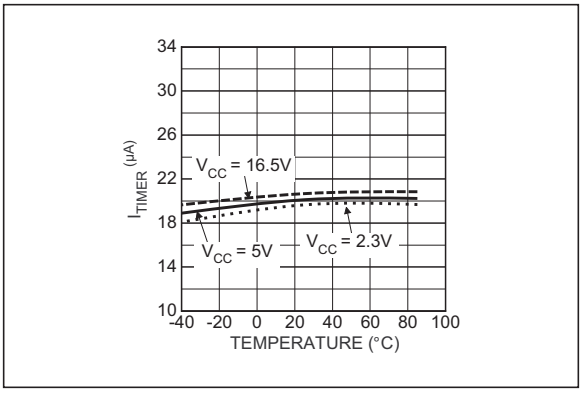


FIGURE 2-4: *Overcurrent Timer Current vs. Temperature.*

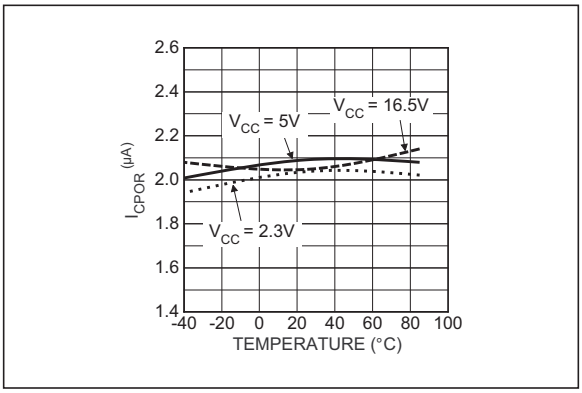


FIGURE 2-2: *Power-On Reset Timer Current vs. Temperature.*

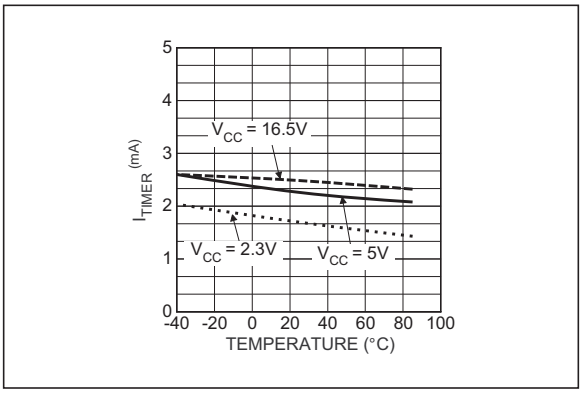


FIGURE 2-5: *Overcurrent Timer (Off) Current vs. Temperature.*

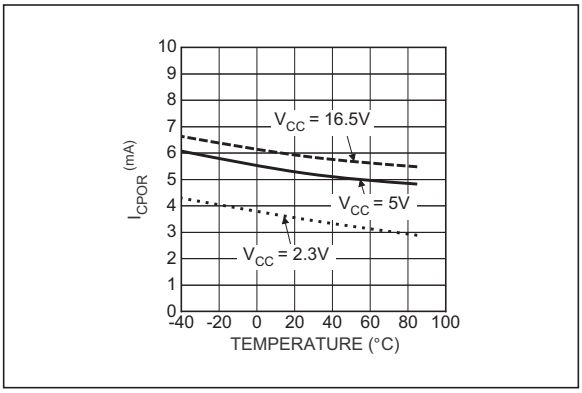


FIGURE 2-3: *Power-On Reset Timer (Off) Current vs. Temperature.*

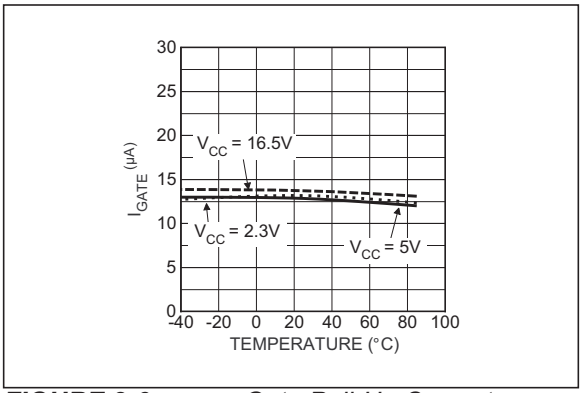


FIGURE 2-6: *Gate Pull-Up Current vs. Temperature.*

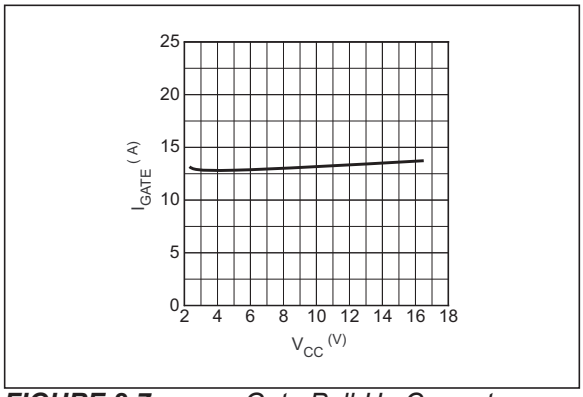


FIGURE 2-7: *Gate Pull-Up Current vs V_{CC}.*

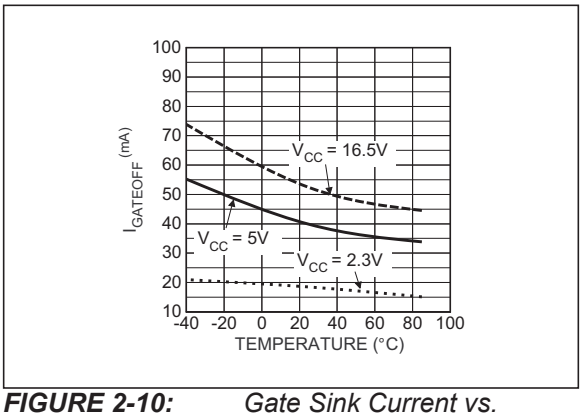


FIGURE 2-10: *Gate Sink Current vs. Temperature.*

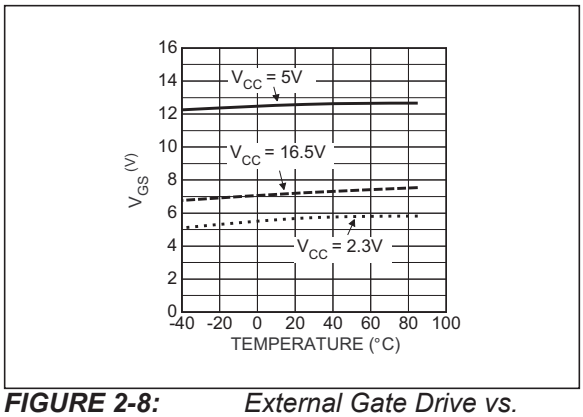


FIGURE 2-8: *External Gate Drive vs. Temperature.*

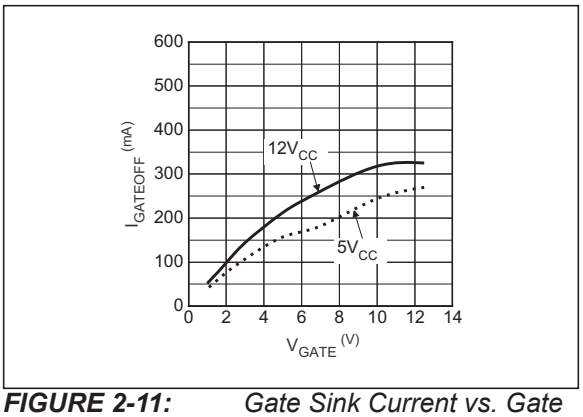


FIGURE 2-11: *Gate Sink Current vs. Gate Voltage.*

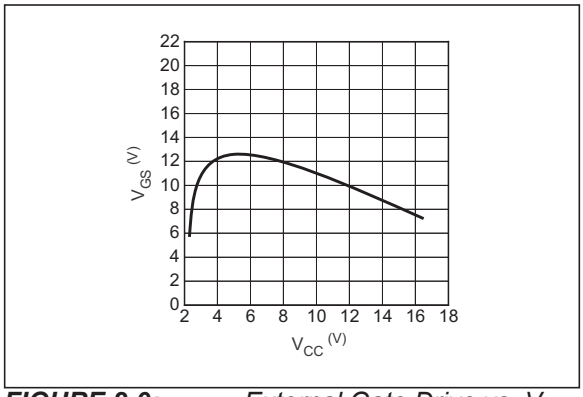


FIGURE 2-9: *External Gate Drive vs. V_{CC}.*

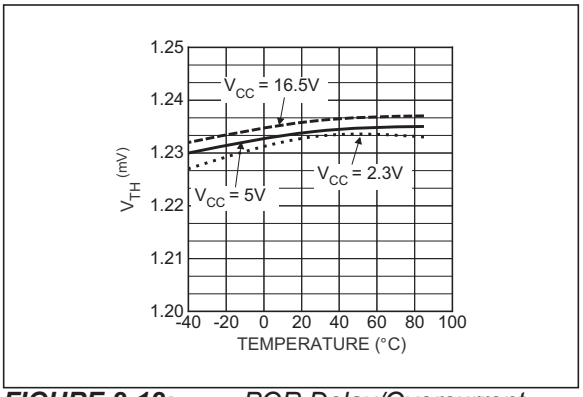


FIGURE 2-12: *POR Delay/Overcurrent Timer Threshold vs. Temperature.*

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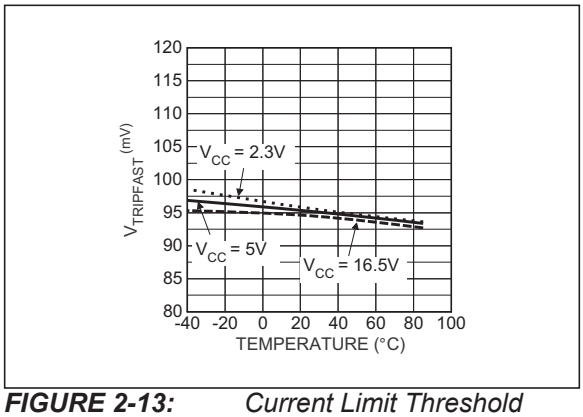


FIGURE 2-13: *Current Limit Threshold (Fast Trip) vs. Temperature.*

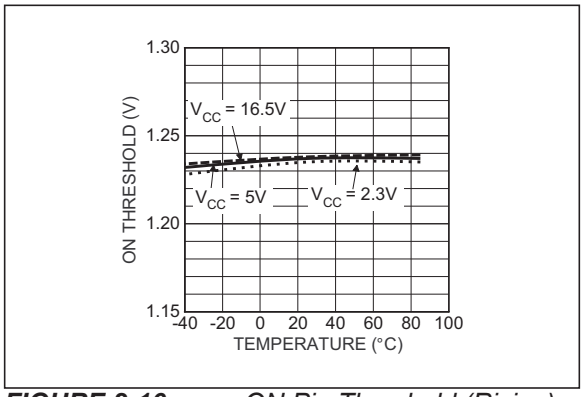


FIGURE 2-16: *ON Pin Threshold (Rising) vs. Temperature.*

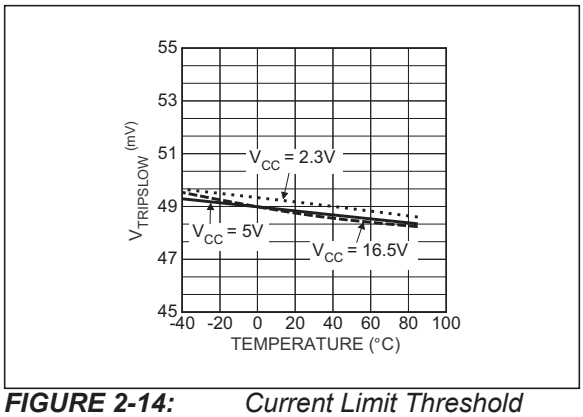


FIGURE 2-14: *Current Limit Threshold (Slow Trip) vs. Temperature.*

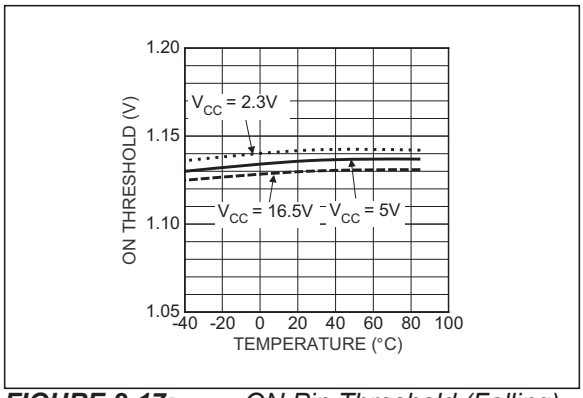


FIGURE 2-17: *ON Pin Threshold (Falling) vs. Temperature.*

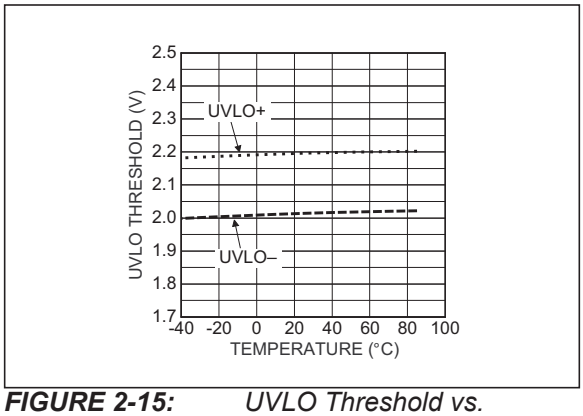


FIGURE 2-15: *UVLO Threshold vs. Temperature.*

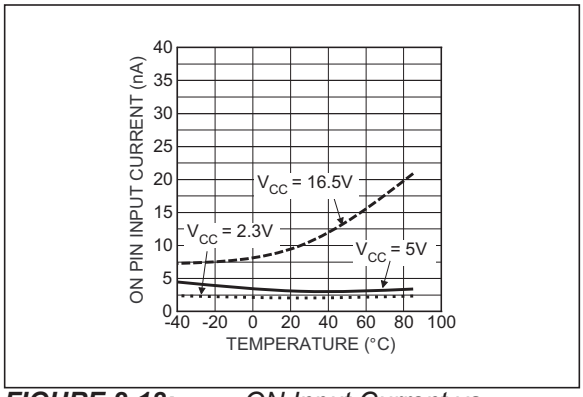


FIGURE 2-18: *ON Input Current vs. Temperature.*

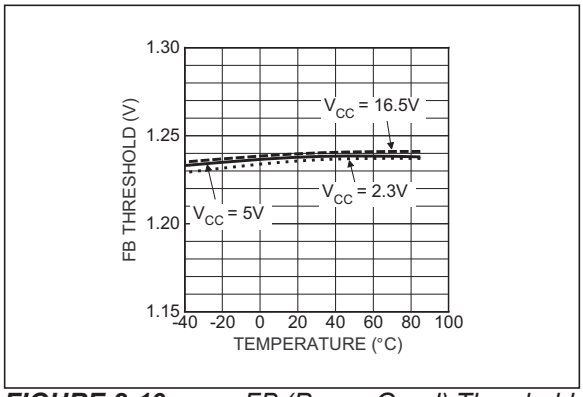


FIGURE 2-19: *FB (Power Good) Threshold vs. Temperature.*

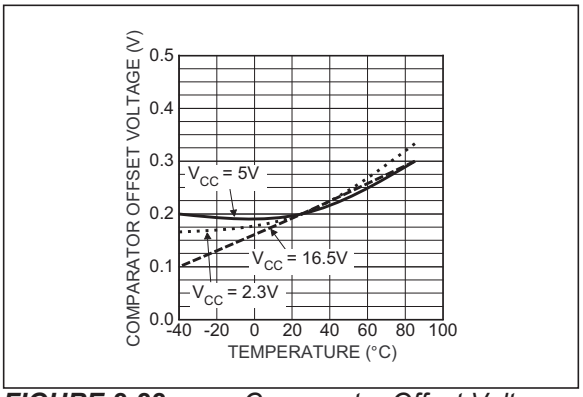


FIGURE 2-22: *Comparator Offset Voltage vs. Temperature.*

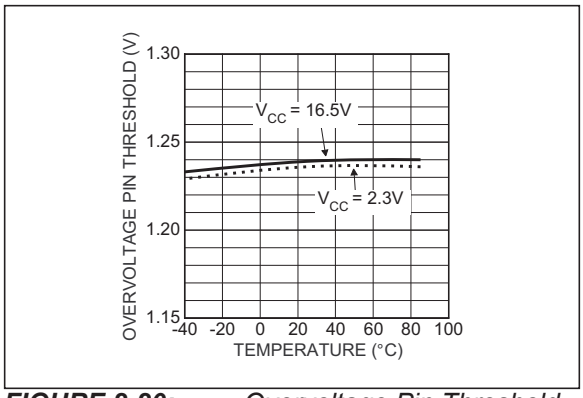


FIGURE 2-20: *Overvoltage Pin Threshold vs. Temperature.*

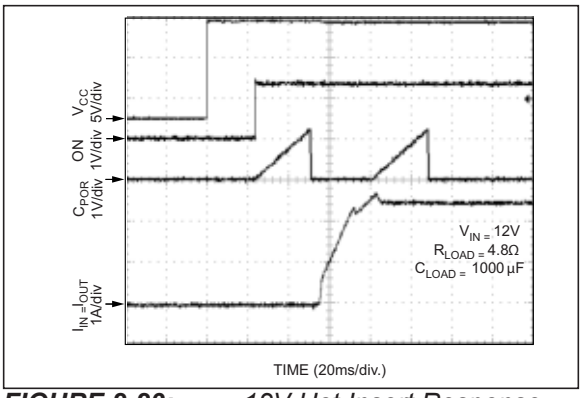


FIGURE 2-23: *12V Hot Insert Response.*

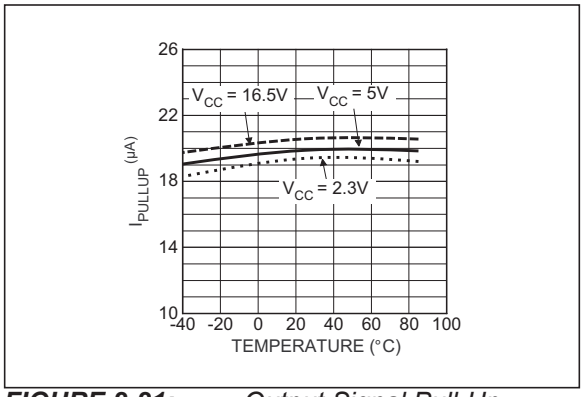


FIGURE 2-21: *Output Signal Pull-Up Current vs. Temperature.*

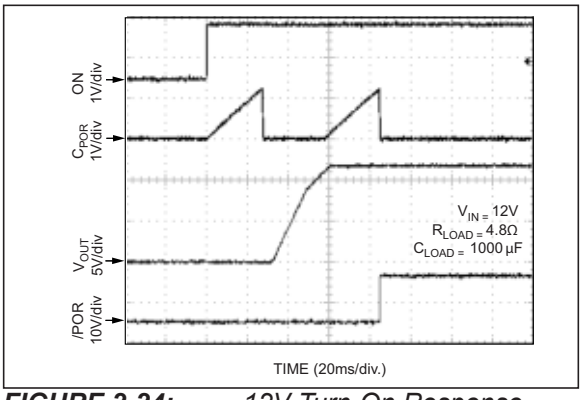


FIGURE 2-24: *12V Turn-On Response.*

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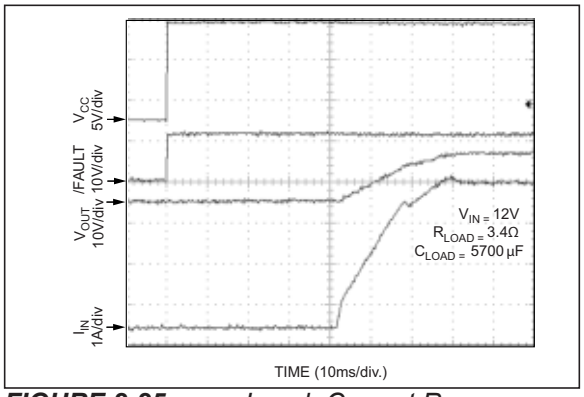


FIGURE 2-25: *Inrush Current Response.*

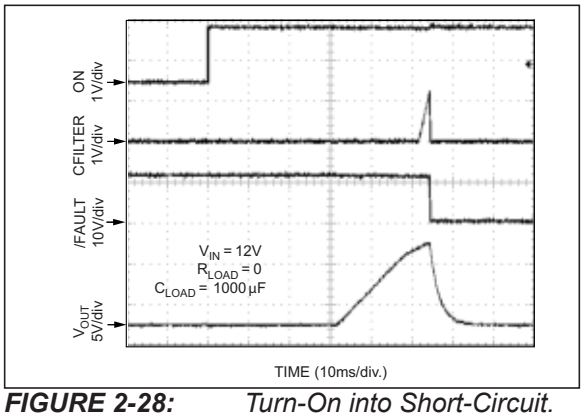


FIGURE 2-28: *Turn-On into Short-Circuit.*

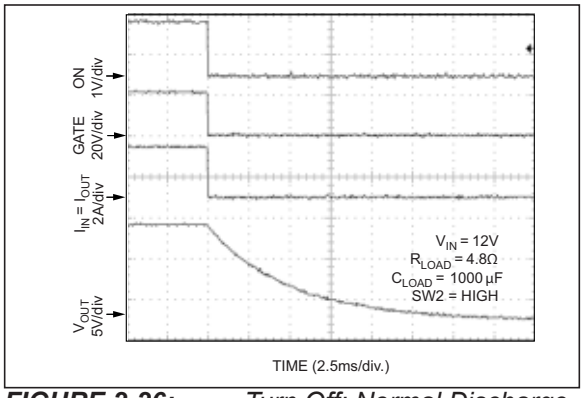


FIGURE 2-26: *Turn Off: Normal Discharge.*

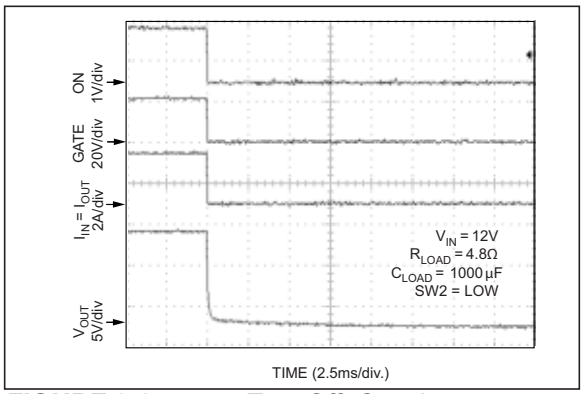


FIGURE 2-27: *Turn Off: Crowbar Discharge.*

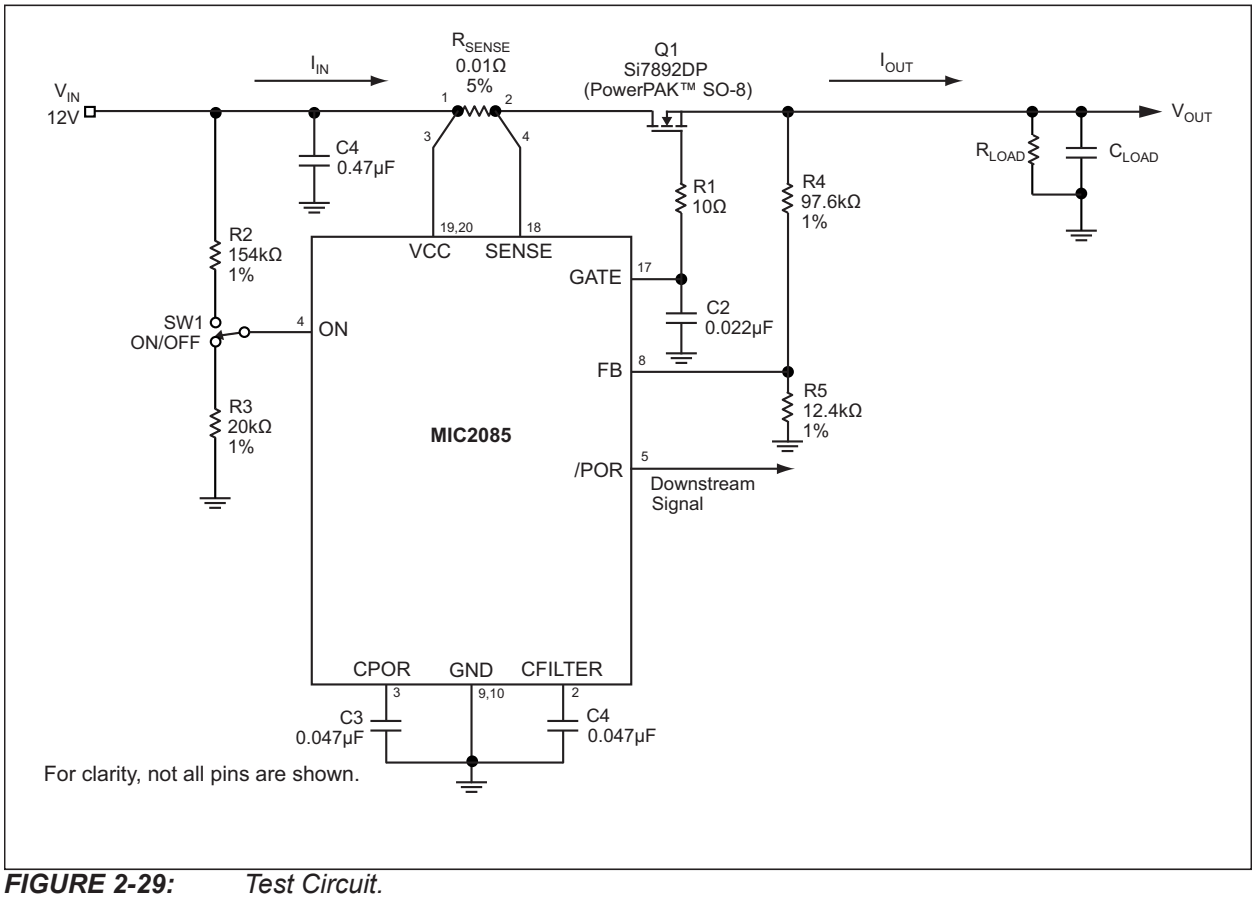


FIGURE 2-29: *Test Circuit.*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number MIC2085	Pin Name	Description
1	CRWBR	Overvoltage Timer and Crowbar Circuit Trigger: A capacitor connected to this pin sets the timer duration for which an overvoltage condition will trigger an external crowbar circuit. This timer begins when the OV input rises above its threshold as an internal 45 µA current source charges the capacitor. Once the voltage reaches 470 mV, the current increases to 1.5 mA.
2	CFILTER	Current Limit Response Timer: A capacitor connected to this pin defines the period of time (t_{OCSLOW}) in which an overcurrent event must last to signal a fault condition and trip the circuit breaker. If no capacitor is connected, then t_{OCSLOW} defaults to 5 µs.
3	CPOR	Power-On Reset Timer: A capacitor connected between this pin and ground sets the start-up delay (t_{START}) and the power-on reset interval (t_{POR}). When V_{CC} rises above the UVLO threshold, the capacitor connected to CPOR begins to charge. When the voltage at CPOR crosses 1.24V, the start-up threshold (V_{START}), a start cycle is initiated if ON is asserted while capacitor CPOR is immediately discharged to ground. When the voltage at FB rises above V_{FB}, capacitor CPOR begins to charge again. When the voltage at CPOR rises above the power-on reset delay threshold (V_{TH}), the timer resets by pulling CPOR to ground, and /POR is deasserted. If CPOR = 0, then t_{START} defaults to 20 µs.
4	ON	ON Input: Active-high. The ON pin, an input to a Schmitt-triggered comparator used to enable/disable the controller, is compared to a V_{TH} reference with 100 mV of hysteresis. Once a logic high is applied to the ON pin (V_{ON} > 1.24V), a start-up sequence is initiated as the GATE pin starts ramping up towards its final operating voltage. When the ON pin receives a low logic signal (V_{ON} < 1.14V), the GATE pin is grounded and /FAULT is high if V_{CC} is above the UVLO threshold. ON must be low for at least 20 µs in order to initiate a start-up sequence. Additionally, toggling the ON pin LOW to HIGH resets the circuit breaker.
5	/POR	Power-On Reset Output: Open-drain N-Channel device, active-low. This pin remains asserted during start-up until a time period t_{POR} after the FB pin voltage rises above the power good threshold (V_{FB}). The timing capacitor CPOR determines t_{POR}. When an output undervoltage condition is detected at the FB pin, /POR is asserted for a minimum of one timing cycle, t_{POR}. The /POR pin has a weak pull-up to V_{CC}.
6	/FAULT	Circuit Breaker Fault Status Output: Open-drain N-Channel device, active-low. The /FAULT pin is asserted when the circuit breaker trips due to an overcurrent condition. Also, this pin indicates undervoltage lockout and overvoltage fault conditions. The /FAULT pin has a weak pull-up to V_{CC}.
7	FB	Power Good Threshold Input: This input is internally compared to a 1.24V reference with 3 mV of hysteresis. An external resistive divider may be used to set the voltage at this pin. If this input momentarily goes below 1.24V, then /POR is activated for one timing cycle, t_{POR}, indicating an output undervoltage condition. The /POR signal deasserts one timing cycle after the FB pin exceeds the power good threshold by 3 mV. A 5 µs filter on this pin prevents glitches from inadvertently activating this signal.
8	GND	Ground Connection: Tie to analog ground
9	OV	OV Input: When the voltage on OV exceeds its trip threshold, the GATE pin is pulled low and the CRWBR timer starts. If OV remains above its threshold long enough for CRWBR to reach its trip threshold, the circuit breaker is tripped. Otherwise, the GATE pin begins to ramp up one POR timing cycle after OV drops below its trip threshold.

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TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number MIC2085	Pin Name	Description
10	COMPOUT	Uncommitted Comparator's Open-Drain Output.
11	COMP+	Comparator's Non-Inverting Input.
12	COMP–	Comparator's Inverting Input.
13	REF	Reference Output: 1.24V nominal. Tie a 0.1 µF capacitor to ground to ensure stability.
14	GATE	Gate Drive Output: Connects to the gate of an external N-Channel MOSFET. An internal clamp ensures that no more than 13V is applied between the GATE pin and the source of the external MOSFET. The GATE pin is immediately brought low when either the circuit breaker trips or an undervoltage lockout condition occurs.
15	SENSE	Circuit Breaker Sense Input: A resistor between this pin and VCC sets the current limit threshold. Whenever the voltage across the sense resistor exceeds the slow trip current limit threshold ($V_{TRIPSLOW}$), the GATE voltage is adjusted to ensure a constant load current. If $V_{TRIPSLOW}$ (48 mV) is exceeded for longer than time period t_{OCSLOW}, then the circuit breaker is tripped and the GATE pin is immediately pulled low. If the voltage across the sense resistor exceeds the fast trip circuit breaker threshold, $V_{TRIPFAST}$, at any point due to fast, high amplitude power supply faults, then the GATE pin is immediately brought low without delay. To disable the circuit breaker, the SENSE and VCC pins can be tied together. The default $V_{TRIPFAST}$ for either device is 95 mV. Other fast trip thresholds are available: 150 mV, 200 mV, or OFF ($V_{TRIPFAST}$ disabled). Please contact Microchip for availability of other options.
16	VCC	Positive Supply Input: 2.3V to 16.5V. The GATE pin is held low by an internal undervoltage lockout circuit until V_{CC} exceeds a threshold of 2.18V.If V_{CC} exceeds 16.5V, an internal shunt regulator protects the chip from VCC and SENSE pin voltages up to 33V.

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4.0 FUNCTIONAL DESCRIPTION

4.1 Hot Swap Insertion

When circuit boards are inserted into live system backplanes and supply voltages, high inrush currents can result due to the charging of bulk capacitance that resides across the supply pins of the circuit board. This inrush current, although transient in nature, may be high enough to cause permanent damage to on-board components or may cause the system's supply voltages to go out of regulation during the transient period which may result in system failures. The MIC2085 acts as a controller for external N-Channel MOSFET devices in which the gate drive is controlled to provide inrush current limiting and output voltage slew rate control during hot plug insertions.

4.2 Power Supply

V_{CC} is the supply input to the MIC2085 controller with a voltage range of 2.3V to 16.5V. The V_{CC} input can withstand transient spikes up to 33V. In order to help suppress transients and ensure stability of the supply voltage, a capacitor of 1.0 µF to 10 µF from V_{CC} to ground is recommended. Alternatively, a low pass filter, shown in the typical application circuit, can be used to eliminate high frequency oscillations as well as help suppress transient spikes.

4.3 Start-Up Cycle

When the voltage on the ON pin rises above its threshold of 1.24V, the MIC2085/6 first checks that its supply (V_{CC}) is above the UVLO threshold. If it does check above, the device is enabled and an internal 2 µA current source begins charging capacitor CPOR to 1.24V to initiate a start-up sequence (i.e., start-up delay times out). Once the start-up delay (t_{START}) elapses, CPOR is pulled immediately to ground and a 15 µA current source begins charging the GATE output to drive the external MOSFET that switches V_{IN} to V_{OUT}. The programmed start-up delay is calculated using the following equation:

EQUATION 4-1:

$$t_{START} = C_{POR} \times \frac{V_{TH}}{I_{CPOR}} \cong 0.62 \times C_{POR}(\mu F)$$

Where:
V_{TH} = 1.24V, the POR delay threshold.
I_{CPOR} = 2 µA, the POR timer current.

As the GATE voltage continues ramping toward its final value (V_{CC} + V_{GS}) at a defined slew rate (See the Load Capacitance Dominated Start-Up/Gate Capacitance Dominated Start-Up sections), a second CPOR timing cycle begins if:

1. /FAULT is high and
2. CFILTER is low (i.e., not an overvoltage, under-voltage lockout, or overcurrent state).

This second timing cycle, t_{POR}, starts when the voltage at the FB pin exceeds its threshold (V_{FB}) indicating that the output voltage is valid. The time period t_{POR} is equivalent to t_{START} and sets the interval for the /POR to go Low-to-High after power is good (See Figure 1-2). Active current regulation is employed to limit the inrush current transient response during start-up by regulating the load current at the programmed current limit value See the Current Limiting and Dual-Level Circuit Breaker section. The following equation is used to determine the nominal current limit value:

EQUATION 4-2:

$$I_{LIM} = \frac{V_{TRIPSLOW}}{R_{SENSE}} = \frac{48mV}{R_{SENSE}}$$

Where:
$V_{TRIPSLOW}$ = The current limit slow trip threshold found in Electrical Characteristics.
R_{SENSE} = The selected value that will set the desired current limit.

There are two basic start-up modes for the MIC2085/6:

- Start-up dominated by load capacitance.
- Start-up dominated by total gate capacitance.

The magnitude of the inrush current delivered to the load will determine the dominant mode. If the inrush current is greater than the programmed current limit (I_{LIM}), then load capacitance is dominant. Otherwise, gate capacitance is dominant. The expected inrush current may be calculated using the following equation:

EQUATION 4-3:

$$INRUSH \cong I_{GATE} \times \frac{C_{LOAD}}{C_{GATE}} \cong 15\mu A \times \frac{C_{LOAD}}{C_{GATE}}$$

Where:
I_{GATE} = The pin pull-up current.
C_{LOAD} = The load capacitance.
C_{GATE} = The total GATE capacitance (C_{ISS} of the external MOSFET and any external capacitor connected from the MIC2085/6 GATE pin to ground).

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4.3.1 LOAD CAPACITANCE DOMINATED START-UP

In this case, the load capacitance, C_{LOAD}, is large enough to cause the inrush current to exceed the programmed current limit, but is less than the fast-trip threshold (or the fast-trip threshold is disabled, 'M' option). During start-up under this condition, the load current is regulated at the programmed current limit value (I_{LIM}) and held constant until the output voltage rises to its final value. The output slew rate and equivalent GATE voltage slew rate is computed by the following equation:

EQUATION 4-4:

$$dV_{OUT}/dt = \frac{I_{LIM}}{C_{LOAD}}$$

Where:
I_{LIM} = The programmed current limit value.

Consequently, the value of CFILTER must be selected to ensure that the overcurrent response time, t_{OCSLOW}, exceeds the time needed for the output to reach its final value. For example, given a MOSFET with an input capacitance C_{ISS} = C_{GATE} = 4700 pF, C_{LOAD} is 2200 µF, and I_{LIM} is set to 6A with a 12V input, then the load capacitance dominates as determined by the calculated INRUSH > I_{LIM}. Therefore, the output voltage slew rate determined from Equation 4-4 is:

EQUATION 4-5:

$$dV_{OUT}/dt = \frac{6A}{2200\mu F} = 2.73V/\text{ms}$$

The resulting t_{OCSLOW} needed to achieve a 12V output is approximately 4.5 ms. See the Power-On Reset, Start-Up, and Overcurrent Timer Delays section to calculate t_{OCSLOW}.

4.3.2 GATE CAPACITANCE DOMINATED START-UP

In this case, the value of the load capacitance relative to the GATE capacitance is small enough such that the load current during start-up never exceeds the current limit threshold as determined by Equation 4-3. The minimum value of C_{GATE} that will ensure that the current limit is never exceeded is given by the equation below:

EQUATION 4-6:

$$C_{GATE(MIN)} = \frac{I_{GATE}}{I_{LIM}} \times C_{LOAD}$$

Where:
C_{GATE} = The sum of the MOSFET input capacitance (C_{ISS}) and the value of the external capacitor connected to the GATE pin of the MOSFET.

Once C_{GATE} is determined, use the following equation to determine the output slew rate for gate capacitance dominated start-up.

EQUATION 4-7:

$$dV_{OUT}/dt(OUTPUT) = \frac{I_{GATE}}{C_{GATE}}$$

Table 4-1 depicts the output slew rate for various values of C_{GATE}.

TABLE 4-1: OUTPUT SLEW RATE SELECTION FOR GATE CAPACITANCE DOMINATED START-UP

C_{GATE}	Output Slew Rate
0.001 µF	15 V/ms
0.01 µF	1.5 V/ms
0.1 µF	0.150 V/ms
1 µF	0.015 V/ms

Note 1: I_{GATE} = 15 µA.

4.4 Current Limiting and Dual-Level Circuit Breaker

Many applications will require that the inrush and steady state supply current be limited at a specific value in order to protect critical components within the system. Connecting a sense resistor between the V_{CC} and SENSE pins sets the nominal current limit value of the MIC2085 and the current limit is calculated using Equation 4-2. However, the MIC2085 exhibits foldback current limit response. The foldback feature allows the nominal current limit threshold to vary from 24 mV up to 48 mV as the FB pin voltage increases or decreases. When FB is at 0V, the current limit threshold is 24 mV and for FB ≥ 0.6V, the current limit threshold is the nominal 48 mV (see Figure 1-4 for Foldback Current Limit Response characteristic). The MIC2085 also features a dual-level circuit breaker triggered via 48 mV and 95 mV current limit thresholds sensed across the V_{CC} and SENSE pins.

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The first level of the circuit breaker functions as follows. Once the voltage sensed across these two pins exceeds 48 mV, the overcurrent timer, its duration set by capacitor CFILTER, starts to ramp the voltage at CFILTER using a 2 µA constant current source. If the voltage at CFILTER reaches the overcurrent timer threshold (V_{TH}) of 1.24V, then CFILTER immediately returns to ground as the circuit breaker trips and the GATE output is immediately shut down.

For the second level, if the voltage sensed across V_{CC} and SENSE exceeds 95 mV at any time, the circuit breaker trips and the GATE shuts down immediately, bypassing the overcurrent timer period. To disable current limit and circuit breaker operation, tie the SENSE and V_{CC} pins together and the CFILTER pin to ground.

4.5 Output Undervoltage Detection

The MIC2085 employs output undervoltage detection by monitoring the output voltage through a resistive divider connected at the FB pin. During turn-on, while the voltage at the FB pin is below the threshold (V_{FB}), the /POR pin is asserted low. Once the FB pin voltage crosses V_{FB}, a 2 µA current source charges capacitor C_{POR}. Once the C_{POR} pin voltage reaches 1.24V, the time period t_{POR} elapses as the C_{POR} pin is pulled to ground and the /POR pin goes high. If the voltage at FB drops below V_{FB} for more than 10 µs, the /POR pin resets for at least one timing cycle defined by t_{POR} (see Application Information for an example).

4.6 Input Overvoltage Protection

The MIC2085 monitors and detects overvoltage conditions in the event of excessive supply transients at the input. Whenever the overvoltage threshold (V_{OV}) is exceeded at the OV pin, the GATE is pulled low and the output is shut off. The GATE will begin ramping one POR timing cycle after the OV pin voltage drops below its threshold. An external CRWBR circuit, as shown in the Typical Application Circuit, provides a time period that an overvoltage condition must exceed in order to trip the circuit breaker. When the OV pin exceeds the overvoltage threshold (V_{OV}), the CRWBR timer begins charging the CRWBR capacitor initially with a 45 µA current source.Once the voltage at CRWBR exceeds its threshold (V_{CR}) of 0.47V, the CRWBR current immediately increases to 1.5 mA and the circuit breaker is tripped, necessitating a device reset by toggling the ON pin from low to high.

4.7 Power-On Reset, Start-Up, and Overcurrent Timer Delays

The Power-On Reset delay, t_{POR}, is the time period for the /POR pin to go high once the voltage at the FB pin exceeds the power good threshold (V_{TH}). A capacitor connected to CPOR sets the interval, t_{POR}, and t_{POR} is equivalent to the start-up delay, t_{START} (see Equation 4-1).

A capacitor connected to CFILTER is used to set the timer that activates the circuit breaker during overcurrent conditions. When the voltage across the sense resistor exceeds the slow trip current limit threshold of 48 mV, the overcurrent timer begins to charge for a period, t_{OCSLOW}, determined by CFILTER. If no capacitor is used at CFILTER, then t_{OCSLOW} defaults to 5 µs. If t_{OCSLOW} elapses, then the circuit breaker is activated and the GATE output is immediately pulled to ground. The following equation is used to determine the overcurrent timer period, t_{OCSLOW}.

EQUATION 4-8:

$$t_{OCSLOW} = C_{FILTER} \times \frac{V_{TH}}{I_{TIMER}} \cong 0.062 \times C_{FILTER}(\mu F)$$

Where:
V_{TH} = The CFILTER timer threshold: 1.24V.
I_{TIMER} = The overcurrent timer current: 20 µA.

Table 4-2 and Table 4-3 provide a quick reference for several timer calculations using select standard value capacitors.

TABLE 4-2: SELECTED POWER-ON RESET AND START-UP DELAYS

C_{POR}	$t_{POR} = t_{START}$
0.01 µF	6 ms
0.02 µF	12 ms
0.033 µF	18.5 ms
0.05 µF	30 ms
0.1 µF	60 ms
0.33 µF	200 ms

TABLE 4-3: SELECTED OVERCURRENT TIMER DELAYS

C_{FILTER}	t_{OCSLOW}
1800 pF	100 µs
4700 pF	290 µs
8200 pF	500 µs
0.01 µF	620 µs
0.02 µF	1.2 ms
0.033 µF	2.0 ms
0.05 µF	3.0 ms
0.1 µF	6.2 ms
0.33 µF	20.7 ms

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5.0 APPLICATION INFORMATION

5.1 Output Undervoltage Detection

For output undervoltage detection, the first consideration is to establish the output voltage level that indicates “power is good.” For this example, the output value for which a 12V supply will signal “good” is 11V. Next, consider the tolerances of the input supply and FB threshold (V_{FB}). For this example, the 12V supply varies ±5%, thus the resulting output voltage may be as low as 11.4V and as high as 12.6V. Additionally, the FB threshold has ±50 mV tolerance and may be as low as 1.19V and as high as 1.29V. Thus, to determine the values of the resistive divider network (R5 and R6) at the FB pin, shown in Figure 5-1, use the following iterative design procedure.

1. Choose R6 so as to limit the current through the divider to approximately 100 µA or less.

EQUATION 5-1:

$$R6 \geq \frac{V_{FB(MAX)}}{100\mu A} \geq \frac{1.29V}{100\mu A} \geq 12.9k\Omega$$

R6 is chosen as 13.3 kΩ ±1%.

2. Next, determine R5 using the output “good” voltage of 11V and the following equation:

EQUATION 5-2:

$$V_{OUT(GOOD)} = V_{FB}\left[\frac{R5 + R6}{R6}\right]$$

Using some basic algebra and simplifying Equation 5-2 to isolate R5, yields:

EQUATION 5-3:

$$R5 = R6\left[\frac{V_{OUT(GOOD)}}{V_{FB(MAX)}} - 1\right]$$

Where:
$V_{FB(MAX)}$ = 1.29V.
$V_{OUT(GOOD)}$ = 11V.
R6 = 13.3 kΩ.

Substituting these values into Equation 5-3 now yields R5 = 100.11 kΩ. A standard 100 kΩ ±1% is selected. Now, consider the 11.4V minimum output voltage, the lower tolerance for R6 and higher tolerance for R5, 13.17 kΩ and 101 kΩ, respectively. With only 11.4V available, the voltage sensed at the FB pin exceeds $V_{FB(MAX)}$, thus the /POR signal will transition from low to high, indicating “power is good” given the worse case tolerances of this example.

5.2 Input Overvoltage Protection

The external CRWBR circuit shown in Figure 5-1 consists of capacitor C4, resistor R7, NPN transistor Q2, and SCR Q3. The capacitor establishes a time duration for an overvoltage condition to last before the circuit breaker trips. The CRWBR timer duration is approximated by the following equation:

EQUATION 5-4:

$$t_{OVCR} \cong \frac{C4 \times V_{CR}}{I_{CR}} \cong 0.01 \times C4(\mu F)$$

Where:
V_{CR} = The CRWBR pin threshold: 0.47V.
I_{CR} = The CRWBR pin current during the timer period: 45 µA.

See the CRWBR timer pin description in Table 3-1 for more information. A design approach similar to the previous undervoltage detection example is recommended for the overvoltage protection circuitry, resistors R2 and R3 in Figure 5-1. For input overvoltage protection, the first consideration is to establish the input voltage level that indicates an overvoltage triggering a system (output voltage) shutdown. For this example, the input value for which a 12V supply will signal an “output shutdown” is 13.2V (+10%). Similarly, from the previous example:

1. Choose R3 to satisfy 100 µA condition.

EQUATION 5-5:

$$R3 \geq \frac{V_{OV(MIN)}}{100\mu A} \geq \frac{1.19V}{100\mu A} \geq 11.9k\Omega$$

R3 is chosen as 13.7 kΩ ±1%.

2. Thus, following the previous example and substituting R2 and R3 for R5 and R6, respectively, and 13.2V overvoltage for 11V output “good”, the same formula yields R2 of 138.3 kΩ. The next highest standard 1% value is 140 kΩ.

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Now, consider the 12.6V maximum input voltage (V_{CC} +5%), the higher tolerance for R3 and lower tolerance for R2, 13.84 kΩ and 138.60 kΩ, respectively. With a 12.6V input, the voltage sensed at the OV pin is below $V_{OV(MIN)}$, and the MIC2085 will not indicate an overvoltage condition until V_{CC} exceeds at least 13.2V.

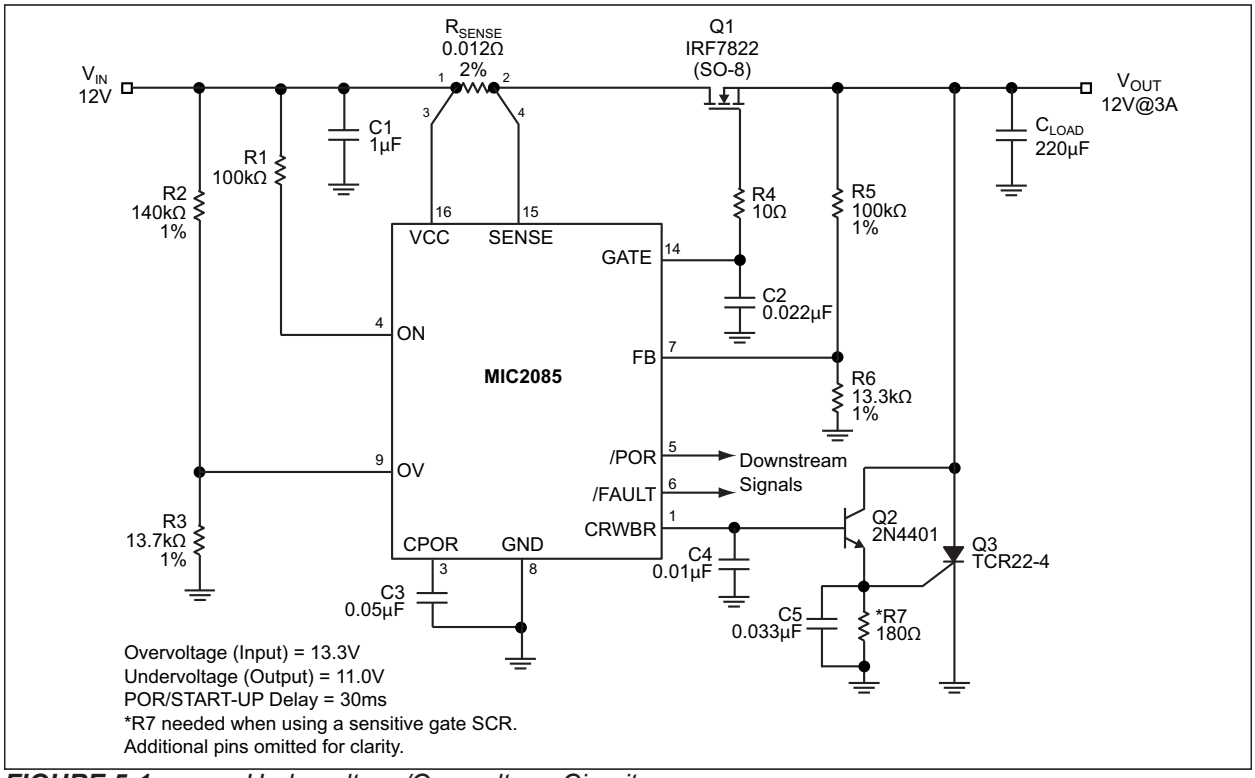


FIGURE 5-1: *Undervoltage/Overvoltage Circuit.*

5.3 PCB Connection Sense

There are several configuration options for the MIC2085's ON pin to detect if the PCB has been fully seated in the backplane before initiating a start-up cycle. In the Typical Application Circuit, the MIC2085 is mounted on the PCB with a resistive divider network connected to the ON pin. R2 is connected to a short pin on the PCB edge connector. Until the connectors mate, the ON pin is held low, which keeps the GATE output charge pump off. Once the connectors mate, the resistor network is pulled up to the input supply, 12V in this example, and the ON pin voltage exceeds its threshold (V_{ON}) of 1.24V and the MIC2085 initiates a start-up cycle.

In Figure 5-2, the connection sense, consisting of a logic-level discrete MOSFET and a few resistors, allows for interrupt control from the processor or other signal controller to shut off the output of the MIC2085. R4 keeps the GATE of Q2 at V_{IN} until the connectors are fully mated. A logic low at the /ON_OFF signal turns Q2 off and allows the ON pin to pull up above its threshold and initiate a start-up cycle. Applying a logic high at the /ON_OFF signal will turn Q2 on and short the ON pin of the MIC2085 to ground, which turns off the GATE output charge pump.

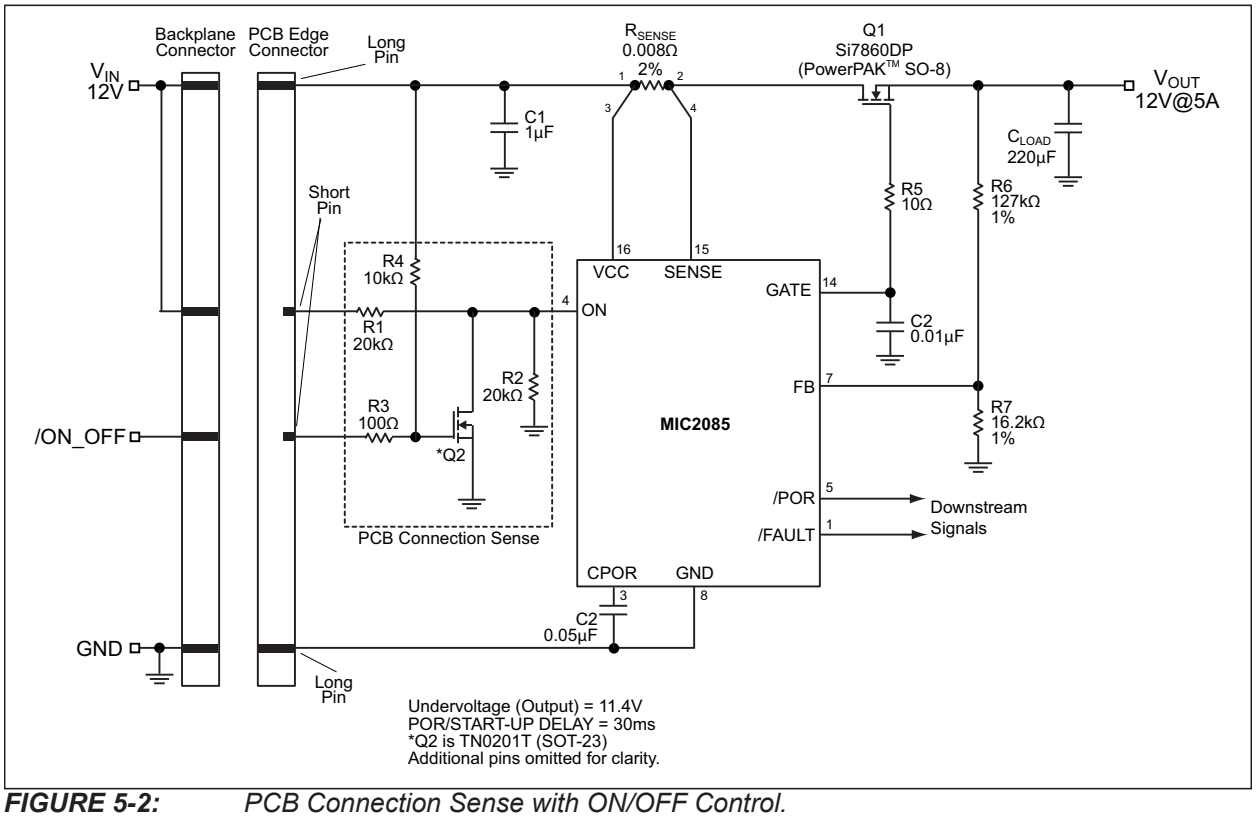


FIGURE 5-2: *PCB Connection Sense with ON/OFF Control.*

5.4 Higher UVLO Setting

Once a PCB is inserted into a backplane (power supply), the internal UVLO circuit of the MIC2085 holds the GATE output charge pump off until V_{CC} exceeds 2.18V. If V_{CC} falls below 2V, the UVLO circuit pulls the GATE output to ground and clears the overvoltage and/or current limit faults. For a higher UVLO threshold, the circuit in Figure 5-3 can be used to delay the output MOSFET from switching on until the desired input voltage is achieved. The circuit allows the charge pump to remain off until V_{IN} exceeds (1 + R1/R2) x 1.24V. The GATE drive output will be shut down when V_{IN} falls below (1 + R1/R2) x 1.14V. In the example circuit (Figure 5-3), the rising UVLO threshold is set at approximately 11V and the falling UVLO threshold is established as 10.1V. The circuit consists of an external resistor divider at the ON pin that keeps the GATE output charge pump off until the voltage at the ON pin exceeds its threshold (V_{ON}) and after the start-up time relapses.

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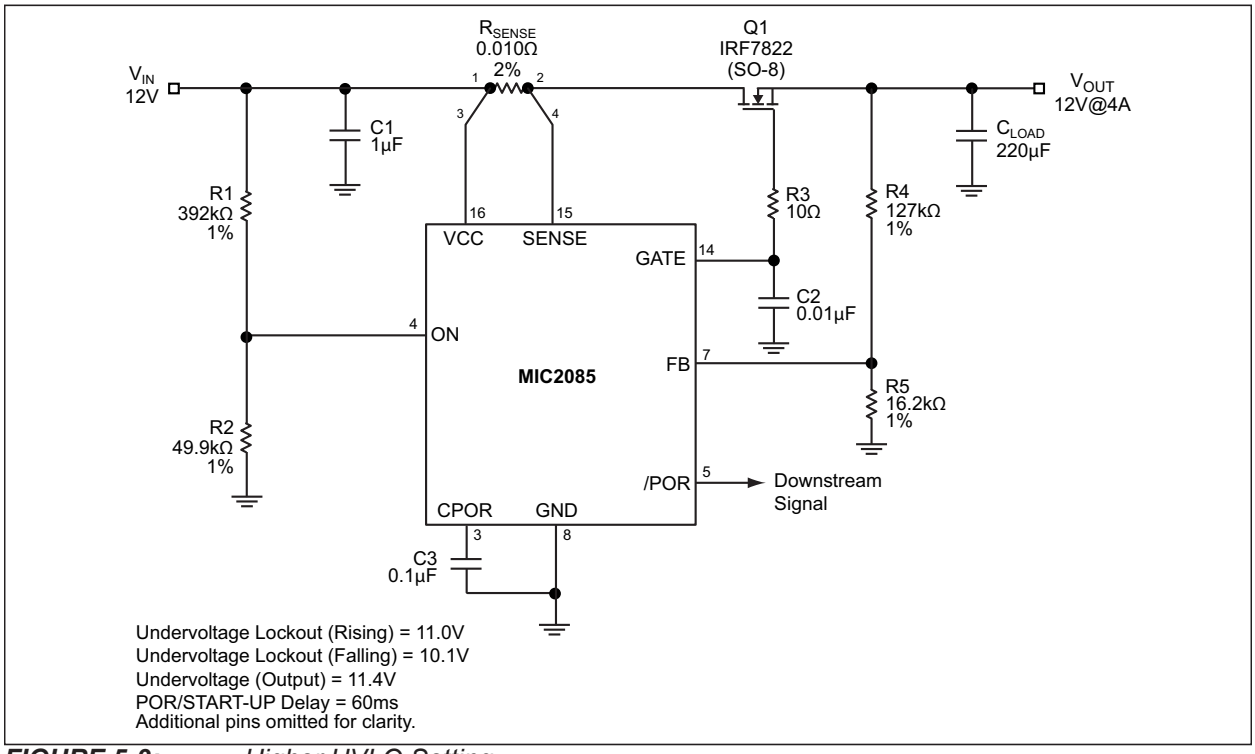


FIGURE 5-3: *Higher UVLO Setting.*

5.5 Auto-Retry Upon Overcurrent Faults

The MIC2085 can be configured for automatic restart after a fault condition. Placing a diode between the ON and/FAULT pins, as shown in Figure 5-4, will enable the auto-restart capability of the controller. When an application is configured for auto-retry, the overcurrent timer should be set to minimize the duty cycle of the overcurrent response to prevent thermal runaway of the power MOSFET. See the MOSFET Transient Thermal Issues section for further detail. A limited duty cycle is achieved when the overcurrent timer duration (t_{OCSLOW}) is much less than the start-up delay timer duration (t_{START}) and is calculated using the following equation:

EQUATION 5-6:

$$Auto-Retry\ \text{Duty Cycle} = \frac{t_{OCSLOW}}{t_{START}} \times 100\%$$

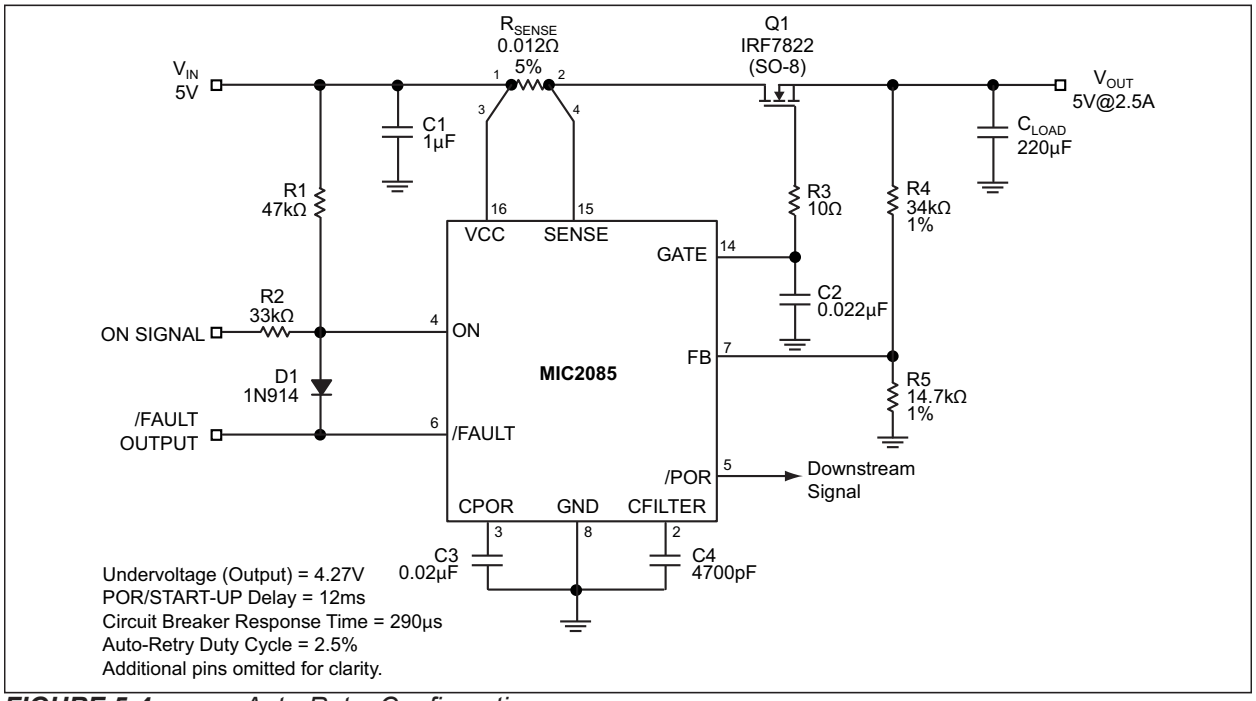


FIGURE 5-4: *Auto-Retry Configuration.*

5.6 An InfiniBand™ Application Circuit

The circuit in Figure 5-5 depicts a single 50W InfiniBand™ module using the MIC2085 controller. An InfiniBand™ backplane distributes bulk power to multiple plug-in modules that employ DC/DC converters for local supply requirements. The circuit in Figure 5-5 distributes 12V from the backplane to the MIC2182 DC/DC converter that steps down +12V to +3.3V for local bias. The pass transistor, Q1, isolates the MIC2182's input capacitance during module plug-in and allows the backplane to accommodate additional plug-in modules without affecting the other modules on the backplane. The two control input signals are VBxEn_L (active-low) and a Local Power Enable (active-high). The MIC2085 in the circuit of Figure 5-5 performs a number of functions. The gate output of Q1 is enabled by the two bit input signal VBxEn_L, Local Power Enable = [0,1]. Also, the MIC2085 limits the drain current of Q1 to 7A, monitors VB_In for an overvoltage condition greater than 16V, and enables the MIC2182 DC/DC converter downstream to supply a local voltage rail. The uncommitted comparator is used to monitor VB_In for an undervoltage condition of less than 10V, indicated by a logic-low at the comparator output (COMPOUT). COMPOUT may be used to control a downstream device such as another DC/DC converter. Additionally, the MIC2085 is configured for auto-retry upon an overcurrent fault condition by placing a diode (D1) between the /FAULT and ON pins of the controller.

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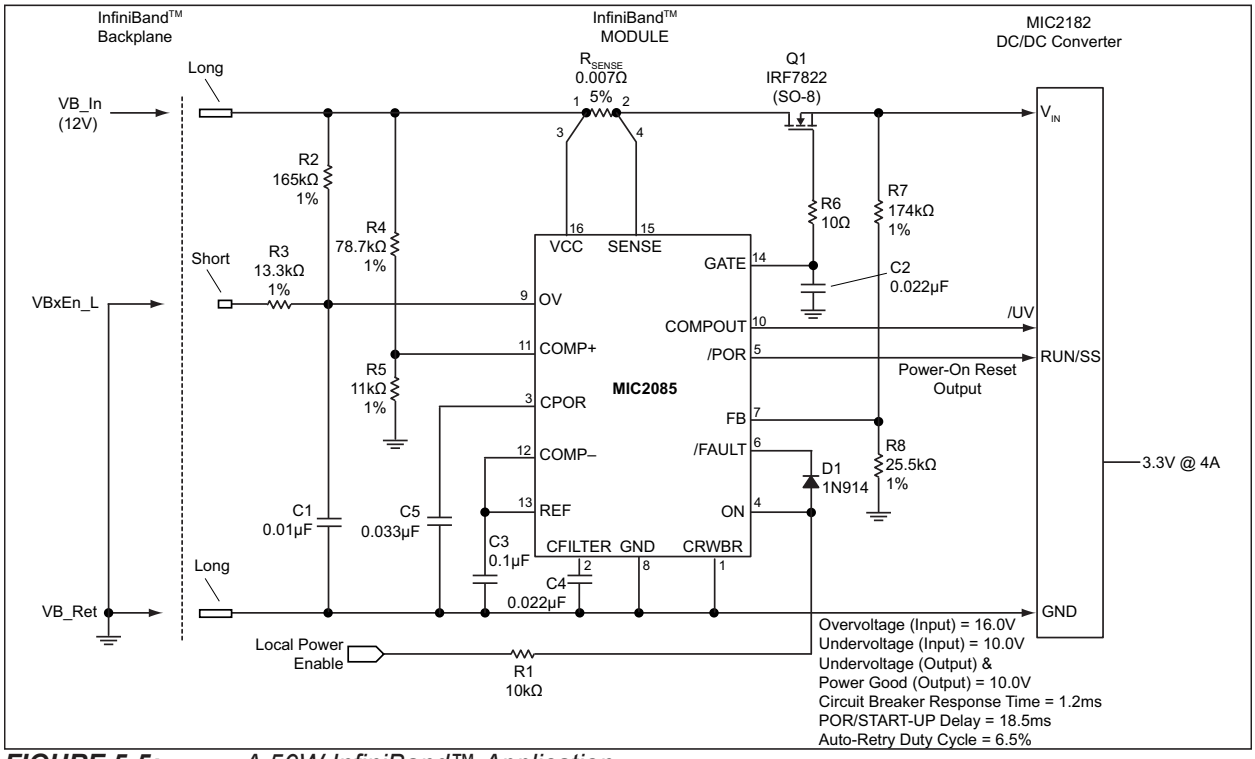


FIGURE 5-5: *A 50W InfiniBand™ Application.*

5.7 Sense Resistor Selection

The MIC2085 uses a low-value sense resistor to measure the current flowing through the MOSFET switch (and therefore the load). This sense resistor is nominally valued at 48 mV/$I_{LOAD(CONT)}$. To accommodate worst-case tolerances for both the sense resistor (allow ±3% over time and temperature for a resistor with ±1% initial tolerance) and still supply the maximum required steady-state load current, a slightly more detailed calculation must be used. The current limit threshold voltage (the “trip point”) for the MIC2085 may be as low as 40 mV, which would equate to a sense resistor value of 40 mV/$I_{LOAD(CONT)}$. Carrying the numbers through for the case where the value of the sense resistor is 3% high yields:

EQUATION 5-7:

$$R_{SENSE(MAX)} = \frac{40mV}{1.03 \times I_{LOAD(CONT)}} = \frac{38.8mV}{I_{LOAD(CONT)}}$$

Once the value of R_{SENSE} has been chosen in this manner, it is good practice to check the maximum $I_{LOAD(CONT)}$ that the circuit may let through in the case of tolerance build-up in the opposite direction. Here, the worst-case maximum current is found using a 55 mV trip voltage and a sense resistor that is 3% low in value. The resulting equation is:

EQUATION 5-8:

$$I_{LOAD(CONTMAX)} = \frac{55mV}{0.97 \times R_{SENSE(NOM)}} = \frac{56.7mV}{R_{SENSE(NOM)}}$$

As an example, if an output must carry a continuous 6A without nuisance trips occurring, Equation 5-7 yields the following:

EQUATION 5-9:

$$R_{SENSE(MAX)} = \frac{38.8mV}{6A} = 6.5m\Omega$$

The next lowest standard value is 6.0 mW. At the other set of tolerance extremes for the output in question:

EQUATION 5-10:

$$I_{LOAD(CONTMAX)} = \frac{56.7mV}{6.0m\Omega} = 9.45A$$

The result is almost 10A. Knowing this final datum, we can determine the necessary wattage of the sense resistor, using $P = I^2R$, where I will be $I_{LOAD(CONT, MAX)}$, and R will be 0.97 x $R_{SENSE(NOM)}$. These numbers yield the following:

EQUATION 5-11:

$$P_{MAX} = 10A^2 \times 5.82m\Omega = 0.582W$$

In this example, a 1W sense resistor is sufficient.

5.8 MOSFET Selection

Selecting the proper external MOSFET for use with the MIC2085 involves three straightforward tasks:

1. Choice of a MOSFET that meets minimum voltage requirements.
2. Selection of a device to handle the maximum continuous current (steady-state thermal issues).
3. Verify the selected part's ability to withstand any peak currents (transient thermal issues).

5.9 MOSFET Voltage Requirements

The first voltage requirement for the MOSFET is that the drain-source breakdown voltage of the MOSFET must be greater than $V_{IN(MAX)}$. For instance, a 16V input may reasonably be expected to see high-frequency transients as high as 24V. Therefore, the drain-source breakdown voltage of the MOSFET must be at least 25V. For ample safety margin and standard availability, the closest minimum value should be 30V.

The second breakdown voltage criterion that must be met is a bit subtler than simple drain-source breakdown voltage. The gate of the external MOSFET is driven up to a maximum of 21V by the internal output MOSFET. At the same time, if the output of the external MOSFET (its source) is suddenly subjected to a short, the gate-source voltage will go to (21V – 0V) = 21V. Because most power MOSFETs generally have a maximum gate-source breakdown of 20V or less, the use of a Zener clamp is recommended in applications with $V_{CC} \geq 8V$. A Zener diode with 10V to 12V rating is recommended as shown in Figure 5-6. At the present time, most power MOSFETs with a 20V gate-source voltage rating have a 30V drain-source break-down rating or higher. As a general tip, choose surface-mount devices with a drain-source rating of 30V or more as a starting point.

Finally, the external gate drive of the MIC2085 requires a low-voltage logic level MOSFET when operating at voltage slower than 3V. There are 2.5V logic-level MOSFETs available. Please see Table 5-1 and Table 5-2 for suggested manufacturers.

5.10 MOSFET Steady-State Thermal Issues

The selection of a MOSFET to meet the maximum continuous current is a fairly straightforward exercise. First, arm yourself with the following data:

- The value of $I_{LOAD(CONT, MAX.)}$ for the output in question (see Sense Resistor Selection).
- The manufacturer's data sheet for the candidate MOSFET.
- The maximum ambient temperature in which the device will be required to operate.
- Any knowledge you can get about the heat sinking available to the device (e.g., can heat be dissipated into the ground plane or power plane, if using a surface-mount part? Is any airflow available?).

The data sheet will almost always give a value of on resistance given for the MOSFET at a gate-source voltage of 4.5V, and another value at a gate-source voltage of 10V. As a first approximation, add the two values together and divide by two to get the on-resistance of the part with 8V of enhancement. Call this value R_{ON}. Because a heavily enhanced MOSFET acts as an ohmic (resistive) device, almost all that's required to determine steady-state power dissipation is to calculate I^2R.The one addendum to this is that MOSFETs have a slight increase in R_{ON} with increasing die temperature. A good approximation for this value is 0.5% increase in R_{ON} per °C rise in junction temperature above the point at which R_{ON} was initially specified by the manufacturer. For instance, if the selected MOSFET has a calculated R_{ON} of 10 mΩ at a T_J = 25°C, and the actual junction temperature ends up at 110°C, a good first cut at the operating value for R_{ON} would be:

EQUATION 5-12:

$$R_{ON} \cong 10m\Omega \times [1 + (110 - 25) \times 0.005] \cong 14.3m\Omega$$

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The final step is to make sure that the heat sinking available to the MOSFET is capable of dissipating at least as much power (rated in °C/W) as that with which the MOSFET's performance was specified by the manufacturer. Here are a few practical tips:

- The heat from a surface-mount device, such as an SO-8 MOSFET, flows almost entirely out of the drain leads. If the drain leads can be soldered down to one square inch or more, the copper will act as the heat sink for the part. This copper must be on the same layer of the board as the MOSFET drain.
- Airflow works. Even a few LFM (linear feet per minute) of air will cool a MOSFET down substantially. If you can, position the MOSFET(s) near the inlet of a power supply's fan, or the outlet of a processor's cooling fan.
- The best test of a surface-mount MOSFET for an application (assuming the above tips show it to be a likely fit) is an empirical one. Check the MOSFET's temperature in the actual layout of the expected final circuit, at full operating current. The use of a thermocouple on the drain leads, or infrared pyrometer on the package, will then give a reasonable idea of the device's junction temperature.

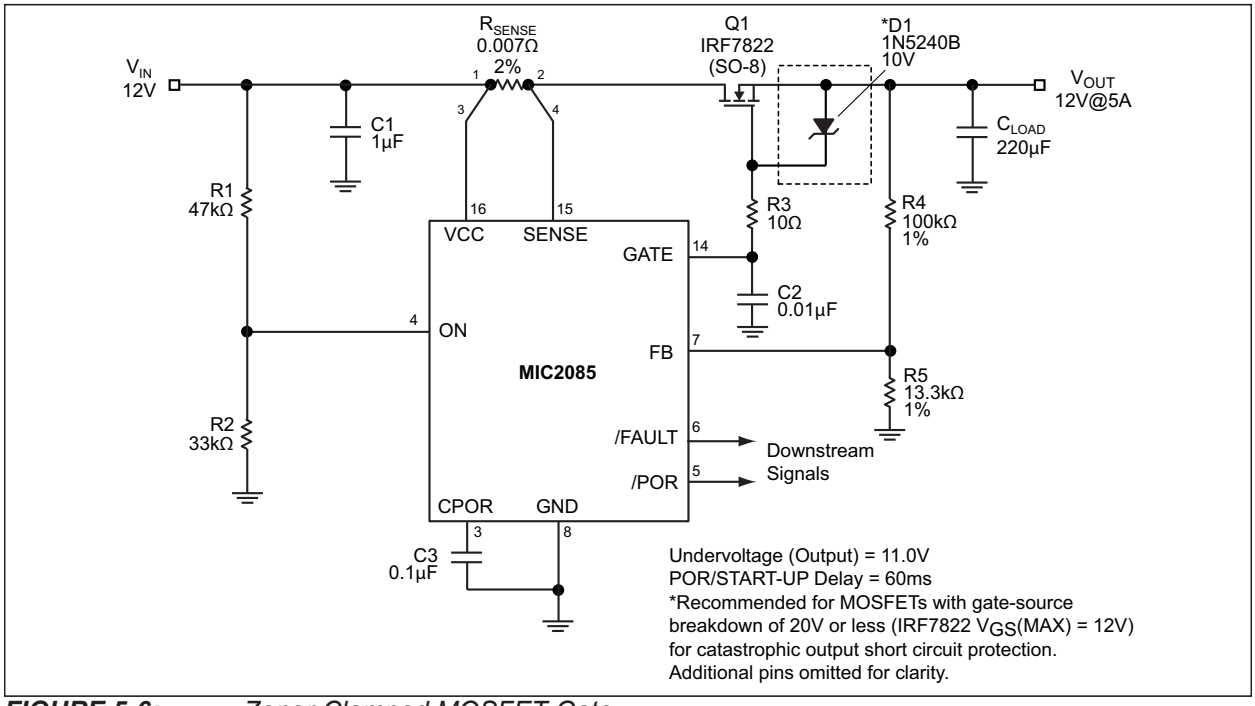


FIGURE 5-6: *Zener-Clamped MOSFET Gate.*

5.11 MOSFET Transient Thermal Issues

Having chosen a MOSFET that will withstand the imposed voltage stresses, and the worse case continuous I^2R power dissipation which it will see, it remains only to verify the MOSFET's ability to handle short-term overload power dissipation without overheating. A MOSFET can handle a much higher pulsed power without damage than its continuous dissipation ratings would imply. The reason for this is that, like everything else, thermal devices (silicon die, lead frames, etc.) have thermal inertia.

In terms related directly to the specification and use of power MOSFETs, this is known as "transient thermal impedance," or $Z_{\theta(JA)}$. Almost all power MOSFET data sheets give a Transient Thermal Impedance Curve. For example, take the following case: V_{IN} = 12V, t_{OCSLOW} has been set to 100 ms, $I_{LOAD(CONT.\ MAX)}$ is 2.5A, the slow-trip threshold is 48 mV, nominal, and the fast-trip threshold is 95 mV. If the output is accidentally connected to a 3Ω load, the output current from the MOSFET will be regulated to 2.5A for 100 ms (t_{OCSLOW}) before the part trips. During that time, the dissipation in the MOSFET is given by:

EQUATION 5-13:

$$P = E \times I$$

$$E_{MOSFET} = (12V - 2.5A \times 3\Omega) = 4.5V$$

$$P_{MOSFET} = 4.5V \times 2.5A = 11.25W \text{ for } 100\text{ms}$$

At first glance, it would appear that a really hefty MOSFET is required to withstand this sort of fault condition. This is where the transient thermal

impedance curves become very useful. Figure 5-7 shows the curve for the Vishay (Siliconix) Si4410DY, a commonly used SO-8 power MOSFET.

Taking the simplest case first, we'll assume that once a fault event such as the one in question occurs, it will be a long time – 10 minutes or more – before the fault is isolated and the channel is reset. In such a case, we can approximate this as a "single pulse" event, that is to say, there's no significant duty cycle. Then, reading up from the X-axis at the point where "Square Wave Pulse Duration" is equal to 0.1 sec (100 ms), we see that the $Z_{\theta(JA)}$ of this MOSFET to a highly infrequent event of this duration is only 8% of its continuous $R_{\theta(JA)}$.

This particular part is specified as having an $R_{\theta(JA)}$ of 50°C/W for intervals of 10 seconds or less. Thus:

Assume T_A = 55°C maximum, 1 square inch of copper at the drain leads, no airflow.

Recalling from our previous approximation hint, the part has an R_{ON} of (0.0335/2) = 17 mΩ at 25°C.

Assume it has been carrying just about 2.5A for some time.

When performing this calculation, be sure to use the highest anticipated ambient temperature ($T_{A(MAX)}$) in which the MOSFET will be operating as the starting temperature, and find the operating junction temperature increase (ΔT_J) from that point. Then, as shown next, the final junction temperature is found by adding $T_{A(MAX)}$ and ΔT_J. Because this is not a closed-form equation, getting a close approximation may take one or two iterations, but it's not a hard calculation to perform, and tends to converge quickly.

Then the starting (steady-state) T_J is:

EQUATION 5-14:

$$T_J \cong T_{A(MAX)} + \Delta T_J$$

$$T_J \cong T_{A(MAX)} + [R_{ON} + (T_{A(MAX)} - T_A)(0.005/°C)(R_{ON})] \times I^2 \times R_{\theta JA}$$

$$T_J \cong 55°C + [17m\Omega + (55°C - 25°C)(0.005)(17m\Omega)] \times 2.5A^2 \times 50°C/\text{W}$$

$$T_J \cong (55°C + 0.122W) \times 50°C/\text{W} \cong 61.1°C$$

Iterate the calculation once to see if this value is within a few percent of the expected final value. For this iteration we will start with T_J equal to the already calculated value of 61.1°C:

EQUATION 5-15:

$$T_J \cong T_A + [17m\Omega + (61.1°C - 25°C)(0.005)(17m\Omega)] \times 2.5A^2 \times 50°C/\text{W}$$

$$T_J \cong 55°C + 0.125W \times 50°C/\text{W} \cong 61.27°C$$

So the original approximation of 61.1°C was very close to the correct value. We will use T_J = 61°C.

Finally, add (11.25W)(50°C/W)(0.08) = 45°C to the steady-state T_J to get $T_{J(\text{TRANSIENT MAX.})}$ = 106°C. This is an acceptable maximum junction temperature for this part.

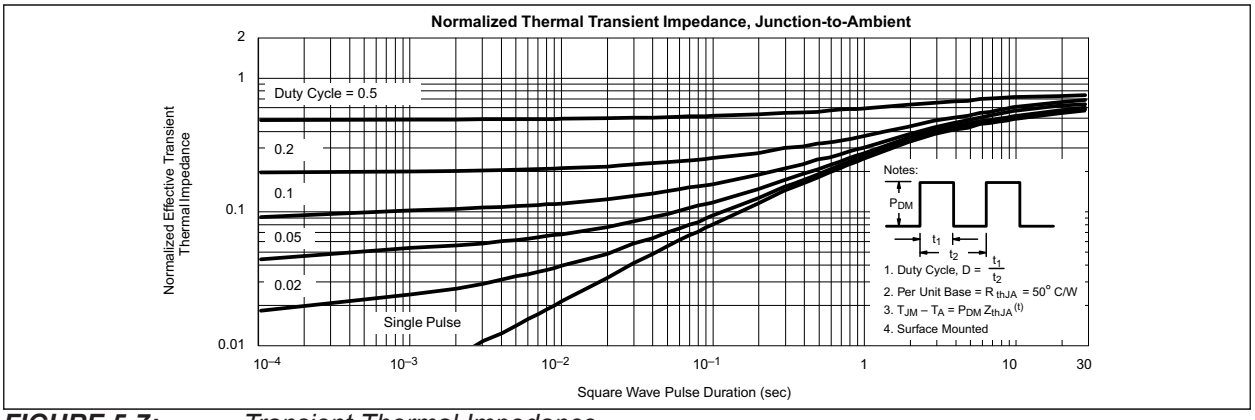


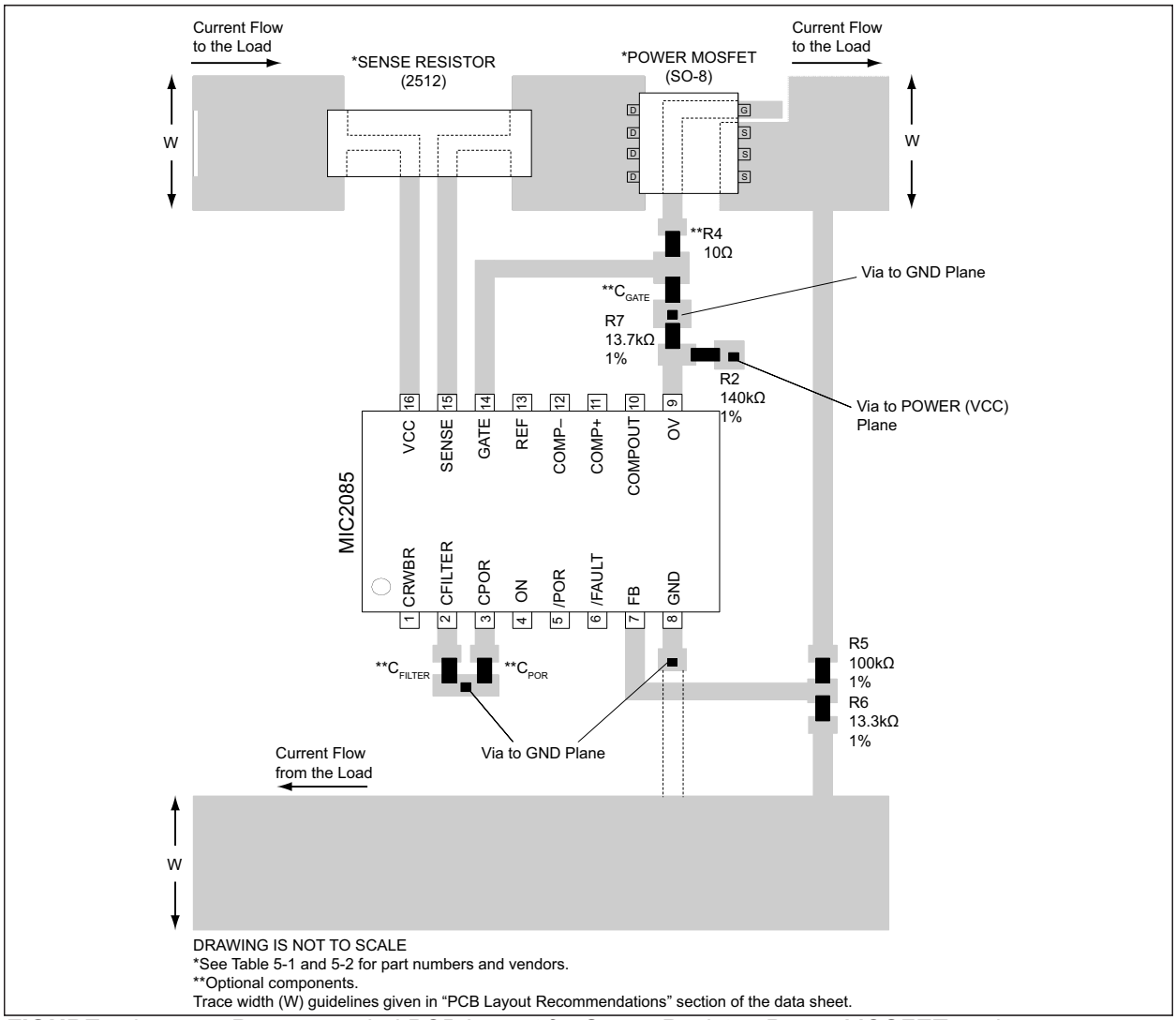
FIGURE 5-7: *Transient Thermal Impedance.*

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5.12 PCB Layout Considerations

Because of the low values of the sense resistors used with the MIC2085 controller, special attention to the layout must be used in order for the device's circuit breaker function to operate properly. Specifically, the use of a 4-wire Kelvin connection to measure the voltage across R_{SENSE} is highly recommended. Kelvin sensing is simply a means of making sure that any voltage drops in the power traces connecting to the resistors does not get picked up by the traces themselves. Additionally, these Kelvin connections should be isolated from all other signal traces to avoid introducing noise onto these sensitive nodes. Figure 5-8 illustrates a recommended, multi-layer layout for the R_{SENSE}, Power MOSFET, timer(s), overvoltage and feedback network connections. The feedback and overvoltage resistive networks are selected for a12V application (from Figure 5-1). Many hot swap applications will require load currents of several amperes. Therefore, the power (V_{CC} and Return) trace widths (W) need to be wide enough to allow the current to flow while the rise in temperature for a given copper plate (e.g., 1 oz. or 2 oz.) is kept to a maximum of 10°C ~ 25°C. Also, these traces should be as short as possible in order to minimize the IR drops between the input and the load.

Finally, plated-through vias are utilized to make circuit connections to the power and ground planes. The trace connections with indicated vias should follow the example shown for the GND pin connection in Figure 5-8.



DRAWING IS NOT TO SCALE
*See Table 5-1 and 5-2 for part numbers and vendors.
**Optional components.
Trace width (W) guidelines given in "PCB Layout Recommendations" section of the data sheet.

FIGURE 5-8: *Recommended PCB Layout for Sense Resistor, Power MOSFET, and Feedback/Overvoltage Network.*

5.13 MOSFET and Sense Resistor Vendors

Device types and manufacturer contact information for power MOSFETs and sense resistors is provided in Table 5-1 and Table 5-2. Some of the recommended MOSFETs include a metal heat sink on the bottom side of the package. The recommended trace for the MOSFET Gate of Figure 5-8 must be redirected when using MOSFETs packaged in this style. Contact the device manufacturer for package information.

TABLE 5-1: MOSFET VENDORS

Vendor	Key MOSFET Type(s)	Applications (Note 1)	Contact Information
Vishay (Siliconix)	Si4420DY (SO-8 package)	$I_{OUT} \le 10A$	www.siliconix.com (203) 452-5664
	Si4442DY (SO-8 package)	$I_{OUT} = 10A – 15A, V_{CC} \le 5V$	
	Si3442DV (SO-8 package)	$I_{OUT} \le 3A, V_{CC} \le 5V$	
	Si7860DP (PowerPAK™ SO-8)	$I_{OUT} \le 12A$	
	Si7892DP (PowerPAK™ SO-8)	$I_{OUT} \le 15A$	
	Si7884DP (PowerPAK™ SO-8)	$I_{OUT} \le 15A$	
	SUB60N06-18 (TO-263)	$I_{OUT} \ge 20A, V_{CC} \ge 5V$	
	SUB70N04-10 (TO-263)	$I_{OUT} \ge 20A, V_{CC} \ge 5V$	
International Rectifier	IRF7413 (SO-8 package)	$I_{OUT} \le 10A$	www.irf.com (310) 322-3331
	IRF7457 (SO-8 package)	$I_{OUT} \le 10A$	
	IRF7822 (SO-8 package)	$I_{OUT} = 10A – 15A, V_{CC} \le 5V$	
	IRLBA1304 (Super220™)	$I_{OUT} \ge 20A, V_{CC} \ge 5V$	
Fairchild Semiconductor	FDS6680A (SO-8 package)	$I_{OUT} \le 10A$	www.fairchildsemi.com (207) 775-8100
	FDS6690A (SO-8 package)	$I_{OUT} \ge 10A, V_{CC} \ge 5V$	
Philips	PH3230 (SOT669-LFPAK)	$I_{OUT} \ge 20A$	www.philips.com
Hitachi	HAT2099H (LFPAK)	$I_{OUT} \ge 20A$	www.halsp.hitachi.com (408) 433-1990

Note 1: These devices are not limited to these conditions in many cases, but these conditions are provided as a helpful reference for customer applications.

TABLE 5-2: SENSE RESISTOR VENDORS

Vendor	Sense Resistors	Contact Information
Vishay (Dale)	“WSL” Series	(203) 452-5664
IRC	“OARS” Series ”LR” Series (second source to “WSL”)	(828) 264-8861

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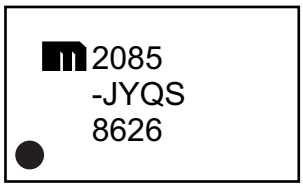
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

16-Lead QSOP*



Example

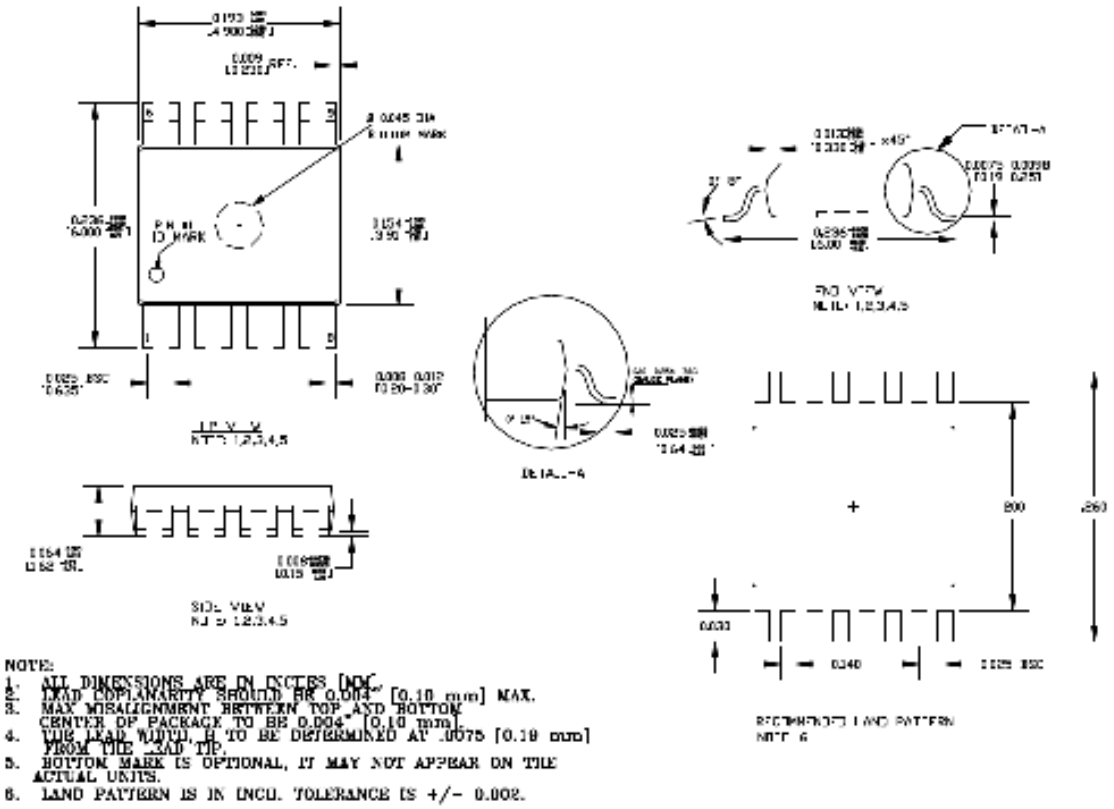


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

16-Lead QSOP Package Outline & Recommended Land Pattern

TITLE
16 LEAD QSOP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	QSOP 16LD PL 1	UNIT	INCH
Lead Frame	Copper	Lead Finish	Matte Tin



NOTES:
1. ALL DIMENSIONS ARE IN INCHES [MM].
2. LEAD COPLANARITY SHOULD BE 0.004" [0.10 mm] MAX.
3. MAX MISALIGNMENT BETWEEN TOP AND BOTTOM CENTER OF PACKAGE TO BE 0.004" [0.10 mm].
4. THIS LEAD WIDTH, B, TO BE DETERMINED AT .0075 [0.19 mm] FROM THE LEAD TIP.
5. BOTTOM MARK IS OPTIONAL, IT MAY NOT APPEAR ON THE ACTUAL UNITS.
6. LAND PATTERN IS IN INCH. TOLERANCE IS +/- 0.002.

RECOMMENDED LAND PATTERN
NOTE 6

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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APPENDIX A: REVISION HISTORY

Revision A (June 2019)

- Converted Micrel document MIC2085 to Microchip data sheet template DS20006094A.
- Minor grammatical text changes throughout.
- All reference to and information about the MIC2086 has been removed.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	-X	X	XX	-XX
Part No.	Feature	Junction Temp. Range	Package	Media Type

Device:	MIC2085:	Single-Channel Low Voltage Hot Swap Controller
Feature:	Fast Circuit Breaker Threshold J = 95mV K = 150mV* L = 200mV* M = Off	
Junction Temperature Range:	Y =	–40°C to +85°C, RoHS-Compliant
Package:	QS =	16-Lead QSOP
Media Type:	<blank>= 98/Tube TR = 2,500/Reel	

* Contact factory for availabilty.

Examples:

a) MIC2085-JYQS: MIC2085, 95mV Fast Circuit Breaker Threshold, –40°C to +85°C Temperature Range, 16-Lead QSOP, 98/Tube

b) MIC2085-KYQS: MIC2085, 150mV* Fast Circuit Breaker Threshold, –40°C to +85°C Temperature Range, 16-Lead QSOP, 98/Tube

c) MIC2085-LYQS-TR: MIC2085, 200mV* Fast Circuit Breaker Threshold, –40°C to +85°C Temperature Range, 16-Lead QSOP, 2,500/Reel

d) MIC2085-MYQS-TR: MIC2085, Fast Circuit Breaker Threshold OFF, –40°C to +85°C Temperature Range, 16-Lead QSOP, 2,500/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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