MIC2168

1 MHz PWM Synchronous Buck Control IC

Features

- 3V to 14.5V Input Voltage Range
- Adjustable Output Voltage Down to 0.8V
- Up to 95% Efficiency
- 1 MHz PWM Operation
- Adjustable Current Limit Senses High-Side N-Channel MOSFET Current
- No External Current Sense Resistor
- Adaptive Gate Drive Increases Efficiency
- Ultra-Fast Response with Hysteretic Transient Recovery Mode
- Overvoltage Protection Protects the Load in Fault Conditions
- Dual-Mode Current Limit Speeds up Recovery Time
- Hiccup Mode Short-Circuit Protection
- Internal Soft-Start
- Dual Function COMP and EN Pin Allows Low-Power Shutdown
- Small Size MSOP 10-Lead Package

Applications

- Point-of-Load DC/DC Conversion
- Set-Top Boxes
- Graphics Cards
- LCD Power Supplies
- Telecom Power Supplies
- Networking Power Supplies
- Cable Modems and Routers

General Description

The MIC2168 is a high-efficiency, simple-to-use 1 MHz PWM synchronous buck control IC housed in a small MSOP-10 package. The MIC2168 allows compact DC/DC solutions with a minimal external component count and cost.

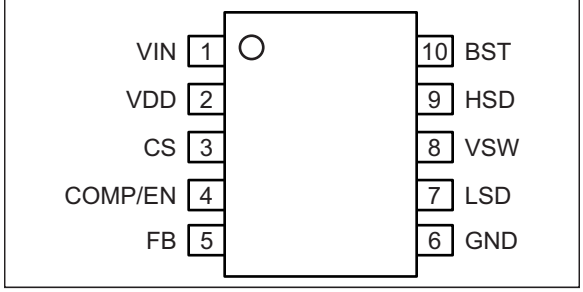
The MIC2168 operates from a 3V to 14.5V input, without the need of any additional bias voltage. The output voltage can be precisely regulated down to 0.8V. The adaptive all N-Channel MOSFET drive scheme allows efficiencies over 95% across a wide load range.

The MIC2168 senses current across the high-side N-Channel MOSFET, eliminating the need for an expensive and lossy current-sense resistor. Current limit accuracy is maintained by a positive temperature coefficient that tracks the increasing $R_{DS(ON)}$ of the external MOSFET. Further cost and space are saved by the internal in-rush-current limiting and digital soft-start.

The MIC2168 is available in a 10-lead MSOP package, with a wide junction operating range of –40°C to +125°C.

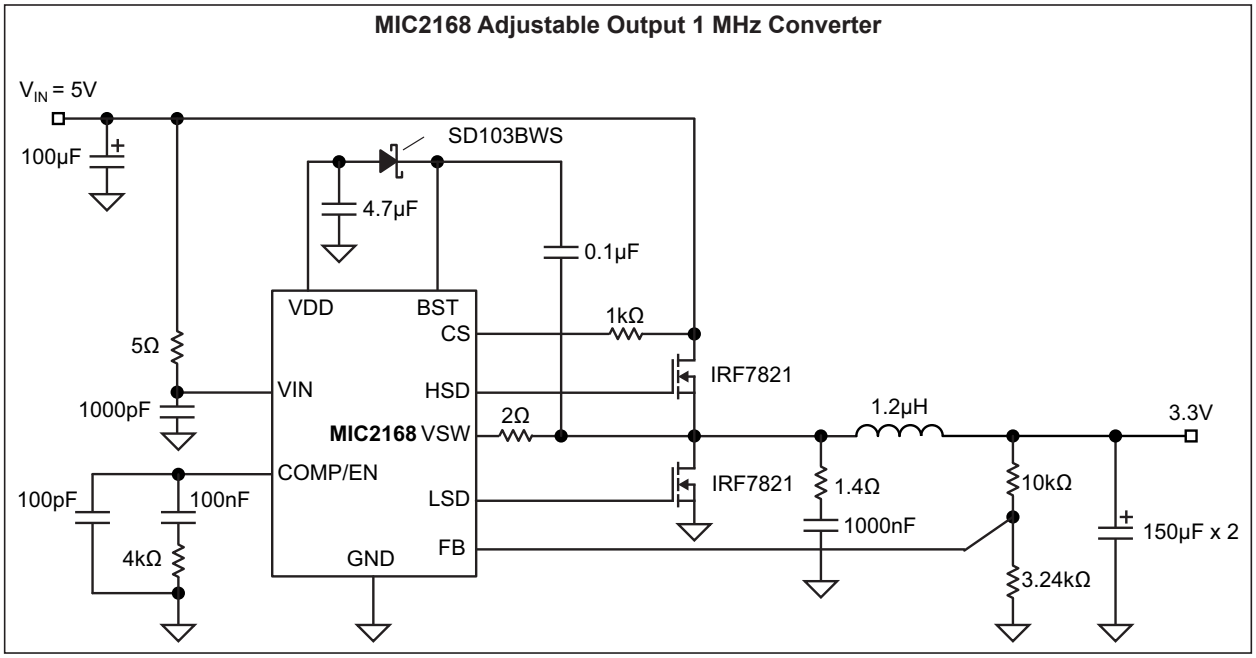
Package Type

MIC2168
10-Lead MSOP (MM)
(Top View)

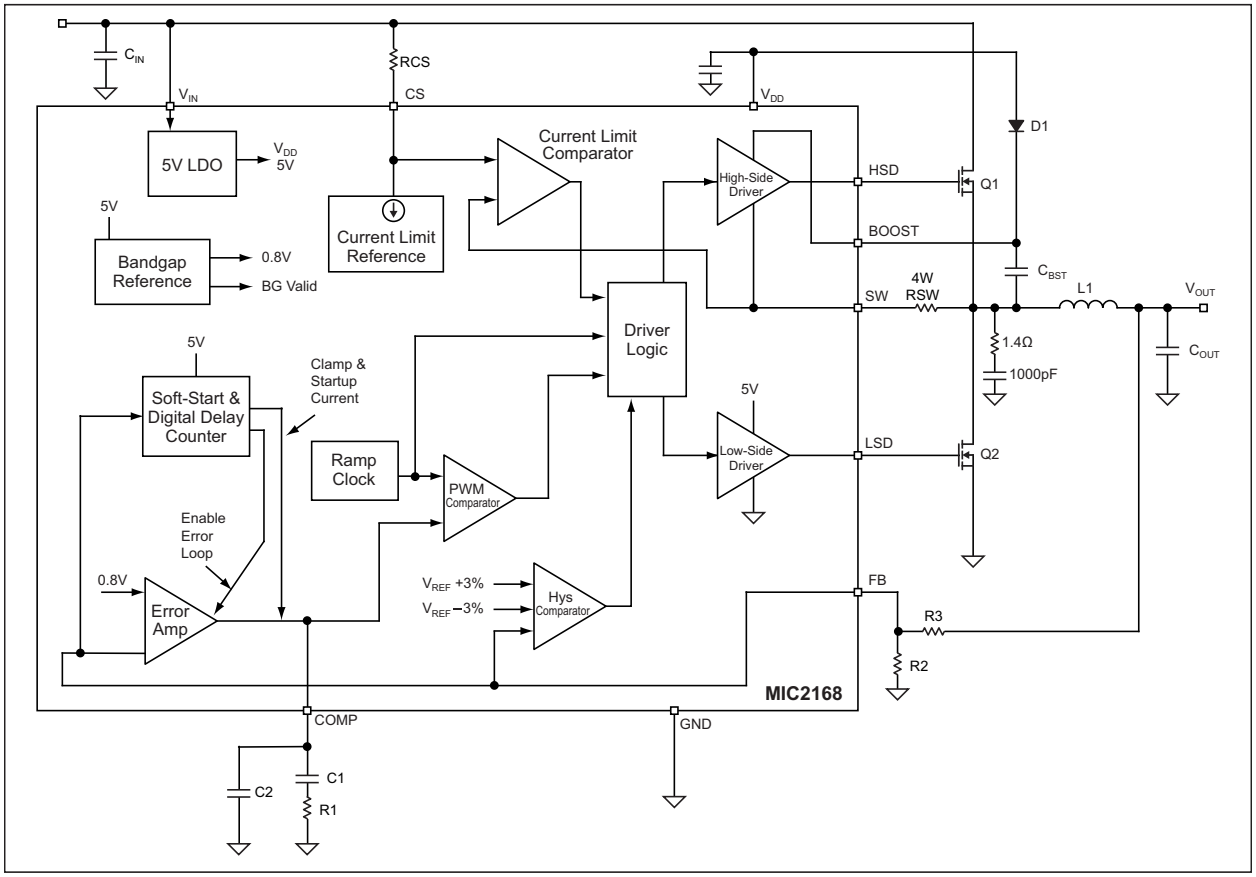


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Typical Application Circuit



Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{IN}) ..... +15.5V
Bootstrapped Voltage (V_{BST}) ..... V_{IN} + 5V

Operating Ratings ††

Supply Voltage (V_{IN}) ..... +3V to +14.5V
Output Voltage Range ..... 0.8V to V_{IN} x D_{MAX}

† Notice: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its operating ratings. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.

†† Notice: Devices are ESD sensitive, handling precautions required.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: T_J = +25°C, V_{IN} = 5V, unless otherwise specified.
Bold values indicate –40°C < T_J < +125°C Note 1

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Feedback Voltage Reference	V_{FB}	0.792	0.8	0.808	V	±1%
		0.784	0.8	**0.816**		±2% over temperature
Feedback Bias Current	I_{BIAS}	—	30	**100**	nA	—
Output Voltage Line Regulation		—	0.03	—	%/V	—
Output Voltage Load Regulation		—	0.5	—	%	—
Output Voltage Total Regulation		—	0.6	—	%	3V ≤ V_{IN} ≤ 14.5V; 1A ≤ I_{OUT} ≤ 10A; (V_{OUT} = 2.5V), Note 2
Oscillator Selection						
Oscillator Frequency	f_O	900	1000	1100	kHz	—
Maximum Duty Cycle	D_{MAX}	—	—	90	%	—
Minimum On-Time	$t_{ON(MIN)}$	—	30	**60**	ns	Note 2
Input and V_{DD} Supply						
PWM Mode Supply Current		—	1.6	**3**	mA	V_{CS} = V_{IN} – 0.25V; V_{FB} = 0.7V (output switching but excluding external MOSFET gate current)
Shutdown Quiescent Current	I_{SHDN}	—	50	**150**	µA	$V_{COMP/EN}$ = 0V
V_{COMP} Shutdown Threshold		0.1	0.25	0.4	V	—
V_{COMP} Shutdown Blanking Period		—	4		ms	C_{COMP} = 100 nF
Digital Supply Voltage	V_{DD}	4.7	5	5.3	V	V_{IN} ≥ 6V

Note 1: Specification for packaged product only.
2: Guaranteed by design.

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: T_J = +25°C, V_{IN} = 5V, unless otherwise specified.
Bold values indicate –40°C < T_J < +125°C Note 1

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Error Amplifier						
DC Gain		—	70	—	dB	—
Transconductance		—	1	—	ms	—
Soft-Start						
Soft-Start Current	I_{SS}	—	8.5	—	µA	After timeout of internal timer. See Soft-Start section.
Current Sense						
CS Overcurrent Trip Point		160	200	240	µA	$V_{CS} = V_{IN} – 0.25V$
Temperature Coefficient			1800		ppm/°C	—
Output Fault Correction Thresholds						
Upper Threshold	V_{FB_OVT}	—	+3	—	%	Relative to V_{FB}
Lower Threshold	V_{FB_UVT}	—	–3	—	%	Relative to V_{FB}
Gate Drivers						
Rise/Fall Time	t_r/t_f	—	30	—	ns	Into 3000 pF at V_{IN} > 5V
Output Driver Impedance		—	—	6	Ω	Source, V_{IN} = 5V
		—	—	6		Sink, V_{IN} = 5V
		—	—	10		Source, V_{IN} = 3V
		—	—	10		Sink, V_{IN} = 3V
Driver Non-Overlap Time		10	20	—	ns	Note 2

Note 1: Specification for packaged product only.
2: Guaranteed by design.

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TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Maximum Junction Temperature Range	T_J	–40	—	+125	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Package Thermal Resistances						
Thermal Resistance, MSOP 10-Ld	θ_{JA}	—	180	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Electrical Characteristics: V_{IN} = 5V.

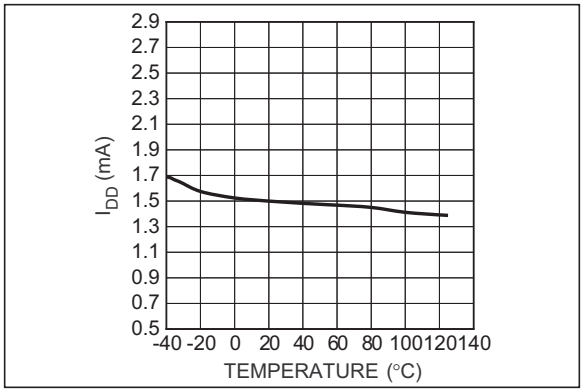


FIGURE 2-1: *PWM Mode Supply Current vs. Temperature.*

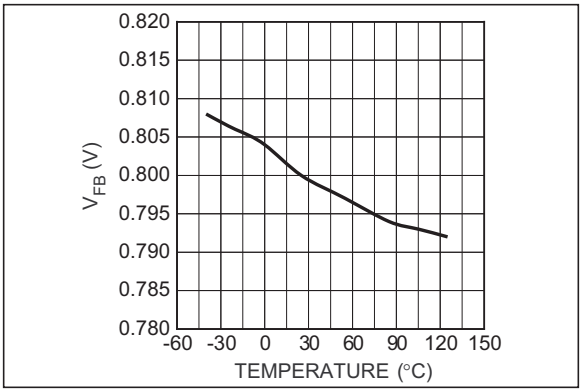


FIGURE 2-4: *V_{FB} vs. Temperature.*

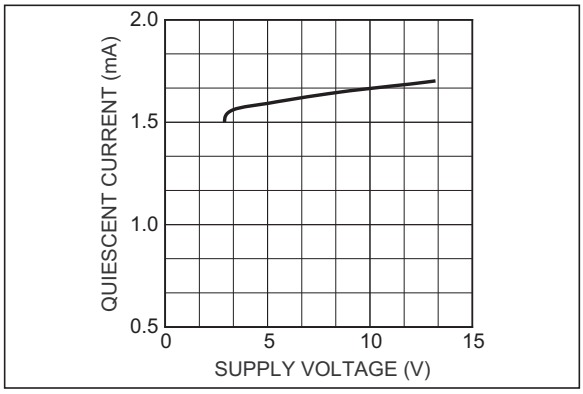


FIGURE 2-2: *PWM Mode Supply Current vs. Supply Voltage.*

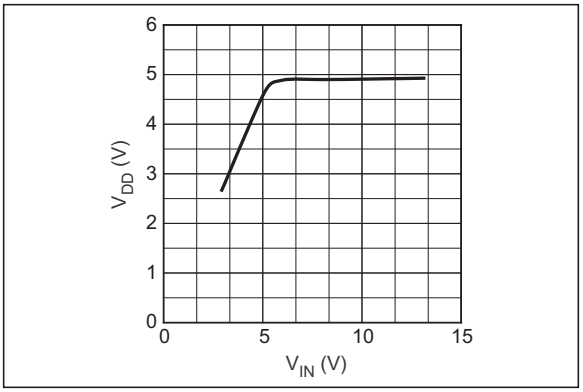


FIGURE 2-5: *V_{DD} Line Regulation.*

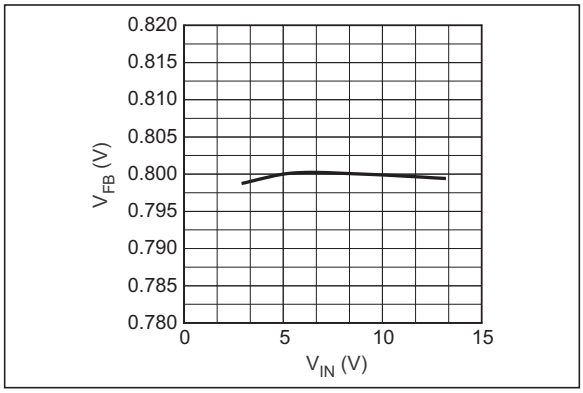


FIGURE 2-3: *V_{FB} Line Regulation.*

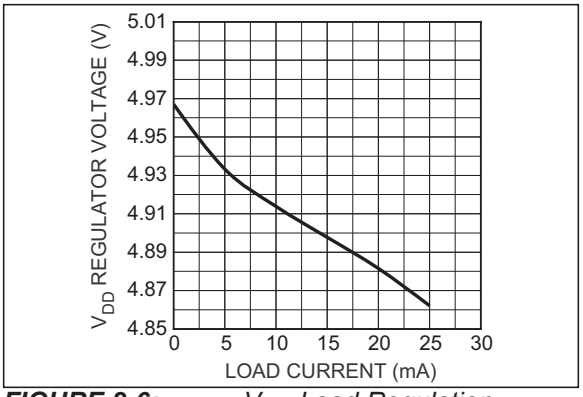


FIGURE 2-6: *V_{DD} Load Regulation.*

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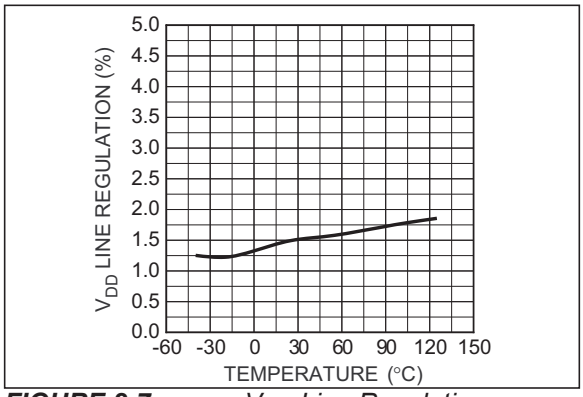


FIGURE 2-7: *V_{DD} Line Regulation vs. Temperature.*

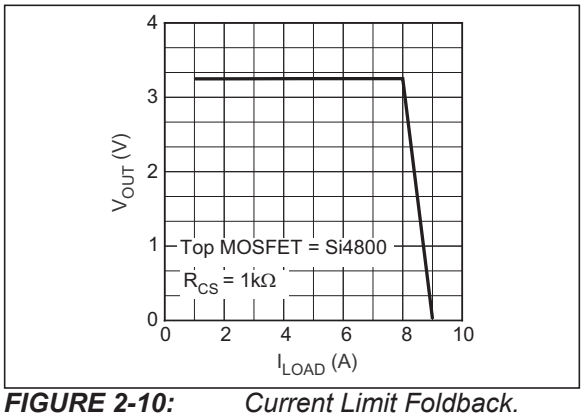


FIGURE 2-10: *Current Limit Foldback.*

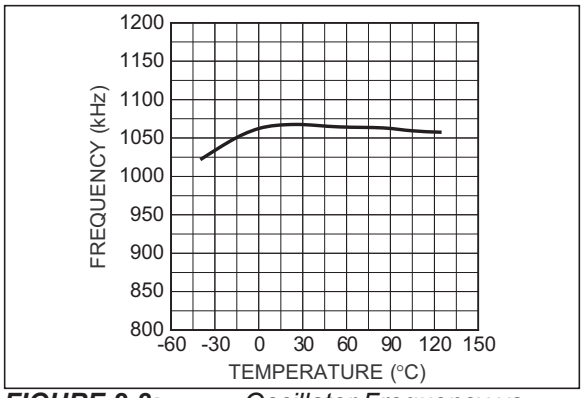


FIGURE 2-8: *Oscillator Frequency vs. Temperature.*

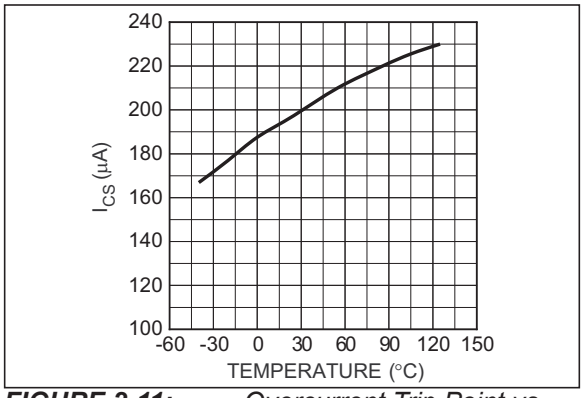


FIGURE 2-11: *Overcurrent Trip Point vs. Temperature.*

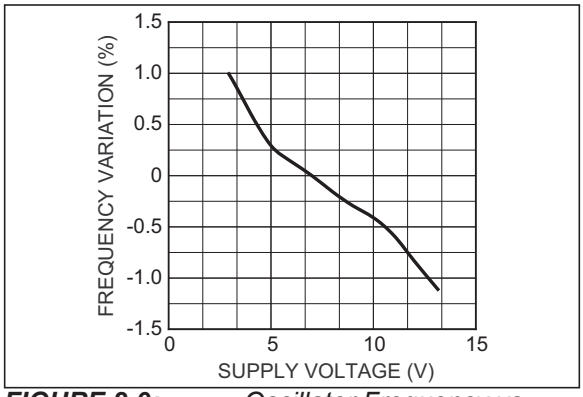


FIGURE 2-9: *Oscillator Frequency vs. Supply Voltage.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	VIN	Supply Voltage (Input): 3V to 14.5V.
2	VDD	5V Internal Linear Regulator (Output): V_{DD} is the external MOSFET gate drive supply voltage and an internal supply bus for the IC. When V_{IN} is < 5V, this regulator operates in dropout mode.
3	CS	Current Sense/Enable (Input): Current limit comparator noninverting input. The current limit is sensed across the MOSFET during the ON time. The current can be set by the resistor in series with the CS pin.
4	COMP/EN	Compensation (Input): Dual function pin. Pin for external compensation. If this pin is pulled below 0.2V, with the reference fully up the device shuts down (50 µA typical current draw).
5	FB	Feedback (Input): Input to error amplifier. Regulates error amplifier to 0.8V.
6	GND	Ground (Return).
7	LSD	Low-Side Drive (Output): High-current driver output for external synchronous MOSFET.
8	VSW	Switch (Return): High-side MOSFET driver return.
9	HSD	High-Side Drive (Output): High-current output-driver for the high-side MOSFET. When V_{IN} is between 3.0V to 5V, 2.5V threshold-rated MOSFETs should be used. At V_{IN} > 5V, 5V threshold MOSFETs should be used.
10	BST	Boost (Input): Provides the drive voltage for the high-side MOSFET driver. The gate-drive voltage is higher than the source voltage by V_{IN} minus a diode drop.

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4.0 FUNCTIONAL DESCRIPTION

The MIC2168 is a voltage mode, synchronous step-down switching regulator controller designed for high output power without the use of an external sense resistor. It includes an internal soft-start function that reduces the power supply input surge current at start-up by controlling the output voltage rise time, a PWM generator, a reference voltage, two MOSFET drivers, and short-circuit current limiting circuitry to form a complete 1 MHz switching regulator.

4.1 Theory of Operation

The MIC2168 is a voltage mode step-down regulator. The Functional Block Diagram illustrates the block diagram for the voltage control loop. The output voltage variation due to load or line changes will be sensed by the inverting input of the transconductance error amplifier via the feedback resistors R3, and R2 and compared to a reference voltage at the non-inverting input. This will cause a small change in the DC voltage level at the output of the error amplifier which is the input to the PWM comparator. The other input to the comparator is a 0V to 1V triangular waveform. The comparator generates a rectangular waveform whose width t_{ON} is equal to the time from the start of the clock cycle t_0 until t_1, the time the triangle crosses the output waveform of the error amplifier. To illustrate the control loop, let us assume the output voltage drops due to sudden load turn-on, this would cause the inverting input of the error amplifier which is divided down version of V_{OUT} to be slightly less than the reference voltage causing the output voltage of the error amplifier to go high. This will cause the PWM comparator to increase t_{ON} time of the top side MOSFET, causing the output voltage to go up and bringing V_{OUT} back in regulation.

4.2 Soft-Start

The COMP/EN pin is used for three functions:

1. Disables the part by grounding this pin.
2. External compensation to stabilize the voltage control loop.
3. Soft-Start.

For better understanding of the soft-start feature, let's assume V_{IN} = 12V and the MIC2168 is allowed to power up by ungrounding the COMP/EN pin. The COMP pin has an internal 8.5 µA current source that charges the external compensation capacitor. As soon as this voltage rises to 180 mV (t = Cap_COMP x 0.18V/8.5 µA), the MIC2168 allows the internal V_{DD} linear regulator to power up. As soon as it crosses the undervoltage lockout of 2.6V, the chip's internal oscillator starts switching. At this point in time, the COMP pin current source increases to 40 µA and an internal 11-bit counter starts counting; this takes approximately 2 ms to complete. During counting, the COMP voltage is clamped at 0.65V. After this counting cycle, the COMP current source is reduced to 8.5 µA and the COMP pin voltage rises from 0.65V to 0.95V, the bottom edge of the saw-tooth oscillator. This is the beginning of 0% duty cycle and it increases slowly, causing the output voltage to slowly rise. The MIC2168 has two hysteretic comparators that are enabled when V_{OUT} is with ±3% of steady state. When the output voltage reaches 97% of the programmed output voltage, the g_m error amplifier is enabled along with the hysteretic comparator. From this point onward, the voltage control loop (g_m error amplifier) is fully in control and will regulate the output voltage.

Soft-start time can be calculated approximately by adding the following four time frames:

EQUATION 4-1:

$$t1 = Cap_\text{COMP} \times 0.18V/8.5\mu A$$

$$t2 = 12 \text{ bit counter, appx. } 2\text{ms}$$

$$t3 = Cap_\text{COMP} \times 0.3V/8.5\mu A$$

$$t4 = \frac{V_{OUT}}{V_{IN}} \times 0.5 \times \frac{Cap_\text{COMP}}{8.5\mu A}$$

$$Soft\text{-Start Time}(Cap_\text{COMP} = 100nF) = t1 + t2 + t3 + t4$$

$$2.1ms + 2ms + 3.5ms + 1.8ms = 10ms$$

4.3 Current Limit

The MIC2168 uses the $R_{DS(ON)}$ of the top power MOSFET to measure the output current. Because it uses the drain to source the resistance of the power MOSFET, it is not very accurate. This scheme is adequate to protect the power supply and external components during a fault condition by cutting back the time the top MOSFET is on if the feedback voltage is greater than 0.67V. In case of a hard short when the feedback voltage is less than 0.67V, the MIC2168 discharges the COMP capacitor to 0.65V, resets the digital counter, automatically shuts off the top gate drive, and the g_m error amplifier and the –3% hysteretic comparators are complete disabled. Then the soft-start cycle restarts. This mode of operation is called the hiccup mode and its purpose is to protect the downstream load in case of a hard shirt. the circuit in Figure 4-1 illustrates the MIC2168 current limiting circuit.

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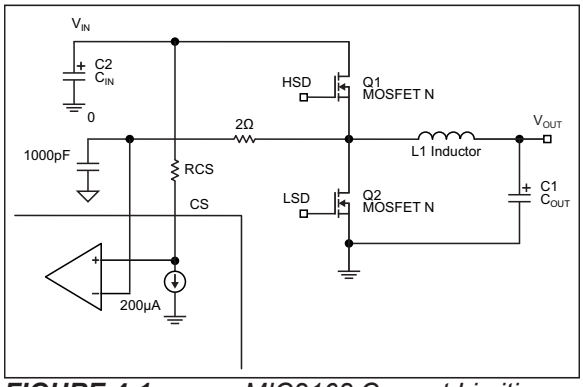


FIGURE 4-1: *MIC2168 Current Limiting Circuit.*

The current limiting resistor R_{CS} is calculated using the following equation:

EQUATION 4-2:

$$R_{CS} = \frac{R_{DS(ON)Q1} \times I_L}{200\mu A}$$

$$I_L = I_{LOAD} = \frac{1}{2(Inductor\ \text{Ripple Current})}$$

$$Inductor\ \text{Ripple Current} = V_{OUT} = \frac{V_{IN} - V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

Where:

f_{SW} = 1 MHz

200 µA is the internal sink current to program the MIC2168 current limit.

The MOSFET $R_{DS(ON)}$ varies 30% to 40% with temperature. Therefore, it is recommended to add a 50% margin to the load current (I_{LOAD}) in Equation 4-2 to avoid false current limiting due to increased MOSFET junction temperature rise. It is also recommended to connect R_{CS} resistor directly to the drain of the top MOSFET Q1, and the R_{SW} resistor to the source of Q1 to accurately sense the MOSFETs $R_{DS(ON)}$. A 0.1 µF capacitor in parallel with R_{CS} should be connected to filter some of the switching noise.

4.4 Internal V_{DD} Supply

The MIC2168 controller internally generates V_{DD} for self-biasing and to provide power to the gate drives. This V_{DD} supply is generated through a low-dropout regulator and generates 5V from V_{IN} supply greater than 5V. For supply voltage less than 5V, the V_{DD} linear regulator is approximately 200 mV in dropout. Therefore, it is recommended to short the V_{DD} supply to the input supply through a 10Ω resistor for input supplies between 2.9V to 5V.

4.5 MOSFET Gate Drive

The MIC2168 high-side drive circuit is designed to switch an N-Channel MOSFET. The Functional Block Diagram shows a bootstrap circuit, consisting of D2 and CBST, supplies energy to the high-side drive circuit. Capacitor CBST is charged while the low-side MOSFET is on and the voltage on the VSW pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from CBST is used to turn the MOSFET on. As the MOSFET turns on, the voltage on the VSW pin increases to approximately V_{IN}. Diode D2 is reversed biased and CBST floats high while continuing to keep the high-side MOSFET on. When the low-side switch is turned back on, CBST is recharged through D2. The drive voltage is derived from the internal 5V V_{DD} bias supply. The nominal low-side gate drive voltage is 5V and the nominal high-side gate drive voltage is approximately 4.5V due the voltage drop across D2. An approximate 20 ns delay between the high- and low-side driver transitions is used to prevent current from simultaneously flowing unimpeded through both MOSFETs.

4.6 MOSFET Selection

The MIC2168 controller works from input voltages of 3V to 13.2V and has an internal 5V regulator to provide power to turn the external N-Channel power MOSFETs for high- and low-side switches. For applications where V_{IN} < 5V, the internal V_{DD} regulator operates in dropout mode, and it is necessary that the power MOSFETs used are low-threshold and are in full conduction mode for V_{GS} of 2.5V. For applications when V_{IN} > 5V; logic-level MOSFETs, whose operation is specified at V_{GS} = 4.5V, must be used.

It is important to note the ON-resistance of a MOSFET increases with increasing temperature. A 75°C rise in junction temperature will increase the channel resistance of the MOSFET by 50% to 75% of the resistance specified at 25°C. This change in resistance must be accounted for when calculating MOSFET power dissipation and in calculating the value of current-sense (CS) resistor. Total gate charge is the charge required to turn the MOSFET on and off under specified operating conditions (V_{DS} and V_{GS}). The gate charge is supplied by the MIC2168 gate drive circuit. At 1 MHz switching frequency and above, the gate charge can be a significant source of power dissipation in the MIC2168. At low output load, this power dissipation is noticeable as a reduction in efficiency. The average current required to drive the high-side MOSFET is:

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EQUATION 4-3:

$$I_{G(HIGH\text{-SIDEAVG})} = Q_G \times f_S$$

Where:
$I_{G(HIGH\text{-SIDEAVG})}$ = Average high-side MOSFET gate current.
Q_G = Total gate charge for the high-side MOSFET taken from the manufacturer's data sheet for V_{GS} = 5V.

The low-side MOSFET is turned on and off at V_{DS} = 0V because the freewheeling diode is conducting during this time. The switching loss for the low-side MOSFET is usually negligible. Also, the gate-drive current for the low-side MOSFET is more accurately calculated using C_{ISS} at V_{DS} = 0V instead of gate charge.

For the low-side MOSFET:

EQUATION 4-4:

$$I_{G(LOW\text{-SIDEAVG})} = C_{ISS} \times V_{GS} \times f_S$$

Because the current from the gate drive comes from the input voltage, the power dissipated in the MIC2168 due to gate drive is:

EQUATION 4-5:

$$P_{GATEDRIVE} = V_{IN}(I_{G(HIGH\text{-SIDEAVG})} + I_{G(LOW\text{-SIDEAVG})})$$

A convenient figure of merit for switching MOSFETs is the ON-resistance times the total gate charge ($R_{DS(ON)} \times Q_G$). Lower numbers translate into higher efficiency. Low gate-charge logic-level MOSFETs are a good choice for use with the MIC2168.

Parameters that are important to MOSFET switch selection are:

- Voltage Rating
- ON-Resistance
- Total Gate Charge

The voltage ratings for the top and bottom MOSFET are essentially equal to the input voltage. A safety factor of 20% should be added to the $V_{DS(MAX)}$ of the MOSFETs to account for voltage spikes due to circuit parasitics.

The power dissipated in the switching transistor is the sum of the conduction losses during the on-time ($P_{CONDUCTION}$) and the switching losses that occur during the period of time when the MOSFETs turn on and off (P_{AC}).

EQUATION 4-6:

$$P_{SW} = P_{CONDUCTION} + P_{AC}$$

Where:
$P_{CONDUCTION} = I_{SW(RMS)}^2 \times R_{SW}$
$P_{AC} = P_{AC(OFF)} + P_{AC(ON)}$
R_{SW} = ON-Resistance of the MOSFET switch.
D = Duty cycle (V_{OUT}/V_{IN})

Making the assumption that the turn-on and turn-off transition times are equal, the transition times can be approximated by:

EQUATION 4-7:

$$t_T = \frac{C_{ISS} \times V_{GS} + C_{OSS} \times V_{IN}}{I_G}$$

Where:
C_{ISS} and C_{OSS} are measured at V_{DS} = 0V.
I_G = Gate-drive current (1A for the MIC2168)

Total high-side MOSFET switching loss is:

EQUATION 4-8:

$$P_{AC} = (V_{IN} + V_D) \times I_{PK} \times t_T \times f_S$$

Where:
t_T = Switching transition time (typ. 20 ns to 50 ns)
V_D = Freewheeling diode drop (typ. 0.5V)
f_S = Switching frequency (nom. 1 MHz)

The low-side MOSFET switching losses are negligible and can be ignored for these calculations.

4.7 Inductor Selection

Values for inductance, peak, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents will increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value and therefore a larger and more expensive inductor. A good compromise between size, loss, and cost is to set the inductor ripple current to be equal to 20% of the maximum output current. The inductance value is calculated by the equation below.

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EQUATION 4-9:

$$L = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_S \times 0.2 \times I_{OUT(MAX)}}$$

Where:
f_S = Switching frequency, 1 MHz
0.2 = The ratio of AC ripple current to DC output current.
$V_{IN(MAX)}$ = Maximum input voltage.

The peak-to-peak inductor current (AC ripple current) is:

EQUATION 4-10:

$$I_{PP} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_S \times L}$$

The peak inductor current is equal to the average output current plus one half of the peak-to-peak inductor ripple current.

EQUATION 4-11:

$$I_{INDUCTOR(RMS)} = I_{OUT(MAX)} \times \sqrt{1 + \frac{1}{3}\left(\frac{I_P}{I_{OUT(MAX)}}\right)^2}$$

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high frequency operation of the MIC2168 requires the use of ferrite materials for all but the most cost sensitive applications. Lower cost iron powder cores may be used but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetics vendor. Copper loss in the inductor is calculated by the equation below:

EQUATION 4-12:

$$P_{INDUCTOR\,CU} = I_{INDUCTOR(RMS)}^2 \times R_{WINDING}$$

The resistance of the copper wire, $R_{WINDING}$, increases with temperature. The value of the winding resistance used should be at the operating temperature.

EQUATION 4-13:

$$R_{WINDING(HOT)} = R_{WINDING(20°C)} \times (1 + 0.0042 \times [T_{HOT} - T_{20°C}])$$

Where:
T_{HOT} = Temperature of the wire under operating load
$T_{20°C}$ = Ambient temperature.
$R_{WINDING(20°C)}$ = Room temperature winding resistance (usually specified by manufacturer).

4.8 Output Capacitor Selection

The output capacitor values are usually determined by the capacitor's ESR (equivalent series resistance). Voltage and RMS current capability are two other important factors selecting the output capacitor. Recommended capacitors tantalum, low-ESR aluminum electrolytics, and POSCAPS. The output capacitor's ESR is usually the main cause of output ripple.

The output capacitor ESR also affects the overall voltage feedback loop from stability point of view. See "Feedback Loop Compensation" section for more information. The maximum value of ESR is calculated:

EQUATION 4-14:

$$R_{ESR} \leq \frac{\Delta V_{OUT}}{I_{PP}}$$

Where:
V_{OUT} = Peak-to-peak output voltage ripple.
I_{PP} = Peak-to-peak inductor ripple current.

The total output ripple is a combination of the ESR output capacitance. The total ripple is calculated below.

EQUATION 4-15:

$$\Delta V_{OUT} = \sqrt{\left(\frac{I_{PP} \times (1 - D)}{C_{OUT} \times f_S}\right)^2 + (I_{PP} \times R_{ESR})^2}$$

Where:
D = Duty cycle.
C_{OUT} = Output capacitance.
f_S = Switching frequency.

The voltage rating of capacitor should be twice the voltage for a tantalum and 20% greater for an aluminum electrolytic.

The output capacitor RMS current is calculated below.

EQUATION 4-16:

$$I_{COUT(RMS)} = \frac{I_{PP}}{\sqrt{12}}$$

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The power dissipated in the output capacitor is:

EQUATION 4-17:

$$P_{DISS(COUT)} = I_{COUT(RMS)}^{2} \times R_{ESR(COUT)}$$

4.9 Input Capacitor Selection

The input capacitor should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents, caused by turning the input supply on. Tantalum input capacitor voltage rating should be at least 2 times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON, and multilayer polymer film capacitors can handle the higher inrush currents without voltage derating. The input voltage ripple will primarily depend on the input capacitor's ESR. The peak input current is equal to the peak inductor current, so:

EQUATION 4-18:

$$\Delta V_{IN} = I_{INDUCTOR(PEAK)} \times R_{ESR(CIN)}$$

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor ripple current is low:

EQUATION 4-19:

$$I_{CIN(RMS)} \approx I_{OUT(MAX)} \times \sqrt{D \times (1 - D)}$$

The power dissipated in the input capacitor is:

EQUATION 4-20:

$$P_{DISS(CIN)} = I_{CIN(RMS)}^{2} \times R_{ESR(CIN)}$$

4.10 Voltage Setting Components

The MIC2168 requires two resistors to set the output voltage as shown in Figure 4-2.

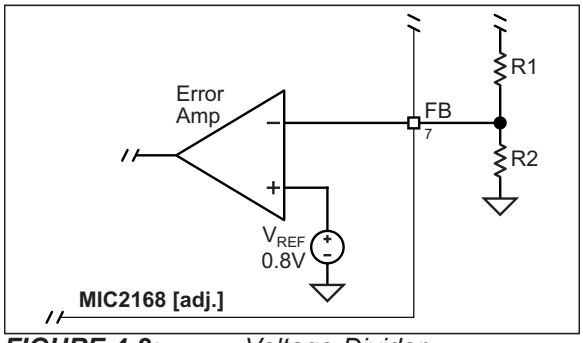


FIGURE 4-2: *Voltage-Divider Configuration.*

In this figure, V_{REF} for MIC2168 is typically 0.8V.

The output voltage is determined by Equation 4-21.

EQUATION 4-21:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

A typical value for R1 can be between 3 kΩ and 10 kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small, it will decrease the efficiency of the power supply, especially at light loads. Once R1 is selected, R2 can be calculated.

EQUATION 4-22:

$$R2 = \frac{V_{REF} \times R1}{V_{OUT} - V_{REF}}$$

4.11 External Schottky Diode

An external freewheeling diode is used to keep the inductor current flow continuous while both MOSFETs are turned off. This dead time prevents current from flowing unimpeded through both MOSFETs and is typically 15 ns. The diode conducts twice during each switching cycle. Although the average current through this diode is small, the diode must be able to handle the peak current.

The reverse voltage requirement of the diode is:

EQUATION 4-23:

$$V_{DIODE(RRM)} = V_{IN}$$

The power dissipated by the Schottky diode is:

EQUATION 4-24:

$$P_{DIODE} = I_{D(AVG)} \times V_F$$

Where:

V_F = Forward voltage at the peak diode current.

The external Schottky diode, D1, is not necessary for circuit operation because the low-side MOSFET contains a parasitic body diode. The external diode will improve efficiency and decrease high frequency noise. If the MOSFET body diode is used, it must be rated to handle the peak and average current. The body diode has a relatively slow reverse recovery time and a relatively high forward voltage drop. The power lost in the diode is proportional to the forward voltage drop of the diode. As the high-side MOSFET starts to turn on, the body diode becomes a short circuit for the reverse recovery period, dissipating additional power. The diode recovery and the circuit inductance will cause ringing during the high-side MOSFET turn-on. An external Schottky diode conducts at a lower forward voltage preventing the body diode in the MOSFET from turning on. The lower forward voltage drop dissipates less power than the body diode. The lack of a reverse recovery mechanism in a Schottky diode causes less ringing and less power loss. Depending on the circuit components and operating conditions, an external Schottky diode will give a 1/2% to 1% improvement in efficiency.

4.12 Feedback Loop Compensation

The MIC2168 controller comes with an internal transconductance error amplifier used for compensating the voltage feedback loop by placing a capacitor (C1) in series with a resistor (R1) and another capacitor C2 in parallel from the COMP pin to ground. See the Functional Block Diagram.

4.13 Power Stage

The power stage of a voltage mode controller has an inductor, L1, with its winding resistance (DCR) connected to the output capacitor, C_{OUT}, with its electrical series resistance (ESR) as shown in Figure 4-3. The transfer function G(s), for such a system is:

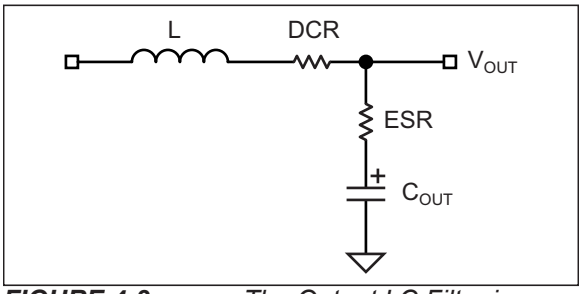


FIGURE 4-3: *The Output LC Filter in a Voltage Mode Buck Converter.*

EQUATION 4-25:

$$G_{(S)} = \left(\frac{(1 + ESR \times s \times C)}{DCR \times s \times C + s^2 \times L \times C + 1 + ESR \times s \times C} \right)$$

Plotting this transfer function with the following assumed values (L = 2 µH, DCR = 0.009Ω, C_{OUT} = 1000 µF, ESR = 0.050Ω) gives much insight toward why one needs to compensate on the COMP pin. Figure 4-4 and Figure 4-5 show the gain curve and phase curve for the transfer function in Equation 4-25.

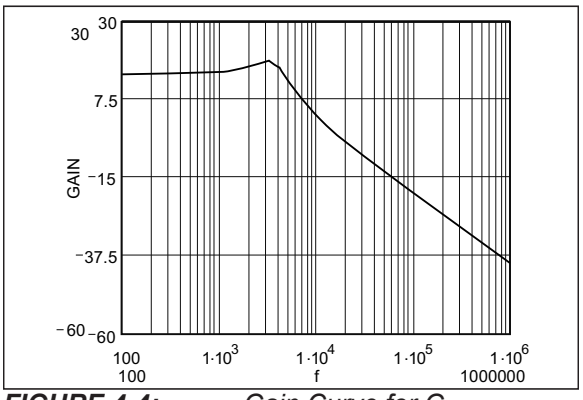


FIGURE 4-4: *Gain Curve for $G_{(S)}$.*

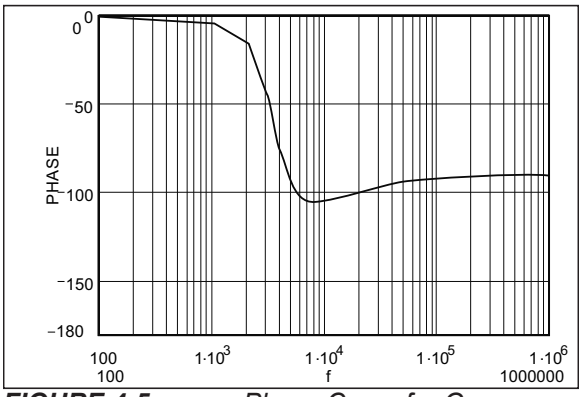


FIGURE 4-5: *Phase Curve for $G_{(S)}$.*

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It can be seen from the transfer function $G_{(S)}$ and the gain curve that the output inductor and capacitor create a two pole system with a break frequency at:

EQUATION 4-26:

$$f_C = \frac{1}{2 \times \pi \sqrt{L \times C_{OUT}}}$$

Therefore, f_{LC} = 3.6 kHz.

By looking at the phase curve, it can be seen that the output capacitor ESR (0.050Ω) cancels one of the two poles (LC_{OUT}) system by introducing a zero at:

EQUATION 4-27:

$$f_{ZERO} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}}$$

Therefore, f_{ZERO} = 6.36 kHz.

From the point of view of compensating the voltage loop, it is recommended to use higher ESR output capacitors because they provide a 90° phase gain in the power path. For comparison purposes, Figure 4-6 shows the same phase curve with an ESR value of 0.002Ω.

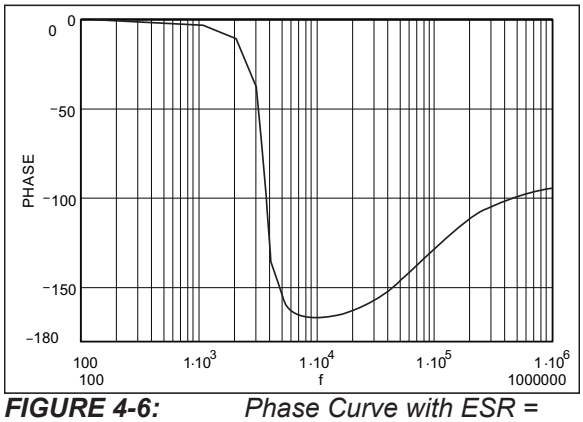


FIGURE 4-6: *Phase Curve with ESR = 0.002Ω.*

It can be seen from Figure 4-5 that at 50 kHz, the phase is approximately –90° versus Figure 4-6 where the number is –150°. This means that the transconductance error amplifier has to provide a phase boost of about 45° to achieve a closed loop phase margin of 45° at a crossover frequency of 50 kHz for Figure 4-4, versus 105° for Figure 4-6. The simple RC and C2 compensation scheme allows a maximum error amplifier phase boost of about 90°. Therefore, it is easier to stabilize the MIC2168 voltage control loop by using high ESR value output capacitors.

4.14 g_m Error Amplifier

It is undesirable to have high error amplifier gain at high frequencies because high frequency noise spikes would be picked up and transmitted at large amplitude to the output, thus, gain should be permitted to fall off at high frequencies. At low frequency, it is desired to have high open-loop gain to attenuate the power line ripple. Thus, the error amplifier gain should be allowed to increase rapidly at low frequencies.

The transfer function with R1, C1, and C2 for the internal g_m error amplifier can be approximated by Equation 4-28.

EQUATION 4-28:

$$\text{Error Amplifer (z)} = g_m \times \left[\frac{1 + R1 \times S \times C1}{s \times (C1 + C2) \times \left(1 + R1 \times \frac{C1 \times C2 \times S}{C1 + C2}\right)} \right]$$

The equation above can be simplified by assuming C2<<C1.

EQUATION 4-29:

$$\text{Error Amplifier (z)} = g_m \times \left(\frac{1 + R1 \times S \times C1}{s \times (C1) \times (1 + R1 \times C2 \times S)} \right)$$

From the transfer function in Equation 4-29, one can see that R1 and C1 introduce a zero while R1 and C2 introduce a pole at the following frequencies:

- F_{ZERO} = 1/2π x R1 x C1
- F_{POLE} = 1/2π x R2 x R1
- $F_{POLE@ORIGIN}$ = 1/2π x C1

Figure 4-7 and Figure 4-8 show the gain and phase curves for the above transfer function with R1 = 9.3 kΩ, C1 = 1000 pF, C2 = 100 pF, and $g_m = 0.005\Omega^{-1}$. It can be seen that at 50 kHz, the error amplifier exhibits approximately 45° of phase margin.

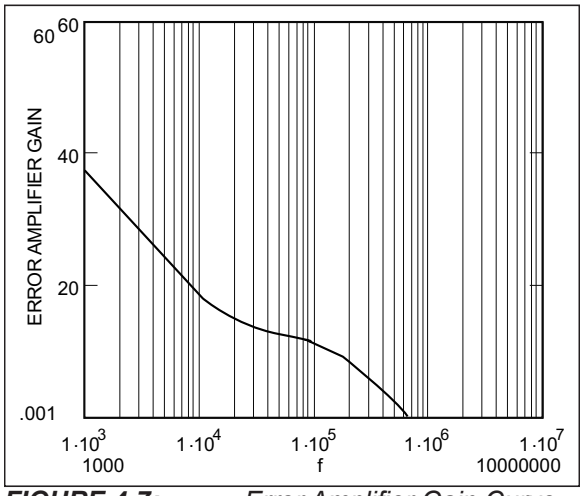


FIGURE 4-7: *Error Amplifier Gain Curve.*

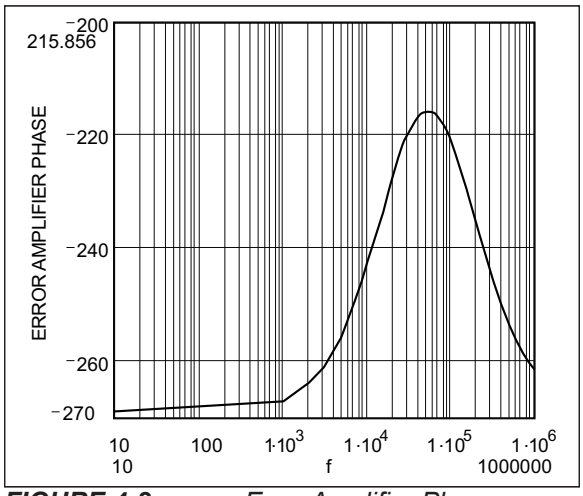


FIGURE 4-8: *Error Amplifier Phase Curve.*

4.15 Total Open-Loop Response

The open-loop response for the MIC2168 controller is easily obtained by adding the power path and the error amplifier gains together because they already are in Log scale. It is desirable to have the gain curve intersect zero dB at tens of kilohertz; this is commonly called crossover frequency. The phase margin at crossover frequency should be at least 45°. Phase margins of 30° or less cause the power supply to have substantial ringing when subjected to transients, and have little tolerance for component or environmental variations. Figure 4-9 and Figure 4-10 show the open-loop gain and phase margin.

It can be seen from Figure 4-9 that the gain curve intersects the 0 dB at approximately 50 kHz, and from Figure 4-10 that at 50 kHz, the phase shows approximately 50° of margin.

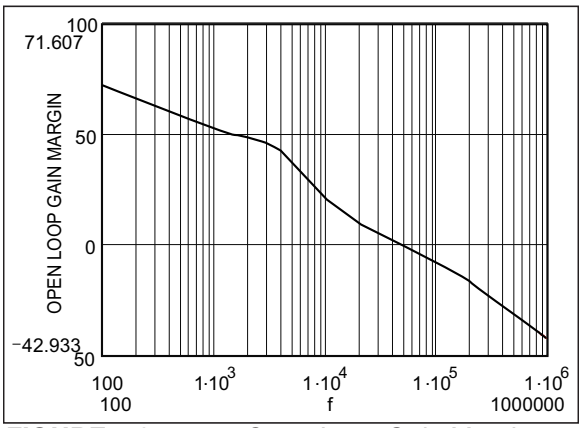


FIGURE 4-9: *Open-Loop Gain Margin.*

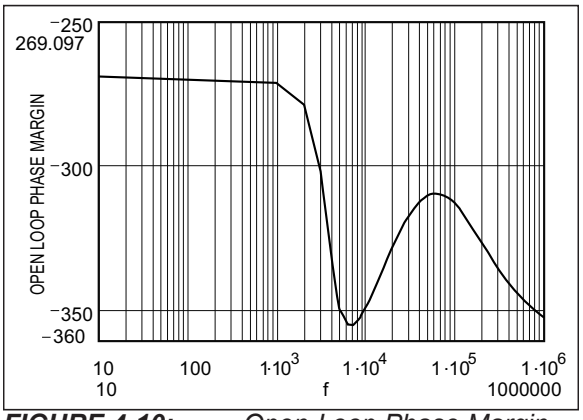


FIGURE 4-10: *Open-Loop Phase Margin.*

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4.16 Design Example

Layout and checklist:

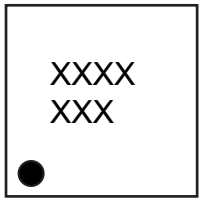
1. Connect the current limiting (CS) resistor directly to the drain of top MOSFET Q1.
2. Connect the VSW pin directly to the source of top MOSFET Q1 through a 4Ω to 10Ω resistor. The purpose of this resistor is to filter the switch node.
3. The feedback resistors R1 and R2 should be placed close to the FB pin. The top side of R1 should connect directly to the output node. Run this trace away from the switch node (junction of Q1, Q2, and L1). The bottom side of R1 should connect to the GND pin.
4. The compensation resistor and capacitors should be placed right next to the COMP/EN pin and the other side should connect directly to the GND pin rather than going to the plane.
5. The input bulk capacitors should be placed close to the drain of the top MOSFET.
6. The 1 µF ceramic capacitor should be placed right on the VIN pin.
7. The 4.7 µF to 10 µF ceramic capacitor should be placed right on the VDD pin.
8. The source of the bottom MOSFET should connect directly to the input capacitor GND with a thick trace. The output capacitor and the input capacitor should connect directly to the ground plane.
9. Place a 0.1 µF ceramic capacitor in parallel with the CS resistor to filter any switching noise.

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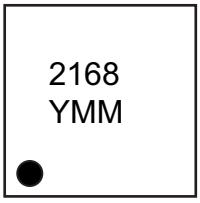
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

10-Lead MSOP*



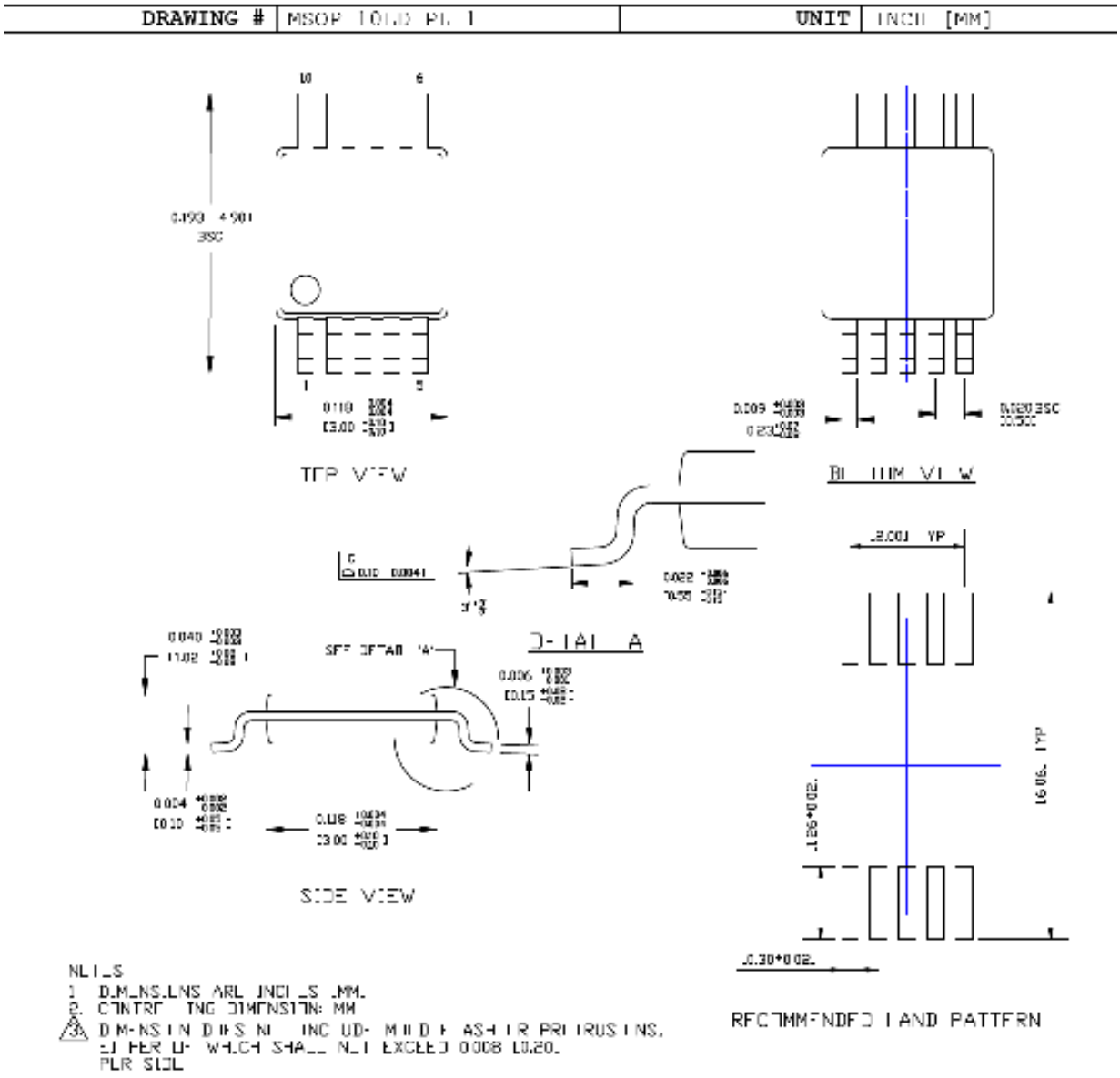
Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

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10-Lead MSOP Package Outline and Recommended Land Pattern



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (January 2020)

- Converted Micrel document MIC2168 to Microchip data sheet template DS20006145A.
- Minor grammatical text changes throughout.

NOTES:

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To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	X	XX	-XX
Part No.	Junction Temp. Range	Package	Media Type

Device:	MIC2168:	1 MHz PWM Synchronous Buck Control IC
Junction Temperature Range:	Y =	–40°C to +125°C, RoHS-Compliant
Package:	MM =	10-Lead MSOP
Media Type:	<blank>=	100/Tube
	TR =	2,500/Reel

Examples:

a) MIC2168YMM: MIC2168, –40°C to +125°C Temperature Range, 10-Lead MSOP, 100/Tube

b) MIC2168YMM-TR: MIC2168, –40°C to +125°C Temperature Range, 10-Lead MSOP, 2,500/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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