MIC59P60

8-Bit Serial-Input Protected Latched Driver

General Description

The MIC59P60 serial-input latched driver is a high-voltage (80V), high-current (500mA) integrated circuit comprised of eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, CLOCK, SERIAL DATA INPUT, and OUTPUT ENABLE functions. Similar to the MIC5842, additional protection circuitry supplied on this device includes thermal shutdown, under voltage lockout (UVLO), and over-current shutdown.

The bipolar/CMOS combination provides an extremely low-power latch with maximum interface flexibility. The MIC59P60 has open-collector outputs capable of sinking 500mA and integral diodes for inductive load transient suppression with a minimum output breakdown voltage rating of 80V (50V sustaining). The drivers can be operated with a split supply, where the negative supply is down to –20V and may be paralleled for higher load current capability.

Using a 5V logic supply, the MIC59P60 will typically operate at better than 5MHz. With a 12V logic supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL circuits may require pull-up resistors. By using the serial data output, drivers may be cascaded for interface applications requiring additional drive lines.

Each of these eight outputs has an independent over current shutdown of 500 mA. Upon over-current shutdown, the affected channel will turn OFF and the flag will go low until V_{DD} is cycled or the ENABLE/RESET pin is pulsed high. Current pulses less than 2µs will not activate current shutdown. Temperatures above 165°C will shut down the device and activate the error flag. The UVLO circuit prevents operation at low V_{DD}; hysteresis of 0.5V is provided.

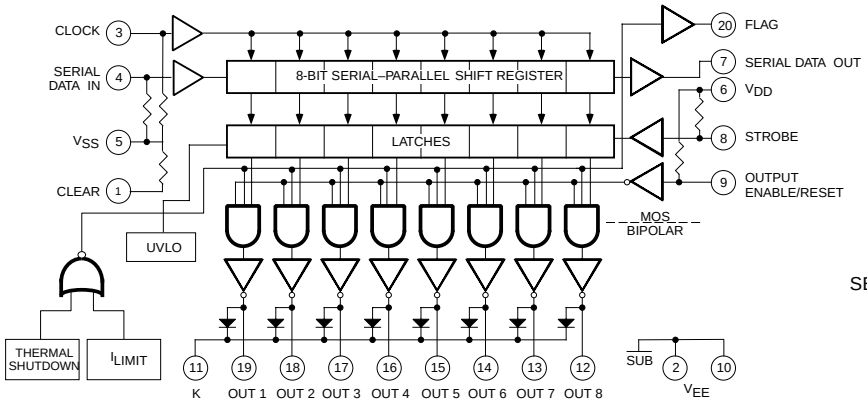
Features

- 3.3 MHz Minimum Data-Input Rate
- Output Current Shutdown (500mA Typical)
- Under Voltage Lockout
- Thermal Shutdown
- Output Fault Flag
- CMOS, PMOS, NMOS, and TTL Compatible
- Internal Pull-Up/Pull-Down Resistors
- Low Power CMOS Logic and Latches
- High Voltage Current Sink Outputs
- Output Transient-Protection Diodes
- Single or Split Supply Operation

Ordering Information

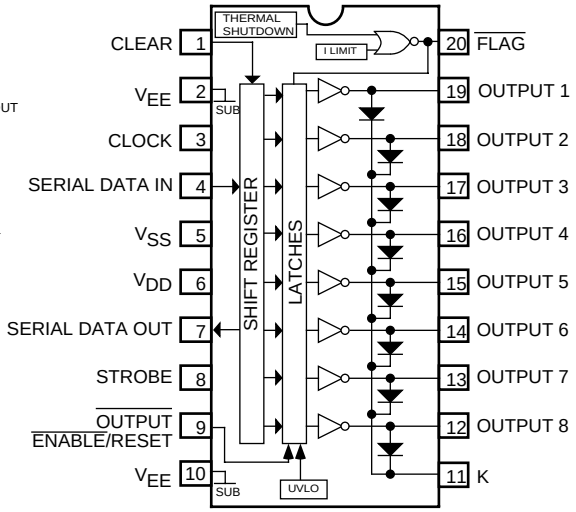
Part Number	Temperature Range	Package
MIC59P60BN	–40°C to +85°C	20-Pin Plastic DIP
MIC59P60BV	–40°C to +85°C	20-Pin PLCC
MIC59P60BWM	–40°C to +85°C	20-Pin Wide SOIC

Functional Diagram

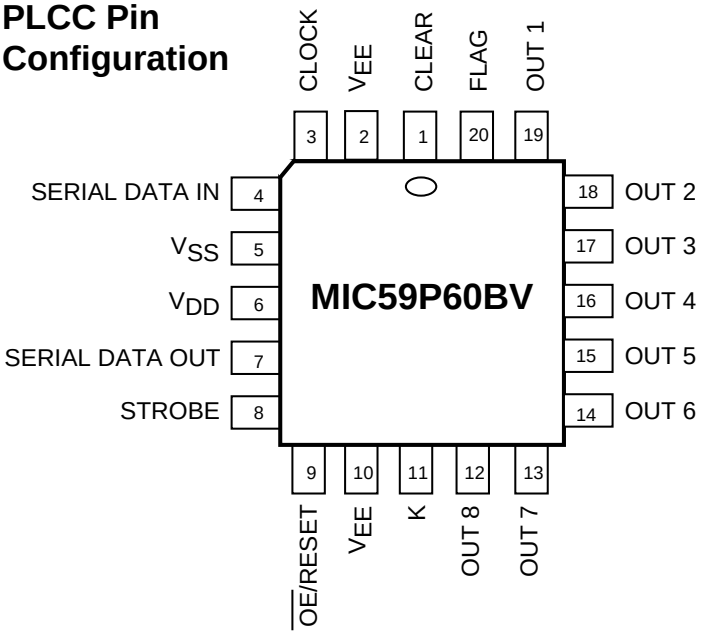


Pin Configuration

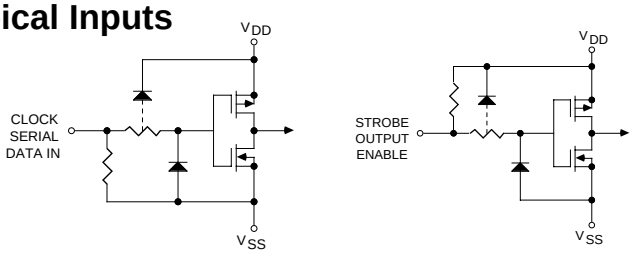
(DIP and SOIC)



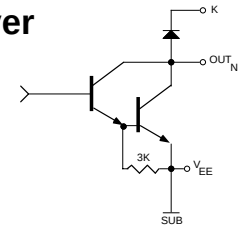
PLCC Pin Configuration



Typical Inputs



Typical Output Driver



Absolute Maximum Ratings V_{SS} = 0; T_A = 25°C

Output Voltage (V_{CE}) 80V
Output Voltage ($V_{CE(SUS)}$) ..... 50V, **Note 1**
V_{DD} with Reference to V_{SS} 15V
V_{DD} with Reference to V_{EE} 25V
Emitter Supply Voltage (V_{EE}) ..... –20V
Input Voltage (V_{IN}) ..... –0.3V to V_{DD}+0.3V
Protected Current ..... 1.5A, **Note 2**
Power Dissipation (P_D)
  Plastic DIP (N) 2.0W
    Derate above T_A = +25°C ..... 20mW/°C
  PLCC (V) 1.4W
    Derate above T_A = +25°C ..... 14mW/°C
  Wide SOIC (WM) 1.2W
    Derate above T_A = +25°C ..... 12mW/°C
Operating Temperature (T_A)
  Plastic DIP (N), PLCC (V), SOIC (WM) .. –40°C to +85°C
Storage Temperature (T_S) ..... –65°C to +150°C
Junction Temperature (T_J) ..... +150°C
ESD ..... **Note 3**

Note 1: For inductive load applications.
Note 2: Each channel. V_{EE} connection must be designed to minimize inductance and resistance.
Note 3: Devices are input-static protected but can be damaged by extremely high static charges.

Pin Description

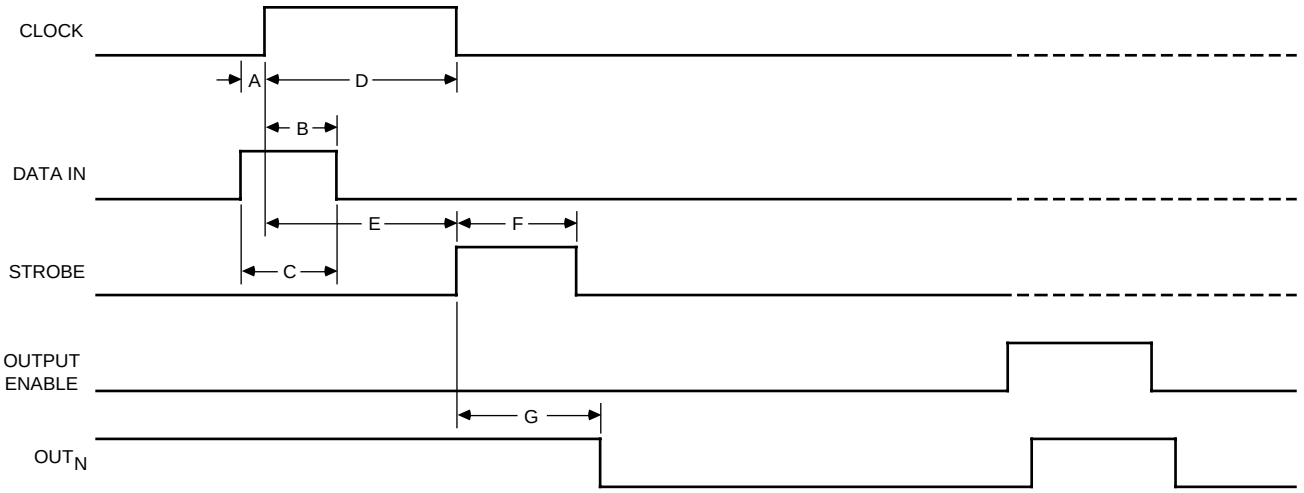
Pin	Name	Description
1	CLEAR	Sets All Latches OFF (open).
2,10	V_{EE}	Output Ground (Substrate). Most negative voltage in the system connects here.
3	CLOCK	Serial Data Clock. A CLEAR must also be clocked into the latches.
4	SERIAL DATA IN	Serial Data Input pin.
5	V_{SS}	Logic reference (Ground) pin.
6	V_{DD}	Logic Positive Supply voltage.
7	SERIAL DATA OUT	Serial Data Output pin. (Flow through).
8	STROBE	Output Strobe pin. Loads output latches when High. A STROBE is needed to CLEAR latches.
9	$\overline{\text{OUTPUT ENABLE}}$/RESET	When Low, Outputs are active. When High, device is inactive and reset from a fault condition. An under voltage condition emulates a high $\overline{\text{OE}}$/ RESET input.
11	K	Transient suppression diode's cathode common pin.
12—19	OUTPUT N	Open Collector outputs 8 through 1.
20	$\overline{\text{FLAG}}$	Error Flag. Open-collector output is Low upon Overcurrent Fault or Overtemperature fault. $\overline{\text{OUTPUT ENABLE}}$/RESET must be pulled high to reset the flag and fault condition.

Electrical Characteristics

V_{DD} = 5V, V_{SS} = V_{EE} = 0V; T_A = +25°C; unless noted.

			Limits			
Characteristic	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Output Leakage Current	I_{CEX}	V_{OUT} = 80V V_{OUT} = 80V, T_A = +70°C		 100	50	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 100mA I_{OUT} = 200mA I_{OUT} = 350mA		0.9 1.1 1.3	1.1 1.3 1.6	V
Collector-Emitter Sustaining Voltage	$V_{CE(SUS)}$	I_{OUT} = 350mA, L = 2mH	50			V
Input Voltage	$V_{IN(0)}$				1.0	V
	$V_{IN(1)}$	V_{DD} = 12V V_{DD} = 10V V_{DD} = 5.0V, **Note 4**	10.5 8.5 3.5			V
Input Resistance	R_{IN}	V_{DD} = 12V V_{DD} = 10V V_{DD} = 5.0V	50 50 50	200 300 600		kΩ
$\overline{\text{Flag}}$ Output Current	I_{OL}	V_{OL} = 0.4V		15		mA
$\overline{\text{Flag}}$ Output Leakage	I_{OH}	V_{OH} = 12.0V		50		nA
Supply Current	$I_{DD(ON)}$	All Drivers ON, V_{DD} = 12V All Drivers ON, V_{DD} = 10V All Drivers ON, V_{DD} = 5.0V		6.4 6.0 4.6	10.0 9.0 7.5	mA
	$I_{DD\ (1\ OUTPUT)}$	One Driver ON, All others OFF, V_{DD} = 12V One Driver ON, All others OFF, V_{DD} = 10V One Driver ON, All others OFF, V_{DD} = 5V		3.1 2.9 2.3	4.5 4.5 3.6	mA
	$I_{DD(OFF)}$	All Drivers OFF, V_{DD} = 12V All Drivers OFF, V_{DD} = 10V All Drivers OFF, V_{DD} = 5.0V		2.6 2.4 1.9	4.2 3.6 3.0	mA
Clamp Diode Leakage Current	I_R	V_R = 80V			50	µA
Clamp Diode Forward Voltage	V_F	I_F = 350mA		1.7	2.0	V
Over Current Shutdown Threshold	I_{LIM}			500		mA
Start Up Voltage	V_{SU}	**Note 5**	3.5	4.0	4.5	V
Minimum Supply (V_{DD})	$V_{DD\ MIN}$		3.0	3.5	4.0	V
Thermal Shutdown				165		°C
Thermal Shutdown Hysteresis				10		°C

Note 4: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".
Note 5: Undervoltage lockout is guaranteed to release device at no more than 4.5V, and disable the device at no less than 3.0V



Timing Conditions

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS}, V_{DD} = 5V)

A. Typical Data Active Time Before Clock Pulse (Data Set-Up Time) ..... 75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) ..... 75 ns
C. Minimum Data Pulse Width ..... 150 ns
D. Minimum Clock Pulse Width ..... 150 ns
E. Minimum Time Between Clock Activation and Strobe ..... 300 ns
F. Minimum Strobe Pulse Width ..... 100 ns
G. Typical Time Between Strobe Activation and Output Transition ..... 500 ns

SERIAL DATA present at the input is transferred to the shift register on the logic “0” to logic “1” transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform. Holding CLEAR high results in a data logic "0" being clocked into the shift register, turning off respective channels.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high to prevent invalid output states.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches. A positive OE/RESET pulse resets the FLAG and the output after a current shutdown fault. Over-temperature faults are not latched and require no reset pulse.

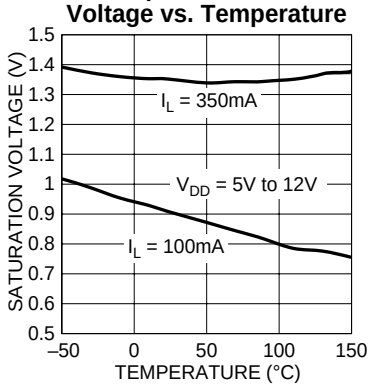
MIC59P60 Truth Table

Serial Data Input	Clear Input	Clock Input	Shift Register Contents					Serial Data Output	Strobe Input	Latch Contents					Output Enable	Output Contents				
			I_1	I_2	I_3	.....	I_8			I_1	I_2	I_3	.....	I_8		I_1	I_2	I_3	.....	I_8
H		⎍	H	R_1	R_2	.....	R_7	R_7												
L		⎍	L	R_1	R_2	.....	R_7	R_7												
X		⎎	R1	R2	R_3	.....	R_8	R_8												
	H	⎍	O	O	O	.....	O	L												
			X	X	X	.....	X	X	L	R_1	R_2	R_3	.....	R_8						
			P_1	P_2	P_3	.....	P_8	P_8	H	P_1	P_2	P_3	.....	P_8	L	P_1	P_2	P_3	.....	P_8
										X	X	X	.....	X	H	H	H	H	.....	H

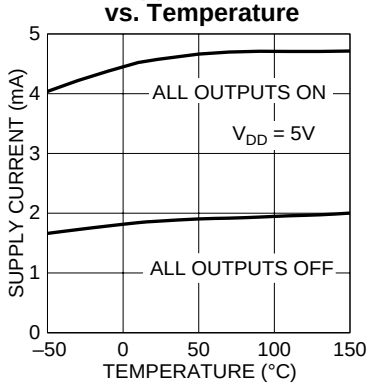
L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State
O = Output OFF

Typical Characteristic Curves

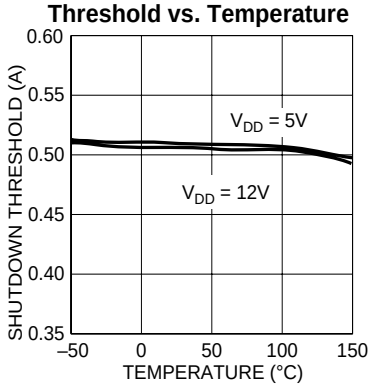
Output Saturation Voltage vs. Temperature



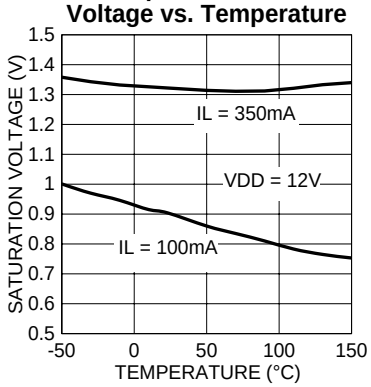
Supply Current vs. Temperature



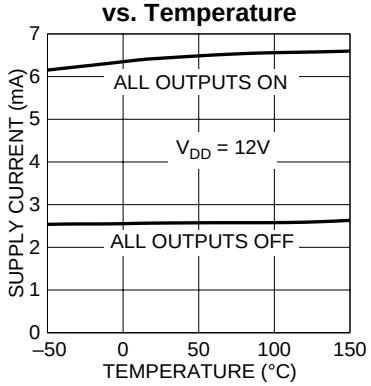
Current Shutdown Threshold vs. Temperature



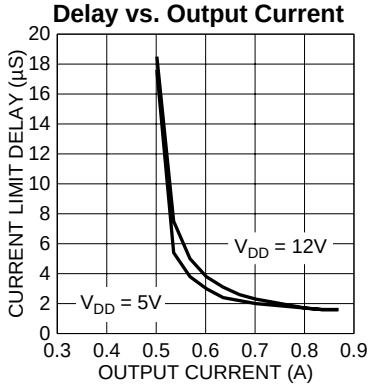
Output Saturation Voltage vs. Temperature



Supply Current vs. Temperature



Current Shutdown Delay vs. Output Current



Maximum Allowable Duty Cycle (Plastic DIP)

V_{DD} = 5.0V

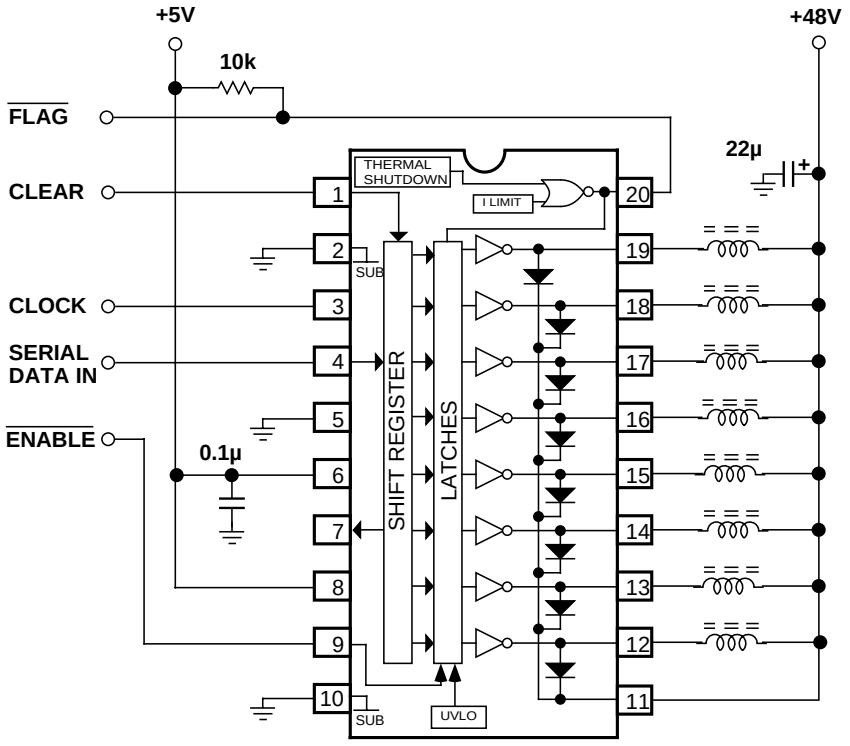
Number of Outputs ON (I_{OUT} = 200mA V_{DD} = 5.0V)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	85%	72%	64%	55%	46%
7	97%	82%	73%	63%	53%
6	100%	96%	85%	73%	62%
5	100%	100%	100%	88%	75%
4	100%	100%	100%	100%	93%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

V_{DD} = 12V

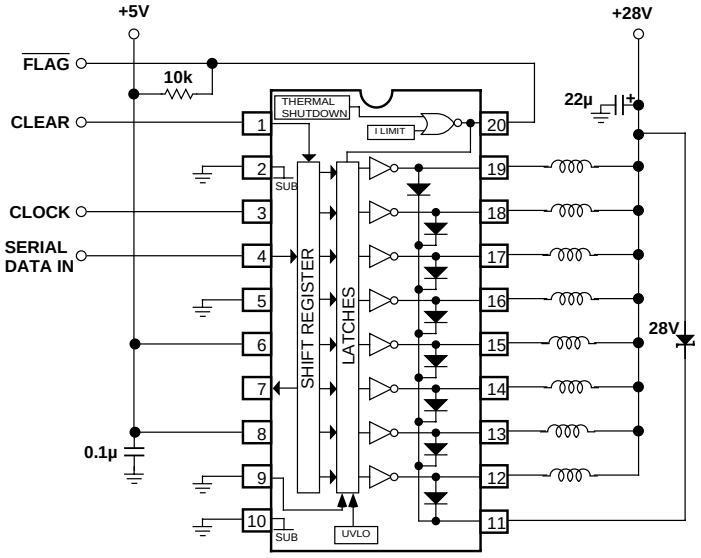
Number of Outputs ON (I_{OUT} = 200mA V_{DD} = 12V)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	80%	68%	60%	52%	44%
7	91%	77%	68%	59%	50%
6	100%	90%	79%	69%	58%
5	100%	100%	95%	82%	69%
4	100%	100%	100%	100%	86%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

Typical Applications

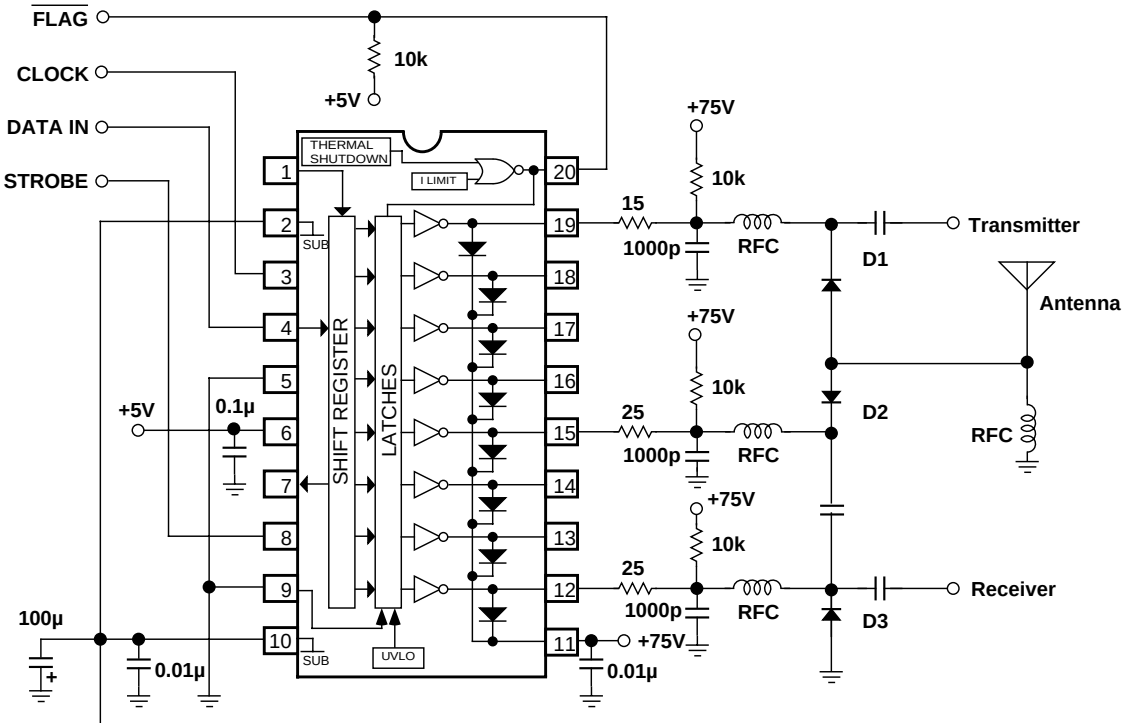
Protected Solenoid Driver with Output Enable



Hammer Driver



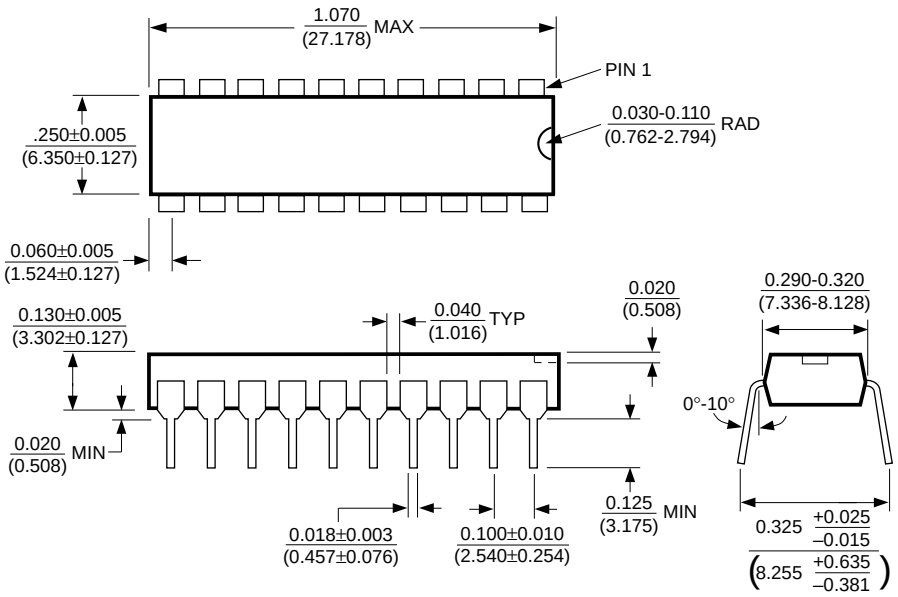
Protected Negative/Positive PIN Diode Driver Transmit/Receive Switch



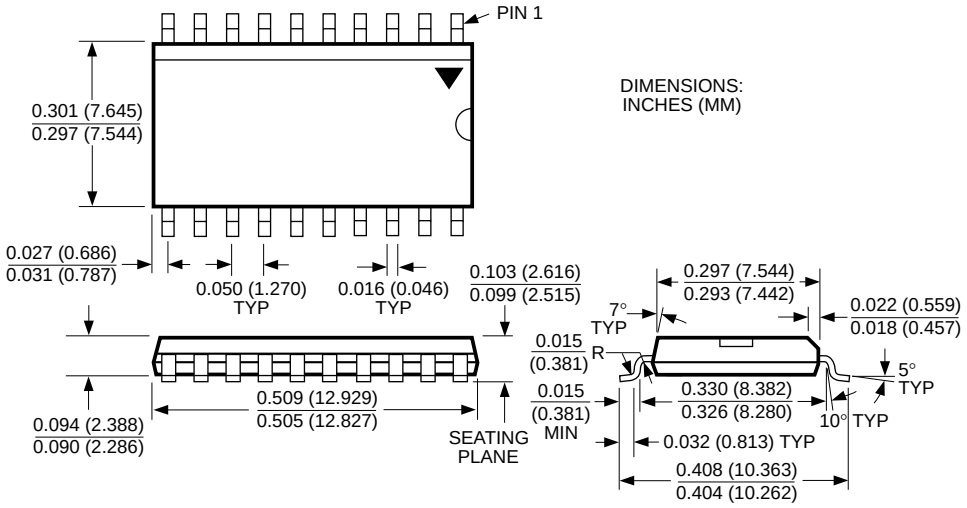
	Diode		
	D1 (Latch 1)	D2 (Latch 5)	D3 (Latch 8)
Receive	OFF	ACTIVE	OFF
Transmit	ACTIVE	OFF	ACTIVE

PIN Diodes: UM9651

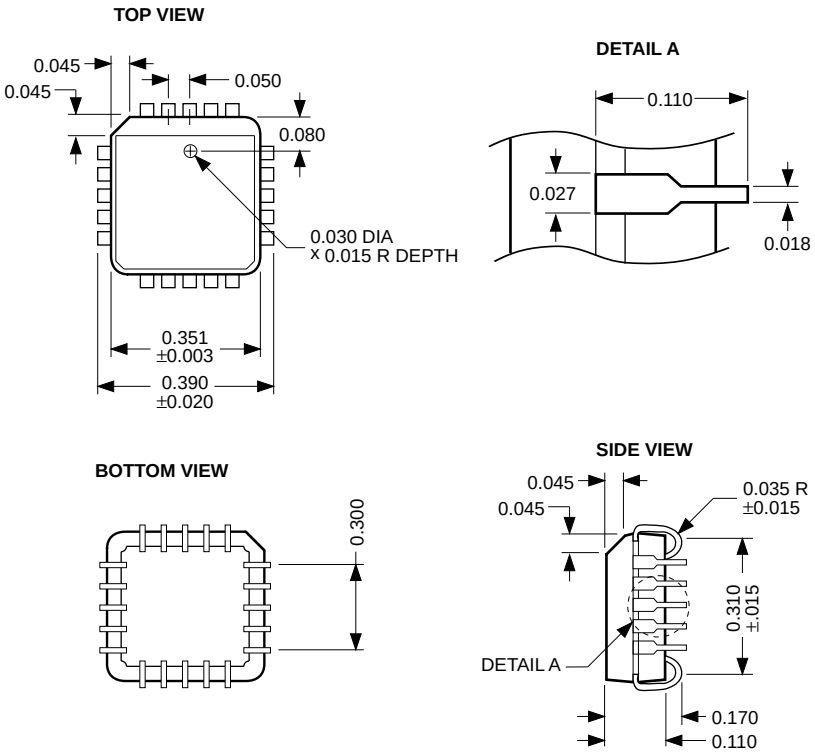
Package Information



20-Pin Plastic DIP (N)



20-Pin Wide SOP (WM)


TOP VIEW
0.045
0.045
0.050
0.080
0.030 DIA
x 0.015 R DEPTH
0.351
±0.003
0.390
±0.020
DETAIL A
0.110
0.027
0.018
BOTTOM VIEW
0.300
SIDE VIEW
0.045
0.045
0.035 R
±0.015
0.310
±.015
DETAIL A
0.170
0.110

20-Pin PLCC (V)

MICREL INC. 1849 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 944-0970 WEB http://www.micrel.com

This information is believed to be accurate and reliable, however no responsibility is assumed by Micrel for its use nor for any infringement of patents or other rights of third parties resulting from its use. No license is granted by implication or otherwise under any patent or patent right of Micrel Inc.

© 2001 Micrel Incorporated