MICRF600

902-928MHz ISM Band Transceiver Module

General Description

The MICRF600 is a self-contained frequency shift keying (FSK) transceiver module, intended for use in half-duplex, bidirectional RF links. The multi-channeled FSK transceiver module is intended for UHF radio equipment in compliance with the North American Federal Communications Commission (FCC) part 15.247 and 249.

The transmitter consists of a fully programmable PLL frequency synthesizer and power amplifier. The frequency synthesizer consists of a voltage-controlled oscillator (VCO), a crystal oscillator, dual modulus prescaler, programmable frequency dividers, and a phase-detector. The output power of the power amplifier can be programmed to seven levels. A lock-detect circuit detects when the PLL is in lock.

In receive mode, the PLL synthesizer generates the local oscillator (LO) signal. The N, M, and A values that give the LO frequency are stored in the N0, M0, and A0 registers.

The receiver is a zero intermediate frequency (IF) type that makes channel filtering possible with low-power, integrated low-pass filters. The receiver consists of a low noise amplifier (LNA) that drives a quadrature mix pair. The mixer outputs feed two identical signal channels in phase quadrature. Each channel includes a pre-amplifier, a third order Sallen-Key RC low-pass filter that protects the following switched-capacitor filter from strong adjacent channel signals, and a limiter. The main channel filter is a switched-capacitor implementation of a six-pole elliptic low pass filter. The cut-off frequency of the Sallen-Key RC filter can be programmed to four different frequencies: 100kHz, 150kHz, 230kHz, and 350kHz. The I and Q channel outputs are demodulated and produce a digital data output. The demodulator detects the relative phase of the I and the Q channel signal. If the I channel signal lags behind the Q channel, the FSK tone frequency is above the LO frequency (data "1"). If the I channel leads the Q channel, then the FSK tone is below the LO frequency (data "0"). The output of the receiver is available on the DataIXO pin. A receive signal strength indicator (RSSI) circuit indicates the received signal level. All support documentation can be found on Micrel's web site at: www.micrel.com.



RadioWire® Module

Features

- "Drop in" RF solution
- Small size: 11.5x14.1mm
- RF tested
- FCC Compliant
- Low Power
- Surface Mountable
- Tape & Reel
- Digital Bit Synchronizer
- Received Signal Strength Indicator (RSSI)
- RX and TX power management
- Power down function
- Register read back function

Applications

- Telemetry
- Remote metering
- Wireless controller
- Remote data repeater
- Remote control systems
- Wireless modem
- Wireless security system

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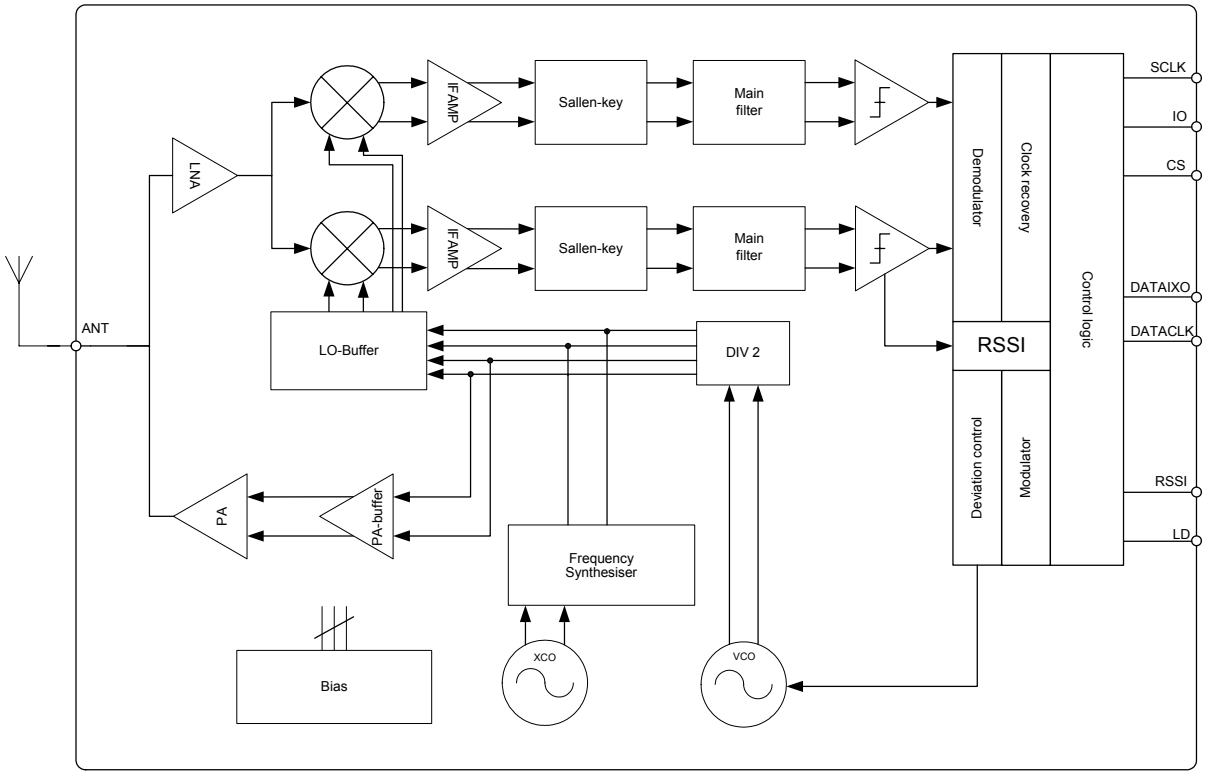
RadioWire® RF Module Selection Guide

Device	Frequency Range	Data Rate	Receive	Supply Voltage	Transmit	Modulation Type	Package
MICRF600	902-928 MHz	<20 kbps	13.5 mA	2.0-2.5 v	28 mA	FSK	11.5x14.1 mm
MICRF600Z	Lead-free MICRF600						
MICRF610	868-870 MHz	<15 kbps	13.5 mA	2.0-2.5 v	28 mA	FSK	11.5x14.1 mm
MICRF610Z	Lead-free MICRF610						
MICRF620	430-440 MHz	<20 kbps	12.0 mA	2.0-2.5 v	24 mA	FSK	11.5x14.1 mm
MICRF620Z	Lead-free MICRF620						
RFB433B	430-440 MHz	19.2 kbaud	8 mA	2.5-3.4 V	42 mA	FSK	1”x1”
RFB868B	868-870 MHz	19.2 kbaud	10 mA	2.5-3.4 V	50 mA	FSK	1”x1”
RFB915B	902-928 MHz	19.2 kbaud	10 mA	2.5-3.4 V	50 mA	FSK	1”x1”

Ordering Information

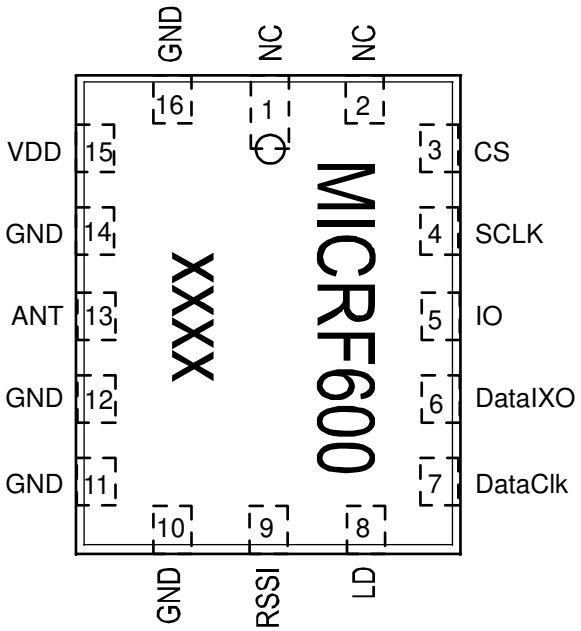
Part Number	Junction Temp. Range[1]	Package
MICRF600 TR	–20° to +75°C	11.5 x 14.1mm
MICRF600Z TR	–20° to +75°C	11.5 x 14.1mm

Block Diagram



MICRF600

Pin Configuration



MICRF600 TR
11.5 x 14.1 mm
(Top view)

Pin Description

Pin Number	Pin Name	Type	Pin Function
1	NC		Not connected
2	NC		Not connected
3	CS	I	Chip select, three wire programming interface
4	SCLK	I	Clock, three wire programming interface
5	IO	I/O	Data, three wire programming interface
6	DATAIXO	I/O	Data receive/transmit, bi-directional
7	DATACLK	O	Data clock receive/transmit
8	LD	O	Lock detect
9	RSSI	O	Receive signal strength indicator
10	GND		Ground
11	GND		Ground
12	GND		Ground
13	ANT	I/O	RF In/Out
14	GND		Ground
15	VDD		VDD (2.0-2.5V)
16	GND		Ground

Absolute Maximum Ratings[1]

Supply Voltage (V_{DD}).....+2.7V
Voltage on any pin (GND = 0V). .....-0.3V to 2.7V
Lead Temperature (soldering, 5 sec.).....+225°C
Storage Temperature (T_s) .....-30°C to +85°C
ESD Rating[3].....2kV

Operating Ratings[2]

Supply voltage (V_{IN}) .....+2.0V to +2.5V
RF Frequencies.....902MHz to 928MHz
Data Rate (NRZ) ..... <20 kbps
Ambient Temperature (T_A) .....–20°C to +75°C

Electrical Characteristics

f_{RF} = 915MHz, Data rate = 20kbps, V_{DD} = 2.5V; T_A = 25°C, **bold** values indicate –20°C≤ T_A ≤ +75°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Power Supply		**2.0**		**2.5**	V
	Power Down Current			0.3		µA
	Standby Current			280		µA
VCO and PLL Section						
	Crystal Oscillator Frequency	Tunable with on-chip cap bank		**16**		MHz
		Tuning range	-30		+40	ppm
	Crystal Initial Tolerance		**-10**		**+10**	ppm
	Crystal Temperature Tolerance		**-10**		**+10**	ppm
	Switch Time	Rx 915MHz – Rx 915.5MHz		**250**		µs
		Rx 903MHz – Rx 926MHz		**850**		µs
		Rx – Tx, same frequency		**200**		µs
		Tx – Rx, same frequency, time to good data		**300**		µs
		Standby – Rx,		1.0		ms
		Standby – Tx		1.0		ms
	Crystal Oscillator Start-Up Time	XCO_tune=13		750		µs
Transmit Section						
	Output Power	R_{LOAD} = 50Ω, Pa2-0-111		9		dBm
		R_{LOAD} = 50Ω, Pa2-0-001		-7		dBm
	Output Power Tolerance	Over temperature range		2		dB
		Over power supply range		3		dB
	Tx Current Consumption	R_{LOAD} = 50Ω, PA2_0: 111		28		mA
		R_{LOAD} = 50Ω, PA2_0: 001		14		mA
	Tx Current Consumption Variation	R_{LOAD} = 50Ω, PA2_0: 111		2.5		mA
	Binary FSK Frequency Separation [5]	Limited by receiver BW	**20**		**400**	kHz
	Data Rate[5]	NRZ	**0**		**20**	kbps
	Occupied bandwidth	20kbps, β = 10 (±100kHz), 20dBc (RBW=10kHz)		320		kHz
	2nd Harmonic	FCC part 15, R_{LOAD} = 50Ω			**-20**	dBc
	3rd Harmonic				**-41.2**	dBm
	Spurious Emission < 902 MHz				**-49.2**	dBm
	Spurious Emission > 928 MHz				**-41.2**	dBm

Symbol	Parameter	Condition		Min	Typ	Max	Units
Receive Section							
	Rx Current Consumption	All functions on			13.2		mA
		LNA bypass			10.9		mA
		Switch cap filter bypass with LNA			10.9		mA
		Bypass of Switch cap and LNA			8.6		mA
	Rx Current Consumption Variation	Over temperature			4		mA
	Receiver Sensitivity (BER < 10^{-3})	2.4 kbps, β = 16, SC=50 kHz			-111		dBm
		4.8 kbps, β = 16, SC=50 kHz			-110		dBm
		4.8 kbps, β = 4, SC=50 kHz			-109		dBm
		19.2 kbps, β =8, SC=200 kHz			-107		dBm
		19.2 kbps, β =2, SC=67 kHz			-104		dBm
	Receiver Maximum Input Power	19.2 kbps, β = 10			-10		dBm
	Receiver Sensitivity Tolerance	Over temperature			4		dB
		Over power supply range			1		dB
	Receiver Bandwidth			**50**		**350**	kHz
	Co-Channel Rejection	19.2 kbps, β = 8, SC=133 kHz			-9		dB
	Adjacent Channel Rejection	200 kHz spacing					
		500 kHz spacing					
		1 MHz spacing					
	Blocking	Desired signal: 19.2 kbps, β =8, 3dB above sens, SC=133 kHz	Offset ±1MHz		55		dB
			Offset ±2MHz		58		dB
			Offset ±5MHz		48		dB
			Offset ±10MHz		50		dB
			Offset ±30MHz		60		dB
	1dB Compression				-35		dB
	Input IP3	2 tones with 1MHz separation			-25		dBm
	Input IP2						dBm
	LO Leakage					-90	dBm
	Spurious Emission	< 902 MHz				**-49.2**	dBm
	(FCC part 15, R_{LOAD} = 50Ω)	> 928 MHz				**-41.1**	dBm
	Input Impedance[5]				41+j7		Ω
	RSSI Dynamic Range				50		dB
	RSSI Output Range	Pin = -110 dBm			0.9		V
		Pin = -60 dBm			1.9		V
Digital Inputs/Outputs							
	Logic Input High			$0.7V_{DD}$		V_{DD}	V
	Logic Input Low			0		$0.3V_{DD}$	V
	Clock/Data Frequency[4]					10	MHz
	Clock/Data Duty Cycle[4]			45		55	%

Notes:
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
4. Guaranteed by design.

Programming

General

The MICRF600 functions are enabled through a number of programming bits. The programming bits are organized as a set of addressable control registers, each register holding 8 bits.

There are 23 control registers in total in the MICRF600, and they have addresses ranging from 0 to 22. The user can read all the control registers. The user can write to the first 22 registers (0 to 21); the register 22 is a read-only register.

All control registers hold 8 bits and all 8 bits must be written to when accessing a control register, or they will be read. Some of the registers do not utilize all 8 bits. The value of an unused bit is “don’t care.”

The control register with address 0 is referred to as ControlRegister0, the control register with address 1 is ControlRegister1 and so on. A summary of the control registers is given in the table below. In addition to the unused bits (marked with”-“) there are a number of fixed bits (marked with “0” or “1”). Always maintain these as shown in the table.

The control registers in MICRF600 are accessed through a 3-wire interface; clock, data and chip select. These lines are referred to as SCLK, IO, and CS, respectively. This 3-wire interface is dedicated to control register access and is referred to as the control interface. Received data (via RF) and data to transmit (via RF) are handled by the DataIXO and DataClk (if enabled) lines; this is referred to as the data interface.

The SCLK line is applied externally; access to the control registers are carried out at a rate determined by the user. The MICRF600 will ignore transitions on the SCLK line if the CS line is inactive. The MICRF600 can be put on a bus, sharing clock and data lines with other devices.

All control registers should be written to after a battery reset. During operation, it is sufficient to write to one register only. The MICRF600 will automatically enter power down mode after a battery reset.

Address	**Data**							
A6…A0	D7	D6	D5	D4	D3	D2	D1	D0
0000000	LNA_by	PA2	PA1	PA0	Sync_en	Mode1	Mode0	‘1’
0000001	‘1’	‘0’	‘0’	‘0’	RSSI_en	LD_en	PF_FC1	PF_FC0
0000010	‘0’	‘SC_by’	‘0’	‘PA_by’	‘0’	‘0’	‘0’	‘0’
0000011	‘1’	‘1’	‘0’	VCO_IB2	VCO_IB1	VCO_IB0	VCO_freq1	VCO_freq0
0000100	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’
0000101	-	-	‘0’	‘1’	‘0’	‘0’	‘0’	‘0’
0000110	-	‘0’	‘0’	‘0’	BitSync_clkS2	BitSync_clkS1	BitSync_clkS0	BitRate_clkS2
0000111	BitRate_clkS1	BitRate_clkS0	RefClk_K5	RefClk_K4	RefClk_K3	RefClk_K2	RefClk_K1	RefClk_K0
0001000	‘1’	‘1’	ScClk5	ScClk4	ScClk3	ScClk2	ScClk1	ScClk0
0001001	‘0’	‘0’	‘1’	XCOtune4	XCOtune3	XCOtune2	XCOtune1	XCOtune0
0001010	-	-	A0_5	A0_4	A0_3	A0_2	A0_1	A0_0
0001011	-	-	-	-	N0_11	N0_10	N0_9	N0_8
0001100	N0_7	N0_6	N0_5	N0_4	N0_3	N0_2	N0_1	N0_0
0001101	-	-	-	-	M0_11	M0_10	M0_9	M0_8
0001110	M0_7	M0_6	M0_5	M0_4	M0_3	M0_2	M0_1	M0_0
0001111	-	-	A1_5	A1_4	A1_3	A1_2	A1_1	A1_0
0010000	-	-	-	-	N1_11	N1_10	N1_9	N1_8
0010001	N1_7	N1_6	N1_5	N1_4	N1_3	N1_2	N1_1	N1_0
0010010	-	-	-	-	M1_11	M1_10	M1_9	M1_8
0010011	M1_7	M1_6	M1_5	M1_4	M1_3	M1_2	M1_1	M1_0
0010100	‘1’	‘0’	‘1’	‘1’	‘0’	‘1’	‘0’	‘1’
0010101	-	-	-	-	FEEC_3	FEEC_2	FEEC_1	FEEC_0
0010110	FEE_7	FEE_6	FEE_5	FEE_4	FEE_3	FEE_2	FEE_1	FEE_0

Table 1. Control Registers in MICRF600

Writing to the Control Registers in MICRF600

Writing: A number of octets are entered into MICRF600, followed by a load-signal to activate the new setting. Making these events is referred to as a "write sequence." It is possible to update all, 1, or n control registers in a write sequence. The address to write to (or the first address to write to) can be any valid address (0-21). The IO line is always an input to the MICRF600 (output from user) when writing.

What to write:

- The address of the control register to write to (or if more than 1 control register should be written to, the address of the 1st control register to write to).
- A bit to enable reading or writing of the control registers. This bit is called the R/W bit.
- The values to write into the control register(s).

Field	Comments
Address:	A 7-bit field, ranging from 0 to 21. MSB is written first.
R/W bit:	A 1-bit field, = "0" for writing
Values:	A number of octets (1-22 octets). MSB in every octet is written first. The first octet is written to the control register with the specified address (="Address"). The next octet (if there is one) is written to the control register with address = "Address + 1" and so on.

Table 2. Writing to the Control Registers

How to write:

Bring CS active to start a write sequence. The active state of the CS line is "high." Use the SCLK/IO serial interface to clock "Address" and "R/W" bit and "Values" into the MICRF600. MICRF600 will sample the IO line at negative edges of SCLK. Make sure to change the state of the IO line before the negative edge. Refer to figures below.

Bring CS inactive to make an internal load-signal and complete the write-sequence.

The two different ways to "program the chip" are:

- Write to a number of control registers (0-22) when the registers have incremental addresses (write to 1, all or n registers)
- Write to a number of control registers when the registers have non-incremental addresses.

Writing to a Single Register

Writing to a control register with address "A6. A5, …A0" is described here. During operation, writing to 1 register is sufficient to change the way the transceiver works. Typical example: Change from receive mode to power-down.

Field	Comments
Address:	7 bit = A6, A5, …A0 (A6 = msb. A0 = lsb)
R/W bit:	"0" for writing
Values:	8 bits = D7, D6, …D0 (D7 = msb, D0 = lsb)

Table 3. "Address" and "R/W bit" together make 1 octet.

In addition, 1 octet with programming bits is entered. Totally, 2 octets are clocked into the MICRF600.

How to write:

- Bring CS high
- Use SCLK and IO to clock in the 2 octets
- Bring CS low

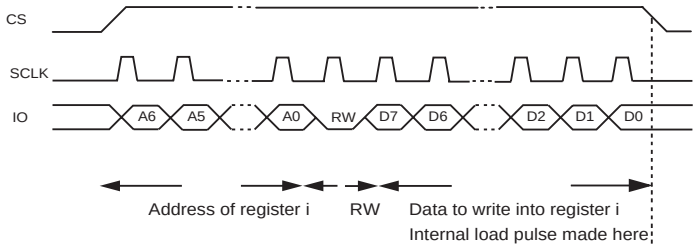


Figure 1. How to write to a single Control Register

In Figure 1, IO is changed at positive edges of SCLK. The MICRF600 samples the IO line at negative edges. The value of the R/W bits is always "0" for writing.

Writing to All Registers

After a power-on, all writable registers must be written. This is described here.

Writing to all register can be done at any time. To get the simplest firmware, always write to all registers. The price to pay for the simplicity is increased write-time, which leads to increased time for changing the way the MICRF600 works.

What to write

Field	Comments
Address:	'000000' (address of the first register to write to, which is 0)
R/W bit:	"0" for writing
Values:	1st Octet: wanted values for ControlRegister0. 2nd Octet: wanted values for ControlRegister1 and so on for all of the octets. So the 22nd octet: wanted values for ControlRegister21. Refer to the specific sections of this document for actual values.

Table 4. "Address" and "R/W bit" together make 1 octet.

In total, 23 octets are clocked into the MICRF600.

How to write:

- Bring CS high
- Use SCLK and IO to clock in the 23 octets
- Bring CS low

Refer to the figure in the next section, "Writing to n registers having incremental addresses".

Writing to n Registers Having Incremental Addresses

In addition to entering all bytes, it is also possible to enter a set of n bytes, starting from address i = "A6, A5, … A0". Typical example: Clock in a new set of frequency dividers (i.e. change the RF frequency). "Incremental addresses". Registers to be written are located in i, i+1, i+2.

What to write:

Field	Comments
Address:	7 bit = A6, A5, …A0 (A6 = msb. A0 = lsb) (address of first byte to write to)
R/W bit:	"0" for writing
Values:	n* 8 bits =
	D7, D6, …D0 (D7 = msb, D0 = lsb) (written to control reg. with address "i")
	D7, D6, …D0 (D7 = msb, D0 = lsb) (written to control reg. with address "i+1")
	D7, D6, …D0 (D7 = msb, D0 = lsb) (written to control reg. with address "i+n-1")

Table 5. "Address" and "R/W bit" together make 1 octet.

In addition, n octets with programming bits are entered. Totally. 1 +n octets are clocked into the MICRF600.

How to write:

- Bring CS high
- Use SCLK and IO to clock in the 1 + n octets
- Bring CS low

In Figure 1, IO is changed at positive edges of SCLK. The MICRF600 samples the IO line at negative edges. The value of the R/W bits is always "0" for writing.

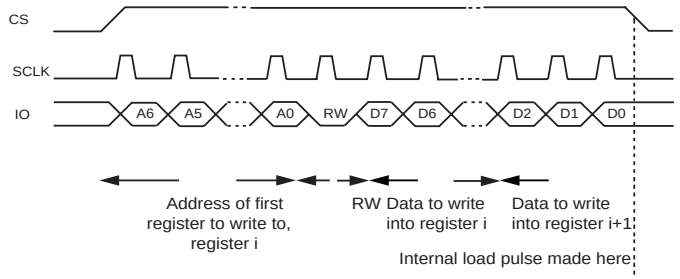


Figure 2. How to write to many Control Registers

Reading from the Control Registers in MICRF600

The "read-sequence" is:

1. Enter address and R/W bit
2. Change direction of IO line
3. Read out a number of octets and change IO direction back again.

It is possible to read all, 1 or n registers. The address to read from (or the first address to read from) can be any valid address (0-22). Reading is not destructive, i.e. values are not changed. The IO line is output from the MICRF600 (input to user) for a part of the read-sequence. Refer to procedure description below.

A read-sequence is described for reading n registers, where n is number 1-23.

Reading n Registers from MICRF600

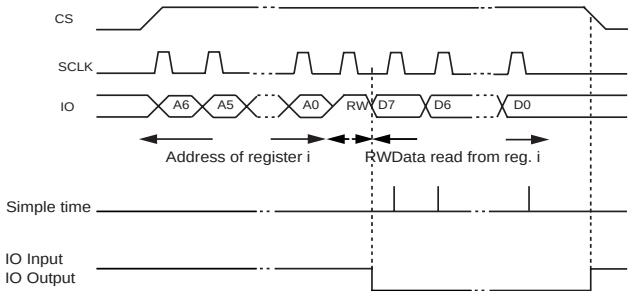


Figure 3. How to read from many Control Registers

In Figure 3, 1 register is read. The address is A6, A5, … A0. A6 = msb. The data read out is D7, D6, …D0. The value of the R/W bit is always "1" for reading.

SCLK and IO together form a serial interface. SCLK is applied externally for reading as well as for writing.

- Bring CS active
- Enter address to read from (or the first address to read from) (7 bits) and
- The R/W bit = 1 to enable reading
- Make the IO line an input to the user (set pin in tristate)
- Read n octets. The first rising edge of SCLK will set the IO as an output from the MICRF600. MICRF will change the IO line at positive edges. The user should read the IO line at the negative edges.
- Make the IO line an output from the user again.

Programming Interface Timing

Figure 4 and Table 6 show the timing specification for the 3-wire serial programming interface.

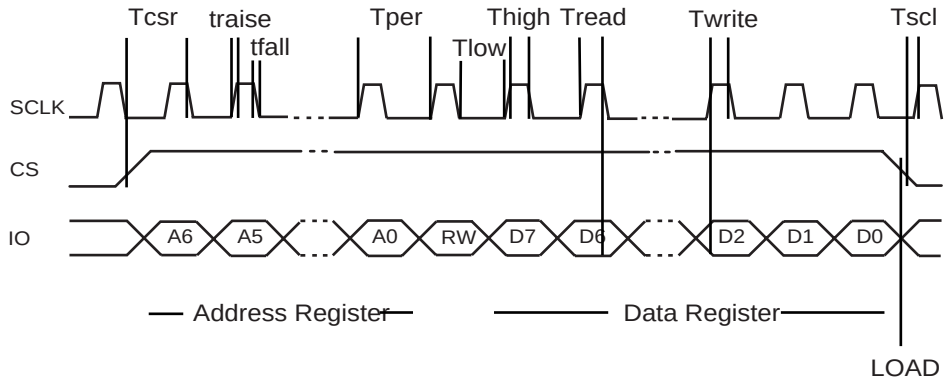


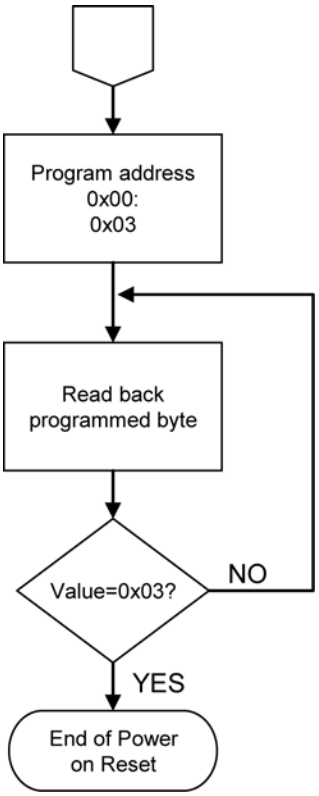
Figure 4. Programming Interface Timing

Symbol	Parameter	Values			Units
		Min.	Typ.	Max.	
Tper	Min. period of SCLK (Voltage dividers on IO lines will slow down the write/read frequency)	50			ns
Thigh	Min. high time of SCLK	20			ns
Tlow	Min. low time of SCLK	20			ns
tfall	Max. time of falling edge of SCLK			1	µs
trise	Max. time of rising edge of SCLK			1	µs
Tcsr	Max. time of rising edge of CS to falling edge of SCLK	0			ns
Tcsf	Min. delay from rising edge of CS to rising edge of SCLK	5			ns
Twrite	Min. delay from valid IO to falling edge of SCLK during a write operation	0			ns
Tread	Min. delay from rising edge of SCLK to valid IO during a read operation (assuming load capacitance of IO is 25pF)	75			ns

Table 6. Timing Specification for the 3-wire Programming Interface

Power on Reset

When applying voltage to the MICRF600 a power on reset state is entered. During the time period of power on reset, the MICRF600 should be considered to be in an unknown state and the user should wait until completed (See Table 6). The power on reset timing given in table 6 is covering all conditions and should be treated as a maximum delay time. In some application it might be beneficial to minimize the power on reset time. In these cases we recommend to follow below procedure:



Programming Summary

- Use CS, SCLK, and IO to get access to the control registers in MICRF600.
- SCLK is user-controlled.
- Write to the MICRF600 at positive edges (MICRF600 reads at negative edges).
- Read from the MICRF600 at negative edges (MICRF600 writes at positive edges)
- After power-on: Write to the complete set of control registers.
- Address field is 7 bits long. Enter msb first.
- R/W bit is 1 bit long (“1” for read, “0” for write)
- Address and R/W bit together make 1 octet
- All control registers are 8 bits long. Enter/read msb in every octet first.
- Always write 8 bits to/read 8 bits from a control register. This is the case for registers with less than 8 used programming bits as well.
- Writing: Bring CS high, write address and R/W bit followed by the new values to fill into the addressed control register(s) and bring CS low for loading, i.e., activation of the new control register values.
- Reading: Bring CS high, write address and R/W bit, set IO as an input, read present contents of the addressed control register(s), bring CS low and set IO an output.

Frequency Synthesizer

A6…A0	D7	D6	D5	D4	D3	D2	D1	D0
0001010	-	-	A0_5	A0_4	A0_3	A0_2	A0_1	A0_0
0001011	-	-	-	-	N0_11	N0_10	N0_9	N0_8
0001100	N0_7	N0_6	N0_5	N0_4	N0_3	N0_2	N0_1	N0_0
0001101	-	-	-	-	M0_11	M0_10	M0_9	M0_8
0001110	M0_7	M0_6	M0_5	M0_4	M0_3	M0_2	M0_1	M0_0
0001111	-	-	A1_5	A1_4	A1_3	A1_2	A1_1	A1_0
0010000	-	-	-	-	N1_11	N1_10	N1_9	N1_8
0010001	N1_7	N1_6	N1_5	N1_4	N1_3	N1_2	N1_1	N1_0
0010010	-	-	-	-	M1_11	M1_10	M1_9	M1_8
s0010011	M1_7	M1_6	M1_5	M1_4	M1_3	M1_2	M1_1	M1_0

The frequency synthesizer consists of a voltage-controlled oscillator (VCO), a crystal oscillator, phase select prescaler, programmable frequency dividers and a phase-detector. The length of the N, M, and A registers are 12, 12 and 6 respectively. The N, M, and A values can be calculated from the formula:

$$f_{PhD} = \frac{f_{XCO}}{M} = \frac{f_{VCO}}{(16 \times N + A) \times 2} = \frac{f_{RF}}{(16 \times N + A)},$$

$$M \neq 0$$

$$1 \leq A < N$$

f_{PHD}: Phase detector comparison frequency

f_{XCO}: Crystal oscillator frequency

f_{VCO}: Voltage controlled oscillator frequency

f_{RF}: Input/output RF frequency

There are two sets of each of the divide factors (i.e. A0 and A1). Storing the '0' and the '1' frequency in the 0- and the 1 registers respectively, does the 2-FSK. The receive frequency must be stored in the '0' registers.

Crystal Oscillator (XCO)

Adr	D7	D6	D5	D4	D3	D2	D1	D0
0001001	'0'	'0'	'1'	XCOtune4	XCOtune3	XCOtune2	XCOtune1	XCOtune0

The crystal oscillator is a reference for the RF output frequency and the LO frequency in the receiver. It is possible to tune the internal crystal oscillator by switching in internal capacitance using 5 tune bits XCOtune4 – XCOtun0. The benefit of tuning the crystal oscillator is to eliminate the initial tolerance and the tolerance over temperature and aging. By using the crystal tuning feature the noise bandwidth of the receiver can be reduced and a higher sensitivity is achieved. When XCOtune4 – XCOtune0 = 0 no internal capacitors are connected to the crystal pins. When XCOtune4 – XCOtune0 = 1 all of the internal capacitors are connected to the crystal pins. Figure 5 shows the tuning range.

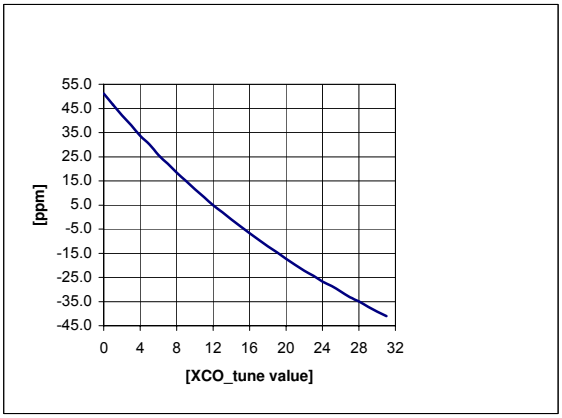


Figure 5. XCO Tuning

The typical start up time for the crystal oscillator (default XCO_tune=13) is ~750us. If more capacitance is added (higher XCO_tune value), then the start-up time will be longer.

To save current in the crystal oscillator start-up period, the XCO is turned on before any other circuit block. When the XCO has settled, rest of the circuit will be turned on. No programming should be made during this period.

The current consumption during the prestart period is approximately 280µA.

VCO

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000011	'1'	'1'	'0'	VCO_IB2	VCO_IB1	VCO_IB0	VCO_freq1	VCO_freq0

The VCO has no external components. It has three bit to set the bias current and two bit to set the VCO frequency. These five bits are set by the RF frequency, as follows:

RF freq.	VCO_IB2	VCO_IB1	VCO_IB0	VCO_freq1	VCO_freq0
915MHz	0	0	1	1	0
950MHz	0	0	0	1	1

Table 7. VCO Bit Setting

The bias bit will optimize the phase noise, and the frequency bit will control a capacitor bank in the VCO. The tuning range the RF frequency versus varactor voltage is dependent on the VCO frequency setting, and can be shown in Figure 6.

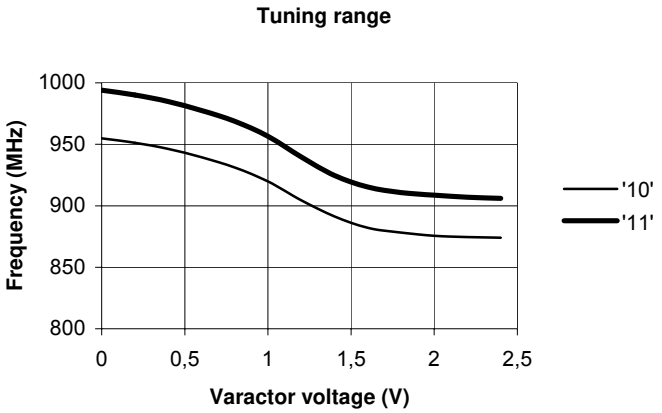


Figure 6. RF Frequency vs. Varactor Voltage and VCO Frequency bit (V_{DD} = 2.25V)

Lock Detect

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000001	'1'	'0'	'0'	'0'	RSSI_en	LD_en	PF_FC1	PF_FC0

A lock detector can be enabled by setting LD_en = 1. When pin LD is high, it indicates that the PLL is in lock.

When entering TX, the procedure is first to load the TX word and then turn on the PA stage. During the PA ramp up time, the LD signal may indicate out of lock. It is first when the PA stage is fully on that the LD signal will indicate in "Lock". During transmission, the Lock Detect signal will have transitions and the user should therefore, ignore the Lock detect signal.

Modes of Operation

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000000	LNA_by	PA2	PA1	PA0	Sync_en	Mode1	Mode0	'1'

Mode1	Mode0	State	Comments
0	0	Power down	Keeps register configuration
0	1	Standby	Only crystal oscillator running
1	0	Receive	Full receive
1	1	Transmit	Full transmit ex PA state

Transceiver Sync/Non-Synchronous Mode

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000000	LNA_by	PA2	PA1	PA0	Sync_en	Mode1	Mode0	'1'
0000110	-	'0'	'0'	'0'	BitSync_clkS2	BitSync_clkS1	BitSync_clkS0	BitRate_clkS2
0000111	BitRate_clkS1	BitRate_clkS0	RefClk_K5	RefClk_K4	RefClk_K3	RefClk_K2	RefClk_K1	RefClk_K0

Sync_en	State	Comments
0	Rx: Bit synchronization off	Transparent reception of data
0	Tx: DataClk pin off	Transparent transmission of data
1	Rx: Bit synchronization on	Bit-clock is generated by transceiver
1	Tx: DataClk pin on	Bit-clock is generated by transceiver

When Sync_en = 1, it will enable the bit synchronizer in receive mode. The bit synchronizer clock needs to be programmed, see chapter Bit synchronizer. The synchronized clock will be set out on pit DataClk.

In transmit mode, when Sync_en = 1, the clock signal on pin DataClk is a programmed bit rate clock. Now the transceiver controls the actual data rate. The data to be transmitted will be sampled on rising edge of DataClk. The micro controller can therefore use the negative edge to change the data to be transmitted. The clock used for this purpose, BitRate-clock, is programmed in the same way as the modulator clock and the bit synchronizer clock:

$$f_{BITRATE_CLK} = \frac{f_{XCO}}{Refclk_K \times 2^{(7\text{-}BITRATE_clkS)}}$$

where:

$f_{BITRATE_CLK}$: The clock frequency used to control the bit rate, should be equal to the bit rate (bit rate of 20 kbit/sec requires a clock frequency of 20kHz)

f_{XCO}: Crystal oscillator frequency

Refclk_K: 6 bit divider, values between 1 and 63

BitRate_clkS: Bit rate setting, values between 0 and 6

Data Interface

The MICRF600 interface can be divided in to two separate interfaces, a "programming interface" and a "Data interface". The "programming interface" has a three wire serial programmable interface and is described in chapter Programming.

The "data interface" can be programmed to sync-/non-synchronous mode. In synchronous mode the MICRF600 is defined as "Master" and provides a data clock that allows users to utilize low cost micro controller reference frequency.

The data interface is defined in such a way that all user actions should take place on falling edge and is illustrated Figure 7 and 8. The two figures illustrate the relationship between DATACLK and DATAIXO in receive mode and transmit mode.

MICRF600 will present data on rising edge and the "USER" sample data on falling edge in receive mode.

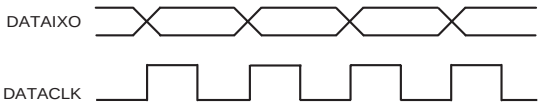


Figure 7. Data interface in Receive Mode

The User presents data on falling edge and MICRF600 samples on rising edge in transmit mode.

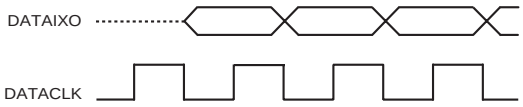


Figure 8. Data interface in Transmit Mode

Receiver

The receiver is a zero intermediate frequency (IF) type in order to make channel filtering possible with low-power integrated low-pass filters. The receiver consists of a low noise amplifier (LNA) that drives a quadrature mixer pair. The mixer outputs feed two identical signal channels in phase quadrature. Each channel includes a pre-amplifier, a third order Sallen-Key RC lowpass filter from strong adjacent channel signals and finally a limiter. The main channel filter is a switched-capacitor implementation of a six-pole elliptic lowpass filter. The elliptic filter minimizes the total capacitance required for a given selectivity and dynamic range. The cut-off frequency of the Sallen-Key RC filter can be programmed to four different frequencies: 100kHz, 150kHz, 230kHz and 340kHz. The demodulator demodulates the I and Q channel outputs and produces a digital data output. If detects the relative phase of the I and Q channel signal. If the I channel signal lags the Q channel, the FSK tone frequency lies above the LO frequency (data '1'). If the I channel leads the Q channel, the FSK tone lies below the LO frequency (data '0'). The output of the receiver is available on the DataIXO pin. A RSSI circuit (receive signal strength indicator) indicates the received signal level.

Front End

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000000	LNA_by	PA2	PA1	PA0	Sync_en	Mode1	Mode0	'1'

A low noise amplifier in RF receivers is used to boost the incoming signal prior to the frequency conversion process. This is important in order to prevent mixer noise from dominating the overall front-end noise performance. The LNA is a two-stage amplifier and has a nominal gain of approximately 23dB at 900MHz. The front end has a gain of about 33dB to 35dB. The gain varies by 1-1.5dB over a 2.0V to 2.5V variation in power supply.

The LNA can be bypassed by setting bit LNA_by to '1'. This can be useful for very strong input signal levels. The front-end gain with the LNA bypassed is about 9-10dB. The mixers have a gain of about 10dB at 900MHz. The input impedance is shown in Figure 9.

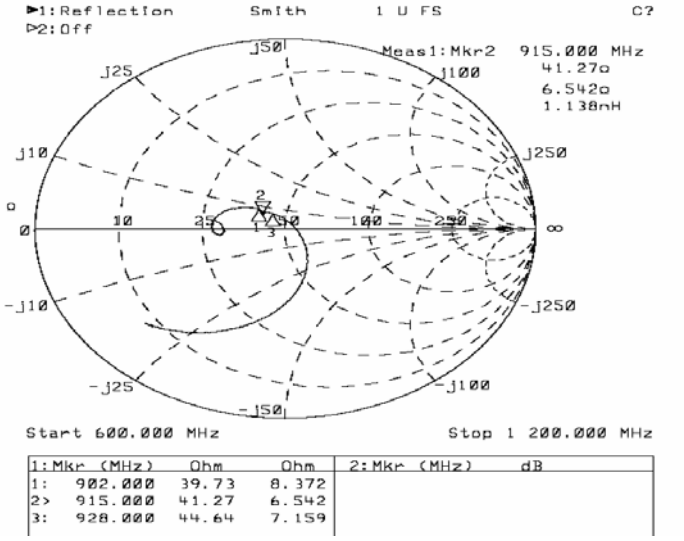


Figure 9. Input Impedance

Sallen-Key Filters

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000001	'1'	'0'	'0'	'0'	RSSI_en	LD_en	PF_FC1	PF_FC0

Each channel includes a pre-amplifier and a prefilter, which is a three-pole Sallen-Key lowpass filter. It protects the following switched-capacitor filter from strong adjacent channel signals, and it also works as an anti-aliasing filter. The preamplifier has a gain of 22.23dB. The maximum output voltage swing is about 1.4Vpp for a 2.25V power supply. In addition, the IF amplifier also performs offset cancellation. Gain varies by less than 0.5dB over a 2.0 – 2.5V variation in power supply. The third order Sallen-Key lowpass filter is programmable to four different cut-off frequencies according to the table below:

PF_FC1	PF_FC0	Cut-off Freq. (kHz)
0	0	100
0	1	150
1	0	230
1	1	340

Switched Capacitor Filter

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0001000	'1'	'1'	ScClk5	ScClk4	ScClk3	ScClk2	ScClk1	ScClk0

The main channel filter is a switched-capacitor implementation of a six-pole elliptic low pass filter. The elliptic filter minimized the total capacitance required for a given selectivity and dynamic range. The cut-off frequency of the switched-capacitor filter is adjustable by changing the clock frequency.

The clock frequency is designed to be 20 times the cut-off frequency. The clock frequency is derived from the reference crystal oscillator. A programmable 6-bit divider divides the frequency of the crystal oscillator. The cut-off frequency of the filter is given by:

$$f_{CUT} = \frac{f_{XCO}}{40 \cdot ScClk}$$

f_{CUT}: Filter cutoff frequency

f_{XCO}: Crystal oscillator frequency

ScCLK: Switched capacitor filter clock, bits ScClk5-0

1st order RC lowpass filters are connected to the output of the SC filter to filter the clock frequency.

The lowest cutoff frequency in the pre- and the main channel filter must be set so that the received signal is passed with no attenuation, that is frequency deviation plus modulation. If there are any frequency offset between the transmitter and the receiver, this must also be taken into consideration. A formula for the receiver bandwidth can be summarized as follows:

$$f_{BW} = + f_{OFFSET} + f_{DEV} + Baudrate / 2$$

where

f_{BW}: Needed receiver bandwidth, fcut above should not be smaller than f_{BW} (Hz)

f_{offset}: Total frequency offset between receiver and transmitter (Hz)

f_{DEV}: Single-sided frequency deviation

Baudrate: The baud rate given is bit/sec

In battery operated applications that do not need very high selectivity, the main channel filter can be bypassed by SC_by=1. This will reduce the Rx current consumption with ~2mA.

RSSI

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000001	'1'	'0'	'0'	'0'	RSSI_en	LD_en	PF_FC1	PF_FC0

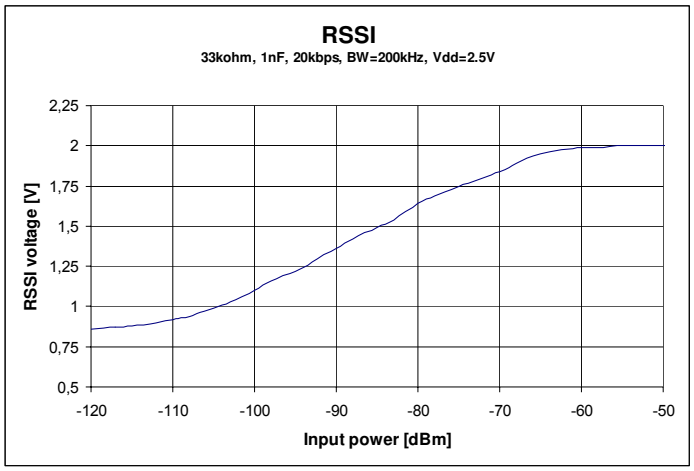


Figure 10. RSSI Voltage

A Typical plot of the RSSI voltage as function of input power is shown in Figure 10. The RSSI has a dynamic range of about 50dB from about -110dBm to -60dBm input power.

The RSSI can be used as a signal presence indicator. When a RF signal is received, the RSSI output increases. This could be used to wake up circuitry that is normally in a sleep mode configuration to conserve battery life.

Another application for which the RSSI could be used is to determine if transmit power can be reduced in a system. If the RSSI detects a strong signal, it could tell the transmitter to reduce the transmit power to reduce current consumption.

FEE

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0010101	-	-	-	-	FEEC_3	FEEC_2	FEEC_1	FEEC_0
0010110	FEE_7	FEE_6	FEE_5	FEE_4	FEE_3	FEE_2	FEE_1	FEE_0

The Frequency Error Estimator (FEE) uses information from the demodulator to calculate the frequency offset between the receive frequency and the transmitter frequency. The output of the FEE can be used to tune the XCO frequency, both for production calibration and for compensation for crystal temperature drift and aging.

The input to the FEE circuit are the up and down pulses from the demodulator. Every time a '1' is updated, an UP-pulse is coming out of the demodulator and the same with the DN-pulse every time the '0' is updated. The expected no. of pulses for every received symbol is 2 times the modulation index (Δ).

The FEE can operate in three different modes; counting only UP-pulses, only DN-pulses or counting UP+DN pulses. The no. of received symbols to be counted is either 8, 16, 32 or 64. This is set by the FEEC_0…FEEC_3 control bit, as follows:

FEEC_1	FEEC_0	FEE Mode
0	0	Off
0	1	Counting UP pulses
1	0	Counting DN pulses
1	1	Counting UP and DN pulses. UP increments the counter, DN decrements it.
FEEC_3	**FEEC_2**	**No. of symbols used for the measurement**
0	0	8
0	1	16
1	0	32
1	1	65

Table 8. FEEC Control Bit

The result of the measurement is the FEE value, this can be read from register with address 0010110b. Negative values are stored as a binary no between 0000000 and 1111111. To calculate the negative value, a two's complement of this value must be performed. Only FEE modes where DN-pulses are counted (10 and 11) will give a negative value.

When the FEE value has been read, the frequency offset can be calculated as follows:

Mode UP: $F_{offset} = R/(2P) \times (FEE - \Delta Fp)$

Mode DN: $F_{offset} = R/(2P) \times (FEE + \Delta Fp)$

Mode UP+DN: $F_{offset} = R/(4P) \times (FEE)$

where FEE is the value stored in the FEE register, (Fp is the single sided frequency deviation, P is the no. of symbols/data bit counted and R is the symbol/data rate. A positive Foffset means that the received signal has a higher frequency than the receiver frequency. To compensate for this, the receivers XCO frequency should be increased.

It is recommended to use Mode UP+DN for two reasons, you do not need to know the actual frequency deviation and this mode gives the best accuracy.

Bit Synchronizer

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000110	-	'0'	'0'	'0'	BitSync_clkS2	BitSync_clkS1	BitSync_clkS0	BitRate_clkS2

0000111	BitRate_clkS1	BitRate_clkS0	RefClk_K5	RefClk_K4	RefClk_K3	RefClk_K2	RefClk_K1	RefClk_K0

A bit synchronizer can be enabled in receive mode by selecting the synchronous mode (Sync_en=1). The DataClk pin will output a clock with twice the frequency of the bit rate (a bit rate of 20 kbit/sec gives a DataClk of 20 kHz). A received symbol/bit on DataIXO will be output on rising edge of DataClk. The micro controller should therefore sample the symbol/bit on falling edge of DataClk.

The bit synchronizer uses a clock that needs to be programmed according to the bit rate. The clock frequency should be 16 times the actual bit rate (a bit rate of 20 kbit/sec needs a bit synchronizer clock with frequency of 320 kHz). The clock frequency is set by the following formula:

$$f_{BITSYNC_CLK} = \frac{f_{XCO}}{Refclk_K \times 2^{(7-BITSYNC_clkS)}}$$

where

$f_{BITSYNC_CLK}$: The bit synchronizer clock frequency (16 times higher than the bit rate)

f_{XCO}: Crystal oscillator frequency

Refclk_K: 6 bit divider, values between 1 and 63

BitSync_clkS: Bit synchronizer setting, values between 0 and 7

Refclk_K is also used to derive the modulator clock and the bit rate clock.

At the beginning of a received data package, the bit synchronizer clock frequency is not synchronized to the bit rate. When these two are maximum offset to each other, it takes 22 bit/symbols before synchronization is achieved.

Transmitter

Power Amplifier

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000000	LNA_by	PA2	PA1	PA0	Sync_en	Mode1	Mode0	'1'
0000001	'1'	'0'	'0'	'0'	RSSI_en	LD_en	PF_FC1	PF_FC0

The maximum output power is approximately 10dBm for a 50Ω load. The output power is programmable in seven steps, with approximately 3dB between each step. Bits PA2 – PA0, control this. PA2 – PA0 = 1 give the maximum output power.

The power amplifier can be turned off by setting PA2 – PA0 = 0.

For all other combinations the PA is on and has maximum power when PA2 – PA0 = 1.

The PA will be bypassed if PA_by=1. Output power will drop ~14dB. It is still possible to control the power by PA2 – PA0.

Frequency Modulation

FSK modulation is applied by switching between two sets of dividers (M,N,A). The formula for calculating the M, N and A values is given in chapter Frequency synthesizer. The divider values stored in the M0-, N0-, and A0-registers will be used when transmitting a '0' and the M1-, N1-, and A1-registers will be used to transmit a '1'. The difference between the two carrier frequencies corresponds to the double sided frequency deviation. The data to be transmitted shall be applied to pin DataIXO (see chapter Transceiver sync-/non-synchronous mode on how to use the pin DataClk). The DataIXO pin is set as input in transmit mode and output in receive mode.

Using the XCO-tune Bits

The module has a built-in mechanism for tuning the frequency of the crystal oscillator and is often used in combination with the Frequency Error Estimator (FEE). The XCO tuning is designed to eliminate or reduce initial frequency tolerance of the crystal and/or the frequency stability over temperature.

A procedure for using the XCO tuning feature in combination with the FEE is given below. The MICRF600 measures the frequency offset between the receivers LO frequency and the frequency of the transmitter. The receiver XCO frequency can be tuned until the receiver and transmitter frequencies are equal.

A procedure like this can be called during production (storing the calibrated XCO_tune value), at regular intervals or implemented in the communication protocol when the frequency has changed. The MICRF600 development system can test this feature.

Example: In FEE, count up+down pulses, counting 8 bits:

A perfect case ==> FEE = 0

If FEE > 0: LO is too low, increase LO by decreasing XCO_tune value

v.v. for FEE < 0

FEE field holds a number in the range -128, … , 127. However, it keeps counting above/below the range, which is:

If FEE = -128 and still counting dwn-pulses:

1) =>-129 = +127
2) 126
3) 125

To avoid this situation, always make sure max count is between limits.

Application Circuit Illustration

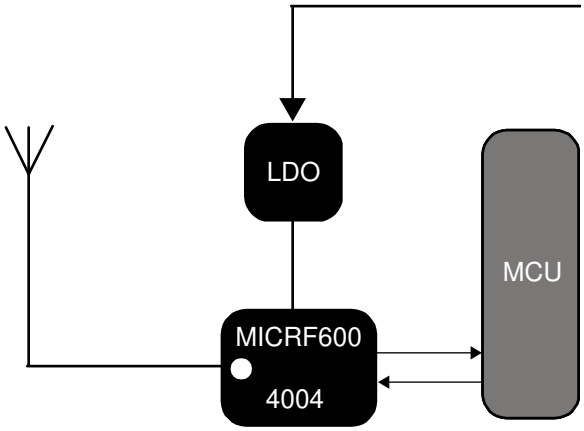


Figure 11. Circuit illustration of MICRF600, LDO and MCU

Figure 11. shows a typical set-up with the MICRF600, a Low-Drop-Out voltage regulator (LDO) and a mikro-controller (MCU). When the MICRF600 and the MCU runs on the same power supply (min 2.0, max. 2.5V), the IO can be connected directly to the MCU. If the MCU needs a higher VDD than the max. specified VDD of the MICRF600 (2.5V), voltage dividers need to be added on the IO lines not to override the max. input voltage.

Figure 12 shows a recommended voltage divider circuit for a MCU running at 3.0V and the MICRF600 at 2.5V.

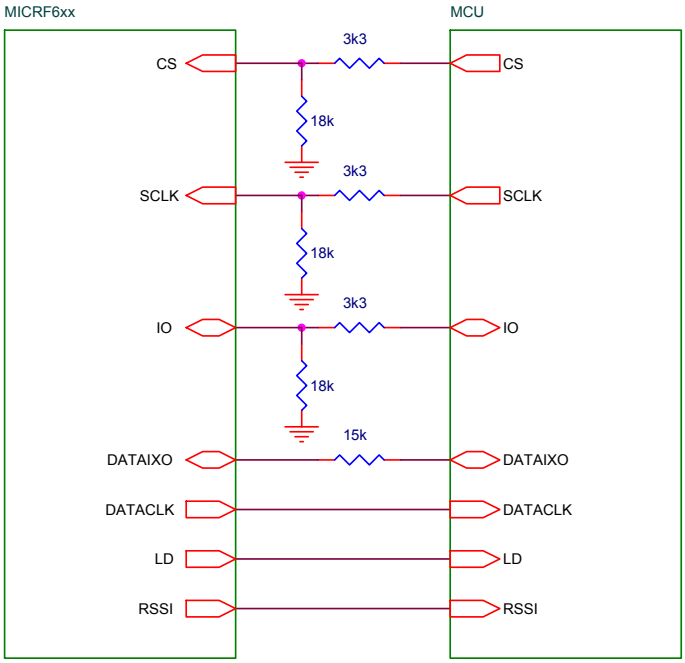


Figure 12. How to connect MCU600 (2.5V) and MCU (3.0V)

Assembling the MICRF600

Recommended Reflow Temperature Profile

When the MICRF600 module is being automatically assembled to a PCB, care must be taken not to expose the module for temperature above the maximum specified. Figure 13 shows the recommended reflow temperature profile.

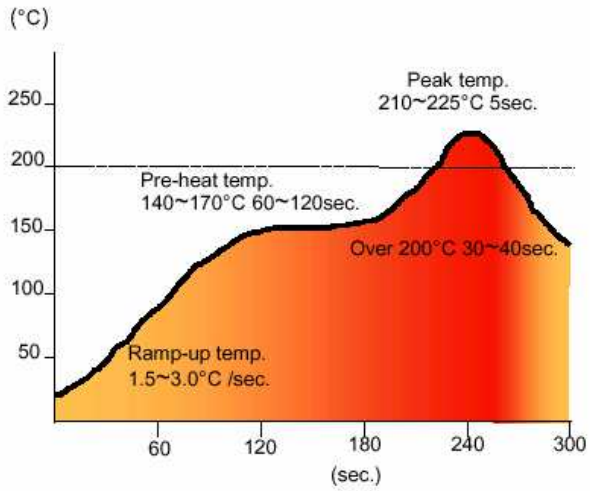


Figure 13. Recommended Reflow Temperature Reflow

Shock/Vibration during Reflow

The module has several components inside which are assembled in a reflow process. These components may reflow again when the module is assembled onto a PCB. It is therefore important that the module is not subjected to any mechanical shock or vibration during this process.

Handassembling the MICRF600

It is recommended to use solder paste also during hand assembling of the module. Because of the module ground pad on the bottom side, the module will be assembled most efficient if the heat is being subjected to the bottom side of the PCB. The heat will be transferred trough the PCB due the ground vias under the module (see Layout Considerations). In addition, it is recommended to use a solder tip on the signal and power pads, to make sure the solder points are properly melted.

Layout

Recommended Land Pattern

Figure 14 shows a recommended land pattern that facilitates both automatic and hand assembling.

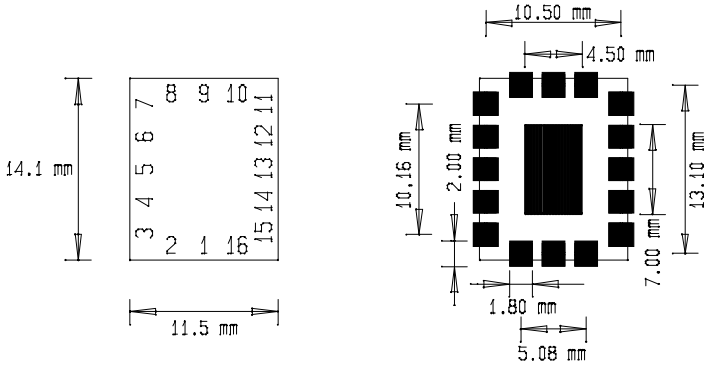


Figure 14. Recommended Land Pattern

Layout Considerations

Except for the antenna input/output signal, only digital and low frequency signals need to interface with the module. There is therefore no need of years of RF expertise to do a successful layout, as long as the following few points are being followed:

- Proper ground is needed. If the PCB is 2-layer, the bottom layer should be kept only for ground. Avoid signal traces that split the ground plane. For a 4-layer PCB, it is recommended to keep the second layer only for ground.
- A ground via should be placed close to all the ground pins. The bottom ground pad should be penetrated with 4-16 ground vias.
- The antenna has a impedance of ~50 ohm. The antenna trace should be kept to 50 ohm to avoid signal reflection and loss of performance. Any transmission line calculator can be used to find the needed trace width given a board build up. Ex: A trace width of 44 mil (1.12 mm) gives 50 impedance on a FR4 board (dielectric cons=4.4) with copper thickness of 35μm and height (layer 1-layer 2 spacing) of 0.61 mm.
- RF circuitry is sensitive to voltage supply and therefore caution should be taken when choosing power circuitry. To achieve the best performance, low noise LDO's with high PSSR should be chosen. What is present on the voltage supply will be directly modulated to the RF spectrum causing degradation and regulatory issues. To make sure you have the right selection, please contact local sales for the latest Micrel offerings in power management and guidance. To avoid "pickup" from other circuitry on the VDD lines, it is recommended to route the VDD in a star configuration with decoupling at each circuitry and at the common connection point (see above layout). If there are noisy circuitry in the design, it is strongly recommended to use a separate power supply and/or place low value resistors (10ohms), inductors in series with the power supply line into these circuitry.
- Digital high speed logic or noisy circuitry should/must be at a safe distance from RF circuitry or RF VDD as this might/will cause degradation of sensitivity and create spurious emissions. Example of such circuitry is LCD display, charge pumps, RS232, clock / data bus etc.

Package Dimensions

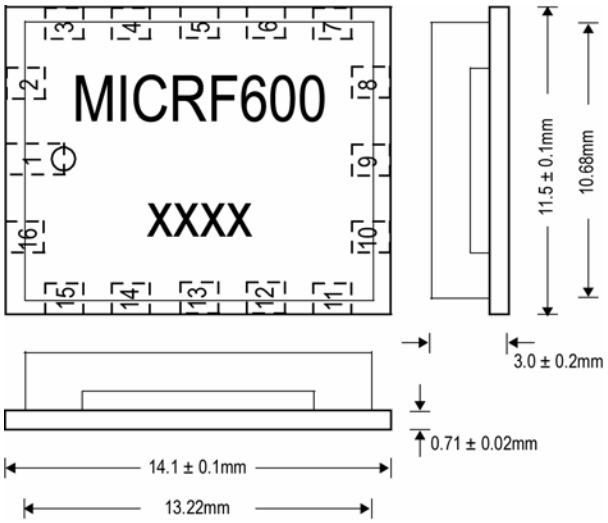


Figure 15. Package Dimensions

Tape Dimensions

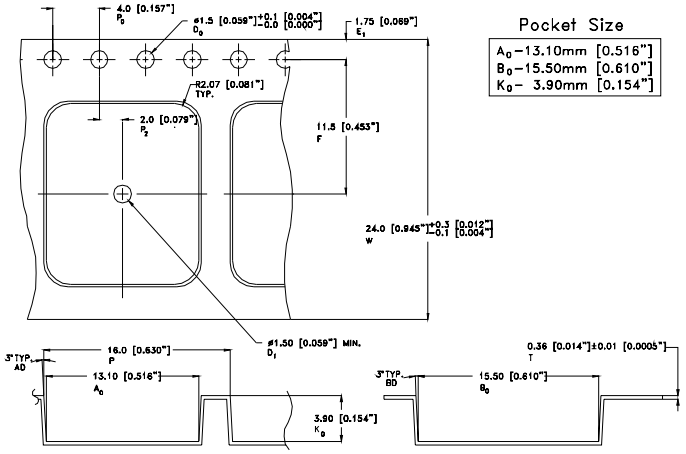


Figure 16. Tape Dimensions

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