MLX71121

300 to 930MHz
FSK/FM/ASK Receiver

Features

- Dual RF input for antenna space and frequency diversity, LNA cascading or differential feeding
- Fully integrated PLL-based synthesizer
- 2nd mixer with image rejection
- Reception of ASK or FSK modulated signals
- Wide operating voltage and temperature ranges
- Very low standby current consumption
- Low operating current consumption
- Internal IF filter
- Internal FSK demodulator
- Average or peak detection data slicer mode
- RSSI output with high dynamic range for RF level indication
- Output noise cancellation filter
- MCU clock output
- High over-all frequency accuracy
- 32-pin Quad Flat No-Lead Package (QFN)

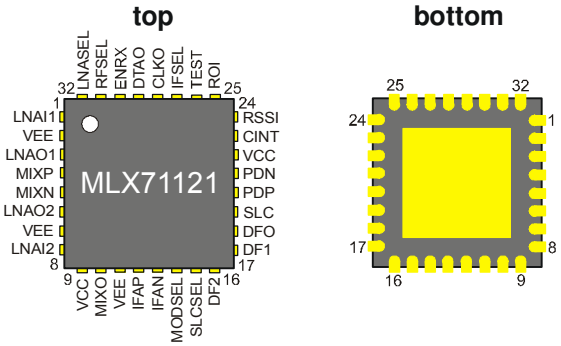
Ordering Information

Part Number	*Temperature Code*	*Package Code*	*Delivery Form*
MLX71121	K (-40 °C to 125 °C)	LQ (32 L QFN 5x5 Quad)	73 pc/tube 5000 pc/T&R

Application Examples

- General digital and analog RF receivers at 300 to 930MHz
- Tire pressure monitoring systems (TPMS)
- Remote keyless entry (RKE)
- Low power telemetry systems
- Alarm and security systems
- Active RFID tags
- Remote controls
- Garage door openers
- Home and building automation

Pin Description



General Description

The MLX71121 is a multi-band, single-channel/dual-channel RF receiver based on a double-conversion super-heterodyne architecture. It can receive FSK and ASK modulated signals. The IC is designed for general purpose applications for example in the European bands at 433MHz and 868MHz or for similar applications in North America or Asia, e.g. at 315MHz or 915MHz.
The receiver's extended temperature and supply voltage ranges make the device a perfect fit for automotive or similar applications where harsh environmental conditions are expected.

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1 Theory of Operation

1.1 General

The MLX71121 receiver architecture is based on a double-conversion super-heterodyne approach. The two LO signals are derived from an on-chip integer-N PLL frequency synthesizer. The PLL reference frequency is derived from a crystal (XTAL). As the first intermediate frequency (IF1) is very high, a reasonably high degree of image rejection is provided even without using an RF front-end filter. At applications asking for very high image rejections, cost-efficient RF front-end filtering can be realized by using a SAW filter in front of the LNA. The second mixer MIX2 is an image-reject mixer.

The receiver signal chain is setup by one (or two) low noise amplifier(s) (LNA1, LNA2), two down-conversion mixers (MIX1, MIX2), an on-chip IF filter (IFF) as well as an IF amplifier (IFA). By choosing the required modulation via an FSK/ASK switch (at pin MODSEL), either the on-chip FSK demodulator (FSK DEMOD) or the RSSI-based ASK detector is selected. A second order data filter (OA1) and a data slicer (OA2) follow the demodulator. The data slicer threshold can be generated from the mean-value of the data stream or by means of the positive and negative peak detectors (PKDET+/-). A digital post-processing of the sliced data signal can be performed by a noise cancellation filter (NCF) building block.

The dual LNA configuration can be used for antenna space diversity or antenna frequency diversity or to setup an LNA cascade (to further improve the input sensitivity). The two LNAs can also be setup to feed the RF signal differentially.

A sequencer circuit (SEQ) controls the timing during start-up. This is to reduce start-up time and to minimize power dissipation.

A clock output, which is a divide-by-8 version of the crystal oscillator signal, can be used to drive a microcontroller. The clock output is open drain and gets activated through a load connected to positive supply.

1.2 Technical Data Overview

- ❒ Input frequency ranges: 300 to 470MHz
  610 to 930MHz
- ❒ Power supply range: 2.1 to 5.5V
- ❒ Temperature range: -40 to +125°C
- ❒ Shutdown current: 50 nA
- ❒ Operating current: 10.0 to 11.1mA
- ❒ FSK input sensitivity: -107dBm* (433MHz)
- ❒ ASK input sensitivity: -112dBm* (433MHz)
- ❒ Internal IF: 1.8MHz with 300kHz 3dB bandwidth
- ❒ FM/FSK deviation range: ±10kHz to ±100kHz
- ❒ Image rejection:
  65dB 1st IF (with external RF front-end filter)
  25dB 2nd IF (internal image rejection)
- ❒ Maximum data rate: 50kps RZ (bi-phase) code,
  100kps NRZ
- ❒ Spurious emission: < -54dBm
- ❒ Linear RSSI range: > 60dB
- ❒ Crystal reference frequency: 16 to 27MHz
- ❒ MCU clock frequency: 2.0 to 3.4MHz

* at 4kbps NRZ, BER = $3 \cdot 10^{-3}$, without SAW front-end-filter loss

1.3 Block Diagram

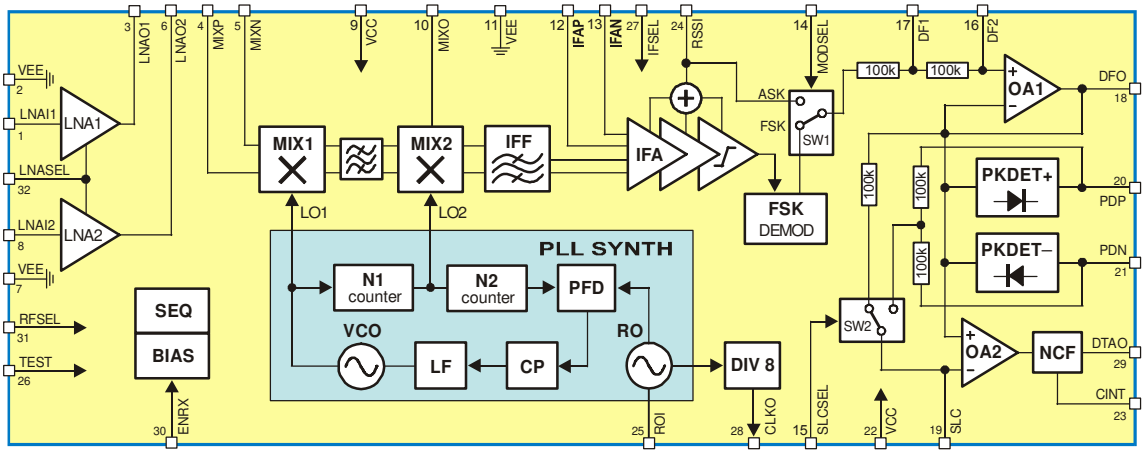


Fig. 1: MLX71121 block diagram

The MLX71121 receiver IC consists of the following building blocks:

- PLL synthesizer (PLL SYNTH) to generate the first and second local oscillator signals LO1 and LO2. The PLL SYNTH consists of a fully integrated voltage-controlled oscillator (VCO), a distributed feedback divider chain (N1,N2), a phase-frequency detector (PFD) a charge pump (CP), a loop filter (LF) and a crystal-based reference oscillator (RO).
- Two low-noise amplifiers (LNA1, LNA2) for high-sensitivity RF signal reception
- First mixer (MIX1) for down-conversion of the RF signal to the first IF (intermediate frequency)
- Second mixer (MIX2) with image rejection for down-conversion from the first to the second IF
- IF Filter (IFF) with a 1.8MHz center frequency and a 300kHz 3dB bandwidth
- IF amplifier (IFA) to provide a high voltage gain and an RSSI signal output
- FSK demodulator (FSK DEMOD)
- Operational amplifiers OA1 and OA2 for low-pass filtering and data slicing, respectively
- Positive (PKDET+) and negative (PKDET-) peak detectors
- Switches SW1 to select between FSK and ASK as well as SW2 to chose between averaging or peak detection mode.
- Noise cancellation filter (NCF)
- Sequencer circuit (SEQ) and biasing (BIAS) circuit
- Clock output (DIV8)

1.4 Operating Modes

The receiver offers two operating modes selectable by setting the corresponding logic level at pin ENRX.

ENRX	Description
0	Shutdown mode
1	Receive mode

Note: ENRX is pulled down internally.

The receiver's start-up procedure is controlled by a sequencer circuit. It performs the sequential activation of the different building blocks. It also initiates the pre-charging of the data filter and data slicer capacitors in order to reduce the overall start-up time and current consumption during the start-up phase.
At ENRX = 0, the receiver is in shutdown mode and draws only a few nA. The bias system and the reference oscillator are activated after enabling the receiver by a positive edge at pin ENRX. The crystal oscillator (RO) is turned on first. Then the crystal oscillation amplitude builds up from noise. After reaching a certain amplitude level at pin ROI, the whole IC is activated and draws the full receive mode current consumption I_{CC}. This event is used to start the pre-charging of the external data path capacitors. Pre-charging is finished after 5504 clock cycles. After that time the data output pin DTAO output is activated.

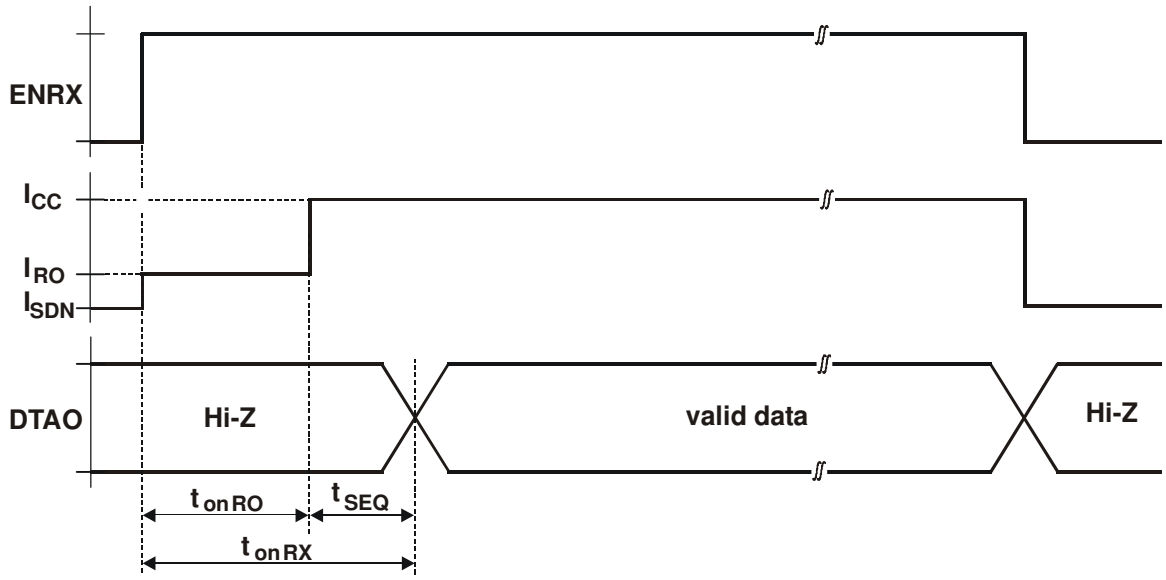


Fig. 2: Timing diagram of start-up and shutdown behavior

1.5 LNA Selection

The receiver features two identical LNAs. Each LNA is a cascode amplifier with a voltage gain of approximately 18dB. The actual gain depends on the antenna matching network at the inputs and the LC tank network between the LNA outputs and mixer input. LNA operation can be controlled by the LNASEL pin.

LNASEL	Description
0	LNA1 active, LNA2 shutdown
Hi-Z	LNA1 and LNA2 active
1	LNA1 shutdown, LNA2 active

Pin LNASEL is internally pulled to VCC/2 during receive mode. Therefore both LNAs are active if LNASEL is left floating (Hi-Z state).

1.6 Mixer Section

The mixer section consists of two mixers. Both are double-balanced mixers. The second mixer is built as an image rejection mixer. The first mixer's inputs (MIXP and MIXN) are functionally the same. For single-ended drive, the unused input has to be tied to ground via a capacitor. A soft band-pass filter is placed between the mixers.

RFSEL	Description
0	Input frequency range 300 to 470MHz
1	Input frequency range 610 to 930MHz

Pin RFSEL is used to select the required RF band. The LO frequencies and the proper sidebands for image suppression will be set accordingly.

1.7 IF Filter

The MLX71121 comprises an internal IF filter with a -3dB bandwidth (B3dB) of 300kHz and a -40dB attenuation bandwidth (B40dB) of 1.4MHz. This filter contains three capacitively coupled bi-quad stages that represent resonant tanks at a filter center frequency (f_{cent}) of 1.8MHz

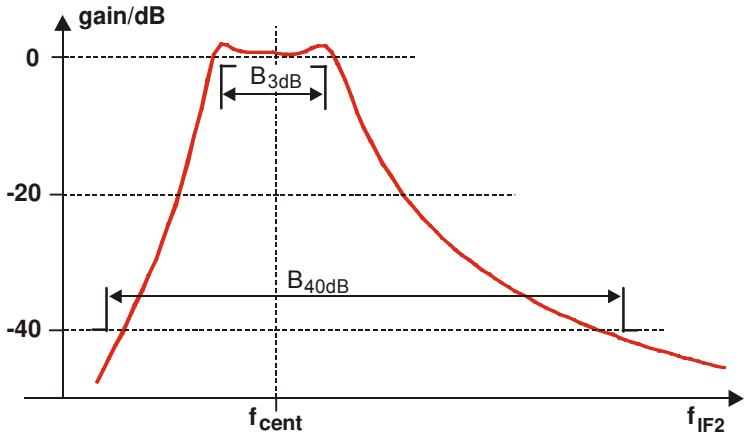


Fig. 3: IF filter tolerance scheme

1.8 IF Amplifier

After having passed the IF filter, the signal is amplified by a high-gain limiting amplifier. It consists of several AC-coupled gain stages with a bandwidth of 400kHz to 11MHz. The overall small-signal pass-band gain is about 80dB. A received-signal-strength indicator (RSSI) signal is generated within the IF amplifier and is available at pin RSSI.

1.9 PLL Synthesizer

The PLL synthesizer consists of a fully integrated voltage-controlled oscillator running at 400MHz to 640MHz, a distributed feedback divider chain, an edge-triggered phase-frequency detector, a charge pump, a loop filter and a crystal-based reference oscillator. The PLL is used for generating the LO signals. The LO1 is directly taken from the VCO output, and the LO2 is derived from the LO1 signal passing the N1 counter. Another counter N2 follows N1. The overall feedback divider ratio N_{tot} is fixed to 24. The values of N1 and N2 are depending on the selected RF band that can be chosen via pin RFSEL.

RFSEL	f_{LO1min} [MHz]	f_{LO1max} [MHz]	f_{LO2min} [MHz]	f_{LO2max} [MHz]	N_1	N_2	N_{tot}
0	400	640	100	160	4	6	24
1	400	640	200	320	2	12	24

1.10 Reference Oscillator

A Colpitts crystal oscillator with integrated functional capacitors is used as the reference oscillator (RO) of the PLL synthesizer. The equivalent input capacitance CRO offered to the crystal at pin ROI is about 18pF. The crystal oscillator features an amplitude control loop. This is to assure a very stable frequency over the specified supply voltage and temperature range together with a short start-up time. A buffer amplifier with hysteresis is between RO and PFD. Also a clock divider follows the buffer.

1.11 Clock Output

The clock output pin CKOUT is an open-drain output. For power saving reasons, the circuit is only active if an external pull-up resistor RCL is applied to the pin. Furthermore, RCL can be used to adjust the clock waveform. It forms an RC low-pass together with the capacitive load at the pin, the parasitics of the PCB and the input capacitance of the external circuitry (e.g. a microcontroller).
The clock output feature is disabled if pin CKOUT is connected to ground or left open.

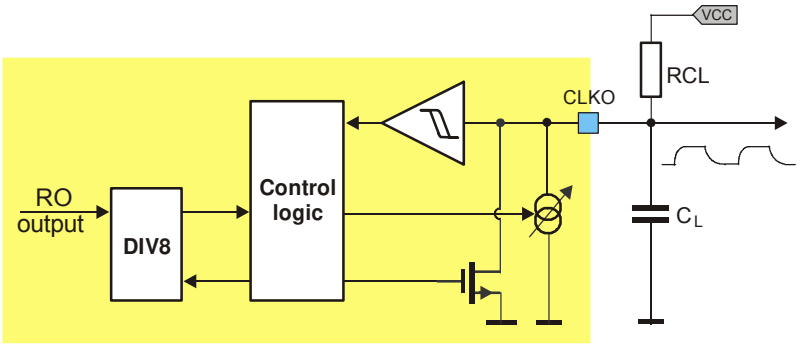


Fig. 4: Clock output implementation

1.12 FSK Demodulator

The integrated FSK demodulator is based on a phase-coincidence demodulator principle. An injection-locked oscillator (ILO) is used as a frequency-dependent phase shifter. This topology features a good linearity of the frequency-phase relationship over the entire locking range. The type of demodulator has no built-in constraints regarding the modulation index. It also offers a wide carrier acceptance range.
In addition, the demodulator provides an AFC loop for correcting the remaining free-running frequency error and drift effects, and also to remove possible frequency offsets between transmitter and receiver frequencies. The AFC loop features a dead band which means that the AFC loop is only closed if the demodulator output voltage leaves the linear region of the demodulator. Most of the time, the control loop is open. This leads to several advantages. The AFC loop bandwidth can be high and therefore the reaction time is short. Furthermore the demodulator itself has no low-end cut-off frequency.
The FSK demodulator has a negative control slope, this means the output voltage decreases by increasing the IF2 frequency. This guarantees an overall positive slope because the mixer section converts the receive frequency to IF2 either with high-low or low-high side injection.
The FSK demodulator is turned off during ASK demodulation.

1.13 Baseband Data Path

The baseband data path can be divided into a data filter section and a data slicer section.

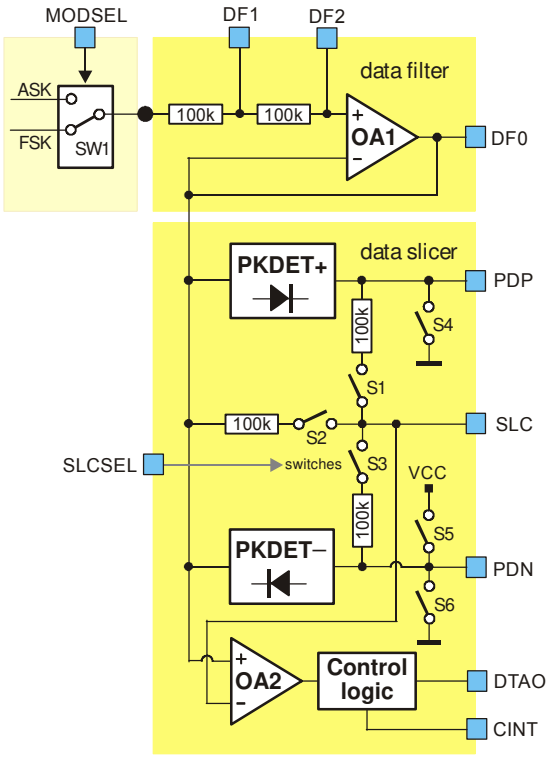


Fig. 5: Block diagram of the data path

The data filter input is either connected to the ASK or to the FSK demodulation output. Pin MODSEL can be used to set the internal switch SW1 accordingly.

MODSEL	Description
0	ASK demodulation
1	FSK demodulation

For ASK demodulation, the RSSI signal of the IFA is used. During FSK demodulation, SW1 is connected to the FSK demodulator output.
The SLCSEL pin is used to control the internal switches depending on operating and slicer mode.

Pins DF1, DF2, DFO, SLC and DTAO are left floating during shutdown mode. So they are in a high-Z state.

1.14 Data Filter

The data filter is formed by the operational amplifier OA1, two internal 100kΩ resistors and two external capacitors. It is implemented as a 2nd order Sallen-Key filter. The low pass filter characteristic rejects noise at higher frequencies and therefore leads to an increased sensitivity.

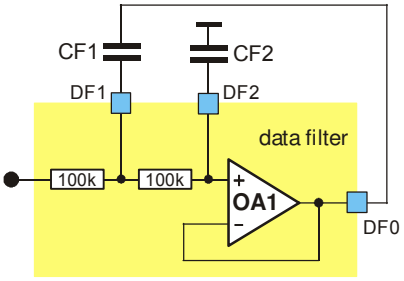


Fig. 6: Data filter

The filter's pole locations can be set by the external capacitors CF1 and CF2. The cut-off frequency f_c has to be adjusted according to the transmission data rate R. It should be set to approximately 1.5 times the fastest expected data rate. For a Butterworth filter characteristic, the data filter capacitors can be calculated as follows.

$$CF1 = \frac{1}{\sqrt{2} \cdot \pi \cdot 100k \cdot f_c} \qquad CF2 = \frac{CF1}{2}$$

R_{RZ} [kbit/s]	R_{NRZ} [kbit/s]	fc [kHz]	CF1 [pF]	CF2 [pF]
0.6	1.2	0.9	2200	1000
1.2	2.4	1.8	1200	680
1.6	3.2	2.4	1000	470
2.4	4.8	3.6	680	330
3.3	6.6	5	470	220
4.8	9.6	7.2	330	150
6.0	12	9	220	100

1.15 Data Slicer

The purpose of the data slicer is to convert the filtered data signal into a digital output. It can therefore be considered as an analog-to-digital converter. This is done by using the operational amplifier OA2 as a comparator that compares the data filter output with a threshold voltage. The threshold voltage can be derived in two different ways from the data signal.

SLCSEL	Description
0	Averaging detection mode
1	Peak detection mode

1.15.1 Averaging Detection Mode

The simplest configuration is the averaging or RC integration method. Here an on-chip 100kΩ resistor together with an external slicer capacitor (CSL) are forming an RC low-pass filter. This way the threshold voltage automatically adjusts to the mean or average value of the analog input voltage.
To create a stable threshold voltage, the cut-off frequency of the low pass has to be lower than the lowest signal frequency.

$$CSL \geq \frac{\tau_{AVG}}{100k} \qquad \tau_{AVG} = \frac{1.5}{R_{RZ}}$$

A long string of zeros or ones, like in NRZ codes, can cause a drift of the threshold. That's why a Manchester or other DC-free coding scheme works best.
The peak detectors are disabled during averaging detection mode, and the output pins PDP and PDN are pulled to ground (S4, S6 are closed).

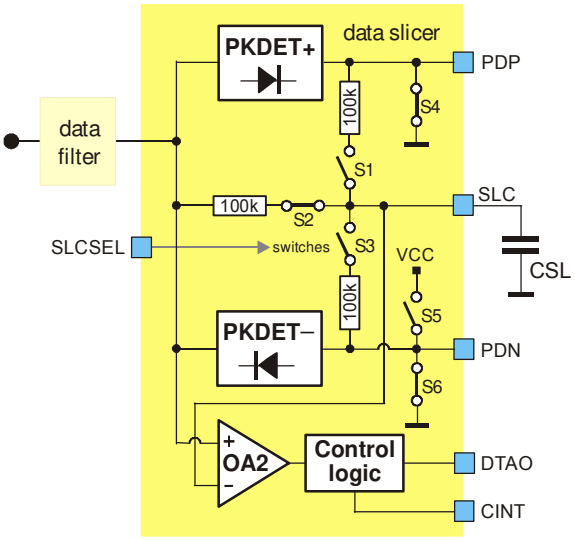


Fig. 7: Data path in averaging detection mode

1.15.2 Peak Detection Mode

Peak detection mode has a general advantage over averaging detection mode because of the part attack and slow release times. Peak detection should be used for all non DC-free codes like NRZ. In this configuration the threshold is generated by using the positive and negative peak detectors. The slicer comparator threshold is set to the midpoint between the high output and the low output of the data filter by an on-chip resistance divider. Two external capacitors (CP1, CP2) determine the release times for the positive and negative envelope. The two on-chip resistors provide a path for the capacitors to discharge. This allows the peak detectors to dynamically follow peak changes of the data filter output voltage. The attack times are very short due to the high peak detector load currents of about 500uA.
The decay time constant mainly depends on the longest time period without bit polarity change. This corresponds to the maximum number of consecutive bits with the same polarity (N_{MAX}).

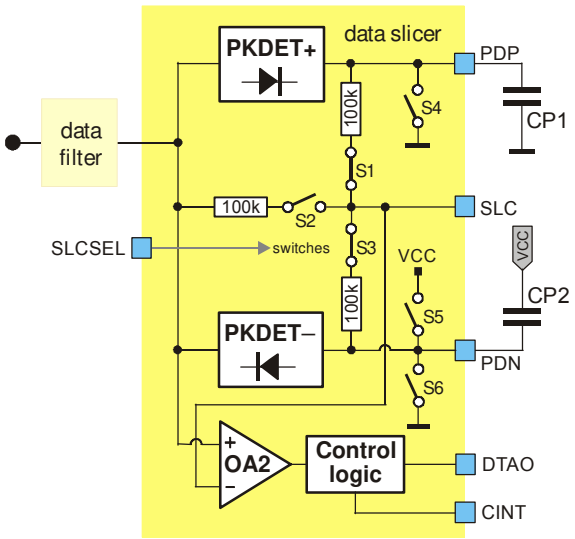


Fig. 8: Data path in peak detection mode

$$CP1/2 \geq \frac{\tau_{DECAY}}{100k} \qquad \tau_{DECAY} = \frac{N_{MAX}}{R_{NRZ}}$$

If the receiver is in shutdown mode and peak detection mode is selected then the peak detectors are disabled and the output of the positive peak detector (PDP) is connected to VEE (S4 is closed) and the output of the negative peak detector (PDN) is connected to VCC (S5 is closed). This guarantees the correct biasing of CP1 and CP2 during start-up.

1.16 Data Output and Noise Cancellation Filter

The data output pin DTAO delivers the demodulated data signal that can be further processed by a noise cancellation filter (NCF). The NCF can be disabled if pin CINT is connected to VEE. In this case the multiplexer (MUX) connects the receiver output DTAO directly to the data slicer output.

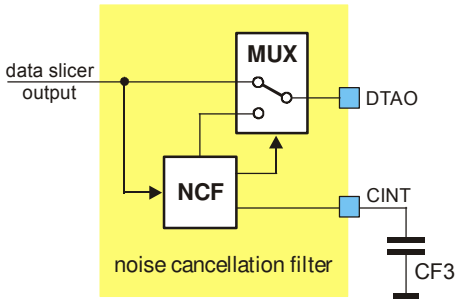


Fig. 9: Data output and noise filter

The noise cancellation filter can suppress random pulses in the data output which are shorter than t_{min}.

$$CF3 = 15 \cdot 10^{-6} \cdot t_{\min} = \frac{15 \cdot 10^{-6}}{R_{NRZ}} = \frac{7.5 \cdot 10^{-6}}{R_{RZ}}$$

The NCF can also operate as a muting circuit for RF input signals that are below sensitivity level if the bandwidth of the preceding data filter is selected much higher than the bandwidth of the NCF. This would be the case if no RF signal is present.

In contrast to conventional muting (or squelch) circuits, this topology does not need the RSSI signal for level indication. The filtering process is done by means of an analogue integrator. The cut-off frequency of the NCF is set by the external capacitor connected to pin CINT. This capacitor C_{F3} should be set according to the maximum data rate. Below table provides some recommendations..

During receiver start-up a sequencer checks if pin CINT is connected to a capacitor or to ground. The maximum value of C_{F3} should not exceed 12nF. This defines the lowest data rate that can be processed if the noise cancellation filter is activated.

R_{RZ} [kbit/s]	R_{NRZ} [kbit/s]	C_{F3}[nF]
0.6	1.2	12
1.2	2.4	6.8
1.6	3.2	4.7
2.4	4.8	3.3
3.3	6.6	2.2
4.8	9.6	1.5
6.0	12	1.2

In shutdown mode pin DTAO is set to Hi-Z state.

2 Functional Description

2.1 Frequency Planning

Because of the double conversion architecture that employs two mixers and two IF signals, there are four different combinations for injecting the LO1 and LO2 signals:

- LO1 high side and LO2 high side: receiving at f_{RF}(high-high)
- LO1 high side and LO2 low side: receiving at f_{RF}(high-low)
- LO1 low side and LO2 high side: receiving at f_{RF}(low-high)
- LO1 low side and LO2 low side: receiving at f_{RF}(low-low)

As a result, four different radio frequencies (RFs) could yield one and the same second IF (IF2). Fig. 10 shows this for the case of receiving at f_{RF}(high-high). In the example of Fig. 10, the image signals at f_{RF}(low-high) and f_{RF}(low-low) are suppressed by the bandpass characteristic provided by the RF front-end. The bandpass shape can be achieved either with a SAW filter (featuring just a couple of MHz bandwidth), or by the tank circuits at the LNA input and output (this typically yields 30 to 60MHz bandwidth). In any case, the high value of the first IF (IF1) helps to suppress the image signals at f_{RF}(low-high) and f_{RF}(low-low).

The two remaining signals at IF1 resulting from f_{RF}(high-high) and f_{RF}(high-low) are entering the second mixer MIX2. This mixer features image rejection with so-called single-sideband (SSB) selection. This means either the upper or lower sideband of IF1 can be selected. In the example of Fig. 10, LO2 high-side injection has been chosen to select the IF2 signal resulting from f_{RF}(high-high).

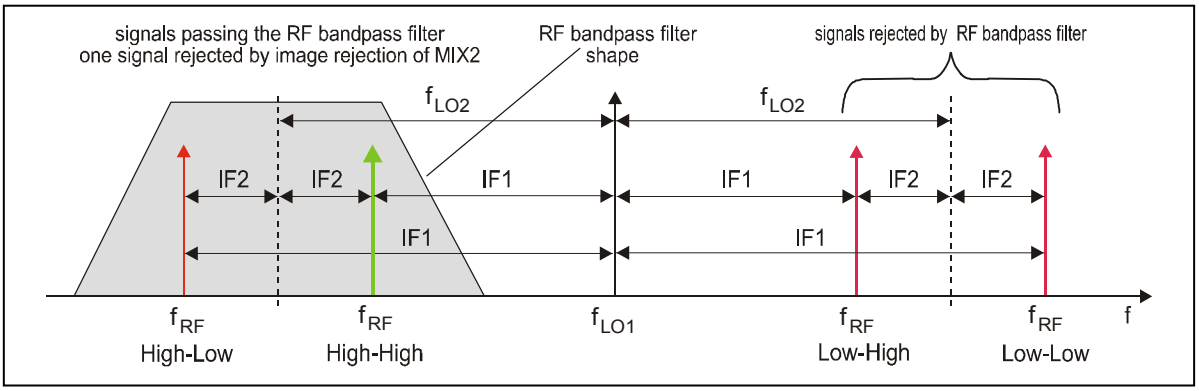


Fig. 10: The four receiving frequencies in a double conversion superhet receiver

It can be seen from the block diagram of Fig. 1 that there is a fixed relationship between the LO signal frequencies (f_{LO1} , f_{LO2}) and the reference oscillator frequency f_{RO}.

$$f_{LO1} = N_1 \cdot f_{LO2} \qquad f_{LO2} = N_2 \cdot f_{RO}$$

The operating frequency of the internal IF filter (IFF) and FSK demodulator (FSK DEMOD) are 1.8MHz. Therefore the second IF (IF2) is set to 1.8MHz as well.

2.2 Calculation of Frequency Settings

The receiver has two predefined receive frequency plans which can be selected by the RFSEL control pin. Depending on the logic level of RFSEL pin the sideband selection of the second mixer and the counter settings for N_1 and N_2 are changed accordingly.

RFSEL	Injection	f_{RFmin} [MHz]	f_{RFmax} [MHz]	N_1	N_2
0	high-low	300	470	4	6
1	low-high	610	930	2	12

The following table shows the relationships of several internal receiver frequencies for the two input frequency ranges.

f_{RF} [MHz]	f_{IF1}	f_{LO1}	f_{LO2}	f_{RO}
300 to 470	$\frac{f_{RF}+N_1 f_{IF2}}{N_1-1}$	$\frac{N_1(f_{RF}+f_{IF2})}{N_1-1}$	$\frac{f_{RF}+f_{IF2}}{N_1-1}$	$\frac{f_{RF}+f_{IF2}}{N_2(N_1-1)}$
610 to 930	$\frac{f_{RF}-N_1 f_{IF2}}{N_1+1}$	$\frac{N_1(f_{RF}+f_{IF2})}{N_1+1}$	$\frac{f_{RF}+f_{IF2}}{N_1+1}$	$\frac{f_{RF}+f_{IF2}}{N_2(N_1+1)}$

Given IF2 = 1.8MHz and the corresponding N_1, N_2 counter settings, above equations can be transferred into the following table.

f_{RF} [MHz]	f_{IF1}	f_{LO1}	f_{LO2}	f_{RO}
300 to 470	$\frac{f_{RF}+7.2\text{MHz}}{3}$	$\frac{4(f_{RF}+1.8\text{MHz})}{3}$	$\frac{f_{RF}+1.8\text{MHz}}{3}$	$\frac{f_{RF}+1.8\text{MHz}}{18}$
610 to 930	$\frac{f_{RF}-3.6\text{MHz}}{3}$	$\frac{2(f_{RF}+1.8\text{MHz})}{3}$		$\frac{f_{RF}+1.8\text{MHz}}{36}$

2.3 Standard Frequency Plans

IF2 = 1.8MHz.

RFSEL	f_{RF} [MHz]	f_{IF1} [MHz]	f_{LO1} [MHz]	f_{LO2} [MHz]	f_{RO} [MHz]
0	315	107.40	422.40	105.60	17.600000
	433.92	147.04	580.96	145.24	24.206667
1	868.3	288.23	580.07	290.03	24.169444
	915	303.80	611.20	305.60	25.466667

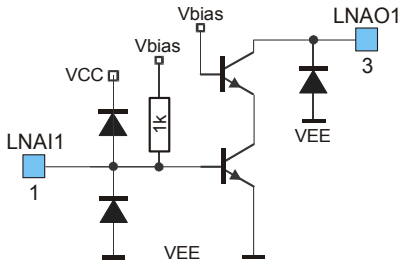
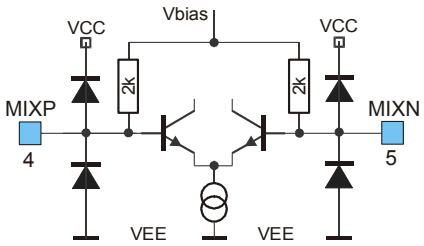
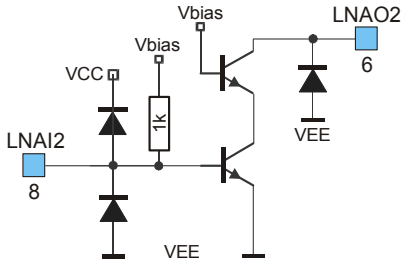
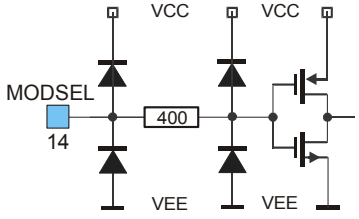
2.4 433/868MHz Frequency Diversity

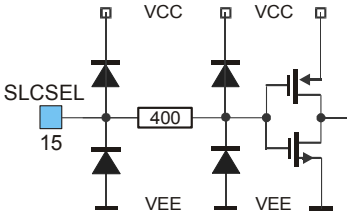
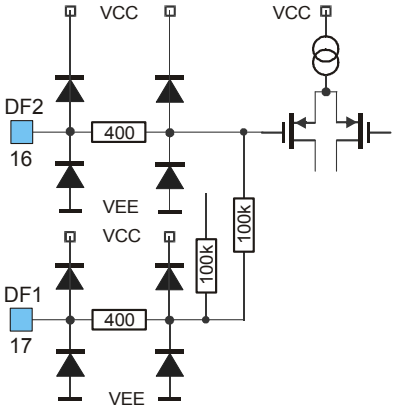
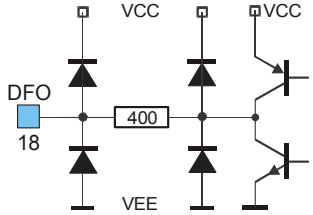
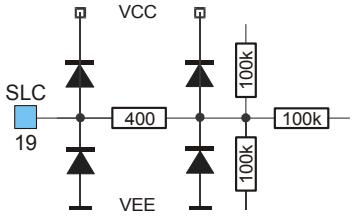
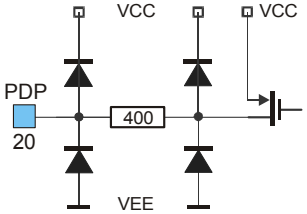
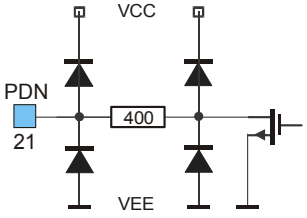
The receiver's multi-band functionality can be used to operate at two different frequency bands just by changing the logic level at pin RFSEL and without changing the crystal. This feature is applicable for common use of the 433 and 868MHz bands. Below table shows the corresponding frequency plans.

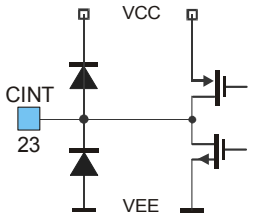
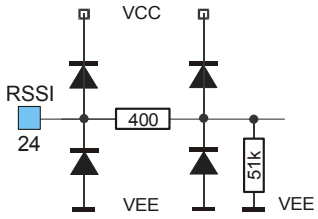
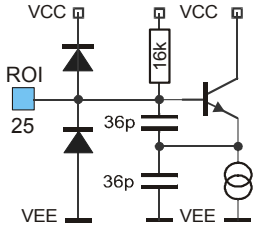
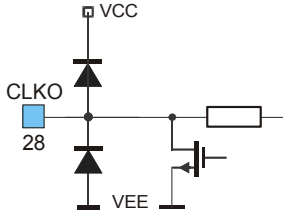
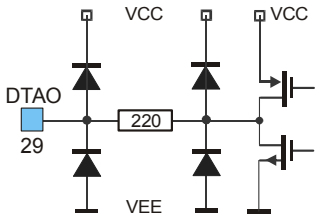
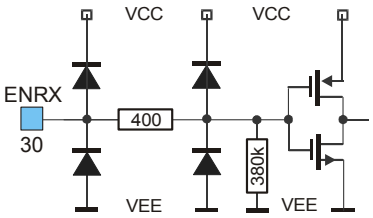
IF2 = 1.8MHz.

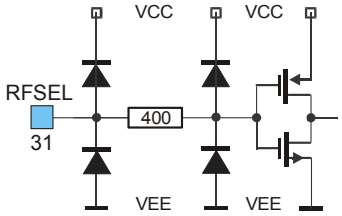
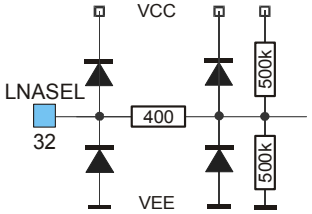
RFSEL	f_{RF} [MHz]	f_{IF1} [MHz]	f_{LO1} [MHz]	f_{LO2} [MHz]	f_{RO} [MHz]
0	433.25	146.82	580.07	145.02	24.169444
1	868.3	288.23	580.07	290.03	

3 Pin Definitions and Descriptions

Pin No.	Name	I/O Type	Functional Schematic	Description
3	LNAO1	analog output		LNA output 1
1	LNAI1	analog input		LNA input 1
2	VEE	ground		negative supply voltage
4	MIXP	analog input		MIX1 positive input
5	MIXN	analog input		MIX1 negative input
6	LNAO2	analog output		LNA output 2
8	LNAI2	analog input		LNA input 2
7	VEE	ground		negative supply voltage
9	VCC	supply		positive supply voltage
10	MIXO	analog output	not used pin left open	mixer 2 output
11	VEE	ground		negative supply voltage
12	IFAP	analog input	not used pins left open	IF amplifier positive input
13	IFAN	analog input		IF amplifier negative input
14	MODSEL	CMOS input		modulation select input

Pin No.	Name	I/O Type	Functional Schematic	Description
15	SLCSEL	CMOS input		slicer mode select input
16	DF2	analog I/O		data filter connection 2
17	DF1	analog I/O		data filter connection 1
18	DFO	analog output		data filter output
19	SLC	analog input		slicer reference input
20	PDP	analog output		peak detector positive output
21	PDN	analog output		peak detector negative output

Pin No.	Name	I/O Type	Functional Schematic	Description
22	VCC	supply		positive supply voltage
23	CINT	analog input		capacitor for noise cancellation filter pin must be connected to ground if noise cancellation filter is not used
24	RSSI	analog output		receive signal strength indication
25	ROI	analog input		reference oscillator input
26	TEST	CMOS input	not used connect to ground	test pin
27	IFSEL	CMOS input	not used connect pin to ground	IF select input
28	CLKO	CMOS output		clock output connect pull-up resistor to activate clock
29	DTAO	CMOS output		data output
30	ENRX	CMOS input		enable RX mode control

Pin No.	Name	I/O Type	Functional Schematic	Description
31	RFSEL	CMOS input		receive frequency select input
32	LNASEL	CMOS input		LNA select input

4 Technical Data

4.1 Absolute Maximum Ratings

Operation beyond absolute maximum ratings may cause permanent damage of the device.

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage	V_{CC}		0	7	V
Input voltage	V_{IN}		-0.3	V_{CC} +0.3	V
Storage temperature	T_{STG}		-55	150	°C
Junction temperature	T_J			150	°C
Thermal Resistance	R_{thJA}			22	K/W
Power dissipation	P_{diss}			0.12	W
Electrostatic discharge	V_{ESD}	HBM according to MIL STD 833D, method 3015.7	±1		kV

4.2 Normal Operating Conditions

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage	V_{CC}		2.1	5.5	V
Operating temperature	T_A		-40	125	°C
Input low voltage (CMOS)	V_{IL}	ENRX, SEL pins		0.3*V_{CC}	V
Input high voltage (CMOS)	V_{IH}	ENRX, SEL pins	0.7*V_{CC}		V
Input frequency range	f_{RF}	RFSEL=0	300	470	MHz
		RFSEL=1	610	930	
First IF range	f_{IF1}	RFSEL=0	100	170	MHz
		RFSEL=1	200	310	
LO1 range (VCO frequency)	f_{LO1}	f_{LO1} = 24*f_{REF}	400	640	MHz
LO2 range	f_{LO2}	RFSEL=0, f_{LO2} = f_{LO1} / 4	100	160	MHz
		RFSEL=1, f_{LO2} = f_{LO1} / 2	200	320	
XOSC frequency	f_{REF}	set by the crystal	16	27	MHz
CLKO frequency	f_{CLK}	f_{CLK} = f_{REF} / 8	2.0	3.375	MHz
FSK deviation	Δf		±10	±100	kHz
Data rate ASK	R_{ASK}	bi-phase code		50	kbps
		NRZ		100	
Data rate FSK	R_{FSK}	bi-phase code		50	
		NRZ		100	

4.3 DC Characteristics

all parameters under normal operating conditions, unless otherwise stated;
typical values at T_A= 23 °C and V_{CC} = 3 V, all parameters based on test circuits as shown Fig. 11

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operating Currents						
Shutdown current	I_{SDN}	ENRX=0, T_A = 85°C		50	200	nA
		ENRX=0, T_A = 125°C			4	µA
Supply current reference oscillator	I_{RO}	ENRX=1, t < t_{onRO}		1.5		mA
Supply current, FSK	I_{FSK}	ENRX=1, MODSEL=1 SLCSEL=0 LNASEL=0 or 1		10.2		mA
Supply current, ASK	I_{ASK}	ENRX= 1, MODSEL= 0 SLCSEL=0 LNASEL=0 or 1		9.8		mA
Digital Pin Characteristics (except of LNASEL)						
Input low voltage (CMOS)	V_{IL}	ENRX, SEL pins			0.3*V_{CC}	V
Input high voltage (CMOS)	V_{IH}	ENRX, SEL pins	0.7*V_{CC}			V
Pull down current ENRX pin	I_{PDEN}	ENRX=1	2	8	30	µA
Low level input current ENRX pin	I_{INLEN}	ENRX=0			1	µA
High level input current	I_{INHSEL}	SEL pins			1	µA
Low level input current	I_{INLSEL}	SEL pins			1	µA
LNASEL Pin Characteristics						
Input voltage LNA1 active	$V_{LNASEL1}$	ENRX=1			0.1*V_{CC}	V
Input voltage LNA2 active	$V_{LNASEL2}$	ENRX=1	0.9*V_{CC}			V
DTAO Pin Characteristics						
Output low voltage	V_{OL}	DTAO pin, I_{SINK} = 600µA			0.3*V_{CC}	V
Output high voltage	V_{OH}	DTAO pin, I_{SOURCE} = 600µA	0.7*V_{CC}			V

4.4 AC System Characteristics

all parameters under normal operating conditions, unless otherwise stated;
typical values at T_A= 23 °C and V_{CC} = 3 V, all parameters based on test circuits as shown Fig. 11

Parameter		Symbol	Condition		Min	Typ	Max	Unit
Receive Characteristics								
Input Sensitivity 1)			MODSEL	RFSEL				
FSK	315MHz	P_{min1}	1	0		-107		dBm
	433MHz	P_{min2}				-107		
	868MHz	P_{min3}		1		-104		
	915MHz	P_{min4}				-102		
ASK	315MHz	P_{min5}	0	0		-112		dBm
	433MHz	P_{min6}				-112		
	868MHz	P_{min7}		1		-108		
	915MHz	P_{min8}				-105		
Maximum input signal – FSK		$P_{max, FSK}$	MODSEL=1			-10		dBm
Maximum input signal – ASK		$P_{max, ASK}$	MODSEL=0, M>70dB			-10		dBm
Spurious emission		P_{spur}					-54	dBm
Image rejection 1st IF		IR_1	w/o SAW filter			20		dB
Image rejection 2nd IF		IR_2				25		dB
LNA Parameters								
Voltage gain		G_{LNA}	depends on external LC tank			18		dB
IF Filter Parameters								
Center frequency		f_{cent}				1.8		MHz
3dB bandwidth		B_{3dB}				300		kHz
40dB bandwidth		B_{40dB}				1.4		MHz
IF Amplifier / RSSI								
Operating frequency		f_{IFA}			0.4		11	MHz
RSSI dynamic range		DR_{RSSI}				60		dB
RSSI slope		S_{RSSI}				20		mV/dB
FSK Demodulator								
Input frequency range		f_{DEM}				1.8		MHz
Carrier acceptance range		Δf_{DEM}				±80		kHz
Demodulator sensitivity		S_{DEM}				5		mV/ kHz

1) at 4kbps NRZ, BER ≤ $3 \cdot 10^{-3}$, peak detector data slicer, LNASEL = 0 or 1

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Baseband Data Path						
Data filter bandwidth	B_{DF}	depending on CF1, CF2			100	kHz
Peak detector load current	I_{PKD}			500		µA
Start-up Parameters						
Reference oscillator start-up time	t_{onRO}	depending on crystal parameters		350	650	µs
Sequencer time	t_{SEQ}	5504 / f_{REF}	200	250	350	µs
Receiver start-up time	t_{onRX}	t_{onRO} + t_{SEQ}		0.6	1	ms
Frequency Stability						
Frequency pulling by supply voltage	df_{VCC}				±3	ppm/V

4.5 External Components

Parameter	Symbol	Condition	Min	Max	Unit
Crystal Parameters					
Crystal frequency	f_0	fundamental mode, AT	16	27	MHz
Load capacitance	C_L		10	15	pF
Static capacitance	C_0			5	pF
Series resistance	R_1			60	Ω
Noise Cancellation Filter					
Integrator capacitor	CF3	depends on data rate		12	nF
Clock Output					
Pull-up resistor	RCL		600		Ω
Load capacitance	C_L			50	pF

5 Test Circuit

5.1 Antenna Diversity Application Circuit

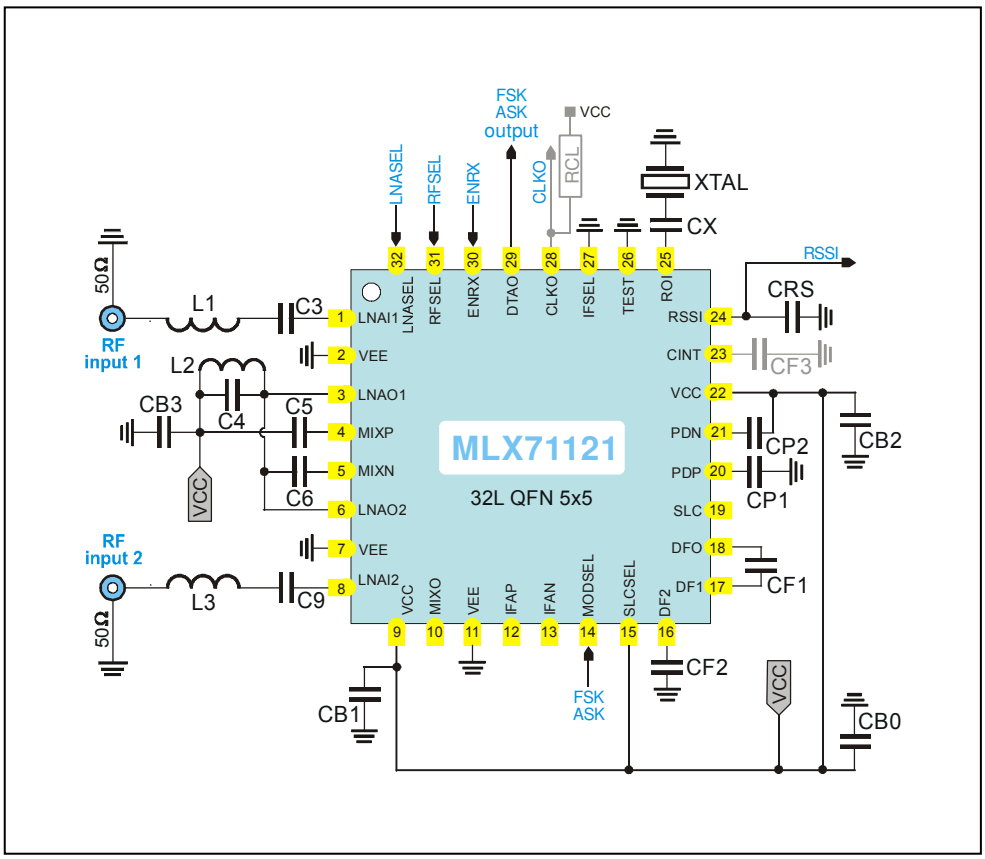


Fig. 11: Antenna diversity circuit schematic, peak detectors activated

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5.1.1 Test Circuit Component List of Figures 11

Part	Size	Value @ 315 MHz	Value @ 433.92 MHz	Value @ 868.3 MHz	Value @ 915 MHz	Tol.	Description
C3	0603	100 pF	100 pF	100 pF	100 pF	±5%	LNA input filtering capacitor
C4	0603	4.7 pF	3.9 pF	2.2 pF	1.5 pF	±5%	LNA output tank capacitor
C5	0603	100 pF	100 pF	100 pF	100 pF	±5%	MIX1 positive input matching capacitor
C6	0603	100 pF	100 pF	100 pF	100 pF	±5%	MIX1 negative input matching capacitor
C9	0603	100 pF	100 pF	100 pF	100 pF	±5%	LNA input filtering capacitor
CB0	0805	33 nF	33 nF	33 nF	33 nF	±10%	decoupling capacitor
CB1	0603	330 pF	330 pF	330 pF	330 pF	±10%	decoupling capacitor
CB2	0603	330 pF	330 pF	330 pF	330 pF	±10%	decoupling capacitor
CB3	0603	330 pF	330 pF	330 pF	330 pF	±10%	decoupling capacitor
CF1	0603	680 pF	680 pF	680 pF	680 pF	±10%	data low-pass filter capacitor, for data rate of 4 kbps NRZ
CF2	0603	330 pF	330 pF	330 pF	330 pF	±10%	data low-pass filter capacitor, for data rate of 4 kbps NRZ
CF3	0603	value according to the data rate connected to ground if noise filter not used				±10%	optional capacitor for noise cancellation filter
CP1	0603	33 nF	33 nF	33 nF	33 nF	±10%	positive PKDET capacitor, for data rate of 4 kbps NRZ
CP2	0603	33 nF	33 nF	33 nF	33 nF	±10%	negative PKDET capacitor, for data rate of 4 kbps NRZ
CRS	0603	1 nF	1 nF	1 nF	1 nF	±10%	RSSI output low pass capacitor
CSL	0603	100 nF for averaging detection mode only	100 nF	100 nF	100 nF	±10%	data slicer capacitor, for data rate of 4 kbps NRZ
CX	0603	27 pF	27 pF	27 pF	27 pF	±5%	crystal series capacitor
L1	0603	56 nH	27 nH	0 Ω	0 Ω	±5%	matching inductor
L2	0603	27 nH	15 nH	3.9 nH	3.9 nH	±5%	LNA output tank inductor
L3	0603	56 nH	27 nH	0 Ω	0 Ω	±5%	matching inductor
RCL	0603	3.3 kΩ	3.3 kΩ	3.3 kΩ	3.3 kΩ	±5%	optional CLK output resistor, to clock output signal generated
XTAL	SMD 5x3.2	17.60000 MHz ±20ppm cal., ±30ppm temp.	24.206667 MHz	24.169444 MHz	25.46667 MHz		fundamental-mode crystal from Telcona, or equivalent part

Note: NIP – not in place, may be used optionally

6 Package Description

The device MLX71121 is RoHS compliant.

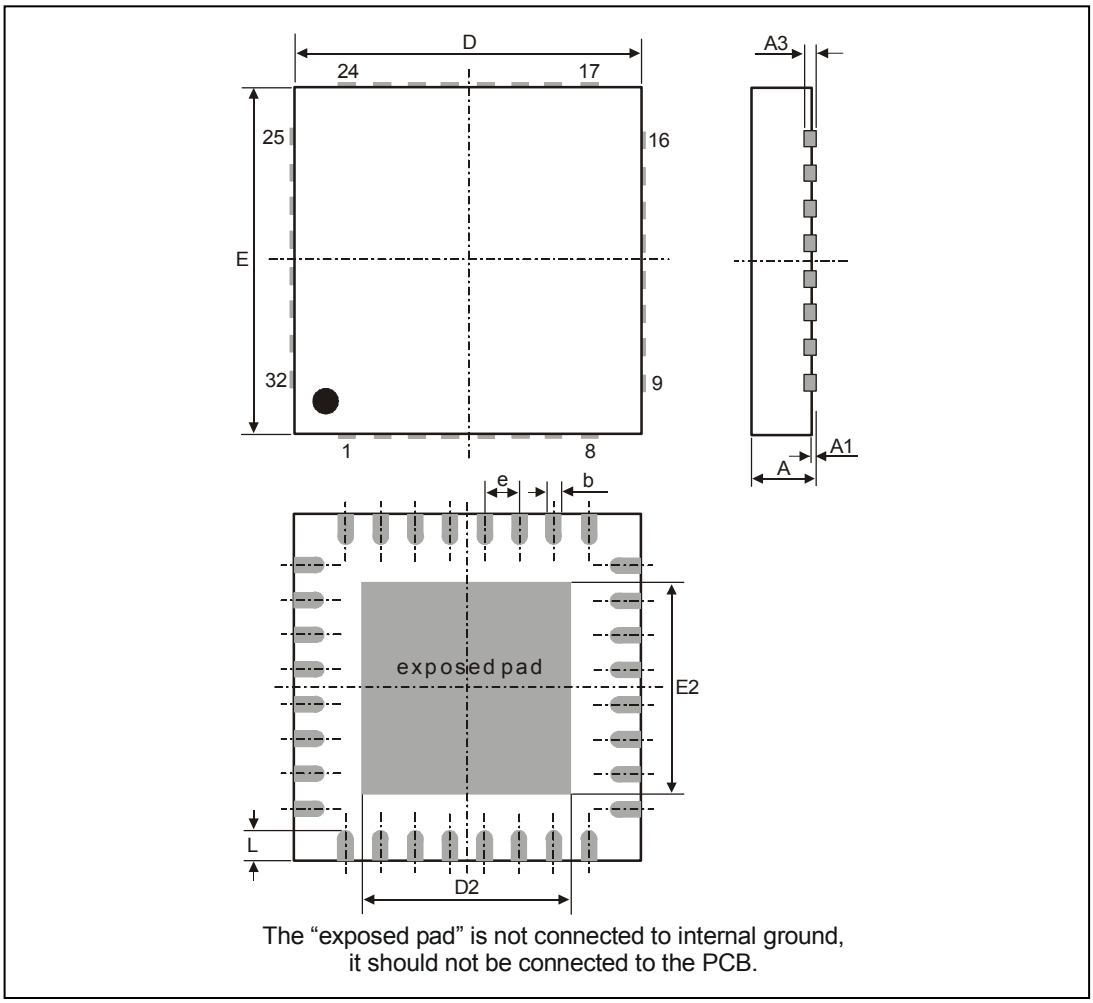


Fig 12: 32L QFN 5x5 Quad

all Dimension in mm										
	D	**E**	**D2**	**E2**	**A**	**A1**	**A3**	**L**	**e**	**b**
min	4.75	4.75	3.00	3.00	0.80	0	0.20	0.3	0.50	0.18
max	5.25	5.25	3.25	3.25	1.00	0.05		0.5		0.30
all Dimension in inch										
min	0.187	0.187	0.118	0.118	0.0315	0	0.0079	0.0118	0.0197	0.0071
max	0.207	0.207	0.128	0.128	0.0393	0.002		0.0197		0.0118

6.1 Soldering Information

- The device MLX71121 is qualified for MSL3 with soldering peak temperature 260 deg C according to JEDEC J-STD-20.

7 Reliability Information

This Melexis device is classified and qualified regarding soldering technology, solderability and moisture sensitivity level, as defined in this specification, according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices (classification reflow profiles according to table 5-2)"

Wave Soldering SMD's (Surface Mount Devices)

- EN60749-20
  "Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat"

Solderability SMD's (Surface Mount Devices)

- EIA/JEDEC JESD22-B102
  "Solderability"

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

8 ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

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