MMA040PP5

Datasheet

DC–27 GHz GaAs MMIC Distributed Low-Noise Amplifier

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Microsemi

Power Matters.™

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

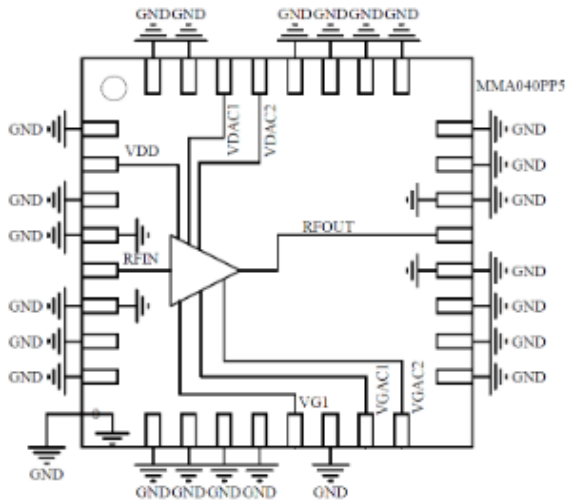
Revision 1.0 was published in May 2017. It was the first publication of this document.

2 Product Overview

MMA040PP5 is a gallium arsenide (GaAs) monolithic microwave integrated circuit (MMIC) pseudomorphic high-electron-mobility transistor (pHEMT) low-noise distributed amplifier in a leadless 5 mm × 5 mm surface-mount package that operates between DC and 27 GHz. It is ideal for test instrumentation and electronic warfare applications. The amplifier provides a flat gain of 16 dB, 2 dB noise figure, and 16 dBm of output power at 1 dBm gain compression while requiring only 60 mA from an 8 V supply. Output IP3 is typically 28 dBm. The MMA040PP5 amplifier features RF I/Os that are internally matched to 50 Ω. It is also available in die form as the MMA040AA.

The following illustration shows the primary functional blocks of the MMA040PP5 device.

Figure 1 • MMA040PP5 Functional Block Diagram



2.1 Applications

The MMA040PP5 device is designed for the following applications:

- Test and measurement instrumentation
- Electronic warfare (EW), electronic countermeasures (ECM), and electronic counter-countermeasures (ECCM)
- Military and space
- Telecom infrastructure
- Wideband microwave radios
- Microwave and millimeter-wave communication systems

2.2 Key Features

The following are key features of the MMA040PP5 device:

- Frequency range: DC to 27 GHz
- Flat gain: 16 dB
- High-output IP3: 28 dBm
- Low-noise figure: 2 dB at 12 GHz
- Supply voltage: 8 V at 60 mA
- 50 Ω matched I/O
- 32-lead 5 mm × 5 mm QFN package: 25 mm²

3 Electrical Specifications

This section details the electrical specifications of the MMA040PP5 device.

3.1 Absolute Maximum Ratings

The following table lists the absolute maximum ratings of the MMA040PP5 device.

Table 1 • Absolute Maximum Ratings

Parameter	Rating
Storage temperature	–65 °C to 150 °C
Operating temperature	–40 °C to 85 °C
Drain bias voltage (V_D)	9 V
Gate bias voltage (V_{G1} and V_{G2})	–2 V to 0.5 V
V_D current (I_{DD})	90 mA
RF input power	22 dBm
DC power dissipation (T = 85 °C)	1.1 W
Channel temperature	150 °C
Thermal impedance	60 °C/W
ESD HBM	TBD

3.2 Specified Electrical Performance

The following table lists the specified electrical performance of the MMA040PP5 device at 25 °C, where V_{DD} is 8 V and I_{DD} is 60 mA.

Table 2 • Specified Electrical Performance

Parameter	Frequency Range	Min	Typ	Max	Units
Operational frequency range		DC	20	27	GHz
Gain	DC–6 GHz	15.5	16		dB
Gain	6 GHz–12 GHz	15.5	16		dB
Gain	12 GHz–20 GHz	15	15.5		dB
Gain flatness	DC–6 GHz		±0.3		dB
Gain flatness	6 GHz–12 GHz		±0.2		dB
Gain flatness	12 GHz–20 GHz		±0.3		dB
Noise figure	DC–6 GHz		3	4	dB
Noise figure	6 GHz–12 GHz		2	3	dB
Noise figure	12 GHz–20 GHz		2.5	3.5	dB
Input return loss	DC–6 GHz		15		dB
Input return loss	6 GHz–12 GHz		15		dB
Input return loss	12 GHz–20 GHz		15		dB
Output return loss	DC–6 GHz		12		dB
Output return loss	6 GHz–12 GHz		12		dB
Output return loss	12 GHz–20 GHz		12		dB
P1dB	DC–6 GHz	13	16		dBm
P1dB	6 GHz–12 GHz	13	16		dBm
P1dB	12 GHz–20 GHz	12	15		dBm
OIP3	DC–6 GHz		28		dBm
OIP3	6 GHz–12 GHz		28		dBm
OIP3	12 GHz–20 GHz		27		dBm
V_{DD} (drain voltage supply)			8		V
I_{DD} (drain current)			60		mA

3.3 Typical Performance Curves

The following graphs show the typical performance curves of the MMA040PP5 device at 25 °C, where V_{DD} = 7 V and I_{DD} = 60 mA (unless otherwise stated).

Figure 2 • S21 vs. Temperature

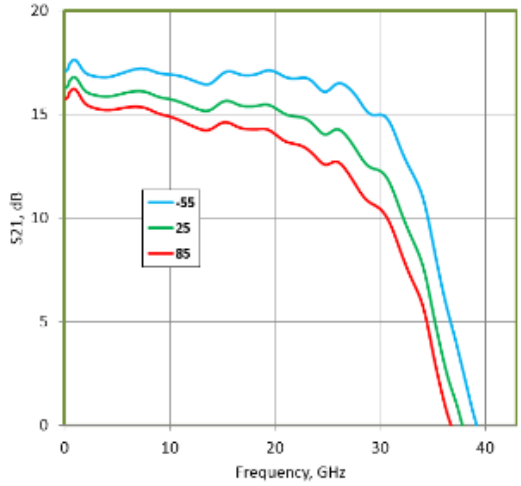


Figure 3 • S11 vs. Temperature

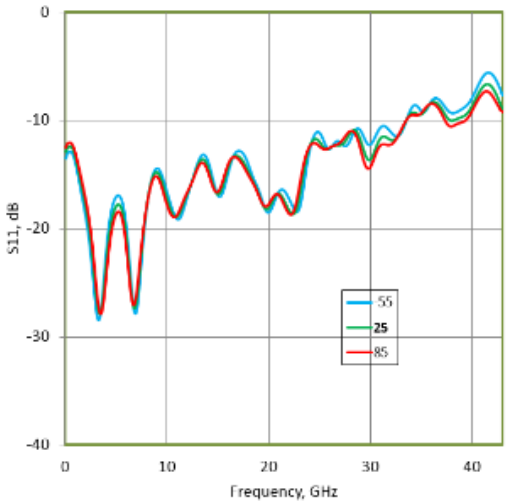


Figure 4 • Output Return Loss vs. Temp (Vdd = 8 V)

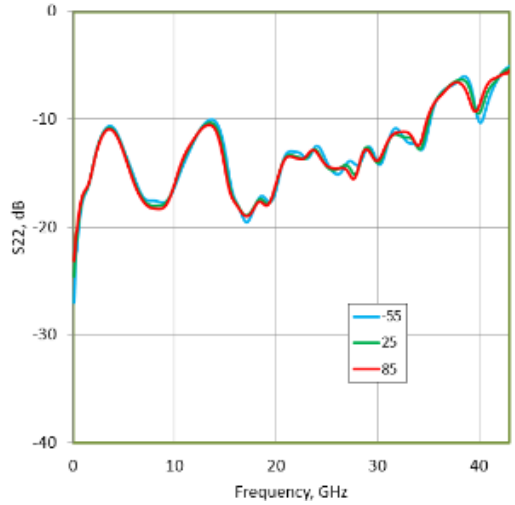


Figure 5 • Noise Figure vs. Temperature

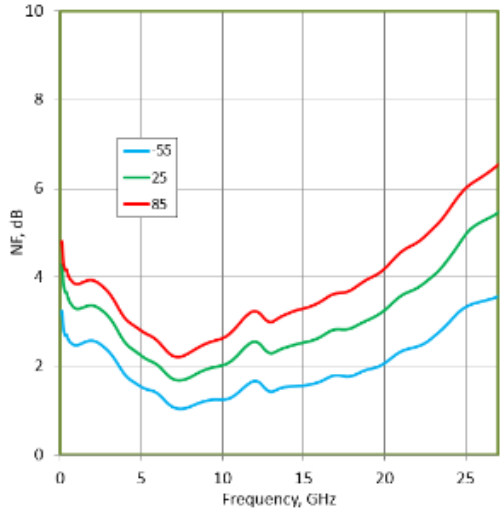


Figure 6 • P1dB Output Power vs. Temperature

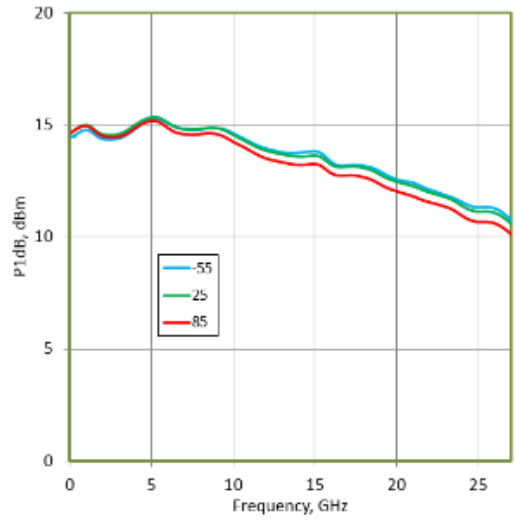


Figure 7 • P3dB Output Power vs. Temperature

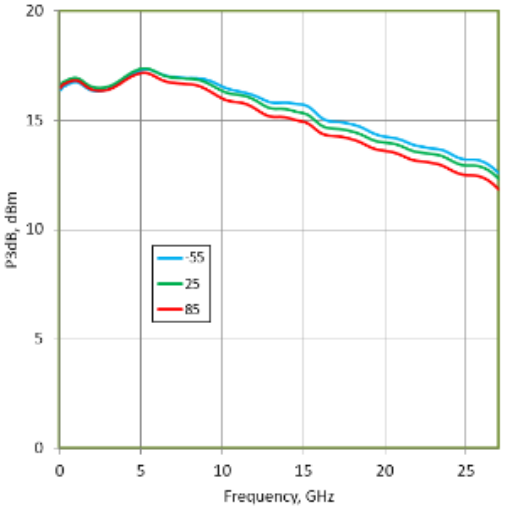


Figure 8 • Output IP3 vs. Temperature

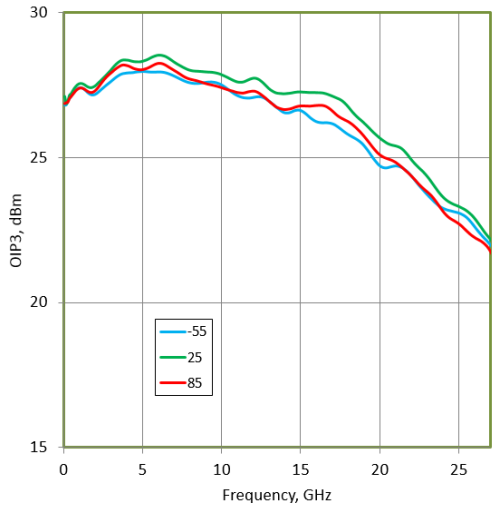


Figure 9 • S21 vs. Vdd

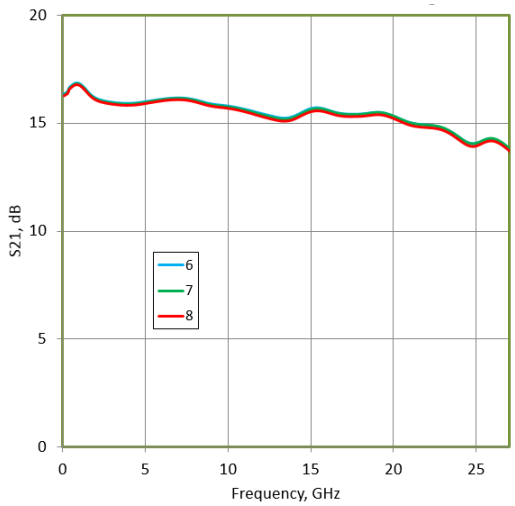


Figure 10 • Noise Figure Response vs. Vdd

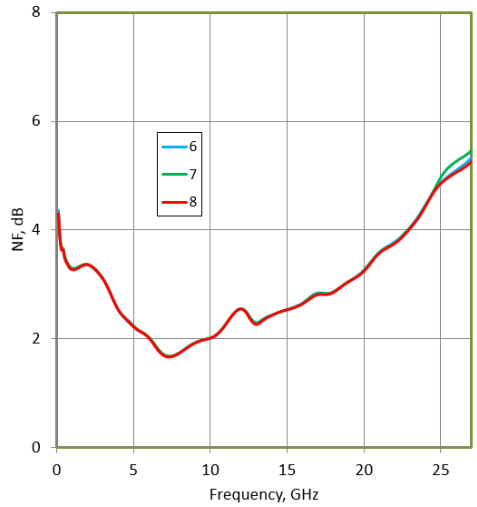


Figure 11 • P1dB vs. Voltage

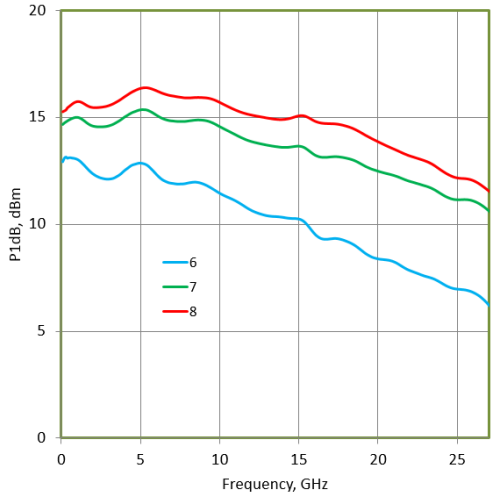


Figure 12 • P3dB vs. Voltage

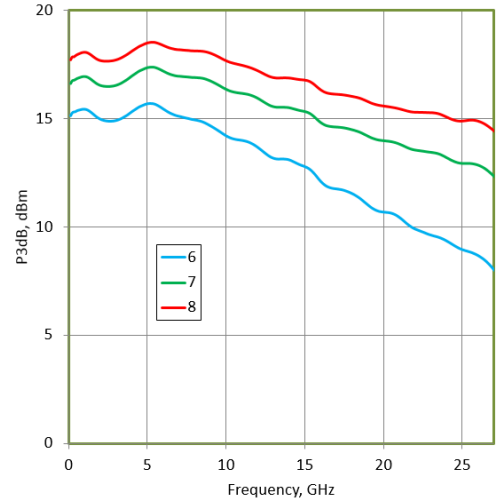


Figure 13 • Output IP3 vs. Voltage

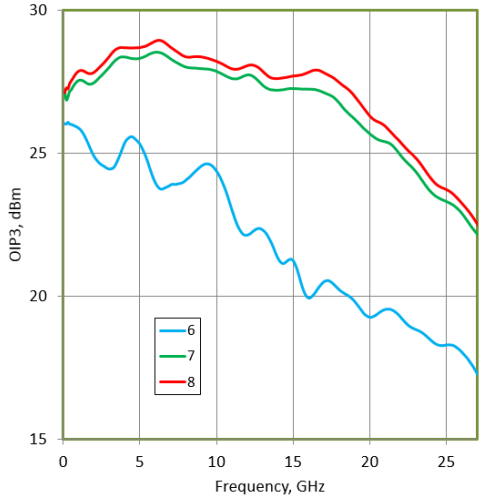


Figure 14 • Second Harmonic Level Suppression (Pout=5 dBm)

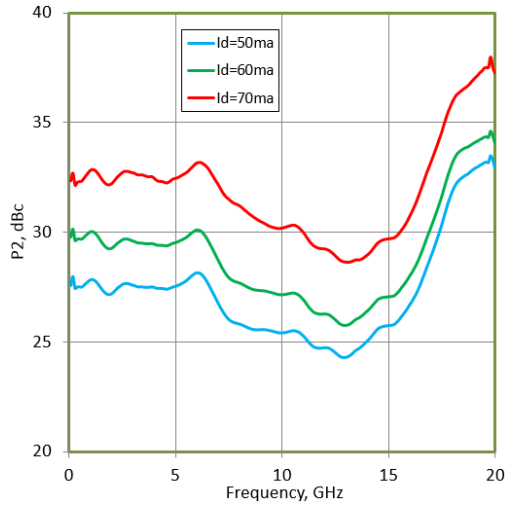
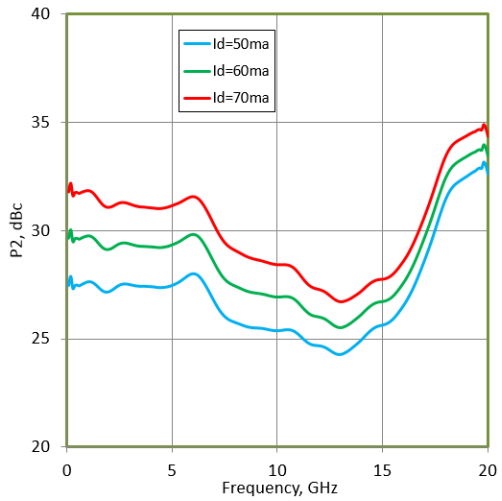


Figure 15 • Second Harmonic Level (Pout=5 dBm, Vdd=8 V)



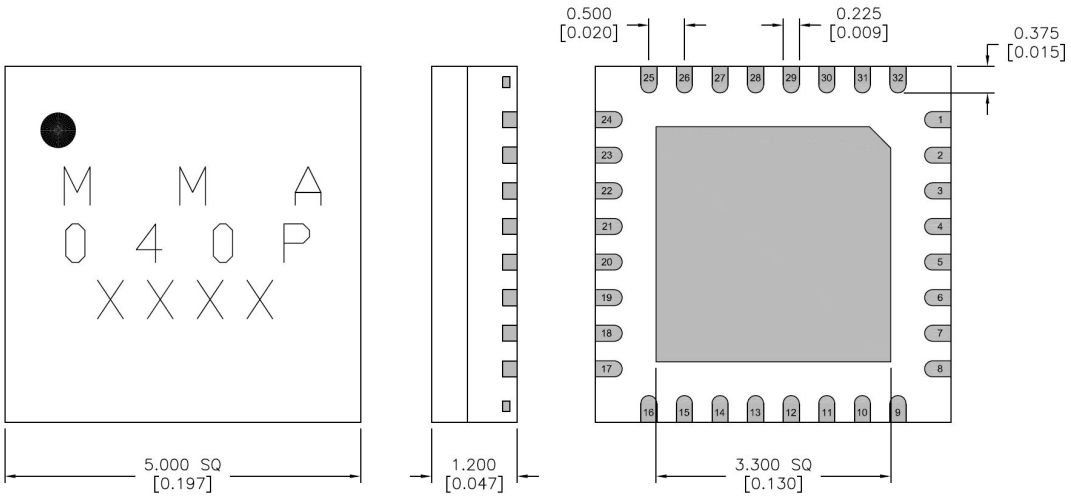
4 Package Specification

This section details the package specifications of the MMA040PP5 device.

4.1 Package Outline Drawing

The following illustration shows the package outline of the MMA040PP5 device. Dimensions are in millimeters [inches].

Figure 16 • Package Outline



4.2 Package Information

The following table lists the package information of the MMA040PP5 device. For additional packaging information, contact your Microsemi sales representative.

Table 3 • Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking
MMA040PP5	Low-stress injection molded plastic	Ni/Pd/Au	TBD	MMA 040P wwyy

4.3 Pin Descriptions

The following table provides pin description information of the MMA040PP5 device.

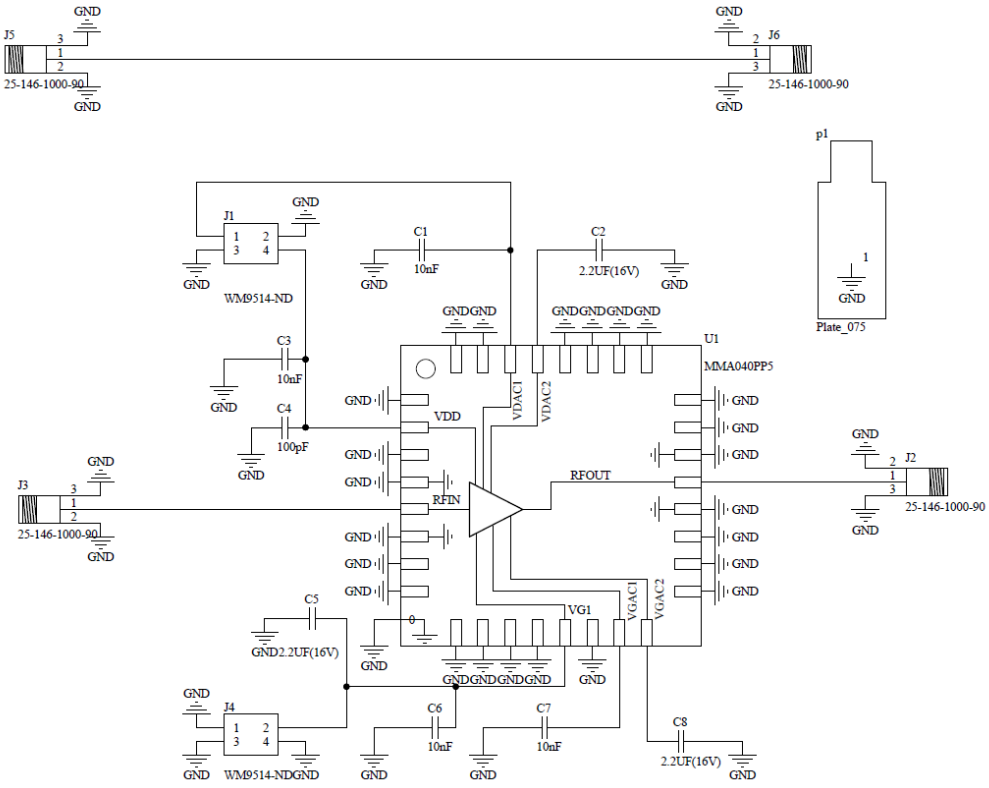
Table 4 • Pin Descriptions

Pin Number	Pin Name	Description
1, 3, 7, 8, 9, 10, 11, 12, 14, 17, 18, 19, 23, 24, 25, 26, 27, 28, 31, 32	N/C	These pins are not connected internally. All data was measured with these pins connected to RF/DC ground externally.
4, 6, 20, 22	GND	Ground paddle must be connected to RF/DC ground.
5	RFIN	This pin is DC-coupled and matched to 50 Ω.
13	VG1	Gate control for the amplifier.
15, 16	VGAC1, VG1B	Low-frequency termination. Connect bypass capacitors per application circuit below.
29, 30	VDAC1, VDAC2	Low-frequency termination. Connect bypass capacitors per application circuit below.
21	RFOUT	This pin is DC-coupled and matched to 50 Ω.
2	VDD	Power supply voltage for the amplifier. External bypass capacitors are required.
Backside paddle	RF/DC GND	RF/DC ground.

4.4 Application Circuit

The following illustration shows the application circuit of the MMA040PP5 device.

Figure 17 • Application Circuit



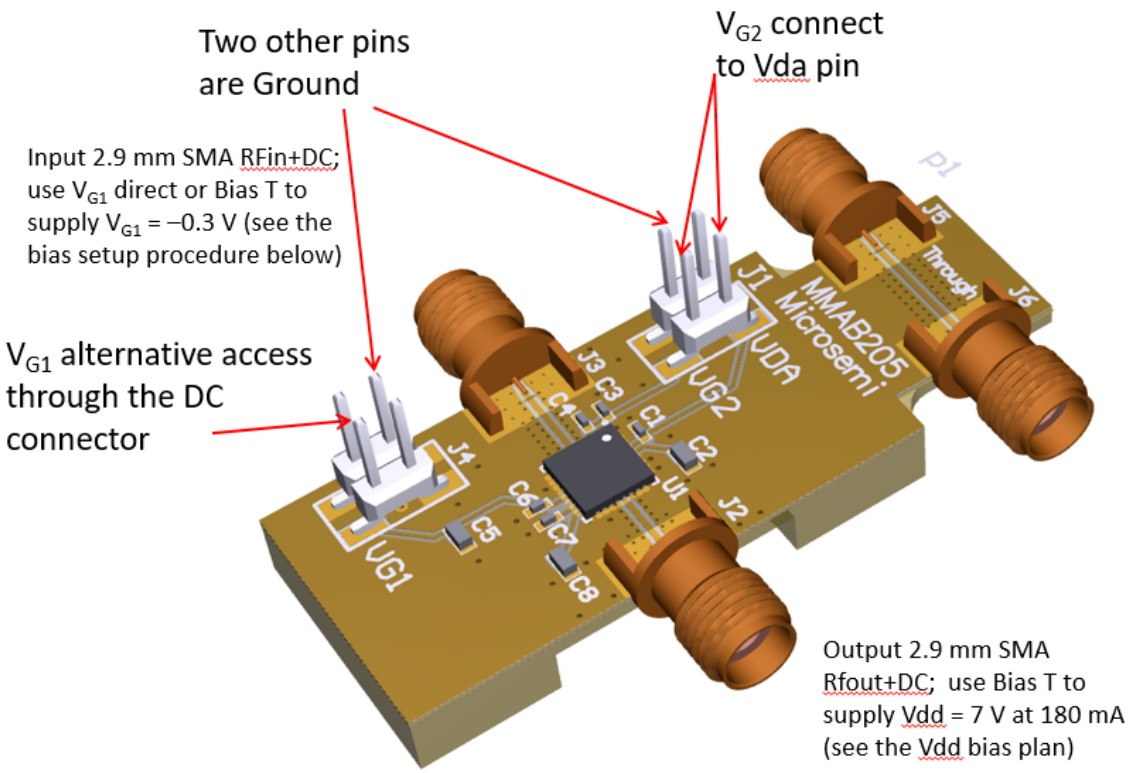
5 Handling Recommendations

Gallium arsenide integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note AN01 GaAs MMIC Handling and Die Attach Recommendations.

6 Evaluation Board Information

The following illustration shows the application circuit of the MMA040PP5 device.

Figure 18 • Evaluation Board



The circuit board used in the application should be generated with proper RF circuit design techniques. Signal lines at the RF port should have 50 Ω impedance, and the package ground leads and backside ground paddle should be connected directly to the ground plane similar to the previous image.

Table 5 • Materials for Evaluation Board

Item	Description
C1, C3, C6, C7	CAP 10 nF 50 V –20% to +80% 0402 (1005 metric) thickness 0.6 mm SMD
C2, C5, C8	2.2 µF 16 V ceramic capacitor X5R 0603 (1608 metric) 0.063" L × 0.031" W (1.60 mm × 0.80 mm)
C4	CAP 100 pF 50 V ±10% 0402 (1005 metric) thickness 0.6 mm SMD
J1, J4	Header, 2-pin, dual row
J2, J3, J5, J6	CONN 2.9 mm female PCB edge mount .012 pin
P1	Plate 749-MM-0198
U1	MMIC MMA040PP5

7 Ordering Information

The following table lists the ordering information for the MMA040PP5 device.

Table 6 • Ordering Information

Part Number	Package
MMA040PP5	5 mm × 5 mm plastic QFN package
MMA040PP5E	Evaluation board for MMA040PP5

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