MP173

700 V Non-Isolated Off-Line Regulator Up to 280 mA Output Current

The Future of Analog IC Technology

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DESCRIPTION

MP173 is a primary-side regulator that provides accurate constant voltage (CV) regulation without an opto-coupler. It supports buck, boost, buck-boost, and flyback topologies. It has an integrated 700 V MOSFET to simplify the structure and reduce cost. These features make it an ideal regulator for offline, low-power applications, such as home appliances and standby power.

MP173 is a green-mode-operation regulator. Both the peak current and switching frequency decrease as the load decreases. This feature provides excellent efficiency at light load and improves the overall average efficiency.

MP173 has various protection features including thermal shutdown (TSD), VCC under-voltage lockout (UVLO), overload protection (OLP), short-circuit protection (SCP), and open-loop protection.

MP173 is available in a small TSOT23-5 package and SOIC-8 package.

FEATURES

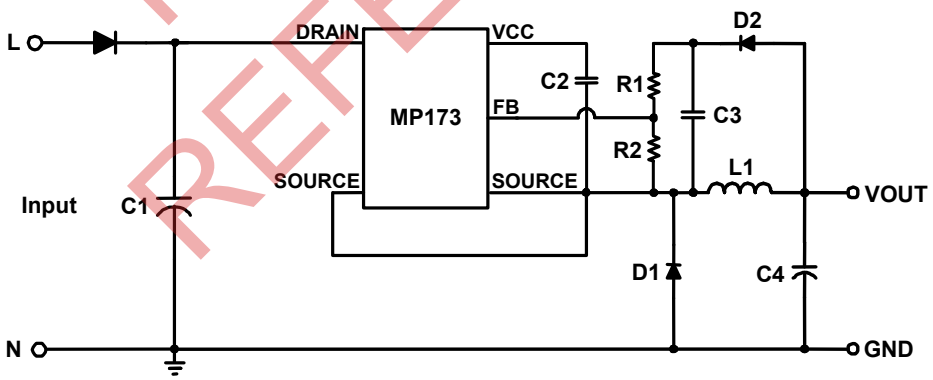
- Primary-Side CV Control, Supporting Buck, Boost, Buck-Boost, and Flyback Topologies
- Integrated 700 V MOSFET and Current Source
- < 30 mW No-Load Power Consumption
- Up to 4 W Output Power
- Maximum DCM Output Current Less than 180 mA
- Maximum CCM Output Current Less than 280 mA
- Low VCC Operating Current
- Frequency Foldback
- Limited Maximum Frequency
- Peak-Current Compression
- Internally Biased VCC
- TSD, UVLO, OLP, SCP, Open-Loop Protection

APPLICATIONS

- Home Appliances, White Goods, and Consumer Electronics
- Industrial Controls
- Standby Power

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number	Package	Top Marking
MP173GJ*	TSOT23-5	*See Below*
MP173GS**	SOIC-8	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP173GJ–Z).

** For Tape & Reel, add suffix –Z (e.g. MP173GS–Z).

TOP MARKING (TSOT23-5)

|ANZY

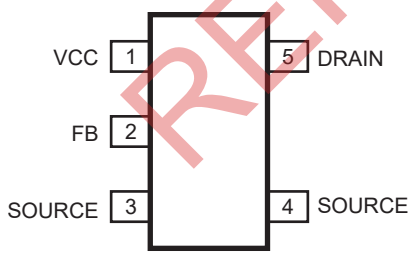
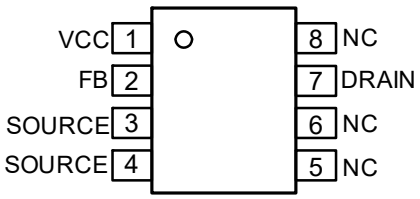
ANZ: product code of MP173GJ;
Y: year code;

TOP MARKING (SOIC-8)

MP173
LLLLLLLL
MPSYWW

MP173: part number;
LLLLLLLL: lot number;
MPS: MPS prefix:
Y: year code;
WW: week code:

PACKAGE REFERENCE

TOP VIEW	TOP VIEW
	
TSOT23-5	**SOIC-8**

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ABSOLUTE MAXIMUM RATINGS (1)

DRAIN to SOURCE (T_J =+25°C).-0.3 V to 700 V
All other pins .....-0.3 V to 6.5 V
Continuous power dissipation .....(T_A = +25°C)(2)
TSOT23-5 ..... 1 W
SOIC-8 ..... 1 W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -60°C to +150°C

Recommended Operating Conditions (3)

Operating junction temp. (T_J). .. -40°C to +125°C
Operating VCC range .....5.5 V to 5.7 V

Thermal Resistance (4)	θ_{JA}	θ_{JC}	
TSOT23-5	100	55	°C/W
SOIC-8	96	45	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature TA. The maximum allowance continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowance power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuit protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

VCC = 5.5 V, T_J = -40°C~125°C, min and max are guaranteed by characterization, typical is tested under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Start-up Current Source and Internal MOSFET (DRAIN)						
Internal regulator supply current	$I_{regulator}$	VCC = 4 V; V_{Drain} = 100 V	2.2	4.1	6	mA
DRAIN leakage current	I_{Leak}	VCC = 5.8 V; V_{Drain} = 400 V		10	17	μA
Breakdown voltage	$V_{(BR)DSS}$	T_J = 25°C	700			V
ON resistance	R_{on}	T_J = 25°C		14	18	Ω
		T_J = 125°C		22	27	Ω
Supply Voltage Management (VCC)						
VCC level (increasing) where the internal regulator stops	VCC_{OFF}		5.4	5.7	6	V
VCC level (decreasing) where the internal regulator turns on	VCC_{ON}		5.1	5.5	5.8	V
VCC regulator on and off hysteresis			130	250		mV
VCC level (decreasing) where the IC stops	VCC_{stop}		3	3.4	3.6	V
VCC level (decreasing) where the protection phase ends	VCC_{pro}		2	2.5	2.8	V
Internal IC consumption	I_{CC}	f_s = 28 kHz, D = 67.8%			720	μA
Internal IC consumption (no switching)	I_{CC}				200	μA
Internal IC consumption, latch-off phase	$I_{CCLATCH}$	VCC = 5.3 V		16	24	μA
Internal Current Sense						
Peak current limit	I_{Limit}	T_J = 25°C	380	420	460	mA
Leading-edge blanking	τ_{LEB1}			350		ns
SCP threshold	I_{SCP}	T_J = 25°C	500	600	760	mA
Leading-edge blanking for SCP (1)	τ_{LEB2}			180		ns
Feedback Input (FB)						
Minimum off time	τ_{minoff}		9	12	15	μs
Maximum on time	τ_{manon}		17	24	31	μs
Primary MOSFET feedback turn-on threshold	V_{FB}		2.45	2.55	2.65	V
OLP feedback trigger threshold	V_{FB_OLP}		1.64	1.74	1.84	V
OLP delay time	τ_{OLP}	f_s = 28 kHz		220		ms
Open-loop detection	V_{OLD}		0.4	0.5	0.6	V
Thermal Shutdown						
Thermal shutdown threshold (1)				150		°C
Thermal shutdown recovery hysteresis (1)				30		°C

NOTE:

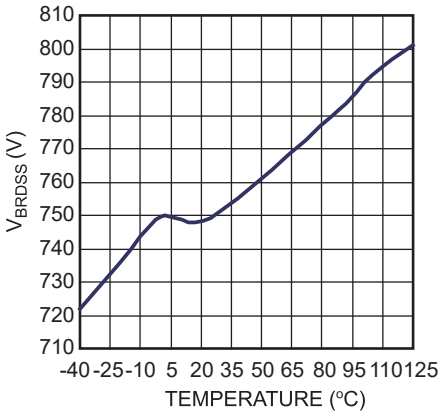
1) This parameter is guaranteed by design.

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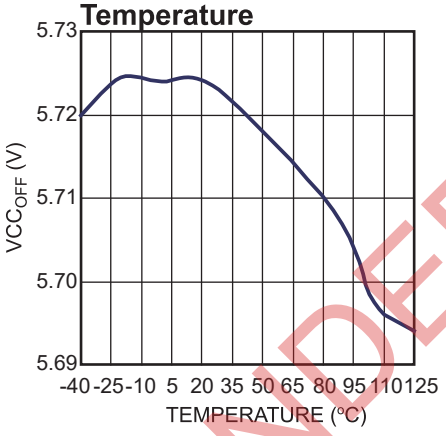
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TYPICAL CHARACTERISTICS

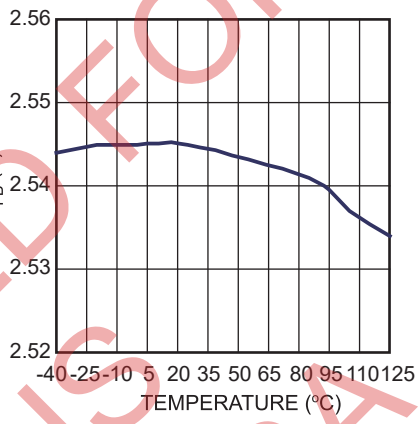
Breakdown Voltage vs. Temperature



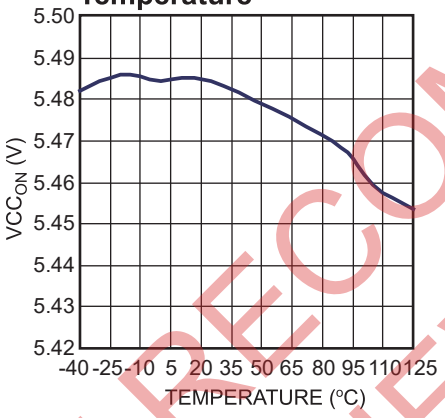
VCC Increasing Level at which the Internal Regulator Stops vs. Temperature



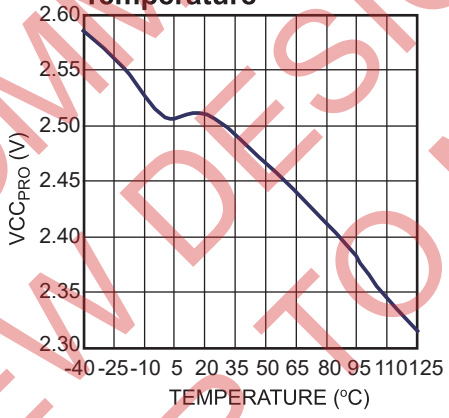
Feedback Voltage vs. Temperature



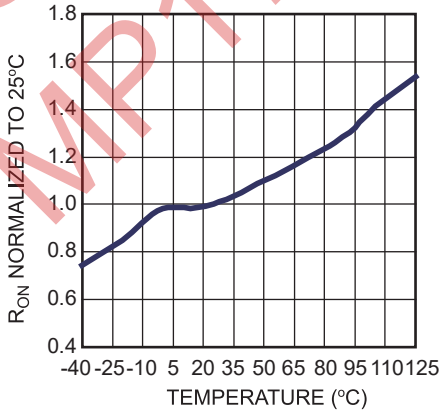
VCC Decreasing Level at which the Internal Regulator Turns On vs. Temperature



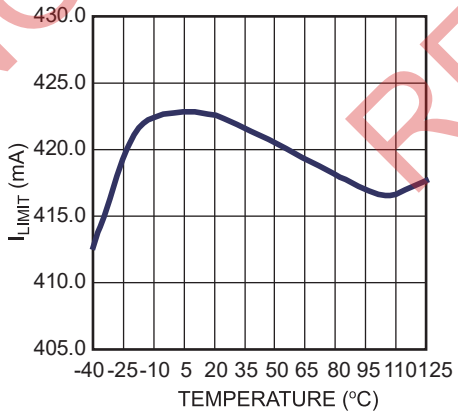
VCC Decreasing Level at which the Protection Phase Ends vs. Temperature



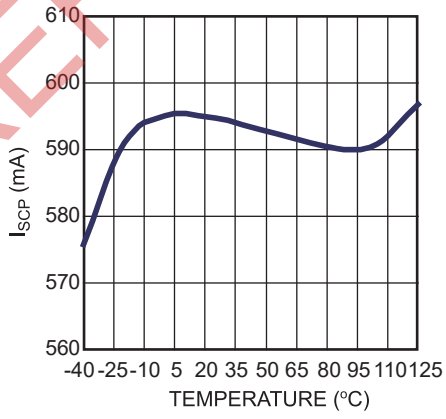
On State Resistance vs. Temperature



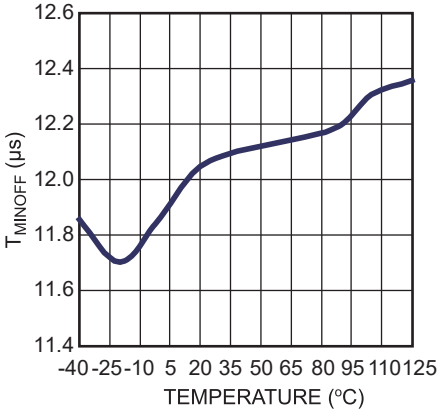
Peak Current Limit vs. Temperature



SCP Point vs. Temperature



Minimum Off Time vs. Temperature



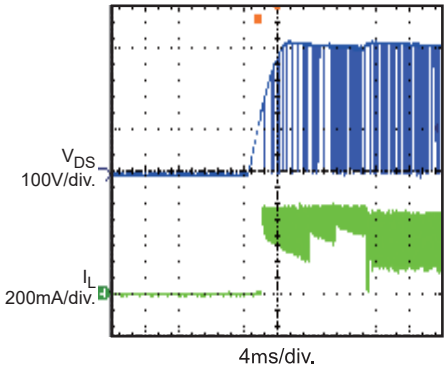
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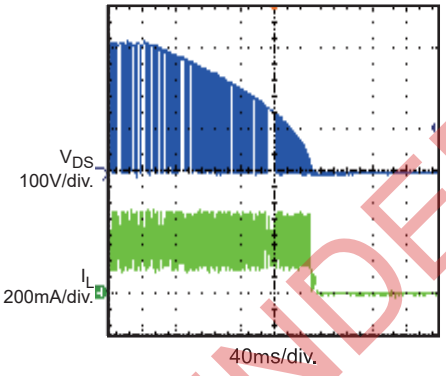
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 230 VAC, V_{OUT} = 12 V, I_{OUT} = 250 mA, L = 1.2 mH, C_{OUT} = 100 µF, T_A = +25°C, unless otherwise noted.

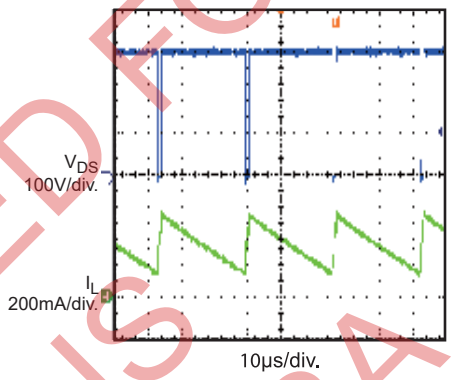
Input Power Start-Up



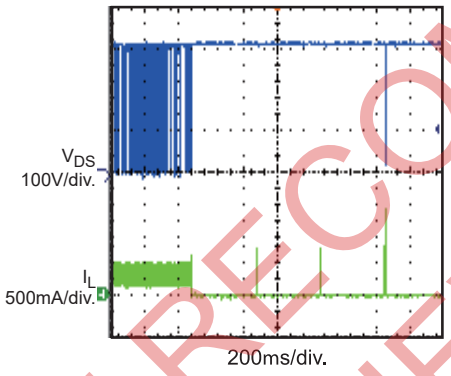
Input Power Shutdown



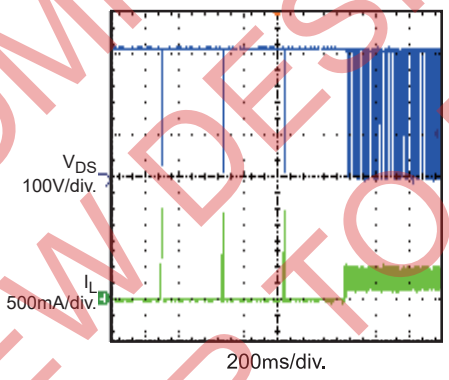
Normal Operation



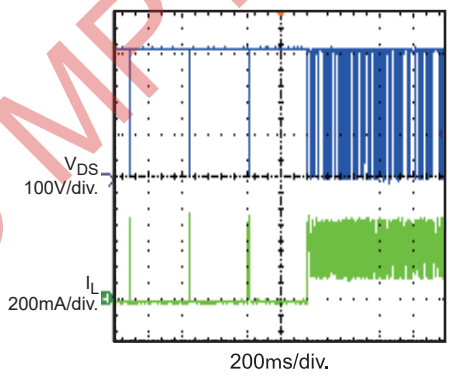
SCP Entry



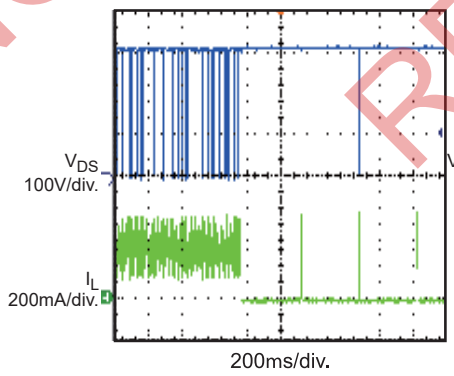
SCP Recovery



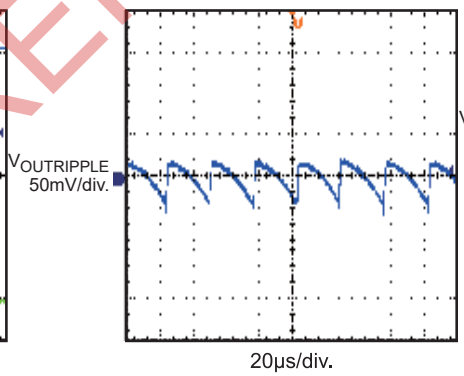
Open Loop Entry



Open Loop Recovery

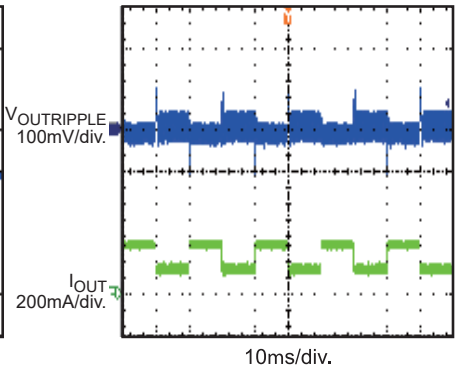


Output Voltage Ripple



Load Transient

1/2 Load to Full Load



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PIN FUNCTIONS

Pin # TSOT23-5	Pin # SOIC8	Name	Description
1	1	VCC	Control circuit power supply.
2	2	FB	Regulator feedback.
3,4	3,4	SOURCE	Internal power MOSFET source and ground reference for VCC and FB.
5	7	DRAIN	Internal power MOSFET drain and high-voltage current source input.
	5,6,8	NC	No connection.

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FUNCTIONAL BLOCK DIAGRAM

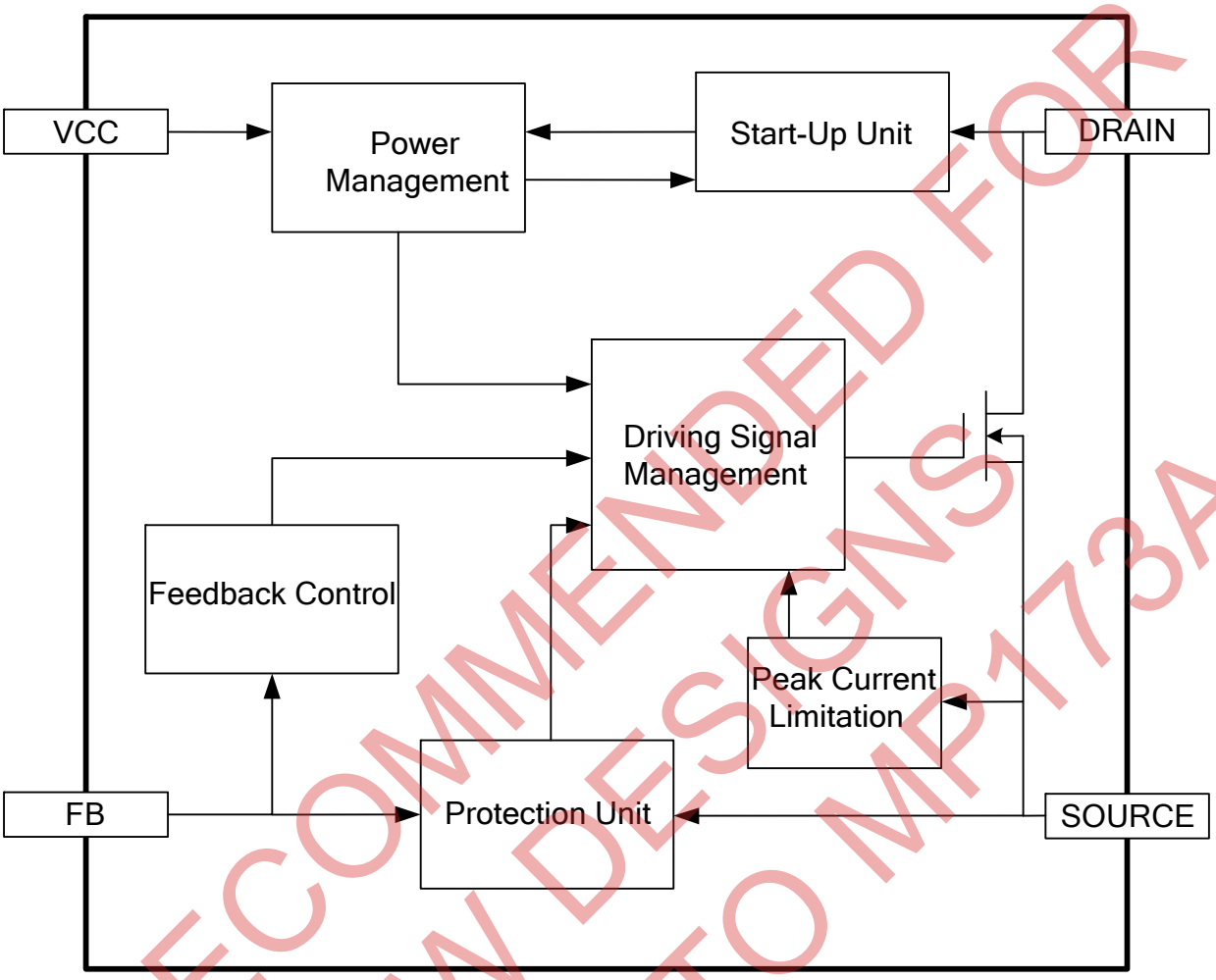


Figure 1—Functional block diagram

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OPERATION

MP173 is a green-mode-operation regulator: The peak current and the switching frequency both decrease with a decreasing load. As a result, it offers excellent light-load efficiency and improves overall average efficiency. Also, the regulator incorporates multiple features and operates with a minimum number of external components.

The MP173 acts as a fully integrated regulator when used in buck topology (see Typical Application on page 1).

Start-Up and Under-Voltage Lockout

The internal high-voltage regulator self-supplies the IC from DRAIN. When VCC voltage reaches VCC_{OFF}, the IC starts switching, and the internal high-voltage regulator turns off. The internal high-voltage regulator turns on to charge the external VCC capacitor when the VCC voltage falls below VCC_{ON}. A small capacitor (in the low µF range) maintains the VCC voltage and thus lowers the capacitor cost.

The IC stops switching when the VCC voltage drops blow VCC_{stop}.

Under fault conditions—such as OLP, SCP, and TSD—the IC stops switching, and an internal current source (~16 µA) discharges the VCC capacitor. The internal high-voltage regulator will not charge the VCC capacitor until the VCC voltage drops below VCC_{pro}. The re-start time can be estimated using Equation (1):

$$\tau_{restart} = C_{VCC} \times \left(\frac{VCC - VCC_{pro}}{I_{CCLATCH}} + \frac{VCC_{OFF} - VCC_{pro}}{I_{regulator}} \right) \quad (1)$$

Soft Start (SS)

The IC stops operation when the VCC voltage drops blow $VCC_{stop;}$ the IC starts operation when VCC charges to VCC_{OFF}. Every time the chip starts operation there is a soft-start period. The soft start prevents the inductor current from overshooting by limiting the minimum off time.

MP173 adopts a 2 phase minimum off time limit soft start. Each soft-start phase retains 128 switching cycles. During a soft start, the off time limit gradually shortens from 48 µs to 24 µs and finally reaches the normal operation off-time limit (see Figure 2).

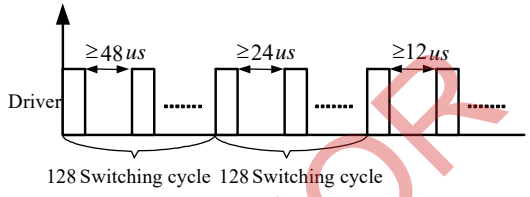


Figure 2—τ_{minoff} at start-up

Constant Voltage (CV) Operation

The MP173 regulates the output voltage by monitoring the sampling capacitor (C3).

At the beginning of each cycle, the integrated MOSFET turns on while the feedback voltage drops below the 2.55 V reference voltage, which indicates insufficient output voltage. The peak current limitation determines the on period. After the on period elapses, the integrated MOSFET turns off. The sampling capacitor (C3) voltage is charged to the output voltage when the freewheeling diode (D1) turns on. In this way, the sampling capacitor (C3) samples and holds the output voltage for output regulation. The sampling capacitor (C3) voltage decreases when the L1 inductor current falls below the output current. When the feedback voltage falls below the 2.55 V reference voltage, a new switching cycle begins. Figure 3 shows this operation in continuous conduction mode (CCM).

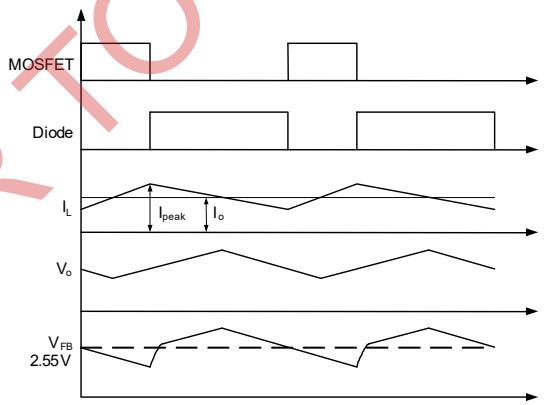


Figure 3—V_{FB} vs. V_O

Equation (2) determines the output voltage:

$$Vo = 2.55V \times \frac{R1 + R2}{R2} \quad (2)$$

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Frequency Foldback and Peak Current Compression

The MP173 remains highly efficient at light-load conditions by reducing the switching frequency automatically.

Under light-load or no-load conditions, the output voltage drops very slowly, which increases the MOSFET off time. Thus, the frequency decreases along with the load.

The switching frequency is determined with Equation (3) and Equation (4):

$$f_s = \frac{(V_{in} - V_o)}{2L(I_{peak} - I_o)} \cdot \frac{V_o}{V_{in}}, \text{ for CCM} \quad (3)$$

$$f_s = \frac{2(V_{in} - V_O)}{LI^2_{peak}} \cdot \frac{I_o V_o}{V_{in}}, \text{ for DCM} \quad (4)$$

As the peak current limit decreases from 420 mA, the off time increases. In standby mode, the frequency and the peak current are both minimized, allowing for a smaller dummy load. As a result, peak current compression helps further reduce no-load consumption. The peak current limit can be estimated from Equation (5) where τ_{off} is the off time of the power module:

$$I_{Peak} = 420mA - (1.6mA/\mu s) \times (\tau_{off} - 12\mu s) \quad (5)$$

EA Compensation

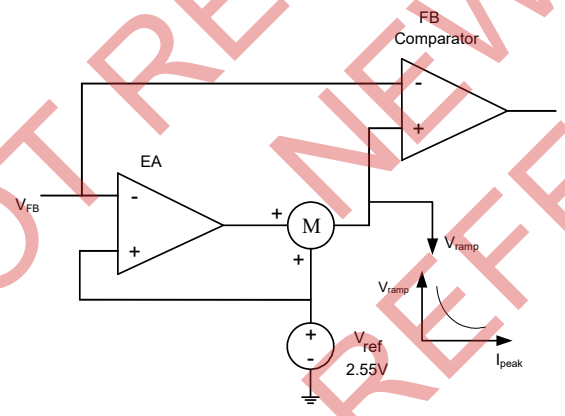


Figure 4—EA and ramp compensation

MP173 has an internal error amplifier (EA) compensation loop. It samples the feedback voltage 6 µs after the MOSFET turns off and regulates the output based on the 2.55 V reference voltage.

Ramp Compensation

An internal ramp compensation circuit improves the load regulation. An exponential voltage signal is added to pull down the reference voltage of the feedback comparator (see Figure 4). The ramp compensation is a function of the load conditions: the compensation is about the 1 mV/µs under full-load conditions. The compensation increases exponentially as the peak current decreases.

Over-Load Protection (OLP)

The maximum output power of the MP173 is limited by the maximum switching frequency and peak current limit. If the load current is too large, the output voltage drops, causing the FB voltage to drop.

When the FB voltage drops below V_{FB_OLP}, it is considered an error flag, and the timer starts. If the timer reaches 220 ms (f_S = 28 kHz), OLP occurs. This timer duration avoids triggering OLP when the power supply starts up or the load transitions. The power supply should start up in less than 220 ms (f_S = 28 kHz). The OLP delay time is calculated using Equation (6):

$$\tau_{Delay} \approx 220ms \times \frac{28kHz}{f_s} \quad (6)$$

Short-Circuit Protection (SCP)

The MP173 monitors the peak current and shuts down when the peak current rises above the SCP threshold through short-circuit protection. The power supply resumes operation with the removal of the fault.

Thermal Shutdown (TSD)

To prevent thermal induced damage, the MP173 stops switching when the junction temperature exceeds 150°C. During thermal shutdown (TSD), the VCC capacitor is discharged to VCC_{pro},, and the the internal high-voltage regulator re-charges. MP173 recovers when the junction temperature drops below 120°C.

Open-Loop Detection

If V_{FB} is less than 0.5 V, the IC stops switching and a re-start cycle begins. During a soft start, the open-loop detection is blanked.

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Leading-Edge Blanking

An internal leading-edge blanking (LEB) unit avoids premature switching pulse termination due to a turn-on spike. A turn-on spike is caused by parasitic capacitance and reverse recovery of the freewheeling diode. During the blanking time, the current comparator is disabled and cannot turn off the external MOSFET. Figure 5 shows the leading-edge blanking.

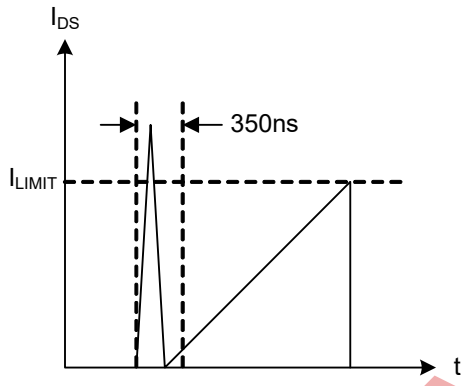


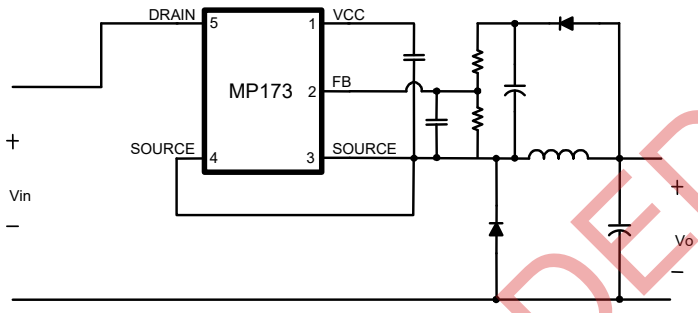
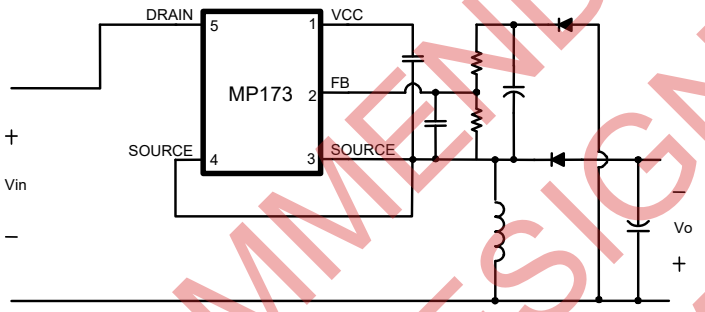
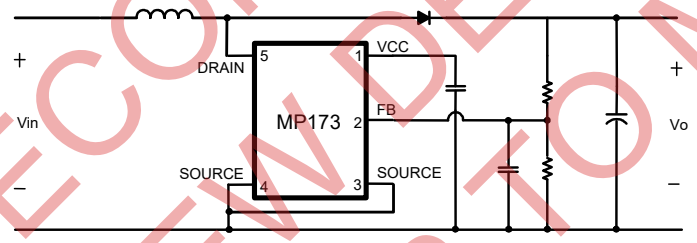
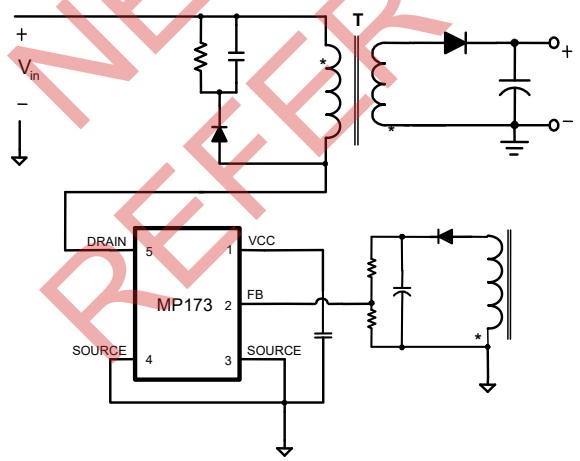
Figure 5—Leading-edge blanking

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APPLICATION INFORMATION

Table 1—Common topologies using MP173

Topology	Circuit Schematic	Features
High-side buck		1. No isolation 2. Positive output 3. Low cost 4. Direct feedback
High-side buck-boost		1. No isolation 2. Negative output 3. Low cost 4. Direct feedback
Boost		1. No isolation 2. Positive output 3. Low cost 4. Direct feedback
Flyback		1. Isolation 2. Positive output 3. Low cost 4. Indirect feedback

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Topology Options

MP173 can be used in common topologies such as buck, boost, buck-boost, and flyback (see Table 1).

Component selection below is based on the typical application of MP173 (see it on page 1).

Component Selection

Input Capacitor

The input capacitor supplies the DC input voltage for the converter. Figure 6 shows the typical DC bus voltage waveform of a half-wave rectifier and a full-wave rectifier.

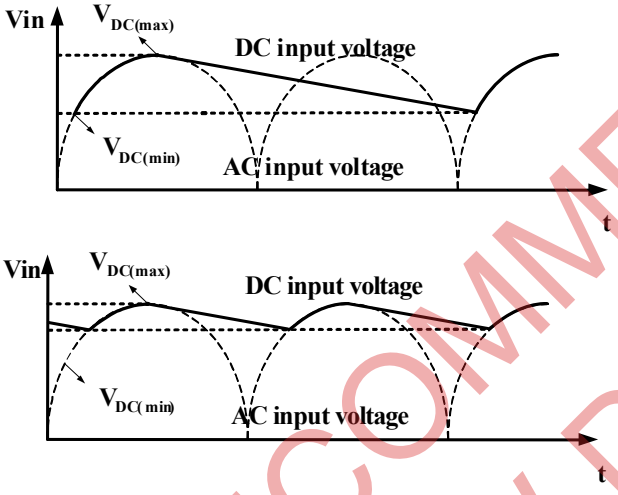


Figure 6—Input voltage waveform

Typically, the use of a half-wave rectifier requires an input capacitor rated at 3 μF/W for the universal input condition. When using a full-wave rectifier, the input capacitor is chosen between 1.5~2 μF/W for the universal input condition. A half-wave rectifier is recommended for a < 2 W output application, otherwise use a full-wave rectifier.

Under very low input voltage, the inductor current ramps up slowly; it may not reach the current limit during T_{manon}, so the MOSFET on time should be less than the minimum value of T_{manon}.

Inductor

The MP173 has a minimum off time limit that determines the maximum power output. A power inductor with a larger inductance increases the maximum power. Using a very small inductor may cause failure at full load. Estimate the maximum power using Equation (7) and Equation (8):

$$P_{omax} = V_o(I_{peak} - \frac{V_o \tau_{minoff}}{2L}), \text{ for CCM} \quad (7)$$

$$P_{omax} = \frac{1}{2} L I_{peak}^2 \cdot \frac{1}{\tau_{minoff}}, \text{ for DCM} \quad (8)$$

For mass production, tolerance on the parameters (such as peak current limitation and the minimum off time) should be taken into consideration.

Freewheeling Diode

Select a diode with a maximum reverse-voltage rating greater than the maximum input voltage and a current rating determined by the output current.

The reverse recovery of the freewheeling diode can affect efficiency and circuit operation during a CCM condition, so use an ultra-fast diode such as the EGC10JH.

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Estimate the output voltage ripple using Equation (9) and Equation (10):

$$V_{CCM_ripple} = \frac{\Delta i}{8 f_s C_o} + \Delta i \cdot R_{ESR}, \text{ for CCM} \quad (9)$$

$$V_{DCM_ripple} = \frac{I_o}{f_s C_o} \cdot \left(\frac{I_{pk} - I_o}{I_{pk}} \right)^2 + I_{pk} \cdot R_{ESR}, \text{ for DCM} \quad (10)$$

It is recommended to use ceramic, tantalum, or low ESR electrolytic capacitors to reduce the output voltage ripple.

Feedback Resistors

The resistor divider determines the output voltage. Choose appropriate R1 and R2 values to maintain V_{FB} at 2.55 V. An excessively large value for R2 should be avoided.

Feedback Capacitor

The feedback capacitor provides a sample and hold function. Small capacitors result in poor regulation at light loads, and large capacitors affect the circuit operation. Roughly estimate an optimal capacitor value using Equation (11):

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$$\frac{1}{2}\frac{V_o}{R_1+R_2}\cdot\frac{C_o}{I_o} \le C_{FB} \le \frac{V_o}{R_1+R_2}\cdot\frac{C_o}{I_o} \quad (11)$$

Dummy Load

A dummy load is required to maintain the load regulation. This ensures sufficient inductor energy to charge the sample and hold capacitor to detect the output voltage. Normally a 3 mA dummy load is needed and can be adjusted according to the regulated voltage. There is a compromise between small, no-load consumption and good, no-load regulation, especially for applications that require 30 mW no-load consumption. Use a zener to reduce no-load consumption if no-load regulation is not a concern.

Auxiliary VCC Supply

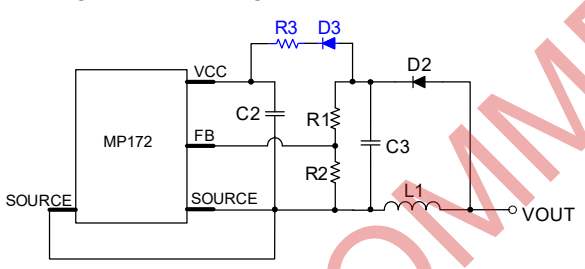


Figure 7—Auxiliary V_{CC} supply circuit

For V_O above 7 V applications, the MP173 achieves the 30 mW no-load power requirement by adopting an external VCC supply to reduce overall power consumption (see Figure 7).

This auxiliary VCC supply is derived from the resistor connected between C2 and C3. C3 should be set larger than the value recommended above. D3 is used in case VCC interferes with FB. R3 is determined Using Equation (12).

$$R3 \approx \frac{V_o - V_{FW} - 5.8V}{I_S} \quad (12)$$

Where I_S is the VCC consumption under a no-load condition, and V_{FW} is the forward voltage drop of D3. Because I_S varies in different applications, R3 should be adjusted to meet the application's specific I_S. In a particular configuration, I_S is measured at about 250 µA.

Surge Performance

An appropriate input capacitor value should be chosen to obtain good surge performance. Figure 8 shows the half-wave rectifier. Table 2 shows the capacitance required under normal conditions for different surge voltages. FR1 is a 20 Ω/2 W fused resistor, and L1 is 1 mH for this recommendation.

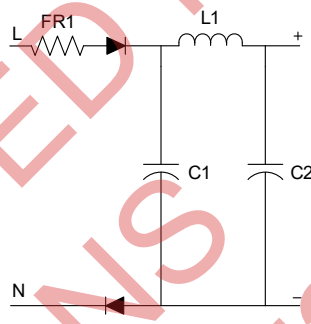


Figure 8—Half-wave rectifier

Table 2—Recommended capacitance

Surge Voltage	500 V	1000 V	2000 V
C1	1 µF	2.2 µF	3.3 µF
C2	1 µF	2.2 µF	3.3 µF

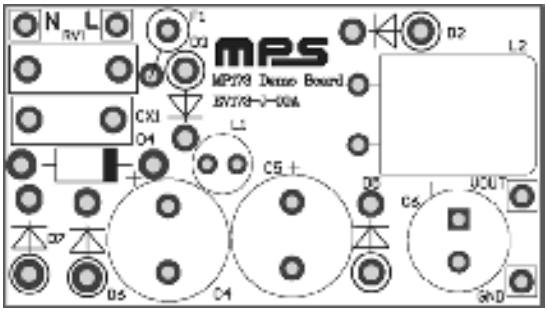
PCB Layout Guidelines

Efficient PCB layout is critical for reliable operation, good EMI, and thermal performance. For best results, follow the guidelines below:

1) Minimize the loop area formed by the input capacitor, IC, freewheeling diode, inductor, and output capacitor.
2) Place the power inductor far away from the input filter while keeping the loop area to the inductor at a minimum (see example below).
3) Place a capacitor valued at several hundred pF between FB and SOURCE as close to the IC as possible.
4) Connect the exposed pads or large copper area with DRAIN to improve thermal performance.

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Top layer

Bottom layer

Design Example

Table 3 shows a design example for the following application guideline specifications:

Table 3—Design example

V_{IN}	85 VAC to 265 VAC
V_{OUT}	12 V
I_{OUT}	250 mA

The detailed application schematic is shown in Figure 9. The typical performance and circuit waveforms have been shown in the “Typical Performance Characteristics” section. For additional device applications, please refer to the related evaluation board datasheets.

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TYPICAL APPLICATION CIRCUITS

Figure 9 shows a typical application example of a 12 V, 250 mA non-isolated power supply using MP173.

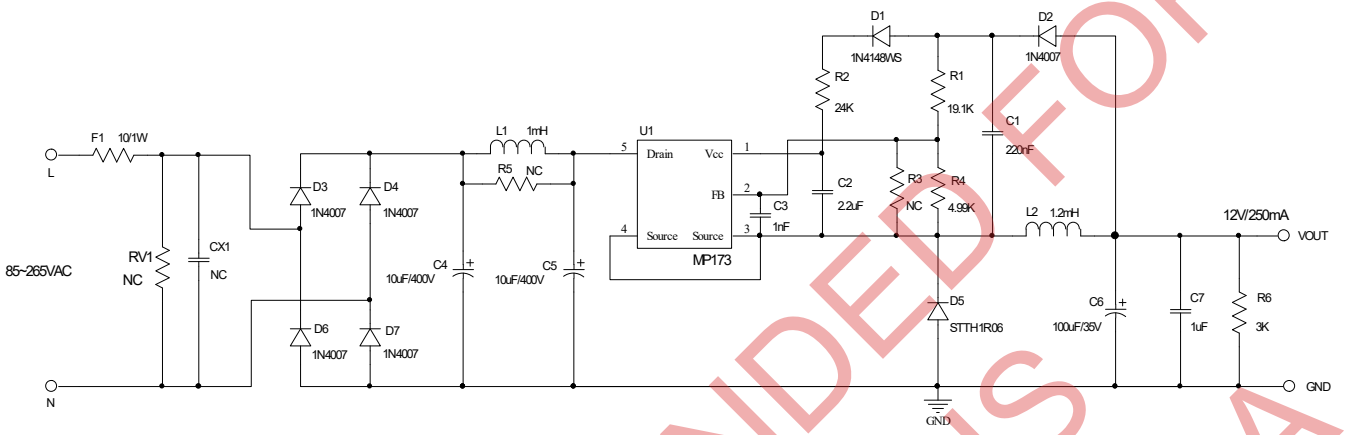
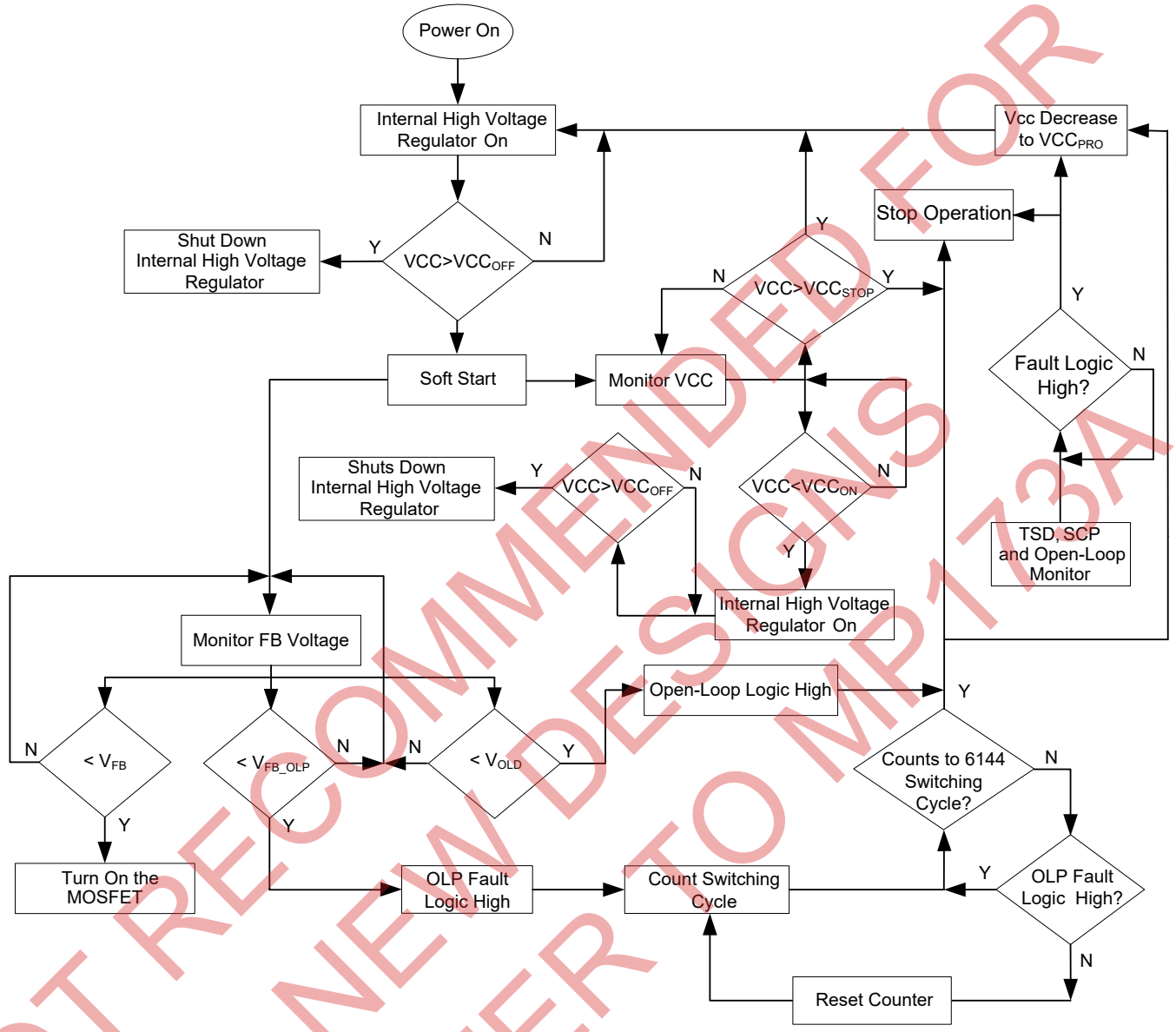


Figure 9—Typical application at 12 V, 250 mA

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FLOW CHART



UVLO, SCP, OLP, OTP and Open-Loop Protections are Auto Restart

Figure 10—Control flow chart

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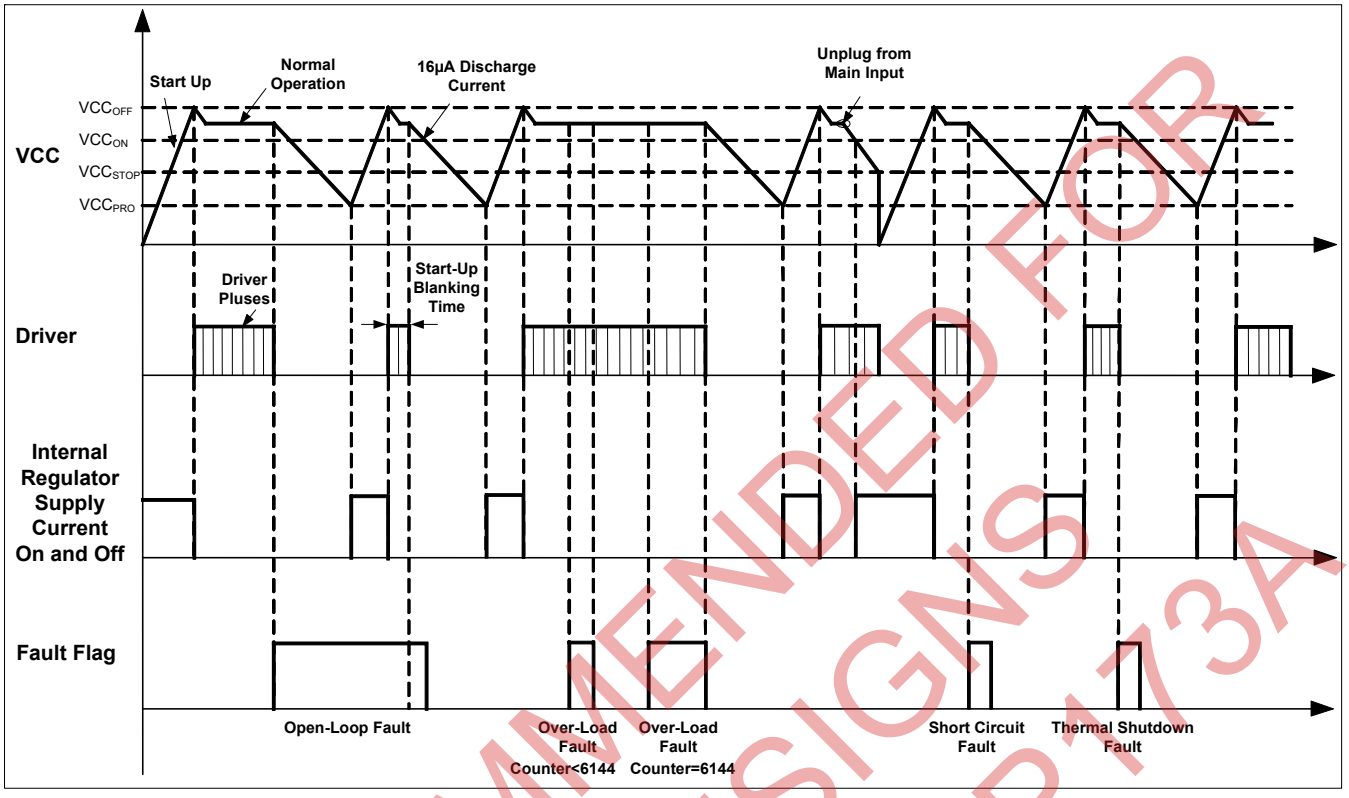


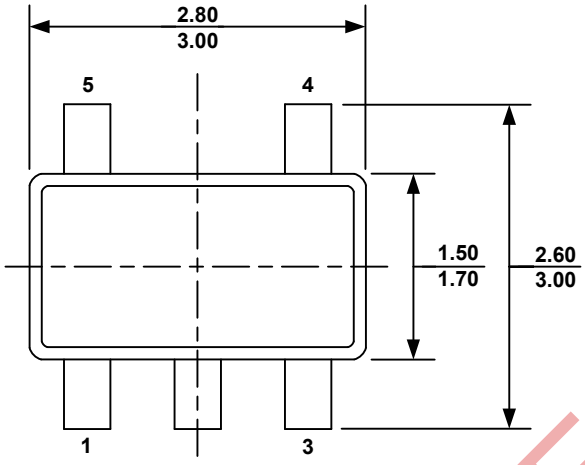
Figure 11—Signal evolution in the presence of a fault

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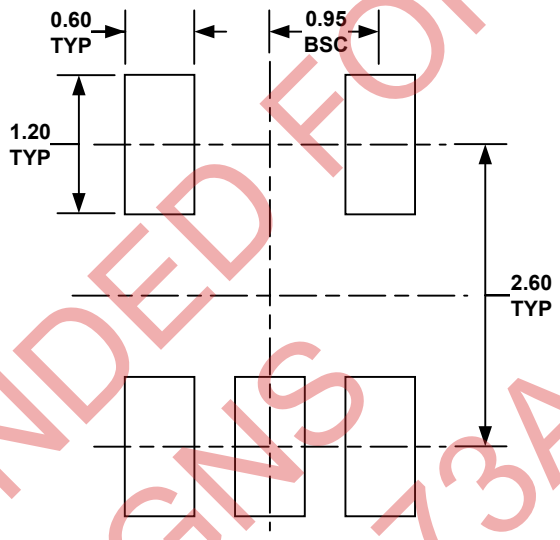
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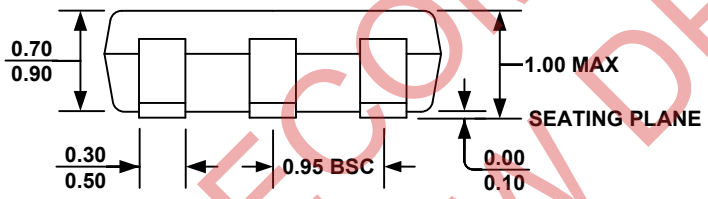
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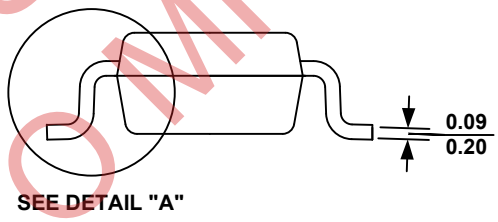
TOP VIEW



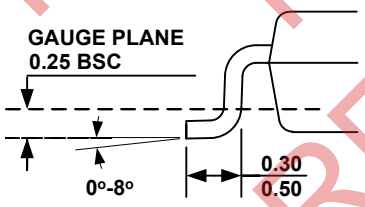
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FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

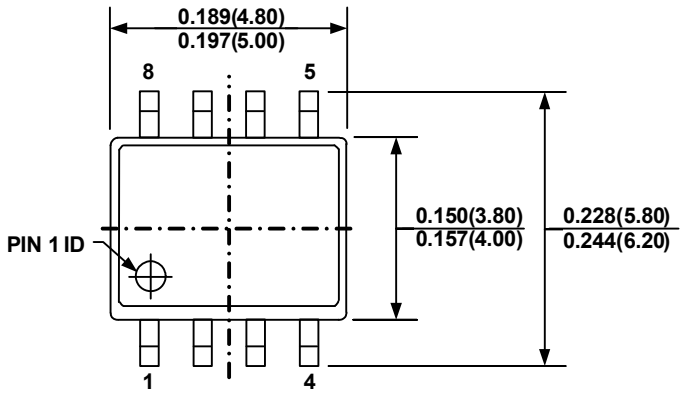
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3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
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6) DRAWING IS NOT TO SCALE.

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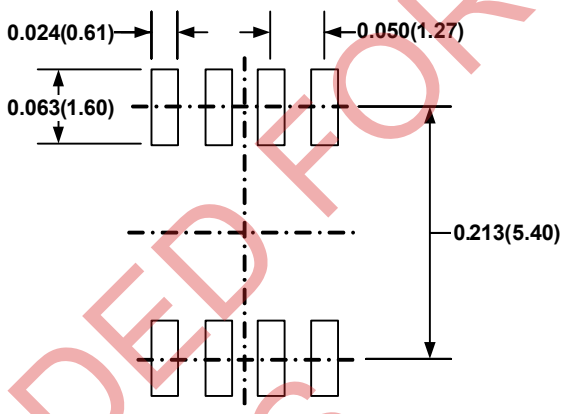
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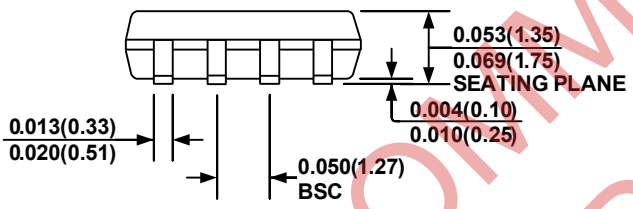
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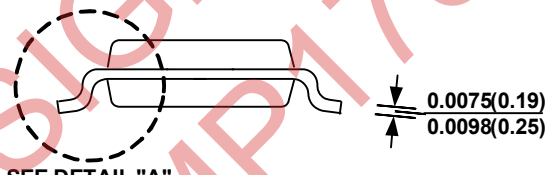
TOP VIEW



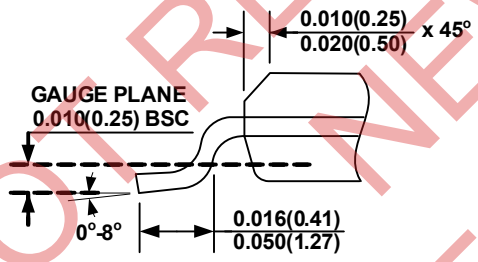
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

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2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS012, VARIATION AA.
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