Freescale Semiconductor
Data Sheet: Advance Information

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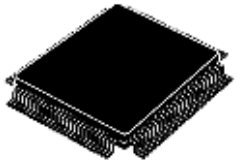
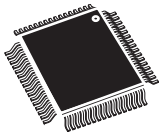
MPC5602P

MPC5602P Microcontroller Data Sheet



100 LQFP (14 mm x 14 mm)



64 LQFP (10 mm x 10 mm)

- Up to 64 MHz, single issue, 32-bit CPU core complex (e200z0h)
  - Compliant with Power Architecture embedded category
  - Variable Length Encoding (VLE)
- Memory organization
  - Up to 256 KB on-chip code flash memory with ECC and erase/program controller
  - Optional: additional 64 (4 × 16) KB on-chip data flash memory with ECC for EEPROM emulation
  - Up to 20 KB on-chip SRAM with ECC
- Fail-safe protection
  - Programmable watchdog timer
  - Non-maskable interrupt
  - Fault collection unit
- Nexus Class 1 interface
- Interrupts and events
  - 16-channel eDMA controller
  - 16 priority level controller
  - Up to 25 external interrupts
  - PIT implements four 32-bit timers
  - 120 interrupts are routed via INTC
- General purpose I/Os
  - Individually programmable as input, output or special function
  - 37 on 64 LQFP
  - 64 on 100 LQFP
- 1 general purpose eTimer unit
  - 6 timers each with up/down capabilities
  - 16-bit resolution, cascadeable counters
  - Quadrature decode with rotation direction flag
  - Double buffer input capture and output compare
- Communications interfaces
  - Up to 2 LINFlex modules (1× Master/Slave, 1× Master only)
  - Up to 3 DSPI channels with automatic chip select generation (up to 8/4/4 chip selects)
  - 1 FlexCAN interface (2.0B Active) with 32 message buffers
  - 1 safety port based on FlexCAN with 32 message buffers and up to 8 Mbit/s at 64 MHz capabilitym usable as second CAN when not used as safety port
- One 10-bit analog-to-digital converter (ADC)
  - Up to 16 input channels (16 ch on 100 LQFP and 12 ch on 64 LQFP)
  - Conversion time < 1 µs including sampling time at full precision
  - Programmable Cross Triggering Unit (CTU)
  - 4 analog watchdogs with interrupt capability
- On-chip CAN/UART bootstrap loader with Boot Assist Module (BAM)
- 1 FlexPWM unit
  - 8 complementary or independent outputs with ADC synchronization signals
  - Polarity control, reload unit
  - Integrated configurable dead time unit and inverter fault input pins
  - 16-bit resolution
  - Lockable configuration
- Clock generation
  - 4–40 MHz main oscillator
  - 16 MHz internal RC oscillator
  - Software-controlled FMPLL capable of up to 64 MHz
- Voltage supply
  - 3.3 V or 5 V supply for I/Os and ADC
  - On-chip single supply voltage regulator with external ballast transistor
- Operating temperature ranges: –40 to 125 °C or –40 to 105 °C

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1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5601P/2P series of microcontroller units (MCUs). It also describes the device features and highlights important electrical and physical characteristics. For functional characteristics, refer to the device reference manual.

1.2 Description

This 32-bit system-on-chip (SoC) automotive microcontroller family is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address chassis applications—specifically, electrical hydraulic power steering (EHPS) and electric power steering (EPS)—as well as airbag applications.

This family is one of a series of next-generation integrated automotive microcontrollers based on the Power Architecture® technology.

The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

1.3 Device comparison

Table 1 provides a summary of different members of the MPC5602P family and their features to enable a comparison among the family members and an understanding of the range of functionality offered within this family.

Table 1. MPC5602P device comparison

Feature	MPC5601P	MPC5602P
Code flash memory (with ECC)	192 KB	256 KB
Data flash memory / EE option (with ECC)	64 KB (optional feature)	
SRAM (with ECC)	12 KB	20 KB
Processor core	32-bit e200z0h	
Instruction set	VLE (variable length encoding)	
CPU performance	0–64 MHz	
FMPLL (frequency-modulated phase-locked loop) module	1	
INTC (interrupt controller) channels	120	
PIT (periodic interrupt timer)	1 (with four 32-bit timers)	
eDMA (enhanced direct memory access) channels	16	
FlexCAN (controller area network)	1[1,2]	2[1,2]
Safety port	Yes (via FlexCAN module)	Yes (via second FlexCAN module)
FCU (fault collection unit)	Yes	
CTU (cross triggering unit)	No	Yes
eTimer	1 (16-bit, 6 channels)	

Table 1. MPC5602P device comparison (continued)

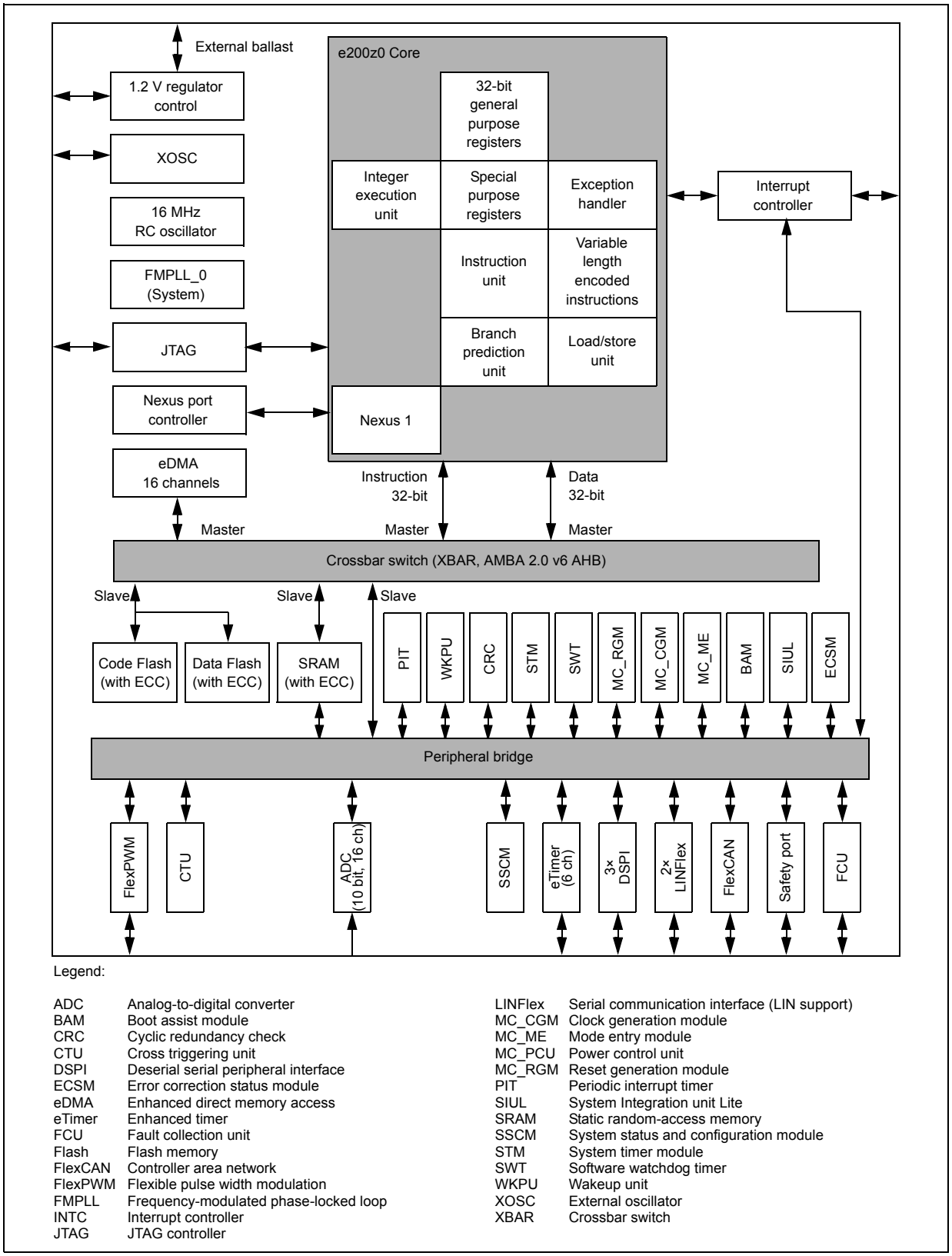
Feature		MPC5601P	MPC5602P
FlexPWM (pulse-width modulation) channels		No	8 (capture capability not supported)
Analog-to-digital converter (ADC)		1 (10-bit, 16 channels)	
LINFlex		1 (1 × Master/Slave)	2 (1 × Master/Slave, 1 × Master only)
DSPI (deserial serial peripheral interface)		1	3
CRC (cyclic redundancy check) unit		Yes	
Junction temperature sensor		No	
JTAG controller		Yes	
Nexus port controller (NPC)		Yes (Nexus Class 1)	
Supply	Digital power supply	3.3 V or 5 V single supply with external transistor	
	Analog power supply	3.3 V or 5 V	
	Internal RC oscillator	16 MHz	
	External crystal oscillator	4–40 MHz	
Packages		64 LQFP 100 LQFP	
Temperature	Standard ambient temperature	–40 to 125 °C	

1 Each FlexCAN module has 32 message buffers.

2 One FlexCAN module can act as a safety port with a bit rate as high as 8 Mbit/s at 64 MHz.

1.4 Block diagram

Figure 1 shows a top-level block diagram of the MPC5602P MCU. Table 1 summarizes the functions of the blocks.



Legend:

ADC	Analog-to-digital converter
BAM	Boot assist module
CRC	Cyclic redundancy check
CTU	Cross triggering unit
DSPI	Deserial serial peripheral interface
ECSM	Error correction status module
eDMA	Enhanced direct memory access
eTimer	Enhanced timer
FCU	Fault collection unit
Flash	Flash memory
FlexCAN	Controller area network
FlexPWM	Flexible pulse width modulation
FMPLL	Frequency-modulated phase-locked loop
INTC	Interrupt controller
JTAG	JTAG controller
LINFlex	Serial communication interface (LIN support)
MC_CGM	Clock generation module
MC_ME	Mode entry module
MC_PCU	Power control unit
MC_RGM	Reset generation module
PIT	Periodic interrupt timer
SIUL	System Integration unit Lite
SRAM	Static random-access memory
SSCM	System status and configuration module
STM	System timer module
SWT	Software watchdog timer
WKPU	Wakeup unit
XOSC	External oscillator
XBAR	Crossbar switch

Figure 1. MPC5602P block diagram

Table 2. MPC5602P series block summary

Block	Function
Analog-to-digital converter (ADC)	Multi-channel, 10-bit analog-to-digital converter
Boot assist module (BAM)	Block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Controller area network (FlexCAN)	Supports the standard CAN communications protocol
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Crossbar switch (XBAR)	Supports simultaneous connections between two master ports and three slave ports; supports a 32-bit address bus width and a 32-bit data bus width
Cyclic redundancy check (CRC)	CRC checksum generator
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced direct memory access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "*n*" programmable channels
Enhanced timer (eTimer)	Provides enhanced programmable up/down modulo counting
Error correction status module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
External oscillator (XOSC)	Provides an output clock used as input reference for FMPLL_0 or as reference clock for specific modules depending on system needs
Fault collection unit (FCU)	Provides functional safety to the device
Flash memory	Provides non-volatile storage for program code, constants and variables
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Peripheral bridge (PBRIDGE)	Is the interface between the system bus and on-chip peripherals
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called "power domains" which are controlled by the PCU

Table 2. MPC5602P series block summary (continued)

Block	Function
Pulse width modulator (FlexPWM)	Contains four PWM submodules, each of which capable of controlling a single half-bridge power stage and two fault input channels
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR[1] and operating system tasks
System watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	Supports up to 18 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events

[1] AUTOSAR: AUTomotive Open System ARchitecture (see http://www.autosar.org)

1.5 Feature details

1.5.1 High performance e200z0 core processor

The e200z0 Power Architecture core provides the following features:

- High performance e200z0 core processor for managing peripherals and interrupts
- Single issue 4-stage pipeline in-order execution 32-bit Power Architecture CPU
- Harvard architecture
- Variable length encoding (VLE), allowing mixed 16- and 32-bit instructions
  - Results in smaller code size footprint
  - Minimizes impact on performance
- Branch processing acceleration using lookahead instruction buffer
- Load/store unit
  - 1-cycle load latency
  - Misaligned access support
  - No load-to-use pipeline bubbles
- Thirty-two 32-bit general purpose registers (GPRs)
- Separate instruction bus and load/store bus Harvard architecture
- Hardware vectored interrupt support
- Reservation instructions for implementing read-modify-write constructs
- Long cycle time instructions, except for guarded loads, do not increase interrupt latency
- Extensive system development support through Nexus debug port
- Non-maskable interrupt support

1.5.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between three master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.

The crossbar allows for two concurrent transactions to occur from any master port to any slave port; but one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic will select the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port will be stalled until the higher priority master completes its transactions. Requesting masters will be treated with equal priority and will be granted access a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

The crossbar provides the following features:

- 3 master ports:
  - e200z0 core complex instruction port
  - e200z0 core complex Load/Store Data port
  - eDMA
- 3 slave ports:
  - Flash memory (Code and Data)
  - SRAM
  - Peripheral bridge
- 32-bit internal address, 32-bit internal data paths
- Fixed Priority Arbitration based on Port Master
- Temporary dynamic priority elevation of masters

1.5.3 Enhanced direct memory access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels.

The eDMA module provides the following features:

- 16 channels support independent 8-, 16- or 32-bit single value or block transfers
- Supports variable-sized queues and circular queues
- Source and destination address registers are independently configured to either post-increment or to remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- DMA transfers possible between system memories, DSPIs, ADC, FlexPWM, eTimer and CTU
- Programmable DMA channel multiplexer allows assignment of any DMA source to any available DMA channel with as many as 30 request sources
- eDMA abort operation through software

1.5.4 Flash memory

The MPC5602P provides 320 KB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used for instruction and/or data storage. The flash memory module is interfaced to the system bus by a dedicated flash memory controller. It supports a 32-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains four 128-bit wide prefetch buffers. Prefetch buffer hits allow no-wait responses. Normal flash memory array accesses are registered and are forwarded to the system bus on the following cycle, incurring two wait-states.

The flash memory module provides the following features:

- As much as 320 KB flash memory
  - 6 blocks (32 KB + 2×16 KB + 32 KB + 32 KB + 128 KB) code flash memory
  - 4 blocks (16 KB + 16 KB + 16 KB + 16 KB) data flash memory
  - Full Read-While-Write (RWW) capability between code flash memory and data flash memory
- Four 128-bit wide prefetch buffers to provide single cycle in-line accesses (prefetch buffers can be configured to prefetch code or data or both)
- Typical flash memory access time: no wait-state for buffer hits, 2 wait-states for page buffer miss at 64 MHz
- Hardware managed flash memory writes handled by 32-bit RISC Krypton engine
- Hardware and software configurable read and write access protections on a per-master basis
- Configurable access timing allowing use in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (up to 31 additional cycles) allowing use for emulation of other memory types
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page sizes
  - Code flash memory: 128 bits (4 words)
  - Data flash memory: 32 bits (1 word)
- ECC with single-bit correction, double-bit detection for data integrity
  - Code flash memory: 64-bit ECC
  - Data flash memory: 32-bit ECC
- Embedded hardware program and erase algorithm
- Erase suspend and program abort
- Censorship protection scheme to prevent flash memory content visibility
- Hardware support for EEPROM emulation

1.5.5 Static random access memory (SRAM)

The MPC5602P SRAM module provides up to 20 KB of general-purpose memory.

ECC handling is done on a 32-bit boundary and is completely software compatible with MPC55xx family devices containing an e200z6 core and 64-bit wide ECC.

The SRAM module provides the following features:

- Supports read/write accesses mapped to the SRAM from any master
- Up to 20 KB general purpose SRAM
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory
- Typical SRAM access time: no wait-state for reads and 32-bit writes; 1 wait-state for 8- and 16-bit writes if back-to-back with a read to same memory block

1.5.6 Interrupt controller (INTC)

The interrupt controller (INTC) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems. The INTC handles 128 selectable-priority interrupt sources.

For high-priority interrupt requests, the time from the assertion of the interrupt request by the peripheral to the execution of the interrupt service routine (ISR) by the processor has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR has to be executed. It also provides a wide number of priorities so that

lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol (PCP) for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the same resource can not preempt each other.

The INTC provides the following features:

- Unique 9-bit vector for each separate interrupt source
- 8 software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority: modifying the priority can be used to implement the priority ceiling protocol for accessing shared resources.
- 1 external high priority interrupt (NMI) directly accessing the main core and I/O processor (IOP) critical interrupt mechanism

1.5.7 System status and configuration module (SSCM)

The system status and configuration module (SSCM) provides central device functionality.

The SSCM includes these features:

- System configuration and status
  - Memory sizes/status
  - Device mode and security status
  - Determine boot vector
  - Search code flash for bootable sector
  - DMA status
- Debug status port enable and selection
- Bus and peripheral abort enable/disable

1.5.8 System clocks and clock generation

The following list summarizes the system clock and clock generation on the MPC5602P:

- Lock detect circuitry continuously monitors lock status
- Loss of clock (LOC) detection for PLL outputs
- Programmable output clock divider (÷1, ÷2, ÷4, ÷8)
- FlexPWM module and eTimer module running at the same frequency as the e200z0h core
- Internal 16 MHz RC oscillator for rapid start-up and safe mode: supports frequency trimming by user application

1.5.9 Frequency-modulated phase-locked loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4–40 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable.

The FMPLL has the following major features:

- Input clock frequency: 4–40 MHz
- Maximum output frequency: 64 MHz
- Voltage controlled oscillator (VCO)—frequency 256–512 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the FMPLL to relock

- Frequency-modulated PLL
  - Modulation enabled/disabled through software
  - Triangle wave modulation
- Programmable modulation depth (±0.25% to ±4% deviation from center frequency): programmable modulation frequency dependent on reference frequency
- Self-clocked mode (SCM) operation

1.5.10 Main oscillator

The main oscillator provides these features:

- Input frequency range: 4–40 MHz
- Crystal input mode or oscillator input mode
- PLL reference

1.5.11 Internal RC oscillator

This device has an RC ladder phase-shift oscillator. The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared by the stable bandgap reference voltage.

The RC oscillator provides these features:

- Nominal frequency 16 MHz
- ±5% variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the PLL
- RC oscillator is used as the default system clock during startup

1.5.12 Periodic interrupt timer (PIT)

The PIT module implements these features:

- 4 general-purpose interrupt timers
- 32-bit counter resolution
- Clocked by system clock frequency
- Each channel usable as trigger for a DMA request

1.5.13 System timer module (STM)

The STM implements these features:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.5.14 Software watchdog timer (SWT)

The SWT has the following features:

- 32-bit time-out register to set the time-out period
- Programmable selection of window mode or regular servicing

- Programmable selection of reset or interrupt on an initial time-out
- Master access protection
- Hard and soft configuration lock bits
- Reset configuration inputs allow timer to be enabled out of reset

1.5.15 Fault collection unit (FCU)

The FCU provides an independent fault reporting mechanism even if the CPU is malfunctioning.

The FCU module has the following features:

- FCU status register reporting the device status
- Continuous monitoring of critical fault signals
- User selection of critical signals from different fault sources inside the device
- Critical fault events trigger 2 external pins (user selected signal protocol) that can be used externally to reset the device and/or other circuitry (for example, a safety relay)
- Faults are latched into a register

1.5.16 System integration unit – Lite (SIUL)

The MPC5602P SIUL controls MCU pad configuration, external interrupt, general purpose I/O (GPIO), and internal peripheral multiplexing.

The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

The SIUL provides the following features:

- Centralized general purpose input output (GPIO) control of up to 49 input/output pins and 16 analog input-only pads (package dependent)
- All GPIO pins can be independently configured to support pull-up, pull-down, or no pull
- Reading and writing to GPIO supported both as individual pins and 16-bit wide ports
- All peripheral pins, except ADC channels, can be alternatively configured as both general purpose input or output pins
- ADC channels support alternative configuration as general purpose inputs
- Direct readback of the pin value is supported on all pins through the SIUL
- Configurable digital input filter that can be applied to some general purpose input pins for noise elimination
- Up to 4 internal functions can be multiplexed onto 1 pin

1.5.17 Boot and censorship

Different booting modes are available in the MPC5602P: booting from internal flash memory and booting via a serial link.

The default booting scheme uses the internal flash memory (an internal pull-down resistor is used to select this mode). Optionally, the user can boot via FlexCAN or LINFlex (using the boot assist module software).

A censorship scheme is provided to protect the content of the flash memory and offer increased security for the entire device.

A password mechanism is designed to grant the legitimate user access to the non-volatile memory.

1.5.17.1 Boot assist module (BAM)

The BAM is a block of read-only memory that is programmed once and is identical for all MPC560xP devices that are based on the e200z0h core. The BAM program is executed every time the device is powered on if the alternate boot mode has been selected by the user.

The BAM provides the following features:

- Serial bootloading via FlexCAN or LINFlex
- Ability to accept a password via the used serial communication channel to grant the legitimate user access to the non-volatile memory

1.5.18 Error correction status module (ECSM)

The ECSM provides a myriad of miscellaneous control functions regarding program-visible information about the platform configuration and revision levels, a reset status register, a software watchdog timer, wakeup control for exiting sleep modes, and information on platform memory errors reported by error-correcting codes and/or generic access error information for certain processor cores.

The Error Correction Status Module supports a number of miscellaneous control functions for the platform. The ECSM includes these features:

- Registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
- For test purposes, optional registers to specify the generation of double-bit memory errors are enabled on the MPC5602P.

The sources of the ECC errors are:

- Flash memory
- SRAM

1.5.19 Peripheral bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access privilege level per peripheral (per master: read access enable; write access enable)
- Write buffering for peripherals
- Checker applied on PBRIDGE output toward periphery
- Byte endianess swap capability

1.5.20 Controller area network (FlexCAN)

The MPC5602P MCU contains one controller area network (FlexCAN) module. This module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module contains 32 message buffers.

The FlexCAN module provides the following features:

- Full implementation of the CAN protocol specification, version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - Up to 8-bytes data length
  - Programmable bit rate up to 1 Mbit/s
- 32 message buffers of up to 8-bytes data length
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- 3 programmable mask registers

- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Transmit features
  - Supports configuration of multiple mailboxes to form message queues of scalable depth
  - Arbitration scheme according to message ID or message buffer number
  - Internal arbitration to guarantee no inner or outer priority inversion
  - Transmit abort procedure and notification
- Receive features
  - Individual programmable filters for each mailbox
  - 8 mailboxes configurable as a 6-entry receive FIFO
  - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
  - System clock
  - Direct oscillator clock to avoid PLL jitter

1.5.21 Safety port (FlexCAN)

The MPC5602P MCU has a second CAN controller synthesized to run at high bit rates to be used as a safety port. The CAN module of the safety port provides the following features:

- Identical to the FlexCAN module
- Bit rate up to 8 Mbit/s at 64 MHz CPU clock using direct connection between CAN modules (no physical transceiver required)
- 32 message buffers of up to 8-bytes data length
- Can be used as a second independent CAN module

1.5.22 Serial communication interface module (LINFlex)

The LINFlex (local interconnect network flexible) on the MPC5602P features the following:

- Supports LIN Master mode (both instances), LIN Slave mode (only one instance) and UART mode
- LIN state machine compliant to LIN1.3, 2.0 and 2.1 specifications
- Handles LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store Identifier and up to 8 data bytes
  - Supports message length of up to 64 bytes
  - Detection and flagging of LIN errors (sync field, delimiter, ID parity, bit framing, checksum, and time-out)
  - Classic or extended checksum calculation
  - Configurable Break duration of up to 36-bit times
  - Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features: Loop back; Self Test; LIN bus stuck dominant detection
  - Interrupt-driven operation with 16 interrupt sources

- LIN slave mode features:
  - Autonomous LIN header handling
  - Autonomous LIN response handling
  - Optional discarding of irrelevant LIN responses using ID filter
- UART mode:
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit or 9-bit words)
  - Error detection and flagging
  - Parity, Noise and Framing errors
  - Interrupt-driven operation with four interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - 2 receiver wake-up methods

1.5.23 Deserial serial peripheral interface (DSPI)

The deserial serial peripheral interface (DSPI) module provides a synchronous serial interface for communication between the MPC5602P MCU and external devices.

The DSPI modules provide these features:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- Up to 8 chip select lines available:
  - 8 on DSPI_0
  - 4 each on DSPI_1 and DSPI_2
- 8 clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for deglitching
- FIFOs for buffering up to 4 transfers on the transmit and receive side
- Queueing operation possible through use of the I/O processor or eDMA
- General purpose I/O functionality on pins when not used for SPI

1.5.24 Pulse width modulator (FlexPWM)

The pulse width modulator module (PWM) contains four PWM submodules each of which is set up to control a single half-bridge power stage. There are also three fault channels.

This PWM is capable of controlling most motor types: AC induction motors (ACIM), permanent magnet AC motors (PMAC), both brushless (BLDC) and brush DC motors (BDC), switched (SRM) and variable reluctance motors (VRM), and stepper motors.

The FlexPWM block implements the following features:

- 16-bit resolution for center, edge-aligned, and asymmetrical PWMs

- Clock frequency same as that used for e200z0h core
- PWM outputs can operate as complementary pairs or independent channels
- Can accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM supported
- Double buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Write protection for critical registers
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software-control for each PWM output
- All outputs can be programmed to change simultaneously via a “Force Out” event
- PWMX pin can optionally output a third PWM signal from each submodule
- Channels not used for PWM generation can be used for buffered output compare functions
- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual-edge capture functionality
- eDMA support with automatic reload
- 2 fault inputs
- Capture capability for PWMA, PWMB, and PWMX channels not supported

1.5.25 eTimer

The MPC5602P includes one eTimer module which provides six 16-bit general purpose up/down timer/counter units with the following features:

- Clock frequency same as that used for the e200z0h core
- Individual channel capability
  - Input capture trigger
  - Output compare
  - Double buffer (to capture rising edge and falling edge)
  - Separate prescaler for each counter
  - Selectable clock source
  - 0–100% pulse measurement
  - Rotation direction flag (quad decoder mode)
- Maximum count rate
  - External event counting: max. count rate = peripheral clock/2
  - Internal clock counting: max. count rate = peripheral clock
- Counters are:
  - Cascadable
  - Preloadable
- Programmable count modulo
- Quadrature decode capabilities

- Counters can share available input pins
- Count once or repeatedly
- Pins available as GPIO when timer functionality not in use

1.5.26 Analog-to-digital converter (ADC) module

The ADC module provides the following features:

Analog part:

- 1 on-chip analog-to-digital converter
  - 10-bit AD resolution
  - 1 sample and hold unit
  - Conversion time, including sampling time, less than 1 µs (at full precision)
  - Typical sampling time is 150 ns minimum (at full precision)
  - DNL/INL ±1 LSB
  - TUE < 1.5 LSB
  - Single-ended input signal up to 3.3 V/5.0 V
  - 3.3 V/5.0 V input reference voltage
  - ADC and its reference can be supplied with a voltage independent from V_{DDIO}
  - ADC supply can be equal or higher than V_{DDIO}
  - ADC supply and ADC reference are not independent from each other (both internally bonded to same pad)
  - Sample times of 2 (default), 8, 64 or 128 ADC clock cycles

Digital part:

- 16 input channels
- 4 analog watchdogs comparing ADC results against predefined levels (low, high, range) before results are stored in the appropriate ADC result location
- 2 modes of operation: Motor Control mode or Regular mode
- Regular mode features
  - Register based interface with the CPU: control register, status register and 1 result register per channel
  - ADC state machine managing 3 request flows: regular command, hardware injected command and software injected command
  - Selectable priority between software and hardware injected commands
  - DMA compatible interface
- CTU-controlled mode features
  - Triggered mode only
  - 4 independent result queues (1×16 entries, 2×8 entries, 1×4 entries)
  - Result alignment circuitry (left justified and right justified)
  - 32-bit read mode allows to have channel ID on one of the 16-bit part
  - DMA compatible interfaces

1.5.27 Cross triggering unit (CTU)

The cross triggering unit allows automatic generation of ADC conversion requests on user selected conditions without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

It implements the following features:

- Double buffered trigger generation unit with up to 8 independent triggers generated from external triggers

- Trigger generation unit configurable in sequential mode or in triggered mode
- Each trigger can be appropriately delayed to compensate the delay of external low pass filter
- Double buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double buffered ADC command list pointers to minimize ADC-trigger unit update
- Double buffered ADC conversion command list with up to 24 ADC commands
- Each trigger capable of generating consecutive commands
- ADC conversion command allows to control ADC channel, single or synchronous sampling, independent result queue selection

1.5.28 Nexus Development Interface (NDI)

The NDI (Nexus Development Interface) block is compliant with Nexus Class 1 of the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NDI block is an integration of several individual Nexus blocks that are selected to provide the development support interface for this device. The NDI block interfaces to the host processor and internal busses to provide development support as per the IEEE-ISTO 5001-2003 Nexus Class 1 standard. The development support provided includes access to the MCU's internal memory map and access to the processor's internal registers.

The NDI provides the following features:

- Configured via the IEEE 1149.1
- All Nexus port pins operate at V_{DDIO} (no dedicated power supply)
- Nexus Class 1 supports Static debug

1.5.29 Cyclic redundancy check (CRC)

The CRC computing unit is dedicated to the computation of CRC off-loading the CPU. The CRC module features:

- Support for CRC-16-CCITT ($x25$ protocol):
  - $x^{16} + x^{12} + x^5 + 1$
- Support for CRC-32 (Ethernet protocol):
  - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Zero wait states for each write/read operations to the CRC_CFG and CRC_INP registers at the maximum frequency

1.5.30 IEEE 1149.1 JTAG controller

The JTAG controller (JTAGC) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE standard.

The JTAG controller provides the following features:

- IEEE test access port (TAP) interface 4 pins (TDI, TMS, TCK, TDO)
- Selectable modes of operation include JTAGC/debug or normal system operation.
- 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS
  - IDCODE
  - EXTEST
  - SAMPLE
  - SAMPLE/PRELOAD
- 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC

— ACCESS_AUX_TAP_ONCE

- 3 test data registers:
  - — Bypass register
  - — Boundary scan register (size parameterized to support a variety of boundary scan chain lengths)
  - — Device identification register
- TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry

1.5.31 On-chip voltage regulator (VREG)

The on-chip voltage regulator module provides the following features:

- Uses external NPN (negative-positive-negative) transistor
- Regulates external 3.3 V/5.0 V down to 1.2 V for the core logic
- Low voltage detection on the internal 1.2 V and I/O voltage 3.3 V

2 Package pinouts and signal descriptions

2.1 Package pinouts

The LQFP pinouts are shown in the following figures. For pin signal descriptions, please refer to Table 5.

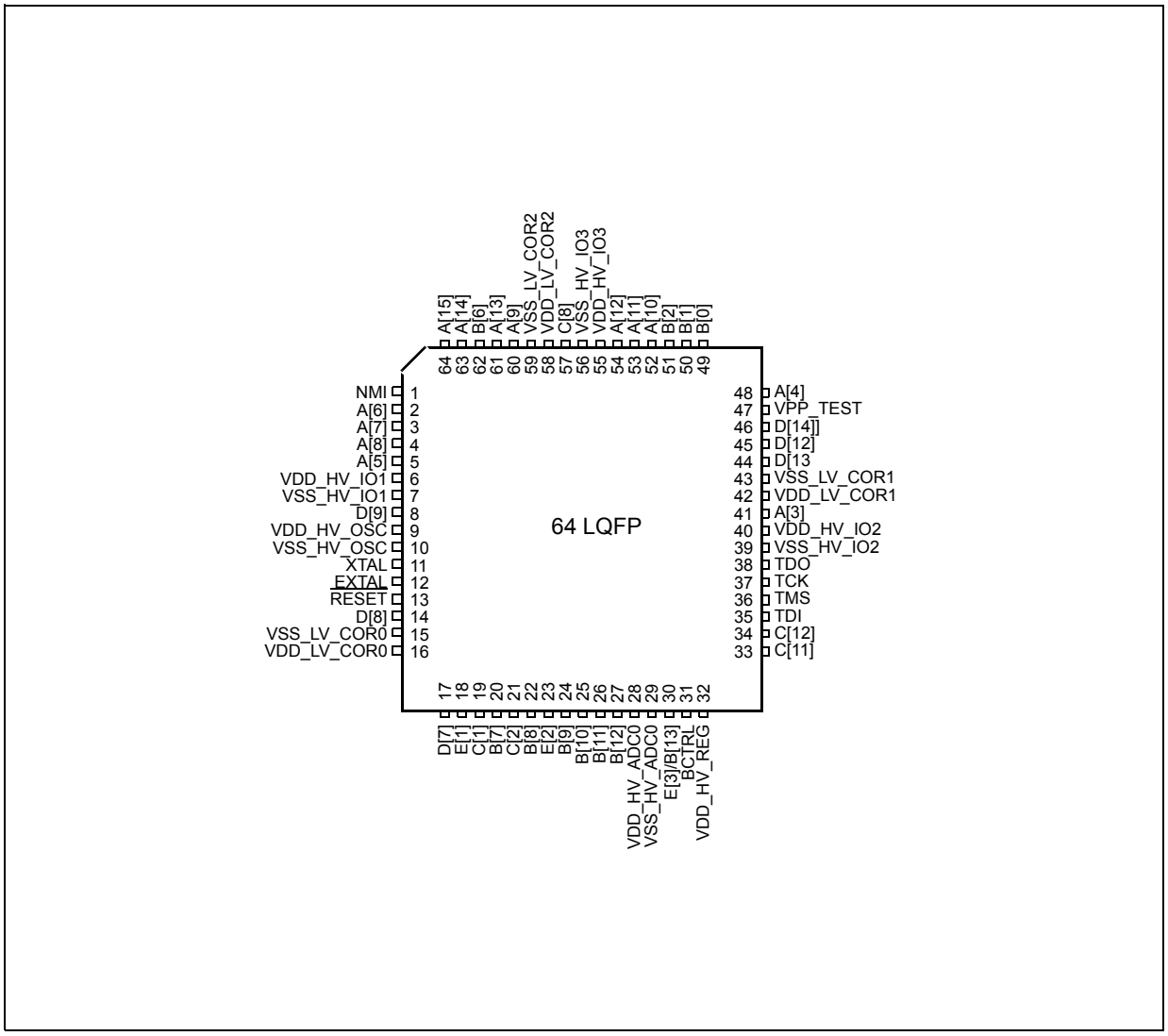


Figure 2. 64-pin LQFP pinout(top view)

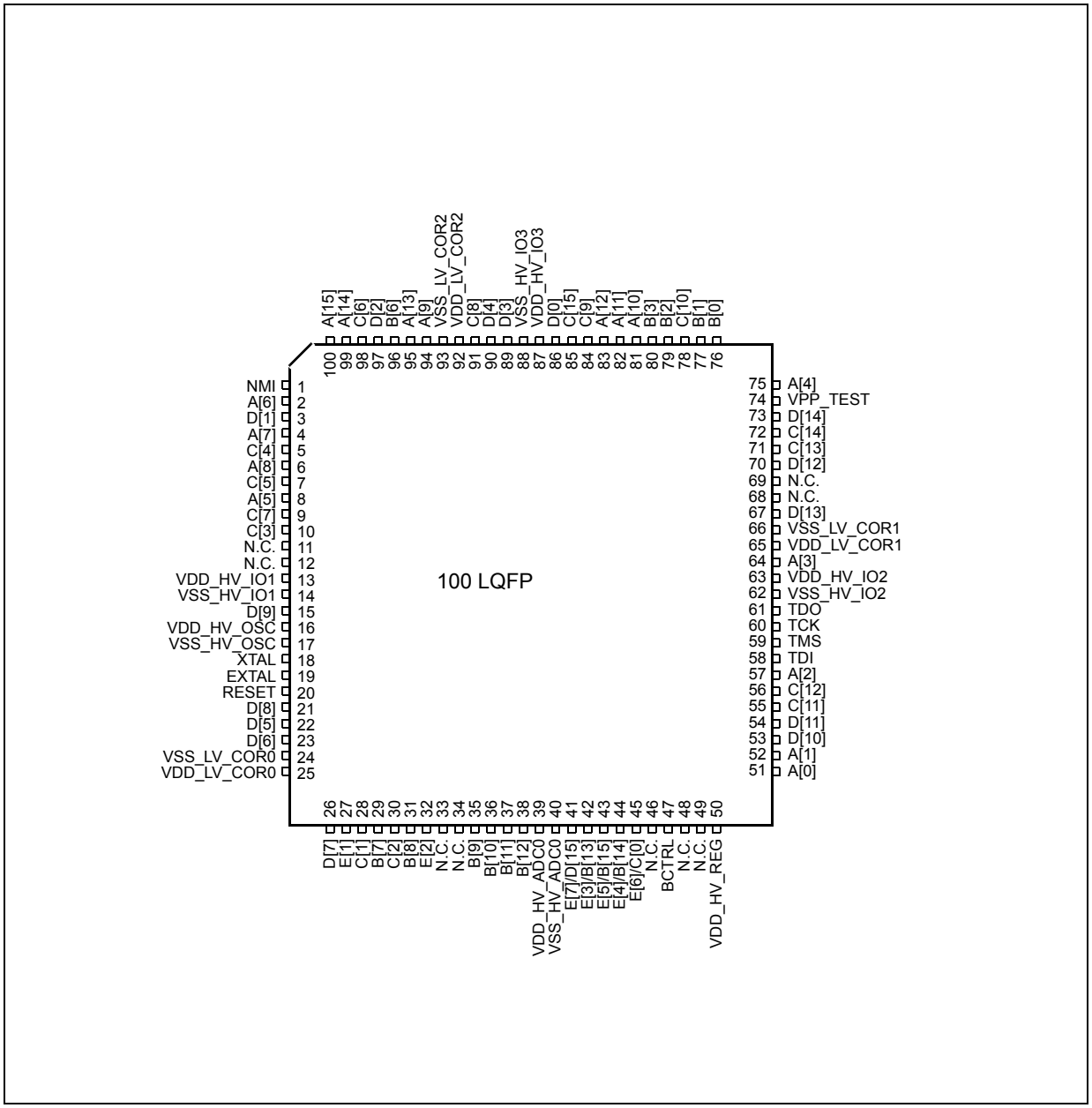


Figure 3. 100-pin LQFP pinout (top view)

2.2 Pin description

The following sections provide signal descriptions and related information about the functionality and configuration of the MPC5602P devices.

2.2.1 Power supply and reference voltage pins

Table 3 lists the power supply and reference voltage for the MPC5602P devices.

Table 3. Supply pins

Supply		Pin	
Symbol	**Description**	**64-pin**	**100-pin**
VREG control and power supply pins. Pins available on 64-pin and 100-pin packages			
BCTRL	Voltage regulator external NPN ballast base control pin	31	47
$V_{DD_HV_REG}$ (3.3 V or 5.0 V)	Voltage regulator supply voltage	32	50
ADC_0 reference and supply voltage. Pins available on 64-pin and 100-pin packages			
$V_{DD_HV_ADC0}$[1]	ADC_0 supply and high reference voltage	28	39
$V_{SS_HV_ADC0}$	ADC_0 ground and low reference voltage	29	40
Power supply pins (3.3 V or 5.0 V). Pins available on 64-pin and 100-pin packages			
$V_{DD_HV_IO1}$	Input/output supply voltage	6	13
$V_{SS_HV_IO1}$	Input/output ground	7	14
$V_{DD_HV_IO2}$	Input/output supply voltage and data Flash memory supply voltage	40	63
$V_{SS_HV_IO2}$	Input/output ground and Flash memory HV ground	39	62
$V_{DD_HV_IO3}$	Input/output supply voltage and code Flash memory supply voltage	55	87
$V_{SS_HV_IO3}$	Input/output ground and code Flash memory HV ground	56	88
$V_{DD_HV_OSC}$	Crystal oscillator amplifier supply voltage	9	16
$V_{SS_HV_OSC}$	Crystal oscillator amplifier ground	10	17
Power supply pins (1.2 V). Pins available on 64-pin and 100-pin packages			
$V_{DD_LV_COR0}$	1.2 V supply pins for core logic and PLL. Decoupling capacitor must be connected between these pins and the nearest $V_{SS_LV_COR}$ pin.	16	25
$V_{SS_LV_COR0}$	1.2 V supply pins for core logic and PLL. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV_COR}$ pin.	15	24
$V_{DD_LV_COR1}$	1.2 V supply pins for core logic and data Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{SS_LV_COR}$ pin.	42	65
$V_{SS_LV_COR1}$	1.2 V supply pins for core logic and data Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV_COR}$ pin.	43	66
$V_{DD_LV_COR2}$	1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{SS_LV_COR}$ pin.	58	92
$V_{SS_LV_COR2}$	1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected betwee.n these pins and the nearest $V_{DD_LV_COR}$ pin.	59	93

[1] Analog supply/ground and high/low reference lines are internally physically separate, but are shorted via a double-bonding connection on $V_{DD_HV_ADCx}$/$V_{SS_HV_ADCx}$ pins.

2.2.2 System pins

Table 4 and Table 5 contain information on pin functions for the MPC5602P devices. The pins listed in Table 4 are single-function pins. The pins shown in Table 5 are multi-function pins, programmable via their respective pad configuration register (PCR) values.

Table 4. System pins

Symbol	Description	Direction	Pad speed[1]		Pin	
			SRC = 0	SRC = 1	64-pin	100-pin
Dedicated pins						
NMI	Non-maskable Interrupt	Input only	Slow	—	1	1
XTAL	Analog output of the oscillator amplifier circuit—needs to be grounded if oscillator is used in bypass mode	—	—	—	11	18
EXTAL	Analog input of the oscillator amplifier circuit, when the oscillator is not in bypass mode Analog input for the clock generator when the oscillator is in bypass mode	—	—	—	12	19
TDI	JTAG test data input	Input only	Slow	—	35	58
TMS	JTAG state machine control	Input only	Slow	—	36	59
TCK	JTAG clock	Input only	Slow	—	37	60
TDO	JTAG test data output	Output only	Slow	Fast	38	61
Reset pin						
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt trigger characteristics and noise filter	Bidirectional	Medium	—	13	20
Test pin						
VPP_TEST	Pin for testing purpose only. To be tied to ground in normal operating mode.	—	—	—	47	74

[1] SRC values refer to the value assigned to the Slew Rate Control bits of the pad configuration register.

2.2.3 Pin multiplexing

Table 5 defines the pin list and muxing for the MPC5602P devices.

Each row of Table 5 shows all the possible ways of configuring each pin, via alternate functions. The default function assigned to each pin after reset is the ALT0 function.

MPC5602P devices provide three main I/O pad types, depending on the associated functions:

- *Slow pads* are the most common, providing a compromise between transition time and low electromagnetic emission.
- *Medium pads* provide fast enough transition for serial communication channels with controlled current to reduce electromagnetic emission.
- *Fast pads* provide maximum speed. They are used for improved NEXUS debugging capability.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance. For more information, see “Pad AC Specifications” in the device data sheet.

Table 5. Pin muxing

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
Port A (16-bit)									
A[0]	PCR[0]	ALT0 ALT1 ALT2 ALT3 —	GPIO[0] ETC[0] SCK F[0] EIRQ[0]	SIUL eTimer_0 DSPI_2 FCU_0 SIUL	I/O I/O I/O O I	Slow	Medium	—	51
A[1]	PCR[1]	ALT0 ALT1 ALT2 ALT3 —	GPIO[1] ETC[1] SOUT F[1] EIRQ[1]	SIUL eTimer_0 DSPI_2 FCU_0 SIUL	I/O I/O O O I	Slow	Medium	—	52
A[2]	PCR[2]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[2] ETC[2] — A[3] SIN ABS[0] EIRQ[2]	SIUL eTimer_0 — FlexPWM_0 DSPI_2 MC_RGM SIUL	I/O I/O — O I I I	Slow	Medium	—	57
A[3]	PCR[3]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[3] ETC[3] CS0 B[3] ABS[1] EIRQ[3]	SIUL eTimer_0 DSPI_2 FlexPWM_0 MC_RGM SIUL	I/O I/O I/O O I I	Slow	Medium	41	64
A[4]	PCR[4]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[4] — CS1 ETC[4] FAB EIRQ[4]	SIUL — DSPI_2 eTimer_0 MC_RGM SIUL	I/O — O I/O I I	Slow	Medium	48	75
A[5]	PCR[5]	ALT0 ALT1 ALT2 ALT3 —	GPIO[5] CS0 — CS7 EIRQ[5]	SIUL DSPI_1 — DSPI_0 SIUL	I/O I/O — O I	Slow	Medium	5	8
A[6]	PCR[6]	ALT0 ALT1 ALT2 ALT3 —	GPIO[6] SCK — — EIRQ[6]	SIUL DSPI_1 — — SIUL	I/O I/O — — I	Slow	Medium	2	2
A[7]	PCR[7]	ALT0 ALT1 ALT2 ALT3 —	GPIO[7] SOUT — — EIRQ[7]	SIUL DSPI_1 — — SIUL	I/O O — — I	Slow	Medium	3	4

Table 5. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
A[8]	PCR[8]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[8] — — — SIN EIRQ[8]	SIUL — — — DSPI_1 SIUL	I/O — — — I I	Slow	Medium	4	6
A[9]	PCR[9]	ALT0 ALT1 ALT2 ALT3 —	GPIO[9] CS1 — B[3] FAULT[0]	SIUL DSPI_2 — FlexPWM_0 FlexPWM_0	I/O O — O I	Slow	Medium	60	94
A[10]	PCR[10]	ALT0 ALT1 ALT2 ALT3 —	GPIO[10] CS0 B[0] X[2] EIRQ[9]	SIUL DSPI_2 FlexPWM_0 FlexPWM_0 SIUL	I/O I/O O O I	Slow	Medium	52	81
A[11]	PCR[11]	ALT0 ALT1 ALT2 ALT3 —	GPIO[11] SCK A[0] A[2] EIRQ[10]	SIUL DSPI_2 FlexPWM_0 FlexPWM_0 SIUL	I/O I/O O O I	Slow	Medium	53	82
A[12]	PCR[12]	ALT0 ALT1 ALT2 ALT3 —	GPIO[12] SOUT A[2] B[2] EIRQ[11]	SIUL DSPI_2 FlexPWM_0 FlexPWM_0 SIUL	I/O O O O I	Slow	Medium	54	83
A[13]	PCR[13]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[13] — B[2] — SIN FAULT[0] EIRQ[12]	SIUL — FlexPWM_0 — DSPI_2 FlexPWM_0 SIUL	I/O — O — I I I	Slow	Medium	61	95
A[14]	PCR[14]	ALT0 ALT1 ALT2 ALT3 —	GPIO[14] TXD — — EIRQ[13]	SIUL Safety Port_0 — — SIUL	I/O O — — I	Slow	Medium	63	99
A[15]	PCR[15]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[15] — — — RXD EIRQ[14]	SIUL — — — Safety Port_0 SIUL	I/O — — — I I	Slow	Medium	64	100

Table 5. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
Port B (16-bit)									
B[0]	PCR[16]	ALT0 ALT1 ALT2 ALT3 —	GPIO[16] TXD — DEBUG[0] EIRQ[15]	SIUL FlexCAN_0 — SSCM SIUL	I/O O — — I	Slow	Medium	49	76
B[1]	PCR[17]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[17] — — DEBUG[1] RXD EIRQ[16]	SIUL — — SSCM FlexCAN_0 SIUL	I/O — — — I I	Slow	Medium	50	77
B[2]	PCR[18]	ALT0 ALT1 ALT2 ALT3 —	GPIO[18] TXD — DEBUG[2] EIRQ[17]	SIUL LIN_0 — SSCM SIUL	I/O O — — I	Slow	Medium	51	79
B[3]	PCR[19]	ALT0 ALT1 ALT2 ALT3 —	GPIO[19] — — DEBUG[3] RXD	SIUL — — SSCM LIN_0	I/O — — — I	Slow	Medium	—	80
B[6]	PCR[22]	ALT0 ALT1 ALT2 ALT3 —	GPIO[22] CLKOUT CS2 — EIRQ[18]	SIUL Control DSPI_2 — SIUL	I/O O O — I	Slow	Medium	62	96
B[7]	PCR[23]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[23] — — — AN[0] RXD	SIUL — — — ADC_0 LIN_0	Input only	—	—	20	29
B[8]	PCR[24]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[24] — — — AN[1] ETC[5]	SIUL — — — ADC_0 eTimer_0	Input only	—	—	22	31
B[9]	PCR[25]	ALT0 ALT1 ALT2 ALT3 —	GPIO[25] — — — AN[11]	SIUL — — — ADC_0	Input only	—	—	24	35

Table 5. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
B[10]	PCR[26]	ALT0 ALT1 ALT2 ALT3 —	GPIO[26] — — — AN[12]	SIUL — — — ADC_0	Input only	—	—	25	36
B[11]	PCR[27]	ALT0 ALT1 ALT2 ALT3 —	GPIO[27] — — — AN[13]	SIUL — — — ADC_0	Input only	—	—	26	37
B[12]	PCR[28]	ALT0 ALT1 ALT2 ALT3 —	GPIO[28] — — — AN[14]	SIUL — — — ADC_0	Input only	—	—	27	38
B[13]	PCR[29]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[29] — — — AN[6] emu. AN[0] RXD	SIUL — — — ADC_0 emu. ADC_1[6] LIN_1	Input only	—	—	30	42
B[14]	PCR[30]	ALT0 ALT1 ALT2 ALT3 — — — —	GPIO[30] — — — AN[7] emu. AN[1] ETC[4] EIRQ[19]	SIUL — — — ADC_0 emu. ADC_1[6] eTimer_0 SIUL	Input only	—	—	—	44
B[15]	PCR[31]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[31] — — — AN[8] emu. AN[2] EIRQ[20]	SIUL — — — ADC_0 emu. ADC_1[6] SIUL	Input only	—	—	—	43
Port C (16-bit)									
C[0]	PCR[32]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[32] — — — AN[9] emu. AN[3]	SIUL — — — ADC_0 emu. ADC_1[6]	Input only	—	—	—	45

Table 5. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
C[1]	PCR[33]	ALT0 ALT1 ALT2 ALT3 —	GPIO[33] — — — AN[2]	SIUL — — — ADC_0	Input only	—	—	19	28
C[2]	PCR[34]	ALT0 ALT1 ALT2 ALT3 —	GPIO[34] — — — AN[3]	SIUL — — — ADC_0	Input only	—	—	21	30
C[3]	PCR[35]	ALT0 ALT1 ALT2 ALT3 —	GPIO[35] CS1 — TXD EIRQ[21]	SIUL DSPI_0 — LIN_1 SIUL	I/O O — O I	Slow	Medium	—	10
C[4]	PCR[36]	ALT0 ALT1 ALT2 ALT3 —	GPIO[36] CS0 X[1] DEBUG[4] EIRQ[22]	SIUL DSPI_0 FlexPWM_0 SSCM SIUL	I/O I/O O — I	Slow	Medium	—	5
C[5]	PCR[37]	ALT0 ALT1 ALT2 ALT3 —	GPIO[37] SCK — DEBUG[5] EIRQ[23]	SIUL DSPI_0 — SSCM SIUL	I/O I/O — — I	Slow	Medium	—	7
C[6]	PCR[38]	ALT0 ALT1 ALT2 ALT3 —	GPIO[38] SOUT B[1] DEBUG[6] EIRQ[24]	SIUL DSPI_0 FlexPWM_0 SSCM SIUL	I/O O O — I	Slow	Medium	—	98
C[7]	PCR[39]	ALT0 ALT1 ALT2 ALT3 —	GPIO[39] — A[1] DEBUG[7] SIN	SIUL — FlexPWM_0 SSCM DSPI_0	I/O — O — I	Slow	Medium	—	9
C[8]	PCR[40]	ALT0 ALT1 ALT2 ALT3	GPIO[40] CS1 — CS6	SIUL DSPI_1 — DSPI_0	I/O O — O	Slow	Medium	57	91
C[9]	PCR[41]	ALT0 ALT1 ALT2 ALT3	GPIO[41] CS3 — X[3]	SIUL DSPI_2 — FlexPWM_0	I/O O — O	Slow	Medium	—	84

Table 5. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
C[10]	PCR[42]	ALT0 ALT1 ALT2 ALT3 —	GPIO[42] CS2 — A[3] FAULT[1]	SIUL DSPI_2 — FlexPWM_0 FlexPWM_0	I/O O — O I	Slow	Medium	—	78
C[11]	PCR[43]	ALT0 ALT1 ALT2 ALT3	GPIO[43] ETC[4] CS2 —	SIUL eTimer_0 DSPI_2 —	I/O I/O O —	Slow	Medium	33	55
C[12]	PCR[44]	ALT0 ALT1 ALT2 ALT3	GPIO[44] ETC[5] CS3 —	SIUL eTimer_0 DSPI_2 —	I/O I/O O —	Slow	Medium	34	56
C[13]	PCR[45]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[45] — — — EXT_IN EXT_SYNC	SIUL — — — CTU_0 FlexPWM_0	I/O — — — I I	Slow	Medium	—	71
C[14]	PCR[46]	ALT0 ALT1 ALT2 ALT3	GPIO[46] — EXT_TGR —	SIUL — CTU_0 —	I/O — O —	Slow	Medium	—	72
C[15]	PCR[47]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[47] — — A[1] EXT_IN EXT_SYNC	SIUL — — FlexPWM_0 CTU_0 FlexPWM_0	I/O — — O I I	Slow	Medium	—	85
Port D (16-bit)									
D[0]	PCR[48]	ALT0 ALT1 ALT2 ALT3	GPIO[48] — — B[1]	SIUL — — FlexPWM_0	I/O — — O	Slow	Medium	—	86
D[1]	PCR[49]	ALT0 ALT1 ALT2 ALT3	GPIO[49] — — EXT_TRG	SIUL — — CTU_0	I/O — — O	Slow	Medium	—	3
D[2]	PCR[50]	ALT0 ALT1 ALT2 ALT3	GPIO[50] — — X[3]	SIUL — — FlexPWM_0	I/O — — O	Slow	Medium	—	97
D[3]	PCR[51]	ALT0 ALT1 ALT2 ALT3	GPIO[51] — — A[3]	SIUL — — FlexPWM_0	I/O — — O	Slow	Medium	—	89

Table 5. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
D[4]	PCR[52]	ALT0 ALT1 ALT2 ALT3	GPIO[52] — — B[3]	SIUL — — FlexPWM_0	I/O — — O	Slow	Medium	—	90
D[5]	PCR[53]	ALT0 ALT1 ALT2 ALT3	GPIO[53] CS3 F[0] —	SIUL DSPI_0 FCU_0 —	I/O O O —	Slow	Medium	—	22
D[6]	PCR[54]	ALT0 ALT1 ALT2 ALT3 —	GPIO[54] CS2 — — FAULT[1]	SIUL DSPI_0 — — FlexPWM_0	I/O O — — I	Slow	Medium	—	23
D[7]	PCR[55]	ALT0 ALT1 ALT2 ALT3	GPIO[55] CS3 F[1] CS4	SIUL DSPI_1 FCU_0 DSPI_0	I/O O O O	Slow	Medium	17	26
D[8]	PCR[56]	ALT0 ALT1 ALT2 ALT3	GPIO[56] CS2 — CS5	SIUL DSPI_1 — DSPI_0	I/O O — O	Slow	Medium	14	21
D[9]	PCR[57]	ALT0 ALT1 ALT2 ALT3	GPIO[57] X[0] TXD —	SIUL FlexPWM_0 LIN_1 —	I/O O O —	Slow	Medium	8	15
D[10]	PCR[58]	ALT0 ALT1 ALT2 ALT3	GPIO[58] A[0] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	—	53
D[11]	PCR[59]	ALT0 ALT1 ALT2 ALT3	GPIO[59] B[0] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	—	54
D[12]	PCR[60]	ALT0 ALT1 ALT2 ALT3 —	GPIO[60] X[1] — — RXD	SIUL FlexPWM_0 — — LIN_1	I/O O — — I	Slow	Medium	45	70
D[13]	PCR[61]	ALT0 ALT1 ALT2 ALT3	GPIO[61] A[1] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	44	67
D[14]	PCR[62]	ALT0 ALT1 ALT2 ALT3	GPIO[62] B[1] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	46	73

Table 5. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
D[15]	PCR[63]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[63] — — — AN[10] emu. AN[4]	SIUL — — — ADC_0 emu. ADC_1[6]	Input only	—	—	—	41
Port E (16-bit)									
E[1]	PCR[65]	ALT0 ALT1 ALT2 ALT3 —	GPIO[65] — — — AN[4]	SIUL — — — ADC_0	Input only	—	—	18	27
E[2]	PCR[66]	ALT0 ALT1 ALT2 ALT3 —	GPIO[66] — — — AN[5]	SIUL — — — ADC_0	Input only	—	—	23	32
E[3]	PCR[67]	ALT0 ALT1 ALT2 ALT3 —	GPIO[67] — — — AN[6]	SIUL — — — ADC_0	Input only	—	—	30	42
E[4]	PCR[68]	ALT0 ALT1 ALT2 ALT3 —	GPIO[68] — — — AN[7]	SIUL — — — ADC_0	Input only	—	—	—	44
E[5]	PCR[69]	ALT0 ALT1 ALT2 ALT3 —	GPIO[69] — — — AN[8]	SIUL — — — ADC_0	Input only	—	—	—	43
E[6]	PCR[70]	ALT0 ALT1 ALT2 ALT3 —	GPIO[70] — — — AN[9]	SIUL — — — ADC_0	Input only	—	—	—	45
E[7]	PCR[71]	ALT0 ALT1 ALT2 ALT3 —	GPIO[71] — — — AN[10]	SIUL — — — ADC_0	Input only	—	—	—	41

1 ALT0 is the primary (default) function for each port after reset.

[2] Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIU module. PCR.PA = 00 → ALT0; PCR.PA = 01 → ALT1; PCR.PA = 10 → ALT2; PCR.PA = 11 → ALT3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".

[3] Module included on the MCU.

[4] Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.

[5] Programmable via the SRC (Slew Rate Control) bits in the respective Pad Configuration Register.

[6] ADC0.AN emulates ADC1.AN. This feature is used to provide software compatibility between MPC5602P and MPC5604P. Refer to ADC chapter of reference manual for more details.

3 Electrical characteristics

3.1 Introduction

This section contains device electrical characteristics as well as temperature and power considerations.

This microcontroller contains input protection against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This can be done by the internal pull-up or pull-down resistors, which are provided by the device for most general purpose pins.

The following tables provide the device characteristics and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

CAUTION

All of the following parameter values can vary depending on the application and must be confirmed during silicon characterization or silicon reliability trial.

3.2 Parameter classification

The electrical parameters are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 6 are used and the parameters are tagged accordingly in the tables where appropriate.

Table 6. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute maximum ratings

Table 7. Absolute maximum ratings[1]

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Device ground	—	0	0	V

Table 7. Absolute maximum ratings[1] (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
$V_{DD_HV_IOx}$[2]	SR	3.3 V/5.0 V input/output supply voltage (supply). Code flash memory supply with $V_{DD_HV_IO3}$ and data flash memory with $V_{DD_HV_IO2}$	—	–0.3	6.0	V
$V_{SS_HV_IOx}$	SR	3.3 V/5.0 V input/output supply voltage (ground). Code flash memory ground with $V_{SS_HV_IO3}$ and data flash memory with $V_{SS_HV_IO2}$	—	–0.1	0.1	V
$V_{DD_HV_OSC}$	SR	3.3 V/5.0 V crystal oscillator amplifier supply voltage (supply)	—	–0.3	6.0	V
			Relative to $V_{DD_HV_IOx}$	–0.3	$V_{DD_HV_IOx}$ + 0.3	
$V_{SS_HV_OSC}$	SR	3.3 V/5.0 V crystal oscillator amplifier supply voltage (ground)	—	–0.1	0.1	V
$V_{DD_HV_ADC0}$	SR	3.3 V/5.0 V ADC_0 supply and high-reference voltage	$V_{DD_HV_REG}$ < 2.7 V	–0.3	$V_{DD_HV_REG}$ + 0.3	V
			$V_{DD_HV_REG}$ > 2.7 V	–0.3	6.0	
$V_{SS_HV_ADC0}$	SR	3.3 V/5.0 V ADC_0 ground and low-reference voltage	—	–0.1	0.1	V
$V_{DD_HV_REG}$	SR	3.3 V/5.0 V voltage-regulator supply voltage	—	–0.3	6.0	V
			Relative to $V_{DD_HV_IOx}$	–0.3	$V_{DD_HV_IOx}$ + 0.3	
TV_{DD}	SR	Slope characteristics on all V_{DD} during power up[3] with respect to ground (V_{SS})	—	3.0[4]	500 x 10^3 (0.5 [V/µs])	V/s
$V_{DD_LV_CORx}$	CC	1.2 V supply pins for core logic (supply)	—	–0.1	1.5	V
$V_{SS_LV_CORx}$	SR	1.2 V supply pins for core logic (ground)	—	–0.1	0.1	V
V_{IN}	SR	Voltage on any pin with respect to ground ($V_{SS_HV_IOx}$)	—	–0.3	6.0	V
			Relative to $V_{DD_HV_IOx}$	–0.3	$V_{DD_HV_IOx}$ + 0.3[5]	
I_{INJPAD}	SR	Input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all input currents during overload condition	—	–50	50	mA
T_{STG}	SR	Storage temperature	—	–55	150	°C
T_J	SR	Junction temperature under bias	—	–40	150	°C

1 Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 The difference between each couple of voltage supplies must be less than 300 mV, $|V_{DD_HV_IOy} - V_{DD_HV_IOx}| < 300$ mV.

3 Guaranteed by device validation.

4 Minimum value of TV_{DD} must be guaranteed until $V_{DD_HV_REG}$ reaches 2.6 V (maximum value of V_{PORH})

5 Only when $V_{DD_HV_IOx} < 5.2$ V

Figure 4 shows the constraints of the different power supplies.

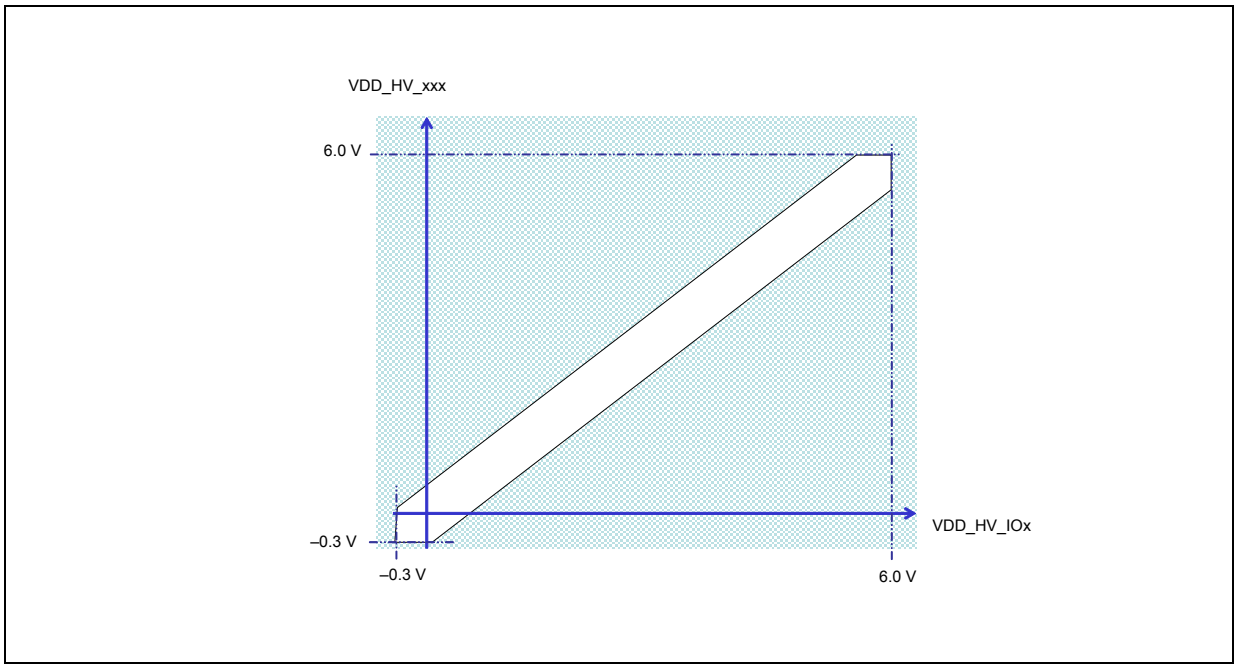


Figure 4. Power supplies constraints (–0.3 V ≤ $V_{DD_HV_IOx}$ ≤ 6.0 V)

The MPC5602P supply architecture allows the ADC supply to be managed independently from the standard V_{DD_HV} supply. Figure 5 shows the constraints of the ADC power supply.

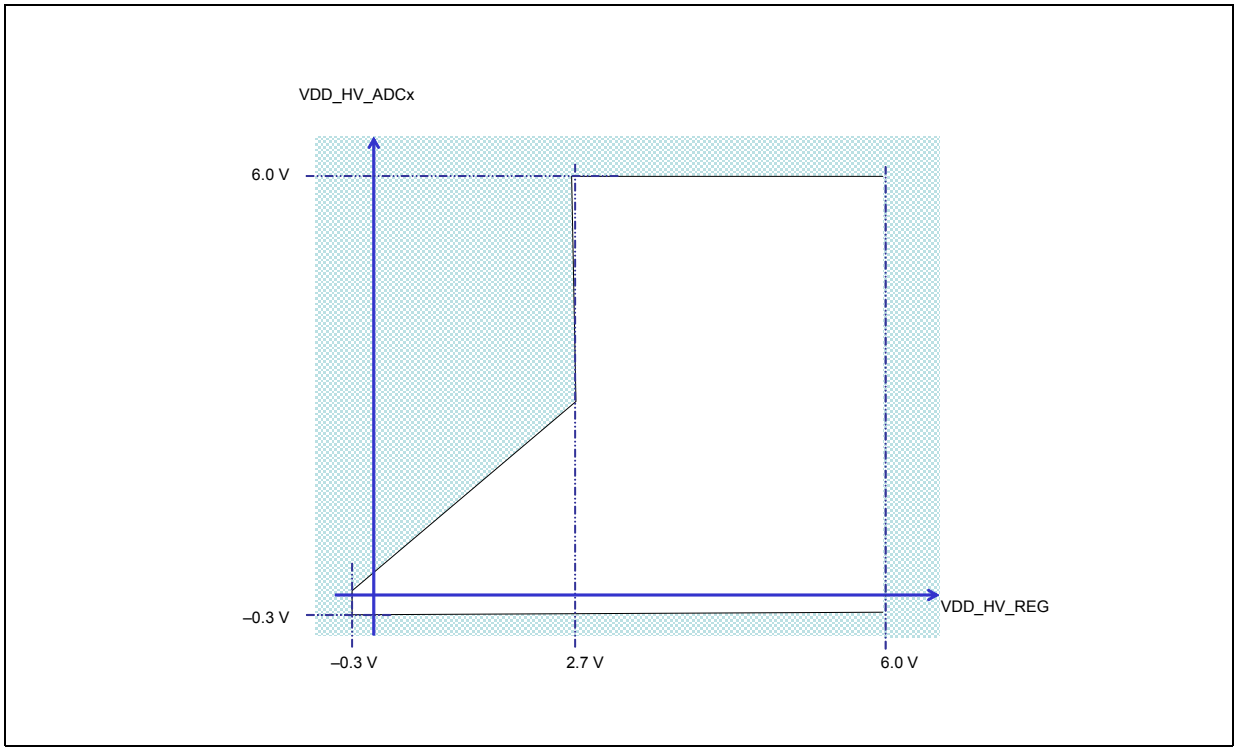


Figure 5. Independent ADC supply (–0.3 V ≤ $V_{DD_HV_REG}$ ≤ 6.0 V)

3.4 Recommended operating conditions

Table 8. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max[1]	
V_{SS}	SR	Device ground	—	0	0	V
$V_{DD_HV_IOx}$[2]	SR	5.0 V input/output supply voltage	—	4.5	5.5	V
$V_{SS_HV_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD_HV_OSC}$	SR	5.0 V crystal oscillator amplifier supply voltage	—	4.5	5.5	V
			Relative to $V_{DD_HV_IOx}$	$V_{DD_HV_IOx}$ – 0.1	$V_{DD_HV_IOx}$ + 0.1	
$V_{SS_HV_OSC}$	SR	5.0 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD_HV_REG}$	SR	5.0 V voltage regulator supply voltage	—	4.5	5.5	V
			Relative to $V_{DD_HV_IOx}$	$V_{DD_HV_IOx}$ – 0.1	$V_{DD_HV_IOx}$ + 0.1	
$V_{DD_HV_ADC0}$	SR	5.0 V ADC_0 supply and high reference voltage	—	4.5	5.5	V
			Relative to $V_{DD_HV_REG}$	$V_{DD_HV_REG}$ – 0.1	—	

Table 8. Recommended operating conditions (5.0 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max[1]	
$V_{SS_HV_ADC0}$	SR	ADC_0 ground and low reference voltage	—	0	0	V
$V_{DD_LV_REGCOR}$[3,4]	CC	Internal supply voltage	—	—	—	V
$V_{SS_LV_REGCOR}$[3]	SR	Internal reference voltage	—	0	0	V
$V_{DD_LV_CORx}$[3,4]	CC	Internal supply voltage	—	—	—	V
$V_{SS_LV_CORx}$[3]	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	—	–40	125	°C

1 Full functionality cannot be guaranteed when voltage drops below 4.5 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.

2 The difference between each couple of voltage supplies must be less than 100 mV, $|V_{DD_HV_IOy} - V_{DD_HV_IOx}| < 100$ mV.

3 To be connected to emitter of external NPN. Low voltage supplies are not under user control—they are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds ($V_{SS_LV_xxx}$) must be shorted to high voltage grounds ($V_{SS_HV_xxx}$) and the low voltage supply pins ($V_{DD_LV_xxx}$) must be connected to the external ballast emitter.

4 The low voltage supplies ($V_{DD_LV_xxx}$) are not all independent.
– $V_{DD_LV_COR1}$ and $V_{DD_LV_COR2}$ are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash memory module. Similarly, $V_{SS_LV_COR1}$ and $V_{SS_LV_COR2}$ are internally shorted.
– $V_{DD_LV_REGCOR}$ and $V_{DD_LV_RECORx}$ are physically shorted internally, as are $V_{SS_LV_REGCOR}$ and $V_{SS_LV_CORx}$.

Table 9. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max[1]	
V_{SS}	SR	Device ground	—	0	0	V
$V_{DD_HV_IOx}$[2]	SR	3.3 V input/output supply voltage	—	3.0	3.6	V
$V_{SS_HV_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD_HV_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	3.0	3.6	V
			Relative to $V_{DD_HV_IOx}$	$V_{DD_HV_IOx} - 0.1$	$V_{DD_HV_IOx} + 0.1$	
$V_{SS_HV_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD_HV_REG}$	SR	3.3 V voltage regulator supply voltage	—	3.0	3.6	V
			Relative to $V_{DD_HV_IOx}$	$V_{DD_HV_IOx} - 0.1$	$V_{DD_HV_IOx} + 0.1$	
$V_{DD_HV_ADC0}$	SR	3.3 V ADC_0 supply and high reference voltage	—	3.0	5.5	V
			Relative to $V_{DD_HV_REG}$	$V_{DD_HV_REG} - 0.1$	5.5	

Table 9. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max[1]	
$V_{SS_HV_ADC0}$	SR	ADC_0 ground and low reference voltage	—	0	0	V
$V_{DD_LV_REGCOR}$[3,4]	CC	Internal supply voltage	—	—	—	V
$V_{SS_LV_REGCOR}$[3]	SR	Internal reference voltage	—	0	0	V
$V_{DD_LV_CORx}$[3,4]	CC	Internal supply voltage	—	—	—	V
$V_{SS_LV_CORx}$[3]	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	—	–40	125	°C

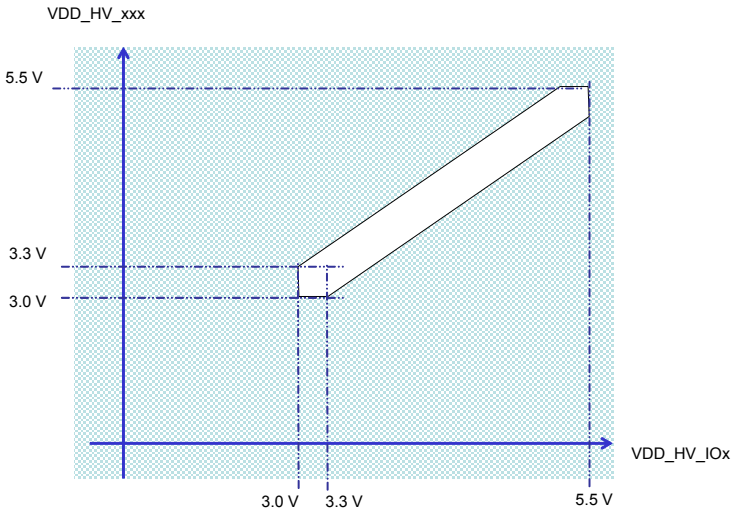
1 Full functionality cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.

2 The difference between each couple of voltage supplies must be less than 100 mV, $|V_{DD_HV_IOy} - V_{DD_HV_IOx}| < 100$ mV.

3 To be connected to emitter of external NPN. Low voltage supplies are not under user control—they are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds ($V_{SS_LV_xxx}$) must be shorted to high voltage grounds ($V_{SS_HV_xxx}$) and the low voltage supply pins ($V_{DD_LV_xxx}$) must be connected to the external ballast emitter.

4 The low voltage supplies ($V_{DD_LV_xxx}$) are not all independent.
– $V_{DD_LV_COR1}$ and $V_{DD_LV_COR2}$ are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash memory module. Similarly, $V_{SS_LV_COR1}$ and $V_{SS_LV_COR2}$ are internally shorted.
– $V_{DD_LV_REGCOR}$ and $V_{DD_LV_RECORx}$ are physically shorted internally, as are $V_{SS_LV_REGCOR}$ and $V_{SS_LV_CORx}$.

Figure 6 shows the constraints of the different power supplies.



Note: IO AC and DC characteristics are guaranteed only in the range of 3.0–3.6 V when PAD3V5V is low, and in the range of 4.5–5.5 V when PAD3V5V is high.

Figure 6. Power supplies constraints (3.0 V ≤ $V_{DD_HV_IOx}$ ≤ 5.5 V)

The MPC5602P supply architecture allows the ADC supply to be managed independently from the standard V_{DD_HV} supply. Figure 7 shows the constraints of the ADC power supply.

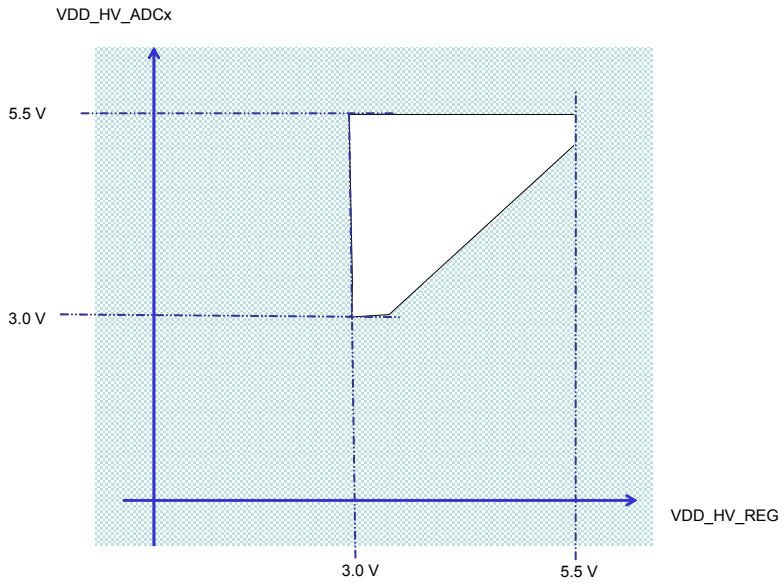


Figure 7. Independent ADC supply (3.0 V ≤ $V_{DD_HV_REG}$ ≤ 5.5 V)

3.5 Thermal characteristics

3.5.1 Package thermal characteristics

Table 10. LQFP thermal characteristics

Symbol	Parameter	Conditions	Typical value		Unit
			100-pin	64-pin	
$R_{\theta JA}$	Thermal resistance junction-to-ambient, natural convection[1]	Single layer board—1s	63	57	°C/W
		Four layer board—2s2p	51	41	°C/W
$R_{\theta JB}$	Thermal resistance junction-to-board[2]	Four layer board—2s2p	33	22	°C/W
$R_{\theta JCtop}$	Thermal resistance junction-to-case (top)[3]	Single layer board—1s	15	13	°C/W
Ψ_{JB}	Junction-to-board, natural convection[4]	Operating conditions	33	22	°C/W
Ψ_{JC}	Junction-to-case, natural convection[5]	Operating conditions	1	1	°C/W

1 Junction-to-ambient thermal resistance determined per JEDEC JESD51-7. Thermal test board meets JEDEC specification for this package.

2 Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. When Greek letters are not available, the symbols are typed as RthJB or Theta-JB.

3 Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4 Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

5 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

3.5.2 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from Equation 1:

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in Equation 2 as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using Equation 3:

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

- Semiconductor Equipment and Materials International
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  San Jose, CA 95134U.S.A.
  (408) 943-6900
- MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at (800) 854-7179 or (303) 397-7956.
- JEDEC specifications are available on the WEB at http://www.jedec.org.
- C.E. Triplett and B. Joiner, *An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module*, Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
- G. Kromann, S. Shidore, and S. Addison, *Thermal Modeling of a PBGA for Air-Cooled Applications*, Electronic Packaging and Production, pp. 53–58, March 1998.
- B. Joiner and V. Adams, *Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling*, Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

3.6 Electromagnetic interference (EMI) characteristics

Table 11. EMI testing specifications

Symbol	Parameter	Conditions	Clocks	Frequency	Level (Typ)	Unit
V_{EME}	Radiated emissions	V_{DD} = 5.0 V; T_A = 25 °C Other device configuration, test conditions and EM testing per standard IEC61967-2	f_{OSC} = 8 MHz f_{CPU} = 64 MHz No PLL frequency modulation	150 kHz–150 MHz	11	dBµV
				150–1000 MHz	13	
				IEC level	M	—
			f_{OSC} = 8 MHz f_{CPU} = 64 MHz ±4% PLL frequency modulation	150 kHz–150 MHz	8	dBµV
				150–1000 MHz	12	
				IEC level	N	—
		V_{DD} = 3.3 V; T_A = 25 °C Other device configuration, test conditions and EM testing per standard IEC61967-2	f_{OSC} = 8 MHz f_{CPU} = 64 MHz No PLL frequency modulation	150 kHz–150 MHz	9	dBµV
				150–1000 MHz	12	
				IEC level	M	—
			f_{OSC} = 8 MHz f_{CPU} = 64 MHz ±4% PLL frequency modulation	150 kHz–150 MHz	7	dBµV
				150–1000 MHz	12	
				IEC level	N	—

3.7 Electrostatic discharge (ESD) characteristics

Table 12. ESD ratings[1,2]

Symbol		Parameter	Conditions	Value	Unit
$V_{ESD(HBM)}$	SR	Electrostatic discharge (Human Body Model)	—	2000	V
$V_{ESD(CDM)}$	SR	Electrostatic discharge (Charged Device Model)	—	750 (corners)	V
				500 (other)	

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3.8 Power management electrical characteristics

3.8.1 Voltage regulator electrical characteristics

The internal voltage regulator requires an external NPN ballast, approved ballast list availbale in Table 13, to be connected as shown in Figure 8. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the $V_{DD_HV_REG}$, BCTRL and $V_{DD_LV_CORx}$ pins to less than L_{Reg}. (refer to Table 14).

NOTE

The voltage regulator output cannot be used to drive external circuits. Output pins are to be used only for decoupling capacitance.

$V_{DD_LV_COR}$ must be generated using internal regulator and external NPN transistor. It is not possible to provide $V_{DD_LV_COR}$ through external regulator.

For the MPC5602P microcontroller, capacitor(s), with total values not below C_{DEC1}, should be placed between $V_{DD_LV_CORx}/V_{SS_LV_CORx}$ close to external ballast transistor emitter. 4 capacitors, with total values not below C_{DEC2}, should be placed close to microcontroller pins between each $V_{DD_LV_CORx}/V_{SS_LV_CORx}$ supply pairs and the $V_{DD_LV_REGCOR}/V_{SS_LV_REGCOR}$ pair . Additionally, capacitor(s) with total values not below C_{DEC3}, should be placed between the $V_{DD_HV_REG}/V_{SS_HV_REG}$ pins close to ballast collector. Capacitors values have to take into account capacitor accuracy, aging and variation versus temperature.

All reported information are valid for voltage and temperature ranges described in recommended operating condition, Table 8 and Table 9.

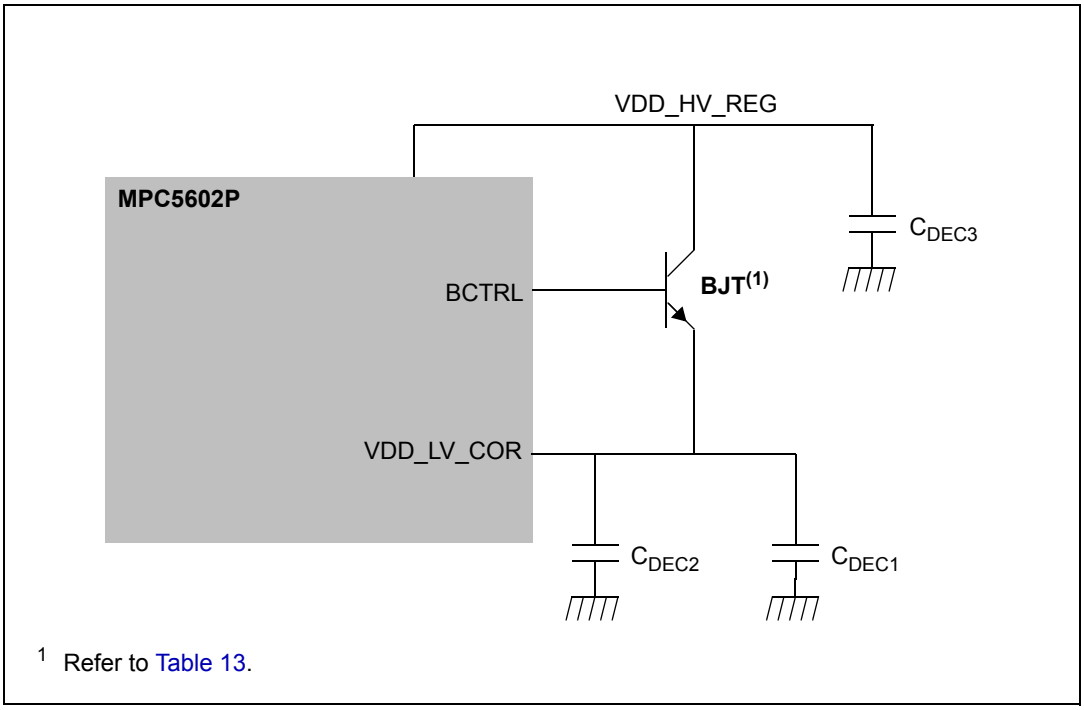


Figure 8. Voltage regulator configuration

Table 13. Approved NPN ballast components

Part	Manufacturer	Approved derivatives[1]
BCP68	ON Semi	BCP68
	NXP	BCP68-25
	Infineon	BCP68-25
BCX68	Infineon	BCX68-10; BCX68-16; BCX-25
BC868	NXP	BC868

Table 13. Approved NPN ballast components

Part	Manufacturer	Approved derivatives[1]
BC817	Infineon	BC817-16; BC817-25; BC817SU
	NXP	BC817-16; BC817-25
BCP56	ST	BCP56-16
	Infineon	BCP56-10; BCP56-16
	ON Semi	BCP56-10
	NXP	BCP56-10; BCP56-16

1 For automotive applications please check with the appropriate transistor vendor for automotive grade certification

Table 14. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$V_{DD_LV_REGCOR}$	CC	P	Output voltage under maximum load run supply current configuration	Post-trimming	1.15	—	1.32	V
C_{DEC1}	SR	—	External decoupling/stability ceramic capacitor	BJT from Table 13. Three capacitors (i.e. X7R or X8R capacitors) with nominal value of 10 µF	19.5	30	—	µF
				BJT BC817, one capacitance of 22 µF	14.3	22	—	µF
R_{REG}	SR	—	Resulting ESR of either one or all three C_{DEC1}	Absolute maximum value between 100 kHz and 10 MHz	—	—	45	mΩ
C_{DEC2}	SR	—	External decoupling/stability ceramic capacitor	Four capacitances (i.e. X7R or X8R capacitors) with nominal value of 440 nF	1200	1760	—	nF
C_{DEC3}	SR	—	External decoupling/stability ceramic capacitor on VDD_HV_REG	Three capacitors (i.e. X7R or X8R capacitors) with nominal value of 10 µF; C_{DEC3} has to be equal or greater than C_{DEC1}	19.5	30	—	µF
L_{Reg}	SR	—	Resulting ESL of $V_{DD_HV_REG}$, BCTRL and $V_{DD_LV_CORx}$ pins	—	—	—	5	nH

3.8.2 Voltage monitor electrical characteristics

The device implements a power on reset module to ensure correct power-up initialization, as well as three low voltage detectors to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the 5.0 V ± 10% range

- LVDLVCOR monitors low voltage digital power domain

Table 15. Low voltage monitor electrical characteristics

Symbol	C	Parameter	Conditions[1]	Value		Unit
				Min	Max	
V_{PORH}	T	Power-on reset threshold	—	1.5	2.7	V
V_{PORUP}	P	Supply for functional POR module	T_A = 25 °C	1.0	—	V
$V_{REGLVDMOK_H}$	P	Regulator low voltage detector high threshold	—	—	2.95	V
$V_{REGLVDMOK_L}$	P	Regulator low voltage detector low threshold	—	2.6	—	V
$V_{FLLVDMOK_H}$	P	Flash low voltage detector high threshold	—	—	2.95	V
$V_{FLLVDMOK_L}$	P	Flash low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDMOK_H}$	P	I/O low voltage detector high threshold	—	—	2.95	V
$V_{IOLVDMOK_L}$	P	I/O low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDM5OK_H}$	P	I/O 5 V low voltage detector high threshold	—	—	4.4	V
$V_{IOLVDM5OK_L}$	P	I/O 5 V low voltage detector low threshold	—	3.8	—	V
$V_{MLVDDOK_H}$	P	Digital supply low voltage detector high	—	—	1.145	V
$V_{MLVDDOK_L}$	P	Digital supply low voltage detector low	—	1.08	—	V

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified

3.9 Power up/down sequencing

To prevent an overstress event or a malfunction within and outside the device, the MPC5602P implements the following sequence to ensure each module is started only when all conditions for switching it ON are available:

- A POWER_ON module working on voltage regulator supply controls the correct start-up of the regulator. This is a key module ensuring safe configuration for all voltage regulator functionality when supply is below 1.5 V. Associated POWER_ON (or POR) signal is active low.
- Several low voltage detectors, working on voltage regulator supply monitor the voltage of the critical modules (voltage regulator, I/Os, flash memory and low voltage domain). LVDs are gated low when POWER_ON is active.
- A POWER_OK signal is generated when all critical supplies monitored by the LVD are available. This signal is active high and released to all modules including I/Os, flash memory and 16 MHz RC oscillator needed during power-up phase and reset phase. When POWER_OK is low the associated modules are set into a safe state.

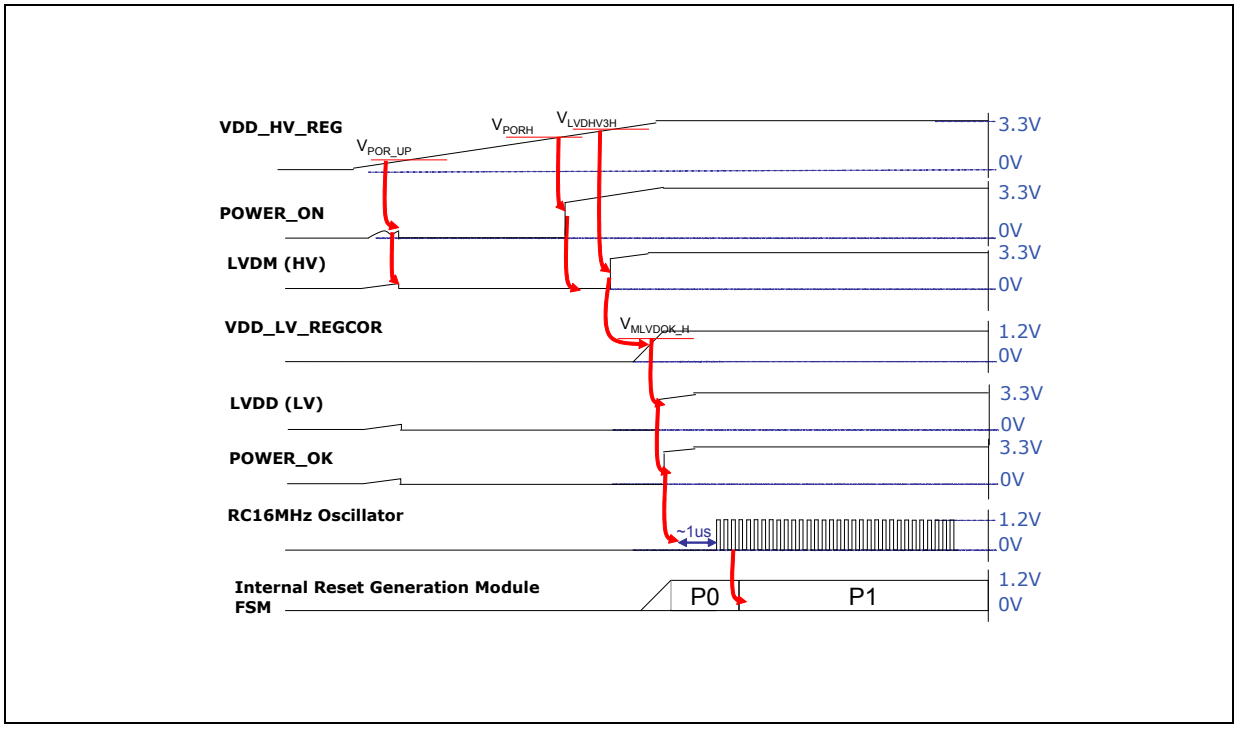


Figure 9. Power-up typical sequence

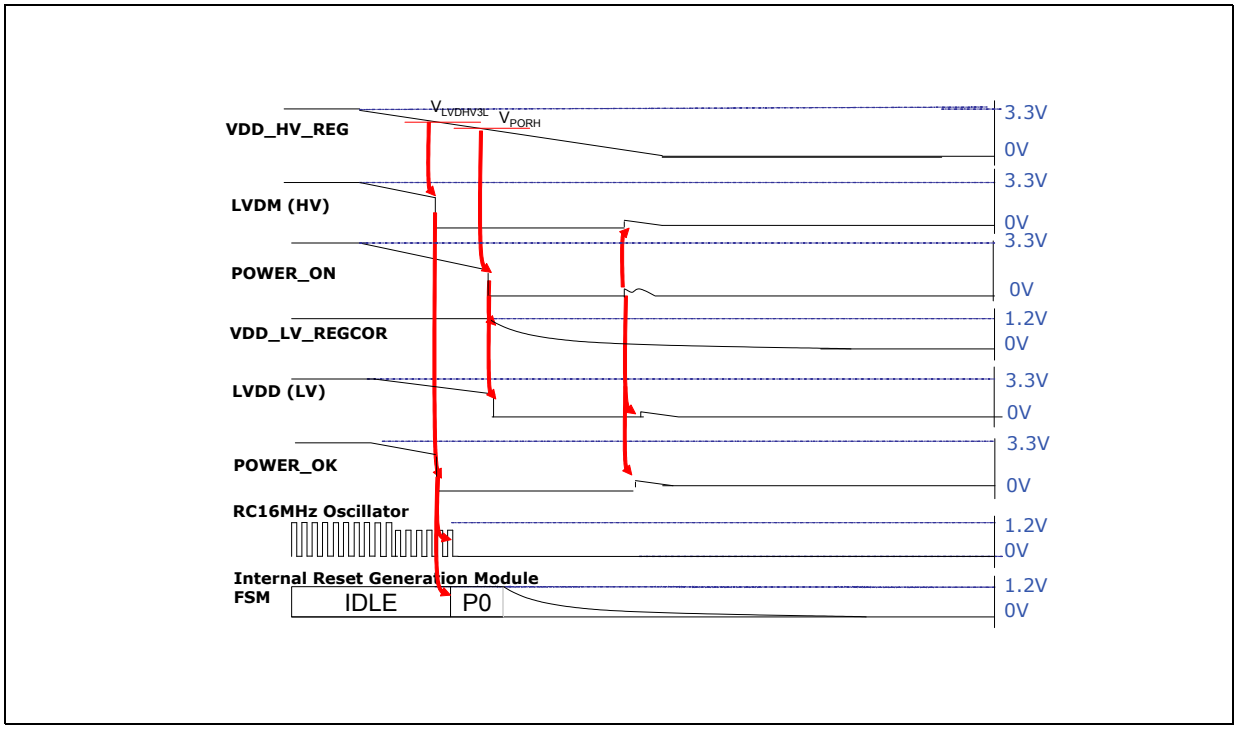


Figure 10. Power-down typical sequence

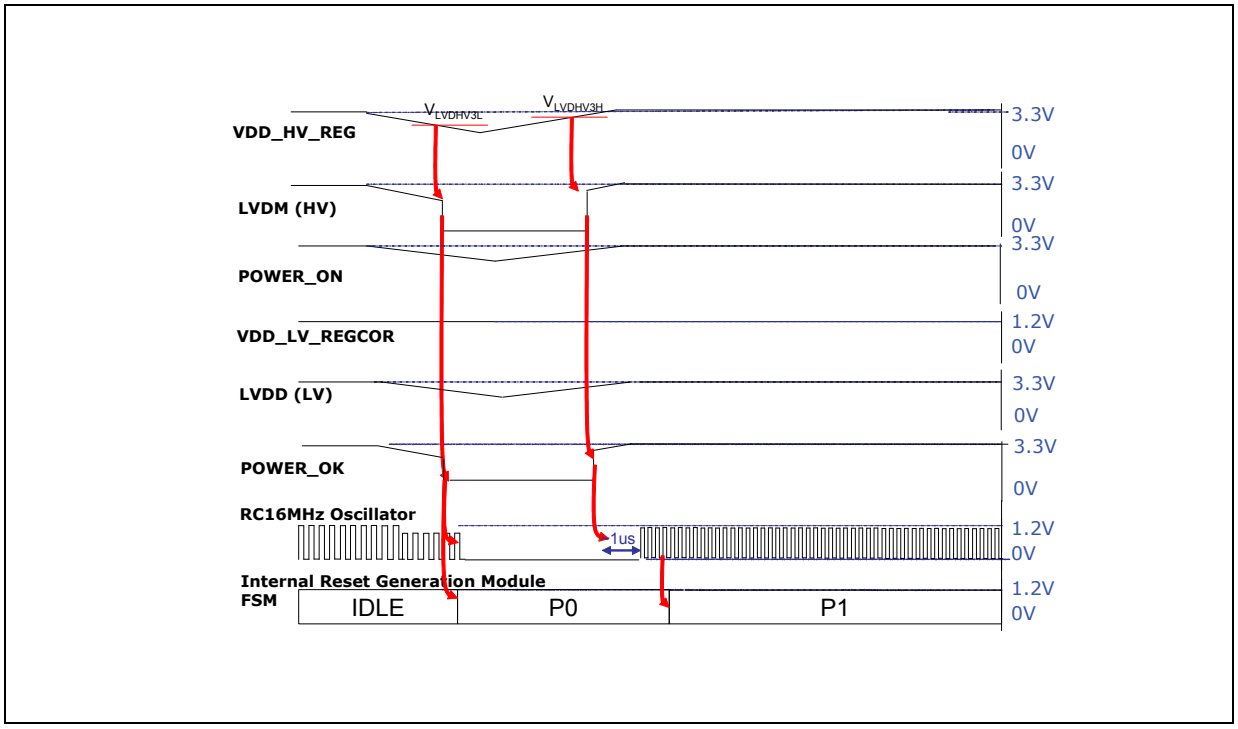


Figure 11. Brown-out typical sequence

3.10 DC electrical characteristics

3.10.1 NVUSRO register

Portions of the device configuration, such as high voltage supply and watchdog enable/disable after reset are controlled via bit values in the non-volatile user options (NVUSRO) register.

For a detailed description of the NVUSRO register, please refer to the device reference manual.

3.10.1.1 NVUSRO[PAD3V5V] field description

The DC electrical characteristics are dependent on the PAD3V5V bit value. Table 16 shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 16. PAD3V5V field description

Value[1]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1 Default manufacturing value before flash initialization is '1' (3.3 V).

3.10.2 DC electrical characteristics (5 V)

Table 17 gives the DC electrical characteristics at 5 V ($4.5\ V < V_{DD_HV_IOx} < 5.5\ V$, NVUSRO[PAD3V5V] = 0).

Table 17. DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Max	
V_{IL}	D	Low level input voltage	—	–0.4[1]	—	V
	P		—	—	0.35 $V_{DD_HV_IOx}$	V
V_{IH}	P	High level input voltage	—	0.65 $V_{DD_HV_IOx}$	—	V
	D		—	—	$V_{DD_HV_IOx}$ + 0.4[1]	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD_HV_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD_HV_IOx}$	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD_HV_IOx}$	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD_HV_IOx}$	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD_HV_IOx}$	—	V
V_{OL_F}	P	Fast, low level output voltage	I_{OL} = 14 mA	—	0.1 $V_{DD_HV_IOx}$	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –14 mA	0.8 $V_{DD_HV_IOx}$	—	V
I_{PU}	P	Equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	
I_{PD}	P	Equivalent pull-down current	V_{IN} = V_{IL}	10	—	µA
			V_{IN} = V_{IH}	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = –40 to 125 °C	–1	1	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = –40 to 125 °C	–0.5	0.5	µA
C_{IN}	D	Input capacitance	—	—	10	pF

[1] “SR” parameter values must not exceed the absolute maximum ratings shown in Table 7.

Table 18. Supply current (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol	C	Parameter		Conditions		Value[1]		Unit
						Typ	Max	
$I_{DD_LV_CORx}$	T	Supply current	RUN—Maximum mode[2]	$V_{DD_LV_CORx}$ externally forced at 1.3 V	40 MHz	44	55	mA
	P				64 MHz	52	65	
	T		RUN—Typical mode[3]		40 MHz	38	46	
					64 MHz	45	54	
	P		HALT mode[4]		—	1.5	10	
			STOP mode[5]		—	1	10	
I_{DD_FLASH}	T		Flash during read	$V_{DD_HV_FL}$ at 5.0 V	—	8	10	
			Flash during erase operation on 1 flash module	$V_{DD_HV_FL}$ at 5.0 V	—	15	19	
I_{DD_ADC}	T		ADC	$V_{DD_HV_ADC0}$ at 5.0 V f_{ADC} = 16 MHz	ADC_0	3	4	
I_{DD_OSC}	T		Oscillator	$V_{DD_HV_OSC}$ at 5.0 V	8 MHz	2.6	3.2	
$I_{DD_HV_REG}$	D		Internal regulator module current consumption	$V_{DD_HV_REG}$ at 5.5 V		—	10	

1 All values to be confirmed after characterization/data collection.

2 Maximum mode: FlexPWM, ADC, CTU, DSPI, LINFlex, FlexCAN, 15 output pins, PLL_0 enabled, 125 °C ambient. I/O supply current excluded.

3 Typical mode configurations: DSPI, LINFlex, FlexCAN, 15 output pins, PLL_0, 105 °C ambient. I/O supply current excluded.

4 Halt mode configurations: Code fetched from SRAM, code flash memory and data flash memory in low power mode, OSC/PLL_0 are OFF, core clock frozen, all peripherals disabled.

5 STOP “P” mode Device Under Test (DUT) configuration: Code fetched from SRAM, code flash memory and data flash memory off, OSC/PLL_0 are OFF, core clock frozen, all peripherals disabled.

3.10.3 DC electrical characteristics (3.3 V)

Table 19 gives the DC electrical characteristics at 3.3 V (3.0 V < $V_{DD_HV_IOx}$ < 3.6 V, NVUSRO[PAD3V5V] = 1); see Figure 12.

Table 19. DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)[1]

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Max	
V_{IL}	D	Low level input voltage	—	–0.4[2]	—	V
	P		—	—	0.35 $V_{DD_HV_IOx}$	V
V_{IH}	P	High level input voltage	—	0.65 $V_{DD_HV_IOx}$	—	V
	D		—	—	$V_{DD_HV_IOx}$ + 0.4[2]	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD_HV_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –1.5 mA	$V_{DD_HV_IOx}$ – 0.8	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 2 mA	—	0.5	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –2 mA	$V_{DD_HV_IOx}$ – 0.8	—	V
V_{OL_F}	P	Fast, low level output voltage	I_{OL} = 11 mA	—	0.5	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –11 mA	$V_{DD_HV_IOx}$ – 0.8	—	V
I_{PU}	P	Equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	
I_{PD}	P	Equivalent pull-down current	V_{IN} = V_{IL}	10	—	µA
			V_{IN} = V_{IH}	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = –40 to 125 °C	—	1	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = –40 to 125 °C	—	0.5	µA
C_{IN}	D	Input capacitance	—	—	10	pF

1 These specifications are design targets and subject to change per device characterization.

2 “SR” parameter values must not exceed the absolute maximum ratings shown in Table 7.

Table 20. Supply current (3.3 V, NVUSRO[PAD3V5V] = 1)

Symbol	C	Parameter		Conditions		Value[1]		Unit
						Typ	Max	
$I_{DD_LV_CORx}$	T	Supply current	RUN—Maximum mode[2]	$V_{DD_LV_CORx}$ externally forced at 1.3 V	40 MHz	44	55	mA
					64 MHz	52	65	
			RUN—Typical mode[3]		40 MHz	38	46	
					64 MHz	45	54	
	P		HALT mode[4]		—	1.5	10	
			STOP mode[5]		—	1	10	
I_{DD_ADC}	T		ADC	$V_{DD_HV_ADC0}$ at 3.3 V f_{ADC} = 16 MHz	ADC_0	3	4	
I_{DD_OSC}	T		Oscillator	$V_{DD_HV_OSC}$ at 3.3 V	8 MHz	2.6	3.2	
$I_{DD_HV_REG}$	D		Internal regulator module current consumption	$V_{DD_HV_REG}$ at 5.5 V		—	10	

1 All values to be confirmed after characterization/data collection.

2 Maximum mode: FlexPWM, ADC, CTU, DSPI, LINFlex, FlexCAN, 15 output pins, PLL_0 enabled, 125 °C ambient. I/O supply current excluded.

3 Typical mode configurations: DSPI, LINFlex, FlexCAN, 15 output pins, PLL_0, 105 °C ambient. I/O supply current excluded.

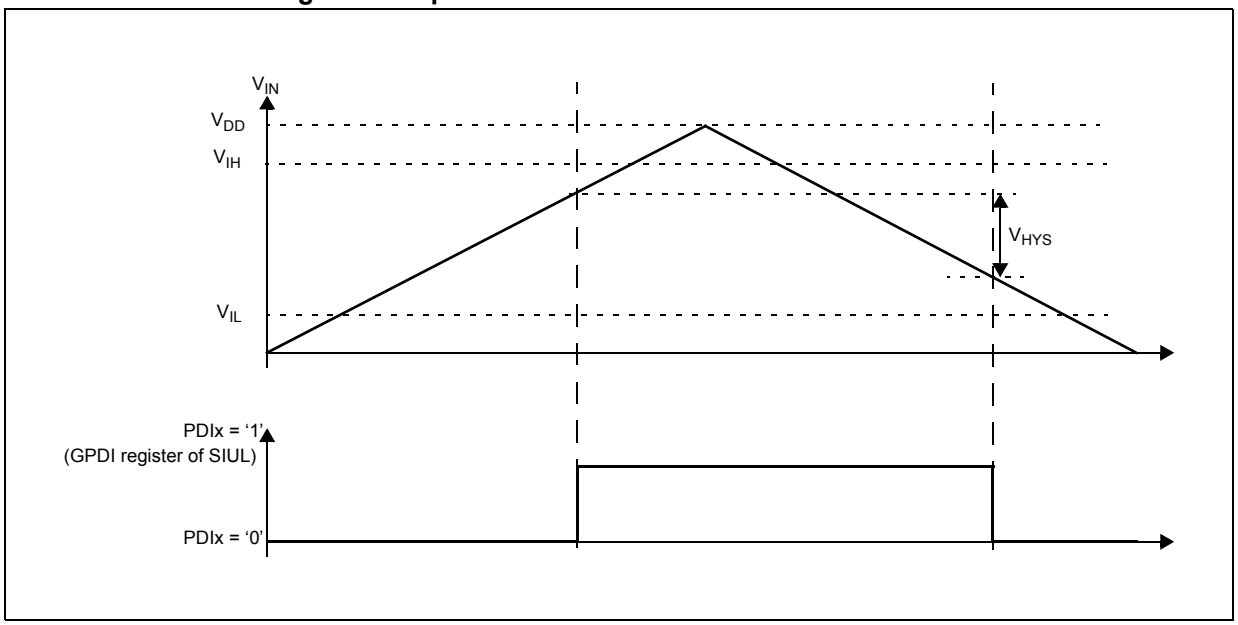
4 Halt mode configurations: Code fetched from SRAM, code flash memory and data flash memory in low power mode, OSC/PLL_0 are OFF, core clock frozen, all peripherals disabled.

5 STOP “P” mode Device Under Test (DUT) configuration: Code fetched from SRAM, code flash memory and data flash memory off, OSC/PLL_0 are OFF, core clock frozen, all peripherals disabled.

3.10.4 Input DC electrical characteristics definition

Figure 12 shows the DC electrical characteristics behavior as function of time.

Figure 12. Input DC electrical characteristics definition



3.10.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in Table 21.

Table 21. I/O supply segment

Package	Supply segment				
	1	2	3	4	5
100 LQFP	pin15–pin26	pin27–pin46	pin51–pin61	pin64–pin86	pin89–pin10
64 LQFP	pin8–pin17	pin18–pin30	pin33–pin38	pin41–pin54	pin57–pin5

Table 22. I/O consumption

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{SWTSLW}[2]	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16	
I_{SWTMED}(2)	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	29	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	17	

Table 22. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{SWTFST}[(2)]	CC	D	Dynamic I/O current for FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	110	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
I_{RMSSLW}	CC	D	Root medium square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
				C_L = 25 pF, 4 MHz		—	—	3.2	
				C_L = 100 pF, 2 MHz		—	—	6.6	
				C_L = 25 pF, 2 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
				C_L = 25 pF, 4 MHz		—	—	2.3	
				C_L = 100 pF, 2 MHz		—	—	4.7	
I_{RMSMED}	CC	D	Root medium square I/O current for MEDIUM configuration	C_L = 25 pF, 13 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	mA
				C_L = 25 pF, 40 MHz		—	—	13.4	
				C_L = 100 pF, 13 MHz		—	—	18.3	
				C_L = 25 pF, 13 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	5	
				C_L = 25 pF, 40 MHz		—	—	8.5	
				C_L = 100 pF, 13 MHz		—	—	11	
I_{RMSFST}	CC	D	Root medium square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	56	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	35	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

3.11 Main oscillator electrical characteristics

The MPC5602P provides an oscillator/resonator driver.

Table 23. Main oscillator output electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{OSC}	SR	—	Oscillator frequency		4	40	MHz
g_m	—	P	Transconductance		6.5	25	mA/V
V_{OSC}	—	T	Oscillation amplitude on XTAL pin		1	—	V
t_{OSCSU}	—	T	Start-up time[1,2]		8	—	ms
C_L	CC	T	XTAL load capacitance[3]	4 MHz	5	30	pf
		T		8 MHz	5	26	
		T		12 MHz	5	23	
		T		16 MHz	5	19	
		T		20 MHz	5	16	
		T		40 MHz	5	8	

1 The start-up time is dependent upon crystal characteristics, board leakage, etc. High ESR and excessive capacitive loads can cause long start-up time.

2 Value captured when amplitude reaches 90% of XTAL

3 This value is determined by the crystal manufacturer and board design. For 4 MHz to 40 MHz crystals specified for this oscillator, load capacitors should not exceed these limits.

Table 24. Main oscillator output electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{OSC}	SR	—	Oscillator frequency		4	40	MHz
g_m	—	P	Transconductance		4	20	mA/V
V_{OSC}	—	T	Oscillation amplitude on XTAL pin		1	—	V
t_{OSCSU}	—	T	Start-up time[1,2]		8	—	ms
C_L	CC	T	XTAL load capacitance[3]	4 MHz	5	30	pf
		T		8 MHz	5	26	
		T		12 MHz	5	23	
		T		16 MHz	5	19	
		T		20 MHz	5	16	
		T		40 MHz	5	8	

1 The start-up time is dependent upon crystal characteristics, board leakage, etc. High ESR and excessive capacitive loads can cause long start-up time.

2 Value captured when amplitude reaches 90% of XTAL

3 This value is determined by the crystal manufacturer and board design. For 4 MHz to 40 MHz crystals specified for this oscillator, load capacitors should not exceed these limits.

Table 25. Input clock characteristics

Symbol		Parameter	Value			Unit
			Min	Typ	Max	
f_{OSC}	SR	Oscillator frequency	4	—	40	MHz
f_{CLK}	SR	Frequency in bypass	—	—	64	MHz
t_{rCLK}	SR	Rise/fall time in bypass	—	—	1	ns
t_{DC}	SR	Duty cycle	47.5	50	52.5	%

3.12 FMPLL electrical characteristics

Table 26. FMPLL electrical characteristics

Symbol	C	Parameter		Conditions[1]	Value		Unit
					Min	Max	
$f_{ref_crystal}$ f_{ref_ext}	D	PLL reference frequency range[2]		Crystal reference	4	40	MHz
f_{PLLIN}	D	Phase detector input frequency range (after pre-divider)		—	4	16	MHz
$f_{FMPLLOUT}$	D	Clock frequency range in normal mode		—	16	64	MHz
f_{FREE}	P	Free-running frequency		Measured using clock division—typically /16	20	150	MHz
t_{CYC}	D	System clock period		—	—	1 / f_{SYS}	ns
f_{LORL}	D	Loss of reference frequency window[3]		Lower limit	1.6	3.7	MHz
f_{LORH}	D			Upper limit	24	56	
f_{SCM}	D	Self-clocked mode frequency[4,5]		—	20	150	MHz
C_{JITTER}	T	CLKOUT period jitter[6,7,8,9]	Short-term jitter[10]	f_{SYS} maximum	–4	4	% f_{CLKOUT}
			Long-term jitter (average over 2 ms interval)	f_{PLLIN} = 16 MHz (resonator), f_{PLLCLK} at 64 MHz, 4000 cycles	—	10	ns
t_{lpll}	D	PLL lock time[11, 12]		—	—	200	µs
t_{dc}	D	Duty cycle of reference		—	40	60	%
f_{LCK}	D	Frequency LOCK range		—	–6	6	% f_{SYS}
f_{UL}	D	Frequency un-LOCK range		—	–18	18	% f_{SYS}
f_{CS}	D	Modulation depth		Center spread	±0.25	±4.0[13]	% f_{SYS}
f_{DS}	D			Down spread	–0.5	–8.0	
f_{MOD}	D	Modulation frequency[14]		—	—	70	kHz

1 $V_{DD_LV_CORx}$ = 1.2 V ±10%; V_{SS} = 0 V; T_A = –40 to 125 °C, unless otherwise specified

2 Considering operation with PLL not bypassed.

3 “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.

[4] Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.

[5] f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.

[6] This value is determined by the crystal manufacturer and board design.

[7] Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via $V_{DD_LV_COR0}$ and $V_{SS_LV_COR0}$ and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.

[8] Proper PC board layout procedures must be followed to achieve specifications.

[9] Values are obtained with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).

[10] Short term jitter is measured on the clock rising edge at cycle n and cycle n+4.

[11] This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits.

[12] This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

[13] This value is true when operating at frequencies above 60 MHz, otherwise f_{CS} is 2% (above 64 MHz).

[14] Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

3.13 16 MHz RC oscillator electrical characteristics

Table 27. 16 MHz RC oscillator electrical characteristics

Symbol	C	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
f_{RC}	P	RC oscillator frequency	T_A = 25 °C	—	16	—	MHz
Δ_{RCMVAR}	P	Fast internal RC oscillator variation over temperature and supply with respect to f_{RC} at T_A = 25 °C in high-frequency configuration	—	–5	—	5	%

3.14 Analog-to-digital converter (ADC) electrical characteristics

The device provides a 10-bit Successive Approximation Register (SAR) analog-to-digital converter.

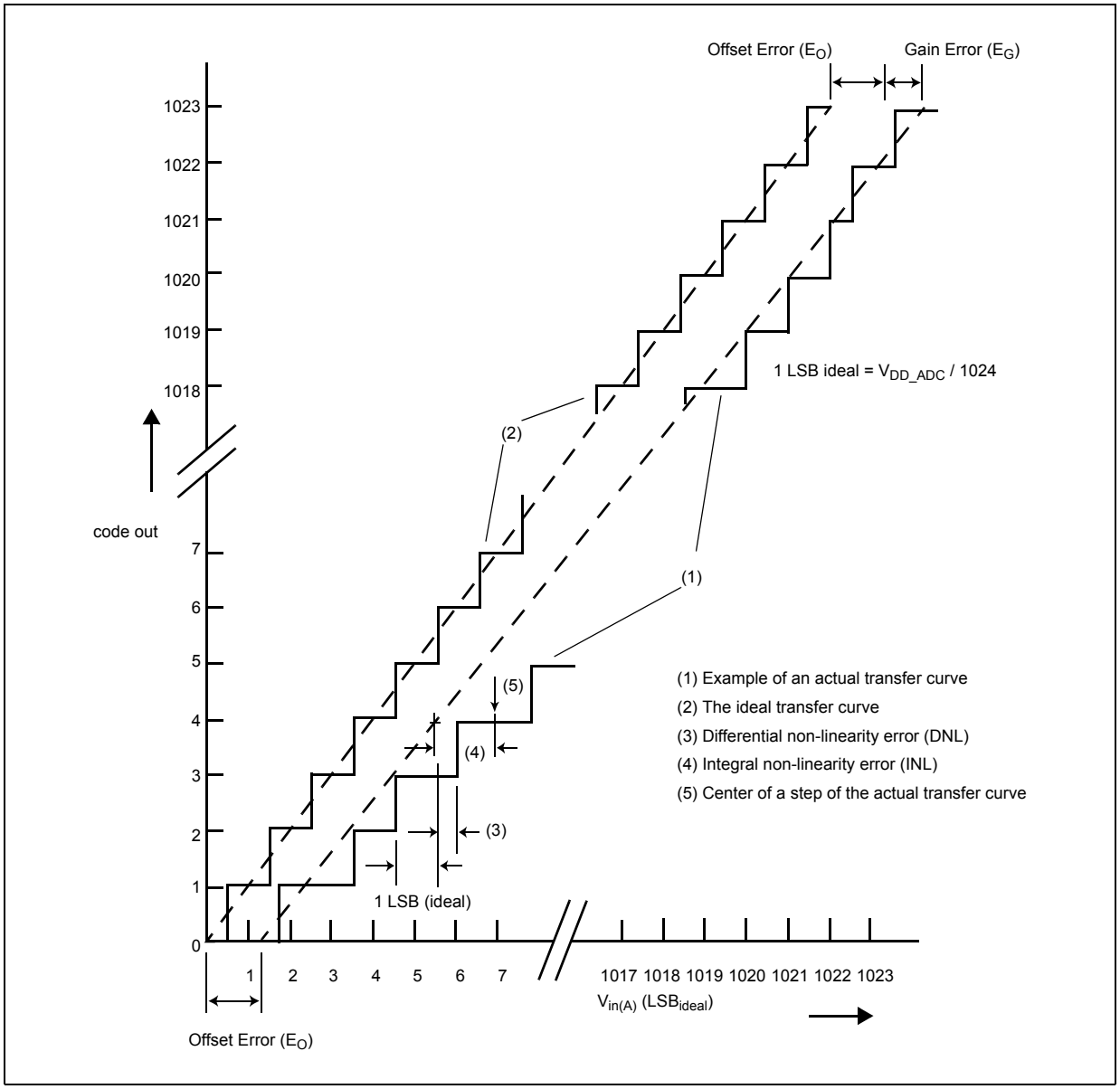


Figure 13. ADC characteristics and error definitions

3.14.1 Input impedance and ADC accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the source impedance value of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S and C_{P2} being substantially two switched capacitances, with a frequency equal to the ADC conversion rate, it can be seen as a resistive path

to ground. For instance, assuming a conversion rate of 1 MHz, with C_S+C_{P2} equal to 3 pF, a resistance of 330 kΩ is obtained (R_{EQ} = 1 / (fc × (C_S+C_{P2})), where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S+C_{P2}) and the sum of R_S + R_F, the external circuit must be designed to respect the Equation 4:

Eqn. 4

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 4 generates a constraint for external network design, in particular on resistive path.

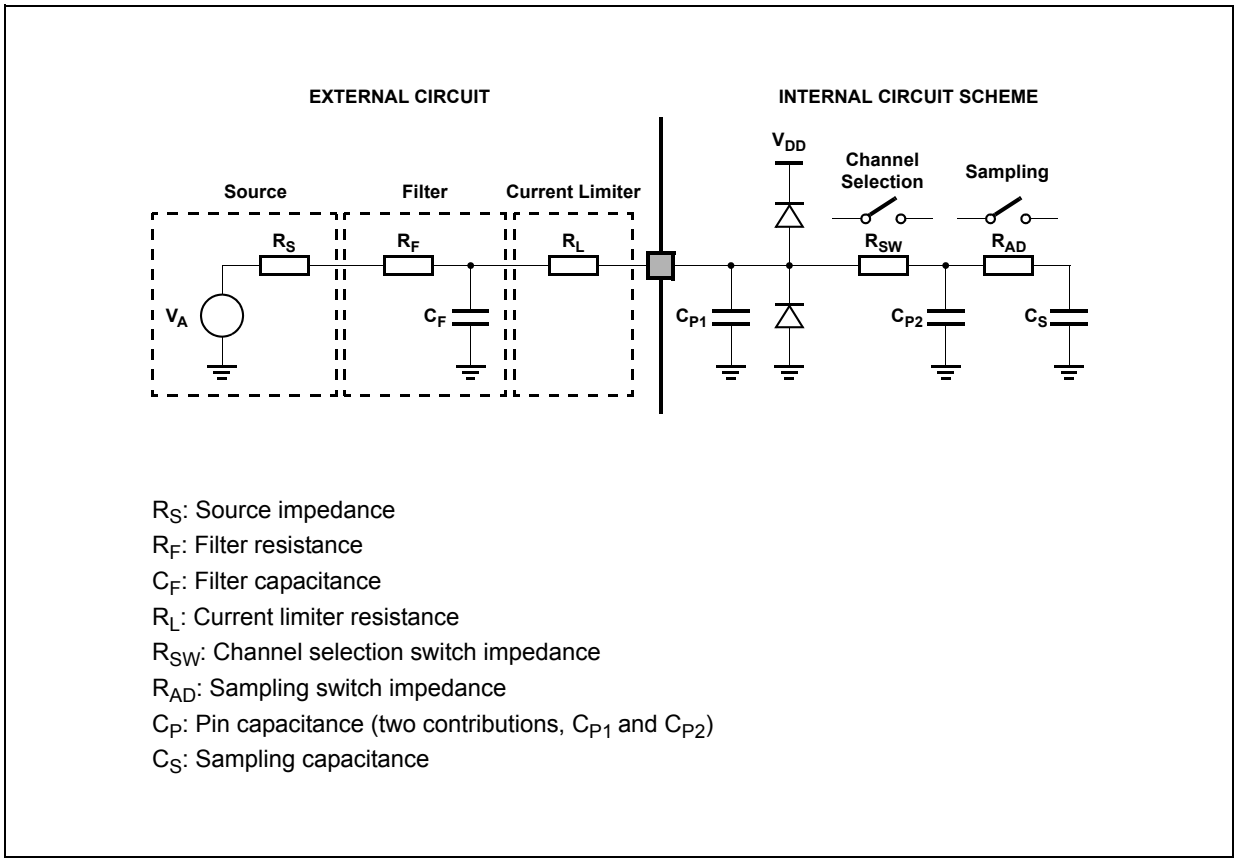


Figure 14. Input equivalent circuit

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 14): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch closed).

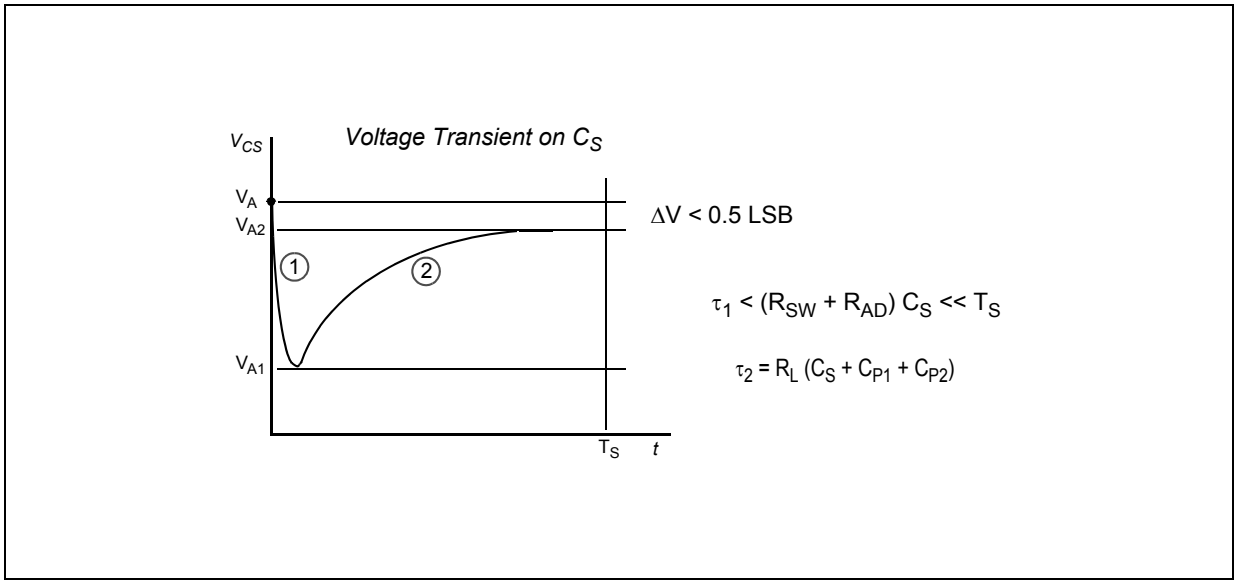


Figure 15. Transient behavior during sampling phase

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Eqn. 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Eqn. 6

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to Equation 7:

Eqn. 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Eqn. 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

Eqn. 9

$$8.5 \bullet \tau_2 = 8.5 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. Equation 10 must be respected (charge balance assuming now C_S already charged at V_{A1}):

Eqn. 10

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the R_FC_F filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

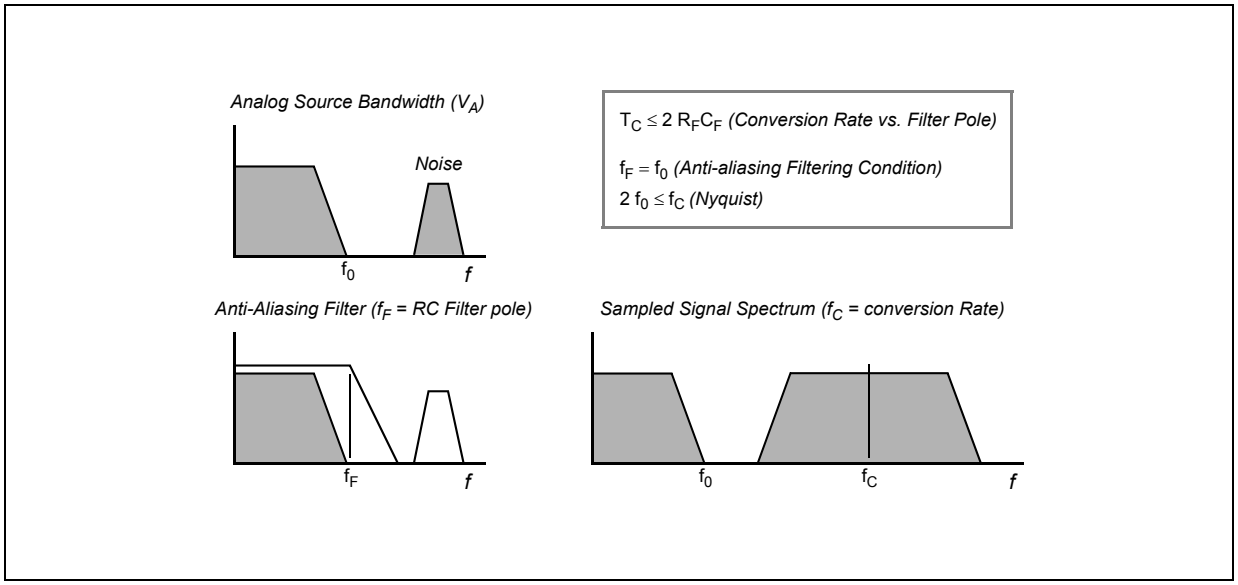


Figure 16. Spectral representation of input signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive Equation 11 between the ideal and real sampled voltage on C_S:

Eqn. 11

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Eqn. 12

$$C_F > 2048 \bullet C_S$$

3.14.2 ADC conversion characteristics

Table 28. ADC conversion characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{CK}	SR	—	ADC clock frequency (depends on ADC configuration) (The duty cycle depends on ADC clock[2] frequency)	—	3[3]	—	60	MHz
f_s	SR	—	Sampling frequency	—	—	—	1.53	MHz
t_s	—	D	Sampling time[4]	f_{ADC} = 20 MHz, INPSAMP = 3	125	—	—	ns
				f_{ADC} = 9 MHz, INPSAMP = 255	—	—	28.2	µs
t_c	—	P	Conversion time[5]	f_{ADC} = 20 MHz[6], INPCMP = 1	0.650	—	—	µs
t_{ADC_PU}	SR	—	ADC power-up delay (time needed for ADC to settle exiting from software power down; PWDN bit = 0)	—	—	—	1.5	µs
C_S[7]	—	D	ADC input sampling capacitance	—	—	—	2.5	pF
C_{P1}[7]	—	D	ADC input pin capacitance 1	—	—	—	3	pF
C_{P2}[7]	—	D	ADC input pin capacitance 2	—	—	—	1	pF
R_{SW}[7]	—	D	Internal resistance of analog source	$V_{DD_HV_ADC0}$ = 5 V ± 10%	—	—	0.6	kΩ
				$V_{DD_HV_ADC0}$ = 3.3 V ± 10%	—	—	3	kΩ
R_{AD}[7]	—	D	Internal resistance of analog source	—	—	—	2	kΩ
I_{INJ}	—	T	Input current injection	Current injection on one ADC input, different from the converted one. Remains within TUE specification	–5	—	5	mA
INL	CC	P	Integral non-linearity	No overload	–1.5	—	1.5	LSB
DNL	CC	P	Differential non-linearity	No overload	–1.0	—	1.0	LSB
E_O	CC	T	Offset error	—	—	±1	—	LSB
E_G	CC	T	Gain error	—	—	±1	—	LSB
TUE	CC	P	Total unadjusted error without current injection	—	–2.5	—	2.5	LSB
TUE	CC	T	Total unadjusted error with current injection	—	–3	—	3	LSB

1 V_{DD} = 3.3 V to 3.6 V / 4.5 V to 5.5 V, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified and analog input voltage from $V_{SS_HV_ADC0}$ to $V_{DD_HV_ADC0}$.

2 AD_clk clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.

3 When configured to allow 60 MHz ADC, the minimum ADC clock speed is 9 MHz, below which the precision is lost.

4 During the sampling time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_s. After the end of the sampling time t_s, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_s depend on programming.

5 This parameter includes the sampling time t_s.

6 20 MHz ADC clock. Specific prescaler is programmed on MC_PLL_CLK to provide 20 MHz clock to the ADC.
7 See Figure 14.

3.15 Flash memory electrical characteristics

3.15.1 Program/Erase characteristics

Table 29. Program and erase specifications

Symbol	C	Parameter	Value				Unit
			Min	Typ[1]	Initial Max[2]	Max[3]	
$T_{wprogram}$	P	Word Program Time for data flash memory[4]	—	30	70	500	µs
$T_{dwprogram}$	P	Double Word Program Time for code flash memory[4]	—	22	50	500	µs
T_{BKPRG}	P	Bank Program (256 KB)[4,5]	—	0.73	0.83	17.5	s
	P	Bank Program (64 KB)[4,5]	—	0.49	1.2	4.1	s
$T_{16kpperase}$	P	16 KB Block Pre-program and Erase Time for code flash memory	—	300	500	5000	ms
		16 KB Block Pre-program and Erase Time for data flash memory	—	700	800	5000	
$T_{32kpperase}$	P	32 KB Block Pre-program and Erase Time	—	400	600	5000	ms
$T_{128kpperase}$	P	128 KB Block Pre-program and Erase Time	—	800	1300	7500	ms
t_{ESRT}	P	Program and erase specifications[6]	10	—	—	—	ms

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.
3 The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
4 Actual hardware programming times. This does not include software overhead.
5 Typical Bank programming time assumes that all cells are programmed in a single pulse. In reality some cells will require more than one pulse, adding a small overhead to total bank programming time (see “Initial Max” column).
6 Time between erase suspend resume and next erase suspend request.

Table 30. Flash memory module life

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Typ	
P/E	C	Number of program/erase cycles per block for 16 KB blocks over the operating temperature range (T_J)	—	100,000	—	cycles
P/E	C	Number of program/erase cycles per block for 32 KB blocks over the operating temperature range (T_J)	—	10,000	100,000	cycles
P/E	C	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	—	1,000	100,000	cycles
Retention	C	Minimum data retention at 85 °C average ambient temperature[1]	Blocks with 0–1,000 P/E cycles	20	—	years
			Blocks with 10,000 P/E cycles	10	—	years
			Blocks with 100,000 P/E cycles	5	—	years

1 Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

Table 31. Flash memory read access timing

Symbol	C	Parameter	Conditions[1]	Max value	Unit
f_{max}	C	Maximum working frequency for code flash memory at given number of wait states in worst conditions	2 wait states	66	MHz
			0 wait states	18	
f_{max}	C	Maximum working frequency for data flash memory at given number of wait states in worst conditions	8 wait states	66	MHz

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

3.15.2 Flash memory power supply DC characteristics

Table 32 shows the power supply DC characteristics on external supply.

Table 32. Flash memory power supply DC electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
I_{FLPW}	CC	D	Sum of the current consumption on $V_{DD_HV_IOx}$ and $V_{DD_LV_CORx}$ during low-power mode	Code flash memory	—	—	900	µA
I_{FPWD}	CC	D	Sum of the current consumption on $V_{DD_HV_IOx}$ and $V_{DD_LV_CORx}$ during power-down mode	Code flash memory	—	—	150	µA
				Data flash memory	—	—	150	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

3.15.3 Start-up/Switch-off timings

Table 33. Start-up time/Switch-off time

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
$T_{FLARSTEXIT}$	CC	T	Delay for Flash module to exit reset mode	Code flash memory	—	—	125	µs
		T		Data flash memory	—	—	125	
$T_{FLALPEXIT}$	CC	D	Delay for Flash module to exit low-power mode	Code flash memory	—	—	0.5	
$T_{FLAPDEXIT}$	CC	T	Delay for Flash module to exit power-down mode	Code flash memory	—	—	30	
		T		Data flash memory	—	—	30	
$T_{FLALPENTRY}$	CC	D	Delay for Flash module to enter low-power mode	Code flash memory	—	—	0.5	

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

3.16 AC specifications

3.16.1 Pad AC specifications

Table 34. Output pin transition times

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin[2] SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
		T		C_L = 50 pF		—	—	50	
		D		C_L = 100 pF		—	—	75	
t_{tr}	CC	D	Output transition time output pin[2] MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	

Table 34. Output pin transition times (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin[2] FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	4	ns
				C_L = 50 pF		—	—	6	
				C_L = 100 pF		—	—	12	
				C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	4	
				C_L = 50 pF		—	—	7	
				C_L = 100 pF		—	—	12	
t_{SYM}[3]	CC	T	Symmetric transition time, same drive strength between N and P transistor	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	4	ns
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	5	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified.

2 C_L includes device and package capacitances (C_{PKG} < 5 pF).

3 Transition timing of both positive and negative slopes will differ maximum 50%.

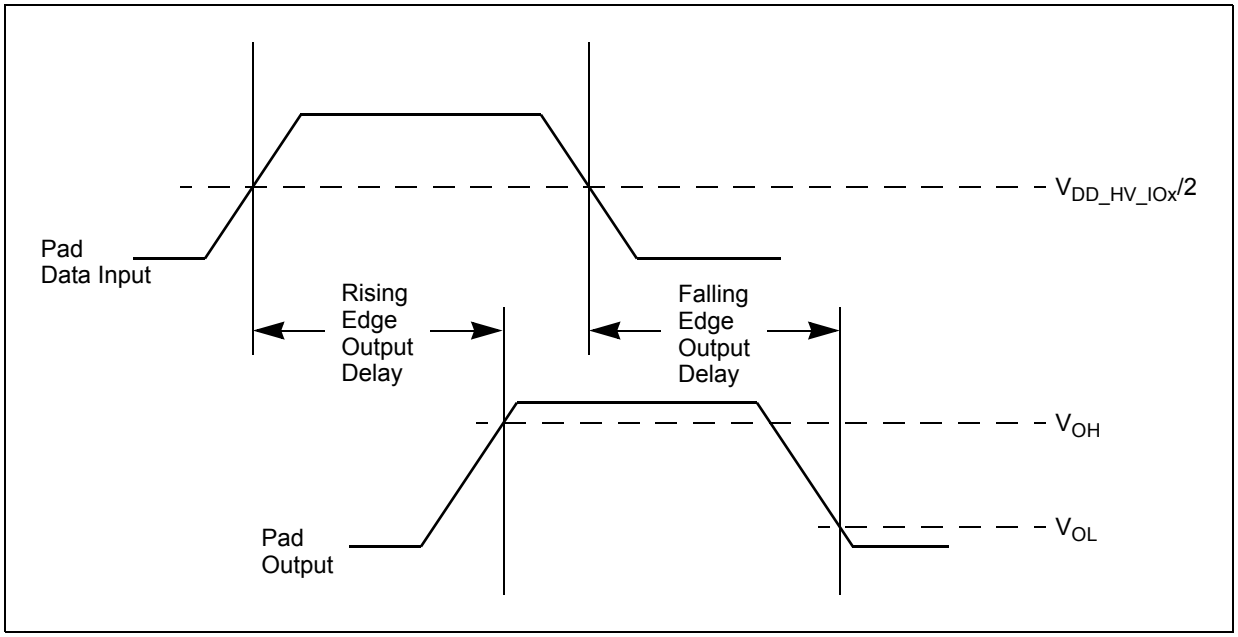


Figure 17. Pad output delay

3.17 AC timing characteristics

3.17.1 $\overline{\text{RESET}}$ pin characteristics

The MPC5602P implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

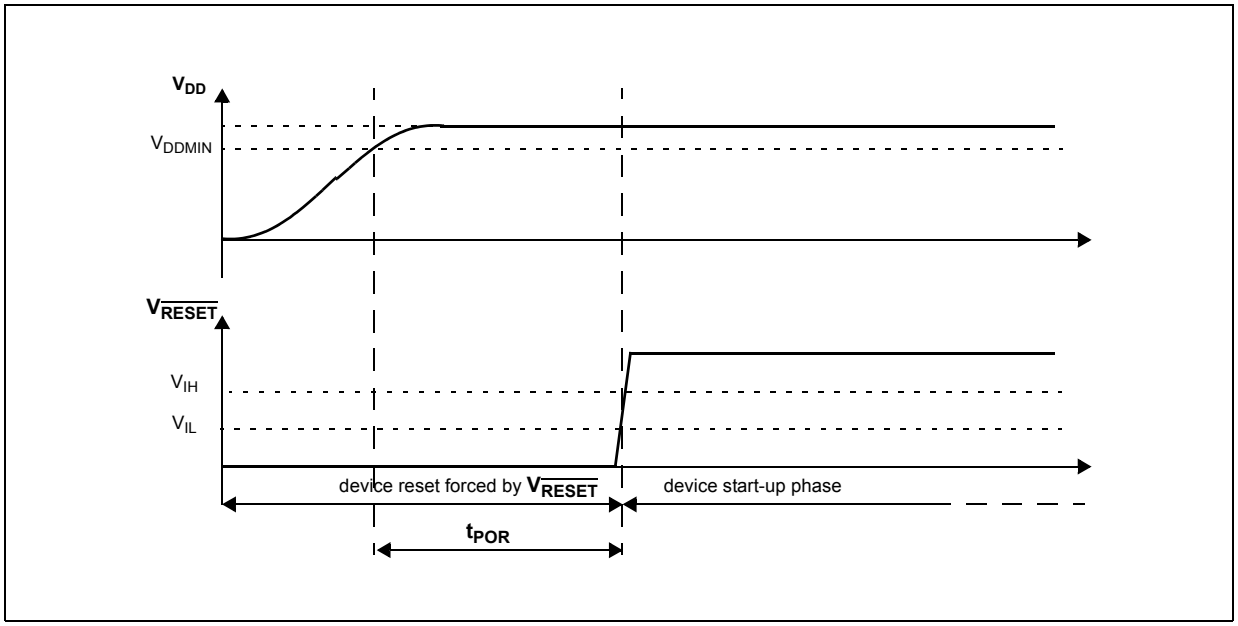


Figure 18. Start-up reset requirements

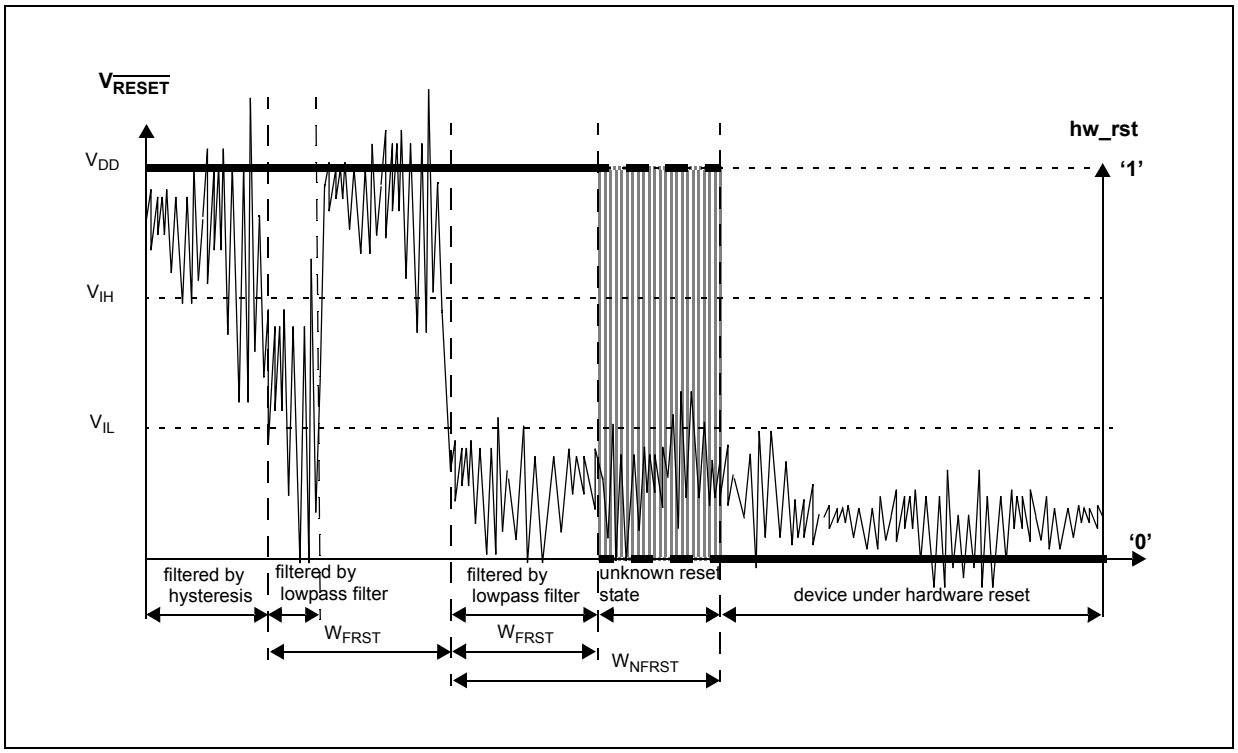


Figure 19. Noise filtering on reset signal

Table 35. $\overline{\text{RESET}}$ electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	V_{DD} + 0.4	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	—	–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
				Push Pull, I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	—	—	$0.1V_{DD}$	
				Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
t_{tr}	CC	D	Output transition time output pin[4] MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
				C_L = 100 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
				C_L = 100 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	500	—	—	ns
t_{POR}	CC	D	Maximum delay before internal reset is released after all V_{DD_HV} reach nominal supply	Monotonic V_{DD_HV} supply ramp	—	—	1	ms
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	—	150	µA
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	10	—	150	
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[5]	10	—	250	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of device reference manual).

[4] C_L includes device and package capacitance (C_{PKG} < 5 pF).

[5] The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.17.2 IEEE 1149.1 interface timing

Table 36. JTAG pin AC electrical characteristics

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{JCYC}	CC	D	TCK cycle time	—	100	—	ns
2	t_{JDC}	CC	D	TCK clock pulse width (measured at $V_{DD_HV_IOx}$/2)	—	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40%–70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	—	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO data valid	—	—	40	ns
7	t_{TDOI}	CC	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	40	—	ns
9	t_{BSDV}	CC	D	TCK falling edge to output valid	—	—	50	ns
10	t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
11	t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	—	50	ns
12	t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
13	t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

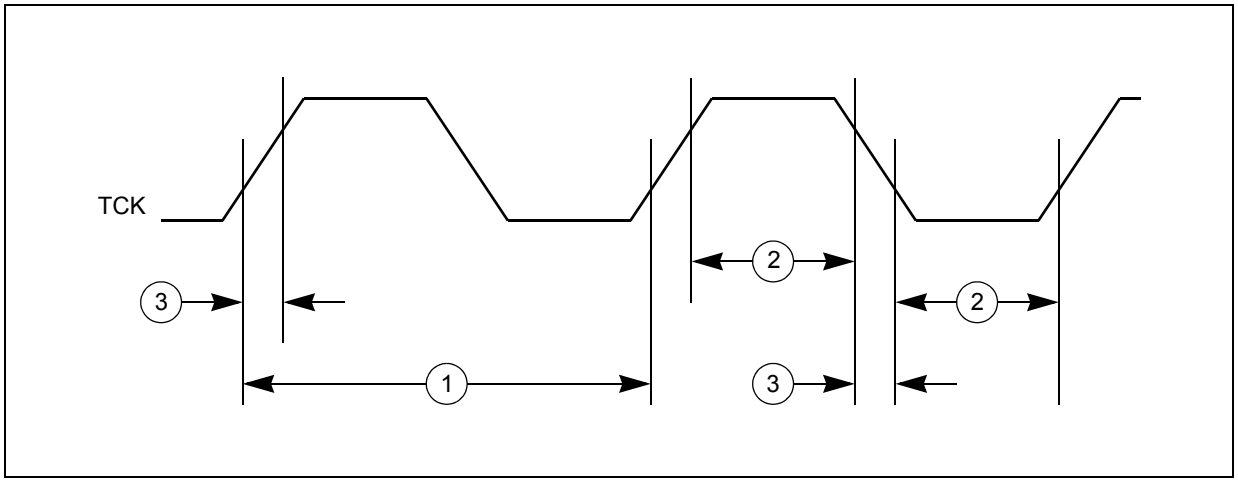


Figure 20. JTAG test clock input timing

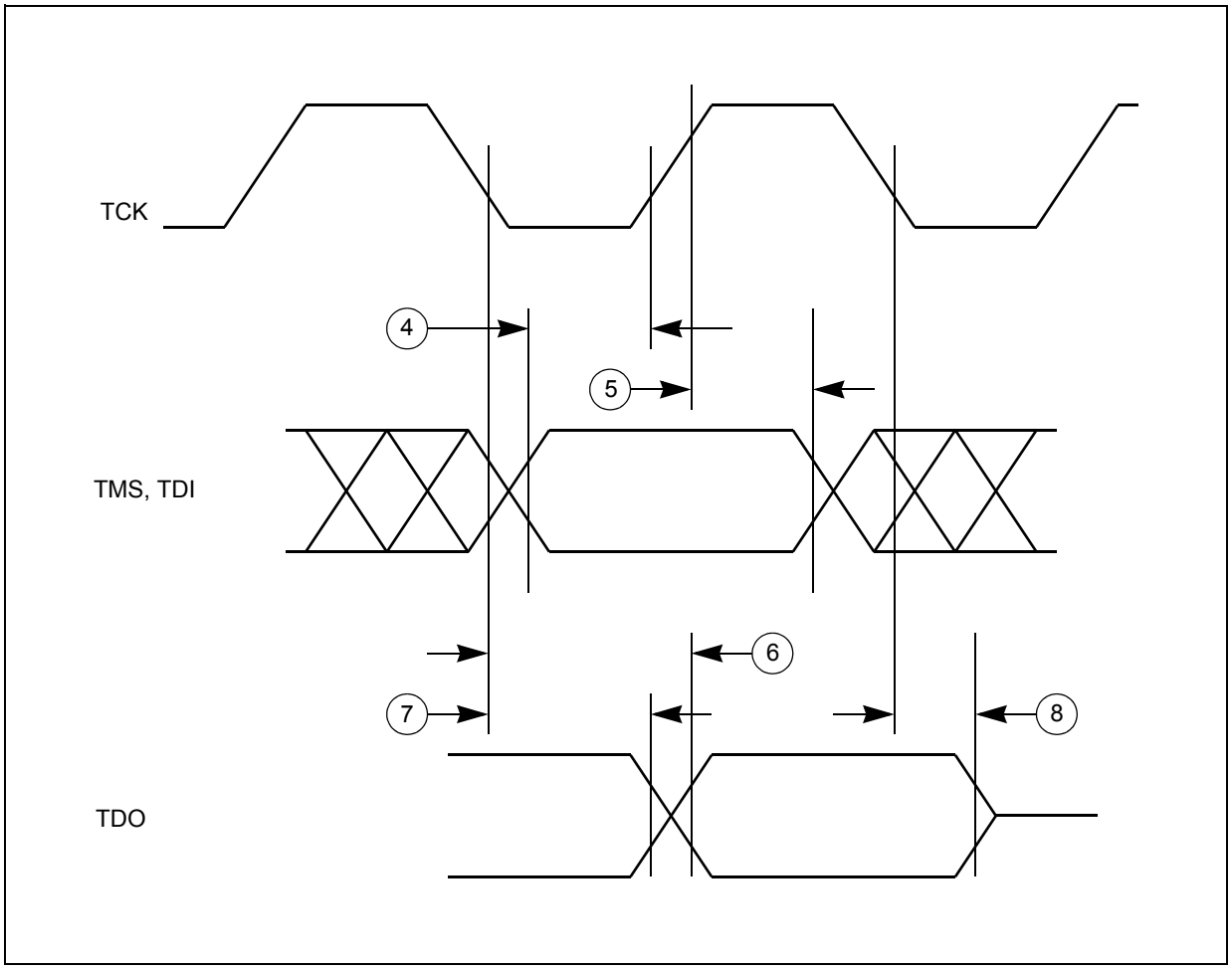


Figure 21. JTAG test access port timing

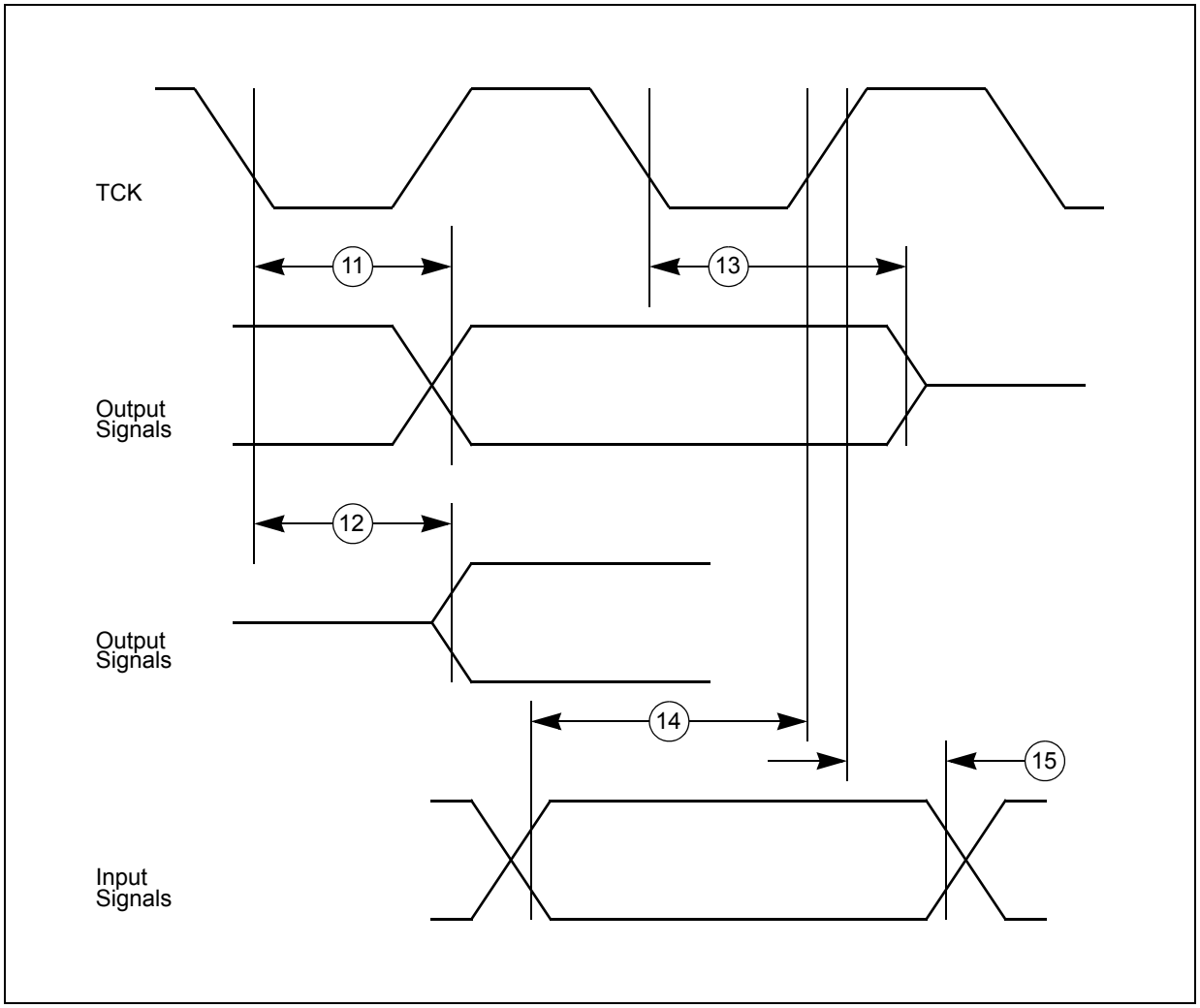


Figure 22. JTAG boundary scan timing

3.17.3 Nexus timing

Table 37. Nexus debug port timing[1]

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{TCYC}	CC	D	TCK cycle time	4[2]	—	—	t_{CYC}
2	t_{NTDIS}	CC	D	TDI data setup time	5	—	—	ns
	t_{NTMSS}	CC	D	TMS data setup time	5	—	—	ns
3	t_{NTDIH}	CC	D	TDI data hold time	25	—	—	ns
	t_{NTMSH}	CC	D	TMS data hold time	25	—	—	ns
4	t_{TDOV}	CC	D	TCK low to TDO data valid	10	—	20	ns
5	t_{TDOI}	CC	D	TCK low to TDO data invalid	—	—	—	ns

1 All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2 Lower frequency is required to be fully compliant to standard.

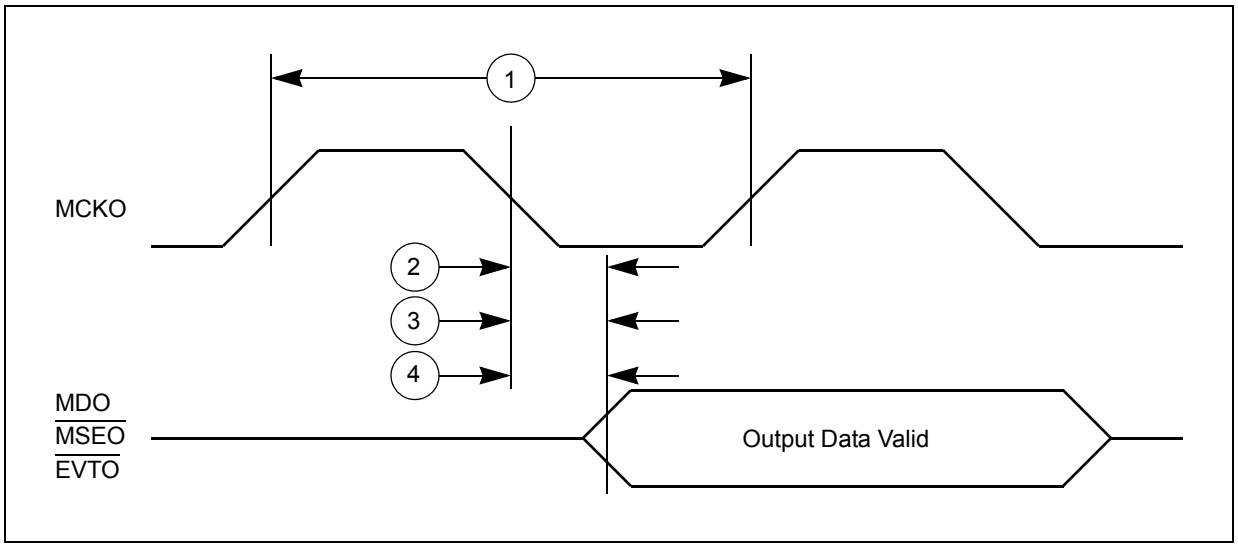


Figure 23. Nexus output timing

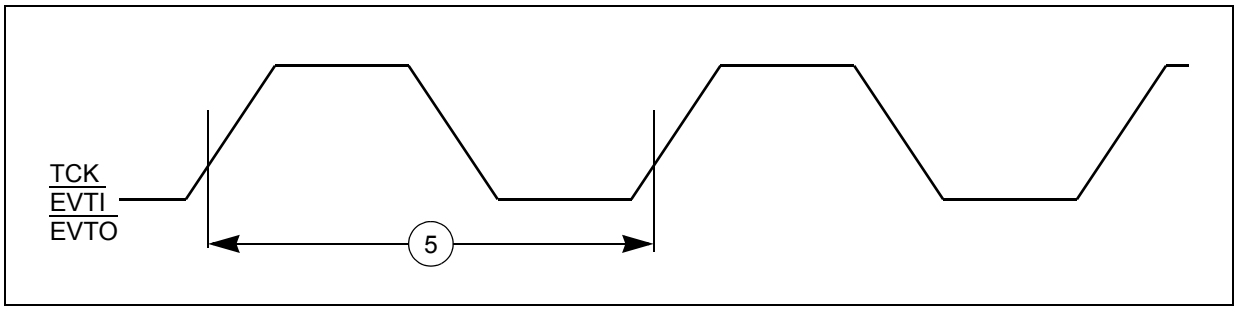


Figure 24. Nexus event trigger and test clock timing

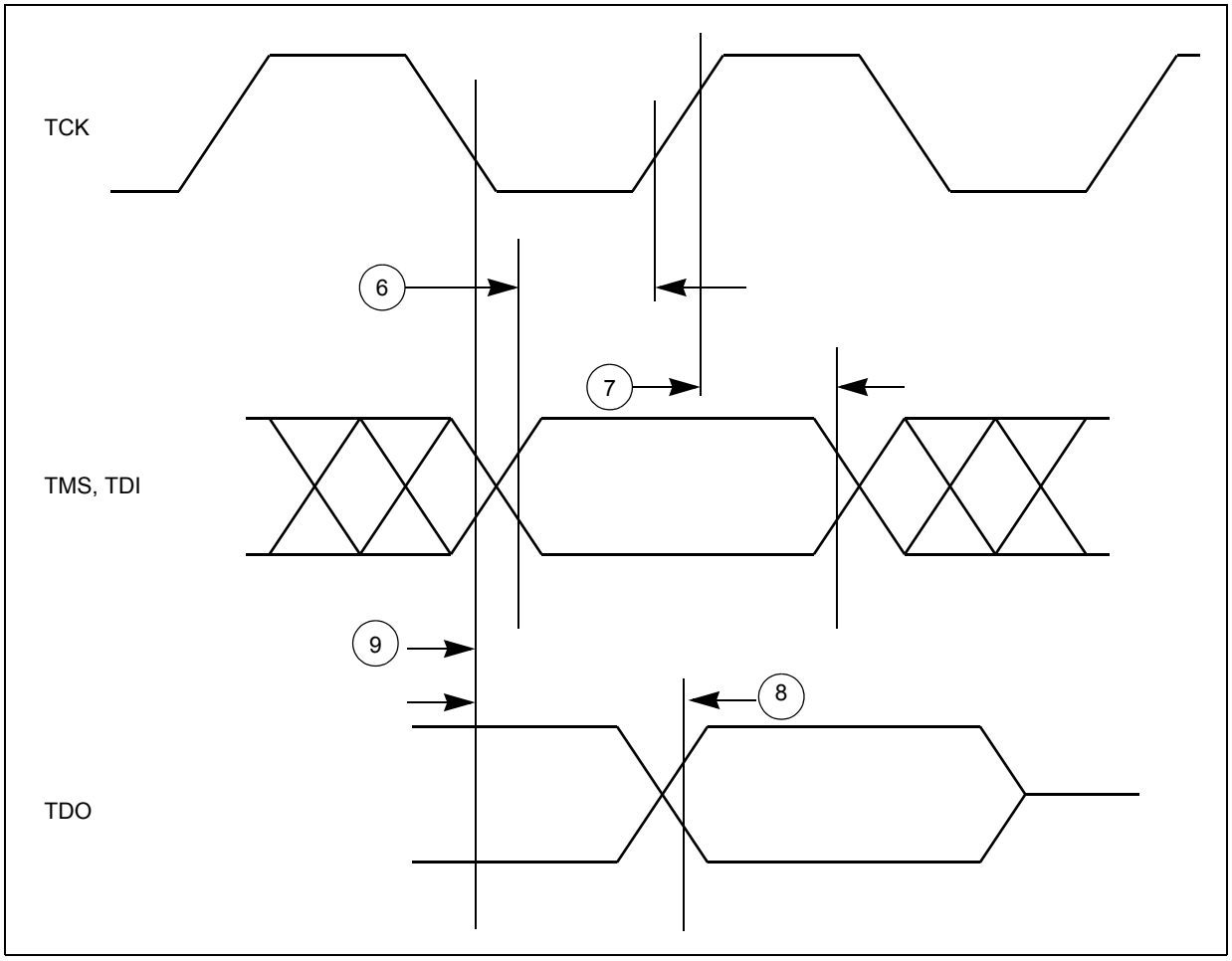


Figure 25. Nexus TDI, TMS, TDO timing

3.17.4 External interrupt timing (IRQ pin)

Table 38. External interrupt timing[1]

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{IPWL}	CC	D	IRQ pulse width low	—	4	—	t_{CYC}
2	t_{IPWH}	CC	D	IRQ pulse width high	—	4	—	t_{CYC}
3	t_{ICYC}	CC	D	IRQ edge to edge time[2]	—	4 + N[3]	—	t_{CYC}

1 IRQ timing specified at f_{SYS} = 64 MHz and $V_{DD_HV_IOx}$ = 3.0 V to 5.5 V, $T_A = T_L$ to T_H, and C_L = 200 pF with SRC = 0b00

2 Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

3 N = ISR time to clear the flag

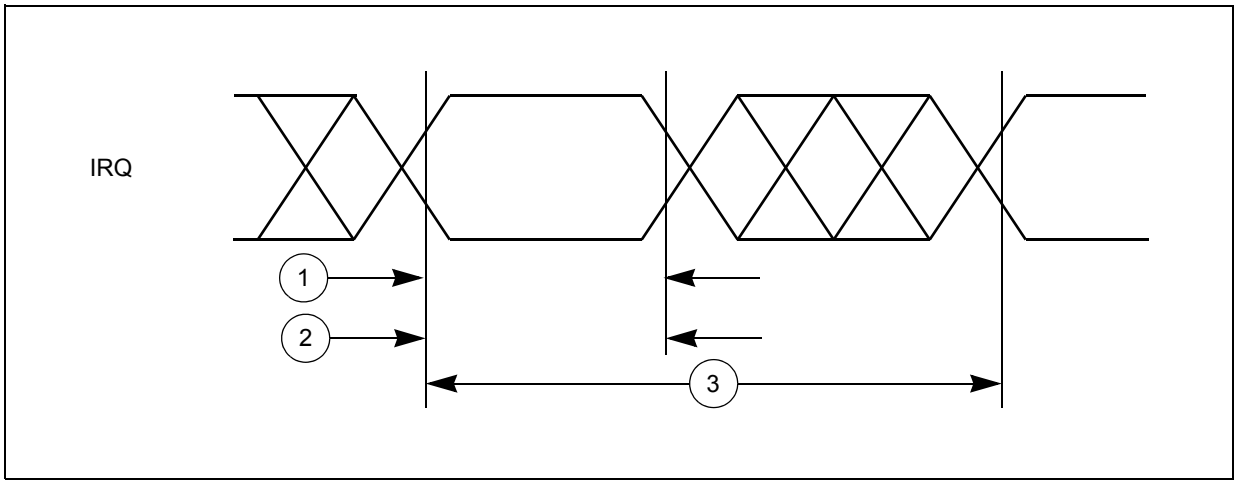


Figure 26. External interrupt timing

3.17.5 DSPI timing

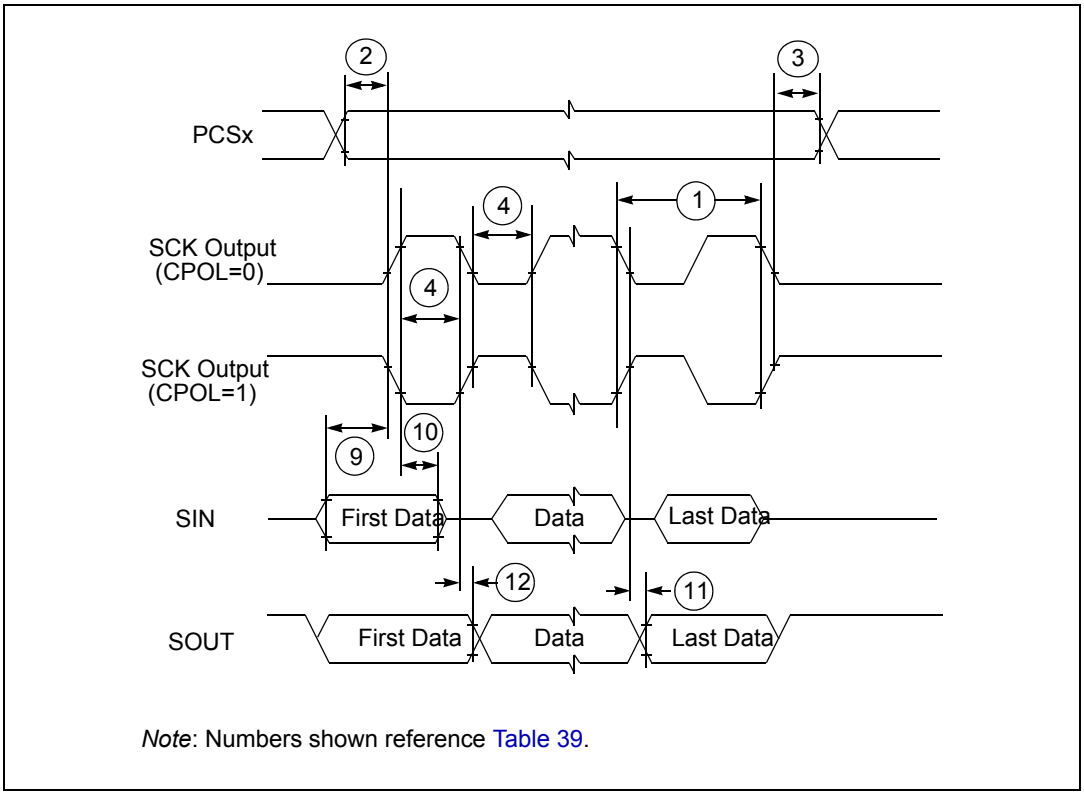
Table 39. DSPI timing[1]

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{SCK}	CC	D	DSPI cycle time	Master (MTFE = 0)	60	—	ns
					Slave (MTFE = 0)	60	—	
2	t_{CSC}	CC	D	CS to SCK delay	—	16	—	ns
3	t_{ASC}	CC	D	After SCK delay	—	26	—	ns
4	t_{SDC}	CC	D	SCK duty cycle	—	0.4 * t_{SCK}	0.6 * t_{SCK}	ns
5	t_A	CC	D	Slave access time	$\overline{SS}$ active to SOUT valid	—	30	ns
6	t_{DIS}	CC	D	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT high impedance or invalid	—	16	ns
7	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time	—	13	—	ns
8	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time	—	13	—	ns
9	t_{SUI}	CC	D	Data setup time for inputs	Master (MTFE = 0)	35	—	ns
					Slave	4	—	
					Master (MTFE = 1, CPHA = 0)	35	—	
					Master (MTFE = 1, CPHA = 1)	35	—	
10	t_{HI}	CC	D	Data hold time for inputs	Master (MTFE = 0)	–5	—	ns
					Slave	4	—	
					Master (MTFE = 1, CPHA = 0)	11	—	
					Master (MTFE = 1, CPHA = 1)	–5	—	

Table 39. DSPI timing[1] (continued)

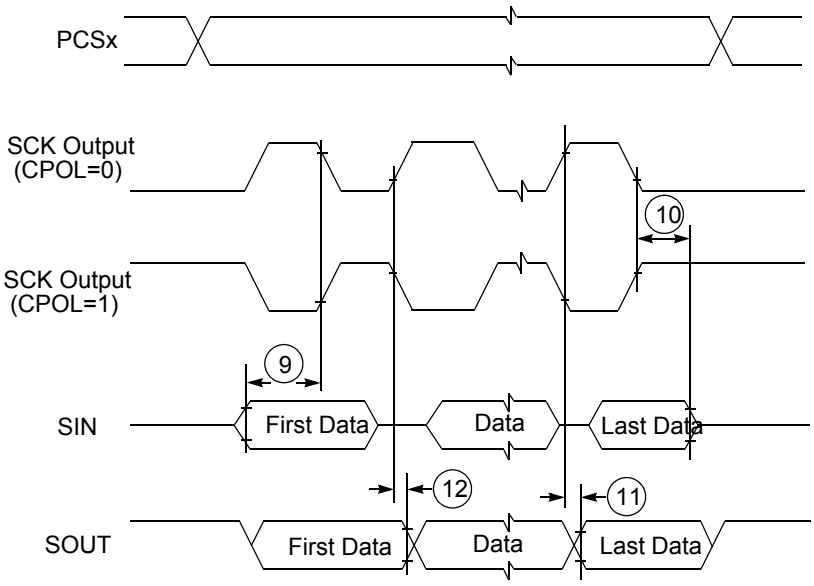
No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
11	t_{SUO}	CC	D	Data valid (after SCK edge)	Master (MTFE = 0)	—	12	ns
					Slave	—	36	
					Master (MTFE = 1, CPHA = 0)	—	12	
					Master (MTFE = 1, CPHA = 1)	—	12	
12	t_{HO}	CC	D	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
					Slave	6	—	
					Master (MTFE = 1, CPHA = 0)	6	—	
					Master (MTFE = 1, CPHA = 1)	–2	—	

1 All timing are provided with 50 pF capacitance on output, 1 ns transition time on input signal



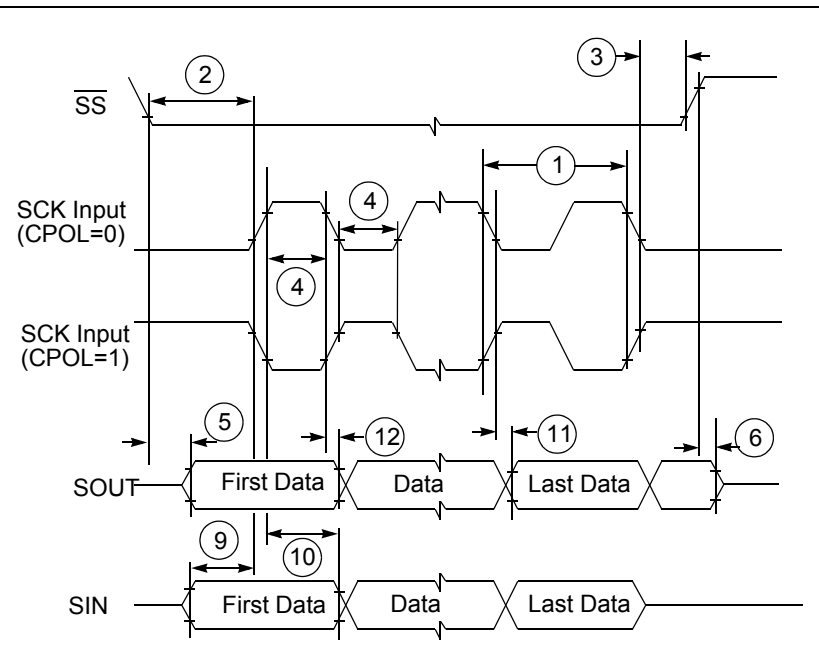
Note: Numbers shown reference Table 39.

Figure 27. DSPI classic SPI timing – Master, CPHA = 0



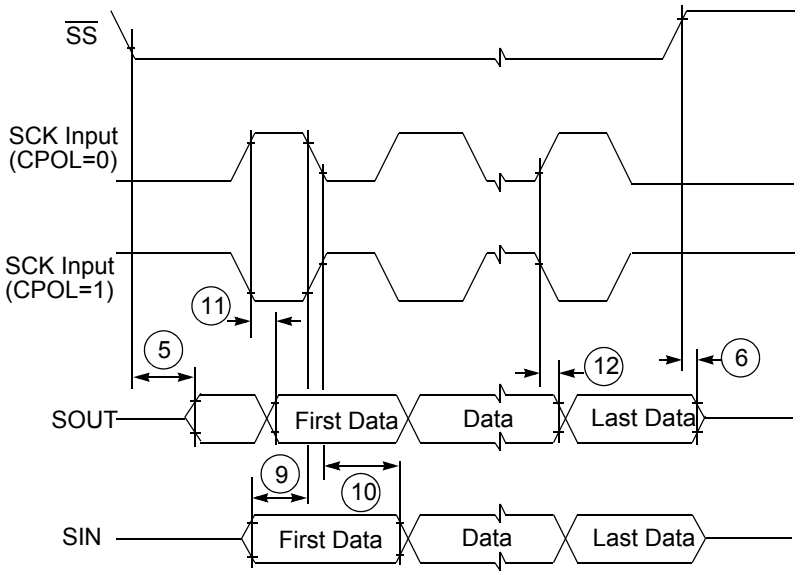
Note: Numbers shown reference Table 39.

Figure 28. DSPI classic SPI timing – Master, CPHA = 1



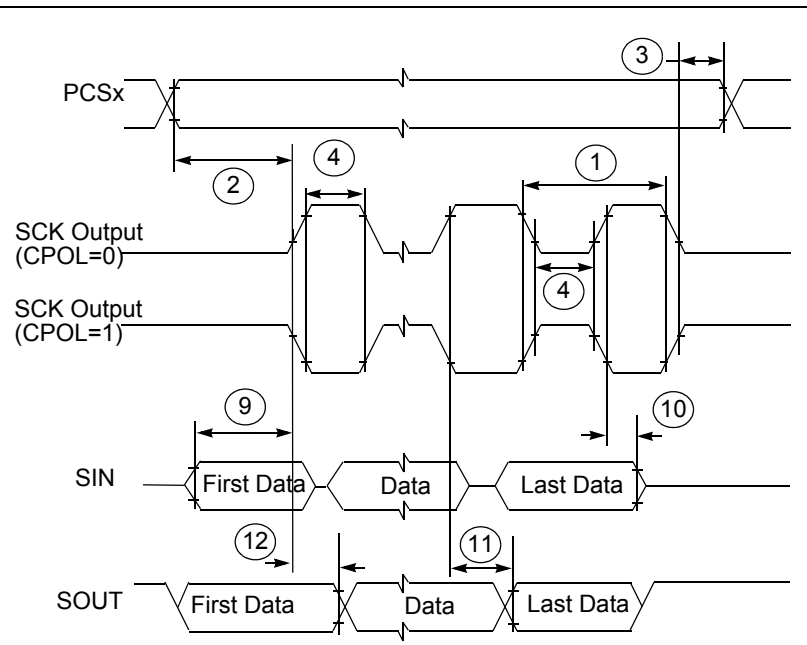
Note: Numbers shown reference Table 39.

Figure 29. DSPI classic SPI timing – Slave, CPHA = 0



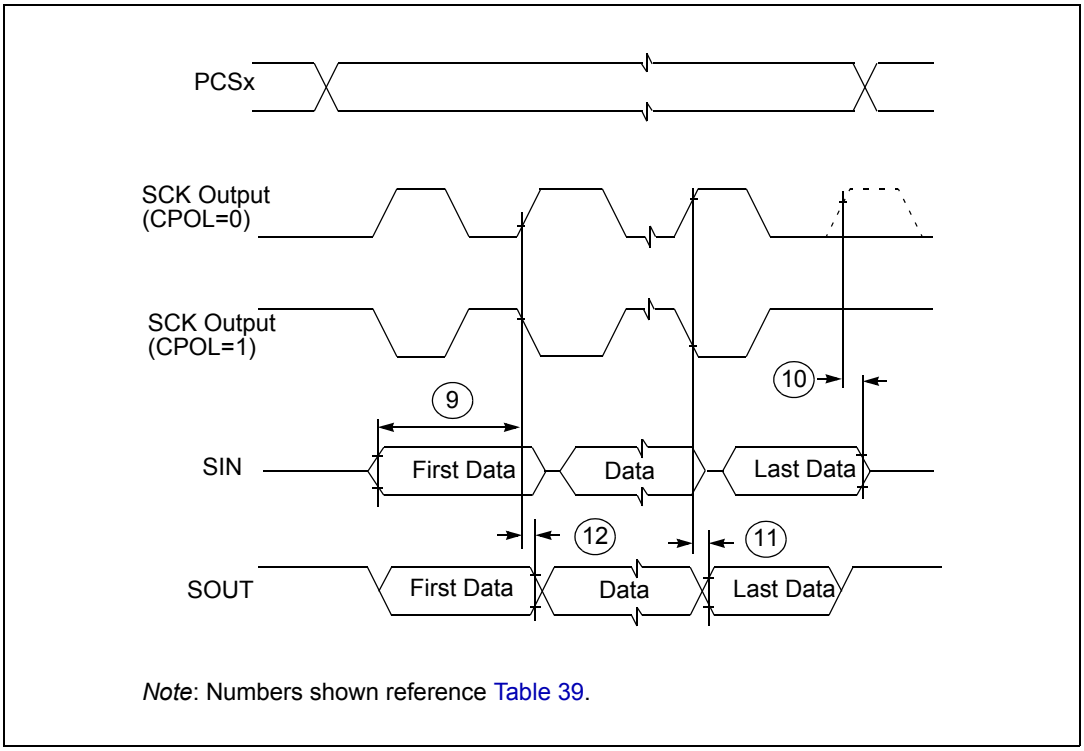
Note: Numbers shown reference Table 39.

Figure 30. DSPI classic SPI timing – Slave, CPHA = 1



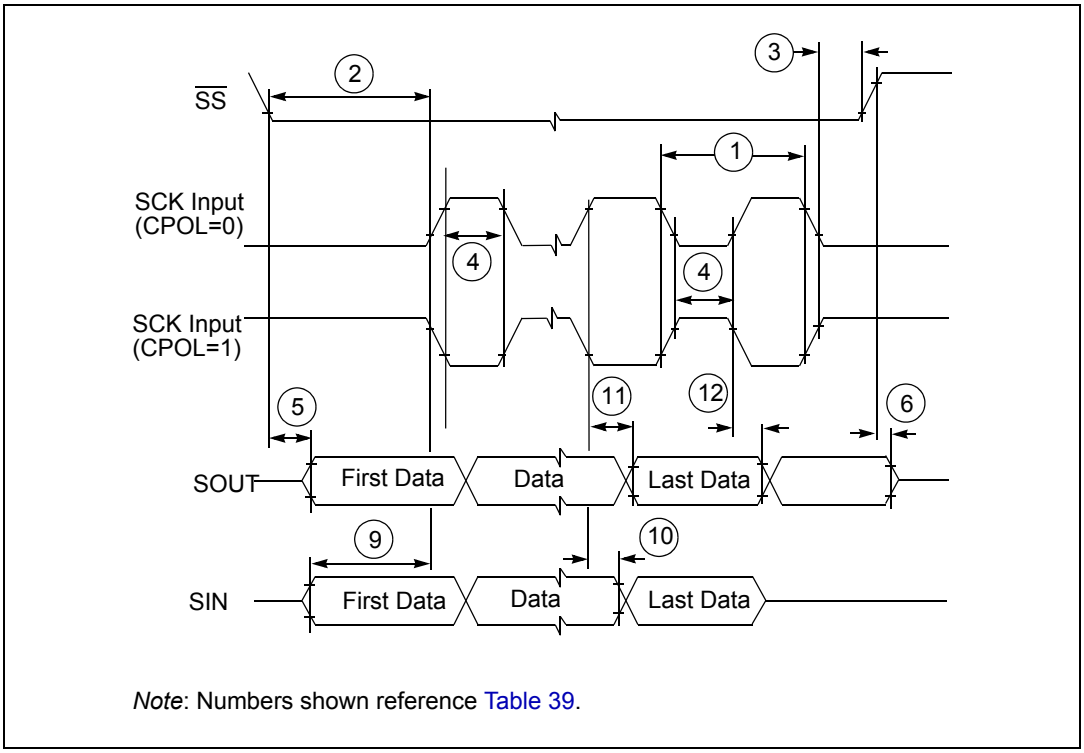
Note: Numbers shown reference Table 39.

Figure 31. DSPI modified transfer format timing – Master, CPHA = 0



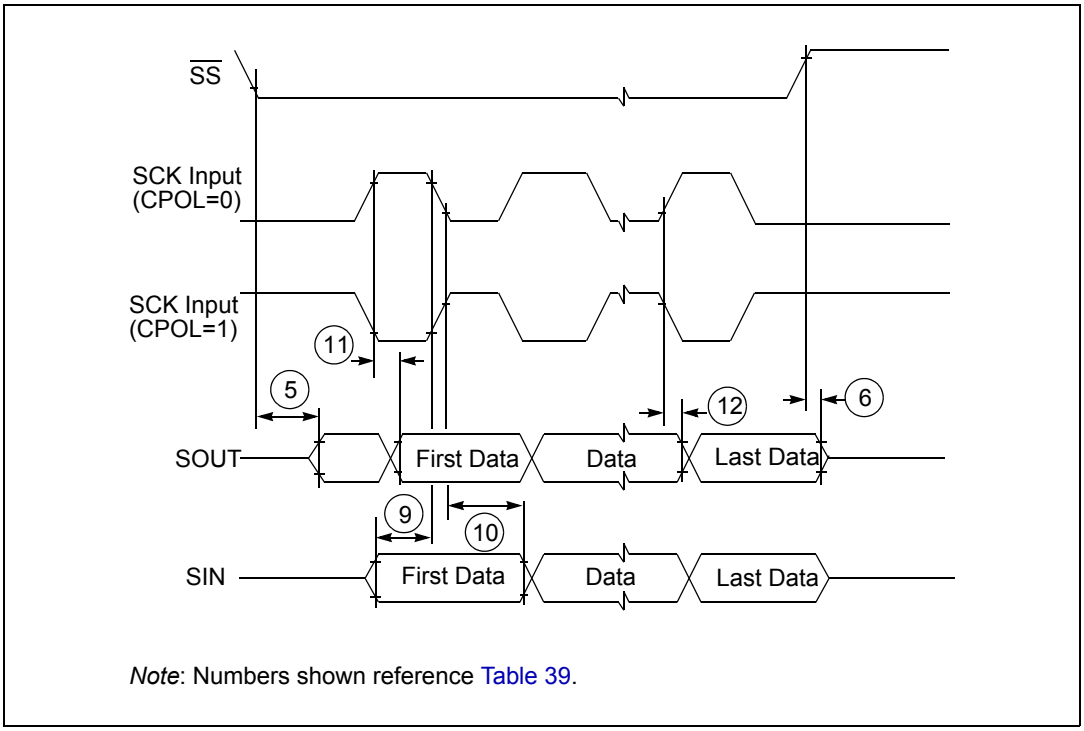
Note: Numbers shown reference Table 39.

Figure 32. DSPI modified transfer format timing – Master, CPHA = 1



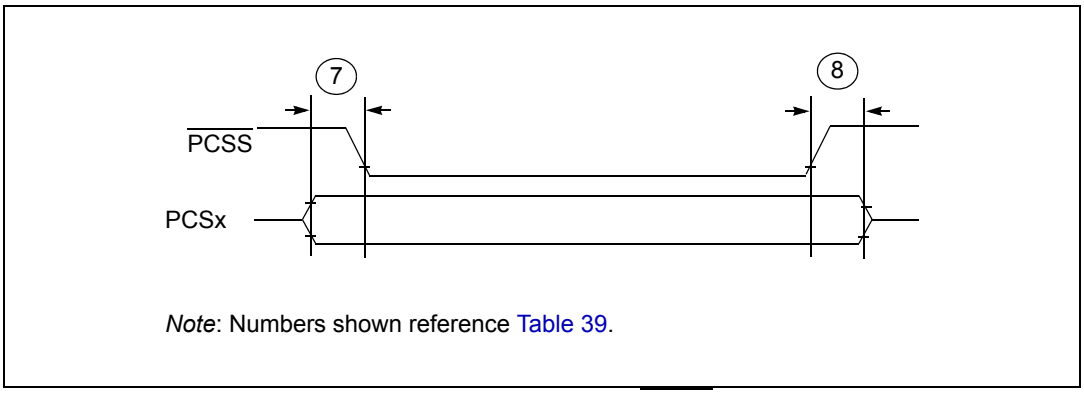
Note: Numbers shown reference Table 39.

Figure 33. DSPI modified transfer format timing – Slave, CPHA = 0



Note: Numbers shown reference Table 39.

Figure 34. DSPI modified transfer format timing – Slave, CPHA = 1



Note: Numbers shown reference Table 39.

Figure 35. DSPI PCS Strobe (PCSS) timing

4 Package characteristics

4.1 Package mechanical data

4.1.1 100 LQFP mechanical outline drawing

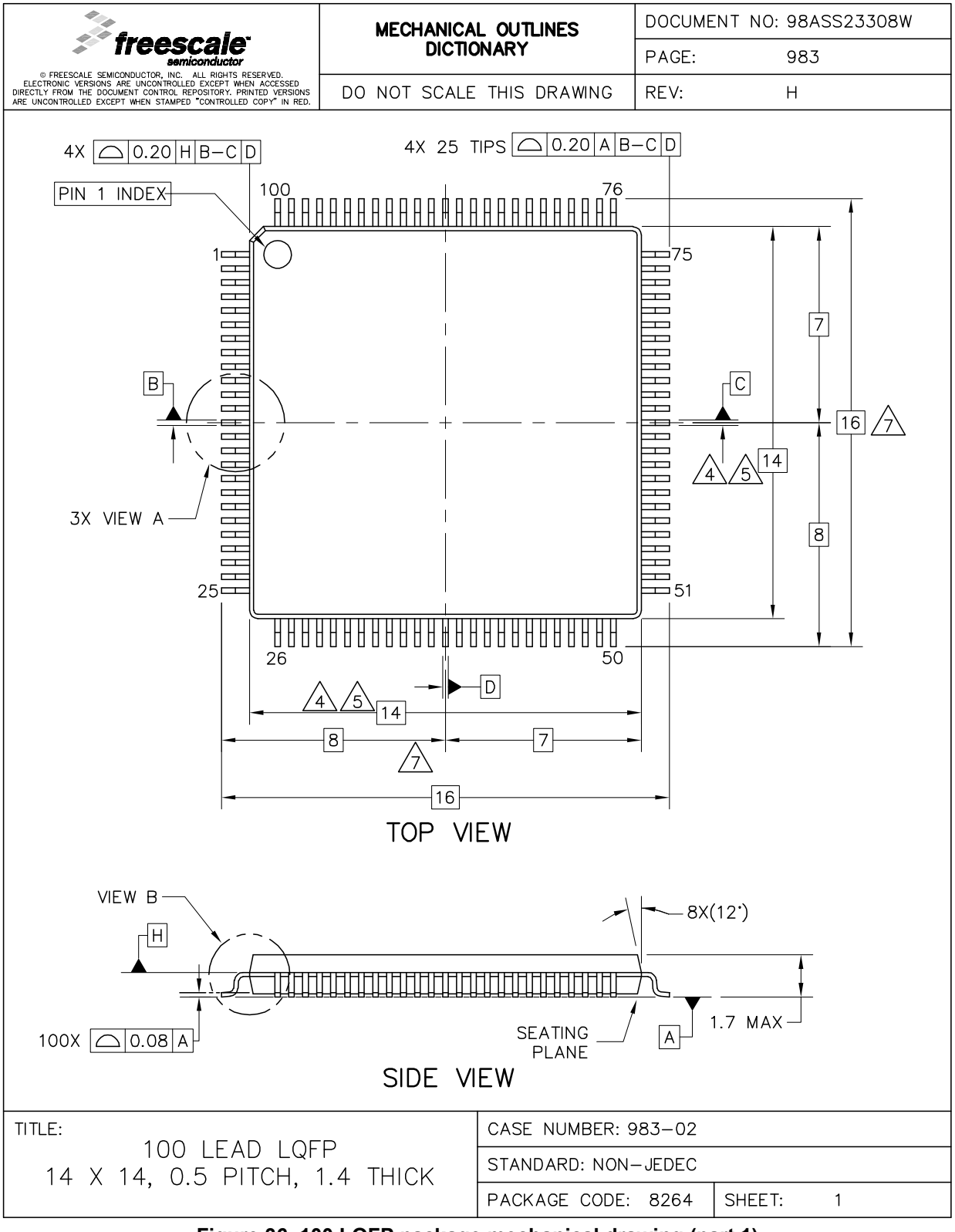


Figure 36. 100 LQFP package mechanical drawing (part 1)

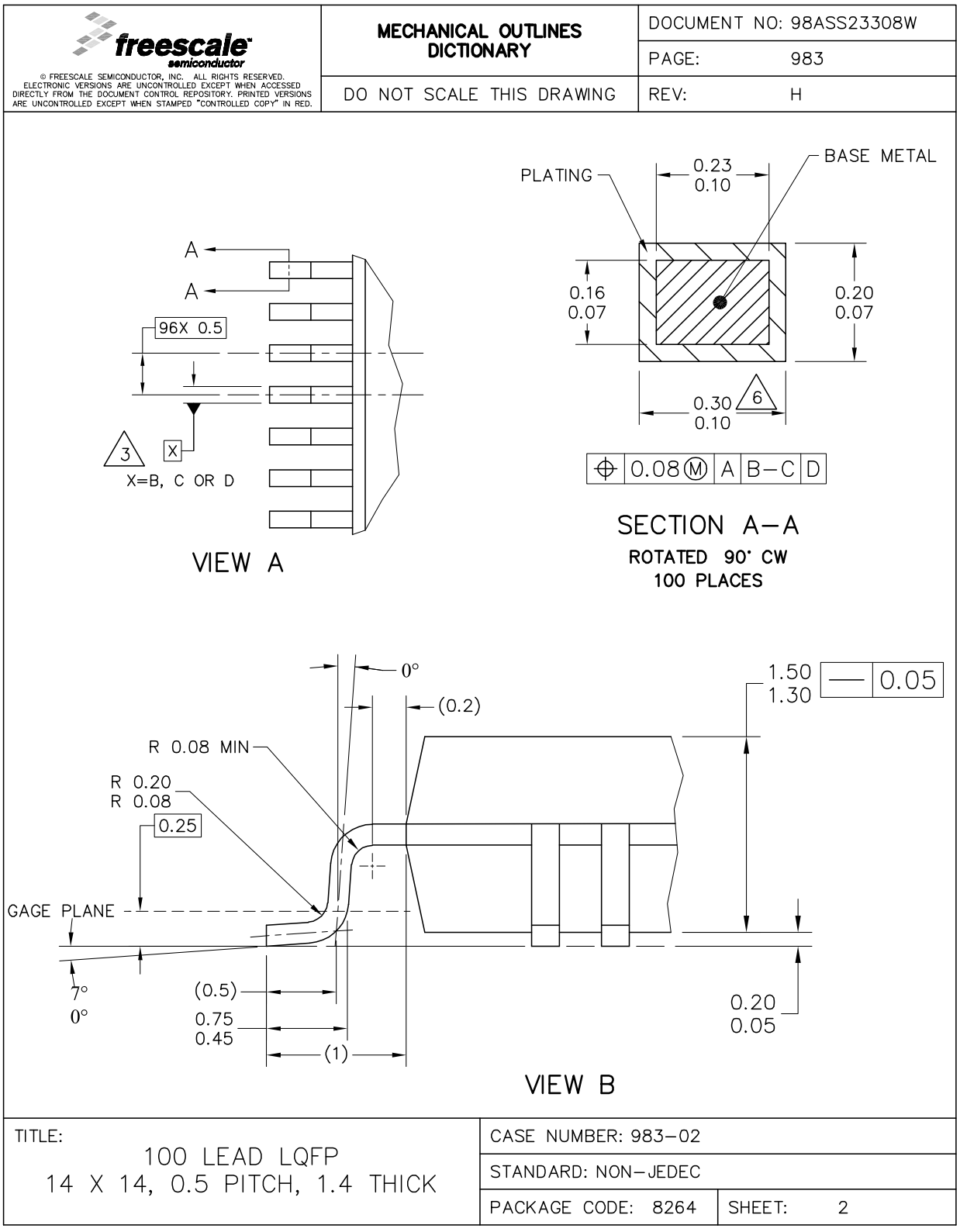


Figure 37. 100 LQFP package mechanical drawing (part 2)

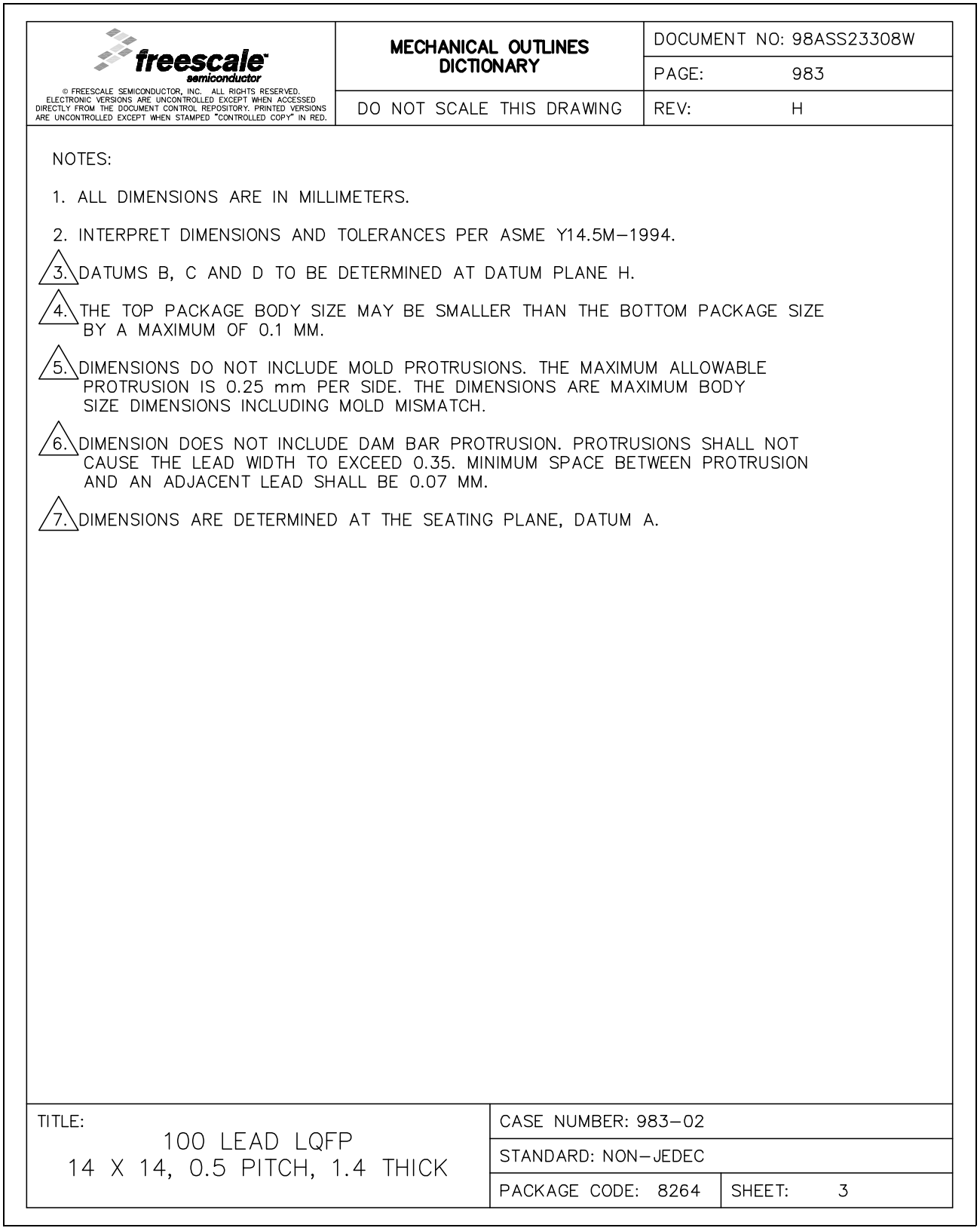


Figure 38. 100 LQFP package mechanical drawing (part 3)

4.1.2 64 LQFP mechanical outline drawing

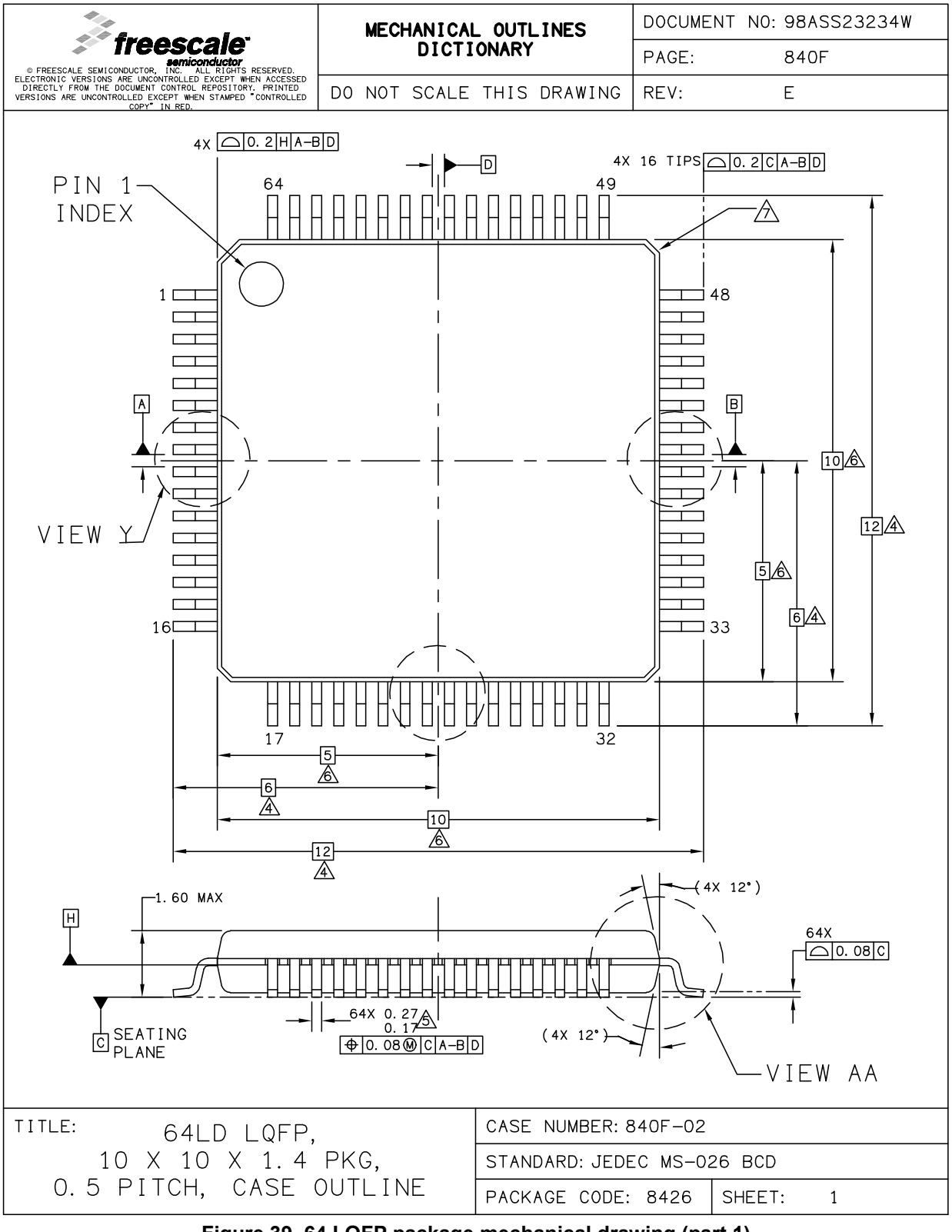


Figure 39. 64 LQFP package mechanical drawing (part 1)

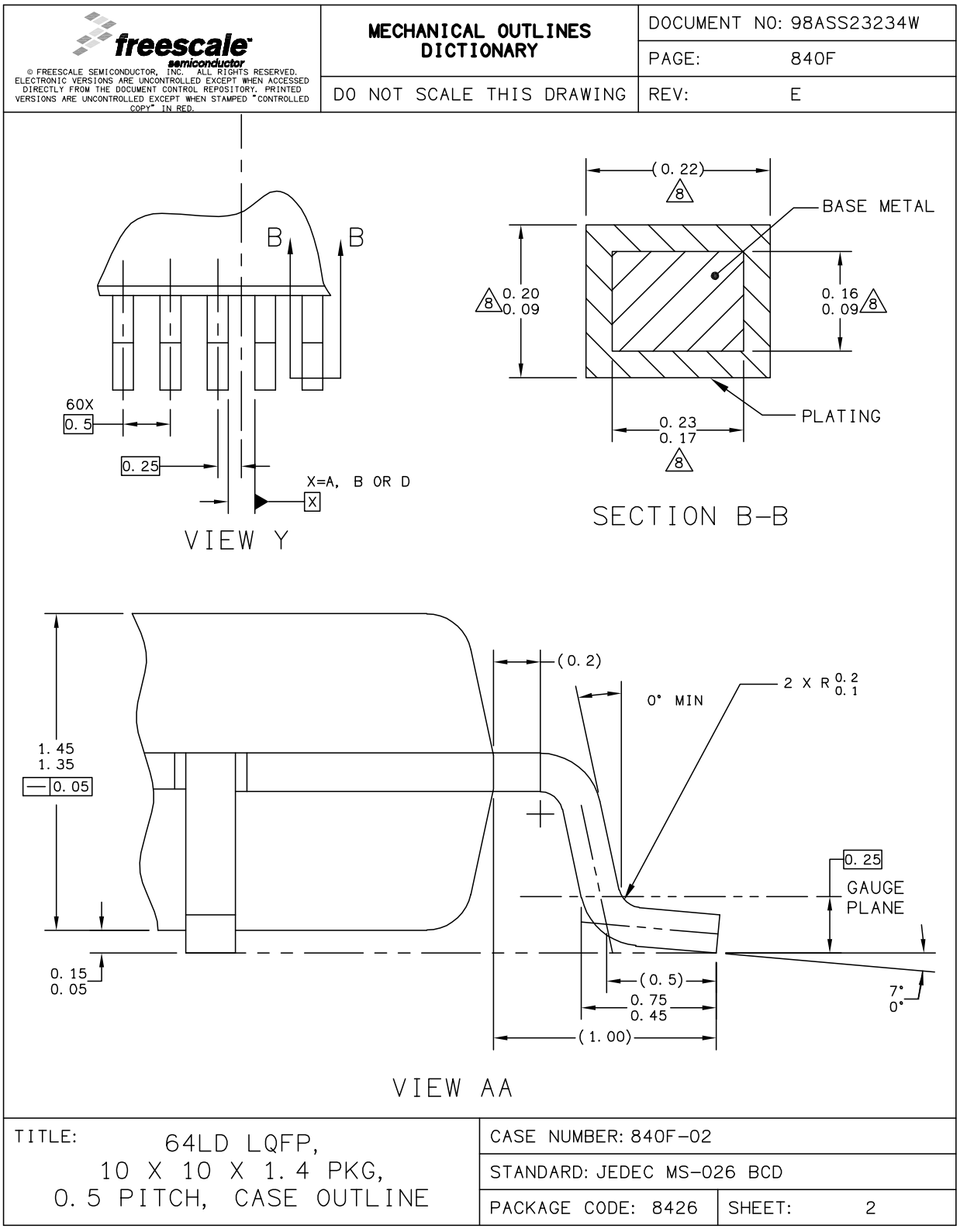


Figure 40. 64LQFP package mechanical drawing (part 2)

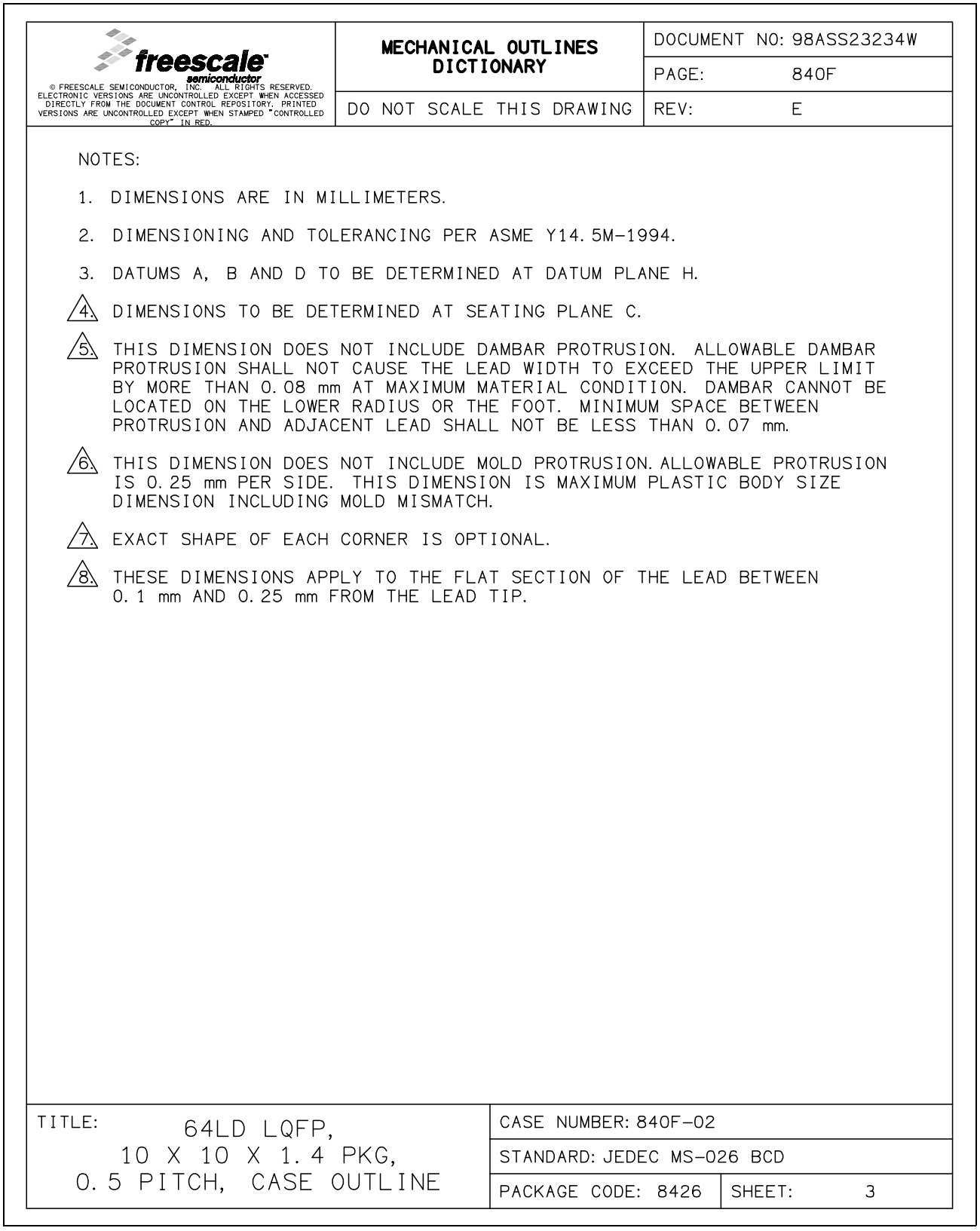
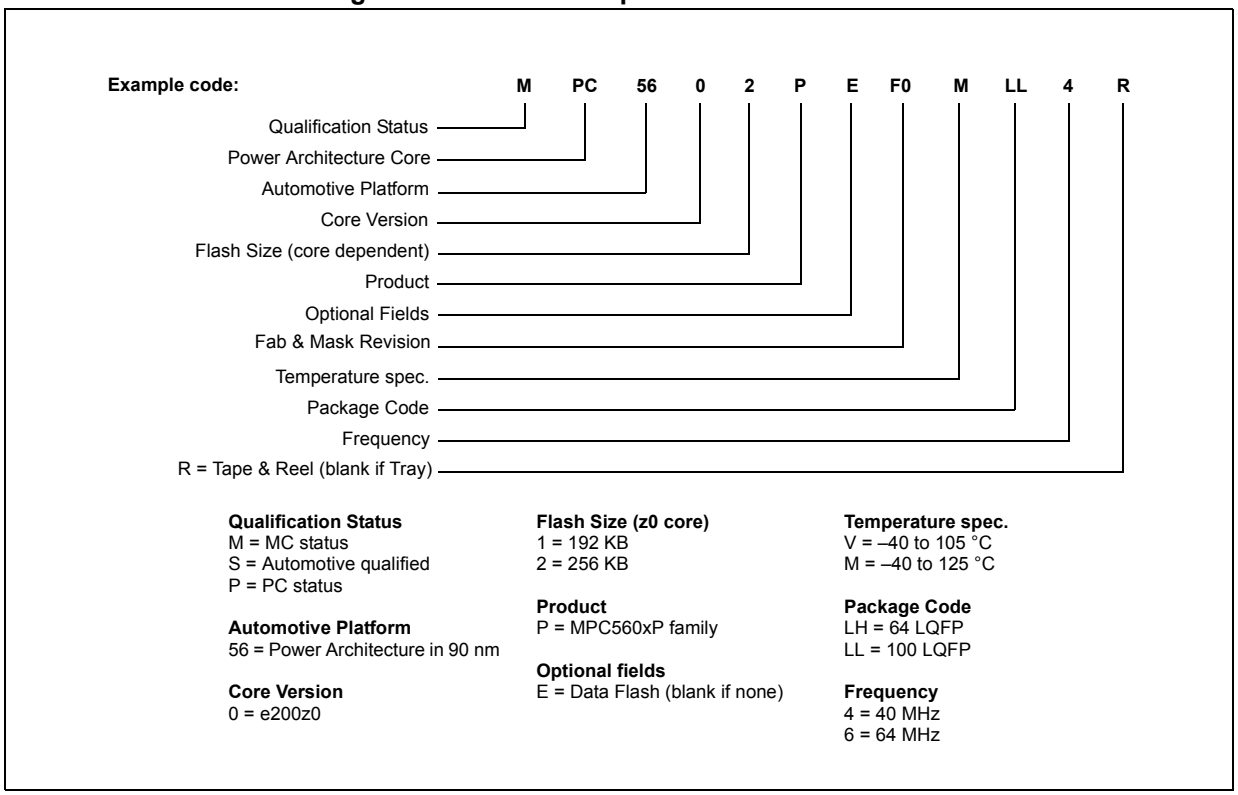


Figure 41. 64LQFP package mechanical drawing (part 3)

5 Ordering information

Figure 42. Commercial product code structure



6 Document revision history

Table 40 summarizes revisions to this document.

Table 40. Revision history

Revision	Date	Description of
1	05 Aug 2009	Initial release.
2	07 Apr 2010	Editorial updates Updated the following items in the “MPC5602P device comparison” table: • The heading • The “SRAM” row • The “FlexCAN” row • The “CTU” row • The “FlexPWM” row • The “LINFlex” row • The “DSPI” row • The “Nexus” row • Deleted the footnote No. 3 Added the “Wakeup unit” block in the MPC5602P block diagram Updated the “Absolute Maximum Ratings“ table Updated the “Recommended operating conditions (5.0 V)“ table Updated the “Recommended operating conditions (3.3 V)“ table Updated the “Thermal characteristics for 100-pin LQFP“ table: • Ψ_{JT}: changed the typical value Updated the “EMI testing specifications“ table: replaced all values in “Level (Max)“ column with TBD Updated the “Electrical characteristics“ section: • Added the “Introduction” section • Added the “Parameter classification“ section • Added the “NVUSRO register“ section • Added the “Power supplies constraints (–0.3 V ≤ $V_{DD_HV_IOx}$ ≤ 6.0 V)” figure • Added the “Independent ADC supply (–0.3 V ≤ $V_{DD_HV_REG}$ ≤ 6.0 V)“ figure • Added the “Power supplies constraints (3.0 V ≤ $V_{DD_HV_IOx}$ ≤ 5.5 V)“ figure • Added the “Independent ADC supply (3.0 V ≤ $V_{DD_HV_REG}$ ≤ 5.5 V)“ figure Updated the “Power management electrical characteristics” section Updated the “Power Up/Down sequencing” section Updated the “DC electrical characteristics“ section • Deleted the “NVUSRO register” section • Updated the “DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)“ section: – Deleted all rows concerning $\overline{\text{RESET}}$ – Deleted “I_{VPP}“ row – Added the max value for C_{IN} • Updated the “DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 0)“ section: – Deleted all rows concerning $\overline{\text{RESET}}$ – Deleted “I_{VPP}“ row – Added the max value for C_{IN} Added the “I/O pad current specification“ section Updated the Orderable part number summarytable.
2 (continued)	07 Apr 2010	Added “Appendix A”

Table 40. Revision history (continued)

Revision	Date	Description of
3	16 Dec 2010	"Introduction" section: • Changed title (was "Overview") • Updated contents "MPC5602P device comparison" table: • Added sentence above table • Removed "FlexRay" row "MPC5602P block diagram": added the following blocks: MC_CGM, MC_ME, MC_PCU, MC_RGM, CRC, and SSCM Added "MPC5602P series block summary" table "Pin muxing" section: removed information on "Symmetric pads" "Electrical characteristics" section: • Updated "Caution" note • Demoted "NVUSRO register" section to subsection of "DC electrical characteristics" section • "NVUSRO register" section: deleted "NVUSRO[WATCHDOG_EN] field description" section Updated "EMI testing specifications" table "Low voltage monitor electrical characteristics" table: updated $V_{MLVDDOK_H}$ max value "DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)" table: removed $_{VOL_SYM}$, and V_{OH_SYM} rows "Supply current (5.0 V, NVUSRO[PAD3V5V] = 0)" table: • $I_{DD_LV_CORE}$, RUN—Maximum mode, 40/64 MHz: updated typ/max values • $I_{DD_LV_CORE}$, RUN—Airbag mode, 40/64 MHz: updated typ/max values • $I_{DD_LV_CORE}$, RUN—Maximum mode, "P" parameter classification: removed • I_{DD_FLASH}: removed rows • I_{DD_ADC}, Maximum mode: updated typ/max values • I_{DD_OSC}: updated max value Updated "DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)" table "Supply current (3.3 V, NVUSRO[PAD3V5V] = 1)" table: • $I_{DD_LV_CORE}$, RUN—Maximum mode, 40/64 MHz: updated typ/max values • $I_{DD_LV_CORE}$, RUN—Airbag mode, 40/64 MHz: updated typ/max values • I_{DD_FLASH}: removed rows • I_{DD_ADC}, Maximum mode: updated typ/max values • I_{DD_OSC}: updated max value Added "I/O consumption" table Removed "I/O weight" table Updated "Main oscillator electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)" table Updated "Main oscillator electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)" table "Input clock characteristics" table: updated f_{CLK} max value "PLLMRFM electrical specifications (V_{DDPLL} = 1.08 V to 1.32 V, $V_{SS} = V_{SSPLL}$ = 0 V, $T_A = T_L$ to T_H)" table: • Updated supply voltage range for V_{DDPLL} in the table title • Updated f_{SCM} max value • Updated C_{JITTER} row • Updated f_{MOD} max value Updated "16 MHz RC oscillator electrical characteristics" table Updated "ADC conversion characteristics" table

Table 40. Revision history (continued)

Revision	Date	Description of
3 (continued)	16 Dec 2010	"Program and erase specifications" table: • $T_{wprogram}$: updated initial max and max values • T_{BKPRG}, 64 KB: updated initial max and max values • added information about "erase time" for Data Flash "Flash module life" table: • P/E, 32 KB: added typ value • P/E, 128 KB: added typ value Replaced "Pad AC specifications (5.0 V, NVUSRO[PAD3V5V] = 0)" and "Pad AC specifications (3.3 V, INVUSRO[PAD3V5V] = 1)" tables with "Output pin transition times" table "JTAG pin AC electrical characteristics" table: • t_{TDOV}: updated max value • t_{TDOHZ}: added min value and removed max value "Nexus debug port timing" table: removed the rows "t_{MCYC}", "t_{MDOV}", "t_{MSEOV}", and "t_{EVTOV}" Updated "External interrupt timing (IRQ pin)" table Updated "FlexCAN timing" table Updated "DSPI timing" table Updated "Ordering information" section

Table 40. Revision history (continued)

Revision	Date	Description of
4	11 May 2011	Editorial and formatting changes throughout Section 1, "Introduction: Reorganized contents MPC5602P block diagram: reorganized blocks above and below peripheral bridge; made arrow going from peripheral bridge to crossbar switch bidirectional Updated Section 1.5, "Feature list: • changed core feature from "64 MHz" to "Up to 64 MHz" • memory organization • moved "16-channel eDMA controller" item to "Interrupts and events" item • LINFlex: changed "2 LINFlex modules" to "Up to 2 LINFlex modules" • DSPI: changed "3 DSPI channels" to "Up to 3 DSPI channels" • ADC: changed "16 input channels" to "Up to 16 input channels" Added Section 1.5, "Feature details 64-pin and 100-pin LQFP pinout diagrams: replaced instances of HV_AD0 with HV_ADC0 System pins: updated "XTAL" and "EXTAL" rows Updated LQFP thermal characteristics Updated EMI testing specifications Section 3.8.1, "Voltage regulator electrical characteristics: removed BCP56 from named BJTs; replaced two configuration diagrams and two electrical characteristics tables with single diagram and single table Voltage regulator electrical characteristics: updated $V_{DD_LV_REGCOR}$ row Low voltage monitor electrical characteristics: updated $V_{MLVDDOK_H}$ max value—was 1.15 V; is 1.145 V Supply current (5.0 V, NVUSRO[PAD3V5V] = 0): changed symbol $I_{DD_LV_CORE}$ to $I_{DD_LV_CORx}$; changed parameter classification from T to P for $I_{DD_LV_CORx}$ RUN—Maximum mode at 64 MHz; added I_{DD_FLASH} characteristics; replaced instances of "Airbag" mode with "Typical mode" Supply current (3.3 V, NVUSRO[PAD3V5V] = 1): changed symbol $I_{DD_LV_CORE}$ to $I_{DD_LV_CORx}$; replaced instances of "Airbag" mode with "Typical mode" DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1): corrected parameter description for V_{OL_F}—was "Fast, high level output voltage"; is "Fast, low level output voltage" Added Section 3.10.4, "Input DC electrical characteristics definition Main oscillator output electrical characteristics tables: replaced instances of EXTAL with XTAL; added load capacitance parameter FMPLL electrical characteristics: updated conditions and table title; removed f_{sys} row; updated $f_{FMPLLOUT}$ values; replaced instances of V_{DDPLL} with $V_{DD_LV_COR0}$; replaced instances of V_{SSPLL} with $V_{SS_LV_COR0}$ 16 MHz RC oscillator electrical characteristics: removed rows $\Delta_{RCMTRIM}$ and $\Delta_{RCMSTEP}$ ADC characteristics and error definitions: updated symbols ADC conversion characteristics: updated symbols; added row t_{ADC_PU} Added Section 3.15.2, "Flash memory power supply DC characteristics Added Section 3.15.3, "Start-up/Switch-off timings Removed section "Generic timing diagrams"
4 (cont'd)	11 May 2011	Updated Start-up reset requirements diagram Removed FlexCAN timing characteristics RESET electrical characteristics: added row for t_{POR} In the range of figures "DSPI Classic SPI Timing — Master, CPHA = 0" to "DSPI PCS Strobe (PCSS) Timing": added note Table A-1: added "DUT", "NPN", and "RISC"

Table 40. Revision history (continued)

Revision	Date	Description of
5	16 Dec 2011	Updated Section 1.5.28, Nexus Development Interface (NDI) Table 1 (MPC5602P device comparison): changed Nexus L1+ with Nexus Class 1 Table 5 (Pin muxing): removed E[0] row Table 7 (Absolute maximum ratings): updated minumum and maximum values for TV_{DD} parameter Section 3.10, DC electrical characteristics: Removed oscillator margin. Removed Section NVUSRO[OSCILLATOR_MARGIN] field description and Table NVUSRO[OSCILLATOR_MARGIN] field description Updated Section 3.8.1, Voltage regulator electrical characteristics Updated Figure 8 (Voltage regulator configuration) Table 14 (Voltage regulator electrical characteristics): added L_{Reg} row, updated condition for C_{DEC1}, C_{DEC2} and C_{DEC3}
6	07 Dec 2012	Table 7 (Absolute maximum ratings): updated TV_{DD} parameter, the minimum value to 3.0 V/s, added note on minimum value, and the maximum value to 0.5 V/µs Table 18 (Supply current (5.0 V, NVUSRO[PAD3V5V] = 0)): added $I_{DD_HV_REG}$ row Table 20 (Supply current (3.3 V, NVUSRO[PAD3V5V] = 1)): added $I_{DD_HV_REG}$ row Updated Section 3.14.1, “Input impedance and ADC accuracy Table 28 (ADC conversion characteristics): renamed “R_{SW1}” in “R_{SW}” Table 29 (Program and erase specifications): added t_{ESRT} row

Appendix A Abbreviations

Table A-1 lists abbreviations used in this document.

Table A-1. Abbreviations

Abbreviation	Meaning
CMOS	Complementary metal–oxide–semiconductor
CPHA	Clock phase
CPOL	Clock polarity
CS	Peripheral chip select
DUT	Device under test
ECC	Error code correction
EVTO	Event out
GPIO	General purpose input / output
MC	Modulus counter
MCKO	Message clock out
MCU	Microcontroller unit
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
NPN	Negative-positive-negative
NVUSRO	Non-volatile user options register
PTF	Post trimming frequency
PWM	Pulse width modulation
RISC	Reduced instruction set computer
SCK	Serial communications clock
SOUT	Serial data out
TBC	To be confirmed
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select

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