

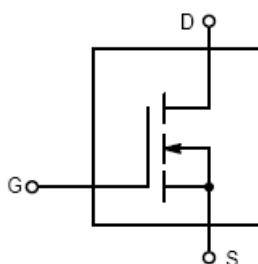
Broadband RF Power MOSFET 600W, to 80MHz, 50V

Rev. V1

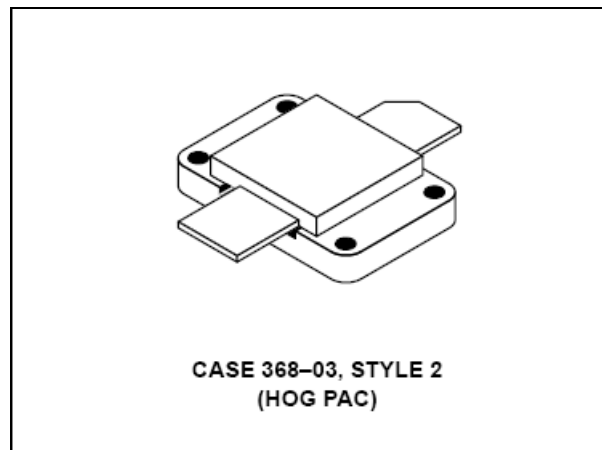
Designed primarily for linear large signal output stages in the 2.0 to 100 MHz frequency range.

N-Channel enhancement mode MOSFET

- Specified 50 volts, 30 MHz characteristics
 - Output power = 600 watts
 - Power gain = 17 dB (typ.)
 - Efficiency = 45% (typ.)



Product Image



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	125	Vdc
Drain-Gate Voltage	V_{DGO}	125	Vdc
Gate-Source Voltage	V_{GS}	± 40	Vdc
Drain Current — Continuous	I_D	60	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	1350 7.7	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.13	$^\circ\text{C/W}$

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

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ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain–Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 100$ mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 50$ V, $V_{GS} = 0$)	I_{DSS}	—	—	20	mAdc
Gate–Body Leakage Current ($V_{GS} = 20$ V, $V_{DS} = 0$)	I_{GSS}	—	—	5.0	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage ($V_{DS} = 10$ V, $I_D = 100$ mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain–Source On–Voltage ($V_{GS} = 10$ V, $I_D = 40$ A)	$V_{DS(on)}$	1.0	3.0	5.0	Vdc
Forward Transconductance ($V_{DS} = 10$ V, $I_D = 20$ A)	g_{fs}	16	20	—	mhos

DYNAMIC CHARACTERISTICS

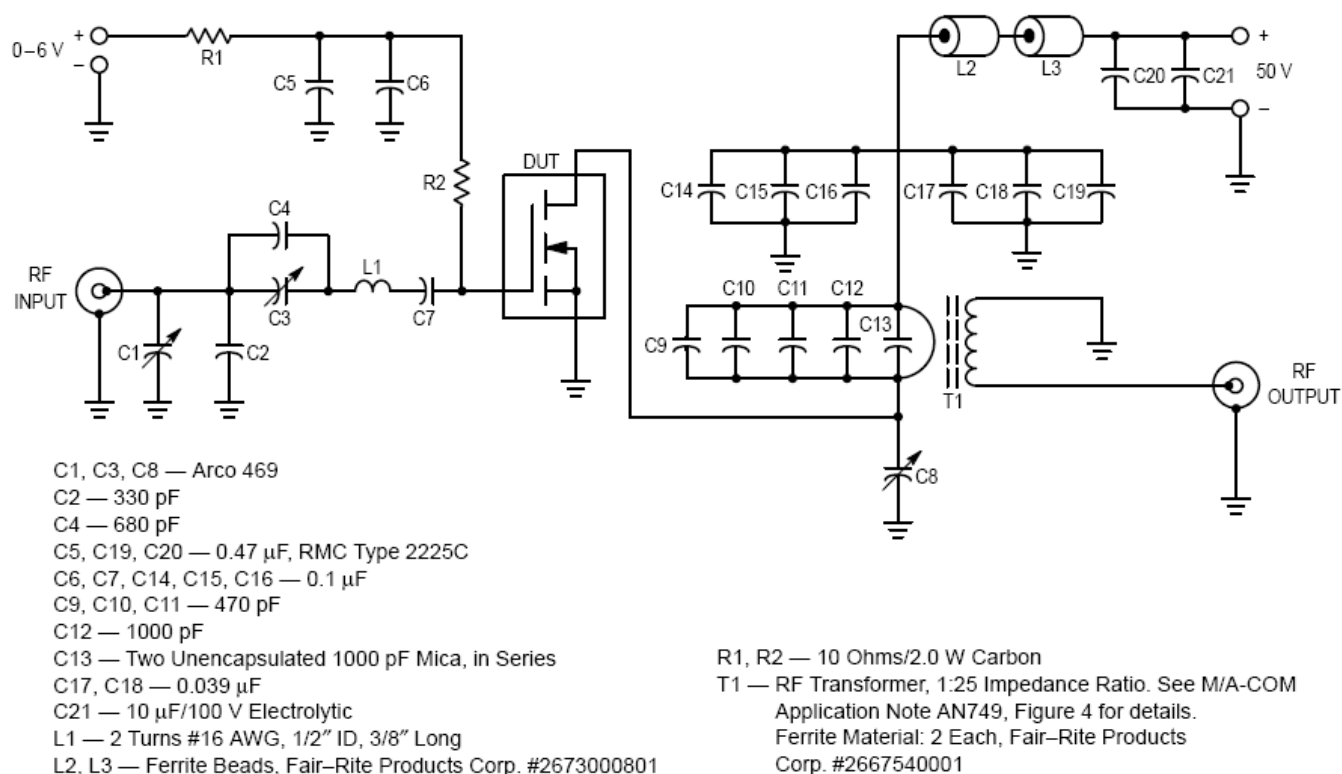
Input Capacitance ($V_{DS} = 50$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{iss}	—	1600	—	pF
Output Capacitance ($V_{DS} = 50$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{oss}	—	950	—	pF
Reverse Transfer Capacitance ($V_{DS} = 50$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{rss}	—	175	—	pF

FUNCTIONAL TESTS

Common Source Amplifier Power Gain ($V_{DD} = 50$ V, $P_{out} = 600$ W, $I_{DQ} = 800$ mA, $f = 30$ MHz)	G_{ps}	—	17	—	dB
Drain Efficiency ($V_{DD} = 50$ V, $P_{out} = 600$ W, $I_{DQ} = 800$ mA, $f = 30$ MHz)	η	—	45	—	%
Intermodulation Distortion ($V_{DD} = 50$ V, $P_{out} = 600$ W (PEP), $f_1 = 30$ MHz, $f_2 = 30.001$ MHz, $I_{DQ} = 800$ mA)	$IMD_{(d3)}$	—	–25	—	dB

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Rev. V1



All capacitors ATC type 100/200 chips or equivalent unless otherwise noted.

Figure 1. 30 MHz Test Circuit

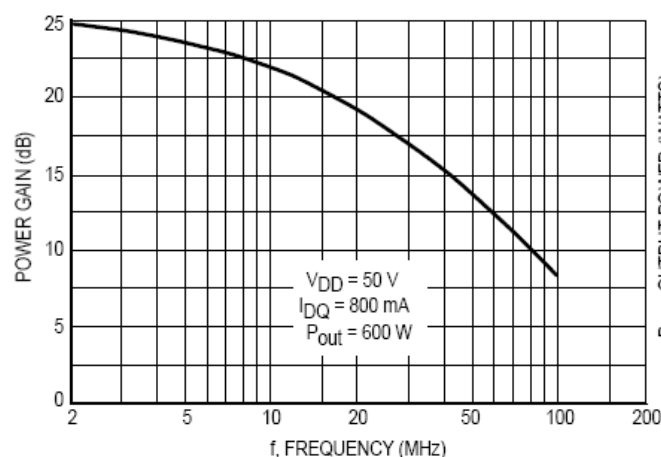


Figure 2. Power Gain versus Frequency

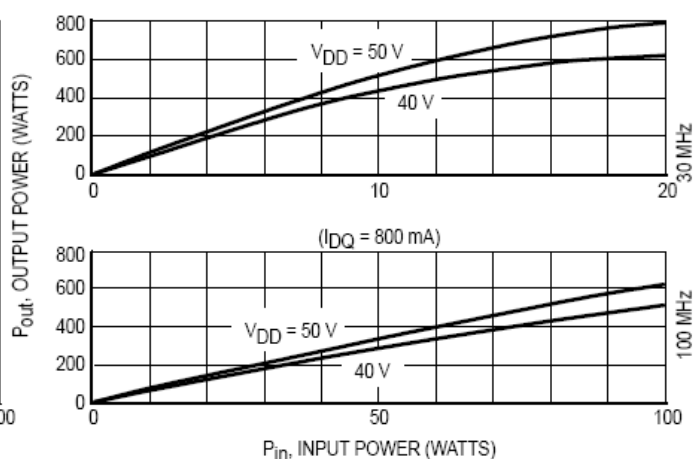


Figure 3. Output Power versus Input Power

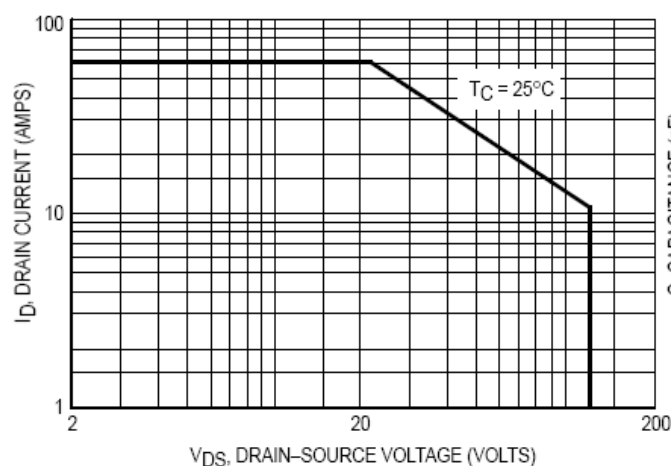


Figure 4. DC Safe Operating Area

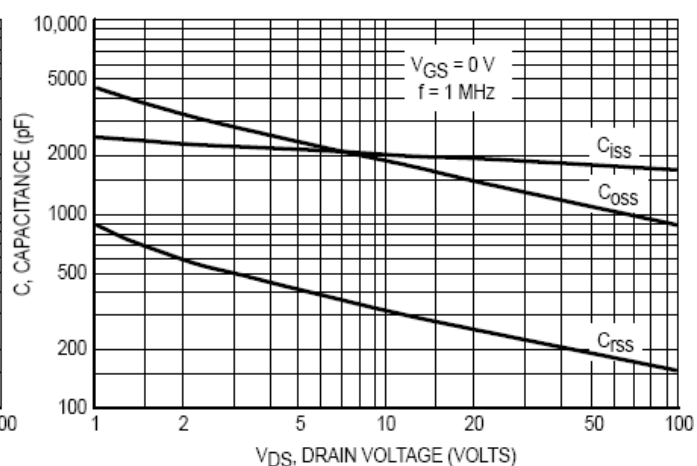


Figure 5. Capacitance versus Drain Voltage

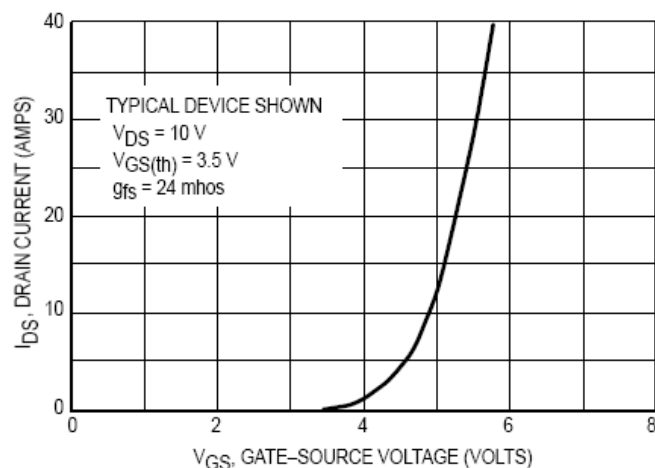


Figure 6. Gate Voltage versus Drain Current

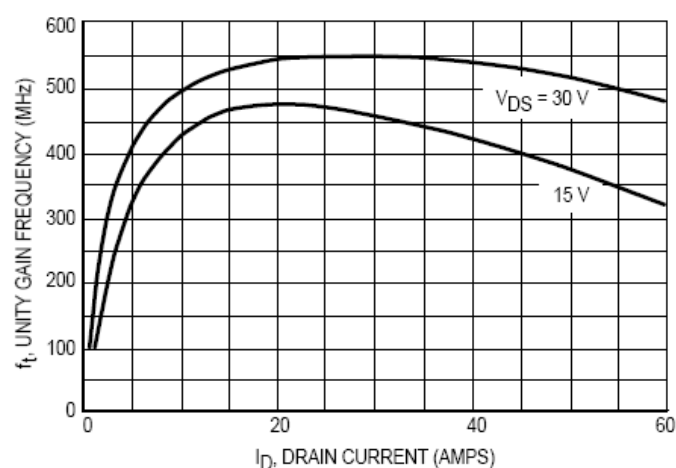


Figure 7. Common Source Unity Gain Frequency versus Drain Current

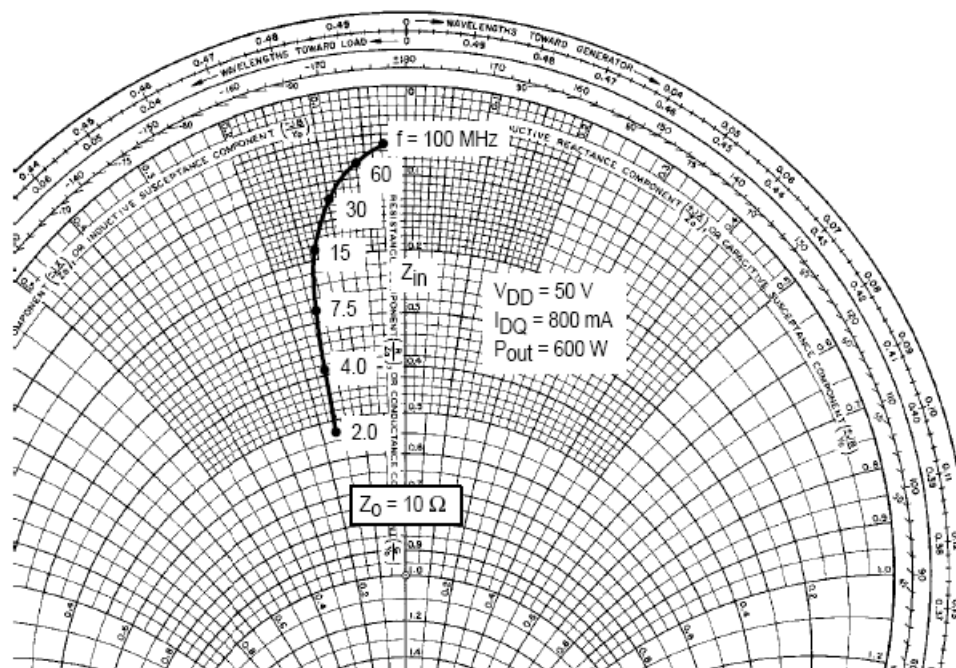
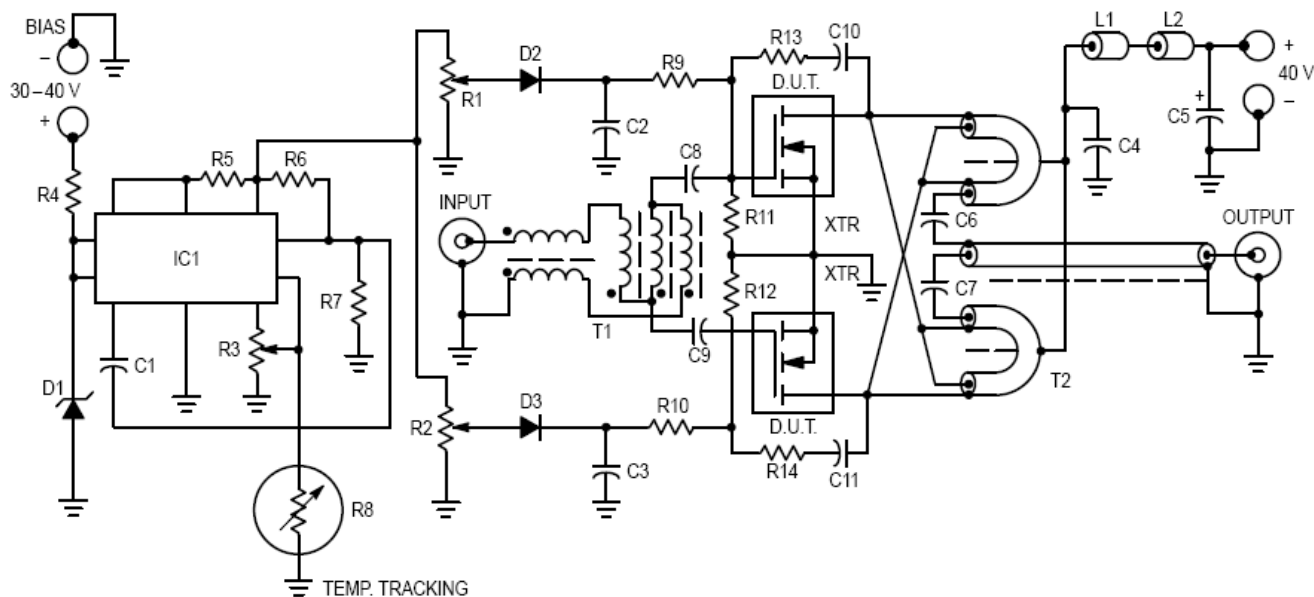


Figure 8. Series Equivalent Impedance

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Rev. V1



C1 — 1000 pF Ceramic
C2, C3, C4, C8, C9, C10, C11 — 0.1 μ F Ceramic
C5 — 10 μ F/100 V Electrolytic
C6, C7 — 0.1 μ F Ceramic, (ATC 200/823 or Equivalent)
D1 — 28 V Zener, 1N5362 or Equivalent
D3 — 1N4148
IC1 — MC1723
L1, L2 — Fair-Rite Products Corp. Ferrite Beads
#2673000801
R1, R2, R3 — 10 k Trimpot
R4 — 1.0 k/1.0 W
R5 — 10 Ohms
R6 — 2.0 k

R7 — 10 k
R8 — Thermistor, 10 k (25°C), 2.5 k (75°C)
R9, R10 — 100 Ohms
R11, R12 — 1.0 k
R13, R14 — 50–100 Ohms, 4.0 x 2.0 W Carbon in Parallel
T1 — 9:1 Transformer, Trifilar and Balun Wound on Separate
Fair-Rite Products Corp. Balun Cores #286100012, 5 Turns Each.
T2 — 1:9 Transformer, Balun 50 Ohm CO-AX Cable RG-188,
Low Impedance Lines W.L. Gore 16 Ohms CO-AX Type CXN 1837.
Each Winding Threaded Through Two Fair-Rite Products Corp.
#2661540001 Ferrite Sleeves (6 Each).
XTR — MRF154

Figure 9. 20–80 MHz 1.0 kW Broadband Amplifier

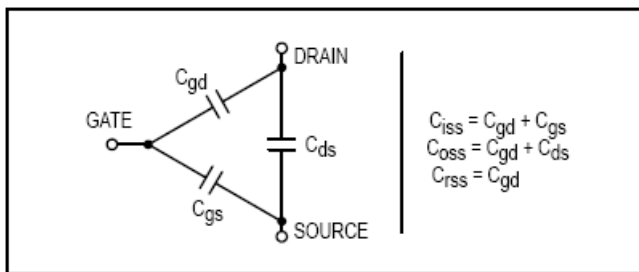
RF POWER MOSFET CONSIDERATIONS

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during the fabrication of the RF MOSFET results in a junction capacitance from drain-to-source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The

C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate-source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 109 ohms

— resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended.

MOUNTING OF HIGH POWER RF POWER TRANSISTORS

The package of this device is designed for conduction cooling. It is extremely important to minimize the thermal resistance between the device flange and the heat dissipator.

Since the device mounting flange is made of soft copper, it may be deformed during various stages of handling or during transportation. It is recommended that the user makes a final inspection on this before the device installation. ± 0.0005 , is considered sufficient for the flange bottom.

The same applies to the heat dissipator in the device mounting area. If copper heatsink is not used, a copper head spreader is strongly recommended between the device mounting surfaces and the main heatsink. It should be at least 1/4, thick and extend at least one inch from the flange edges. A thin layer of thermal compound in all interfaces is, of course, essential. The recommended torque on the 4–40 mounting screws should be in the area of 4–5 lbs. –inch, and spring type lock washers along with flat washers are recommended.

For die temperature calculations, the Δ temperature from a corner mounting screw area to the bottom center of the flange is approximately 5°C and 10°C under normal operating conditions (dissipation 150 W and 300 W respectively).

The main heat dissipater must be sufficiently large and have low R_{θ} for moderate air velocity, unless liquid cooling is employed.

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Rev. V1

CIRCUIT CONSIDERATIONS

At high power levels (500 W and up), the circuit layout becomes critical due to the low impedance levels and high RF currents associated with the output matching. Some of the components, such as capacitors and inductors must also withstand these currents. The component losses are directly proportional to the operating frequency. The manufacturers

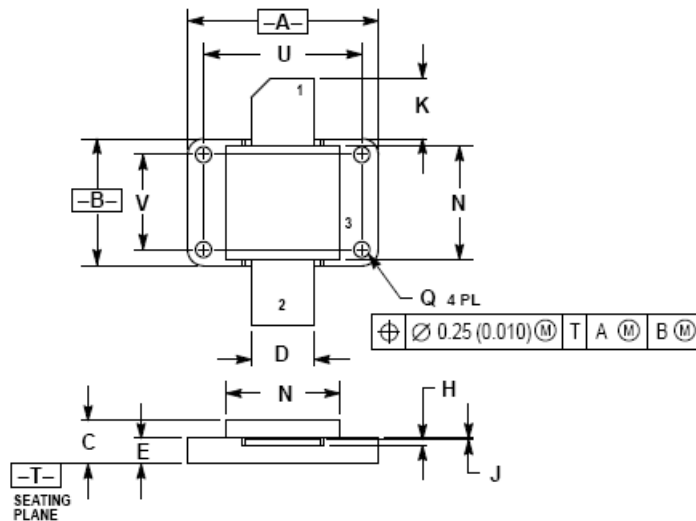
specifications on capacitor ratings should be consulted on these aspects prior to design.

Push-pull circuits are less critical in general, since the ground referenced RF loops are practically eliminated, and the impedance levels are higher for a given power output. High power broadband transformers are also easier to design than comparable LC matching networks.

EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
V_{CBO}	V_{DGO}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{fe}	g_{fs}
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$

PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.480	1.510	37.85	38.35
B	0.990	1.010	25.15	25.65
C	0.330	0.365	8.38	9.27
D	0.460	0.510	12.45	12.95
E	0.185	0.205	4.65	5.21
H	0.045	0.055	1.14	1.39
J	0.004	0.008	0.10	0.15
K	0.425	0.500	10.80	12.70
N	0.880	0.910	22.87	23.11
Q	0.120	0.130	3.05	3.30
U	1.250 BSC		31.75 BSC	
V	0.750 BSC		19.05 BSC	

STYLE 2:
 PIN 1. DRAIN
 2. GATE
 3. SOURCE

CASE 368-03
ISSUE C

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