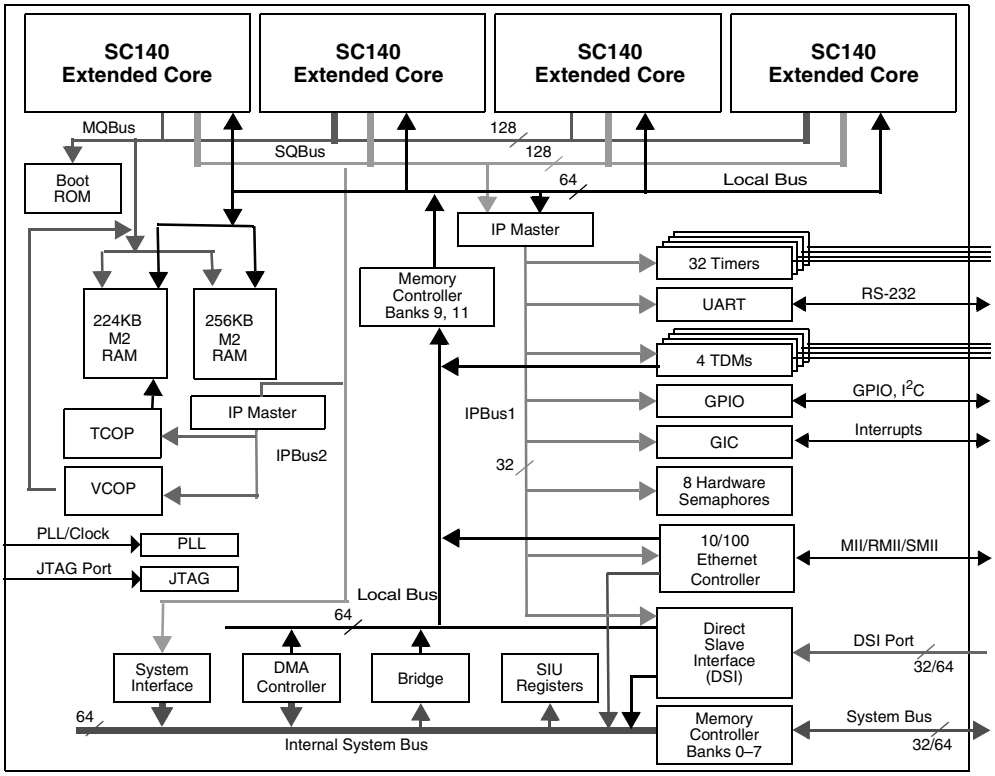
MSC8126

Quad Core 16-Bit Digital Signal Processor



Note: The arrows show the direction from which the transfer originates.

Figure 1. MSC8126 Block Diagram

The raw processing power of this highly integrated system-on-a-chip device will enable developers to create next-generation networking products that offer tremendous channel densities, while maintaining system flexibility, scalability, and upgradeability. The MSC8126 is offered in two core speed levels: 400 and 500 MHz.

What's New?

Rev. 11 includes the following:

- **Chapter 2** updates **Table 2-11** reset timing values.

The MSC8126 is a highly integrated system-on- a-chip that combines four SC140 extended cores with a turbo coprocessor (TCOP), a Viterbi coprocessor (VCOP), an RS-232 serial interface, four time-division multiplexed (TDM) serial interfaces, thirty-two general-purpose timers, a flexible system interface unit (SIU), an Ethernet interface, and a multi-channel DMA controller. The four extended cores can deliver a total 8000 DSP MMACS performance at 500 MHz. Each core has four arithmetic logic units (ALUs), internal memory, a write buffer, and two interrupt controllers (see **Figure 2**). The MSC8126 device targets high-bandwidth highly computational DSP applications and is optimized for wireless transcoding and packet telephony as well as high-bandwidth base station applications. The MSC8126 delivers enhanced performance while maintaining low power dissipation and greatly reducing system cost.

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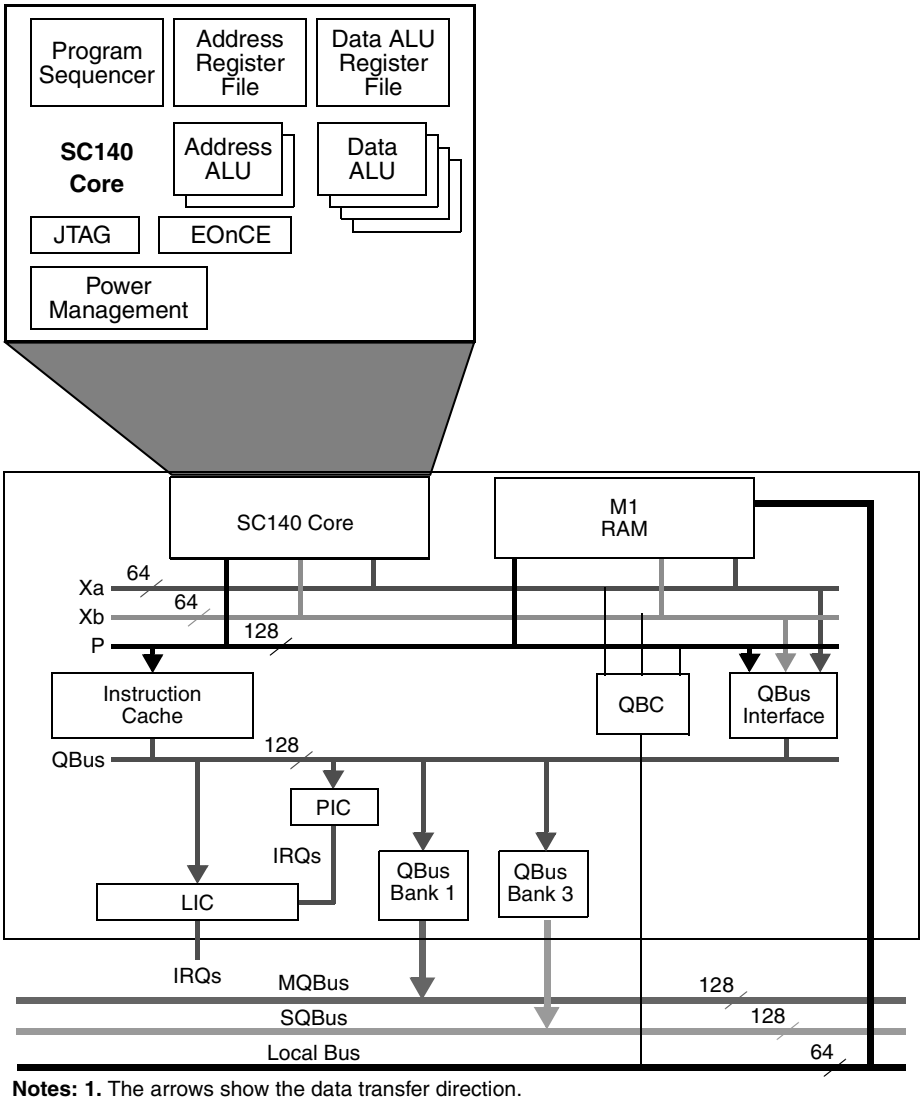
Data Sheet Conventions

$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
"asserted"	Means that a high true (active high) signal is high or that a low true (active low) signal is low
"deasserted"	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

Signal/Symbol	Logic State	Signal State	Voltage
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.



Notes: 1. The arrows show the data transfer direction.
2. The QBus interface includes a bus switch, write buffer, fetch unit, and a control unit that defines four QBus banks. In addition, the QBC handles internal memory contentions.

Figure 2. SC140 Extended Core Block Diagram

Features

The tables in this section list the features of the MSC8126 device.

Table 1. Extended SC140 Cores and Core Memories

Feature	Description
SC140 Core	Four SC140 cores: • Up to 8000 MMACS using 16 ALUs running at up to 500 MHz. • A total of 1436 KB of internal SRAM (224 KB per core + 16 KB ICache per core + the shared M2 memory). Each SC140 core provides the following: • Up to 2000 MMACS using an internal 500 MHz clock. A MAC operation includes a multiply-accumulate command with the associated data move and pointer update. • 4 ALUs per SC140 core. • 16 data registers, 40 bits each. • 27 address registers, 32 bits each. • Hardware support for fractional and integer data types. • Very rich 16-bit wide orthogonal instruction set. • Up to six instructions executed in a single clock cycle. • Variable-length execution set (VLES) that can be optimized for code density and performance. • JTAG port complies with **IEEE**® Std 1149.1™. • Enhanced on-device emulation (EOnCE) with real-time debugging capabilities.
Extended Core	Each SC140 core is embedded within an extended core that provides the following: • 224 KB M1 memory that is accessed by the SC140 core with zero wait states. • Support for atomic accesses to the M1 memory. • 16 KB instruction cache, 16 ways. • A four-entry write buffer that frees the SC140 core from waiting for a write access to finish. • External cache support by asserting the global signal (GBL) when predefined memory banks are accessed. • Programmable interrupt controller (PIC). • Local interrupt controller (LIC).
Multi-Core Shared Memories	• M2 memory (shared memory): —A 476 KB memory working at the core frequency. —Accessible from the local bus. —Accessible from all four SC140 cores using the MQBus. • 4 KB bootstrap ROM.
M2-Accessible Multi-Core Bus (MQBus)	• A QBus protocol multi-master bus connecting the four SC140 cores and the VCOP to the M2 memory. • Data bus access of up to 128-bit read and up to 64-bit write. • Operation at the SC140 core frequency. • A central efficient round-robin arbiter controlling SC140 core access on the MQBus. • Atomic operation control of access to M2 memory by the four SC140 cores and the local bus.

Table 2. Phase-Lock Loop (PLL)

Feature	Description
Internal PLL	• Generates up to 500 MHz core clock and up to 166 MHz bus clocks for the 60x-compatible local and system buses and other modules. • PLL values are determined at reset based on configuration signal values.

Table 3. Buses and Memory Controller

Feature	Description
60x-Compatible System Bus	• 64/32-bit data and 32-bit address 60x bus. • Support for multiple-master designs. • Four-beat burst transfers (eight-beat in 32-bit wide mode). • Port size of 64, 32, 16, and 8 controlled by the internal memory controller. • Bus can access external memory expansion or off-device peripherals, or it can enable an external host device to access internal resources. • Slave support, direct access by an external host to internal resources including the M1 and M2 memories. • On-device arbitration between up to four master devices.
Direct Slave Interface (DSI)	A 32/64-bit wide slave host interface that operates only as a slave device under the control of an external host processor. • 21–25 bit address, 32/64-bit data. • Direct access by an external host to internal and external resources, including the M1 and the M2 memories as well as external devices on the system bus. • Synchronous and asynchronous accesses, with burst capability in the synchronous mode. • Dual or single-strobe modes. • Write and read buffers improve host bandwidth. • Byte enable signals enables 1, 2, 4, and 8 byte write access granularity. • Sliding window mode enables access with reduced number of address pins. • Chip ID decoding enables using one $\overline{CS}$ signal for multiple DSPs. • Broadcast $\overline{CS}$ signal enables parallel write to multiple DSPs. • Big-endian, little-endian, and munged little-endian support.
3-Mode Signal Multiplexing	• 64-bit DSI, 32-bit system bus. • 32-bit DSI, 64-bit system bus. • 32-bit DSI, 32-bit system bus.
Memory Controller	Flexible eight-bank memory controller: • Three user-programmable machines (UPMs), general-purpose chip-select machine (GPCM), and a page-mode SDRAM machine. • Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash memory, and other user-definable peripherals. • Byte enables for either 64-bit or 32-bit bus width mode. • Eight external memory banks (banks 0–7). Two additional memory banks (banks 9, 11) control IPBus peripherals and internal memories. Each bank has the following features: —32-bit address decoding with programmable mask. —Variable block sizes (32 KB to 4 GB). —Selectable memory controller machine. —Two types of data errors check/correction: normal odd/even parity and read-modify-write (RMW) odd/even parity for single accesses. —Write-protection capability. —Control signal generation machine selection on a per-bank basis. —Support for internal or external masters on the system bus. —Data buffer controls activated on a per-bank basis. —Atomic operation. —RMW data parity check (on system bus only). —Extensive external memory-controller/bus-slave support. —Parity byte select pin, which enables a fast, glueless connection to RMW-parity devices (on the system bus only). —Data pipeline to reduce data set-up time for synchronous devices.

Table 4. DMA Controller

Feature	Description
Multi-Channel DMA Controller	• 16 time-multiplexed unidirectional channels. • Services up to four external peripherals. • Supports $\overline{\text{DONE}}$ or $\overline{\text{DRACK}}$ protocol on two external peripherals. • Each channel group services 16 internal requests generated by eight internal FIFOs. Each FIFO generates: —A watermark request to indicate that the FIFO contains data for the DMA to empty and write to the destination. —A hungry request to indicate that the FIFO can accept more data. • Priority-based time-multiplexing between channels using 16 internal priority levels. • Round-robin time-multiplexing between channels. • A flexible channel configuration: —All channels support all features. —All channels connect to the system bus or local bus. • Flyby transfers in which a single data access is transferred directly from the source to the destination without using a DMA FIFO.

Table 5. Serial Interfaces

Feature	Description
Time-Division Multiplexing (TDM)	Up to four independent TDM modules, each with the following features: • Optional operating configurations: —Totally independent receive and transmit channels, each having one data line, one clock line, and one frame sync line. —Four data lines with one clock and one frame sync shared among the transmit and receive lines. • Connects gluelessly to most T1/E1 framers as well as to common buses such as the ST-BUS. • Hardware A-law/μ-law conversion. • Up to 62.5 Mbps per TDM (62.5 MHz bit clock if one data line is used, 31.25 MHz if two data lines are used, 15.63 MHz if four data lines are used). • Up to 256 channels. • Up to 16 MB per channel buffer (granularity 8 bytes), where A/μ law buffer size is double (granularity 16 byte). • Receive buffers share one global write offset pointer that is written to the same offset relative to their start address. • Transmit buffers share one global read offset pointer that is read from the same offset relative to their start address. • All channels share the same word size. • Two programmable receive and two programmable transmit threshold levels with interrupt generation that can be used, for example, to implement double buffering. • Each channel can be programmed to be active or inactive. • 2-, 4-, 8-, or 16-bit channels are stored in the internal memory as 2-, 4-, 8-, or 16-bit channels, respectively. • The TDM transmitter sync signal (TxTSYN) can be configured as either input or output. • Frame sync and data signals can be programmed to be sampled either on the rising edge or on the falling edge of the clock. • Frame sync can be programmed as active low or active high. • Selectable delay (0–3 bits) between the frame sync signal and the beginning of the frame. • MSB or LSB first support.

Table 5. Serial Interfaces (Continued)

Feature	Description
Ethernet Controller	• Complies with **IEEE** Std 802® including Std. 802.3™, 802.3u™, 802.3x™, and 802.3ac™. • Three Ethernet physical interfaces: —10/100 Mbps MII. —10/100 Mbps RMII. —10/100 Mbps SMII. • Full and half-duplex support. • Full-duplex flow control (automatic PAUSE frame generation or software programmed PAUSE frame generation and recognition). • Out-of-sequence transmit queue for initiating flow-control. • Programmable maximum frame length supports jumbo frames (up to 9.6 K) and virtual local area network (VLAN) tags and priority. • Retransmission from transmit FIFO following a collision. • CRC generation and verification of inbound/outbound packets. • Address recognition: —Each exact match can be programmed to be accepted or rejected. —Broadcast address (accept/reject). —Exact match 48-bit individual (unicast) address. —Hash (256-bit hash) check of individual (unicast) addresses. —Hash (256-bit hash) check of group (multicast) addresses. —Promiscuous mode. • Pattern matching: —Up to 16 unique 4-byte patterns. —Pattern match on bit-basis. —Matching range up to 256 bytes deep into the frame. —Offsets to a maximum of 252 bytes. —Programmable pattern size in 4-byte increments up to 64 bytes. —Accept or reject frames if a match is detected. —Up to eight unicast addresses for exact matches. —Pattern matching accepts/rejects IP addresses. • Filing of receive frames based on pattern match; prioritization of frames. • Insertion with expansion or replacement for transmit frames; VLAN tag insertion. • RMON statistics. • Master DMA on the local bus for fetching descriptors and accessing the buffers. • Ethernet PHY can be exposed either on GPIO pins or on the high most significant bits of the DSI/system when the DSI and the system bus are both 32 bits. • MPC8260 8-byte width buffer descriptor mode as well as 32-byte width buffer descriptor mode. • MII Bridge (MIIGSK): —Programmable selection of the 50 MHz RMII reference clock source (external or internal). —Independent 2 bit wide transmit and receive data paths. —Six operating modes. —Four general-purpose control signals. —Programmable transmitted inter-frame bits to support inter-frame gap for frames in the SMII domain. • SMII features: —Convey complete MII information between the PHY and MAC. —Allow direct MAC-to-MAC communication in SMII mode. —Can generate an interrupt request line while receiving inter-frame segments.

Table 5. Serial Interfaces (Continued)

Feature	Description
UART	• Two signals for transmit data and receive data. • No clock, asynchronous mode. • Can be serviced either by the SC140 DSP cores or an external host on the system bus or the DSI. • Full-duplex operation. • Standard mark/space non-return-to-zero (NRZ) format. • 13-bit baud rate selection. • Programmable 8-bit or 9-bit data format. • Separately enabled transmitter and receiver. • Programmable transmitter output polarity. • Two receiver wake-up methods: —Idle line wake-up. —Address mark wake-up. • Separate receiver and transmitter interrupt requests. • Nine flags, the first five can generate interrupt request: —Transmitter empty. —Transmission complete. —Receiver full. —Idle receiver input. —Receiver overrun. —Receiver active. —Noise error. —Framing error. —Parity error. • Receiver framing error detection. • Hardware parity checking. • 1/16 bit-time noise detection. • Maximum bit rate 6.25 Mbps. • Single-wire and loop operations.
General-Purpose I/O (GPIO) Port	• 32 bidirectional signal lines that either serve the peripherals or act as programmable I/O ports. • Each port can be programmed separately to serve up to two dedicated peripherals, and each port supports open-drain output mode.
I^2C Software Module	• Supports booting from a serial EEPROM • Uses GPIO timing.

Table 6. Miscellaneous Modules

Feature	Description
Timers	Two modules of 16 timers each. • Cyclic or one-shot. • Input clock polarity control. • Interrupt request when counting reaches a programmed threshold. • Pulse or level interrupts. • Dynamically updated programmed threshold. • Read counter any time. Watchdog mode for the timers that connect to the device.
Hardware Semaphores	Eight coded hardware semaphores, locked by simple write access without need for read-modify-write mechanism.
Global Interrupt Controller (GIC)	• Consolidation of chip maskable interrupt and non-maskable interrupt sources and routing to $\overline{\text{INT_OUT}}$, $\overline{\text{NMI_OUT}}$, and to the cores. • Generation of 32 virtual interrupts (eight to each SC140 core) by a simple write access. • Generation of virtual $\overline{\text{NMI}}$ (one to each SC140 core) by a simple write access.

Table 7. Coprocessors

Feature	Description
VCOP	• Fully programmable feed-forward channel decoding, feed-forward channel equalization and traceback sessions. • Up to 400 3GPP 12.2kbps AMR channels (channel decoding, number of channels linear to frequency). • Up to 200 blind transport format detect (BTFD) channels according to the 3GPP standard. Number of channels linear to frequency. • For channel decoding: —Constraint length between K = 5 and K = 9. —Puncture Codes. —Rate 1/2, 1/3, 1/4 and 1/6. —Four fully programmable polynomials (rate 1/6 is implemented by three polynomials only). —History buffer with up to 768 stages for 3G standards. —Input symbols are 8-bit (256 levels) signed soft symbols. —Output is hard decision (1-bit). • For GSM channel equalization: —Fully programmable 4 to 6 estimated channel autocorrelation coefficients (S-Parameters). —History buffer with up to 4090 stages for GSM. —Matched filter input is 8-bit (256 levels). —SOVA assist algorithm. —Output 8-bit coded delta values for SOVA assist algorithm, 1-bit hard decision traceback and history buffer or recursive traceback. • Fully programmable block length for all sessions. • Programmable traceback methods of Max Path, Min Path or End State. • Programmable learning period length for the traceback session. • Supports the start of feed-forward according to a presaved PM memory content. However the history buffer is not saved. Therefore the traceback is according to the current block only. • Each SC140 can program the VCOP parameters while the VCOP is in IDLE mode and then the VCOP can run independently on the whole block of data. • Dumping path metrics to the internal memory on up to 12 predefined stages; this is needed for BTFD applications. • Interrupt lines and status bits notify the cores on session completion. • Performance monitoring unit with 6 monitored behaviors.
TCOP	• Full support of 3GPP and CDMA2000 standards in Turbo decode. • Up to 20 turbo-coding 384 kbps channels. • 8 state PCCC with polynomial as supported by the 3G standards. • Iterative decoding structure based on Maximum A-Posteriori probability (MAP), with calculations performed in the LOG domain. • Encoding rate of 1/2, 1/3, 1/4, 1/5 with programmable puncturing for the parity symbols. • Full flexibility interleave function via a look-up table. • Flexible block size (1–32767 bits). • MAX log MAP and log MAP (MAX*) approximation. • Programmable MAX* using linear approximation. • Programmable number of iterations, with resolution of half iteration (one MAP). • Fully automatic execution when the GO command executes. • High data rates (for multi-channel systems or multiple channel accumulating to high data rates). • Can stop processing after every MAP when soft lambda all reach a programmable quality threshold. • Minimum and maximum number of iterations to execute in conjunction with the stop criteria. • The SC140 core or host can stop the processing after every MAP during run time. • Automatic, internal normalization for α, β overflow handling, with zero overhead. • Automatic, internal Λ clipping for Λ overflow handling, with zero overhead. • Additional least significant bit in α, β, γ arithmetic guarding against precision loss during the gamma calculation due to the division by 2.

Table 8. Power and Packaging

Feature	Description
Reduced Power Dissipation	• Low-power CMOS design. • Separate power supply for internal logic (1.2 V for 400 MHz or 500 MHz) and I/O (3.3 V). • Low-power standby modes. • Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent).
Packaging	• 0.8 mm pitch Flip-Chip Plastic Ball-Grid Array (FC-PBGA). • 431-connection (ball). • 20 mm × 20 mm.

Table 9. Software Support

Feature	Description
Real-Time Operating System (RTOS)	The real-time operating system (RTOS) fully supports device architecture (multi-core, memory hierarchy, ICache, timers, DMA controller, interrupts, peripherals), as follows: • High-performance and deterministic, delivering predictive response time. • Optimized to provide low interrupt latency with high data throughput. • Preemptive and priority-based multitasking. • Fully interrupt/event driven. • Small memory footprint. • Comprehensive set of APIs.
Multi-Core Support	• One instance of kernel code in all four SC140 cores. • Dynamic and static memory allocation from local memory (M1) and shared memory (M2).
Distributed System Support	Transparent inter-task communications between tasks running inside the SC140 cores and the other tasks running in on-board devices or remote network devices: • Messaging mechanism between tasks using mailboxes and semaphores. • Networking support; data transfer between tasks running inside and outside the device using networking protocols. • Includes integrated device drivers for such peripherals as TDM, UART, and external buses.
Software Support	• Task debugging utilities integrated with compilers and vendors. • Board support package (BSP) for the application development system (ADS). • Integrated development environment (IDE): —C/C++ compiler with in-line assembly so developers can generate highly optimized DSP code. Translates C/C++ code into parallel fetch sets and maintains high code density. —Librarian. User can create libraries for modularity. —A collection of C/C++ functions for developer use. —Highly efficient linker to produce executables from object code. —Seamlessly integrated real-time, non-intrusive multi-mode debugger for debugging highly optimized DSP algorithms. The developer can choose to debug in source code, assembly code, or mixed mode. —Device simulation models enable design and simulation before hardware availability. —Profiler using a patented binary code instrumentation (BCI) technique helps developers identify program design inefficiencies. —Version control. Metrowerks® CodeWarrior® includes plug-ins for ClearCase, Visual SourceSafe, and CVS.
Boot Options	• External memory. • External host. • UART. • TDM. • I^2C

Table 10. Application Development System (ADS) Board

Feature	Description
MSC8126ADS	• Host debug through single JTAG connector supports both processors. • MSC8103 as the MSC8126 host with both devices on the board. The MSC8103 system bus connects to the MSC8126 DSI. • Flash memory for stand-alone applications. • Communications ports: —10/100Base-T. —155 Mbit ATM over Optical. —T1/E1 TDM interface. —H.110. —Voice codec. —RS-232. —High-density (MICTOR) logic analyzer connectors to monitor MSC8126 signals —6U CompactPCI form factor. • Emulates MSC8126 DSP farm by connecting to three other ADS boards.

Product Documentation

The documents listed in **Table 11** are required for a complete description of the MSC8126 and are necessary to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale Semiconductor sales office, or a Freescale Literature Distribution Center. For documentation updates, visit the Freescale DSP website. See the contact information on the back of this document.

Table 11. MSC8126 Documentation

Name	Description	Order Number
MSC8126 Technical Data	MSC8126 features list and physical, electrical, timing, and package specifications.	MSC8126
MSC8126 User's Guide	User information includes system functionality, getting started, and programming topics.	Availability TBD
MSC8126 Reference Manual	Detailed functional description of the MSC8126 memory and peripheral configuration, operation, and register programming.	MSC8126RM
StarCore™ SC140 DSP Core Reference Manual	Detailed description of the SC140 family processor core and instruction set.	MNSC140CORE
Application Notes	Documents describing specific applications or optimized device operation including code examples.	See the website product page.

Signals/Connections 1

The MSC8126 external signals are organized into functional groups, as shown in **Table 1-1** and **Figure 1-1**. **Table 1-1** lists the functional groups, the number of signal connections in each group, and references the table that gives a detailed listing of multiplexed signals within each group. **Figure 1-1** shows MSC8126 external signals organized by function.

Table 1-1. MSC8126 Functional Signal Groupings

Functional Group	Number of Signal Connections	Description
Power (V_{DD}, V_{CC}, and GND)	155	**Table 1-2** on page 1-3
Clock	3	**Table 1-3** on page 1-3
Reset and configuration	4	**Table 1-4** on page 1-3
DSI, system bus, Ethernet, and interrupts	210	**Table 1-5** on page 1-4
Memory controller	16	**Table 1-6** on page 1-14
General-purpose input/output (GPIO), time-division multiplexed (TDM) interface, universal asynchronous receiver/ transmitter (UART), Ethernet, and timers	32	**Table 1-7** on page 1-16
Dedicated Ethernet signals	3	**Table 1-8** on page 1-23
EOnCE and JTAG test access port	7	**Table 1-9** on page 1-24
Reserved (denotes connections that are always reserved)	1	**Table 1-10** on page 1-24

HD0/SWTE	↔	1	DSI/SYS.BUS/ETHERNET	SYSTEM BUS	32	↔	A[0–31]
HD1/DSISYNC	↔	1			1	↔	TT0/HA7
HD2/DSI64	↔	1			1	↔	TT1
HD3/MODCK1	↔	1			3	↔	TT[2–4]/CS[5–7]
HD4/MODCK2	↔	1			5	→	CS[0–4]
HD5/CNFGS	↔	1			4	↔	TSZ[0–3]
HD[6–31]	↔	26			1	↔	TBST
HD[32-39]/D[32-39]/reserved	↔	8			1	↔	IRQ1/GBL
HD40/D40/ETHRXD0	↔	1			1	↔	IRQ3/BADDR31
HD41/D41/ETHRXD1	↔	1			1	↔	IRQ2/BADDR30
HD42/D42/ETHRXD2/reserved	↔	1			1	↔	IRQ5/BADDR29
HD43/D43/ETHRXD3/reserved	↔	1			1	→	BADDR28
HD[44-45]/D[44-45]/reserved	↔	2			1	→	BADDR27
HD46/D46/ETHTXD0	↔	1			1	↔	BR
HD47/D47/ETHTXD1	↔	1			1	↔	BG
HD48/D48/ETHTXD2/reserved	↔	1			1	↔	DBG
HD49/D49/ETHTXD3/reserved	↔	1			1	↔	ABB/IRQ4
HD[50-53]/D[50-53]/reserved	↔	4			1	↔	DBB/IRQ5
HD54/D54/ETHTX_EN	↔	1			1	↔	TS
HD55/D55/ETHTX_ER/reserved	↔	1			1	↔	AACK
HD56/D56/ETHRX_DV/ETHCRS_DV	↔	1			1	↔	ARTRY
HD57/D57/ETHRX_ER	↔	1			32	↔	D[0–31]
HD58/D58/ETHMDC	↔	1			1	↔	reserved/DP0/DREQ1/EXT_BR2
HD59/D59/ETHMDIO	↔	1			1	↔	IRQ1/DP1/DACK1/EXT_BG2
HD60/D60/ETHCOL/reserved	↔	1			1	↔	IRQ2/DP2/DACK2/EXT_DBG2
HD[61–63]/D[61-63]/reserved	↔	3			1	↔	IRQ3/DP3/DREQ2/EXT_BR3
HCID[0–2]	→	3	MEMC DSI		1	↔	IRQ4/DP4/DACK3/EXT_DBG3
HCID3/HA8	→	1			1	↔	IRQ5/DP5/DACK4/EXT_BG3
HA[11–29]	→	19			1	↔	IRQ6/DP6/DREQ3
HWBS[0–3]/HDBS[0–3]/HWBE[0–3]/HDBE[0–3]	→	4			1	↔	IRQ7/DP7/DREQ4
HWBS[4–7]/HDBS[4–7]/HWBE[4–7]/HDBE[4–7]/PWE[4–7]/PSDDQM[4–7]/PBS[4–7]	↔	4			1	↔	TA
HRDS/HRW/HRDE	→	1			1	↔	TEA
HBRST	→	1			1	←	NMI
HDST[0–1]/HA[9–10]	→	2			1	→	NMI_OUT
HCS	→	1			1	↔	PSDVAL
HBCS	→	1			1	↔	IRQ7/INT_OUT
HTA	←	1		MEMC SYS	1	→	BCTL0
HCLKIN	→	1			1	→	BCTL1/CS5
GPIO0/CHIP_ID0/IRQ4/ETHTXD0	↔	1	GPIO/TDM/ETHERNET/TIMERS/I2C		3	↔	BM[0–2]/TC[0–2]/BNKSEL[0–2]
GPIO1/TIMER0/CHIP_ID1/IRQ5/ETHTXD1	↔	1			1	→	ALE
GPIO2/TIMER1/CHIP_ID2/IRQ6	↔	1			4	→	PWE[0–3]/PSDDQM[0–3]/PBS[0–3]
GPIO3/TDM3TSYN/IRQ1/ETHTXD2	↔	1			1	→	PSDA10/PGPL0
GPIO4/TDM3TCLK/IRQ2/ETHTX_ER	↔	1			1	→	PSDWE/PGPL1
GPIO5/TDM3TDAT/IRQ3/ETHRXD3	↔	1			1	→	POE/PSDRAS/PGPL2
GPIO6/TDM3RSYN/IRQ4/ETHRXD2	↔	1			1	→	PSDCAS/PGPL3
GPIO7/TDM3RCLK/IRQ5/ETHTXD3	↔	1			1	↔	PGTA/PUPMWAIT/PGPL4/PPBS
GPIO8/TDM3RDAT/IRQ6/ETHCOL	↔	1			1	→	PSDAMUX/PGPL5
GPIO9/TDM2TSYN/IRQ7/ETHMDIO	↔	1					
GPIO10/TDM2TCLK/IRQ8/ETHRX_DV/ETHCRS_DV/NC	↔	1		Debug	1	←	EE0
GPIO11/TDM2TDAT/IRQ9/ETHRX_ER/ETHTXD	↔	1			1	→	EE1
GPIO12/TDM2RSYN/IRQ10/ETHRXD1/ETHSYNC	↔	1		CLK	1	→	CLKOUT
GPIO13/TDM2RCLK/IRQ11/ETHMDC	↔	1			1	←	Reserved
GPIO14/TDM2RDAT/IRQ12/ETHRXD0/NC	↔	1			1	←	CLKIN
GPIO15/TDM1TSYN/DREQ1	↔	1		RESET	1	←	PORESET
GPIO16/TDM1TCLK/DONE1/DRACK1	↔	1			1	↔	HRESET
GPIO17/TDM1TDAT/DACK1	↔	1			1	↔	SRESET
GPIO18/TDM1RSYN/DREQ2	↔	1			1	←	RSTCONF
GPIO19/TDM1RCLK/DACK2	↔	1		JTAG	1	←	TMS
GPIO20/TDM1RDAT	↔	1			1	←	TDI
GPIO21/TDM0TSYN	↔	1			1	←	TCK
GPIO22/TDM0TCLK/DONE2/DRACK2	↔	1			1	←	TRST
GPIO23/TDM0TDAT/IRQ13	↔	1			1	→	TDO
GPIO24/TDM0RSYN/IRQ14	↔	1					
GPIO25/TDM0RCLK/IRQ15	↔	1					
GPIO26/TDM0RDAT	↔	1					
GPIO27/URXD/DREQ1	↔	1					
GPIO28/UTXD/DREQ2	↔	1					
GPIO29/CHIP_ID3/ETHTX_EN	↔	1		Ded. Eth. Net	1	←	ETHRX_CLK/ETHSYNC_IN
GPIO30/TIMER2/TMCLK/SDA	↔	1			1	←	ETHTX_CLK/ETHREF_CLK/ETHCLOCK
GPIO31/TIMER3/SCL	↔	1			1	←	ETHCRS/ETHRXD

Power signals are: V_{DD}, V_{DDH}, V_{CCSYN}, GND, GND_H, and GND_{SYN}. Reserved signals can be left unconnected. NC signals must not be connected.

Figure 1-1. MSC8126 External Signals

1.1 Power Signals

Table 1-2. Power and Ground Signal Inputs

Signal Name	Description
V_{DD}	**Internal Logic Power** V_{DD} dedicated for use with the device core. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{DD} power rail.
V_{DDH}	**Input/Output Power** This source supplies power for the I/O buffers. The user must provide adequate external decoupling capacitors.
V_{CCSYN}	**System PLL Power** V_{CC} dedicated for use with the system Phase Lock Loop (PLL). The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail.
GND	**System Ground** An isolated ground for the internal processing logic and I/O buffers. This connection must be tied externally to all chip ground connections, except GND_{SYN}. The user must provide adequate external decoupling capacitors.
GND_{SYN}	**System PLL Ground** Ground dedicated for system PLL use. The connection should be provided with an extremely low-impedance path to ground.

1.2 Clock Signals

Table 1-3. Clock Signals

Signal Name	Type	Signal Description
CLKIN	Input	**Clock In** Primary clock input to the MSC8126 PLL.
CLKOUT	Output	**Clock Out** The bus clock.
Reserved	Input	Reserved. Pull down to ground.

1.3 Reset and Configuration Signals

Table 1-4. Reset and Configuration Signals

Signal Name	Type	Signal Description
$\overline{\text{PORESET}}$	Input	**Power-On Reset** When asserted, this line causes the MSC8126 to enter power-on reset state.
$\overline{\text{RSTCONF}}$	Input	**Reset Configuration** Used during reset configuration sequence of the chip. A detailed explanation of its function is provided in the *MSC8126 Reference Manual*. This signal is sampled upon deassertion of $\overline{\text{PORESET}}$. **Note:** When $\overline{\text{PORESET}}$ is deasserted, the MSC8126 also samples the following signals: • BM[0–2]—Selects the boot mode. • MODCK[1–2]—Selects the clock configuration. • SWTE—Enables the software watchdog timer. • DSISYNC, DSI64, CNFGS, and CHIP_ID[0–3]—Configures the DSI. Refer to **Table 1-5** for details on these signals.
$\overline{\text{HRESET}}$	Input/Output	**Hard Reset** When asserted as an input, this signal causes the MSC8126 to enter the hard reset state. After the device enters a hard reset state, it drives the signal as an open-drain output.
$\overline{\text{SRESET}}$	Input/Output	**Soft Reset** When asserted as an input, this signal causes the MSC8126 to enter the soft reset state. After the device enters a soft reset state, it drives the signal as an open-drain output.

1.4 Direct Slave Interface, System Bus, Ethernet, and Interrupt Signals

The direct slave interface (DSI) is combined with the system bus because they share some common signal lines. Individual assignment of a signal to a specific signal line is configured through internal registers. **Table 1-5** describes the signals in this group.

Note: Although there are fifteen interrupt request (IRQ) connections to the core processors, there are multiple external lines that can connect to these internal signal lines. After reset, the default configuration enables only $\overline{\text{IRQ[1–7]}}$, but includes two input lines each for $\overline{\text{IRQ[1–3]}}$ and $\overline{\text{IRQ7}}$. The designer must select one line for each required interrupt and reconfigure the other external signal line or lines for alternate functions. Additional alternate IRQ lines and $\overline{\text{IRQ[8–15]}}$ are enabled through the GPIO signal lines.

Table 1-5. DSI, System Bus, Ethernet, and Interrupt Signals

Signal Name	Type	Description
HD0	Input/ Output	**Host Data Bus 0** Bit 0 of the DSI data bus.
SWTE	Input	**Software Watchdog Timer Disable**. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD1	Input/ Output	**Host Data Bus 1** Bit 1 of the DSI data bus.
DSISYNC	Input	**DSI Synchronous** Distinguishes between synchronous and asynchronous operation of the DSI. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD2	Input/ Output	**Host Data Bus 2** Bit 2 of the DSI data bus.
DSI64	Input	**DSI 64** Defines the width of the DSI and SYSTEM Data buses. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD3	Input/ Output	**Host Data Bus 3** Bit 3 of the DSI data bus.
MODCK1	Input	**Clock Mode 1** Defines the clock frequencies. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD4	Input/ Output	**Host Data Bus 4** Bit 4 of the DSI data bus.
MODCK2	Input	**Clock Mode 2** Defines the clock frequencies. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD5	Input/ Output	**Host Data Bus 5** Bit 5 of the DSI data bus.
CNFGS	Input	**Configuration Source** One signal out of two that indicates reset configuration mode. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD[6–31]	Input/ Output	**Host Data Bus 6–31** Bits 6–31 of the DSI data bus.

Table 1-5. DSI, System Bus, Ethernet, and Interrupt Signals (Continued)

Signal Name	Type	Description
HD[32–39]	Input/ Output	**Host Data Bus 32–39** Bits 32–39 of the DSI data bus.
D[32–39]	Input/ Output	**System Bus Data 32–39** For write transactions, the bus master drives valid data on this bus. For read transactions, the slave drives valid data on this bus.
Reserved	Input	If the Ethernet port is enabled and multiplexed with the DSI/System bus, these signals are reserved and can be left unconnected.
HD40	Input/ Output	**Host Data Bus 40** Bit 40 of the DSI data bus.
D40	Input/ Output	**System Bus Data 40** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHRXD0	Input	**Ethernet Receive Data 0** In MII and RMII modes, bit 0 of the Ethernet receive data.
HD41	Input/ Output	**Host Data Bus 41** Bit 41 of the DSI data bus.
D41	Input/ Output	**System Bus Data 41** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHRXD1	Input	**Ethernet Receive Data 1** In MII and RMII modes, bit 1 of the Ethernet receive data.
HD42	Input/ Output	**Host Data Bus 42** Bit 42 of the DSI data bus.
D42	Input/ Output	**System Bus Data 42** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHRXD2	Input	**Ethernet Receive Data 2** In MII mode only, bit 2 of the Ethernet receive data.
Reserved	Input	In RMII mode, this signal is reserved and can be left unconnected.
HD43	Input/ Output	**Host Data Bus 43** Bit 43 of the DSI data bus.
D43	Input/ Output	**System Bus Data 43** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHRXD3	Input	**Ethernet Receive Data 3** In MII mode only, bit 3 of the Ethernet receive data.
Reserved	Input	In RMII mode, this signal is reserved and can be left unconnected.
HD[44–45]	Input/ Output	**Host Data Bus 44–45** Bits 44–45 of the DSI data bus.
D[44–56]	Input/ Output	**System Bus Data 44–45** For write transactions, the bus master drives valid data on this bus. For read transactions, the slave drives valid data on this bus.
Reserved	Input	If the Ethernet port is enabled and multiplexed with the DSI/System bus, these signals are reserved and can be left unconnected.

Table 1-5. DSI, System Bus, Ethernet, and Interrupt Signals (Continued)

Signal Name	Type	Description
HD46	Input/ Output	**Host Data Bus 46** Bit 46 of the DSI data bus.
D46	Input/ Output	**System Bus Data 46** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHTXD0	Output	**Ethernet Transmit Data 0** In MII and RMII modes, bit 0 of the Ethernet transmit data.
HD47	Input/ Output	**Host Data Bus 47** Bit 47 of the DSI data bus.
D47	Input/ Output	**System Bus Data 47** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHTXD1	Output	**Ethernet Transmit Data 1** In MII and RMII modes, bit 1 of the Ethernet transmit data.
HD48	Input/ Output	**Host Data Bus 48** Bit 48 of the DSI data bus.
D48	Input/ Output	**System Bus Data 48** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHTXD2	Output	**Ethernet Transmit Data 2** In MII mode only, bit 2 of the Ethernet transmit data.
Reserved	Input	In RMII mode, this signal is reserved and can be left unconnected.
HD49	Input/ Output	**Host Data Bus 49** Bit 49 of the DSI data bus.
D49	Input/ Output	**System Bus Data 49** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHTXD3	Output	**Ethernet Transmit Data 3** In MII mode only, bit 3 of the Ethernet transmit data.
Reserved	Input	In RMII mode, this signal is reserved and can be left unconnected.
HD[50–53]	Input/ Output	**Host Data Bus 50–53** Bits 50–53 of the DSI data bus.
D[50–53]	Input/ Output	**System Bus Data 50–53** For write transactions, the bus master drives valid data on this bus. For read transactions, the slave drives valid data on this bus.
Reserved	Input	If the Ethernet port is enabled and multiplexed with the DSI/System bus, these signals are reserved and can be left unconnected.
HD54	Input/ Output	**Host Data Bus 54** Bit 54 of the DSI data bus.
D54	Input/ Output	**System Bus Data 54** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHTX_EN	Output	**Ethernet Transmit Data Enable** In MII and RMII modes, indicates that the transmit data is valid.

Table 1-5. DSI, System Bus, Ethernet, and Interrupt Signals (Continued)

Signal Name	Type	Description
HD55	Input/ Output	**Host Data Bus 55** Bit 55 of the DSI data bus.
D55	Input/ Output	**System Bus Data 55** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHTX_ER	Output	**Ethernet Transmit Data Error** In MII mode only, indicates a transmit data error.
Reserved	Input	In RMII mode, this signal is reserved and can be left unconnected.
HD56	Input/ Output	**Host Data Bus 56** Bit 56 of the DSI data bus.
D56	Input/ Output	**System Bus Data 56** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHRX_DV	Input	**Ethernet Receive Data Valid** Indicates that the receive data is valid.
ETHCRS_DV	Input	**Ethernet Carrier Sense/Receive Data Valid** In RMII mode, indicates that a carrier is detected and after the connection is established that the receive data is valid.
HD57	Input/ Output	**Host Data Bus 57** Bit 57 of the DSI data bus.
D57	Input/ Output	**System Bus Data 57** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHRX_ER	Input	**Ethernet Receive Data Error** In MII and RMII modes, indicates a receive data error.
HD58	Input/ Output	**Host Data Bus 58** Bit 58 of the DSI data bus.
D58	Input/ Output	**System Bus Data 58** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHMDC	Output	**Ethernet Management Clock** In MII and RMII modes, used for the MDIO reference clock.
HD59	Input/ Output	**Host Data Bus 59** Bit 59 of the DSI data bus.
D59	Input/ Output	**System Bus Data 59** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHMDIO	Input/ Output	**Ethernet Management Data** In MII and RMII modes, used for station management data input/output.

Table 1-5. DSI, System Bus, Ethernet, and Interrupt Signals (Continued)

Signal Name	Type	Description
HD60	Input/ Output	**Host Data Bus 60** Bit 60 of the DSI data bus.
D60	Input/ Output	**System Bus Data 60** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHCOL	Input/ Output	**Ethernet Collision** In MII mode only, indicates that a collision was detected.
Reserved	Input	In RMII mode, this signal is reserved and can be left unconnected.
HD[61–63]	Input/ Output	**Host Data Bus 61–63** Bits 61–63 of the DSI data bus.
D[61–63]	Input/ Output	**System Bus Data 61–63** For write transactions, the bus master drives valid data on this bus. For read transactions, the slave drives valid data on this bus.
Reserved	Input	If the Ethernet port is enabled and multiplexed with the DSI/System bus, these signals are reserved and can be left unconnected.
HCID[0–2]	Input	**Host Chip ID 0–2** With HCID3, carries the chip ID of the DSI. The DSI is accessed only if $\overline{\text{HCS}}$ is asserted and HCID[0–3] matches the Chip_ID, or if $\overline{\text{HBCS}}$ is asserted.
HCID3	Input	**Host Chip ID 3** With HCI[0–2], carries the chip ID of the DSI. The DSI is accessed only if $\overline{\text{HCS}}$ is asserted and HCID[0–3] matches the Chip_ID, or if $\overline{\text{HBCS}}$ is asserted.
HA8	Input	**Host Bus Address 8** Used by an external host to access the internal address space.
HA[11–29]	Input	**Host Bus Address 11–29** Used by external host to access the internal address space.
$\overline{\text{HWBS[0–3]}}$	Input	**Host Write Byte Strobes** (In Asynchronous dual mode) One bit per byte is used as a strobe for host write accesses.
$\overline{\text{HDBS[0–3]}}$	Input	**Host Data Byte Strobe** (in Asynchronous single mode) One bit per byte is used as a strobe for host read or write accesses
$\overline{\text{HWBE[0–3]}}$	Input	**Host Write Byte Enable** (In Synchronous dual mode) One bit per byte is used to indicate a valid data byte for host read or write accesses.
$\overline{\text{HDBE[0–3]}}$	Input	**Host Data Byte Enable** (in Synchronous single mode) One bit per byte is used as a strobe enable for host write accesses

Table 1-5. DSI, System Bus, Ethernet, and Interrupt Signals (Continued)

Signal Name	Type	Description
$\overline{\text{HWBS[4–7]}}$	Input	**Host Write Byte Strobes** (In Asynchronous dual mode) One bit per byte is used as a strobe for host write accesses.
$\overline{\text{HDBS[4–7]}}$	Input	**Host Data Byte Strobe** (in Asynchronous single mode) One bit per byte is used as a strobe for host read or write accesses
$\overline{\text{HWBE[4–7]}}$	Input	**Host Write Byte Enable** (In Synchronous dual mode) One bit per byte is used to indicate a valid data byte for host write accesses.
$\overline{\text{HDBE[4–7]}}$	Input	**Host Data Byte Enable** (in Synchronous single mode) One bit per byte is used as a strobe enable for host read or write accesses
$\overline{\text{PWE[4–7]}}$	Output	**System Bus Write Enable** Outputs of the bus general-purpose chip-select machine (GPCM). These signals select byte lanes for write operations.
$\overline{\text{PSDDQM[4–7]}}$	Output	**System Bus SDRAM DQM** From the SDRAM control machine. These signals select specific byte lanes of SDRAM devices.
$\overline{\text{PBS[4–7]}}$	Output	**System Bus UPM Byte Select** From the UPM in the memory controller, these signals select specific byte lanes during memory operations. The timing of these signals is programmed in the UPM. The actual driven value depends on the address and size of the transaction and the port size of the accessed device.
$\overline{\text{HRDS}}$	Input	**Host Read Data Strobe** (In Asynchronous dual mode) Used as a strobe for host read accesses.
HRW	Input	**Host Read/Write Select** (in Asynchronous/Synchronous single mode) Host read/write select.
$\overline{\text{HRDE}}$	Input	**Host Read Data Enable** (In Synchronous dual mode) Indicates valid data for host read accesses.
$\overline{\text{HBRST}}$	Input	**Host Burst** The host asserts this signal to indicate that the current transaction is a burst transaction in synchronous mode only.
HDST[0–1]	Input	**Host Data Structure 0–1** Defines the data structure of the host access in DSI little-endian mode.
HA[9–10]		**Host Bus Address 9–10** Used by an external host to access the internal address space.
$\overline{\text{HCS}}$	Input	**Host Chip Select** DSI chip select. The DSI is accessed only if $\overline{\text{HCS}}$ is asserted and HCID[0–3] matches the Chip_ID.
$\overline{\text{HBCS}}$	Input	**Host Broadcast Chip Select** DSI chip select for broadcast mode. Enables more than one DSI to share the same host chip-select signal for broadcast write accesses.
$\overline{\text{HTA}}$	Output	**Host Transfer Acknowledge** Upon a read access, indicates to the host when the data on the data bus is valid. Upon a write access, indicates to the host that the data on the data bus was written to the DSI write buffer.
HCLKIN	Input	**Host Clock Input** Host clock signal for DSI synchronous mode.
A[0–31]	Input/ Output	**Address Bus** When the MSC8126 is in external master bus mode, these signals function as the system address bus. The MSC8126 drives the address of its internal bus masters and responds to addresses generated by external bus masters. When the MSC8126 is in internal master bus mode, these signals are used as address lines connected to memory devices and are controlled by the MSC8126 memory controller.
TT0	Input/ Output	**Bus Transfer Type 0** The bus master drives this signals during the address tenure to specify the type of the transaction.
HA7		**Host Bus Address 7** Used by an external host to access the internal address space.

Table 1-5. DSI, System Bus, Ethernet, and Interrupt Signals (Continued)

Signal Name	Type	Description
TT1	Input/ Output	**Bus Transfer Type 1** The bus master drives this signals during the address tenure to specify the type of the transaction. Some applications use only the TT1 signal, for example, from MSC8126 to MSC8126 or MSC8126 to MSC8101 and *vice versa*. In these applications, TT1 functions as read/write signal.
TT[2–4]	Input/ Output	**Bus Transfer Type 2–4** The bus master drives these signals during the address tenure to specify the type of the transaction.
CS[5–7]	Output	**Chip Select 5–7** Enables specific memory devices or peripherals connected to the system bus.
CS[0–4]	Output	**Chip Select 0–4** Enables specific memory devices or peripherals connected to the system bus.
TSZ[0–3]	Input/ Output	**Transfer Size 0–3** The bus master drives these signals with a value indicating the number of bytes transferred in the current transaction.
TBST	Input/ Output	**Bus Transfer Burst** The bus master asserts this signal to indicate that the current transaction is a burst transaction (transfers eight words).
IRQ1	Input	**Interrupt Request 1**[1] One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GBL	Output	**Global**[1] When a master within the MSC8126 initiates a bus transaction, it drives this signal. This signal indicates whether the transfer is global and should be snooped by caches in the system.
IRQ3	Input	**Interrupt Request 3**[1] One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
BADDR31	Output	**Burst Address 31**[1] One of five burst address outputs of the memory controller. These signals connect directly to burstable memory devices without internal address incrementors controlled by the MSC8126 memory controller.
IRQ2	Input	**Interrupt Request 2**[1] One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
BADDR30	Output	**Burst Address 30**[1] One of five address outputs of the memory controller. These signals connect directly to burstable memory devices without internal address incrementors controlled by the MSC8126 memory controller.
IRQ5	Input	**Interrupt Request 5**[1] One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
BADDR29	Output	**Bus Burst Address 29**[1] One of five burst address outputs of the memory controller. These signals connect directly to burstable memory devices without internal address incrementors controlled by the MSC8126 memory controller.
BADDR28	Output	**Burst Address 28** One of five burst address outputs of the memory controller. These signals connect directly to burstable memory devices without internal address incrementors controlled by the MSC8126 memory controller.
BADDR27	Output	**Burst Address 27** One of five burst address outputs of the memory controller. These signals connect directly to burstable memory devices without internal address incrementors controlled by the MSC8126 memory controller.
BR	Input/ Output	**Bus Request**[2] When an external arbiter is used, the MSC8126 asserts this signal as an output to request ownership of the bus. When the MSC8126 controller is used as an internal arbiter, an external master asserts this signal as an input to request bus ownership.

Table 1-5. DSI, System Bus, Ethernet, and Interrupt Signals (Continued)

Signal Name	Type	Description
$\overline{BG}$	Input/ Output	**Bus Grant**[2] When the MSC8126 acts as an internal arbiter, it asserts this signal as an output to grant bus ownership to an external bus master. When an external arbiter is used, it asserts this signal as an input to grant bus ownership to the MSC8126.
$\overline{DBG}$	Input/ Output	**Data Bus Grant**[2] When the MSC8126 acts as an internal arbiter, it asserts this signal as an output to grant data bus ownership to an external bus master. When an external arbiter is used, it asserts this signal as an input to grant data bus ownership to the MSC8126.
$\overline{ABB}$	Input/ Output	**Address Bus Busy**[1] The MSC8126 asserts this signal as an output for the duration of the address bus tenure. Following an $\overline{AACK}$, which terminates the address bus tenure, the MSC8126 deasserts $\overline{ABB}$ for a fraction of a bus cycle and then stops driving this signal. The MSC8126 does not assume bus ownership as long as it senses this signal is asserted as an input by an external bus master.
$\overline{IRQ4}$	Input	**Interrupt Request 4** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
$\overline{DBB}$	Input/ Output	**Data Bus Busy**[1] The MSC8126 asserts this signal as an output for the duration of the data bus tenure. Following a $\overline{TA}$, which terminates the data bus tenure, the MSC8126 deasserts $\overline{DBB}$ for a fraction of a bus cycle and then stops driving this signal. The MSC8126 does not assume data bus ownership as long as it senses that this signal is asserted as an input by an external bus master.
$\overline{IRQ5}$	Input	**Interrupt Request 5** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
$\overline{TS}$	Input/ Output	**Bus Transfer Start** This signal indicates the beginning of a new address bus tenure. The MSC8126 asserts this signal when one of its internal bus masters begins an address tenure. When the MSC8126 senses that this signal is asserted by an external bus master, it responds to the address bus tenure as required (snoop if enabled, access internal MSC8126 resources, memory controller support).
$\overline{AACK}$	Input/ Output	**Address Acknowledge** A bus slave asserts this signal to indicate that it has identified the address tenure. This signal terminates the address tenure.
$\overline{ARTRY}$	Input/ Output	**Address Retry** This signal indicates whether the bus master should retry the bus transaction. An external master asserts this signal to enforce data coherency with its caches and to prevent deadlock situations.
D[0–31]	Input/ Output	**Data Bus Bits 0–31** In write transactions, the bus master drives the valid data on this bus. In read transactions, the slave drives the valid data on this bus.
Reserved	Input	The primary configuration selection (default after reset) is reserved.
DP0	Input/ Output	**System Bus Data Parity 0** The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 0 signal should give odd parity (odd number of ones) on the group of signals that includes data parity 0 and D[0–7].
DREQ1	Input	**DMA Request 1** Used by an external peripheral to request DMA service.
$\overline{EXT_BR2}$	Input	**External Bus Request 2** An external master asserts this signal to request bus ownership from the internal arbiter.

Table 1-5. DSI, System Bus, Ethernet, and Interrupt Signals (Continued)

Signal Name	Type	Description
$\overline{\text{IRQ1}}$	Input	**Interrupt Request 1** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP1	Input/ Output	**System Bus Data Parity** 1 The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 1 signal should give odd parity (odd number of ones) on the group of signals that includes data parity 1 and D[8–15].
$\overline{\text{DACK1}}$	Output	**DMA Acknowledge 1** The DMA controller drives this output to acknowledge the DMA transaction on the bus.
$\overline{\text{EXT_BG2}}$	Output	**External Bus Grant 2**[2] The MSC8126 asserts this signal to grant bus ownership to an external bus master.
$\overline{\text{IRQ2}}$	Input	**Interrupt Request 2** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP2	Input/ Output	**System Bus Data Parity 2** The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 2 signal should give odd parity (odd number of ones) on the group of signals that includes data parity 2 and D[16–23].
$\overline{\text{DACK2}}$	Output	**DMA Acknowledge 2** The DMA controller drives this output to acknowledge the DMA transaction on the bus.
$\overline{\text{EXT_DBG2}}$	Output	**External Data Bus Grant 2**[2] The MSC8126 asserts this signal to grant data bus ownership to an external bus master.
$\overline{\text{IRQ3}}$	Input	**Interrupt Request 3** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP3	Input/ Output	**System Bus Data Parity 3** The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 3 signal should give odd parity (odd number of ones) on the group of signals that includes data parity 3 and D[24–31].
DREQ2	Input	**DMA Request 2** Used by an external peripheral to request DMA service.
$\overline{\text{EXT_BR3}}$	Input	**External Bus Request 3**[2] An external master should assert this signal to request bus ownership from the internal arbiter.
$\overline{\text{IRQ4}}$	Input	**Interrupt Request 4** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP4	Input/ Output	**System Bus Data Parity 4** The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 4 signal should give odd parity (odd number of ones) on the group of signals that includes data parity 4 and D[32–39].
$\overline{\text{DACK3}}$	Output	**DMA Acknowledge 3** The DMA controller drives this output to acknowledge the DMA transaction on the bus.
$\overline{\text{EXT_DBG3}}$	Output	**External Data Bus Grant 3**[2] The MSC8126 asserts this signal to grant data bus ownership to an external bus master.

Table 1-5. DSI, System Bus, Ethernet, and Interrupt Signals (Continued)

Signal Name	Type	Description
$\overline{\text{IRQ5}}$	Input	**Interrupt Request 5** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP5	Input/ Output	**System Bus Data Parity 5** The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 5 signal should give odd parity (odd number of ones) on the group of signals that includes data parity 5 and D[40–47].
$\overline{\text{DACK4}}$	Output	**DMA Acknowledge 4** The DMA controller drives this output to acknowledge the DMA transaction on the bus.
$\overline{\text{EXT_BG3}}$	Output	**External Bus Grant 3**[2] The MSC8126 asserts this signal to grant bus ownership to an external bus.
$\overline{\text{IRQ6}}$	Input	**Interrupt Request 6** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP6	Input/ Output	**System Bus Data Parity 6** The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 6 signal should give odd parity (odd number of ones) on the group of signals that includes data parity 6 and D[48–55].
DREQ3	Input	**DMA Request 3** Used by an external peripheral to request DMA service.
$\overline{\text{IRQ7}}$	Input	**Interrupt Request 7** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP7	Input/ Output	**System Bus Data Parity 7** The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 7 signal should give odd parity (odd number of ones) on the group of signals that includes data parity 7 and D[56–63].
DREQ4	Input	**DMA Request 4** Used by an external peripheral to request DMA service.
$\overline{\text{TA}}$	Input/ Output	**Transfer Acknowledge** Indicates that a data beat is valid on the data bus. For single-beat transfers, $\overline{\text{TA}}$ assertion indicates the termination of the transfer. For burst transfers, $\overline{\text{TA}}$ is asserted eight times to indicate the transfer of eight data beats, with the last assertion indicating the termination of the burst transfer.
$\overline{\text{TEA}}$	Input/ Output	**Transfer Error Acknowledge** This signal indicates a failure of the data tenure transaction.The masters within the MSC8126 monitor the state of this signal. The MSC8126 internal bus monitor can assert this signal if it identifies a bus transfer that does not complete.
$\overline{\text{NMI}}$	Input	**Non-Maskable Interrupt** When an external device asserts this line, it generates an non-maskable interrupt in the MSC8126, which is processed internally (default) or is directed to an external host for processing (see $\overline{\text{NMI_OUT}}$).
$\overline{\text{NMI_OUT}}$	Output	**Non-Maskable Interrupt Output** An open-drain signal driven from the MSC8126 internal interrupt controller. This output indicates whether a non-maskable interrupt is pending in the MSC8126 internal interrupt controller, waiting to be handled by an external host.
$\overline{\text{PSDVAL}}$	Input/ Output	**Port Size Data Valid** Indicates that a data beat is valid on the data bus. The difference between the $\overline{\text{TA}}$ signal and the $\overline{\text{PSDVAL}}$ signal is that the $\overline{\text{TA}}$ signal is asserted to indicate data transfer terminations, while the $\overline{\text{PSDVAL}}$ signal is asserted with each data beat movement. When $\overline{\text{TA}}$ is asserted, $\overline{\text{PSDVAL}}$ is always asserted. However, when $\overline{\text{PSDVAL}}$ is asserted, $\overline{\text{TA}}$ is not necessarily asserted. For example, if the DMA controller initiates a double word (2×64 bits) transaction to a memory device with a 32-bit port size, $\overline{\text{PSDVAL}}$ is asserted three times without $\overline{\text{TA}}$ and, finally, both signals are asserted to terminate the transfer.

Table 1-5. DSI, System Bus, Ethernet, and Interrupt Signals (Continued)

Signal Name	Type	Description
IRQ7	Input	**Interrupt Request 7** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
INT_OUT	Output	**Interrupt Output** This output indicates whether an unmasked interrupt is pending in the MSC8126 internal interrupt controller.

Notes: **1.** See the System Interface Unit (SIU) chapter in the *MSC8126 Reference Manual* for details on how to configure these signals.
2. When used as the bus control arbiter, the MSC8126 can support up to three external bus masters. Each master uses its own set of Bus Request, Bus Grant, and Data Bus Grant signals (BR/BG/DBG, EXT_BR2/EXT_BG2/EXT_DBG2, and EXT_BR3/EXT_BG3/EXT_DBG3). Each of these signal sets must be configured to indicate whether the external master is or is not a MSC8126 master device. See the Bus Configuration Register (BCR) description in the System Interface Unit (SIU) chapter in the *MSC8126 Reference Manual* for details on how to configure these signals. The second and third set of signals is defined by EXT_xxx to indicate that they can only be used with external master devices. The first set of signals (BR/BG/DBG) have a dual function. When the MSC8126 is not the bus arbiter, it uses these signals (BR/BG/DBG) to obtain master control of the bus.

1.5 Memory Controller Signals

Refer to the Memory Controller chapter in the *MSC8126 Reference Manual* for details on configuring these signals.

Table 1-6. Memory Controller Signals

Signal Name	Type	Description
BCTL0	Output	**System Bus Buffer Control 0** Controls buffers on the data bus. Usually used with BCTL1. The exact function of this signal is defined by the value of SIUMCR[BCTLC].
BCTL1	Output	**System Bus Buffer Control 1** Controls buffers on the data bus. Usually used with BCTL0. The exact function of this signal is defined by the value of SIUMCR[BCTLC].
CS5	Output	**System and Local Bus Chip Select 5** Enables specific memory devices or peripherals connected to MSC8126 buses.
BM[0–2]	Input	**Boot Mode 0–2** Defines the boot mode of the MSC8126. This signal is sampled on PORESET deassertion.
TC[0–2]	Input/ Output	**Transfer Code 0–2** The bus master drives these signals during the address tenure to specify the type of the code.
BNKSEL[0–2]	Output	**Bank Select 0–2** Selects the SDRAM bank when the MSC8126 is in 60x-compatible bus mode.
ALE	Output	**Address Latch Enable** Controls the external address latch used in an external master bus.
PWE[0–3]	Output	**System Bus Write Enable** Outputs of the bus general-purpose chip-select machine (GPCM). These signals select byte lanes for write operations.
PSDDQM[0–3]	Output	**System Bus SDRAM DQM** From the SDRAM control machine. These signals select specific byte lanes of SDRAM devices.
PBS[0–3]	Output	**System Bus UPM Byte Select** From the UPM in the memory controller, these signals select specific byte lanes during memory operations. The timing of these signals is programmed in the UPM. The actual driven value depends on the address and size of the transaction and the port size of the accessed device.

Table 1-6. Memory Controller Signals (Continued)

Signal Name	Type	Description
PSDA10	Output	**System Bus SDRAM A10** From the bus SDRAM controller. The precharge command defines which bank is precharged. When the row address is driven, it is a part of the row address. When column address is driven, it is a part of column address.
PGPL0	Output	**System Bus UPM General-Purpose Line 0** One of six general-purpose output lines from the UPM. The values and timing of this signal are programmed in the UPM.
$\overline{\text{PSDWE}}$	Output	**System Bus SDRAM Write Enable** From the bus SDRAM controller. Should connect to SDRAM WE input.
PGPL1	Output	**System Bus UPM General-Purpose Line 1** One of six general-purpose output lines from the UPM. The values and timing of this signal are programmed in the UPM.
$\overline{\text{POE}}$	Output	**System Bus Output Enable** From the bus GPCM. Controls the output buffer of memory devices during read operations.
$\overline{\text{PSDRAS}}$	Output	**System Bus SDRAM $\overline{\text{RAS}}$** From the bus SDRAM controller. Should connect to SDRAM $\overline{\text{RAS}}$ input.
PGPL2	Output	**System Bus UPM General-Purpose Line 2** One of six general-purpose output lines from the UPM. The values and timing of this signal are programmed in the UPM.
$\overline{\text{PSDCAS}}$	Output	**System Bus SDRAM $\overline{\text{CAS}}$** From the bus SDRAM controller. Should connect to SDRAM $\overline{\text{CAS}}$ input.
PGPL3	Output	**System Bus UPM General-Purpose Line 3** One of six general-purpose output lines from the UPM. The values and timing of this signal are programmed in the UPM.
$\overline{\text{PGTA}}$	Input	**System GPCM TA** Terminates external transactions during GPCM operation. Requires an external pull-up resistor for proper operation.
PUPMWAIT	Input	**System Bus UPM Wait** An external device holds this signal low to force the UPM to wait until the device is ready to continue the operation.
PGPL4	Output	**System Bus UPM General-Purpose Line 4** One of six general-purpose output lines from the UPM. The values and timing of this signal are programmed in the UPM.
$\overline{\text{PPBS}}$	Output	**System Bus Parity Byte Select** In systems that store data parity in a separate chip, this output is used as the byte-select for that chip.
PSDAMUX	Output	**System Bus SDRAM Address Multiplexer** Controls the system bus SDRAM address multiplexer when the MSC8126 is in external master mode.
PGPL5	Output	**System Bus UPM General-Purpose Line 5** One of six general-purpose output lines from the UPM. The values and timing of this signal are programmed in the UPM.

1.6 GPIO, TDM, UART, and Timer Signals

The general-purpose input/output (GPIO), time-division multiplexed (TDM), universal asynchronous receiver/transmitter (UART), and timer signals are grouped together because they use a common set of signal lines. Individual assignment of a signal to a specific signal line is configured through internal registers. **Table 1-7** describes the signals in this group.

Table 1-7. GPIO, TDM, UART, Ethernet, and Timer Signals

Signal Name	Type	Description
GPIO0	Input/ Output	**General-Purpose Input Output 0** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs.
CHIP_ID0	Input	**Chip ID 0** Determines the chip ID of the MSC8126 DSI. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
$\overline{\text{IRQ4}}$	Input	**Interrupt Request 4** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHTXD0	Output	**Ethernet Transmit Data 0** For MII or RMII mode, bit 0 of the Ethernet transmit data.
GPIO1	Input/ Output	**General-Purpose Input Output 1** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs.
TIMER0	Input/ Output	**Timer 0** Each signal is configured as either input to or output from the counter. See the *MSC8126 Reference Manual* for configuration details.
CHIP_ID1	Input	**Chip ID 1** Determines the chip ID of the MSC8126 DSI. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
$\overline{\text{IRQ5}}$	Input	**Interrupt Request 5** One of the fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHTXD1	Output	**Ethernet Transmit Data 1** For MII or RMII mode, bit 1 of the Ethernet transmit data.
GPIO2	Input/ Output	**General-Purpose Input Output 2** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual*.
TIMER1	Input/ Output	**Timer 1** Each signal is configured as either input to or output from the counter. For the configuration of the signal direction, refer to the *MSC8126 Reference Manual*.
CHIP_ID2	Input	**Chip ID 2** Determines the chip ID of the MSC8126 DSI. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
$\overline{\text{IRQ6}}$	Input	**Interrupt Request 6** One of the fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.

Table 1-7. GPIO, TDM, UART, Ethernet, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO3	Input/ Output	**General-Purpose Input Output 3** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM3TSYN	Input/ Output	**TDM3 Transmit Frame Sync** Transmit frame sync for TDM 3.
$\overline{\text{IRQ1}}$	Input	**Interrupt Request 1** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHTXD2	Output	**Ethernet Transmit Data 2** For MII mode only, bit 2 of the Ethernet transmit data.
GPIO4	Input/ Output	**General-Purpose Input Output 4** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM3TCLK	Input	**TDM3 Transmit Clock** Transmit Clock for TDM 3
$\overline{\text{IRQ2}}$	Input	**Interrupt Request 2** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHTX_ER	Output	**Ethernet Transmit Data Error** For MII mode only, indicates whether a transmit data error occurred.
GPIO5	Input/ Output	**General-Purpose Input/Output 5** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM3TDAT	Input/ Output	**TDM3 Serial Transmitter Data** The serial transmit data signal for TDM 3. As an output, it provides the DATA_D signal for TDM 3. For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ3}}$	Input	**Interrupt Request 3** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHRXD3	Input	**Ethernet Receive Data 3** For MII mode only, bit 3 of the Ethernet receive data.
GPIO6	Input/ Output	**General-Purpose Input Output 6** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM3RSYN	Input/ Output	**TDM3 Receive Frame Sync** The receive sync signal for TDM 3. As an input, this can be the DATA_B data signal for TDM 3.For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ4}}$	Input	**Interrupt Request 4** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHRXD2	Input	**Ethernet Receive Data 2** For MII mode only, bit 2 of the Ethernet receive data.

Table 1-7. GPIO, TDM, UART, Ethernet, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO7	Input/ Output	**General-Purpose Input Output 7** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM3RCLK	Input/ Output	**TDM3 Receive Clock** The receive clock signal for TDM 3. As an output, this can be the DATA_C data signal for TDM 3. For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ5}}$	Input	**Interrupt Request 5** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHTXD3	Output	**Ethernet Transmit Data 3** For MII mode only, bit 3 of the Ethernet transmit data.
GPIO8	Input/ Output	**General-Purpose Input Output 8** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM3RDAT	Input/ Output	**TDM3 Serial Receiver Data** The receive data signal for TDM 3. As an input, this can be the DATA_A data signal for TDM 3. For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ6}}$	Input	**Interrupt Request 6** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHCOL	Input	**Ethernet Collision** For MII mode only, indicates whether a collision was detected.
GPIO9	Input/ Output	**General-Purpose Input Output 9** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM2TSYN	Input/ Output	**TDM2 Transmit frame Sync** Transmit Frame Sync for TDM 2.
$\overline{\text{IRQ7}}$	Input	**Interrupt Request 7** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHMDIO	Input/ Output	**Ethernet Management Data** Station management data input/output line in MII, RMII, and SMII modes.
GPIO10	Input/ Output	**General-Purpose Input Output 10** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM2TCLK	Input	**TDM 2 Transmit Clock** Transmit Clock for TDM 2.
$\overline{\text{IRQ8}}$	Input	**Interrupt Request 8** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHRX_DV	Input	**Ethernet Receive Data Valid** In MII mode, this signal indicates that the receive data is valid.
ETHCRS_DV	Input	**Ethernet Carrier Sense/Receive Data Valid** In RMII mode, this signal indicates that a carrier is sense or that the receive data is valid.
NC	Input	**Not Connected** For SMII mode, this signal must be left unconnected.

Table 1-7. GPIO, TDM, UART, Ethernet, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO11	Input/ Output	**General-Purpose Input Output 11** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM2TDAT	Input/ Output	**TDM2 Serial Transmitter Data** The transmit data signal for TDM 2. As an output, this can be the DATA_D data signal for TDM 2. For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ9}}$	Input	**Interrupt Request 9** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHRX_ER	Input	**Ethernet Receive Data Error** In MII and RMII modes, indicates a receive data error.
ETHTXD	Output	**Ethernet Transmit Data** In SMII, used as the Ethernet transmit data line.
GPIO12	Input/ Output	General-Purpose Input Output 12 One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM2RSYN	Input/ Output	**TDM2 Receive Frame Sync** The receive sync signal for TDM 2. As an input, this can be the DATA_B data signal for TDM 2. For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ10}}$	Input	**Interrupt Request 10** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHRXD1	Input	**Ethernet Receive Data 1** Bit 1 of the Ethernet receive data (MII and RMII mode).
ETHSYNC	Output	**Ethernet Sync Signal** In SMII mode, this is the Ethernet sync signal input.
GPIO13	Input/ Output	**General-Purpose Input Output 13** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM2RCLK	Input/ Output	**TDM2 Receive Clock** The receive clock signal for TDM 2. As an input, this can be the DATA_C data signal for TDM 2. For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ11}}$	Input	**Interrupt Request 11** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHMDC	Output	**Ethernet Management Clock** Used for the MDIO reference clock for MII, RMII, and SMII modes.

Table 1-7. GPIO, TDM, UART, Ethernet, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO14	Input/ Output	**General-Purpose Input Output 14** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM2RDAT	Input/ Output Input	**TDM2 Serial Receiver Data** The receive data signal for TDM 2. As an input, this can be the DATA_A data signal for TDM 2. For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ12}}$	Input	**Interrupt Request 12** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHRXD0	Input	**Ethernet Receive Data 0** Bit 0 of the Ethernet receive data (MII and RMII).
NC	Input	**Not Connected** For SMII mode, this signal must be left unconnected.
GPIO15	Input/ Output	**General-Purpose Input Output 15** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM1TSYN	Input/ Output	**TDM1 Transmit frame Sync** Transmit Frame Sync for TDM 1.
DREQ1	Input	**DMA Request 1** Used by an external peripheral to request DMA service.
GPIO16	Input/ Output	**General-Purpose Input Output 16** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM1TCLK	Input	**TDM1 Transmit Clock** Transmit Clock for TDM 1.
$\overline{\text{DONE1}}$	Input/ Output	**DMA Done 1** Signifies that the channel must be terminated. If the DMA controller generates $\overline{\text{DONE}}$, the channel handling this peripheral is inactive. As an input to the DMA controller, $\overline{\text{DONE}}$ closes the channel much like a normal channel closing. See the *MSC8126 Reference Manual* chapters on the DMA controller and GPIO for information on configuring the $\overline{\text{DRACK}}$ or $\overline{\text{DONE}}$ mode and signal direction.
$\overline{\text{DRACK1}}$	Output	**DMA Data Request Acknowledge 1** Asserted by the DMA controller to indicate that the DMA controller has sampled the peripheral request.
GPIO17	Input/ Output	**General-Purpose Input Output 17** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM1TDAT	Input/ Output	**TDM1 Serial Transmitter Data** The transmit data signal for TDM 1. As an output, this can be the DATA_D data signal for TDM 1.For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{DACK1}}$	Output	**DMA Acknowledge 1** The DMA controller drives this output to acknowledge the DMA transaction on the bus.

Table 1-7. GPIO, TDM, UART, Ethernet, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO18	Input/ Output	**General-Purpose Input Output 18** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM1RSYN	Input/ Output	**TDM1 Receive Frame Sync** The receive sync signal for TDM 1. As an input, this can be the DATA_B data signal for TDM 1. For configuration details, refer to the *MSC8126 Reference Manual*.
DREQ2	Input	**DMA Request 1** Used by an external peripheral to request DMA service.
GPIO19	Input/ Output	**General-Purpose Input Output 19** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM1RCLK	Input/ Output	**TDM1 Receive Clock** The receive clock signal for TDM 1. As an input, this can be the DATA_C data signal for TDM 1. For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{DACK2}}$	Output	**DMA Acknowledge 2** The DMA controller drives this output to acknowledge the DMA transaction on the bus.
GPIO20	Input/ Output	**General-Purpose Input Output 20** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM1RDAT	Input/ Output	**TDM1 Serial Receiver Data** The receive data signal for TDM 1. As an input, this can be the DATA_A data signal for TDM 1. For configuration details, refer to the *MSC8126 Reference Manual*.
GPIO21	Input/ Output	**General-Purpose Input Output 21** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM0TSYN	Input/ Output	**TDM0 Transmit frame Sync** Transmit Frame Sync for TDM 0.
GPIO22	Input/ Output	**General-Purpose Input Output 22** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs.For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM0TCLK	Input	**TDM 0 Transmit Clock** Transmit Clock for TDM 0.
$\overline{\text{DONE2}}$	Input/ Output	**DMA Done 2** Signifies that the channel must be terminated. If the DMA generates DONE, the channel handling this peripheral is inactive. As an input to the DMA, DONE closes the channel much like a normal channel closing. **Note:** See the *MSC8126 Reference Manual* chapters on DMA and GPIO for information on configuring the $\overline{\text{DRACK}}$ or $\overline{\text{DONE}}$ mode and signal direction.
$\overline{\text{DRACK2}}$	Output	**DMA Data Request Acknowledge 2** Asserted by the DMA controller to indicate that the DMA controller has sampled the peripheral request.

Table 1-7. GPIO, TDM, UART, Ethernet, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO23	Input/ Output	**General-Purpose Input Output 23** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM0TDAT	Input/ Output	**TDM0 Serial Transmitter Data** The transmit data signal for TDM 0. As an output, this can be the DATA_D data signal for TDM 0. For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ13}}$	Input	**Interrupt Request 13** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO24	Input/ Output	**General-Purpose Input Output 24** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM0RSYN	Input/ Output	**TDM0 Receive Frame Sync** The receive sync signal for TDM 0. As an input, this can be the DATA_B data signal for TDM 0. For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ14}}$	Input	**Interrupt Request 14** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO25	Input/ Output	**General-Purpose Input Output 25** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM0RCLK	Input/ Output	**TDM0 Receive Clock** The receive clock signal for TDM 0. As an input, this can be the DATA_C data signal for TDM 0. For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ15}}$	Input	**Interrupt Request 15** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO26	Input/ Output	**General-Purpose Input Output 26** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM0RDAT	Input/ Output	**TDM0 Serial Receiver Data** The receive data signal for TDM 0. As an input, this can be the DATA_A data signal for TDM 0. For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
GPIO27	Input/ Output	**General-Purpose Input Output 27** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
DREQ1	Input	**DMA Request 1** Used by an external peripheral to request DMA service.
URXD	Input	**UART Receive Data**
GPIO28	Input/ Output	**General-Purpose Input Output 28** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
DREQ2	Input	**DMA Request 2** Used by an external peripheral to request DMA service.
UTXD	Output	**UART Transmit Data**

Table 1-7. GPIO, TDM, UART, Ethernet, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO29	Input/ Output	**General-Purpose Input Output 29** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
CHIP_ID3	Input	**Chip ID 3** Determines the chip ID of the MSC8126 DSI. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
ETHTX_EN	Output	**Ethernet Transmit Enable** Used to enable the Ethernet transmit controller for MII and RMII modes.
GPIO30	Input/ Output	**General-Purpose Input Output 30** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs.For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TIMER2	Input/ Output	**Timer 2** Each signal is configured as either input to the counter or output from the counter. For the configuration of the signal direction, refer to the *MSC8126 Reference Manual*.
TMCLK	Input	**External TIMER Clock** An external timer can connect directly to the SIU as the SIU Clock.
SDA	Input/ Output	**I^2C-Bus Data Line** This is the data line for the I^2C bus.
GPIO31	Input/ Output	**General-Purpose Input Output 31** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or as one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TIMER3	Input/ Output	**Timer 3** Each signal is configured as either input to or output from the counter. For the configuration of the signal direction, refer to the *MSC8126 Reference Manual*.
SCL	Input/ Output	**I^2C-Bus Clock Line** This the clock line for the I^2C bus.

1.7 Dedicated Ethernet Signals

Most of the Ethernet signals are multiplexed with the DSI/system bus and the GPIO ports. There are three additional dedicated Ethernet signals that are described in **Table 1-8.**

Table 1-8. Dedicated Ethernet Signals

Signal Name	Type	Signal Description
ETHRX_CLK	Input	**Receive Clock** In MII and RMII modes, provides the timing reference for the receive signals in MII mode.
ETHSYNC_IN	Input	**Sync Input** In SMII mode, is the sync signal input line.
ETHTX_CLK	Input	**Transmit Clock** In MII mode, provides the timing reference for transmit signals.
ETHREF_CLK	Input	**Reference Clock** In RMII mode, provides the timing reference.
ETHCLOCK	Input	**Ethernet Clock** In SMII mode, provides the Ethernet clock signal.

Table 1-8. Dedicated Ethernet Signals

Signal Name	Type	Signal Description
ETHCRS	Input	**Carrier Sense** In MII mode, indicates that either the transmit or receive medium is non-idle.
ETHRXD	Input	**Ethernet Receive Data** In SMII mode, used for the Ethernet receive data.

1.8 EOnCE Event and JTAG Test Access Port Signals

The MSC8126 uses two sets of debugging signals for the two types of internal debugging modules: EOnCE and the JTAG TAP controller. Each internal SC140 core has an EOnce module, but they are all accessed externally by the same two signals EE0 and EE1. The MSC8126 supports the standard set of test access port (TAP) signals defined by **IEEE** Std 1149.1 Standard Test Access Port and Boundary-Scan Architecture specification and described in **Table 1-9**.

Table 1-9. JTAG TAP Signals

Signal Name	Type	Signal Description
EE0	Input	**EOnCE Event Bit 0** Puts the internal SC140 cores into Debug mode.
EE1	Output	**EOnCE Event Bit 1** Indicates that at least one on-device SC140 core is in Debug mode.
TCK	Input	**Test Clock** Synchronizes the JTAG test logic.
TDI	Input	**Test Data Input** A test data serial signal for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor.
TDO	Output	**Test Data Output** A test data serial signal for test instructions and data. TDO can be tri-stated. The signal is actively driven in the shift-IR and shift-DR controller states and changes on the falling edge of TCK.
TMS	Input	**Test Mode Select** Sequences the test controller state machine, is sampled on the rising edge of TCK, and has an internal pull-up resistor.
$\overline{\text{TRST}}$	Input	**Test Reset** Asynchronously initializes the test controller; must be asserted during power up.

1.9 Reserved Signals

Table 1-10. Reserved Signals

Signal Name	Type	Signal Description
TEST	Input	**Test** For manufacturing testing. You *must* connect this signal to GND.

Specifications 2

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8126 User's Guide* and *MSC8126 Reference Manual*.

Note: The MSC8126 electrical specifications are preliminary and many are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after thorough characterization and device qualifications have been completed.

2.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification never occurs in the same device with a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2-1 describes the maximum electrical ratings for the MSC8126.

Table 2-1. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Core and PLL supply voltage	V_{DD}	–0.2 to 1.6	V
I/O supply voltage	V_{DDH}	–0.2 to 4.0	V
Input voltage	V_{IN}	–0.2 to 4.0	V
Maximum operating temperature: • 400 MHz • 500 MHz	T_J	 105 90	 °C °C
Minimum operating temperature • 400 MHz • 500 MHz	T_J	 –40 0	 °C °C
Storage temperature range	T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in **Table 2-2.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. **Section 4.5**, *Thermal Considerations* includes a formula for computing the chip junction temperature (T_J).

2.2 Recommended Operating Conditions

Table 2-2 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2-2. Recommended Operating Conditions

Rating	Symbol	Value	Unit
Core supply voltage: • 400 MHz • 500 MHz	V_{DD}	 1.14 to 1.26 1.16 to 1.24	 V V
PLL supply voltage: • 400 MHz • 500 MHz	V_{CCSYN}	 1.14 to 1.26 1.16 to 1.24	 V V
I/O supply voltage	V_{DDH}	3.135 to 3.465	V
Input voltage	V_{IN}	–0.2 to V_{DDH}+0.2	V
Operating temperature range: • 400 MHz • 500 MHz	 T_J T_J	 –40 to 105 0 to 90	 °C °C

2.3 Thermal Characteristics

Table 2-3 describes thermal characteristics of the MSC8126 for the FC-PBGA packages.

Table 2-3. Thermal Characteristics for the MSC8126

Characteristic	Symbol	FC-PBGA 20 × 20 mm[5]		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	26	21	°C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$	19	15	°C/W
Junction-to-board (bottom)[4]	$R_{\theta JB}$	9		°C/W
Junction-to-case[5]	$R_{\theta JC}$	0.9		°C/W
Junction-to-package-top[6]	Ψ_{JT}	1		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Section 4.5, *Thermal Considerations* provides a detailed explanation of these characteristics.

2.4 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8126. The measurements in **Table 2-4** assume the following system conditions:

- T_A = 25 °C
- V_{DD} =
  - 400 MHz = 1.14–1.26 V_{DC}
  - 500 MHz = 1.16–1.24 V_{DC}
- V_{DDH} = 3.3 V ± 5% V_{DC}
- GND = 0 V_{DC}

Note: The leakage current is measured for nominal V_{DDH} and V_{DD}.

Table 2-4. DC Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit
Input high voltage[1], all inputs except CLKIN	V_{IH}	2.0	—	3.465	V
Input low voltage[1]	V_{IL}	GND	0	0.4	V
CLKIN input high voltage	V_{IHC}	2.4	3.0	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0	0.4	V
Input leakage current, $V_{IN} = V_{DDH}$	I_{IN}	–1.0	0.09	1	μA
Tri-state (high impedance off state) leakage current, $V_{IN} = V_{DDH}$	I_{OZ}	–1.0	0.09	1	μA
Signal low input current, V_{IL} = 0.4 V[2]	I_L	–1.0	0.09	1	μA
Signal high input current, V_{IH} = 2.0 V[2]	I_H	–1.0	0.09	1	μA
Output high voltage, I_{OH} = –2 mA, except open drain pins	V_{OH}	2.0	3.0	—	V
Output low voltage, I_{OL}= 3.2 mA	V_{OL}	—	0	0.4	V
Internal supply current: • Wait mode • Stop mode	 I_{DDW} I_{DDS}	 — —	 375[3] 290[3]	 — —	 mA mA
Typical power at 400 MHz[4]	P	—	1.15	—	W

Notes:
1. See **Figure 2-1** for undershoot and overshoot voltages.
2. Not tested. Guaranteed by design.
3. Measured for 1.2 V core at 25°C junction temperature.
4. The typical power values were measured using an EFR code with the device running at a junction temperature of 25°C. No peripherals were enabled and the ICache was not enabled. The source code was optimized to use all the ALUs and AGUs and all four cores. It was created using CodeWarrior® 2.5. These values are provided as examples only. Power consumption is application dependent and varies widely. To assure proper board design with regard to thermal dissipation and maintaining proper operating temperatures, evaluate power consumption for your application and use the design guidelines in **Chapter 4** of this document and in *MSC8102, MSC8122, and MSC8126 Thermal Management Design Guidelines* (AN2601).

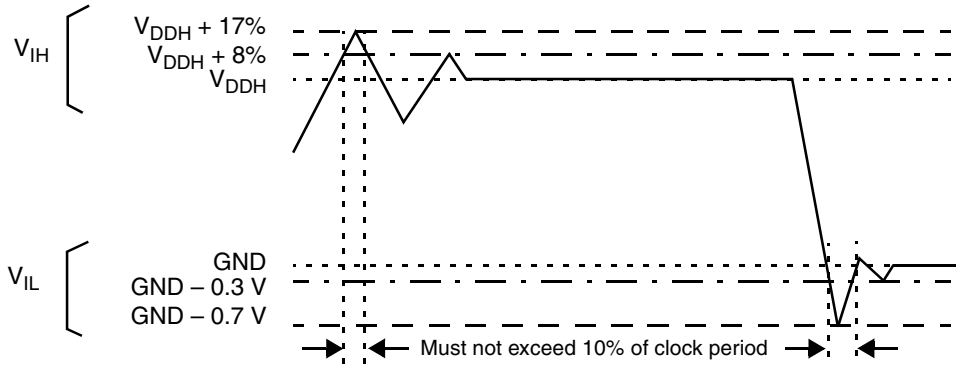


Figure 2-1. Overshoot/Undershoot Voltage for V_{IH} and V_{IL}

2.5 AC Timings

The following sections include illustrations and tables of clock diagrams, signals, and parallel I/O outputs and inputs. When systems such as DSP farms are developed using the DSI, use a device loading of 4 pF per pin. AC timings are based on a 20 pF load, except where noted otherwise, and a 50 Ω transmission line. For loads smaller than 20 pF, subtract 0.06 ns per pF down to 10 pF load. For loads larger than 20 pF, add 0.06 ns for SIU/Ethernet/DSI delay and 0.07 ns for GPIO/TDM/timer delay. When calculating overall loading, also consider additional RC delay.

2.5.1 Output Buffer Impedances

Table 2-5. Output Buffer Impedances

Output Buffers	Typical Impedance (Ω)
System bus	50
Memory controller	50
Parallel I/O	50
Note: These are typical values at 65°C. The impedance may vary by ±25% depending on device process and operating temperature.	

2.5.2 Start-Up Timing

Starting the device requires coordination among several input sequences including clocking, reset, and power. **Section 2.5.3** describes the clocking characteristics. **Section 2.5.4** describes the reset and power-up characteristics. You must use the following guidelines when starting up an MSC8126 device:

- $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ must be asserted externally for the duration of the power-up sequence. See **Table 2-10** for timing.
- If possible, bring up the V_{DD} and V_{DDH} levels together. For designs with separate power supplies, bring up the V_{DD} levels and then the V_{DDH} levels (see **Figure 2-3**).
- CLKIN should start toggling at least 16 cycles (starting after V_{DDH} reaches its nominal level) before $\overline{\text{PORESET}}$ deassertion to guarantee correct device operation (see **Figure 2-2** and **Figure 2-3**).
- CLKIN must not be pulled high during V_{DDH} power-up. CLKIN can toggle during this period.

The following figures show acceptable start-up sequence examples. **Figure 2-2** shows a sequence in which V_{DD} and V_{DDH} are raised together. **Figure 2-3** shows a sequence in which V_{DDH} is raised after V_{DD} and CLKIN begins to toggle as V_{DDH} rises.

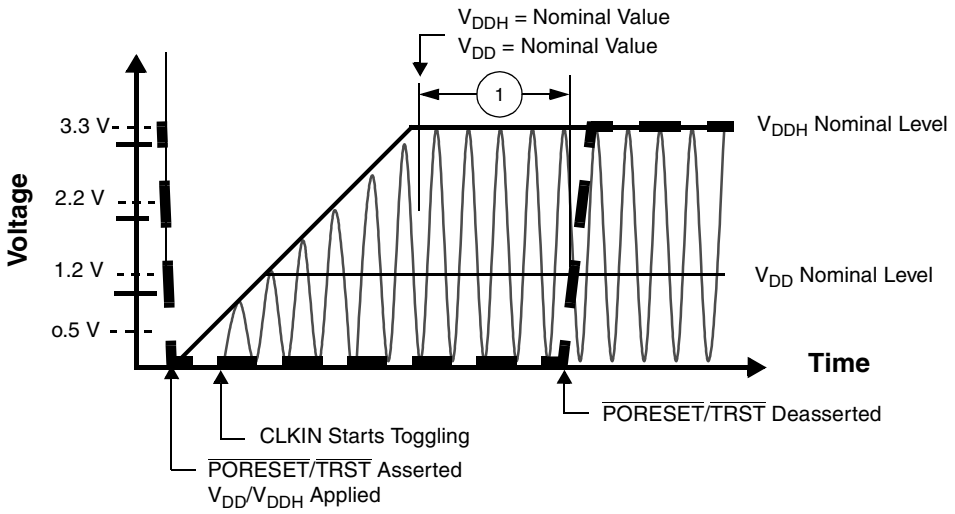


Figure 2-2. Start-Up Sequence with V_{DD} and V_{DDH} Raised Together

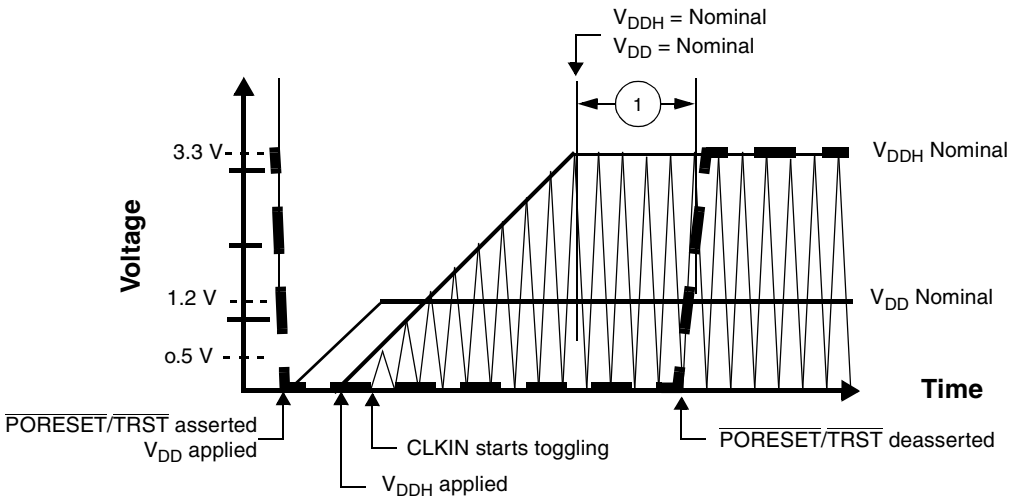


Figure 2-3. Start-Up Sequence with V_{DD} Raised Before V_{DDH} with CLKIN Started with V_{DDH}

2.5.3 Clock and Timing Signals

The following sections include a description of clock signal characteristics. **Table 2-6** shows the maximum frequency values for internal (Core, Reference, Bus, and DSI) and external (CLKIN and CLKOUT) clocks. The user must ensure that maximum frequency values are not exceeded.

Table 2-6. Maximum Frequencies

Characteristic	Maximum in MHz
Core frequency	400/500
Reference frequency (REFCLK)	133/166
Internal bus frequency (BLCK)	133/166
DSI clock frequency (HCLKIN)	HCLKIN ≤(min{100 MHz, CLKOUT})
External clock frequency (CLKIN or CLKOUT)	133/166

Table 2-7. Clock Frequencies

Characteristics	Symbol	400 MHz Device		500 MHz Device	
		Min	Max	Min	Max
CLKIN frequency	F_{CLKIN}	20	133.3	20	166.7
BCLK frequency	F_{BCLK}	40	133.3	40	166.7
Reference clock (REFCLK) frequency	F_{REFCLK}	40	133.3	40	166.7
Output clock (CLKOUT) frequency	F_{CLKOUT}	40	133.3	40	166.7
SC140 core clock frequency	F_{CORE}	200	400	200	500
Note: The rise and fall time of external clocks should be 5 ns maximum					

Table 2-8. System Clock Parameters

Characteristic	Min	Max	Unit
Phase jitter between BCLK and CLKIN	—	0.3	ns
CLKIN frequency	20	see **Table 2-7**	MHz
CLKIN slope	—	3	ns
PLL input clock (after predivider)	20	100	MHz

Table 2-8. System Clock Parameters

Characteristic	Min	Max	Unit
PLL output frequency (VCO output) • 400 MHz core • 500 MHz core	800	 1600 2000	MHz MHz MHz
CLKOUT frequency jitter[1]	—	200	ps
CLKOUT phase jitter[1] with CLKIN phase jitter of ±100 ps	—	500	ps

Notes: **1.** Peak-to-peak.
2. Not tested. Guaranteed by design.

2.5.4 Reset Timing

The MSC8126 has several inputs to the reset logic:

- Power-on reset ($\overline{\text{PORESET}}$)
- External hard reset ($\overline{\text{HRESET}}$)
- External soft reset ($\overline{\text{SRESET}}$)
- Software watchdog reset
- Bus monitor reset
- Host reset command through JTAG

All MSC8126 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. **Table 2-9** describes the reset sources.

Table 2-9. Reset Sources

Name	Direction	Description
Power-on reset ($\overline{\text{PORESET}}$)	Input	Initiates the power-on reset flow that resets the MSC8126 and configures various attributes of the MSC8126. On $\overline{\text{PORESET}}$, the entire MSC8126 device is reset. SPLL states is reset, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are driven, the SC140 extended cores are reset, and system configuration is sampled. The clock mode (MODCK bits), reset configuration mode, boot mode, Chip ID, and use of either a DSI 64 bits port or a System Bus 64 bits port are configured only when $\overline{\text{PORESET}}$ is asserted.
External hard reset ($\overline{\text{HRESET}}$)	Input/ Output	Initiates the hard reset flow that configures various attributes of the MSC8126. While $\overline{\text{HRESET}}$ is asserted, $\overline{\text{SRESET}}$ is also asserted. $\overline{\text{HRESET}}$ is an open-drain pin. Upon hard reset, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are driven, the SC140 extended cores are reset, and system configuration is sampled. The most configurable features are reconfigured. These features are defined in the 32-bit hard reset configuration word described in *Hard Reset Configuration Word* section of the *Reset* chapter in the *MSC8126 Reference Manual*.
External soft reset ($\overline{\text{SRESET}}$)	Input/ Output	Initiates the soft reset flow. The MSC8126 detects an external assertion of $\overline{\text{SRESET}}$ only if it occurs while the MSC8126 is not asserting reset. $\overline{\text{SRESET}}$ is an open-drain pin. Upon soft reset, $\overline{\text{SRESET}}$ is driven, the SC140 extended cores are reset, and system configuration is maintained.
Software watchdog reset	Internal	When the MSC8126 watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence.
Bus monitor reset	Internal	When the MSC8126 bus monitor count reaches zero, a bus monitor hard reset is asserted. The enabled bus monitor event then generates an internal hard reset sequence.
Host reset command through the TAP	Internal	When a host reset command is written through the Test Access Port (TAP), the TAP logic asserts the soft reset signal and an internal soft reset sequence is generated.

Table 2-10 summarizes the reset actions that occur as a result of the different reset sources.

Table 2-10. Reset Actions for Each Reset Source

Reset Action/Reset Source	Power-On Reset ($\overline{\text{PORESET}}$)	Hard Reset ($\overline{\text{HRESET}}$)	Soft Reset ($\overline{\text{SRESET}}$)	
	External only	External or Internal (Software Watchdog or Bus Monitor)	External	JTAG Command: EXTEST, CLAMP, or HIGHZ
Configuration pins sampled (Refer to **Section 2.5.4.1** for details).	Yes	No	No	No
SPLL state reset	Yes	No	No	No
System reset configuration write through the DSI	Yes	No	No	No
System reset configuration write though the system bus	Yes	Yes	No	No
$\overline{\text{HRESET}}$ driven	Yes	Yes	No	No
SIU registers reset	Yes	Yes	No	No
IPBus modules reset (TDM, UART, timers, DSI, IPBus master, GIC, HS, and GPIO)	Yes	Yes	Yes	Yes
$\overline{\text{SRESET}}$ driven	Yes	Yes	Yes	Depends on command
SC140 extended cores reset	Yes	Yes	Yes	Yes
MQBS reset	Yes	Yes	Yes	Yes

2.5.4.1 Power-On Reset ($\overline{\text{PORESET}}$) Pin

Asserting $\overline{\text{PORESET}}$ initiates the power-on reset flow. $\overline{\text{PORESET}}$ must be asserted externally for at least 16 CLKIN cycles after V_{DD} and V_{DDH} are both at their nominal levels.

2.5.4.2 Reset Configuration

The MSC8126 has two mechanisms for writing the reset configuration:

- Through the direct slave interface (DSI)
- Through the system bus. When the reset configuration is written through the system bus, the MSC8126 acts as a configuration master or a configuration slave. If configuration slave is selected, but no special configuration word is written, a default configuration word is applied.

Fourteen signal levels (see **Chapter 1** for signal description details) are sampled on $\overline{\text{PORESET}}$ deassertion to define the reset configuration mode and boot and operating conditions:

- $\overline{\text{RSTCONF}}$
- CNFGS
- DSISYNC
- DSI64
- CHIP_ID[0–3]
- BM[0–2]
- SWTE
- MODCK[1–2]

2.5.4.3 Reset Timing Tables

Table 2-11 and **Figure 2-4** describe the reset timing for a reset configuration write through the direct slave interface (DSI) or through the system bus.

Table 2-11. Timing for a Reset Configuration Write through the DSI or System Bus

No.	Characteristics	Expression	Min	Max	Unit
1	Required external $\overline{\text{PORESET}}$ duration minimum • CLKIN = 20 MHz • CLKIN = 133 MHz (400 MHz core) • CLKIN = 166 MHz (500 MHz core)	16/CLKIN	 800 120 96	 800 — —	 ns ns ns
2	Delay from deassertion of external $\overline{\text{PORESET}}$ to deassertion of internal $\overline{\text{PORESET}}$ • CLKIN = 20 MHz to 166 MHz	1024/CLKIN	 6.17	 51.2	 µs
3	Delay from de-assertion of internal $\overline{\text{PORESET}}$ to SPLL lock • CLKIN = 20 MHz (RDF = 1) • CLKIN = 133 MHz (RDF = 2) (400 MHz core) • CLKIN = 166 MHz (RDF = 2) (500 MHz core)	6400/(CLKIN/RDF) (PLL reference clock-division factor)	 320 96 77	 320 96 77	 µs µs µs
5	Delay from SPLL to $\overline{\text{HRESET}}$ deassertion • REFCLK = 40 MHz to 166 MHz	512/REFCLK	3.08	12.8	µs
6	Delay from SPLL lock to $\overline{\text{SRESET}}$ deassertion • REFCLK = 40 MHz to 166 MHz	515/REFCLK	3.10	12.88	µs
7	Setup time from assertion of $\overline{\text{RSTCONF}}$, CNFGS, DSISYNC, DSI64, CHIP_ID[0–3], BM[0–2], SWTE, and MODCK[1–2] before deassertion of $\overline{\text{PORESET}}$		3	—	ns
8	Hold time from deassertion of $\overline{\text{PORESET}}$ to deassertion of $\overline{\text{RSTCONF}}$, CNFGS, DSISYNC, DSI64, CHIP_ID[0–3], BM[0–2], SWTE, and MODCK[1–2]		5	—	ns
Note:	Timings are not tested, but are guaranteed by design.				

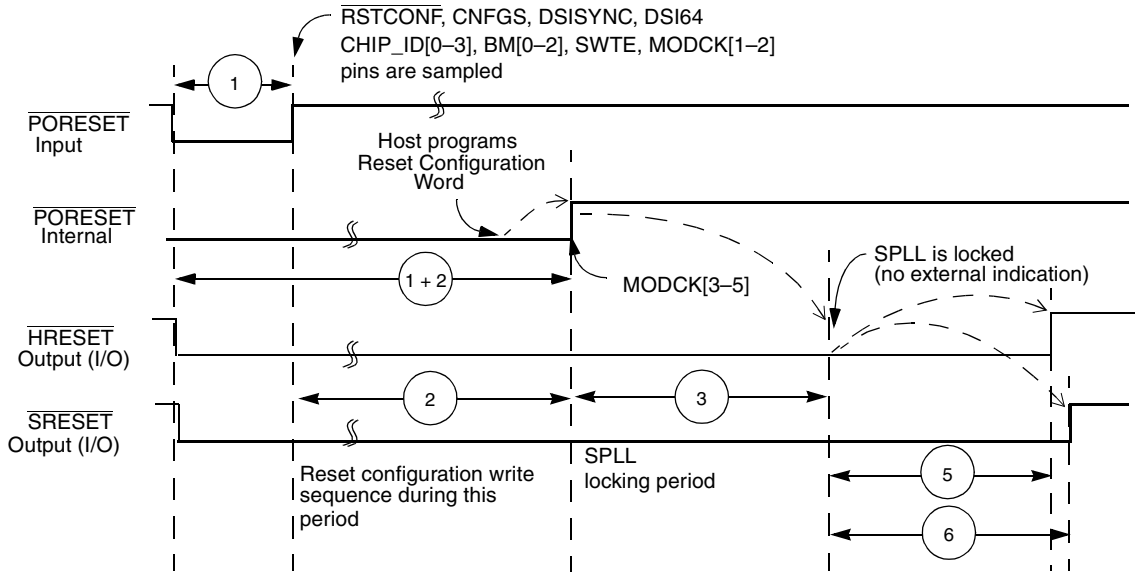


Figure 2-4. Timing Diagram for a Reset Configuration Write

2.5.5 System Bus Access Timing

2.5.5.1 Core Data Transfers

Generally, all MSC8126 bus and system output signals are driven from the rising edge of the reference clock (REFCLK). The REFCLK is the CLKIN signal. Memory controller signals, however, trigger on four points within a REFCLK cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge of REFCLK (and T3 at the falling edge), but the spacing of T2 and T4 depends on the PLL clock ratio selected, as **Table 2-12** shows.

Table 2-12. Tick Spacing for Memory Controller Signals

BCLK/SC140 clock	Tick Spacing (T1 Occurs at the Rising Edge of REFCLK)		
	T2	T3	T4
1:4, 1:6, 1:8, 1:10	1/4 REFCLK	1/2 REFCLK	3/4 REFCLK
1:3	1/6 REFCLK	1/2 REFCLK	4/6 REFCLK
1:5	2/10 REFCLK	1/2 REFCLK	7/10 REFCLK

Figure 2-5 is a graphical representation of **Table 2-12**.

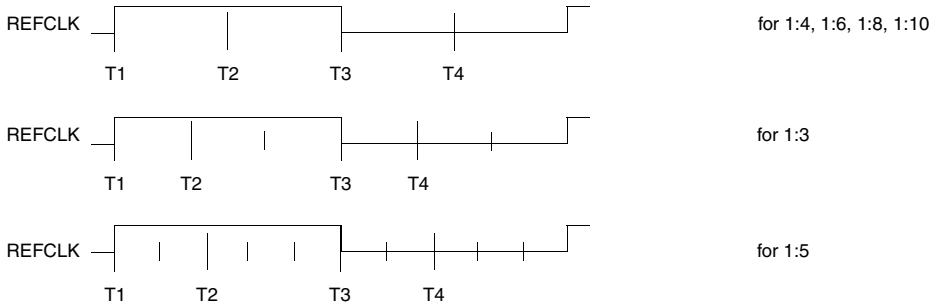


Figure 2-5. Internal Tick Spacing for Memory Controller Signals

The UPM machine and GPCM machine outputs change on the internal tick determined by the memory controller configuration. The AC specifications are relative to the internal tick. SDRAM machine outputs change only on the REFCLK rising edge.

Table 2-13. AC Timing for SIU Inputs

No.	Characteristic	Value for Bus Speed in MHz			Units
		Ref = CLKIN		Ref = CLKOUT	
		133	166	133	
10	Hold time for all signals after the 50% level of the REFCLK rising edge	0.5	0.5	0.5	ns
11a	$\overline{\text{ARTRY}}$/$\overline{\text{ABB}}$ set-up time before the 50% level of the REFCLK rising edge	3.0	3.0	3.0	ns
11b	$\overline{\text{DBG}}$/$\overline{\text{DBB}}$/$\overline{\text{BG}}$/$\overline{\text{BR}}$/$\overline{\text{TC}}$ set-up time before the 50% level of the REFCLK rising edge	3.3	3.3	3.3	ns
11c	$\overline{\text{AACK}}$ set-up time before the 50% level of the REFCLK rising edge	2.9	2.9	2.9	ns
11d	$\overline{\text{TA}}$/$\overline{\text{TEA}}$/$\overline{\text{PSDVAL}}$ set-up time before the 50% level of the REFCLK rising edge • Data-pipeline mode • Non-pipeline mode	 3.4 4.0	 3.4 4.0	 3.4 4.0	 ns ns
12	Data bus set-up time before REFCLK rising edge in Normal mode • Data-pipeline mode • Non-pipeline mode	 1.8 4.0	 1.7 4.0	 1.8 4.0	 ns ns
13	Data bus set-up time before the 50% level of the REFCLK rising edge in ECC and PARITY modes • Data-pipeline mode • Non-pipeline mode	 2.0 7.3	 2.0 7.3	 2.0 7.3	 ns ns
14	DP set-up time before the 50% level of the REFCLK rising edge • Data-pipeline mode • Non-pipeline mode	 2.0 6.1	 2.0 6.1	 2.0 6.1	 ns ns
15a	$\overline{\text{TS}}$ and Address bus set-up time before the 50% level of the REFCLK rising edge • Extra cycle mode (SIUBCR[EXDD] = 0) • No extra cycle mode (SIUBCR[EXDD] = 1)	 3.6 5.0	 3.6 5.0	 3.8 5.0	 ns ns
15b	Address attributes: TT/$\overline{\text{TBST}}$/TSZ/$\overline{\text{GBL}}$ set-up time before the 50% level of the REFCLK rising edge • Extra cycle mode (SIUBCR[EXDD] = 0) • No extra cycle mode (SIUBCR[EXDD] = 1)	 3.5 4.4	 3.5 4.4	 3.5 4.4	 ns ns
16[1]	PUPMWAIT signal set-up time before the 50% level of the REFCLK rising edge	3.7	3.7	3.7	ns
Note:	Values are measured from the 50% TTL transition level relative to the 50% level of the REFCLK rising edge.				

Table 2-14. AC Timing for SIU Outputs

No.	Characteristic	Value for Bus Speed in MHz			Units
		Ref = CLKIN		Ref = CLKOUT	
		133	166	133	
30[2]	Minimum delay from the 50% level of the REFCLK for all signals	0.8	0.8	1.0	ns
31	$\overline{PSDVAL}$/$\overline{TEA}$/$\overline{TA}$ max delay from the 50% level of the REFCLK rising edge	4.9	4.9	5.8	ns
32a	Address bus max delay from the 50% level of the REFCLK rising edge • Multi-master mode (SIUBCR[EBM] = 1) • Single-master mode (SIUBCR[EBM] = 0)	 5.5 4.2	 5.5 3.9	 6.4 5.1	 ns ns
32b	Address attributes: TT[0–1]/$\overline{TBST}$/TSZ/$\overline{GBL}$ max delay from the 50% level of the REFCLK rising edge	5.1	5.1	6.0	ns
32c	Address attributes: TT[2–4]/TC max delay from the 50% level of the REFCLK rising edge	5.7	5.7	6.6	ns
32d	BADDR max delay from the 50% level of the REFCLK rising edge	4.2	4.2	5.1	ns
33a	Data bus max delay from the 50% level of the REFCLK rising edge • Data-pipeline mode • Non-pipeline mode	 3.9 6.1	 3.7 6.1	 4.8 7.0	 ns ns
33b	DP max delay from the 50% level of the REFCLK rising edge • Data-pipeline mode • Non-pipeline mode	 5.3 6.5	 5.3 6.5	 6.2 7.4	 ns ns
34	Memory controller signals/ALE/$\overline{CS[0–4]}$ max delay from the 50% level of the REFCLK rising edge	4.2	3.9	5.1	ns
35a	$\overline{DBG}$/$\overline{BG}$/$\overline{BR}$/$\overline{DBB}$ max delay from the 50% level of the REFCLK rising edge	4.7	4.7	5.6	ns
35b	$\overline{AACK}$/$\overline{ABB}$/$\overline{TS}$/$\overline{CS[5–7]}$ max delay from the 50% level of the REFCLK rising edge	4.5	4.5	5.4	ns

Notes:
1. Values are measured from the 50% level of the REFCLK rising edge to the 50% signal level and assume a 20 pF load except where otherwise specified.
2. The load for specification 30 is 10 pF. The load for the other specifications in this table is 20 pF. For a 15 pF load, subtract 0.3 ns from the listed value.
3. The maximum bus frequency depends on the mode:
   • In 60x-compatible mode connected to another MSC8126 device, the frequency is determined by adding the input and output longest timing values, which results in the total delay for 20 pF output capacitance. You must also account for other influences that can affect timing, such as on-board clock skews, on-board noise delays, and so on.
   • In single-master mode, the frequency depends on the timing of the devices connected to the MSC8126.
   • To achieve maximum performance on the bus in single-master mode, disable the $\overline{DBB}$ signal by writing a 1 to the SIUMCR[BDD] bit. See the SIU chapter in the *MSC8122 Reference Manual* for details.

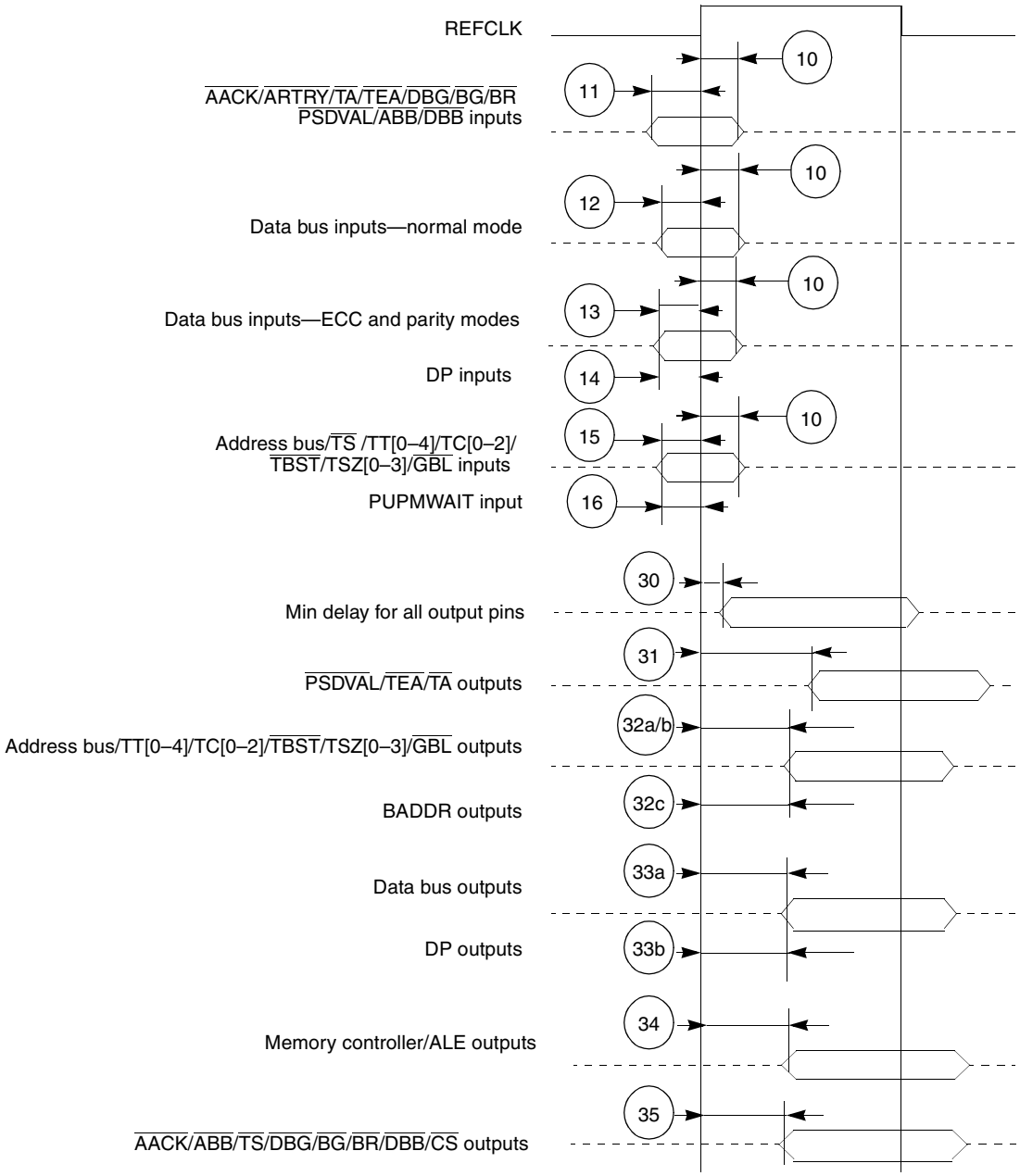


Figure 2-6. Bus Signal Timing

2.5.5.2 CLKIN to CLKOUT Skew

Table 2-15 describes the CLKOUT-to-CLKIN skew timing.

Table 2-15. CLKOUT Skew

No.	Characteristic	Min[1]	Max[1]	Units
20	Rise-to-rise skew	0	0.85	ns
21	Fall-to-fall skew	–0.8	1.0	ns
22	CLKOUT phase high and low (1.2 V, 133 MHz)	2.8	—	ns

Notes:
1. A positive number indicates that CLKOUT precedes CLKIN, A negative number indicates that CLKOUT follows CLKIN.
2. Skews are measured in clock mode 29, with a CLKIN:CLKOUT ratio of 1:1. The same skew is valid for all clock modes.
3. CLKOUT skews are measured using a load of 10 pF.
4. CLKOUT skews and phase are not measured for 500/166 Mhz parts because these parts only use CLKIN mode.

For designs that use the CLKOUT synchronization mode, use the skew values listed in **Table 2-15** to adjust the rise-to-fall timing values specified for CLKIN synchronization. **Figure 2-7** shows the relationship between the CLKOUT and CLKIN timings. CLKOUT synchronization mode is not supported above 400 MHz core operation.

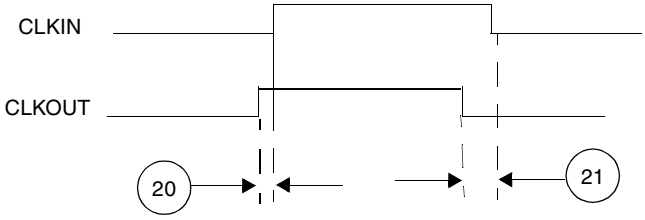


Figure 2-7. CLKOUT and CLKIN Signals.

2.5.5.3 DMA Data Transfers

Table 2-16 describes the DMA signal timing.

Table 2-16. DMA Signals

No.	Characteristic	Ref = CLKIN		Ref = CLKOUT		Units
		Min	Max	Min	Max	
37	DREQ set-up time before the 50% level of the falling edge of REFCLK	5.0	—	5.0	—	ns
38	DREQ hold time after the 50% level of the falling edge of REFCLK	0.5	—	0.5	—	ns
39	$\overline{\text{DONE}}$ set-up time before the 50% level of the rising edge of REFCLK	5.0	—	5.0	—	ns
40	$\overline{\text{DONE}}$ hold time after the 50% level of the rising edge of REFCLK	0.5	—	0.5	—	ns
41	$\overline{\text{DACK}}$/$\overline{\text{DRACK}}$/$\overline{\text{DONE}}$ delay after the 50% level of the REFCLK rising edge	0.5	7.5	0.5	8.4	ns
Note:	CLKOUT synchronization mode is not supported in cores operating above 400 MHz.					

The DREQ signal is synchronized with REFCLK. To achieve fast response, a synchronized peripheral should assert DREQ according to the timings in **Table 2-16**. **Figure 2-8** shows synchronous peripheral interaction.

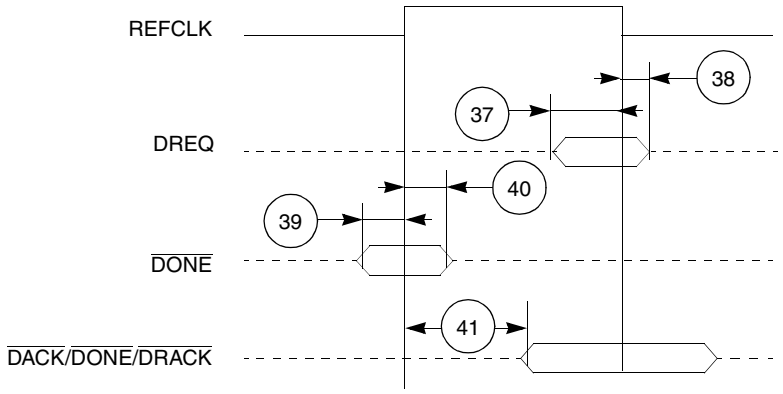


Figure 2-8. DMA Signals

2.5.6 DSI Timing

The timings in the following sections are based on a 20 pF capacitive load.

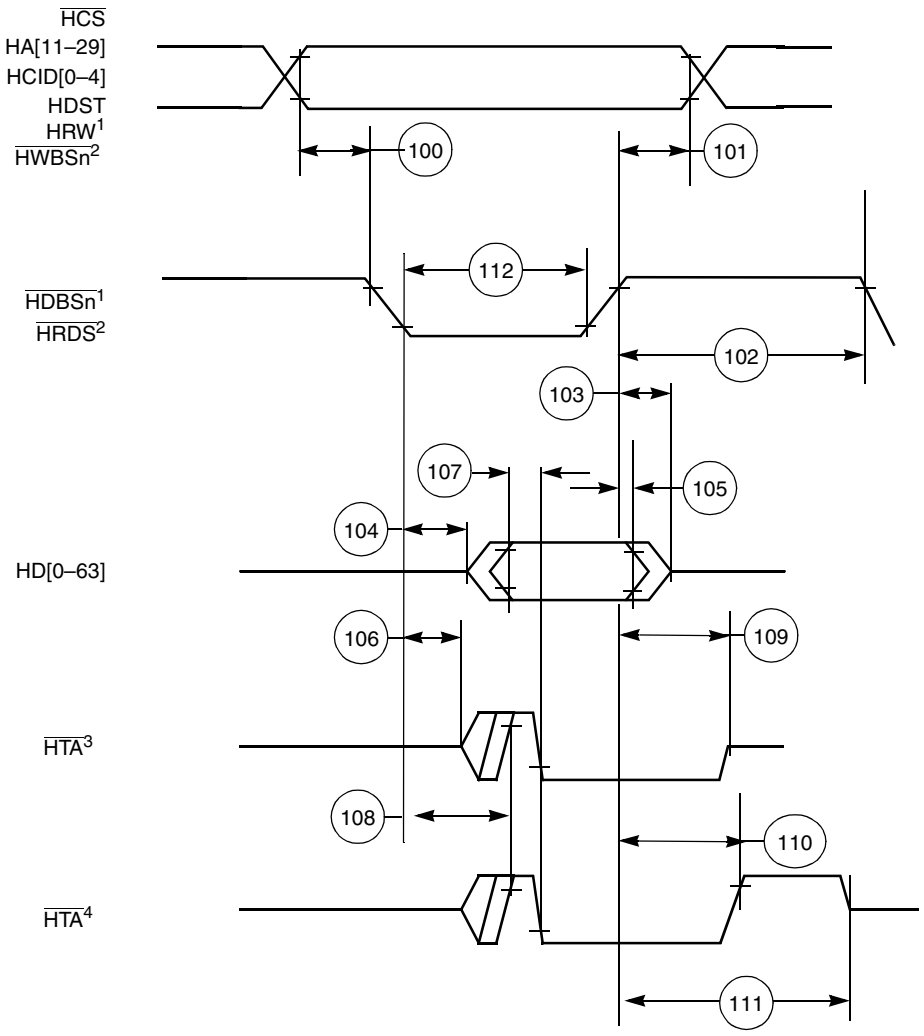
2.5.6.1 DSI Asynchronous Mode

Table 2-17. DSI Asynchronous Mode Timing

No.	Characteristics	Min	Max	Unit
100	Attributes[1] set-up time before strobe ($\overline{\text{HWBS[n]}}$) assertion	1.5	—	ns
101	Attributes[1] hold time after data strobe deassertion	1.3	—	ns
102	Read/Write data strobe deassertion width: • DCR[HTAAD] = 1 — Consecutive access to the same DSI — Different device with DCR[HTADT] = 01 — Different device with DCR[HTADT] = 10 — Different device with DCR[HTADT] = 11 • DCR[HTAAD] = 0	 $1.8 + T_{REFCLK}$ $5 + T_{REFCLK}$ $5 + (1.5 \times T_{REFCLK})$ $5 + (2.5 \times T_{REFCLK})$ $1.8 + T_{REFCLK}$	—	 ns ns ns ns ns
103	Read data strobe deassertion to output data high impedance	—	8.5	ns
104	Read data strobe assertion to output data active from high impedance	2.0	—	ns
105	Output data hold time after read data strobe deassertion	2.2	—	ns
106	Read/Write data strobe assertion to $\overline{\text{HTA}}$ active from high impedance	2.2	—	ns
107	Output data valid to $\overline{\text{HTA}}$ assertion	3.2	—	ns
108	Read/Write data strobe assertion to $\overline{\text{HTA}}$ valid[2]	—	6.7	ns
109	Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ high impedance. (DCR[HTAAD] = 0, $\overline{\text{HTA}}$ at end of access released at logic 0)	—	6.5	ns
110	Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ deassertion. (DCR[HTAAD] = 1, $\overline{\text{HTA}}$ at end of access released at logic 1)	—	6.5	ns
111	Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ high impedance. (DCR[HTAAD] = 1, $\overline{\text{HTA}}$ at end of access released at logic 1 • DCR[HTADT] = 01 • DCR[HTADT] = 10 • DCR[HTADT] = 11	—	 $5 + T_{REFCLK}$ $5 + (1.5 \times T_{REFCLK})$ $5 + (2.5 \times T_{REFCLK})$	 ns ns ns
112	Read/Write data strobe assertion width	$1.8 + T_{REFCLK}$	—	ns
201	Host data input set-up time before write data strobe deassertion	1.0	—	ns
202	Host data input hold time after write data strobe deassertion	1.5	—	ns

Notes:
1. *Attributes* refers to the following signals: $\overline{\text{HCS}}$, HA[11–29], HCID[0–4], HDST, HRW, $\overline{\text{HRDS}}$, and $\overline{\text{HWBSn}}$.
2. This specification is tested in dual strobe mode. Timing in single strobe mode is guaranteed by design.
3. All values listed in this table are tested or guaranteed by design.

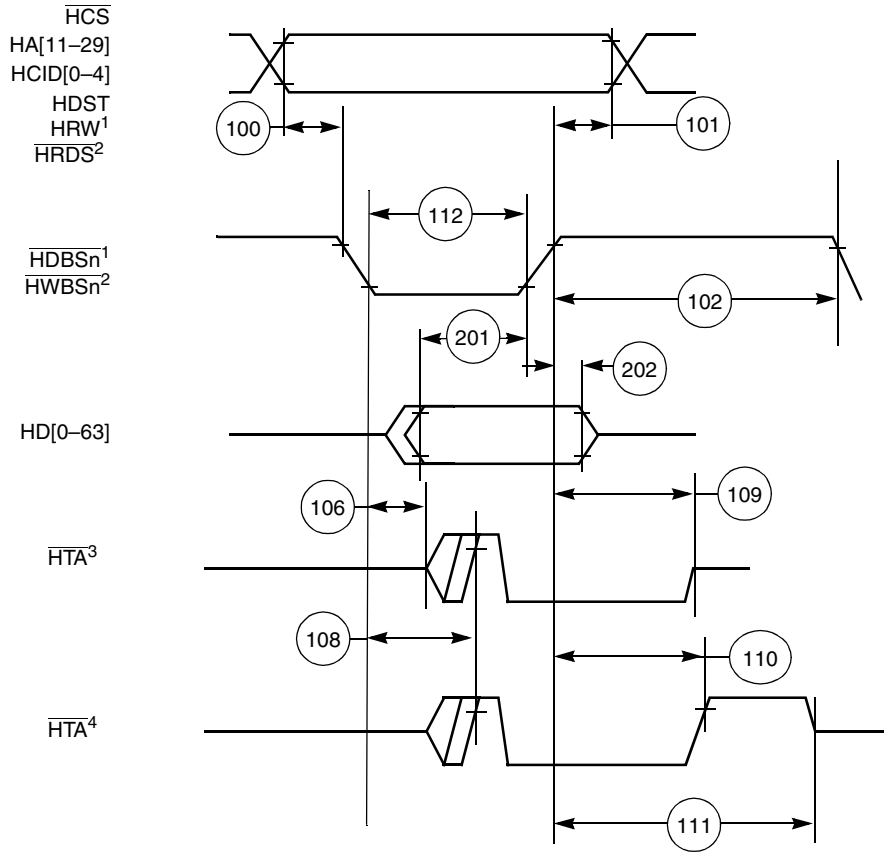
Figure 2-9 shows DSI asynchronous read signals timing.



Notes:
1. Used for single-strobe mode access.
2. Used for dual-strobe mode access.
3. $\overline{\text{HTA}}$ released at logic 0 (DCR[HTAAD] = 0) at end of access; used with pull-down implementation.
4. $\overline{\text{HTA}}$ released at logic 1 (DCR[HTAAD] = 1) at end of access; used with pull-up implementation.

Figure 2-9. Asynchronous Single and Dual Modes Read Timing Diagram

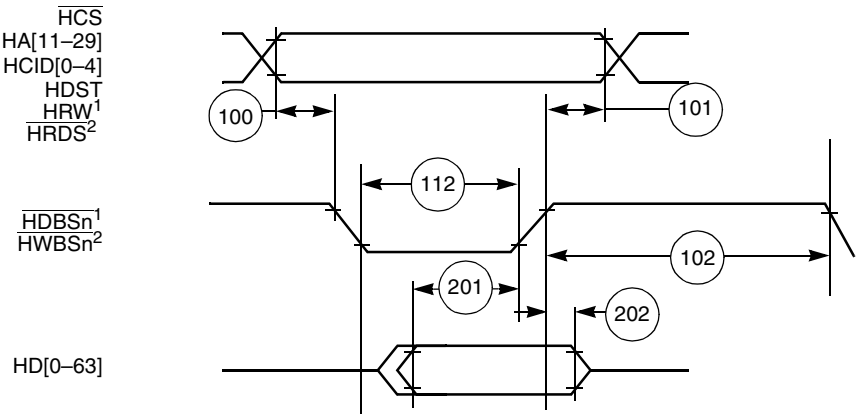
Figure 2-10 shows DSI asynchronous write signals timing.



Notes:
1. Used for single-strobe mode access.
2. Used for dual-strobe mode access.
3. $\overline{\text{HTA}}$ released at logic 0 (DCR[HTAAD] = 0) at end of access; used with pull-down implementation.
4. $\overline{\text{HTA}}$ released at logic 1 (DCR[HTAAD] = 1) at end of access; used with pull-up implementation.

Figure 2-10. Asynchronous Single and Dual Modes Write Timing Diagram

Figure 2-11 shows DSI asynchronous broadcast write signals timing.



Notes:
1. Used for single-strobe mode access.
2. Used for dual-strobe mode access.

Figure 2-11. Asynchronous Broadcast Write Timing Diagram

2.5.6.2 DSI Synchronous Mode

Table 2-18. DSI Inputs—Synchronous Mode

No.	Characteristic	Expression	Min	Max	Units
120	HCLKIN Cycle Time[1, 2]	HTC	10.0	55.6	ns
121	HCLKIN high Pulse Width	$(0.5 \pm 0.1) \times$ HTC	4.0	33.3	ns
122	HCLKIN low Pulse Width	$(0.5 \pm 0.1) \times$ HTC	4.0	33.3	ns
123	HA[11–29] inputs set-up time	—	1.2	—	ns
124	HD[0–63] inputs set-up time	—	0.4	—	ns
125	HCID[0–4] inputs set-up time	—	1.3	—	ns
126	All other inputs set-up time	—	1.2	—	ns
127	All inputs hold time	—	1.5	—	ns

Notes: **1.** Values are based on a frequency range of 18–100 MHz.
2. Refer to **Table 2-6** for HCLKIN frequency limits.

Table 2-19. DSI Outputs—Synchronous Mode

No.	Characteristic	Min	Max	Units
128	HCLKIN high to HD[0–63] output active	2.0	—	ns
129	HCLKIN high to HD[0–63] output valid	—	6.3	ns
130	HD[0–63] output hold time	1.7	—	ns
131	HCLKIN high to HD[0–63] output high impedance	—	7.6	ns
132	HCLKIN high to $\overline{\text{HTA}}$ output active	2.0	—	ns
133	HCLKIN high to $\overline{\text{HTA}}$ output valid	—	5.9	ns
134	$\overline{\text{HTA}}$ output hold time	1.7	—	ns
135	HCLKIN high to $\overline{\text{HTA}}$ high impedance	—	6.3	ns

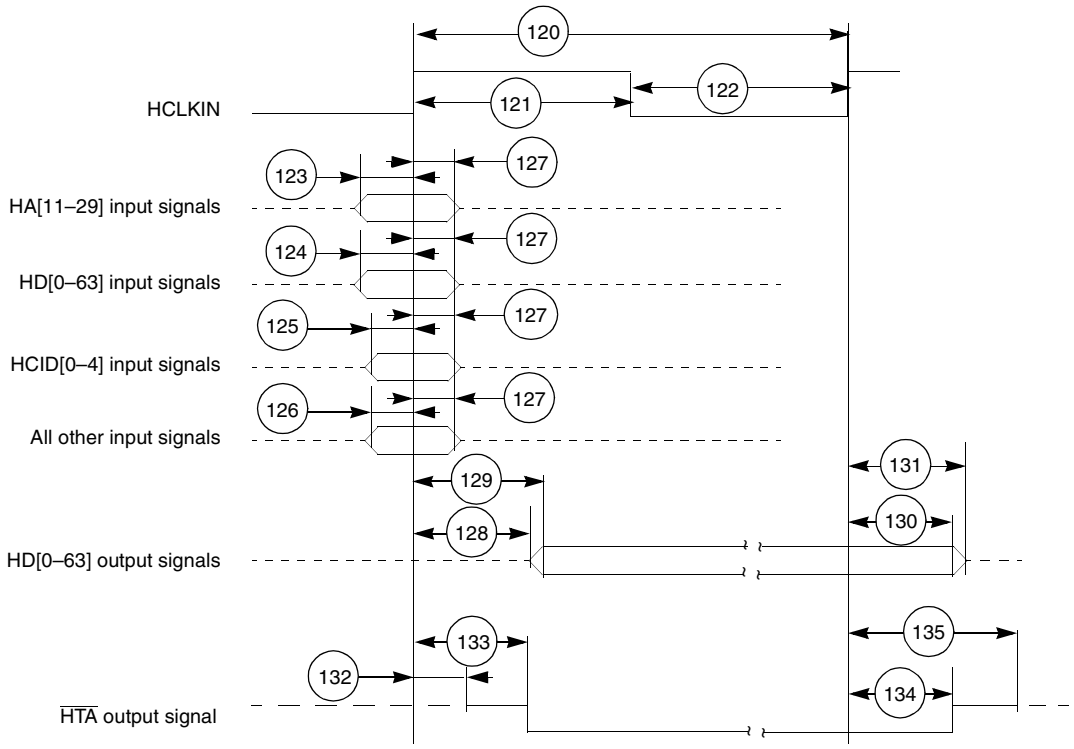


Figure 2-12. DSI Synchronous Mode Signals Timing Diagram

2.5.7 TDM Timing

Table 2-20. TDM Timing

No.	Characteristic	Expression	Ref = CLKIN		Units
			Min	Max	
300	TDMxRCLK/TDMxTCLK	TC[1]	16	—	ns
301	TDMxRCLK/TDMxTCLK high pulse width	(0.5 ±0.1) × TC	7	—	ns
302	TDMxRCLK/TDMxTCLK low pulse width	(0.5 ±0.1) × TC	7	—	ns
303	TDM receive all input set-up time		1.3	—	ns
304	TDM receive all input hold time		1.0	—	ns
305	TDMxTCLK high to TDMxTDAT/TDMxRCLK output active[2,3]		2.8	—	ns
306	TDMxTCLK high to TDMxTDAT/TDMxRCLK output valid[2,3]		—	8.8	ns
307	All output hold time[5]		2.5	—	ns
308	TDMxTCLK high to TDmXTDAT/TDMxRCLK output high impedance[2,3]		—	10.5	ns
309	TDMxTCLK high to TDMXTSYN output valid[2]		—	8.5	ns
310	TDMxTSYN output hold time[5]		2.5	—	ns

Notes:
1. Values are based on a a maximum frequency of 62.5 MHz. The TDM interface supports any frequency below 62.5 MHz.
2. Values are based on 20 pF capacitive load.
3. When configured as an output, TDMxRCLK acts as a second data link. See the *MSC8126 Reference Manual* for details.
4. CLKOUT synchronization is not supported for cores operating at above 400 MHz.
5. Values are based on 10 pF capacitive load.

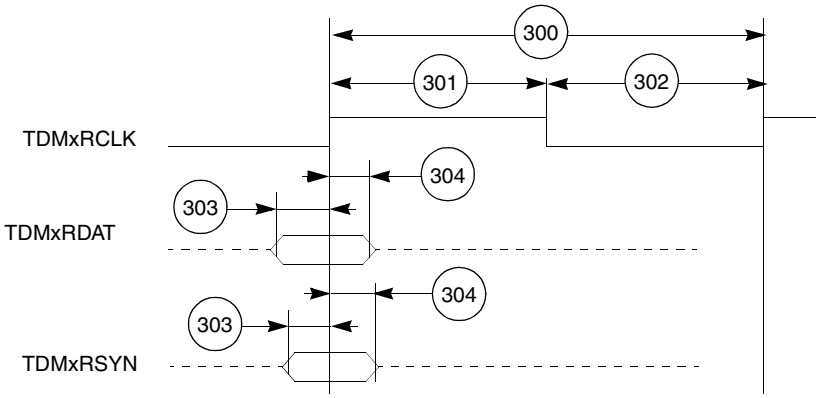


Figure 2-13. TDM Inputs Signals

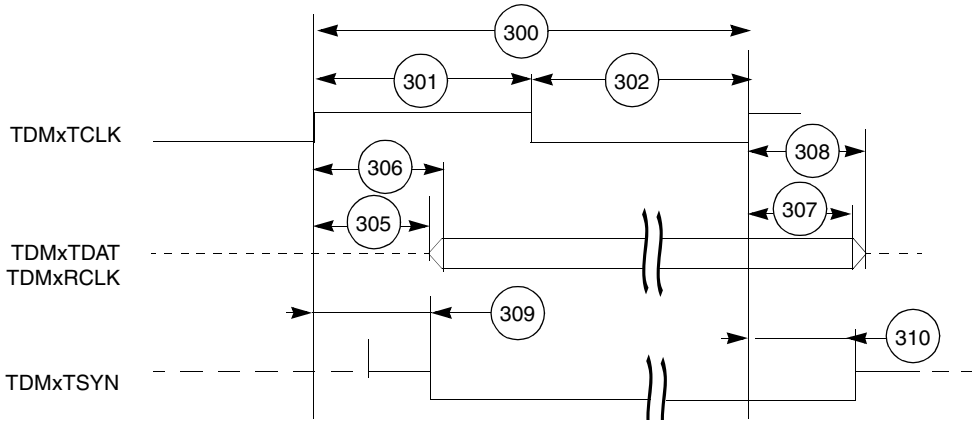


Figure 2-14. TDM Output Signals

2.5.8 UART Timing

Table 2-21. UART Timing

No.	Characteristics	Expression	Min	Max	Unit
400	URXD and UTXD inputs high/low duration	$16 \times T_{REFCLK}$	160.0	—	ns
401	URXD and UTXD inputs rise/fall time			10	ns
402	UTXD output rise/fall time			10	ns

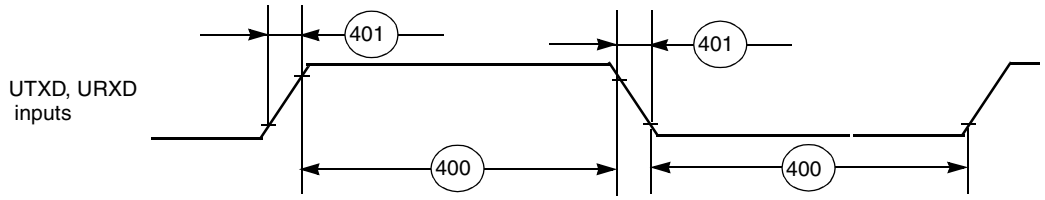


Figure 2-15. UART Input Timing

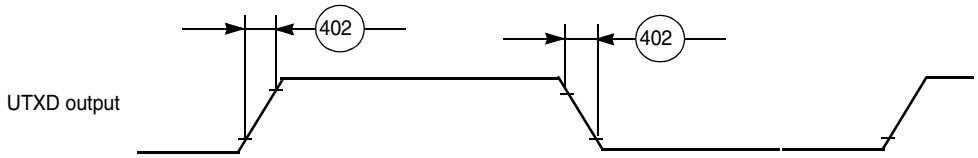


Figure 2-16. UART Output Timing

2.5.9 Timer Timing

Table 2-22. Timer Timing

No.	Characteristics	Ref = CLKIN		Unit
		Min	Max	
500	TIMERx frequency	10.0	—	ns
501	TIMERx Input high period	4.0	—	ns
502	TIMERx Output low period	4.0	—	ns
503	TIMERx Propagations delay from its clock input	2.8	8.1	ns
Note:	CLKOUT synchronization mode is not supported for cores operating at above 400 MHz.			

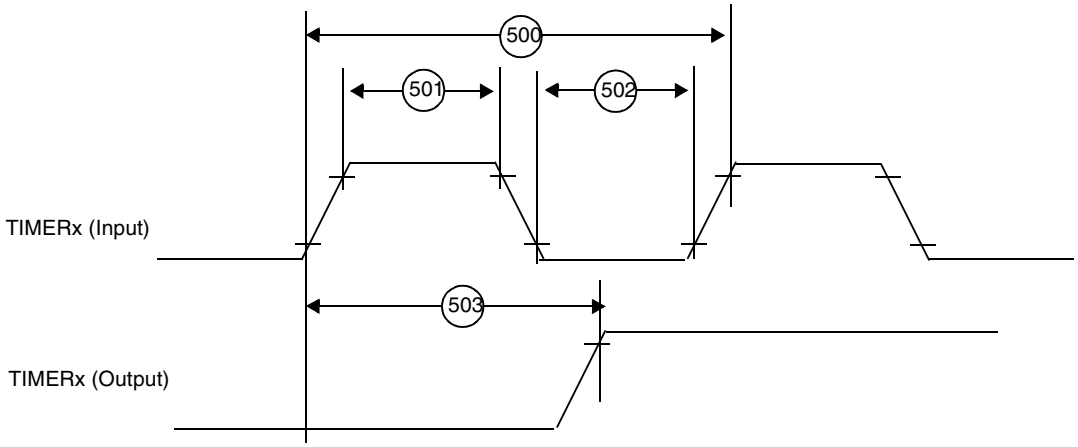


Figure 2-17. Timer Timing

2.5.10 Ethernet Timing

2.5.10.1 Management Interface Timing

Table 2-23. Ethernet Controller Management Interface Timing

No.	Characteristics	Min	Max	Unit
801	ETHMDIO to ETHMDC rising edge set-up time	10	—	ns
802	ETHMDC rising edge to ETHMDIO hold time	10	—	ns

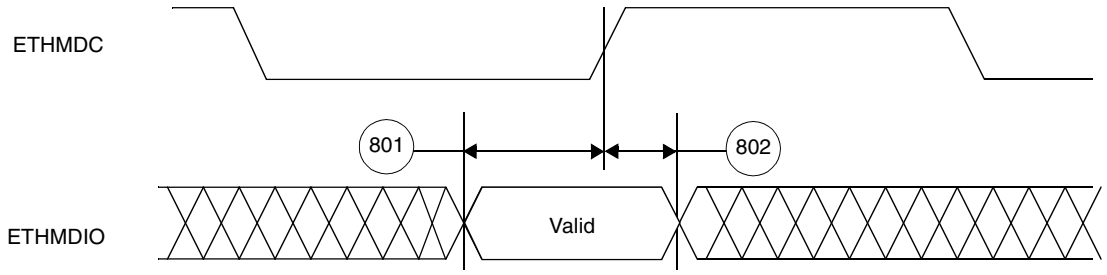


Figure 2-18. MDIO Timing Relationship to MDC

2.5.10.2 MII Mode Timing

Table 2-24. MII Mode Signal Timing

No.	Characteristics	Min	Max	Unit
803	ETHRX_DV, ETHRXD[0–3], ETHRX_ER to ETHRX_CLK rising edge set-up time	3.5	—	ns
804	ETHRX_CLK rising edge to ETHRX_DV, ETHRXD[0–3], ETHRX_ER hold time	3.5	—	ns
805	ETHTX_CLK to ETHTX_EN, ETHTXD[0–3], ETHTX_ER output delay	1	12.6	ns

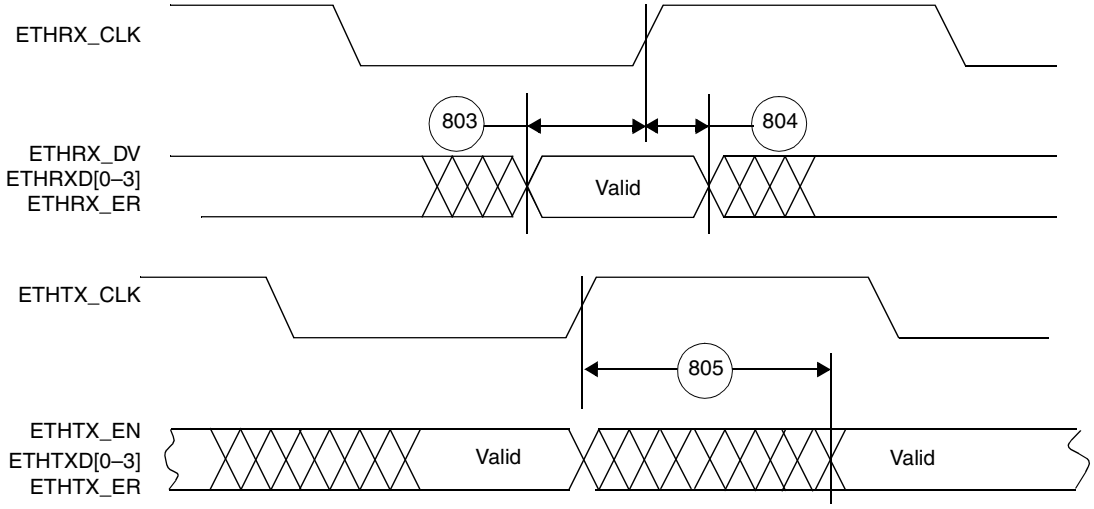


Figure 2-19. MII Mode Signal Timing

2.5.10.3 RMII Mode

Table 2-25. RMII Mode Signal Timing

No.	Characteristics	Min	Max	Unit
806	ETHTX_EN,ETHRXD[0–1], ETHCRS_DV, ETHRX_ER to ETHREF_CLK rising edge set-up time	2	—	ns
807	ETHREF_CLK rising edge to ETHRXD[0–1], ETHCRS_DV, ETHRX_ER hold time	1.6	—	ns
811	ETHREF_CLK rising edge to ETHTXD[0–1], ETHTX_EN output delay.	3	11	ns

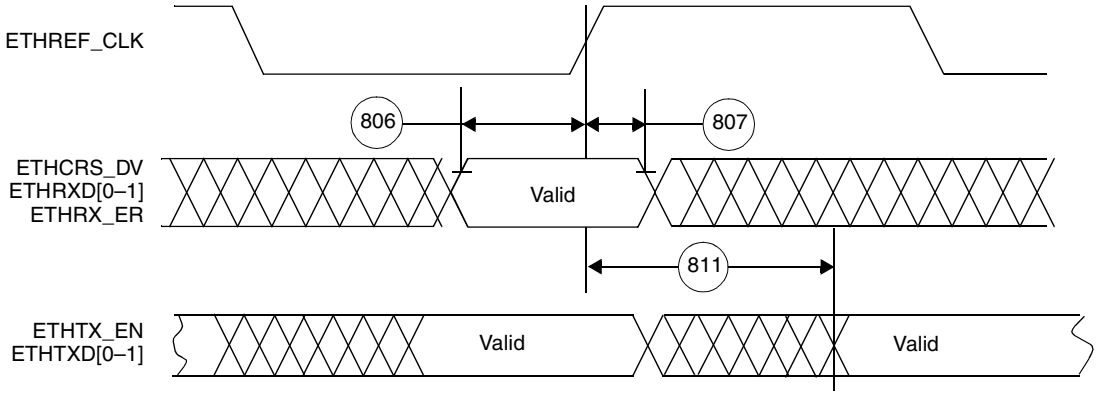


Figure 2-20. RMII Mode Signal Timing

2.5.10.4 SMII Mode

Table 2-26. SMII Mode Signal Timing

No.	Characteristics	Min	Max	Unit
808	ETHSYNC_IN, ETHRXD to ETHCLOCK rising edge set-up time	1.0	—	ns
809	ETHCLOCK rising edge to ETHSYNC_IN, ETHRXD hold time	1.0	—	ns
810	ETHCLOCK rising edge to ETHSYNC, ETHTXD output delay	1.5[1]	5.0[2]	ns

Notes: **1.** Measured using a 5 pF load.
2. Measured using a 15 pF load.

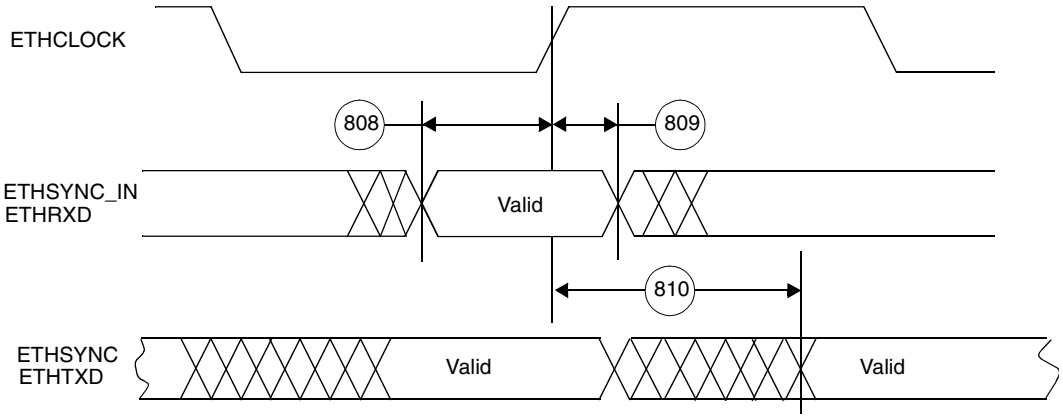


Figure 2-21. SMII Mode Signal Timing

2.5.11 GPIO Timing

Table 2-27. GPIO Timing

No.	Characteristics	Ref = CLKIN		Ref = CLKOUT		Unit
		Min	Max	Min	Max	
601	REFCLK edge to GPIO out valid (GPIO out delay time)	—	6.1	—	6.9	ns
602	REFCLK edge to GPIO out not valid (GPIO out hold time)	1.1	—	1.3	—	ns
603	REFCLK edge to high impedance on GPIO out	—	5.4	—	6.2	ns
604	GPIO in valid to REFCLK edge (GPIO in set-up time)	3.5	—	3.7	—	ns
605	REFCLK edge to GPIO in not valid (GPIO in hold time)	0.5	—	0.5	—	ns
Note:	CLKOUT synchronization mode is not supported for cores operating at above 400 MHz.					

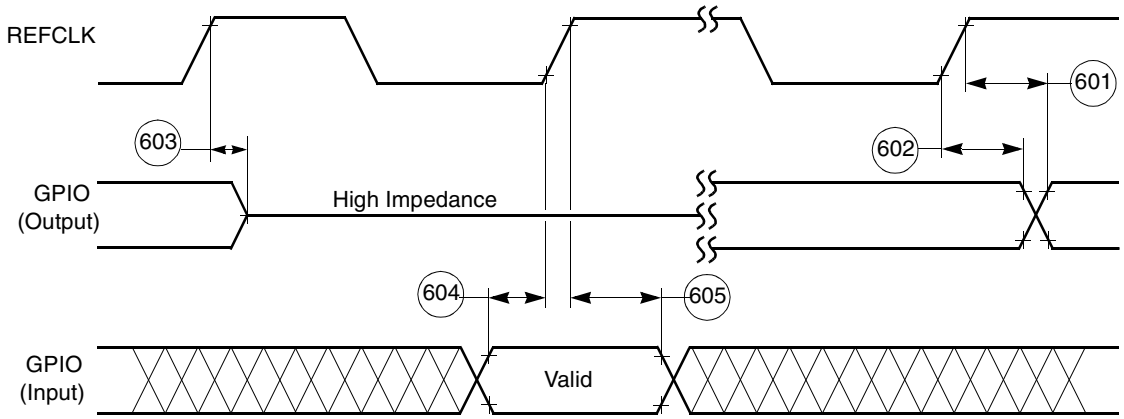


Figure 2-22. GPIO Timing

2.5.12 EE Signals

Table 2-28. EE Pin Timing

Number	Characteristics	Type	Min
65	EE0 (input)	Asynchronous	4 core clock periods
66	EE1 (output)	Synchronous to Core clock	1 core clock period

Notes: **1.** The core clock is the SC140 core clock. The ratio between the core clock and CLKOUT is configured during power-on-reset.
2. Refer to **Table 1-4** on page 1-6 for details on EE pin functionality.

Figure 2-23 shows the signal behavior of the EE pins.

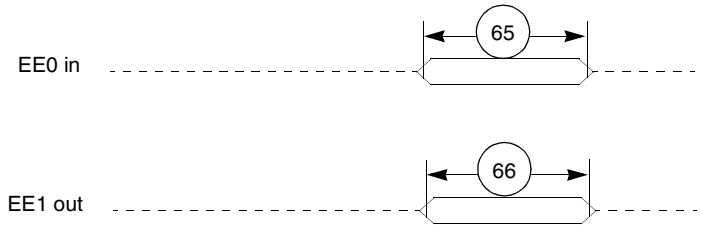


Figure 2-23. EE Pin Timing

2.5.13 JTAG Signals

Table 2-29. JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
700	TCK frequency of operation (1/(T_C × 4); maximum 25 MHz)	0.0	25	MHz
701	TCK cycle time	40.0	—	ns
702	TCK clock pulse width measured at V_M = 1.6 V • High • Low	 20.0 16.0	 — —	 ns ns
703	TCK rise and fall times	0.0	3.0	ns
704	Boundary scan input data set-up time	5.0	—	ns
705	Boundary scan input data hold time	20.0	—	ns
706	TCK low to output data valid	0.0	30.0	ns
707	TCK low to output high impedance	0.0	30.0	ns
708	TMS, TDI data set-up time	5.0	—	ns
709	TMS, TDI data hold time	20.0	—	ns
710	TCK low to TDO data valid	0.0	20.0	ns
711	TCK low to TDO high impedance	0.0	20.0	ns
712	$\overline{TRST}$ assert time	100.0	—	ns
713	$\overline{TRST}$ set-up time to TCK low	30.0	—	ns
Note:	All timings apply to OnCE module data transfers as well as any other transfers via the JTAG port.			

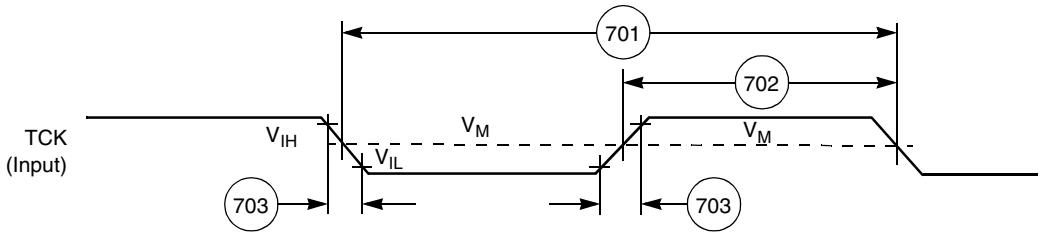


Figure 2-24. Test Clock Input Timing Diagram

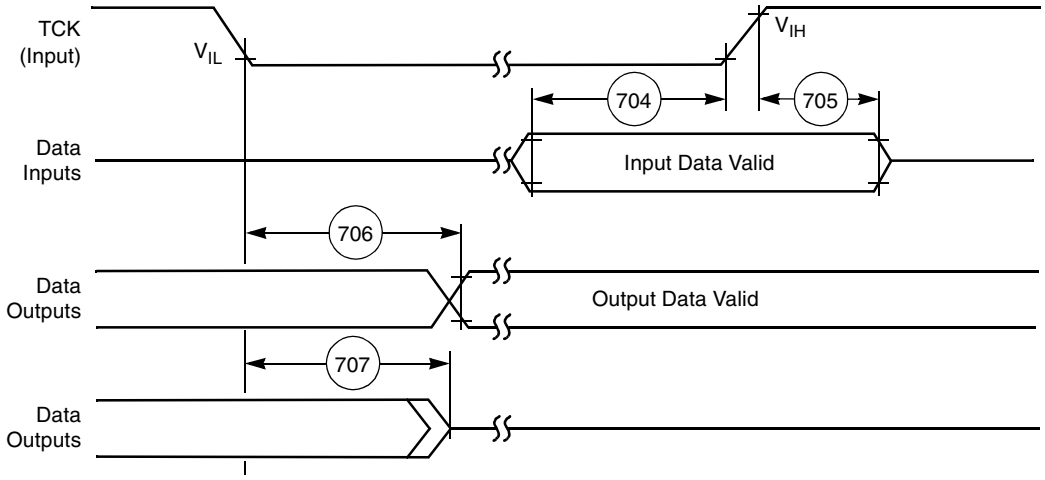


Figure 2-25. Boundary Scan (JTAG) Timing Diagram

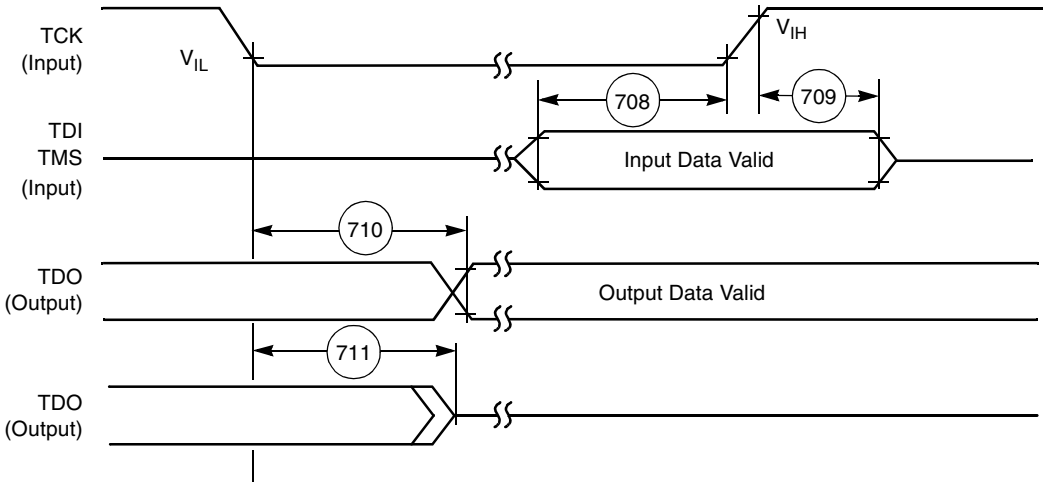


Figure 2-26. Test Access Port Timing Diagram

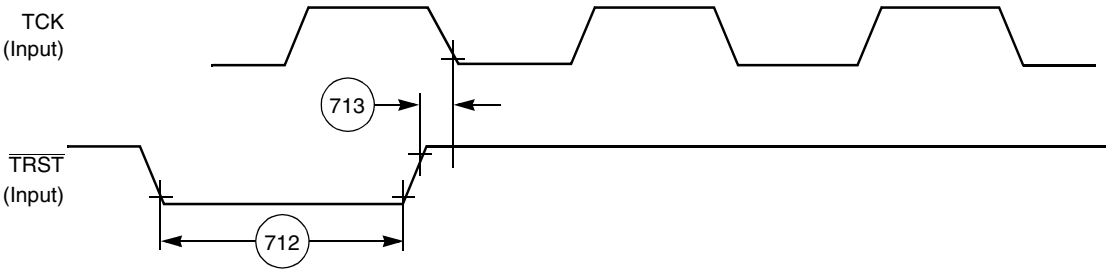


Figure 2-27. $\overline{TRST}$ Timing Diagram

Packaging 3

This section provides information on the MSC8126 package, including diagrams of the package pinouts and tables showing how the signals discussed in **Chapter 1** are allocated. The MSC8126 is available in a 431-pin flip chip-plastic ball grid array (FC-PBGA).

3.1 Package Description

Figure 3-1 and **Figure 3-2** show top and bottom views of the package, including pinouts. To conform to JEDEC requirements, the package is based on a 23 × 23 position (20 × 20 mm) layout with the outside perimeter depopulated. Therefore, ball position numbering starts with B2. Signal names shown in the figures are typically the signal assigned after reset. Signals that are only used during power-on reset (SWTE, DSISYNC, DSI64, MODCK[1–2], CNFGS, and CHIP_ID[0–3]) are not shown in these figures if there is another signal assigned to the pin after reset. Also, there are several signals that are designated as $\overline{\text{IRQ}}$ lines immediately after reset, but represent duplicate $\overline{\text{IRQ}}$ lines that should be reconfigured by the user. To represent these signals uniquely in the figures, the second functions (BADDR[29–31], DP[1–7], and $\overline{\text{INT_OUT}}$) are used.

Table 3-1 lists the MSC8126 signals alphabetically by signal name. Connections with multiple names are listed individually by each name. Signals with programmable polarity are shown both as signals which are asserted low (default) and high (that is, $\overline{\text{NAME}}$/NAME). **Table 3-2** lists the signals numerically by pin number. Each pin number is listed once with the various signals that are multiplexed to it. For simplicity, signals with programmable polarity are shown in this table only with their default name (asserted low).

Note: For Ethernet signals multiplexed with the DSI/system Bus (MII and RMII modes only), signals not used by the RMII mode are reserved when the Ethernet controller is multiplexed with the DSI/system bus and RMII mode is selected. These reserved signals can be left unconnected. These RMII reserved signals are not included in **Table 3-1**, but are indicated in **Table 3-2**.

Note: For Ethernet signals multiplexed with the GPIO/TDM signals, signals not used by the RMII or SMII mode can be assigned to their alternate GPIO or dedicated function, except for GPIO10 and GPIO14. If the Ethernet controller is enabled and multiplexed with the GPIO signals and SMII mode is selected, GPIO10 and GPIO14 (E21 and F21, respectively) must be left unconnected. These signals are designated as NC (no connect) in **Table 3-1** and **Table 3-2**.

Top View

	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
B		V_{DD}	GND	GND	NMI/OUT	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GPIO0	V_{DD}	V_{DD}	GND
C	GND	V_{DD}	TDO	S/RESET	GPIO28	HCID1	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	GND	GPIO30	GPIO2	GPIO1	GPIO7	GPIO3	GPIO5	GPIO6
D	TDI	EE0	EE1	GND	V_{DDH}	HCID2	HCID3	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	V_{DD}	GPIO31	GPIO29	V_{DDH}	GPIO4	V_{DDH}	GND	GPIO8
E	TCK	TRST	TMS	HRESET	GPIO27	HCID0	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	GND	V_{DD}	GND	GND	GPIO9	GPIO13	GPIO10	GPIO12
F	PO/RESET	RST/CONF	NMI	HA29	HA22	GND	V_{DD}	V_{DD}	V_{DD}	GND	V_{DD}	GND	V_{DD}	ETHRX_CLK	ETHTX_CLK	GPIO20	GPIO18	GPIO16	GPIO11	GPIO14	GPIO19
G	HA24	HA27	HA25	HA23	HA17	PWE0	V_{DD}	V_{DD}	BADDR31	BM0	ABB	V_{DD}	INT/OUT	ETHCRS	V_{DD}	CS1	BCTL0	GPIO15	GND	GPIO17	GPIO22
H	HA20	HA28	V_{DD}	HA19	TEST	PSD/CAS	PGTA	V_{DD}	BM1	ARTRY	AACK	DBB	HTA	V_{DD}	TT4	CS4	GPIO24	GPIO21	V_{DD}	V_{DDH}	A31
J	HA18	HA26	V_{DD}	HA13	GND	PSDA MUX	BADDR27	V_{DD}	CLKIN	BM2	DBG	V_{DD}	GND	V_{DD}	TT3	PSDA10	BCTL1	GPIO23	GND	GPIO25	A30
K	HA15	HA21	HA16	PWE3	PWE1	POE	BADDR30	Res.	GND	GND	GND	GND	CLKOUT	V_{DD}	TT2	ALE	CS2	GND	A26	A29	A28
L	HA12	HA14	HA11	V_{DDH}	V_{DDH}	BADDR28	BADDR29	GND	GND	MSC8126			GND	V_{DDH}	GND	GND	CS3	V_{DDH}	A27	A25	A22
M	HD28	HD31	V_{DDH}	GND	GND	V_{DDH}	V_{DD}	V_{DDH}	GND				GND	V_{DDH}	HB/RST	V_{DDH}	V_{DDH}	GND	V_{DDH}	A24	A21
N	HD26	HD30	HD29	HD24	PWE2	V_{DDH}	HWBS0	HBCS	GND				GND	HRDS	BG	HCS	CS0	PSDWE	GPIO26	A23	A20
P	HD20	HD27	HD25	HD23	HWBS3	HWBS2	HWBS1	HCLKIN	GND	GND_{SYN}	V_{CCSYN}	GND	GND	TA	BR	TEA	PSD/VAL	DP0	V_{DDH}	GND	A19
R	HD18	V_{DDH}	GND	HD22	HWBS6	HWBS4	TSZ1	TSZ3	GBL	V_{DD}	V_{DD}	V_{DD}	TT0	DP7	DP6	DP3	TS	DP2	A17	A18	A16
T	HD17	HD21	HD1	HD0	HWBS7	HWBS5	TSZ0	TSZ2	TBST	V_{DD}	D16	TT1	D21	D23	DP5	DP4	DP1	D30	GND	A15	A14
U	HD16	HD19	HD2	D2	D3	D6	D8	D9	D11	D14	D15	D17	D19	D22	D25	D26	D28	D31	V_{DDH}	A12	A13
V	HD3	V_{DDH}	GND	D0	D1	D4	D5	D7	D10	D12	D13	D18	D20	GND	D24	D27	D29	A8	A9	A10	A11
W	HD6	HD5	HD4	GND	GND	V_{DDH}	V_{DDH}	GND	HDST1	HDST0	V_{DDH}	GND	HD40	V_{DDH}	HD33	V_{DDH}	HD32	GND	GND	A7	A6
Y	HD7	HD15	V_{DDH}	HD9	V_{DD}	HD60	HD58	GND	V_{DDH}	HD51	GND	V_{DDH}	HD43	GND	V_{DDH}	GND	HD37	HD34	V_{DDH}	A4	A5
AA	V_{DD}	HD14	HD12	HD10	HD63	HD59	GND	V_{DDH}	HD54	HD52	V_{DDH}	GND	V_{DDH}	HD46	GND	HD42	HD38	HD35	A0	A2	A3
AB	GND	HD13	HD11	HD8	HD62	HD61	HD57	HD56	HD55	HD53	HD50	HD49	HD48	HD47	HD45	HD44	HD41	HD39	HD36	A1	V_{DD}

Figure 3-1. MSC8126 Package, Top View

Bottom View

	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2
B	GND	V_{DD}	V_{DD}	GPIO0	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	$\overline{NMI_OUT}$	GND	GND	V_{DD}	
C	GPIO6	GPIO5	GPIO3	GPIO7	GPIO1	GPIO2	GPIO30	GND	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	HCID1	GPIO28	$\overline{S}$ $\overline{RESET}$	TDO	V_{DD}	GND
D	GPIO8	GND	V_{DDH}	GPIO4	V_{DDH}	GPIO29	GPIO31	V_{DD}	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	HCID3	HCID2	V_{DDH}	GND	EE1	EE0	TDI
E	GPIO12	GPIO10	GPIO13	GPIO9	GND	GND	V_{DD}	GND	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	HCID0	GPIO27	$\overline{HRESET}$	TMS	$\overline{TRST}$	TCK
F	GPIO19	GPIO14	GPIO11	GPIO16	GPIO18	GPIO20	ETHTX_CLK	ETHRX_CLK	V_{DD}	GND	V_{DD}	GND	V_{DD}	V_{DD}	V_{DD}	GND	HA22	HA29	$\overline{NMI}$	$\overline{RST}$ $\overline{CONF}$	$\overline{PO}$ $\overline{RESET}$
G	GPIO22	GPIO17	GND	GPIO15	$\overline{BCTL0}$	$\overline{CS1}$	V_{DD}	ETHCRS	$\overline{INT}$ $\overline{OUT}$	V_{DD}	$\overline{ABB}$	BM0	BADDR31	V_{DD}	V_{DD}	$\overline{PWE0}$	HA17	HA23	HA25	HA27	HA24
H	A31	V_{DDH}	V_{DD}	GPIO21	GPIO24	$\overline{CS4}$	TT4	V_{DD}	$\overline{HTA}$	$\overline{DBB}$	$\overline{AACK}$	$\overline{ARTRY}$	BM1	V_{DD}	$\overline{PGTA}$	$\overline{PSD}$ $\overline{CAS}$	TEST	HA19	V_{DD}	HA28	HA20
J	A30	GPIO25	GND	GPIO23	BCTL1	PSDA10	TT3	V_{DD}	GND	V_{DD}	$\overline{DBG}$	BM2	CLKIN	V_{DD}	BADDR27	PSDA MUX	GND	HA13	V_{DD}	HA26	HA18
K	A28	A29	A26	GND	$\overline{CS2}$	ALE	TT2	V_{DD}	CLKOUT	GND	GND	GND	GND	Res.	BADDR30	$\overline{POE}$	$\overline{PWE1}$	$\overline{PWE3}$	HA16	HA21	HA15
L	A22	A25	A27	V_{DDH}	$\overline{CS3}$	GND	GND	V_{DDH}	GND	MSC8126			GND	GND	BADDR29	BADDR28	V_{DDH}	V_{DDH}	HA11	HA14	HA12
M	A21	A24	V_{DDH}	GND	V_{DDH}	V_{DDH}	$\overline{HB}$ $\overline{RST}$	V_{DDH}	GND				GND	V_{DDH}	V_{DD}	V_{DDH}	GND	GND	V_{DDH}	HD31	HD28
N	A20	A23	GPIO26	PSDWE	$\overline{CS0}$	$\overline{HCS}$	$\overline{BG}$	$\overline{HRDS}$	GND				GND	$\overline{HBCS}$	$\overline{HWBS}$ $\overline{0}$	V_{DDH}	$\overline{PWE2}$	HD24	HD29	HD30	HD26
P	A19	GND	V_{DDH}	DP0	$\overline{PSD}$ $\overline{VAL}$	$\overline{TEA}$	$\overline{BR}$	$\overline{TA}$	GND	GND	V_{CCSYN}	GND_{SYN}	GND	HCLKIN	$\overline{HWBS}$ $\overline{1}$	$\overline{HWBS}$ $\overline{2}$	$\overline{HWBS}$ $\overline{3}$	HD23	HD25	HD27	HD20
R	A16	A18	A17	DP2	$\overline{TS}$	DP3	DP6	DP7	TT0	V_{DD}	V_{DD}	V_{DD}	$\overline{GBL}$	TSZ3	TSZ1	$\overline{HWBS}$ $\overline{4}$	$\overline{HWBS}$ $\overline{6}$	HD22	GND	V_{DDH}	HD18
T	A14	A15	GND	D30	DP1	DP4	DP5	D23	D21	TT1	D16	V_{DD}	$\overline{TBST}$	TSZ2	TSZ0	$\overline{HWBS}$ $\overline{5}$	$\overline{HWBS}$ $\overline{7}$	HD0	HD1	HD21	HD17
U	A13	A12	V_{DDH}	D31	D28	D26	D25	D22	D19	D17	D15	D14	D11	D9	D8	D6	D3	D2	HD2	HD19	HD16
V	A11	A10	A9	A8	D29	D27	D24	GND	D20	D18	D13	D12	D10	D7	D5	D4	D1	D0	GND	V_{DDH}	HD3
W	A6	A7	GND	GND	HD32	V_{DDH}	HD33	V_{DDH}	HD40	GND	V_{DDH}	HDST0	HDST1	GND	V_{DDH}	V_{DDH}	GND	GND	HD4	HD5	HD6
Y	A5	A4	V_{DDH}	HD34	HD37	GND	V_{DDH}	GND	HD43	V_{DDH}	GND	HD51	V_{DDH}	GND	HD58	HD60	V_{DD}	HD9	V_{DDH}	HD15	HD7
AA	A3	A2	A0	HD35	HD38	HD42	GND	HD46	V_{DDH}	GND	V_{DDH}	HD52	HD54	V_{DDH}	GND	HD59	HD63	HD10	HD12	HD14	V_{DD}
AB	V_{DD}	A1	HD36	HD39	HD41	HD44	HD45	HD47	HD48	HD49	HD50	HD53	HD55	HD56	HD57	HD61	HD62	HD8	HD11	HD13	GND

Figure 3-2. MSC8126 Package, Bottom View

Table 3-1. MSC8126 Signal Listing By Name

Signal Name	Location Designator	Signal Name	Location Designator
A0	AA20	BADDR27	J8
A1	AB21	BADDR28	L7
A2	AA21	BADDR29	L8
A3	AA22	BADDR30	K8
A4	Y21	BADDR31	G10
A5	Y22	$\overline{\text{BCTL0}}$	G18
A6	W22	$\overline{\text{BCTL1}}$	J18
A7	W21	$\overline{\text{BG}}$	N16
A8	V19	BNKSEL0	G11
A9	V20	BNKSEL1	H10
A10	V21	BNKSEL2	J11
A11	V22	BM0	G11
A12	U21	BM1	H10
A13	U22	BM2	J11
A14	T22	$\overline{\text{BR}}$	P16
A15	T21	CHIP_ID0	B19
A16	R22	CHIP_ID1	C18
A17	R20	CHIP_ID2	C17
A18	R21	CHIP_ID3	D17
A19	P22	CLKIN	J10
A20	N22	CLKOUT	K14
A21	M22	CNFGS	W3
A22	L22	$\overline{\text{CS0}}$	N18
A23	N21	$\overline{\text{CS1}}$	G17
A24	M21	$\overline{\text{CS2}}$	K18
A25	L21	$\overline{\text{CS3}}$	L18
A26	K20	$\overline{\text{CS4}}$	H17
A27	L20	$\overline{\text{CS5}}$	K16
A28	K22	$\overline{\text{CS5}}$	J18
A29	K21	$\overline{\text{CS6}}$	J16
A30	J22	$\overline{\text{CS7}}$	H16
A31	H22	D0	V5
$\overline{\text{AACK}}$	H12	D1	V6
$\overline{\text{ABB}}$	G12	D2	U5
ALE	K17	D3	U6
$\overline{\text{ARTRY}}$	H11	D4	V7

Table 3-1. MSC8126 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
D5	V8	D41	AB18
D6	U7	D42	AA17
D7	V9	D43	Y14
D8	U8	D44	AB17
D9	U9	D45	AB16
D10	V10	D46	AA15
D11	U10	D47	AB15
D12	V11	D48	AB14
D13	V12	D49	AB13
D14	U11	D50	AB12
D15	U12	D51	Y11
D16	T12	D52	AA11
D17	U13	D53	AB11
D18	V13	D54	AA10
D19	U14	D55	AB10
D20	V14	D56	AB9
D21	T14	D57	AB8
D22	U15	D58	Y8
D23	T15	D59	AA7
D24	V16	D60	Y7
D25	U16	D61	AB7
D26	U17	D62	AB6
D27	V17	D63	AA6
D28	U18	$\overline{\text{DACK1}}$	G21
D29	V18	$\overline{\text{DACK1}}$	T18
D30	T19	$\overline{\text{DACK2}}$	F22
D31	U19	$\overline{\text{DACK2}}$	R19
D32	W18	$\overline{\text{DACK3}}$	T17
D33	W16	$\overline{\text{DACK4}}$	T16
D34	Y19	$\overline{\text{DBB}}$	H13
D35	AA19	$\overline{\text{DBG}}$	J12
D36	AB20	$\overline{\text{DONE1}}$	F19
D37	Y18	$\overline{\text{DONE2}}$	G22
D38	AA18	DP0	P19
D39	AB19	DP1	T18
D40	W14	DP2	R19

Table 3-1. MSC8126 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
DP3	R17	ETHRXD0	F21
DP4	T17	ETHRXD0	W14
DP5	T16	ETHRXD1	E22
DP6	R16	ETHRXD1	AB18
DP7	R15	ETHRXD2	C22
$\overline{\text{DRACK1}}$	F19	ETHRXD2	AA17
$\overline{\text{DRACK2}}$	G22	ETHRXD3	C21
DREQ1	E6	ETHRXD3	Y14
DREQ1	G19	ETHSYNC	E22
DREQ1	P19	ETHSYNC_IN	F15
DREQ2	C6	ETHTX_CLK	F16
DREQ2	F18	ETHTX_EN	D17
DREQ2	R17	ETHTX_EN	AA10
DREQ3	R16	ETHTX_ER	D19
DREQ4	R15	ETHTX_ER	AB10
DSI64	U4	ETHTXD	F20
DSISYNC	T4	ETHTXD0	B19
EE0	D3	ETHTXD0	AA15
EE1	D4	ETHTXD1	C18
ETHCLOCK	F16	ETHTXD1	AB15
ETHCOL	D22	ETHTXD2	C20
ETHCOL	Y7	ETHTXD2	AB14
ETHCRS	G15	ETHTXD3	C19
ETHCRS_DV	E21	ETHTXD3	AB13
ETHCRS_DV	AB9	$\overline{\text{EXT_BG2}}$	T18
ETHMDC	E20	$\overline{\text{EXT_BG3}}$	T16
ETHMDC	Y8	$\overline{\text{EXT_BR2}}$	P19
ETHMDIO	E19	$\overline{\text{EXT_BR3}}$	R17
ETHMDIO	AA7	$\overline{\text{EXT_DBG2}}$	R19
ETHREF_CLK	F16	$\overline{\text{EXT_DBG3}}$	T17
ETHRX_CLK	F15	$\overline{\text{GBL}}$	R10
ETHRX_DV	E21	GND	B4
ETHRX_DV	AB9	GND	B5
ETHRX_ER	F20	GND	B7
ETHRX_ER	AB8	GND	B9
ETHRXD	G15	GND	B11

Table 3-1. MSC8126 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
GND	B13	GND	L14
GND	B15	GND	L16
GND	B17	GND	L17
GND	B22	GND	M5
GND	C2	GND	M6
GND	C8	GND	M10
GND	C10	GND	M14
GND	C12	GND	M19
GND	C14	GND	N10
GND	C15	GND	N14
GND	D5	GND	P10
GND	D9	GND	P13
GND	D11	GND	P14
GND	D13	GND	P21
GND	D21	GND	R4
GND	E8	GND	T20
GND	E10	GND	V4
GND	E12	GND	V15
GND	E14	GND	W5
GND	E15	GND	W6
GND	E17	GND	W9
GND	E18	GND	W13
GND	F7	GND	W19
GND	F11	GND	W20
GND	F13	GND	Y9
GND	G20	GND	Y12
GND	J6	GND	Y15
GND	J14	GND	Y17
GND	J20	GND	AA8
GND	K10	GND	AA13
GND	K11	GND	AA16
GND	K12	GND	AB2
GND	K13	GND_{SYN}	P11
GND	K19	GPIO0	B19
GND	L9	GPIO1	C18
GND	L10	GPIO2	C17

Table 3-1. MSC8126 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
GPIO3	C20	HA14	L3
GPIO4	D19	HA15	K2
GPIO5	C21	HA16	K4
GPIO6	C22	HA17	G6
GPIO7	C19	HA18	J2
GPIO8	D22	HA19	H5
GPIO9	E19	HA20	H2
GPIO10	E21	HA21	K3
GPIO11	F20	HA22	F6
GPIO12	E22	HA23	G5
GPIO13	E20	HA24	G2
GPIO14	F21	HA25	G4
GPIO15	G19	HA26	J3
GPIO16	F19	HA27	G3
GPIO17	G21	HA28	H3
GPIO18	F18	HA29	F5
GPIO19	F22	$\overline{\text{HBCS}}$	N9
GPIO20	F17	$\overline{\text{HBRST}}$	M16
GPIO21	H19	HCID0	E7
GPIO22	G22	HCID1	C7
GPIO23	J19	HCID2	D7
GPIO24	H18	HCID3	D8
GPIO25	J21	HCLKIN	P9
GPIO26	N20	$\overline{\text{HCS}}$	N17
GPIO27	E6	HD0	T5
GPIO28	C6	HD1	T4
GPIO29	D17	HD2	U4
GPIO30	C16	HD3	V2
GPIO31	D16	HD4	W4
HA7	R14	HD5	W3
HA8	D8	HD6	W2
HA9	W11	HD7	Y2
HA10	W10	HD8	AB5
HA11	L4	HD9	Y5
HA12	L2	HD10	AA5
HA13	J5	HD11	AB4

Table 3-1. MSC8126 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
HD12	AA4	HD48	AB14
HD13	AB3	HD49	AB13
HD14	AA3	HD50	AB12
HD15	Y3	HD51	Y11
HD16	U2	HD52	AA11
HD17	T2	HD53	AB11
HD18	R2	HD54	AA10
HD19	U3	HD55	AB10
HD20	P2	HD56	AB9
HD21	T3	HD57	AB8
HD22	R5	HD58	Y8
HD23	P5	HD59	AA7
HD24	N5	HD60	Y7
HD25	P4	HD61	AB7
HD26	N2	HD62	AB6
HD27	P3	HD63	AA6
HD28	M2	$\overline{\text{HDBE0}}$	N8
HD29	N4	$\overline{\text{HDBE1}}$	P8
HD30	N3	$\overline{\text{HDBE2}}$	P7
HD31	M3	$\overline{\text{HDBE3}}$	P6
HD32	W18	$\overline{\text{HDBE4}}$	R7
HD33	W16	$\overline{\text{HDBE5}}$	T7
HD34	Y19	$\overline{\text{HDBE6}}$	R6
HD35	AA19	$\overline{\text{HDBE7}}$	T6
HD36	AB20	$\overline{\text{HDBS0}}$	N8
HD37	Y18	$\overline{\text{HDBS1}}$	P8
HD38	AA18	$\overline{\text{HDBS2}}$	P7
HD39	AB19	$\overline{\text{HDBS3}}$	P6
HD40	W14	$\overline{\text{HDBS4}}$	R7
HD41	AB18	$\overline{\text{HDBS5}}$	T7
HD42	AA17	$\overline{\text{HDBS6}}$	R6
HD43	Y14	$\overline{\text{HDBS7}}$	T6
HD44	AB17	HDST0	W11
HD45	AB16	HDST1	W10
HD46	AA15	$\overline{\text{HRDE}}$	N15
HD47	AB15	$\overline{\text{HRDS}}$	N15

Table 3-1. MSC8126 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
HRESET	E5	IRQ5	L8
HRW	N15	IRQ5	T16
HTA	H14	IRQ6	C17
HWBE0	N8	IRQ6	D22
HWBE1	P8	IRQ6	R16
HWBE2	P7	IRQ7	E19
HWBE3	P6	IRQ7	G14
HWBE4	R7	IRQ7	R15
HWBE5	T7	IRQ8	E21
HWBE6	R6	IRQ9	F20
HWBE7	T6	IRQ10	E22
HWBS0	N8	IRQ11	E20
HWBS1	P8	IRQ12	F21
HWBS2	P7	IRQ13	J19
HWBS3	P6	IRQ14	H18
HWBS4	R7	IRQ15	J21
HWBS5	T7	MODCK1	V2
HWBS6	R6	MODCK2	W4
HWBS7	T6	HWBE4	R7
INT_OUT	G14	HWBE5	T7
IRQ1	C20	HWBE6	R6
IRQ1	R10	HWBE7	T6
IRQ1	T18	NC	E21
IRQ2	D19	NC	F21
IRQ2	K8	NMI	F4
IRQ2	R19	NMI_OUT	B6
IRQ3	C21	PBS0	G7
IRQ3	G10	PBS1	K6
IRQ3	R17	PBS2	N6
IRQ4	B19	PBS3	K5
IRQ4	C22	PBS4	R7
IRQ4	G12	PBS5	T7
IRQ4	T17	PBS6	R6
IRQ5	C18	PBS7	T6
IRQ5	C19	PGPL0	J17
IRQ5	H13	PGPL1	N19

Table 3-1. MSC8126 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
PGPL2	K7	SWTE	T5
PGPL3	H7	$\overline{\text{TA}}$	P15
PGPL4	H8	$\overline{\text{TBST}}$	T10
PGPL5	J7	TC0	G11
$\overline{\text{PGTA}}$	H8	TC1	H10
$\overline{\text{POE}}$	K7	TC2	J11
$\overline{\text{PORESET}}$	F2	TCK	E2
$\overline{\text{PPBS}}$	H8	TDI	D2
PSDA10	J17	TDM0RCLK	J21
PSDAMUX	J7	TDM0RDAT	N20
$\overline{\text{PSDCAS}}$	H7	TDM0RSYN	H18
$\overline{\text{PSDDQM0}}$	G7	TDM0TCLK	G22
$\overline{\text{PSDDQM1}}$	K6	TDM0TDAT	J19
$\overline{\text{PSDDQM2}}$	N6	TDM0TSYN	H19
$\overline{\text{PSDDQM3}}$	K5	TDM1RCLK	F22
$\overline{\text{PSDDQM4}}$	R7	TDM1RDAT	F17
$\overline{\text{PSDDQM5}}$	T7	TDM1RSYN	F18
$\overline{\text{PSDDQM6}}$	R6	TDM1TCLK	F19
$\overline{\text{PSDDQM7}}$	T6	TDM1TDAT	G21
$\overline{\text{PSDRAS}}$	K7	TDM1TSYN	G19
$\overline{\text{PSDVAL}}$	P18	TDM2RCLK	E20
$\overline{\text{PSDWE}}$	N19	TDM2RDAT	F21
$\overline{\text{PWE0}}$	G7	TDM2RSYN	E22
$\overline{\text{PWE1}}$	K6	TDM2TCLK	E21
$\overline{\text{PWE2}}$	N6	TDM2TDAT	F20
$\overline{\text{PWE3}}$	K5	TDM2TSYN	E19
$\overline{\text{PWE4}}$	R7	TDM3RCLK	C19
$\overline{\text{PWE5}}$	T7	TDM3RDAT	D22
$\overline{\text{PWE6}}$	R6	TDM3RSYN	C22
$\overline{\text{PWE7}}$	T6	TDM3TCLK	D19
PUPMWAIT	H8	TDM3TDAT	C21
Reserved	K9	TDM3TSYN	C20
$\overline{\text{RSTCONF}}$	F3	TDO	C4
SCL	D16	$\overline{\text{TEA}}$	P17
SDA	C16	TEST	H6
$\overline{\text{SRESET}}$	C5	TIMER0	C18

Table 3-1. MSC8126 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
TIMER1	C17	V_{DD}	E11
TIMER2	C16	V_{DD}	E13
TIMER3	D16	V_{DD}	E16
TMCLK	C16	V_{DD}	F8
TMS	E4	V_{DD}	F9
$\overline{TRST}$	E3	V_{DD}	F10
$\overline{TS}$	R18	V_{DD}	F12
TSZ0	T8	V_{DD}	F14
TSZ1	R8	V_{DD}	G8
TSZ2	T9	V_{DD}	G9
TSZ3	R9	V_{DD}	G13
TT0	R14	V_{DD}	G16
TT1	T13	V_{DD}	H4
TT2	K16	V_{DD}	H9
TT3	J16	V_{DD}	H15
TT4	H16	V_{DD}	H20
URXD	E6	V_{DD}	J4
UTXD	C6	V_{DD}	J9
V_{CCSYN}	P12	V_{DD}	J13
V_{DD}	B8	V_{DD}	J15
V_{DD}	B10	V_{DD}	K15
V_{DD}	B12	V_{DD}	M8
V_{DD}	B14	V_{DD}	R11
V_{DD}	B16	V_{DD}	R12
V_{DD}	B18	V_{DD}	R13
V_{DD}	B20	V_{DD}	T11
V_{DD}	B21	V_{DD}	Y6
V_{DD}	C3	V_{DD}	AA2
V_{DD}	C9	V_{DD}	B3
V_{DD}	C11	V_{DD}	AB22
V_{DD}	C13	V_{DDH}	D6
V_{DD}	D10	V_{DDH}	D18
V_{DD}	D12	V_{DDH}	D20
V_{DD}	D14	V_{DDH}	H21
V_{DD}	D15	V_{DDH}	L5
V_{DD}	E9	V_{DDH}	L6

Table 3-1. MSC8126 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
V_{DDH}	L15	V_{DDH}	W7
V_{DDH}	L19	V_{DDH}	W8
V_{DDH}	M4	V_{DDH}	W12
V_{DDH}	M7	V_{DDH}	W15
V_{DDH}	M9	V_{DDH}	W17
V_{DDH}	M15	V_{DDH}	Y4
V_{DDH}	M17	V_{DDH}	Y10
V_{DDH}	M18	V_{DDH}	Y13
V_{DDH}	M20	V_{DDH}	Y16
V_{DDH}	N7	V_{DDH}	Y20
V_{DDH}	P20	V_{DDH}	AA9
V_{DDH}	R3	V_{DDH}	AA12
V_{DDH}	U20	V_{DDH}	AA14
V_{DDH}	V3		

Note: This table lists every signal name. Because many signals are multiplexed, an individual ball designator number may be listed several times.

Table 3-2. MSC8126 Signal Listing by Ball Designator

Des.	Signal Name	Des.	Signal Name
B3	V_{DD}	C18	GPIO1/TIMER0/CHIP_ID1/$\overline{IRQ5}$/ETHTXD1
B4	GND	C19	GPIO7/TDM3RCLK/$\overline{IRQ5}$/ETHTXD3
B5	GND	C20	GPIO3/TDM3TSYN/$\overline{IRQ1}$/ETHTXD2
B6	$\overline{NMI_OUT}$	C21	GPIO5/TDM3TDAT/$\overline{IRQ3}$/ETHRXD3
B7	GND	C22	GPIO6/TDM3RSYN/$\overline{IRQ4}$/ETHRXD2
B8	V_{DD}	D2	TDI
B9	GND	D3	EE0
B10	V_{DD}	D4	EE1
B11	GND	D5	GND
B12	V_{DD}	D6	V_{DDH}
B13	GND	D7	HCID2
B14	V_{DD}	D8	HCID3/HA8
B15	GND	D9	GND
B16	V_{DD}	D10	V_{DD}
B17	GND	D11	GND
B18	V_{DD}	D12	V_{DD}
B19	GPIO0/CHIP_ID0/$\overline{IRQ4}$/ETHTXD0	D13	GND
B20	V_{DD}	D14	V_{DD}
B21	V_{DD}	D15	V_{DD}
B22	GND	D16	GPIO31/TIMER3/SCL
C2	GND	D17	GPIO29/CHIP_ID3/ETHTX_EN
C3	V_{DD}	D18	V_{DDH}
C4	TDO	D19	GPIO4/TDM3TCLK/$\overline{IRQ2}$/ETHTX_ER
C5	$\overline{SRESET}$	D20	V_{DDH}
C6	GPIO28/DREQ2/UTXD	D21	GND
C7	HCID1	D22	GPIO8/TDM3RDAT/$\overline{IRQ6}$/ETHCOL
C8	GND	E2	TCK
C9	V_{DD}	E3	$\overline{TRST}$
C10	GND	E4	TMS
C11	V_{DD}	E5	$\overline{HRESET}$
C12	GND	E6	GPIO27/DREQ1/URXD
C13	V_{DD}	E7	HCID0
C14	GND	E8	GND
C15	GND	E9	V_{DD}
C16	GPIO30/TIMER2/TMCLK/SDA	E10	GND
C17	GPIO2/TIMER1/CHIP_ID2/$\overline{IRQ6}$	E11	V_{DD}

Table 3-2. MSC8126 Signal Listing by Ball Designator (Continued)

Des.	Signal Name	Des.	Signal Name
E12	GND	G6	HA17
E13	V_{DD}	G7	$\overline{PWE0}/\overline{PSDDQM0}/\overline{PBS0}$
E14	GND	G8	V_{DD}
E15	GND	G9	V_{DD}
E16	V_{DD}	G10	$\overline{IRQ3}$/BADDR31
E17	GND	G11	BM0/TC0/BNKSEL0
E18	GND	G12	$\overline{ABB}/\overline{IRQ4}$
E19	GPIO9/TDM2TSYN/$\overline{IRQ7}$/ETHMDIO	G13	V_{DD}
E20	GPIO13/TDM2RCLK/$\overline{IRQ11}$/ETHMDC	G14	$\overline{IRQ7}/\overline{INT_OUT}$
E21	GPIO10/TDM2TCLK/$\overline{IRQ8}$/ETHRX_DV/ETHCRS_DV/NC	G15	ETHCRS/ETHRXD
E22	GPIO12/TDM2RSYN/$\overline{IRQ10}$/ETHRXD1/ETHSYNC	G16	V_{DD}
F2	$\overline{PORESET}$	G17	$\overline{CS1}$
F3	$\overline{RSTCONF}$	G18	$\overline{BCTL0}$
F4	$\overline{NMI}$	G19	GPIO15/TDM1TSYN/DREQ1
F5	HA29	G20	GND
F6	HA22	G21	GPIO17/TDM1TDAT/$\overline{DACK1}$
F7	GND	G22	GPIO22/TDM0TCLK/$\overline{DONE2}/\overline{DRACK2}$
F8	V_{DD}	H2	HA20
F9	V_{DD}	H3	HA28
F10	V_{DD}	H4	V_{DD}
F11	GND	H5	HA19
F12	V_{DD}	H6	TEST
F13	GND	H7	$\overline{PSDCAS}$/PGPL3
F14	V_{DD}	H8	$\overline{PGTA}$/PUPMWAIT/PGPL4/$\overline{PPBS}$
F15	ETHRX_CLK/ETHSYNC_IN	H9	V_{DD}
F16	ETHTX_CLK/ETHREF_CLK/ETHCLOCK	H10	BM1/TC1/BNKSEL1
F17	GPIO20/TDM1RDAT	H11	$\overline{ARTRY}$
F18	GPIO18/TDM1RSYN/DREQ2	H12	$\overline{AACK}$
F19	GPIO16/TDM1TCLK/$\overline{DONE1}/\overline{DRACK1}$	H13	$\overline{DBB}/\overline{IRQ5}$
F20	GPIO11/TDM2TDAT/$\overline{IRQ9}$/ETHRX_ER/ETHTXD	H14	$\overline{HTA}$
F21	GPIO14/TDM2RDAT/$\overline{IRQ12}$/ETHRXD0/NC	H15	V_{DD}
F22	GPIO19/TDM1RCLK/$\overline{DACK2}$	H16	TT4/$\overline{CS7}$
G2	HA24	H17	$\overline{CS4}$
G3	HA27	H18	GPIO24/TDM0RSYN/$\overline{IRQ14}$
G4	HA25	H19	GPIO21/TDM0TSYN
G5	HA23	H20	V_{DD}

Table 3-2. MSC8126 Signal Listing by Ball Designator (Continued)

Des.	Signal Name	Des.	Signal Name
H21	V_{DDH}	K15	V_{DD}
H22	A31	K16	TT2/$\overline{CS5}$
J2	HA18	K17	ALE
J3	HA26	K18	$\overline{CS2}$
J4	V_{DD}	K19	GND
J5	HA13	K20	A26
J6	GND	K21	A29
J7	PSDAMUX/PGPL5	K22	A28
J8	BADDR27	L2	HA12
J9	V_{DD}	L3	HA14
J10	CLKIN	L4	HA11
J11	BM2/TC2/BNKSEL2	L5	V_{DDH}
J12	$\overline{DBG}$	L6	V_{DDH}
J13	V_{DD}	L7	BADDR28
J14	GND	L8	$\overline{IRQ5}$/BADDR29
J15	V_{DD}	L9	GND
J16	TT3/$\overline{CS6}$	L10	GND
J17	PSDA10/PGPL0	L14	GND
J18	$\overline{BCTL1}$/$\overline{CS5}$	L15	V_{DDH}
J19	GPIO23/TDM0TDAT/$\overline{IRQ13}$	L16	GND
J20	GND	L17	GND
J21	GPIO25/TDM0RCLK/$\overline{IRQ15}$	L18	$\overline{CS3}$
J22	A30	L19	V_{DDH}
K2	HA15	L20	A27
K3	HA21	L21	A25
K4	HA16	L22	A22
K5	$\overline{PWE3}$/$\overline{PSDDQM3}$/$\overline{PBS3}$	M2	HD28
K6	$\overline{PWE1}$/$\overline{PSDDQM1}$/$\overline{PBS1}$	M3	HD31
K7	$\overline{POE}$/$\overline{PSDRAS}$/PGPL2	M4	V_{DDH}
K8	$\overline{IRQ2}$/BADDR30	M5	GND
K9	Reserved	M6	GND
K10	GND	M7	V_{DDH}
K11	GND	M8	V_{DD}
K12	GND	M9	V_{DDH}
K13	GND	M10	GND
K14	CLKOUT	M14	GND

Table 3-2. MSC8126 Signal Listing by Ball Designator (Continued)

Des.	Signal Name	Des.	Signal Name
M15	V_{DDH}	P12	V_{CCSYN}
M16	$\overline{HBRST}$	P13	GND
M17	V_{DDH}	P14	GND
M18	V_{DDH}	P15	$\overline{TA}$
M19	GND	P16	$\overline{BR}$
M20	V_{DDH}	P17	$\overline{TEA}$
M21	A24	P18	$\overline{PSDVAL}$
M22	A21	P19	DP0/DREQ1/$\overline{EXT_BR2}$
N2	HD26	P20	V_{DDH}
N3	HD30	P21	GND
N4	HD29	P22	A19
N5	HD24	R2	HD18
N6	$\overline{PWE2}$/$\overline{PSDDQM2}$/$\overline{PBS2}$	R3	V_{DDH}
N7	V_{DDH}	R4	GND
N8	$\overline{HWBS0}$/$\overline{HDBS0}$/$\overline{HWBE0}$/$\overline{HDBE0}$	R5	HD22
N9	$\overline{HBCS}$	R6	$\overline{HWBS6}$/$\overline{HDBS6}$/$\overline{HWBE6}$/$\overline{HDBE6}$/$\overline{PWE6}$/$\overline{PSDDQM6}$/$\overline{PBS6}$
N10	GND	R7	$\overline{HWBS4}$/$\overline{HDBS4}$/$\overline{HWBE4}$/$\overline{HDBE4}$/$\overline{PWE4}$/$\overline{PSDDQM4}$/$\overline{PBS4}$
N14	GND	R8	TSZ1
N15	$\overline{HRDS}$/HRW/$\overline{HRDE}$	R9	TSZ3
N16	$\overline{BG}$	R10	$\overline{IRQ1}$/$\overline{GBL}$
N17	$\overline{HCS}$	R11	V_{DD}
N18	$\overline{CS0}$	R12	V_{DD}
N19	$\overline{PSDWE}$/PGPL1	R13	V_{DD}
N20	GPIO26/TDM0RDAT	R14	TT0/HA7
N21	A23	R15	$\overline{IRQ7}$/DP7/DREQ4
N22	A20	R16	$\overline{IRQ6}$/DP6/DREQ3
P2	HD20	R17	$\overline{IRQ3}$/DP3/DREQ2/$\overline{EXT_BR3}$
P3	HD27	R18	$\overline{TS}$
P4	HD25	R19	$\overline{IRQ2}$/DP2/$\overline{DACK2}$/$\overline{EXT_DBG2}$
P5	HD23	R20	A17
P6	$\overline{HWBS3}$/$\overline{HDBS3}$/$\overline{HWBE3}$/$\overline{HDBE3}$	R21	A18
P7	$\overline{HWBS2}$/$\overline{HDBS2}$/$\overline{HWBE2}$/$\overline{HDBE2}$	R22	A16
P8	$\overline{HWBS1}$/$\overline{HDBS1}$/$\overline{HWBE1}$/$\overline{HDBE1}$	T2	HD17
P9	HCLKIN	T3	HD21
P10	GND	T4	HD1/DSISYNC
P11	GND_{SYN}	T5	HD0/SWTE

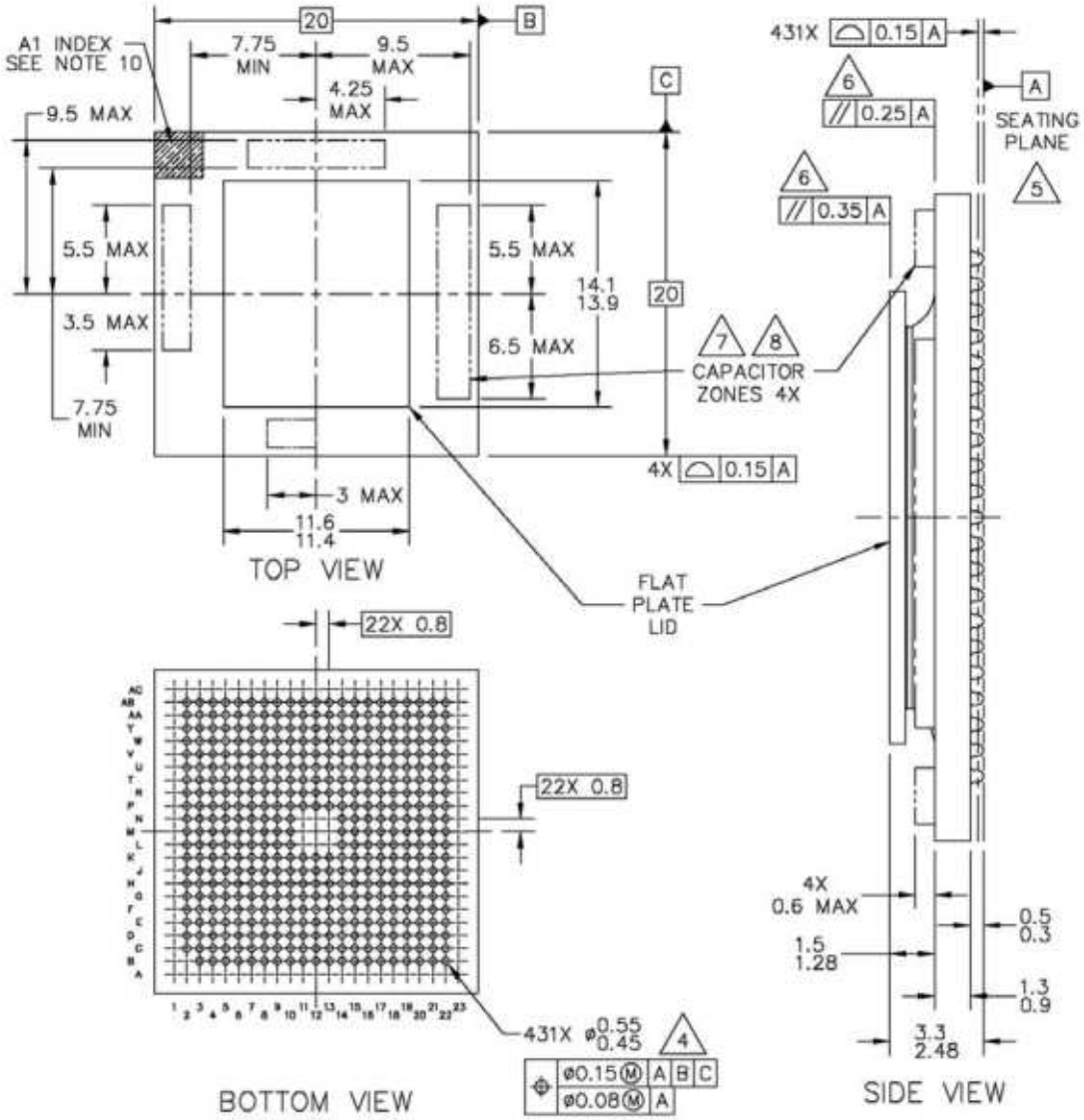
Table 3-2. MSC8126 Signal Listing by Ball Designator (Continued)

Des.	Signal Name	Des.	Signal Name
T6	$\overline{\text{HWBS7}}$/$\overline{\text{HDBS7}}$/$\overline{\text{HWBE7}}$/$\overline{\text{HDBE7}}$/$\overline{\text{PWE7}}$/$\overline{\text{PSDDQM7}}$/$\overline{\text{PBS7}}$	U21	A12
T7	$\overline{\text{HWBS5}}$/$\overline{\text{HDBS5}}$/$\overline{\text{HWBE5}}$/$\overline{\text{HDBE5}}$/$\overline{\text{PWE5}}$/$\overline{\text{PSDDQM5}}$/$\overline{\text{PBS5}}$	U22	A13
T8	TSZ0	V2	HD3/MODCK1
T9	TSZ2	V3	V_{DDH}
T10	$\overline{\text{TBST}}$	V4	GND
T11	V_{DD}	V5	D0
T12	D16	V6	D1
T13	TT1	V7	D4
T14	D21	V8	D5
T15	D23	V9	D7
T16	$\overline{\text{IRQ5}}$/DP5/$\overline{\text{DACK4}}$/$\overline{\text{EXT_BG3}}$	V10	D10
T17	$\overline{\text{IRQ4}}$/DP4/$\overline{\text{DACK3}}$/$\overline{\text{EXT_DBG3}}$	V11	D12
T18	$\overline{\text{IRQ1}}$/DP1/$\overline{\text{DACK1}}$/$\overline{\text{EXT_BG2}}$	V12	D13
T19	D30	V13	D18
T20	GND	V14	D20
T21	A15	V15	GND
T22	A14	V16	D24
U2	HD16	V17	D27
U3	HD19	V18	D29
U4	HD2/DSI64	V19	A8
U5	D2	V20	A9
U6	D3	V21	A10
U7	D6	V22	A11
U8	D8	W2	HD6
U9	D9	W3	HD5/CNFGS
U10	D11	W4	HD4/MODCK2
U11	D14	W5	GND
U12	D15	W6	GND
U13	D17	W7	V_{DDH}
U14	D19	W8	V_{DDH}
U15	D22	W9	GND
U16	D25	W10	HDST1/HA10
U17	D26	W11	HDST0/HA9
U18	D28	W12	V_{DDH}
U19	D31	W13	GND
U20	V_{DDH}	W14	HD40/D40/ETHRXD0

Table 3-2. MSC8126 Signal Listing by Ball Designator (Continued)

Des.	Signal Name	Des.	Signal Name
W15	V_{DDH}	AA9	V_{DDH}
W16	HD33/D33/reserved	AA10	HD54/D54/ETHTX_EN
W17	V_{DDH}	AA11	HD52/D52
W18	HD32/D32/reserved	AA12	V_{DDH}
W19	GND	AA13	GND
W20	GND	AA14	V_{DDH}
W21	A7	AA15	HD46/D46/ETHTXT0
W22	A6	AA16	GND
Y2	HD7	AA17	HD42/D42/ETHRXD2/reserved
Y3	HD15	AA18	HD38/D38/reserved
Y4	V_{DDH}	AA19	HD35/D35/reserved
Y5	HD9	AA20	A0
Y6	V_{DD}	AA21	A2
Y7	HD60/D60/ETHCOL/reserved	AA22	A3
Y8	HD58/D58/ETHMDC	AB2	GND
Y9	GND	AB3	HD13
Y10	V_{DDH}	AB4	HD11
Y11	HD51/D51	AB5	HD8
Y12	GND	AB6	HD62/D62
Y13	V_{DDH}	AB7	HD61/D61
Y14	HD43/D43/ETHRXD3/reserved	AB8	HD57/D57/ETHRX_ER
Y15	GND	AB9	HD56/D56/ETHRX_DV/ETHCRS_DV
Y16	V_{DDH}	AB10	HD55/D55/ETHTX_ER/reserved
Y17	GND	AB11	HD53/D53
Y18	HD37/D37/reserved	AB12	HD50/D50
Y19	HD34/D34/reserved	AB13	HD49/D49/ETHTXD3/reserved
Y20	V_{DDH}	AB14	HD48/D48/ETHTXD2/reserved
Y21	A4	AB15	HD47/D47/ETHTXD1
Y22	A5	AB16	HD45/D45
AA2	V_{DD}	AB17	HD44/D44
AA3	HD14	AB18	HD41/D41/ETHRXD1
AA4	HD12	AB19	HD39/D39/reserved
AA5	HD10	AB20	HD36/D36/reserved
AA6	HD63/D63	AB21	A1
AA7	HD59/D59/ETHMDIO	AB22	V_{DD}
AA8	GND		

3.2 MSC8126 Package Mechanical Drawing



Notes:

1. All dimensions in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M–1994.
3. Features are symmetrical about the package center lines unless dimensioned otherwise.
4. Maximum solder ball diameter measured parallel to Datum A.
5. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
6. Parallelism measurement shall exclude any effect of mark on top surface of package.
7. Capacitors may not be present on all devices.
8. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
9. FC CBGA (Ceramic) package code: 5238.
   FC PBGA (Plastic) package code: 5263.
10. Pin 1 indicator can be in the form of number 1 marking or an “L” shape marking.

Figure 3-3. MSC8126 Mechanical Information, 431-pin FC-PBGA Package

Design Considerations 4

The following sections discuss areas to consider when the MSC8126 device is designed into a system.

4.1 Start-up Sequencing Recommendations

Use the following guidelines for start-up and power-down sequences:

- Assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ before applying power and keep the signals driven low until the power reaches the required minimum power levels. This can be implemented via weak pull-down resistors.
- CLKIN can be held low or allowed to toggle during the beginning of the power-up sequence. However, CLKIN must start toggling before the deassertion of $\overline{\text{PORESET}}$ and after both power supplies have reached nominal voltage levels.
- If possible, bring up V_{DD}/V_{CCSYN} and V_{DDH} together. If it is not possible, raise V_{DD}/V_{CCSYN} first and then bring up V_{DDH}. V_{DDH} should not exceed V_{DD}/V_{CCSYN} until V_{DD}/V_{CCSYN} reaches its nominal voltage level. Similarly, bring both voltage levels down together. If that is not possible reverse the power-up sequence, with V_{DDH} going down first and then V_{DD}/V_{CCSYN}.

Note: This recommended power sequencing for the MSC8126 is different from the MSC8102.

External voltage applied to any input line must not exceed the I/O supply V_{DDH} by more than 0.8 V at any time, including during power-up. Some designs require pull-up voltages applied to selected input lines during power-up for configuration purposes. This is an acceptable exception to the rule. However, each such input can draw up to 80 mA per input pin per device in the system during start-up.

After power-up, V_{DDH} must not exceed V_{DD}/V_{CCSYN} by more than 2.6 V.

4.2 Power Supply Design Considerations

Note: *MSC8122 and MSC8126 Power Circuit Design Recommendations and Examples* (AN2937) provides detailed design information.

Figure 4-1 shows the recommended power decoupling circuit for the core power supply. The voltage regulator and the decoupling capacitors should supply the required device current without any drop in voltage on the device pins. The voltage on the package pins should not drop below the minimum specified voltage level even for a very short spikes. This can be achieved by using the following guidelines:

- For the core supply, use a voltage regulator rated at 1.2 V with nominal rating of at least 3 A. This rating does not reflect actual average current draw, but is recommended because it resists changes imposed by transient spikes and has better voltage recovery time than supplies with lower current ratings.

- Decouple the supply using low-ESR capacitors mounted as close as possible to the socket. **Figure 4-1** shows three capacitors in parallel to reduce the resistance. Three capacitors is a recommended minimum number. If possible, mount at least one of the capacitors directly below the MSC8126 device.

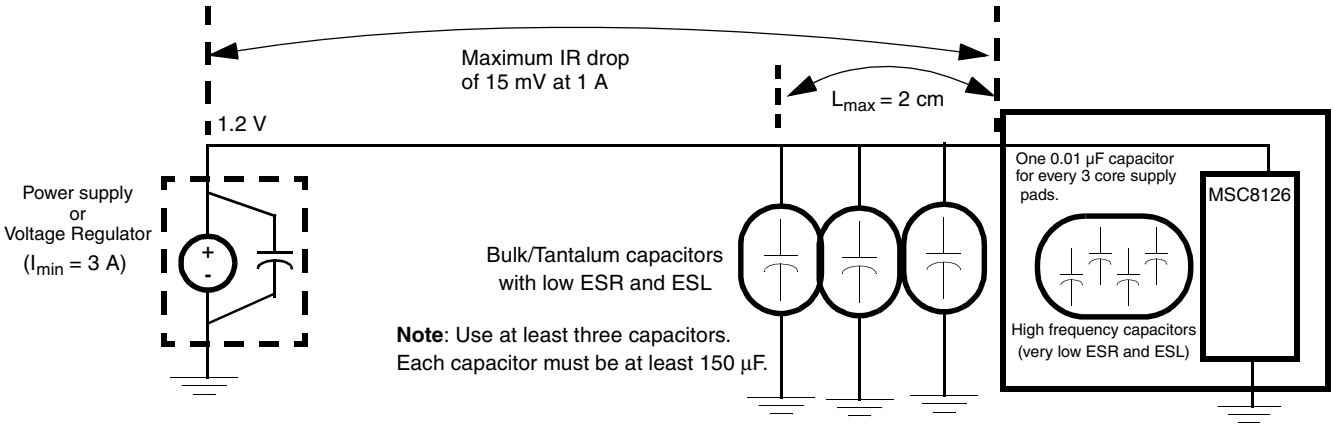


Figure 4-1. Core Power Supply Decoupling

Each V_{CC} and V_{DD} pin on the MSC8126 device should have a low-impedance path to the board power supply. Similarly, each GND pin should have a low-impedance path to the ground plane. The power supply pins drive distinct groups of logic on the chip. The V_{CC} power supply should have at least four 0.1 µF by-pass capacitors to ground located as closely as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC}, V_{DD}, and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MSC8126 have fast rise and fall times. PCB trace interconnection length should be minimized to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PCB trace lengths of six inches are recommended. For the DSI control signals in synchronous mode, ensure that the layout supports the DSI AC timing requirements and minimizes any signal crosstalk. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PCB traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC}, V_{DD}, and GND circuits. Pull up all unused inputs or signals that will be inputs during reset.

Special care should be taken to minimize the noise levels on the PLL supply pins. There is one pair of PLL supply pins: V_{CCSYN}-GND_{SYN}. To ensure internal clock stability, filter the power to the V_{CCSYN} input with a circuit similar to the one in **Figure 4-2**. For optimal noise filtering, place the circuit as close as possible to V_{CCSYN}. The 0.01-µF capacitor should be closest to V_{CCSYN}, followed by the 10-µF capacitor, the 10-nH inductor, and finally the 10-Ω resistor to V_{DD}. These traces should be kept short and direct. Provide an extremely low impedance path to the ground plane for GND_{SYN}. Bypass GND_{SYN} to V_{CCSYN} by a 0.01-µF capacitor located as close as possible to the chip package. For best results, place this capacitor on the backside of the PCB aligned with the depopulated void on the MSC8126 located in the square defined by positions, L11, L12, L13, M11, M12, M13, N11, N12, and N13.

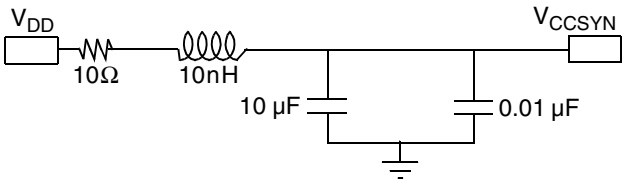


Figure 4-2. V_{CCSYN} Bypass

4.3 Connectivity Guidelines

Unused output pins can be disconnected, and unused input pins should be connected to the non-active value, via resistors to V_{DDH} or GND, except for the following:

- If the DSI is unused (DDR[DSIDIS] is set), $\overline{\text{HCS}}$ and $\overline{\text{HBCS}}$ must pulled up and all the rest of the DSI signals can be disconnected.
- When the DSI uses synchronous mode, $\overline{\text{HTA}}$ must be pulled up. In asynchronous mode, $\overline{\text{HTA}}$ should be pulled either up or down, depending on design requirements.
- $\overline{\text{HDST}}$ can be disconnected if the DSI is in big-endian mode, or if the DSI is in little-endian mode and the DCR[DSRFA] bit is set.
- When the DSI is in 64-bit data bus mode and DCR[BEM] is cleared, pull up $\overline{\text{HWBS[1–3]}}$/$\overline{\text{HDBS[1–3]}}$/$\overline{\text{HWBE[1–3]}}$/$\overline{\text{HDBE[1–3]}}$ and $\overline{\text{HWBS[4–7]}}$/$\overline{\text{HDBS[4–7]}}$/$\overline{\text{HWBE[4–7]}}$/$\overline{\text{HDBE[4–7]}}$/$\overline{\text{PWE[4–7]}}$/$\overline{\text{PSDDQM[4–7]}}$/$\overline{\text{PBS[4–7]}}$.
- When the DSI is in 32-bit data bus mode and DCR[BEM] is cleared, $\overline{\text{HWBS[1–3]}}$/$\overline{\text{HDBS[1–3]}}$/$\overline{\text{HWBE[1–3]}}$/$\overline{\text{HDBE[1–3]}}$ must be pulled up.
- When the DSI is in asynchronous mode, $\overline{\text{HBRST}}$ and HCLKIN should either be disconnected or pulled up.
- The following signals must be pulled up: $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, $\overline{\text{ARTRY}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{PSDVAL}}$, and $\overline{\text{AACK}}$.
- In single-master mode (BCR[EBM] = 0) with internal arbitration (PPC_ACR[EARB] = 0):
  - — $\overline{\text{BG}}$, $\overline{\text{DBG}}$, and $\overline{\text{TS}}$ can be left unconnected.
  - — $\overline{\text{EXT_BG[2–3]}}$, $\overline{\text{EXT_DBG[2–3]}}$, and $\overline{\text{GBL}}$ can be left unconnected if they are multiplexed to the system bus functionality. For any other functionality, connect the signal lines based on the multiplexed functionality.
  - — $\overline{\text{BR}}$ must be pulled up.
  - — $\overline{\text{EXT_BR[2–3]}}$ must be pulled up if multiplexed to the system bus functionality.
- If there is an external bus master (BCR[EBM] = 1):
  - — $\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{DBG}}$, and $\overline{\text{TS}}$ must be pulled up.
  - — $\overline{\text{EXT_BR[2–3]}}$, $\overline{\text{EXT_BG[2–3]}}$, and $\overline{\text{EXT_DBG[2–3]}}$ must be pulled up if multiplexed to the system bus functionality.
- In single-master mode, $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ can be selected as $\overline{\text{IRQ}}$ inputs and be connected to the non-active value. In other modes, they must be pulled up.

Note: The MSC8126 does not support DLL-enabled mode. For the following two clock schemes, ensure that the DLL is disabled (that is, the DLLDIS bit in the Hard Reset Configuration Word is set).

- If no system synchronization is required (for example, the design does not use SDRAM), you can use any of the available clock modes.
- In the CLKIN synchronization mode, use the following connections:
  - — Connect the oscillator output through a buffer to CLKIN.
  - — Connect the CLKIN buffer output to the slave device (for example, SDRAM) making sure that the delay path between the clock buffer to the MSC8126 and the SDRAM is equal (that is, has a skew less than 100 ps).
  - — Valid clock modes in this scheme are: 0, 7, 15, 19, 21, 23, 28, 29, 30, and 31.

- In CLKOUT synchronization mode (for 400 MHz devices only), CLKOUT is the main clock to SDRAM. Use the following connections:
  - Connect the oscillator output through a buffer to CLKIN.
  - Connect CLKOUT through a zero-delay buffer to the slave device (for example, SDRAM) using the following guidelines:
    - The maximum delay between the slave and CLKOUT must not exceed 0.7 ns.
    - The maximum load on CLKOUT must not exceed 10 pF.
    - Use a zero-delay buffer with a jitter less than 0.3 ns.
  - All clock modes are valid in this clock scheme.

Note: See the Clock chapter in the *MSC8126 Reference Manual* for details.

- If the 60x-compatible system bus is not used and SIUMCR[PBSE] is set, $\overline{\text{PPBS}}$ can be disconnected. Otherwise, it should be pulled up.
- The following signals: SWTE, DSISYNC, DSI64, MODCK[1–2], CNFGS, CHIPID[0–3], RSTCONF and BM[0–2] are used to configure the MSC8126 and are sampled on the deassertion of the $\overline{\text{PORESET}}$ signal. Therefore, they should be tied to GND or V_{DDH} or through a pull-down or a pull-up resistor until the deassertion of the $\overline{\text{PORESET}}$ signal.
- When they are used, $\overline{\text{INT_OUT}}$ (if SIUMCR[INTODC] is cleared), $\overline{\text{NMI_OUT}}$, and $\overline{\text{IRQxx}}$ (if not full drive) signals must be pulled up.
- When the Ethernet controller is enabled and the SMII mode is selected, GPIO10 and GPIO14 must not be connected externally to any signal line.

Note: For details on configuration, see the *MSC8126 User's Guide* and *MSC8126 Reference Manual*. For additional information, refer to the *MSC8126 Design Checklist* (AN2903).

4.4 External SDRAM Selection

The external bus speed implemented in a system determines the speed of the SDRAM used on that bus. However, because of differences in timing characteristics among various SDRAM manufacturers, you may have use a faster speed rated SDRAM to assure efficient data transfer across the bus. For example, for 166 MHz operation, you may have to use 183 or 200 MHz SDRAM. Always perform a detailed timing analysis using the MSC8126 bus timing values and the manufacturer specifications for the SDRAM to ensure correct operation within your system design. The output delay listed in SDRAM specifications is usually given for a load of 30 pF. Scale the number to your specific board load using the typical scaling number provided by the SDRAM manufacturer.

4.5 Thermal Considerations

An estimation of the chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$ **Equation 1**

where

T_A = ambient temperature near the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$P_D = P_{INT} + P_{I/O}$ = power dissipation in the package (W)
$P_{INT} = I_{DD} \times V_{DD}$ = internal power dissipation (W)
$P_{I/O}$ = power dissipated from device on output pins (W)

The power dissipation values for the MSC8126 are listed in **Table 2-3**. The ambient temperature for the device is the air temperature in the immediate vicinity that would cool the device. The junction-to-ambient thermal resistances are JEDEC standard values that provide a quick and easy estimation of thermal performance. There are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. The value that more closely approximates a specific application depends on the power dissipated by other components on the printed circuit board (PCB). The value obtained using a single layer board is appropriate for tightly packed PCB configurations. The value obtained using a board with internal planes is more appropriate for boards with low power dissipation (less than 0.02 W/cm^2 with natural convection) and well separated components. Based on an estimation of junction temperature using this technique, determine whether a more detailed thermal analysis is required. Standard thermal management techniques can be used to maintain the device thermal junction temperature below its maximum. If T_J appears to be too high, either lower the ambient temperature or the power dissipation of the chip. You can verify the junction temperature by measuring the case temperature using a small diameter thermocouple (40 gauge is recommended) or an infrared temperature sensor on a spot on the device case that is painted black. The MSC8126 device case surface is too shiny (low emissivity) to yield an accurate infrared temperature measurement. Use the following equation to determine T_J:

$$T_J = T_T + (\theta_{JA} \times P_D)$$ **Equation 2**

where

T_T = thermocouple (or infrared) temperature on top of the package (°C)
θ_{JA} = thermal characterization parameter (°C/W)
P_D = power dissipation in the package (W)

Note: See *MSC8102, MSC8122, and MSC8126 Thermal Management Design Guidelines* (AN2601/D).

Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Package Type	Spheres	Core Voltage	Operating Temperature	Core Frequency (MHz)	Order Number
MSC8126	Flip Chip Plastic Ball Grid Array (FC-PBGA)	Lead-free	1.2 V	–40° to 105°C	400	MSC8126TVT6400
		Lead-bearing				MSC8126TMP6400
		Lead-free		0° to 90°C	500	MSC8126VT8000
		Lead-bearing				MSC8126MP8000

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