MIXED SIGNAL MICROCONTROLLER

FEATURES

- **Qualified for Automotive Applications**
- **Low Supply-Voltage Range: 1.8 V to 3.6 V**
- **Ultralow Power Consumption**
  - **Active Mode: 220 µA at 1 MHz, 2.2 V**
  - **Standby Mode: 0.5 µA**
  - **Off Mode (RAM Retention): 0.1 µA**
- **Five Power-Saving Modes**
- **Ultrafast Wake-Up From Standby Mode in Less Than 1 µs**
- **16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time**
- **Basic Clock Module Configurations**
  - **Internal Frequencies up to 16 MHz With One Calibrated Frequency**
  - **Internal Very Low Power Low-Frequency (LF) Oscillator**
  - **32-kHz Crystal**
  - **External Digital Clock Source**
- **16-Bit Timer_A With Two Capture/Compare Registers**
- **Brownout Detector**
- **On-Chip Comparator for Analog Signal Compare Function or Slope A/D (See Table 1)**
- **Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse**
- **On-Chip Emulation Logic With Spy-Bi-Wire Interface**
- **For Family Members Details, See Table 1 and Table 2**
- **Available in a 14-Pin Plastic Small-Outline Thin Package (TSSOP) (PW) and 16-Pin QFN (RSA)**
- **For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide* (SLAU144)**

DESCRIPTION

The Texas Instruments MSP430™ family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 µs.

The MSP430G2x01/MSP430G2x11 series is an ultralow-power mixed signal microcontroller with a built-in 16-bit timer and ten I/O pins. The MSP430G2x11 family members have a versatile analog comparator. For configuration details see Table 1.

Typical applications include low-cost sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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Table 1. Available Options

Device	BSL	EEM	Flash (KB)	RAM (B)	Timer_A	Comp_A+ Channel	Clock	I/O	Package Type
MSP430G2211	-	1	2	128	1x TA2	8	LF, DCO, VLO	10	16-QFN 14-TSSOP
MSP430G2201	-	1	2	128	1x TA2	-	LF, DCO, VLO	10	16-QFN 14-TSSOP
MSP430G2111	-	1	1	128	1x TA2	8	LF, DCO, VLO	10	16-QFN 14-TSSOP
MSP430G2101	-	1	1	128	1x TA2	-	LF, DCO, VLO	10	16-QFN 14-TSSOP
MSP430G2001	-	1	0.5	128	1x TA2	-	LF, DCO, VLO	10	16-QFN 14-TSSOP

Table 2. Ordering Information(1)(2)

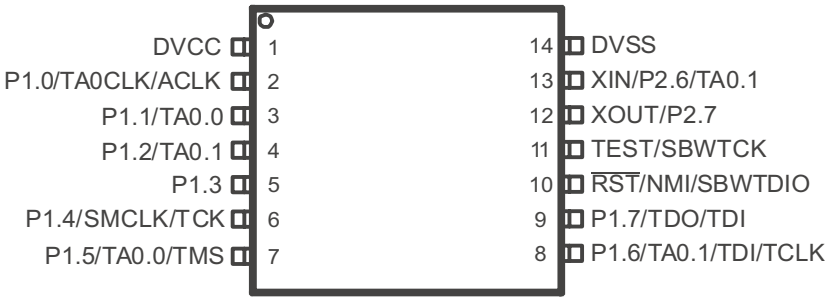
T_A	PACKAGED DEVICES(3)	
	PLASTIC 14-PIN TSSOP (PW)	PLASTIC 16-PIN QFN (RSA)
-40°C to 85°C	MSP430G2001IPW4Q1	MSP430G2001IRSAQ1
	MSP430G2101IPW4Q1	MSP430G2101IRSAQ1
	MSP430G2111IPW4Q1	MSP430G2111IRSAQ1
	MSP430G2201IPW4Q1	MSP430G2201IRSAQ1
	MSP430G2211IPW4Q1	MSP430G2211IRSAQ1
-40°C to 105°C	MSP430G2001TPW4Q1	MSP430G2001TRSAQ1
	MSP430G2101TPW4Q1	MSP430G2101TRSAQ1
	MSP430G2111TPW4Q1	MSP430G2111TRSAQ1
	MSP430G2201TPW4Q1	MSP430G2201TRSAQ1
	MSP430G2211TPW4Q1	MSP430G2211TRSAQ1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) All part numbers in this table correspond to die revision E.
(3) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

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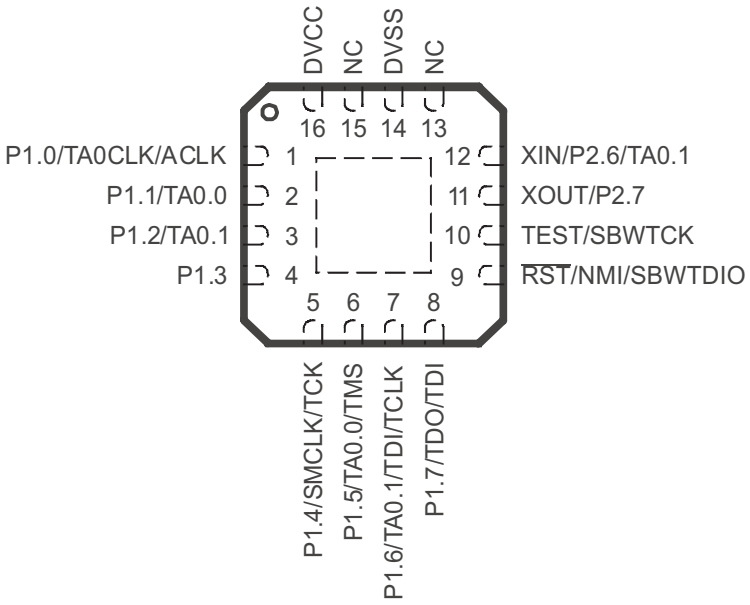
Device Pinout, MSP430G2x01

PW PACKAGE
(TOP VIEW)



NOTE: See port schematics in Application Information for detailed I/O information.

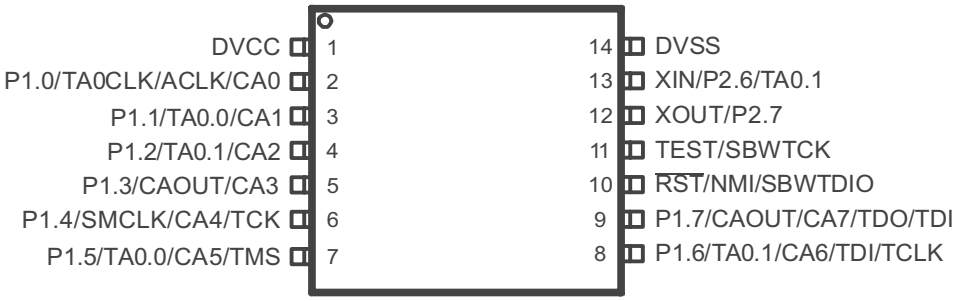
RSA PACKAGE
(TOP VIEW)



NOTE: See port schematics in Application Information for detailed I/O information.

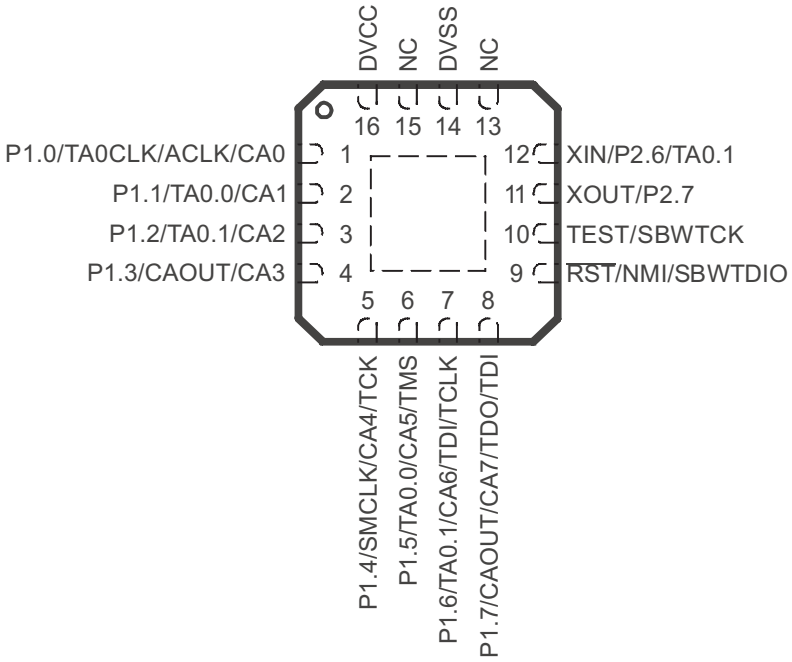
Device Pinout, MSP430G2x11

PW PACKAGE
(TOP VIEW)



NOTE: See port schematics in Application Information for detailed I/O information.

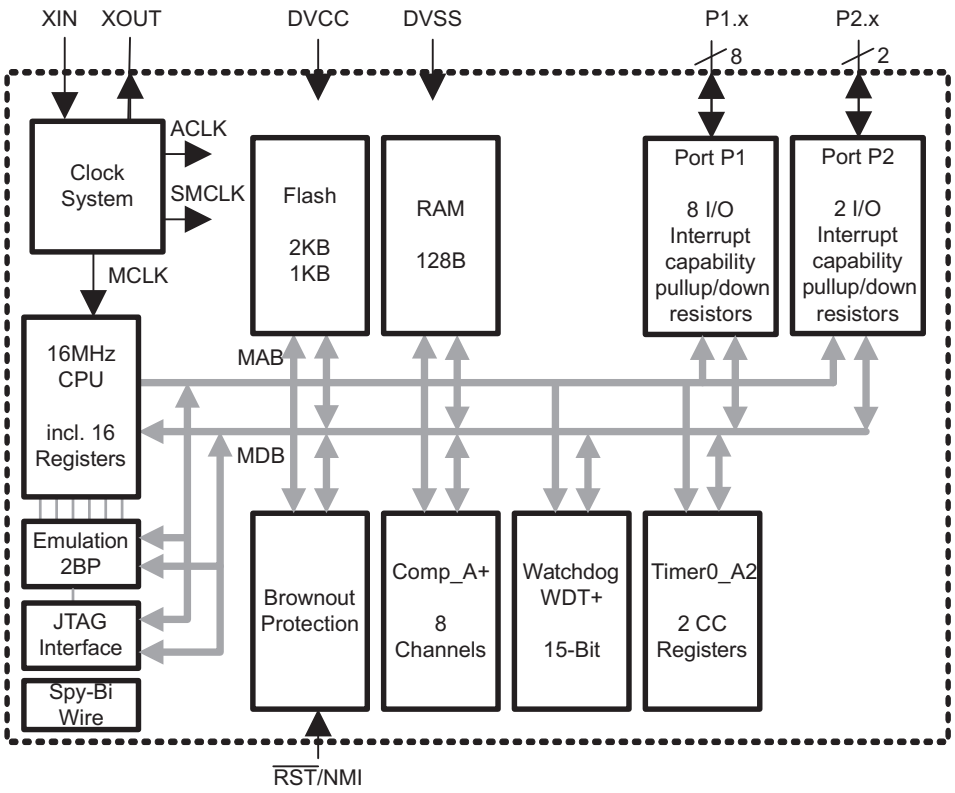
RSA PACKAGE
(TOP VIEW)



NOTE: See port schematics in Application Information for detailed I/O information.

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Functional Block Diagram, MSP430G2x11



Functional Block Diagram, MSP430G2x01

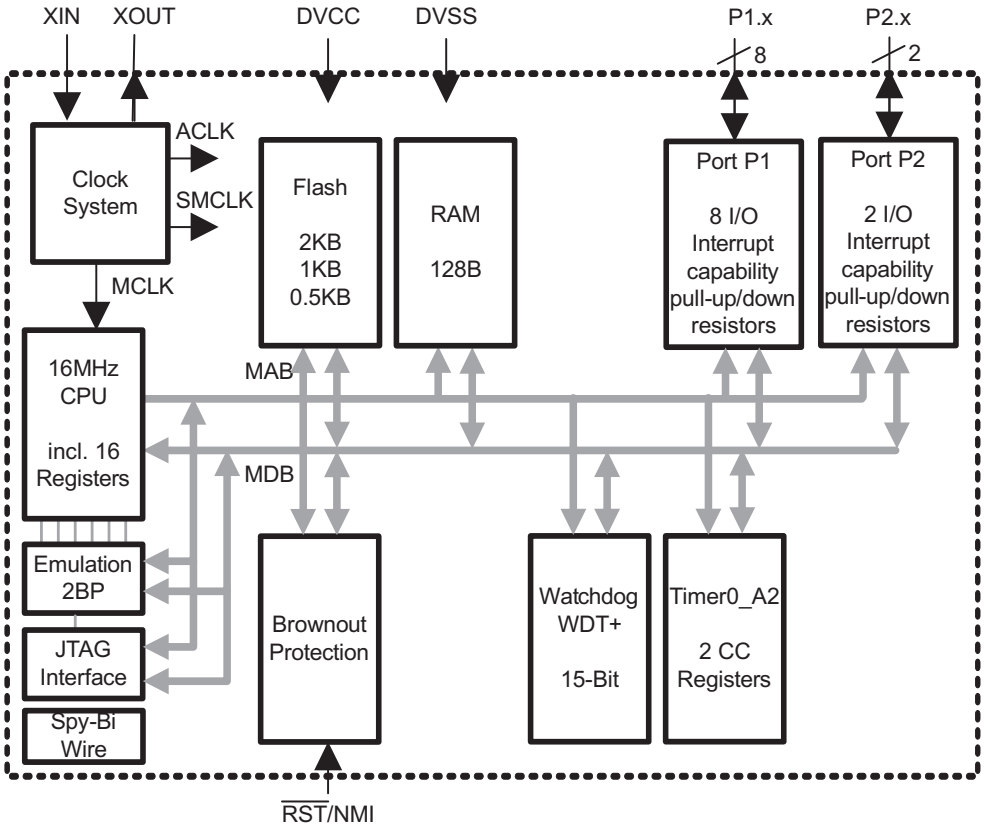


Table 3. Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	14 PW	16 RSA		
P1.0/ TA0CLK/ ACLK/ CA0	2	1	I/O	General-purpose digital I/O pin Timer0_A, clock signal TACLK input ACLK signal output Comparator_A+, CA0 input(1)
P1.1/ TA0.0/ CA1	3	2	I/O	General-purpose digital I/O pin Timer0_A, capture: CCI0A input, compare: Out0 output Comparator_A+, CA1 input(1)
P1.2/ TA0.1/ CA2	4	3	I/O	General-purpose digital I/O pin Timer0_A, capture: CCI1A input, compare: Out1 output Comparator_A+, CA2 input(1)
P1.3/ CA3/ CAOUT	5	4	I/O	General-purpose digital I/O pin Comparator_A+, CA3 input(1) Comparator_A+, output(1)
P1.4/ SMCLK/ CA4/ TCK	6	5	I/O	General-purpose digital I/O pin SMCLK signal output Comparator_A+, CA4 input(1) JTAG test clock, input terminal for device programming and test
P1.5/ TA0.0/ CA5/ TMS	7	6	I/O	General-purpose digital I/O pin Timer0_A, compare: Out0 output Comparator_A+, CA5 input(1) JTAG test mode select, input terminal for device programming and test
P1.6/ TA0.1/ CA6/ TDI/TCLK	8	7	I/O	General-purpose digital I/O pin Timer0_A, compare: Out1 output Comparator_A+, CA6 input(1) JTAG test data input or test clock input during programming and test
P1.7/ CA7/ CAOUT/ TDO/TDI(2)	9	8	I/O	General-purpose digital I/O pin CA7 input(1) Comparator_A+, output(1) JTAG test data output terminal or test data input during programming and test
XIN/ P2.6/ TA0.1	13	12	I/O	Input terminal of crystal oscillator General-purpose digital I/O pin Timer0_A, compare: Out1 output
XOUT/ P2.7	12	11	I/O	Output terminal of crystal oscillator(3) General-purpose digital I/O pin
$\overline{\text{RST}}$/ NMI/ SBWTDIO	10	9	I	Reset Nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/ SBWTCK	11	10	I	Selects test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test
DVCC	1	16	NA	Supply voltage
DVSS	14	14	NA	Ground reference
NC	-	15	NA	Not connected
QFN Pad	-	Pad	NA	QFN package pad connection to V_{SS} recommended.

(1) MSP430G2x11 only
(2) TDO or TDI is selected via JTAG instruction.
(3) If XOUT/P2.7 is used as an input, excess current flows until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

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SHORT-FORM DESCRIPTION

CPU

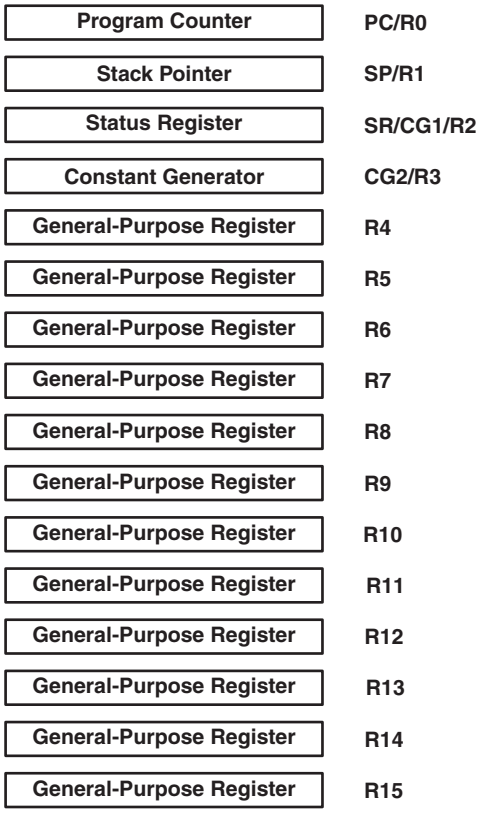
The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.



Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 4 shows examples of the three types of instruction formats; Table 5 shows the address modes.

Table 4. Instruction Word Formats

INSTRUCTION FORMAT	EXMPLE	OPERATION
Dual operands, source-destination	ADD R4,R5	R4 + R5 --> R5
Single operands, destination only	CALL R8	PC ->(TOS), R8-> PC
Relative jump, un/conditional	JNE	Jump-on-equal bit = 0

Table 5. Address Mode Descriptions(1)

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 - -> R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) - -> M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) - -> M(TONI)
Absolute	✓	✓	MOV &MEM,&TCDAT		M(MEM) - -> M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) - -> M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) - -> R11 R10 + 2- -> R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 - -> M(TONI)

(1) S = source, D = destination

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Operating Modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - DCO's dc generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator is disabled
  - Crystal oscillator is stopped

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Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (e.g., flash is not programmed) the CPU will go into LPM4 immediately after power-up.

Table 6. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Timer+ Flash key violation PC out-of-range(1)	PORIFG RSTIFG WDTIFG KEYV(2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(2)(3)	(non)-maskable (non)-maskable (non)-maskable	0FFFCh	30
			0FFFAh	29
			0FFF8h	28
Comparator_A+	CAIFG(4)(5)		0FFF6h	27
Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer_A2	TACCR0 CCIFG(4)	maskable	0FFF2h	25
Timer_A2	TACCR1 CCIFG, TAIFG(2)(4)	maskable	0FFF0h	24
			0FFEEh	23
			0FFECh	22
			0FFEAh	21
			0FFE8h	20
I/O Port P2 (two flags)	P2IFG.6 to P2IFG.7(2)(4)	maskable	0FFE6h	19
I/O Port P1 (eight flags)	P1IFG.0 to P1IFG.7(2)(4)	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
See (6)			0FFDEh to 0FFC0h	15 to 0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
(2) Multiple source flags
(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
(4) Interrupt flags are located in the module.
(5) Devices with Comparator_A+ only
(6) The interrupt vectors at addresses 0FFDEh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

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Special Function Registers (SFRs)

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

Legend		
	rw:	Bit can be read and written.
	rw-0,1:	Bit can be read and written. It is reset or set by PUC.
	rw-(0,1):	Bit can be read and written. It is reset or set by POR.
		SFR bit is not present in device.

Table 7. Interrupt Enable Register 1 and 2

Address	7	6	5	4	3	2	1	0
00h			**ACCVIE**	**NMIIE**			**OFIE**	**WDTIE**
			rw-0	rw-0			rw-0	rw-0

WDTIE	Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.
OFIE	Oscillator fault interrupt enable
NMIIE	(Non)maskable interrupt enable
ACCVIE	Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h								

Table 8. Interrupt Flag Register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				**NMIIFG**	**RSTIFG**	**PORIFG**	**OFIFG**	**WDTIFG**
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG	Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power-on or a reset condition at the $\overline{RST}$/NMI pin in reset mode.
OFIFG	Flag set on oscillator fault.
PORIFG	Power-On Reset interrupt flag. Set on V_{CC} power-up.
RSTIFG	External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power-up.
NMIIFG	Set via $\overline{RST}$/NMI pin

Address	7	6	5	4	3	2	1	0
03h								

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Memory Organization

Table 9. Memory Organization

		MSP430G2001 MSP430G2011	MSP430G2101 MSP430G2111	MSP430G2201 MSP430G2211
Memory	Size	512B	1kB	2kB
Main: interrupt vector	Flash	0xFFFF to 0xFFC0	0xFFFF to 0xFFC0	0xFFFF to 0xFFC0
Main: code memory	Flash	0xFFFF to 0xFE00	0xFFFF to 0xFC00	0xFFFF to 0xF800
Information memory	Size	256 Byte	256 Byte	256 Byte
	Flash	010FFh to 01000h	010FFh to 01000h	010FFh to 01000h
RAM	Size	128B	128B	128B
		027Fh to 0200h	027Fh to 0200h	027Fh to 0200h
Peripherals	16-bit	01FFh to 0100h	01FFh to 0100h	01FFh to 0100h
	8-bit	0FFh to 010h	0FFh to 010h	0FFh to 010h
	8-bit SFR	0Fh to 00h	0Fh to 00h	0Fh to 00h

Flash Memory

The flash memory can be programmed via the Spy-Bi-Wire/JTAG port or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset segment A is protected against programming and erasing. It can be unlocked but care should be taken not to erase this segment if the device-specific calibration data is required.

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Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide* (SLAU144).

Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator and an internal digitally controlled oscillator (DCO). The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced either from a 32768-Hz watch crystal or the internal LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

Table 10. DCO Calibration Data (Provided From Factory In Flash Information Memory Segment A)

DCO FREQUENCY	CALIBRATION REGISTER	SIZE	ADDRESS
1 MHz	CALBC1_1MHZ	byte	010FFh
	CALDCO_1MHZ	byte	010FEh

Brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

Digital I/O

There is one 8-bit I/O port implemented—port P1—and two bits of I/O port P2:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all the eight bits of port P1 and the two bits of port P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup/pulldown resistor.

WDT+ Watchdog Timer

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

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Timer_A2

Timer_A2 is a 16-bit timer/counter with two capture/compare registers. Timer_A2 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 11. Timer_A2 Signal Connections - Devices With No Analog

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PW	RSA					PW	RSA
2 - P1.0	1 - P1.0	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
2 - P1.0	1 - P1.0	TACLK	INCLK				
3 - P1.1	2 - P1.1	TA0	CCI0A	CCR0	TA0	3 - P1.1	2 - P1.1
		ACLK (internal)	CCI0B			7 - P1.5	6 - P1.5
		V_{SS}	GND				
		V_{CC}	V_{CC}				
4 - P1.2	3 - P1.2	TA1	CCI1A	CCR1	TA1	4 - P1.2	3 - P1.2
		TA1	CCI1B			8 - P1.6	7 - P1.6
		V_{SS}	GND			13 - P2.6	12 - P2.6
		V_{CC}	V_{CC}				

Table 12. Timer_A2 Signal Connections - Devices With Comparator_A+

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PW	RSA					PW	RSA
2 - P1.0	1 - P1.0	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
2 - P1.0	1 - P1.0	TACLK	INCLK				
3 - P1.1	2 - P1.1	TA0	CCI0A	CCR0	TA0	3 - P1.1	2 - P1.1
		ACLK (internal)	CCI0B			7 - P1.5	6 - P1.5
		V_{SS}	GND				
		V_{CC}	V_{CC}				
4 - P1.2	3 - P1.2	TA1	CCI1A	CCR1	TA1	4 - P1.2	3 - P1.2
		CAOUT (internal)	CCI1B			8 - P1.6	7 - P1.6
		V_{SS}	GND			13 - P2.6	12 - P2.6
		V_{CC}	V_{CC}				

Comparator_A+ (MSP430G2x11 Only)

The primary function of the comparator_A+module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

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Peripheral File Map

Table 13. Peripherals With Word Access

MODULE	REGISTER DESCRIPTION	REGISTER NAME	OFFSET
Timer_A	Capture/compare register	TACCR1	0174h
	Capture/compare register	TACCR0	0172h
	Timer_A register	TAR	0170h
	Capture/compare control	TACCTL1	0164h
	Capture/compare control	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Flash Memory	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
Watchdog Timer+	Watchdog/timer control	WDTCTL	0120h

Table 14. Peripherals With Byte Access

MODULE	REGISTER DESCRIPTION	REGISTER NAME	OFFSET
Comparator_A+ (MSP430G2x11 only)	Comparator_A+ port disable	CAPD	05Bh
	Comparator_A+ control 2	CACTL2	05Ah
	Comparator_A+ control 1	CACTL1	059h
Basic Clock System+	Basic clock system control 3	BCSCTL3	053h
	Basic clock system control 2	BCSCTL2	058h
	Basic clock system control 1	BCSCTL1	057h
	DCO clock frequency control	DCOCTL	056h
Port P2	Port P2 resistor enable	P2REN	02Fh
	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 resistor enable	P1REN	027h
	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Function	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

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Absolute Maximum Ratings(1)

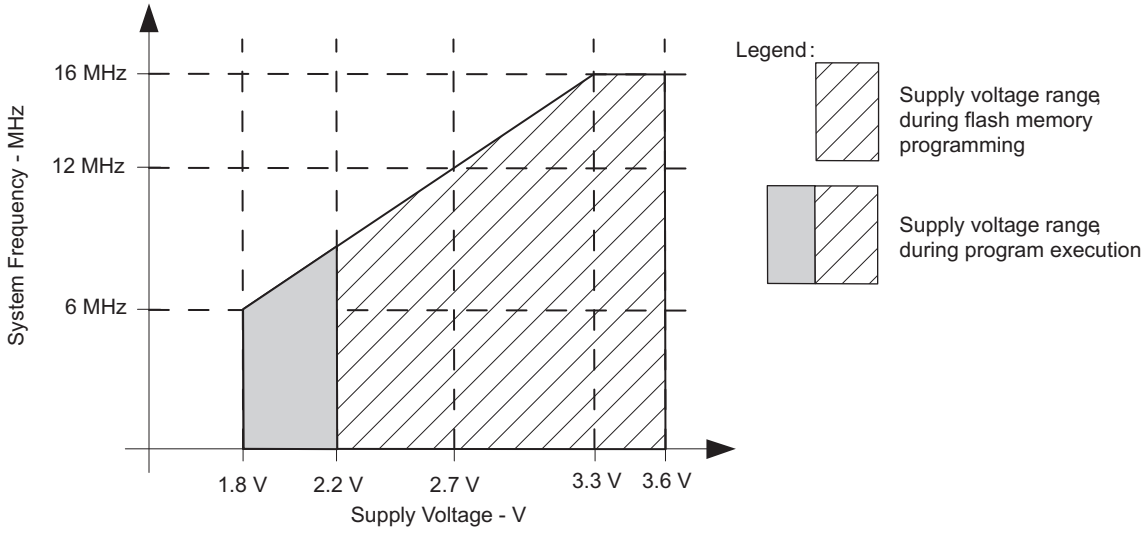
Voltage applied at V_{CC} to V_{SS}		-0.3 V to 4.1 V
Voltage applied to any pin(2)		-0.3 V to V_{CC} + 0.3 V
Diode current at any device pin		±2 mA
Storage temperature range, T_{stg} (3)	Unprogrammed device	-55°C to 150°C
	Programmed device	-55°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	During program execution	1.8		3.6	V
		During flash program/erase	2.2		3.6	
V_{SS}	Supply voltage			0		V
T_A	Operating free-air temperature	I version	-40		85	°C
		T version	-40		105	
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(1)(2)	V_{CC} = 1.8 V, Duty cycle = 50% ± 10%	dc		6	MHz
		V_{CC} = 2.7 V, Duty cycle = 50% ± 10%	dc		12	
		V_{CC} ≥ 3.3 V, Duty cycle = 50% ± 10%	dc		16	

(1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
(2) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.



Note: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1. Safe Operating Area

Electrical Characteristics

Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{AM,1MHz}$	Active mode (AM) current (1 MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32768 Hz, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		220		µA
				3 V		300	370	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

Typical Characteristics - Active Mode Supply Current (Into V_{CC})

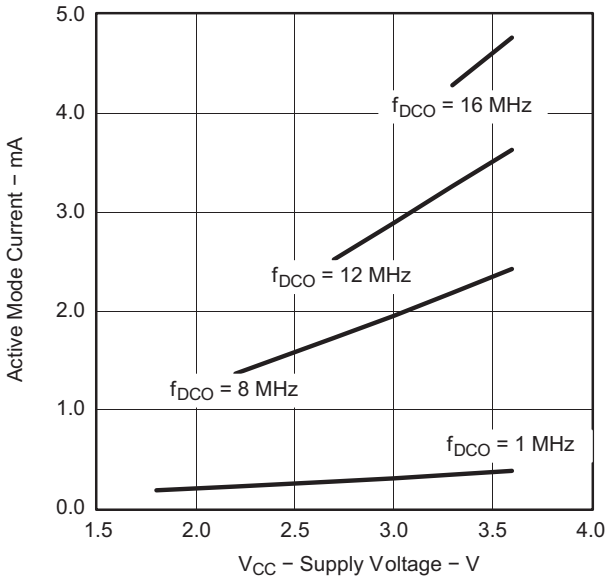


Figure 2. Active Mode Current vs V_{CC}, T_A = 25°C

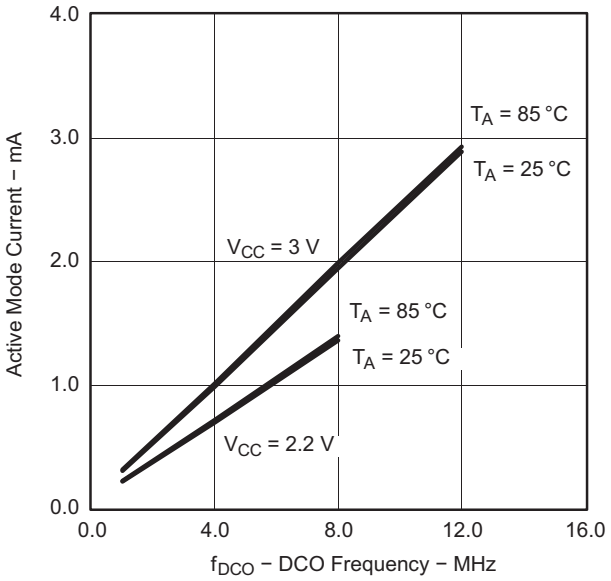


Figure 3. Active Mode Current vs DCO Frequency

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Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{LPM0,1MHz}$	Low-power mode 0 (LPM0) current(3)	f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz, f_{ACLK} = 32768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	25°C	2.2 V		65		µA
I_{LPM2}	Low-power mode 2 (LPM2) current(4)	f_{MCLK} = f_{SMCLK} = 0 MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		22		µA
			105°C				31	
$I_{LPM3,LFXT1}$	Low-power mode 3 (LPM3) current(4)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		0.7	1.5	µA
			105°C			3	6	
$I_{LPM3,VLO}$	Low-power mode 3 current, (LPM3)(4)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		0.5	0.7	µA
			105°C			2	5	
I_{LPM4}	Low-power mode 4 (LPM4) current(5)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	25°C	2.2 V		0.1	0.5	µA
			85°C			0.8	1.5	
			105°C			2	4	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF.
(3) Current for brownout and WDT clocked by SMCLK included.
(4) Current for brownout and WDT clocked by ACLK included.
(5) Current for brownout included.

Typical Characteristics Low-Power Mode Supply Currents

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

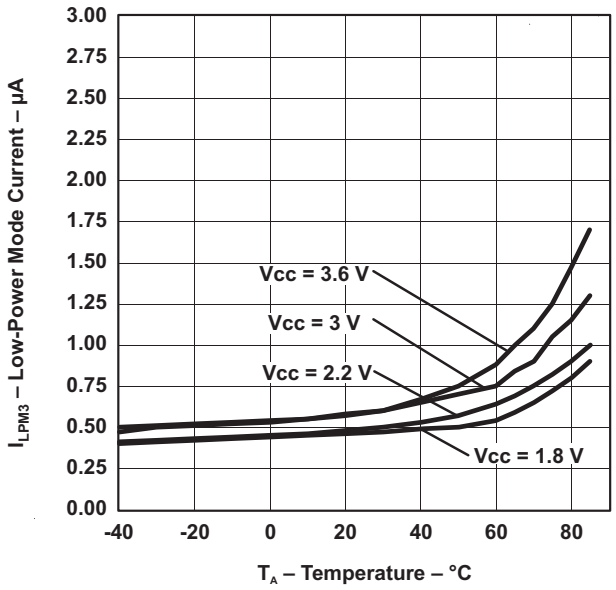


Figure 4. LPM3 Current vs Temperature

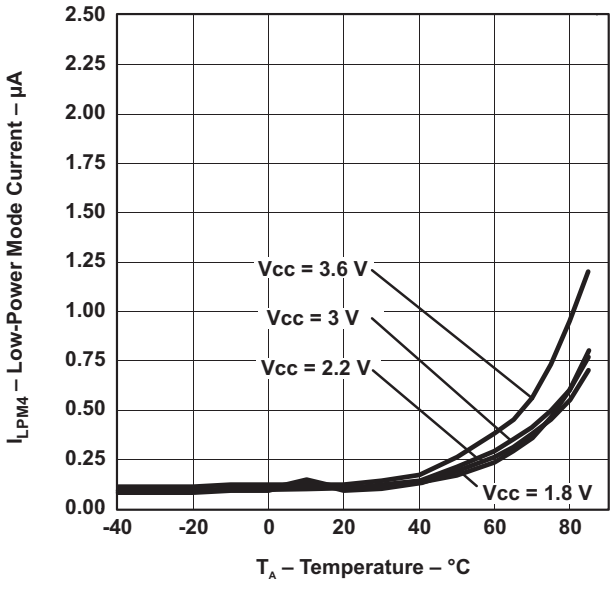


Figure 5. LPM4 Current vs Temperature

Schmitt-Trigger Inputs - Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			0.45 V_{CC}		0.75 V_{CC}	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage			0.25 V_{CC}		0.55 V_{CC}	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis (V_{IT+} - V_{IT-})		3 V	0.3		1	V
R_{Pull}	Pullup/pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$	3 V	20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

Leakage Current - Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.x)}$	High-impedance leakage current	(1) (2)	3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

Outputs - Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = -6 mA(1)	3 V		V_{CC} - 0.3		V
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 6 mA(1)	3 V		V_{SS} + 0.3		V

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

Output Frequency - Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	Px.y, C_L = 20 pF, R_L = 1 kΩ(1) (2)	3 V		12		MHz
f_{Port_CLK}	Clock output frequency	Px.y, C_L = 20 pF(2)	3 V		16		MHz

(1) A resistive divider with 2 × 0.5 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

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Typical Characteristics - Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

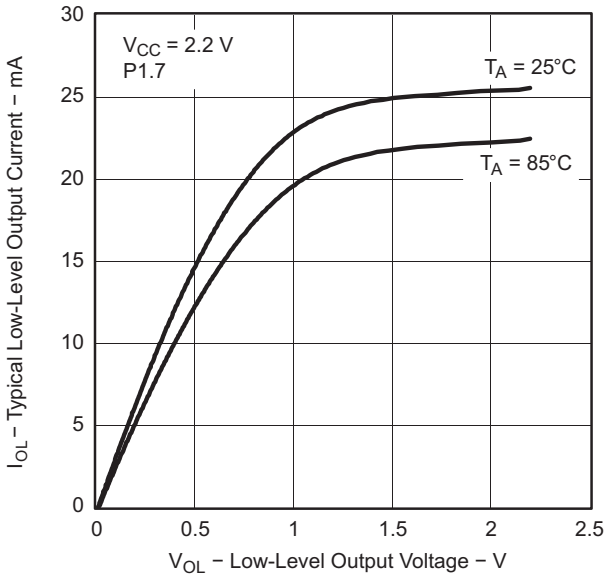


Figure 6.

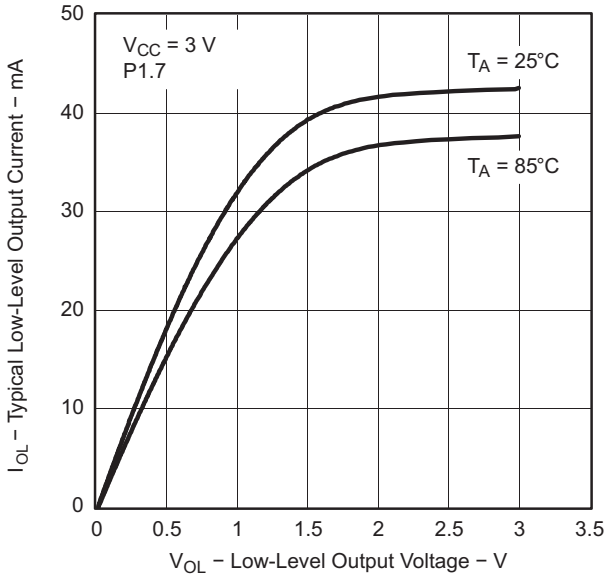


Figure 7.

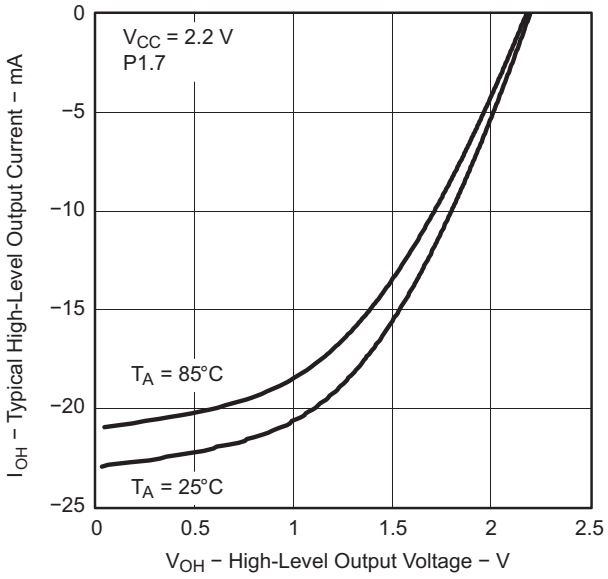


Figure 8.

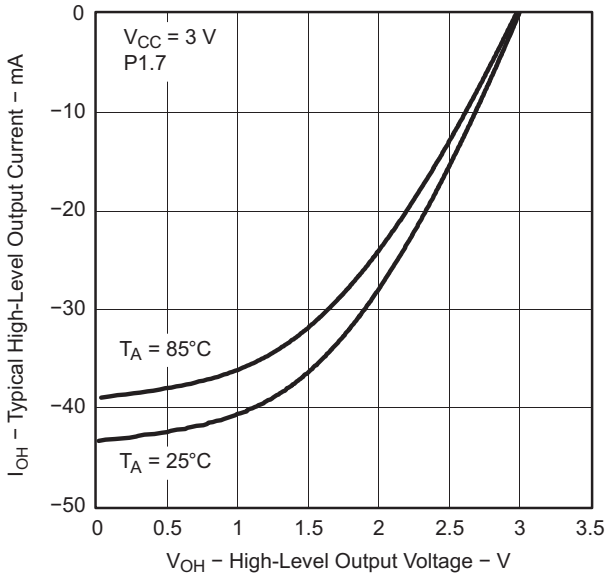


Figure 9.

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POR/Brownout Reset (BOR)(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(start)}$	See Figure 10	$dV_{CC}/dt \le 3$ V/s			0.7 × $V_{(B_IT-)}$		V
$V_{(B_IT-)}$	See Figure 10 through Figure 12	$dV_{CC}/dt \le 3$ V/s			1.35		V
$V_{hys(B_IT-)}$	See Figure 10	$dV_{CC}/dt \le 3$ V/s			130		mV
$t_{d(BOR)}$	See Figure 10					2000	µs
$t_{(reset)}$	Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally		2.2 V/3 V	2			µs

(1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B_IT-)}$ + $V_{hys(B_IT-)}$is ≤ 1.8 V.

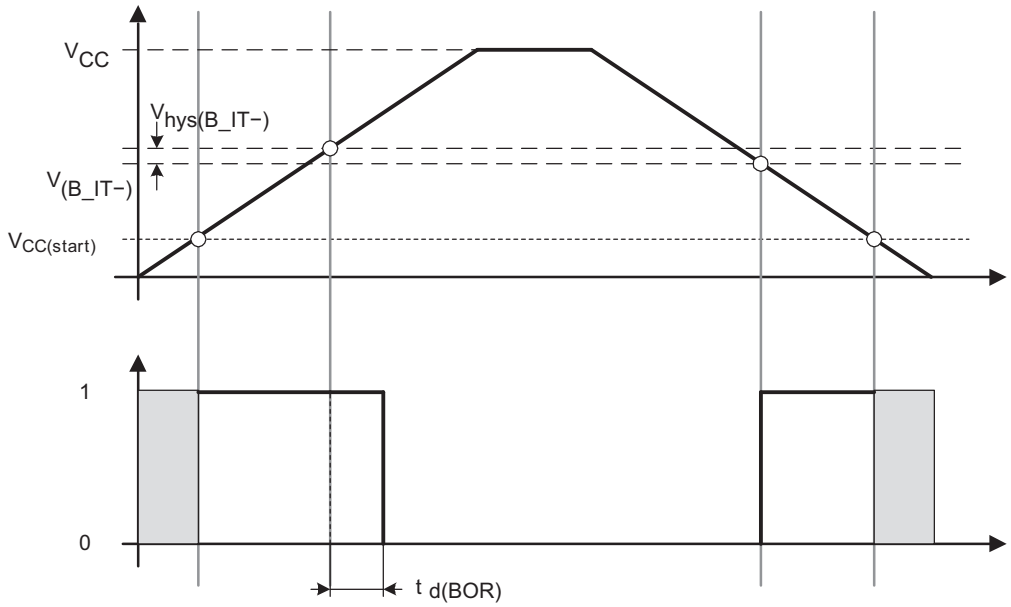


Figure 10. POR/Brownout Reset (BOR) vs Supply Voltage

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Typical Characteristics - POR/Brownout Reset (BOR)

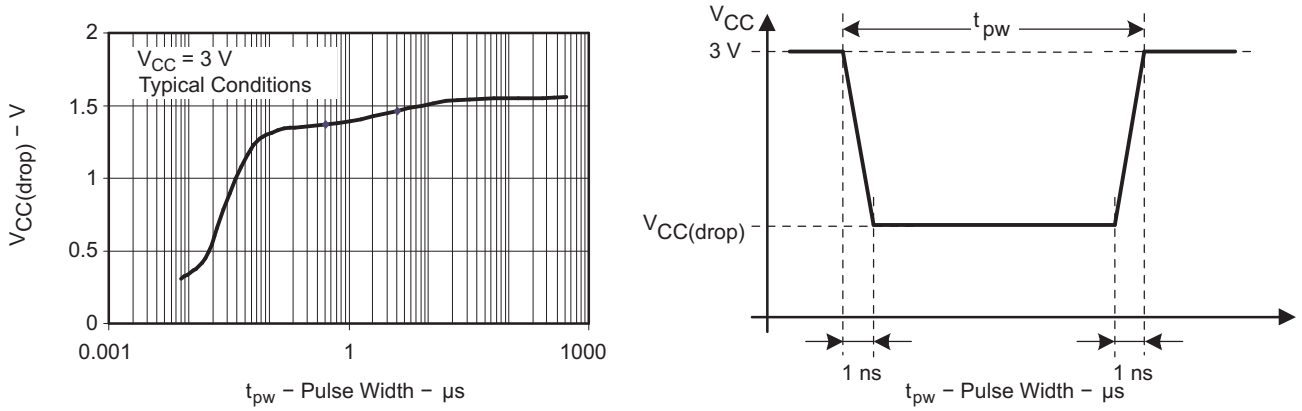


Figure 11. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

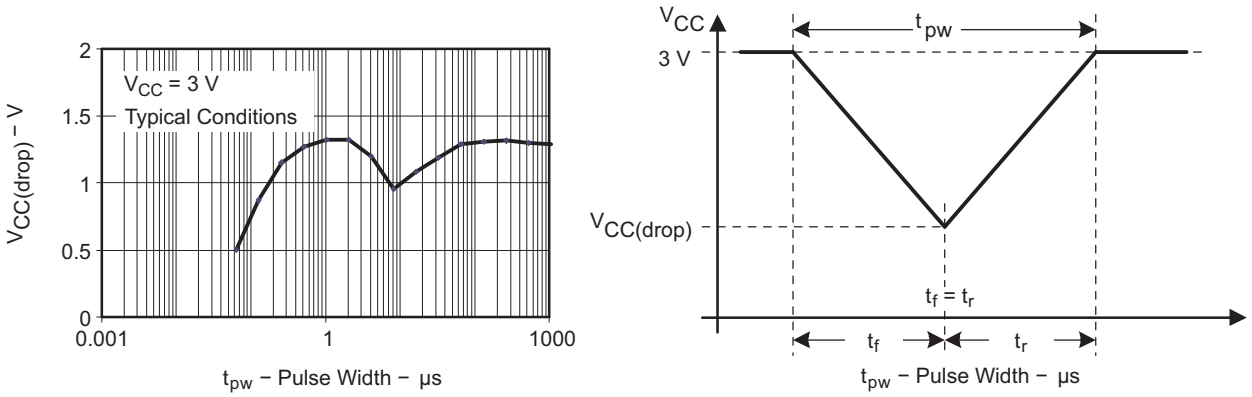


Figure 12. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	RSELx < 14		1.8		3.6	V
		RSELx = 14		2.2		3.6	V
		RSELx = 15		3		3.6	V
$f_{DCO(0,0)}$	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	3 V	0.06		0.14	MHz
$f_{DCO(0,3)}$	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	3 V		0.12		MHz
$f_{DCO(1,3)}$	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	3 V		0.15		MHz
$f_{DCO(2,3)}$	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	3 V		0.21		MHz
$f_{DCO(3,3)}$	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	3 V		0.3		MHz
$f_{DCO(4,3)}$	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	3 V		0.41		MHz
$f_{DCO(5,3)}$	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	3 V		0.58		MHz
$f_{DCO(6,3)}$	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	3 V		0.8		MHz
$f_{DCO(7,3)}$	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	3 V	0.8		1.5	MHz
$f_{DCO(8,3)}$	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	3 V		1.6		MHz
$f_{DCO(9,3)}$	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	3 V		2.3		MHz
$f_{DCO(10,3)}$	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	3 V		3.4		MHz
$f_{DCO(11,3)}$	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	3 V		4.25		MHz
$f_{DCO(12,3)}$	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	3 V	4.3		7.3	MHz
$f_{DCO(13,3)}$	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	3 V		7.8		MHz
$f_{DCO(14,3)}$	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	3 V	8.6		13.9	MHz
$f_{DCO(15,3)}$	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	3 V		15.25		MHz
$f_{DCO(15,7)}$	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	3 V		21		MHz
S_{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)}/f_{DCO(RSEL,DCO)}$	3 V		1.35		ratio
S_{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$	3 V		1.08		ratio
	Duty cycle	Measured at SMCLK output	3 V		50		%

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Calibrated DCO Frequencies - Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance over temperature(1)	BCSCTL1= CALBC1_1MHz, DCOCTL = CALDCO_1MHz, calibrated at 30°C and 3 V	0°C to 85°C -40°C to 105°C	3 V	-3	±0.5	+3	%
1-MHz tolerance over V_{CC}	BCSCTL1= CALBC1_1MHz, DCOCTL = CALDCO_1MHz, calibrated at 30°C and 3 V	30°C	1.8 V to 3.6 V	-3	±2	+3	%
1-MHz tolerance overall	BCSCTL1= CALBC1_1MHz, DCOCTL = CALDCO_1MHz, calibrated at 30°C and 3 V	-40°C to 85°C -40°C to 105°C	1.8 V to 3.6 V	-6	±3	+6	%

(1) This is the frequency change from the measured frequency at 30°C over temperature.

Wake-Up From Lower-Power Modes (LPM3/4) Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{DCO,LPM3/4}$	DCO clock wake-up time from LPM3/4(1)	BCSCTL1= CALBC1_1MHz, DCOCTL = CALDCO_1MHz	3 V		1.5		µs
$t_{CPU,LPM3/4}$	CPU wake-up time from LPM3/4(2)				$1/f_{MCLK}$ + $t_{Clock,LPM3/4}$		

(1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (e.g., port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
(2) Parameter applicable only if DCOCLK is used for MCLK.

Typical Characteristics - DCO Clock Wake-Up Time From LPM3/4

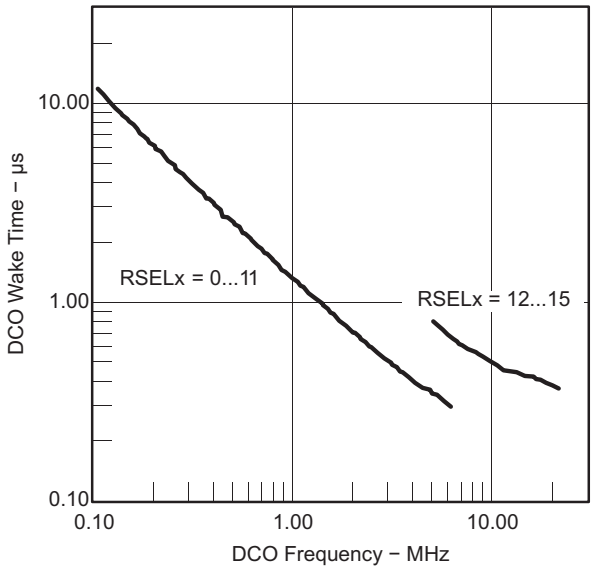


Figure 13. DCO Wake-Up Time From LPM3 vs DCO Frequency

Crystal Oscillator, XT1, Low-Frequency Mode(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V		32768		Hz
$f_{LFXT1,LF,logic}$	LFXT1 oscillator logic level square wave input frequency, LF mode	XTS = 0, XCAPx = 0, LFXT1Sx = 3	1.8 V to 3.6 V	10000	32768	50000	Hz
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			200		
$C_{L,eff}$	Integrated effective load capacitance, LF mode(2)	XTS = 0, XCAPx = 0			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			11		
	Duty cycle, LF mode	XTS = 0, Measured at P2.0/ACLK, $f_{LFXT1,LF}$ = 32768 Hz	2.2 V	30	50	70	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode(3)	XTS = 0, XCAPx = 0, LFXT1Sx = 3(4)	2.2 V	10		10000	Hz

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
(a) Keep the trace between the device and the crystal as short as possible.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
(d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
(f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
(g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(3) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

(4) Measured with logic-level input frequency but also applies to operation with crystals.

Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		T_A	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	-40°C to 85°C	3 V	4	12	20	kHz
		105°C				22	
df_{VLO}/d_T	VLO frequency temperature drift	I: -40°C to 85°C T: -40°C to 105°C	3 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	25°C	1.8 V to 3.6 V		4		%/V

Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK, ACLK External: TACLK, INCLK Duty cycle = 50% ± 10%			f_{SYSTEM}		MHz
$t_{TA,cap}$	Timer_A capture timing	TA0, TA1	3 V	20			ns

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Comparator_A+ (MSP430G2x11 only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(DD)}$		CAON = 1, CARSEL = 0, CAREF = 0	3 V		45		µA
$I_{(Refladder/RefDiode)}$		CAON = 1, CARSEL = 0, CAREF = 1/2/3, No load at CA0 and CA1	3 V		45		µA
$V_{(IC)}$	Common-mode input voltage	CAON = 1	3 V	0		V_{CC}-1	V
$V_{(Ref025)}$	$\frac{\text{Voltage @ 0.25 } V_{CC} \text{ node}}{V_{CC}}$	PCA0 = 1, CARSEL = 1, CAREF = 1, No load at CA0 and CA1	3 V		0.24		
$V_{(Ref050)}$	$\frac{\text{Voltage @ 0.5 } V_{CC} \text{ node}}{V_{CC}}$	PCA0 = 1, CARSEL = 1, CAREF = 2, No load at CA0 and CA1	3 V		0.48		
$V_{(RefVT)}$	See Figure 14 and Figure 15	PCA0 = 1, CARSEL = 1, CAREF = 3, No load at CA0 and CA1, TA = 85°C	3 V		490		mV
$V_{(offset)}$	Offset voltage(1)		3 V		±10		mV
V_{hys}	Input hysteresis	CAON = 1	3 V		0.7		mV
$t_{(response)}$	Response time (low-high and high-low)	T_A = 25°C, Overdrive 10 mV, Without filter: CAF = 0	3 V		120		ns
		T_A = 25°C, Overdrive 10 mV, With filter: CAF = 1			1.5		µs

(1) The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A+ inputs on successive measurements. The two successive measurements are then summed together.

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Typical Characteristics - Comparator_A+

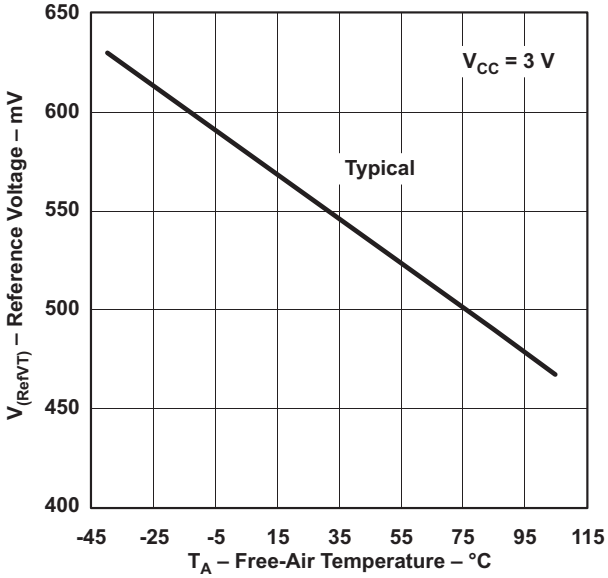


Figure 14. $V_{(RefVT)}$ vs Temperature, V_{CC} = 3 V

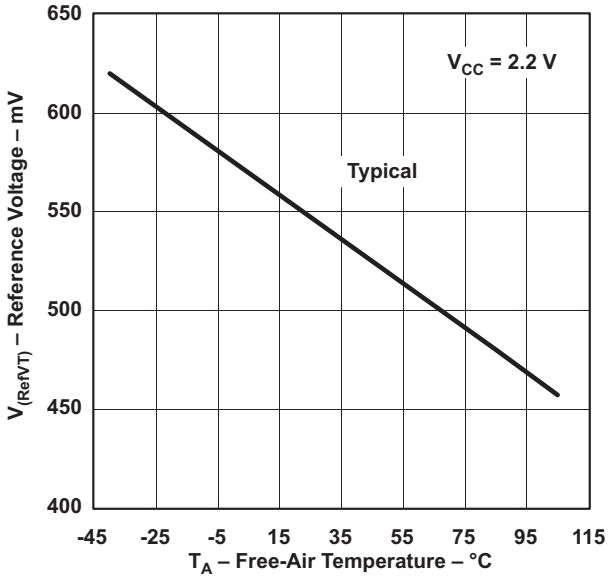


Figure 15. $V_{(RefVT)}$ vs Temperature, V_{CC} = 2.2 V

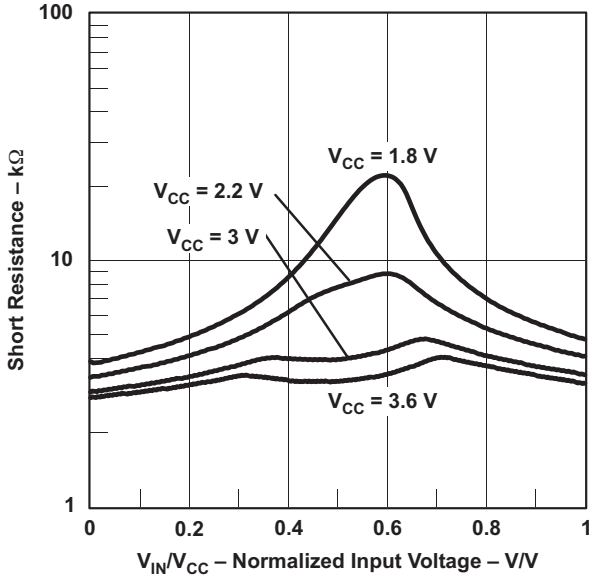


Figure 16. Short Resistance vs V_{IN}/V_{CC}

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Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage			2.2		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		2.2 V/3.6 V		1	5	mA
I_{ERASE}	Supply current from V_{CC} during erase		2.2 V/3.6 V		1	7	mA
t_{CPT}	Cumulative program time (1)		2.2 V/3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time		2.2 V/3.6 V	20			ms
	Program/erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		15			years
t_{Word}	Word or byte program time	(2)			30		t_{FTG}
$t_{Block, 0}$	Block program time for first byte or word	(2)			25		t_{FTG}
$t_{Block, 1-63}$	Block program time for each additional byte or word	(2)			18		t_{FTG}
$t_{Block, End}$	Block program end-sequence wait time	(2)			6		t_{FTG}
$t_{Mass\ Erase}$	Mass erase time	(2)			10593		t_{FTG}
$t_{Seg\ Erase}$	Segment erase time	(2)			4819		t_{FTG}

(1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
(2) These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).

RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(RAMh)}$	RAM retention supply voltage (1)	CPU halted	1.6		V

(1) This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

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JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency		2.2 V/3 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse length		2.2 V/3 V	0.025		15	µs
$t_{SBW,En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge(1))		2.2 V/3 V			1	µs
$t_{SBW,Ret}$	Spy-Bi-Wire return to normal operation time		2.2 V/3 V	15		100	µs
f_{TCK}	TCK input frequency(2)		2.2 V	0		5	MHz
			3 V	0		10	MHz
$R_{Internal}$	Internal pulldown resistance on TEST		2.2 V/3 V	25	60	90	kΩ

(1) Tools accessing the Spy-Bi-Wire interface need to wait for the maximum $t_{SBW,En}$ time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

JTAG Fuse(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C	2.5		V
V_{FB}	Voltage level on TEST for fuse blow		6	7	V
I_{FB}	Supply current into TEST during fuse blow			100	mA
t_{FB}	Time to blow fuse			1	ms

(1) Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.

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APPLICATION INFORMATION

Port P1 Pin Schematic: P1.0 to P1.3, Input/Output With Schmitt Trigger - MSP430G2x01

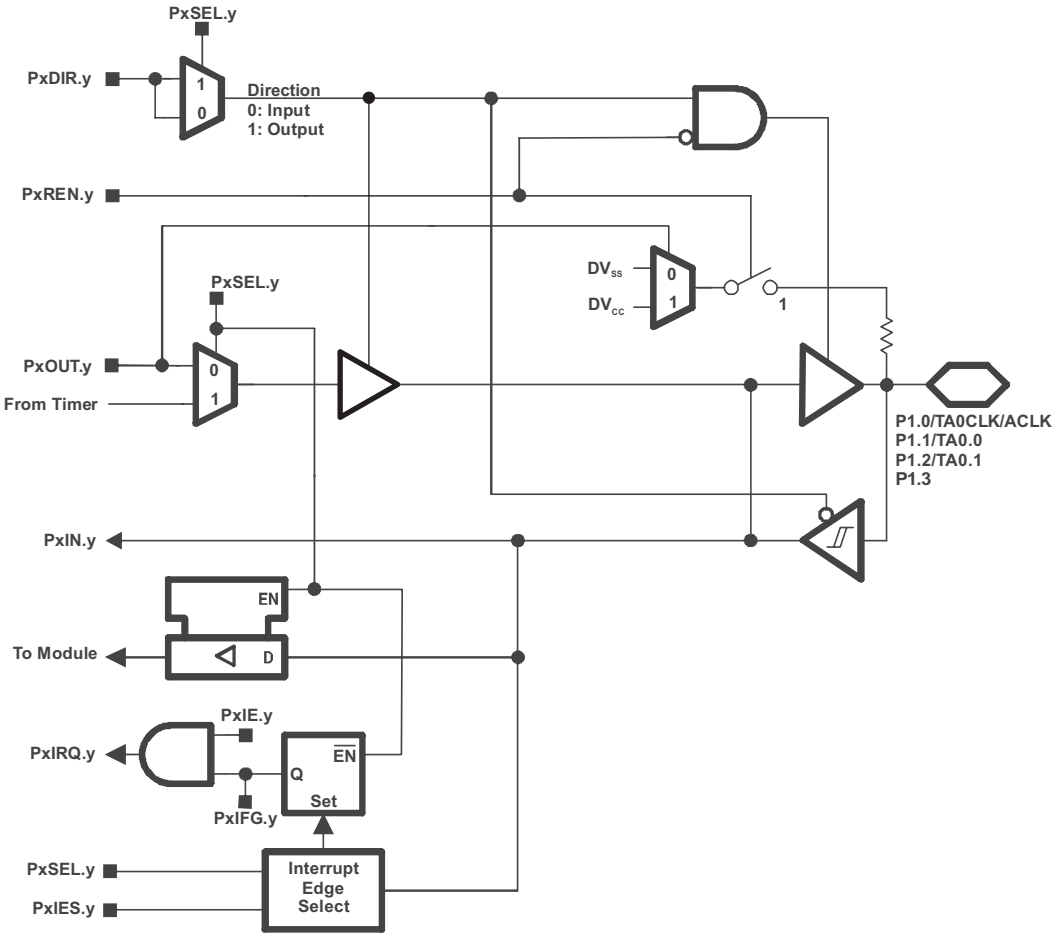


Table 15. Port P1 (P1.0 to P1.3) Pin Functions - MSP430G2x01

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/	0	P1.x (I/O)	I: 0; O: 1	0
TA0CLK/		TA0CLK	0	1
ACLK		ACLK	1	1
P1.1/	1	P1.x (I/O)	I: 0; O: 1	0
TA0.0		TA0.CCI0A	0	1
		TA0.0	1	1
P1.2/	2	P1.x (I/O)	I: 0; O: 1	0
TA0.1		TA0.CCI1A	0	1
		TA0.1	1	1
P1.3	3	P1.x (I/O)	I: 0; O: 1	0

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Port P1 Pin Schematic: P1.4 to P1.7, Input/Output With Schmitt Trigger - MSP430G2x01

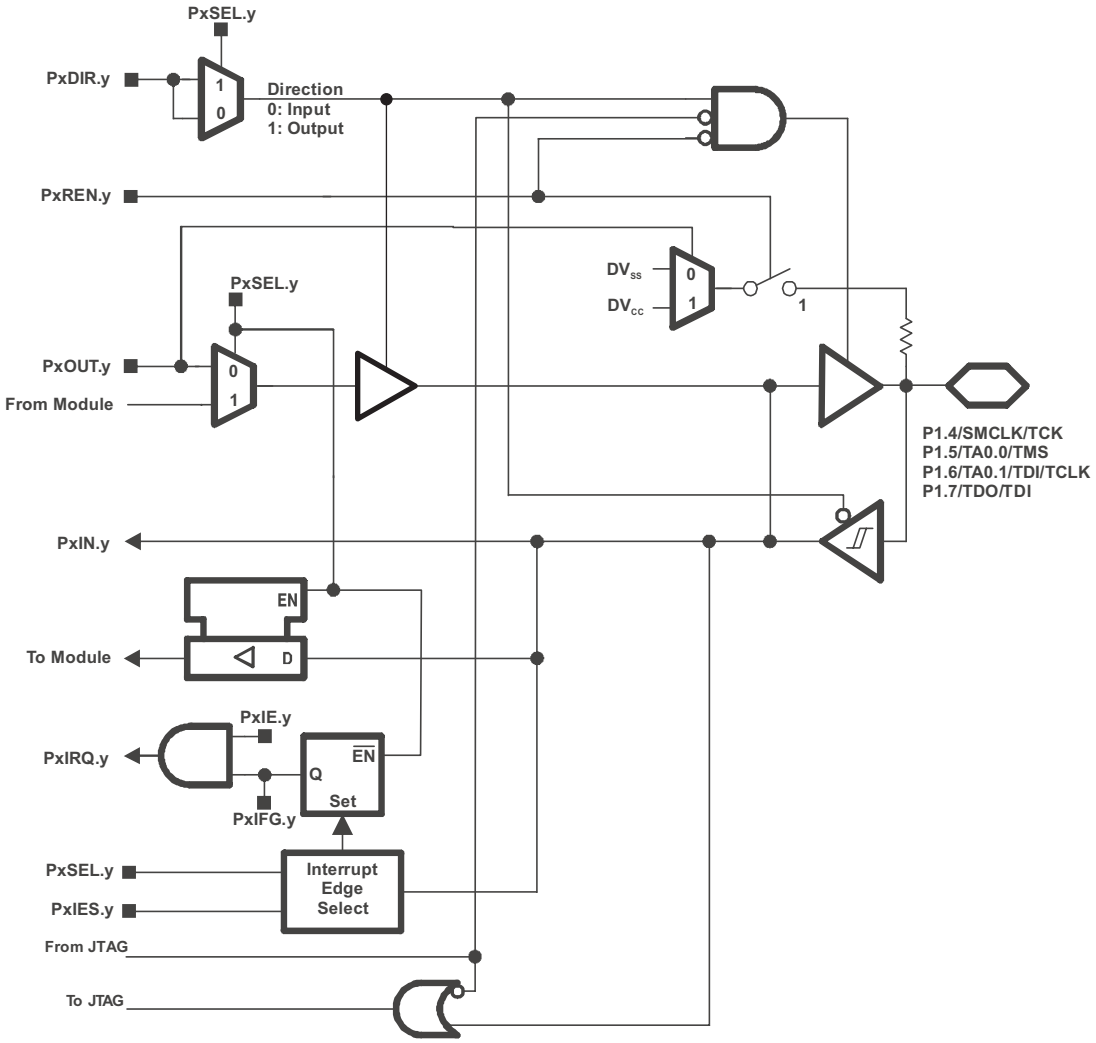


Table 16. Port P1 (P1.4 to P1.7) Pin Functions - MSP430G2x01

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]		
			P1DIR.x	P1SEL.x	JTAG Mode
P1.4/	4	P1.x (I/O)	I: 0; O: 1	0	0
SMCLK/		SMCLK	1	1	0
TCK		TCK	X	X	1
P1.5/	5	P1.x (I/O)	I: 0; O: 1	0	0
TA0.0/		TA0.0	1	1	0
TMS		TMS	X	X	1
P1.6/	6	P1.x (I/O)	I: 0; O: 1	0	0
TA0.1/		TA0.1	1	1	0
TDI/TCLK		TDI/TCLK	X	X	1
P1.7/	7	P1.x (I/O)	I: 0; O: 1	0	0
TDO/TDI		TDO/TDI	X	X	1

(1) X = Don't care

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Port P1 Pin Schematic: P1.0 to P1.3, Input/Output With Schmitt Trigger - MSP430G2x11

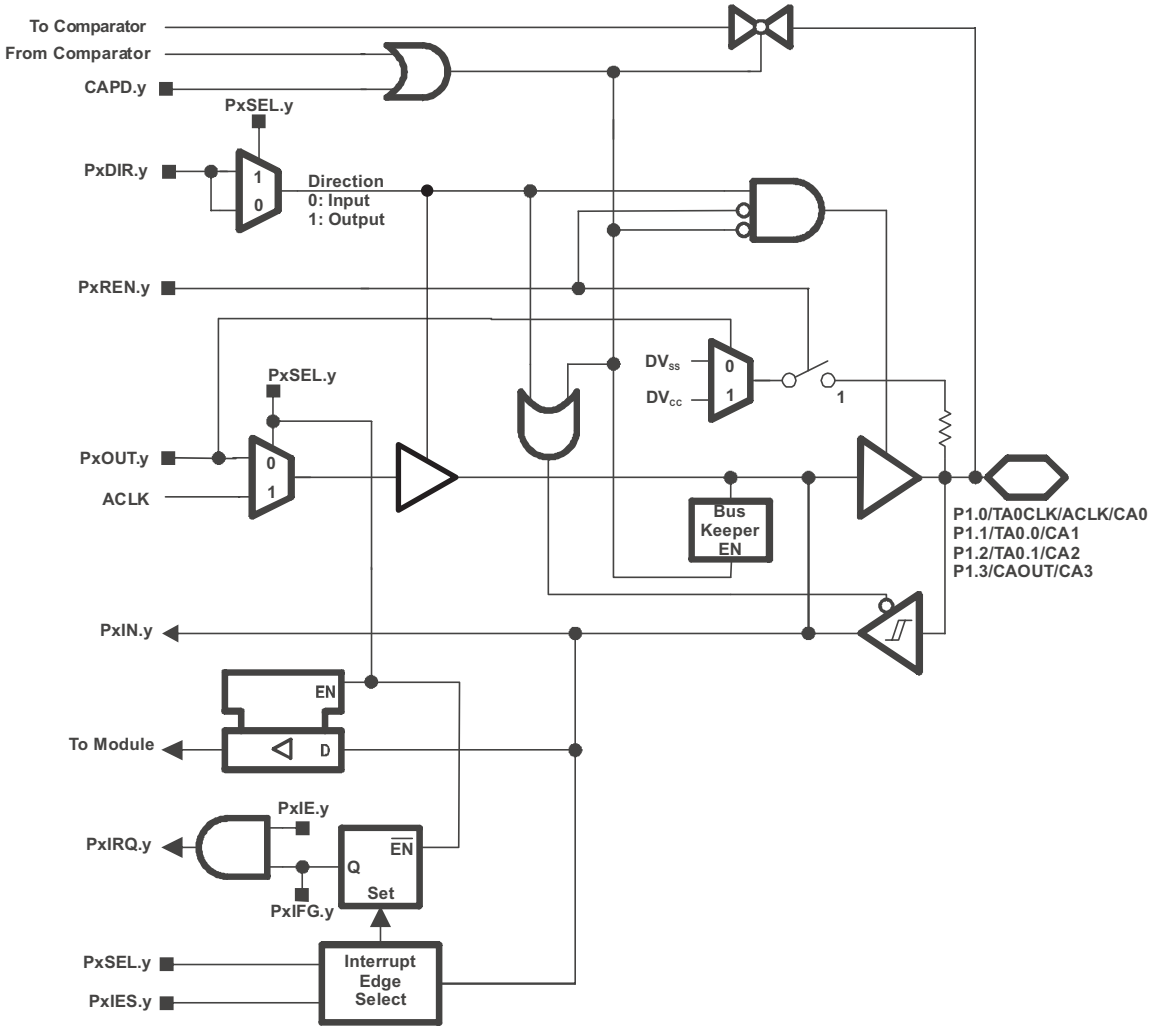


Table 17. Port P1 (P1.0 to P1.3) Pin Functions - MSP430G2x11

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNALS(1)		
			P1DIR.x	P1SEL.x	CAPD.y
P1.0/	0	P1.x (I/O)	I: 0; O: 1	0	0
TA0CLK/		TA0.TACLK	0	1	0
ACLK/		ACLK	1	1	0
CA0		CA0	X	X	1 (y = 0)
P1.1/	1	P1.x (I/O)	I: 0; O: 1	0	0
TA0.0/		TA0.0	1	1	0
		TA0.CCI0A	0	1	0
CA1		CA1	X	X	1 (y = 1)
P1.2/	2	P1.x (I/O)	I: 0; O: 1	0	0
TA0.1/		TA0.1	1	1	0
		TA0.CCI1A	0	1	0
CA2		CA2	X	X	1 (y = 2)
P1.3/	3	P1.x (I/O)	I: 0; O: 1	0	0
CAOUT/		CAOUT	1	1	0
CA3		CA3	X	X	1 (y = 3)

(1) X = Don't care

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Port P1 Pin Schematic: P1.4 to P1.7, Input/Output With Schmitt Trigger - MSP430G2x11

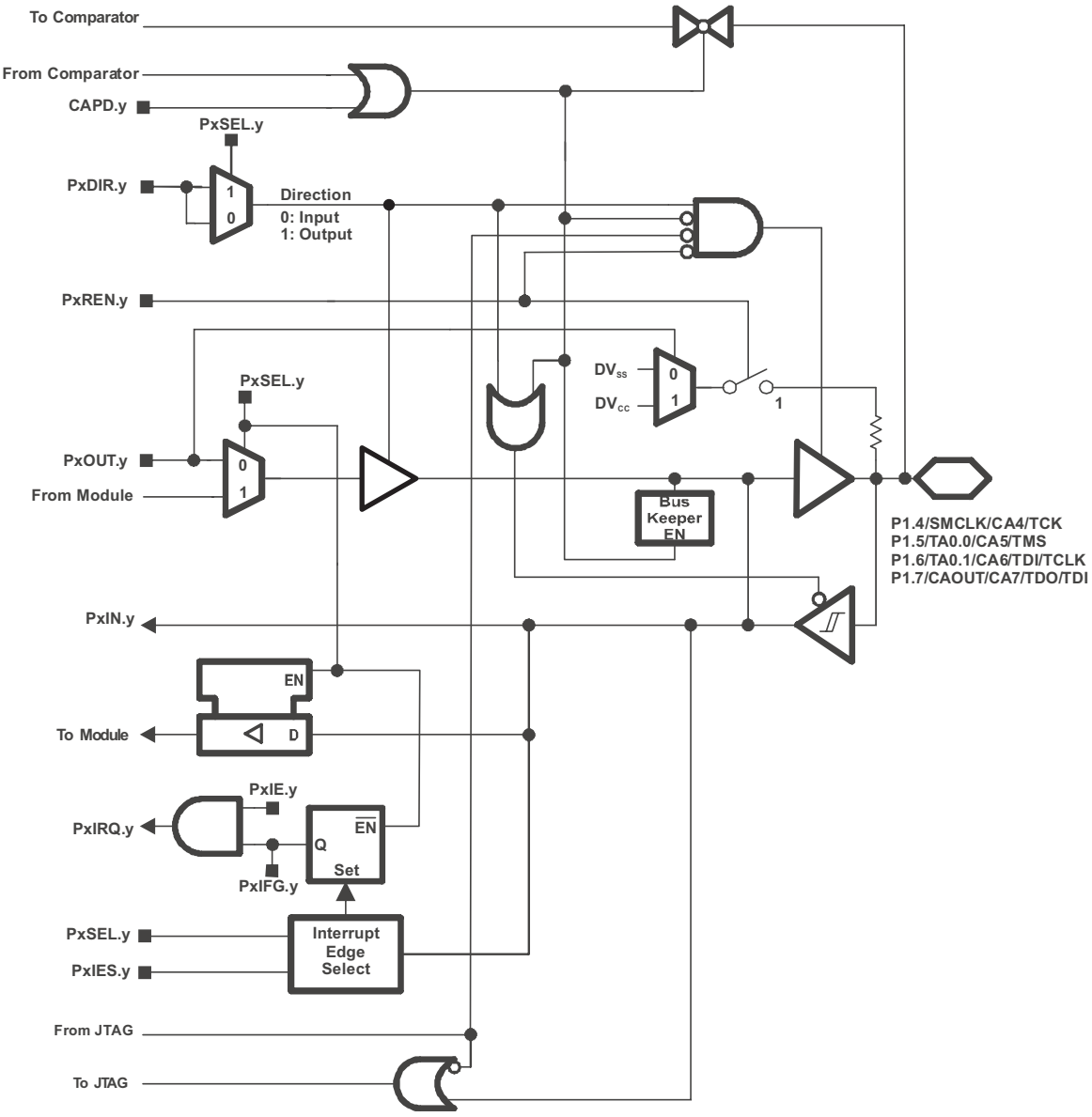


Table 18. Port P1 (P1.4 to P1.7) Pin Functions - MSP430G2x11

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]			
			P1DIR.x	P1SEL.x	JTAG Mode	CAPD.y
P1.4/	4	P1.x (I/O)	I: 0; O: 1	0	0	0
SMCLK/		SMCLK	1	1	0	0
CA4/		CA4	X	X	0	1 (y = 4)
TCK		TCK	X	X	1	0
P1.5/	5	P1.x (I/O)	I: 0; O: 1	0	0	0
TA0.0/		TA0.0	1	1	0	0
CA5/		CA5	X	X	0	1 (y = 5)
TMS		TMS	X	X	1	0
P1.6/	6	P1.x (I/O)	I: 0; O: 1	0	0	0
TA0.1/		TA0.1	1	1	0	0
CA6/		CA6	X	X	0	1 (y = 6)
TDI/TCLK		TDI/TCLK	X	X	1	0
P1.7/	7	P1.x (I/O)	I: 0; O: 1	0	0	0
CAOUT/		CAOUT	1	1	0	0
CA7/		CA7	X	X	0	1 (y = 7)
TDO/TDI		TDO/TDI	X	X	1	0

(1) X = Don't care

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Port P2 Pin Schematic: P2.6, Input/Output With Schmitt Trigger - MSP430G2x01 and MSP430G2x11

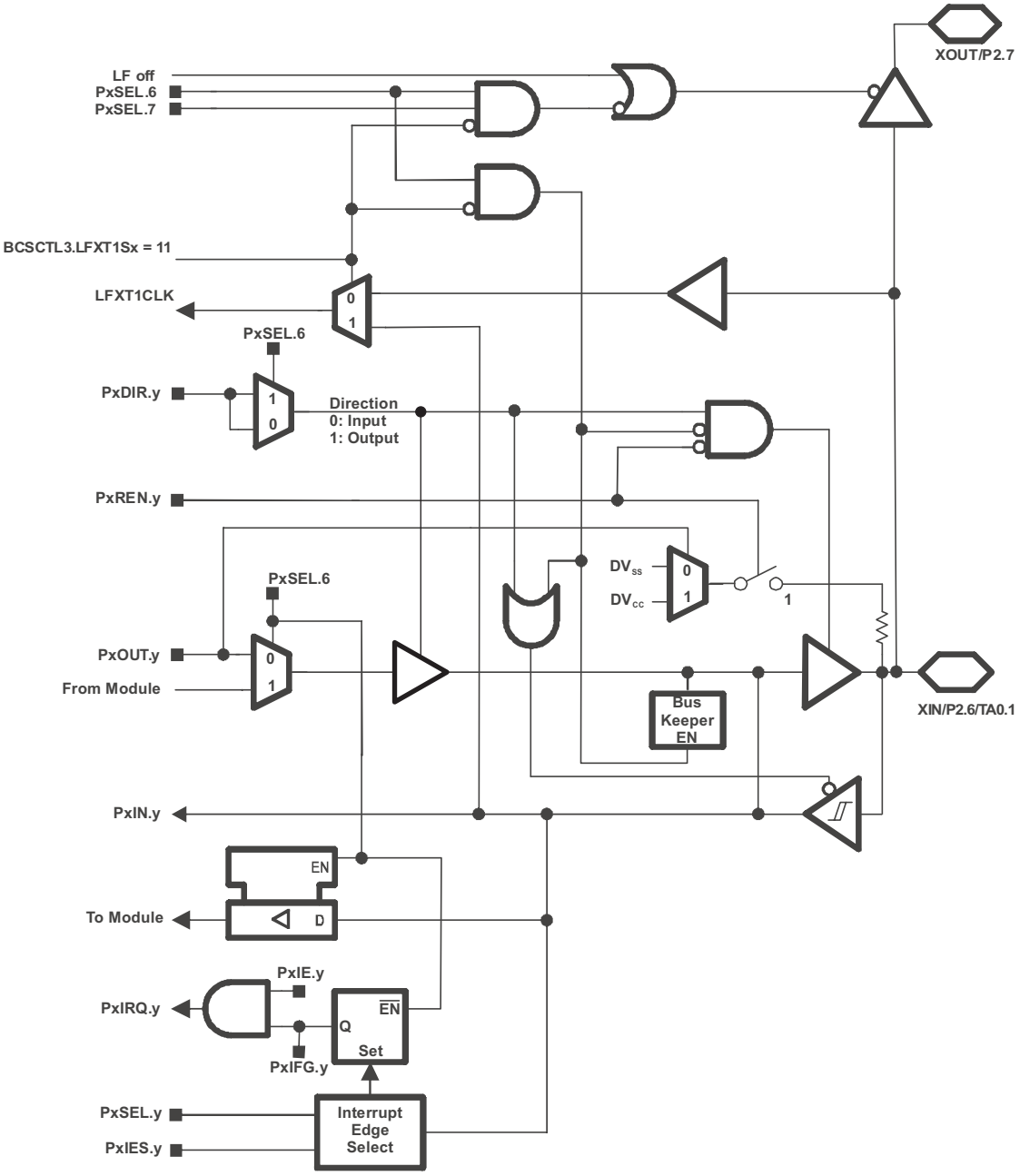


Table 19. Port P2 (P2.6) Pin Functions - MSP430G2x01 and MSP430G2x11

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]		
			P2DIR.x	P2SEL.6	P2SEL.7
XIN	6	XIN	0	1	1
P2.6		P2.x (I/O)	I: 0; O: 1	0	X
TA0.1		Timer0_A2.TA1	1	1	X

(1) X = Don't care

Port P2 Pin Schematic: P2.7, Input/Output With Schmitt Trigger - MSP430G2x01 and MSP430G2x11

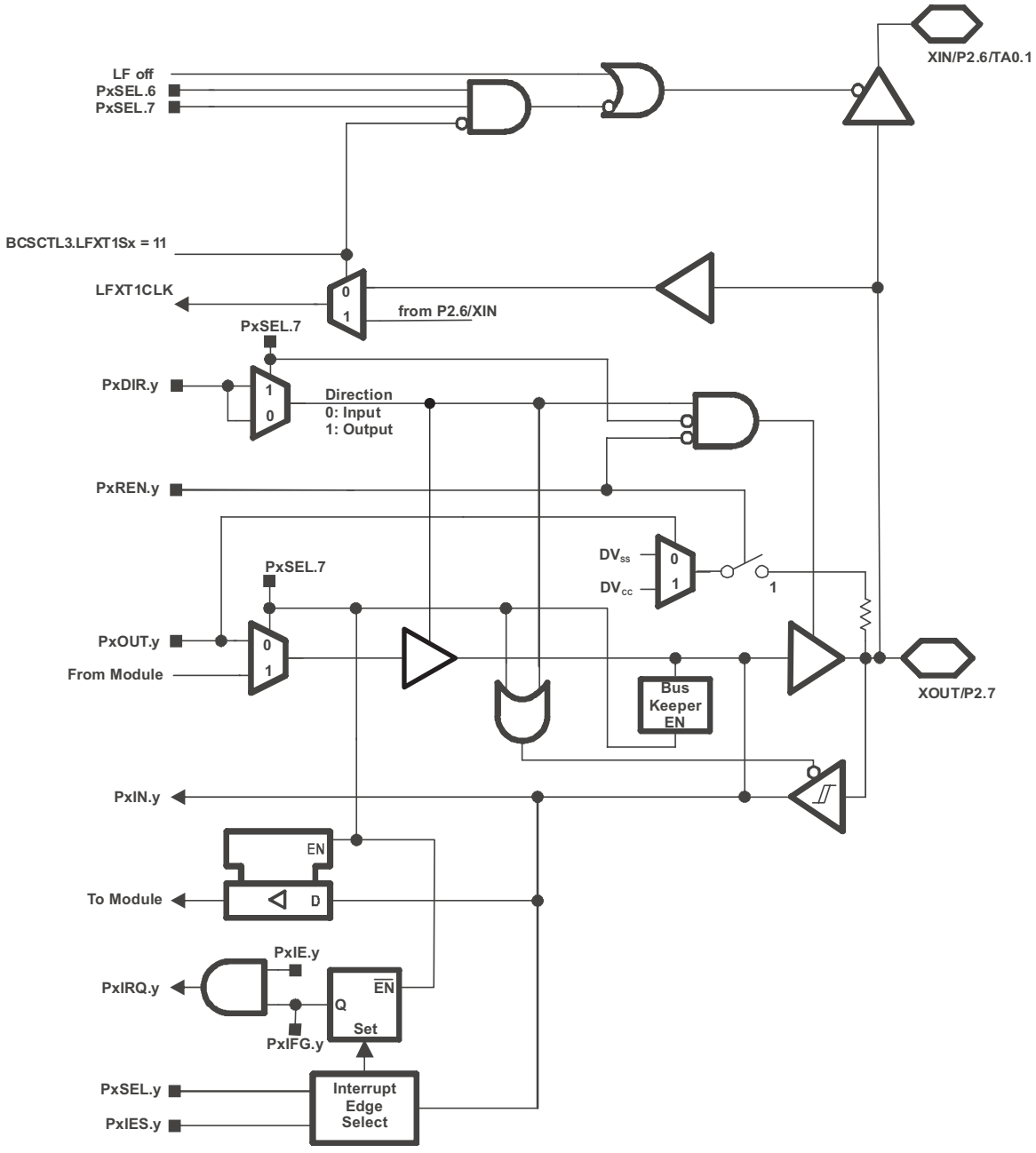


Table 20. Port P2 (P2.7) Pin Functions - MSP430G2x01 and MSP430G2x11

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS / SIGNALS		
			P2DIR.x	P2SEL.6	P2SEL.7
XOUT	7	XOUT	1	1	1
P2.7		P2.x (I/O)	I: 0; O: 1	0	0

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REVISION HISTORY

REVISION	DESCRIPTION
SLAS775	Product Preview release
SLAS775A	Production Data release
SLAS775B	Changed port schematics (added buffer after PxOUT.y mux) in APPLICATION INFORMATION

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
MSP430G2001IPW4Q1	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430G2001IRSAQ1	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
MSP430G2101IPW4Q1	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430G2101IRSAQ1	ACTIVE	QFN	RSA	16	250	TBD	Call TI	Call TI	
MSP430G2111IPW4Q1	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430G2111IRSAQ1	ACTIVE	QFN	RSA	16	250	TBD	Call TI	Call TI	
MSP430G2201IPW4Q1	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430G2201IRSAQ1	ACTIVE	QFN	RSA	16	250	TBD	Call TI	Call TI	
MSP430G2201TRSAQ1	PREVIEW	QFN	RSA	16	250	TBD	Call TI	Call TI	
MSP430G2211IPW4Q1	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430G2211IRSAQ1	ACTIVE	QFN	RSA	16	250	TBD	Call TI	Call TI	
MSP430G2211TPW4Q1	PREVIEW	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430G2211TRSAQ1	PREVIEW	QFN	RSA	16	250	TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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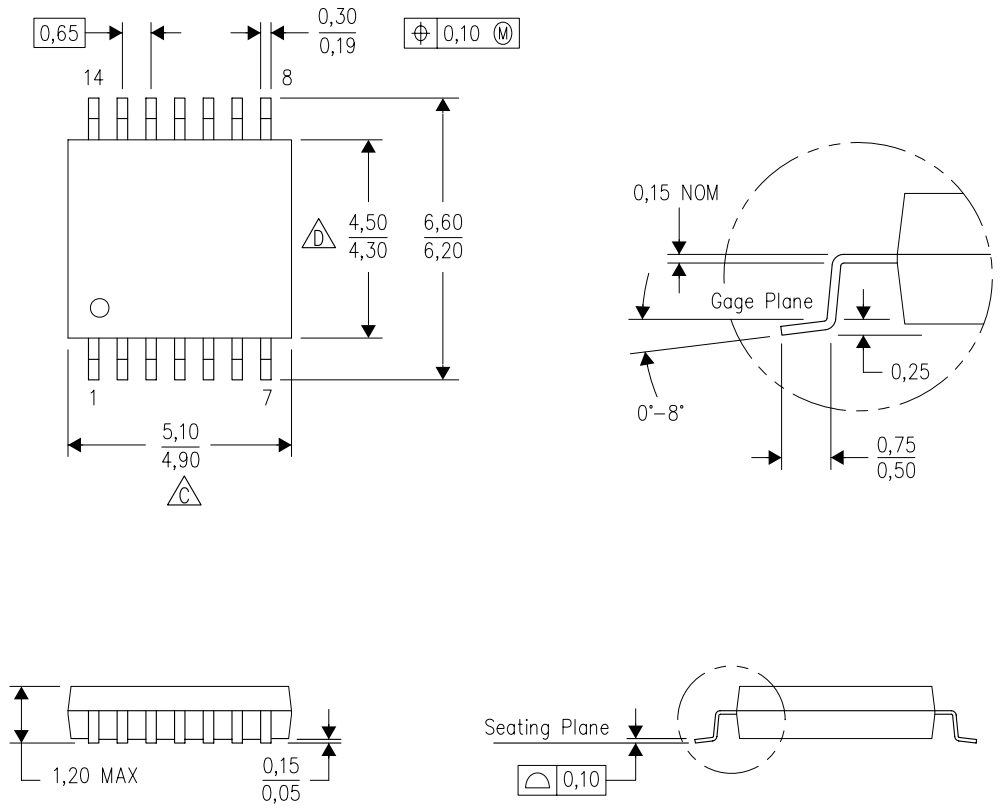
OTHER QUALIFIED VERSIONS OF MSP430G2001-Q1, MSP430G2101-Q1, MSP430G2111-Q1, MSP430G2201-Q1, MSP430G2211-Q1 :

- Catalog: MSP430G2001, MSP430G2101, MSP430G2111, MSP430G2201, MSP430G2211

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

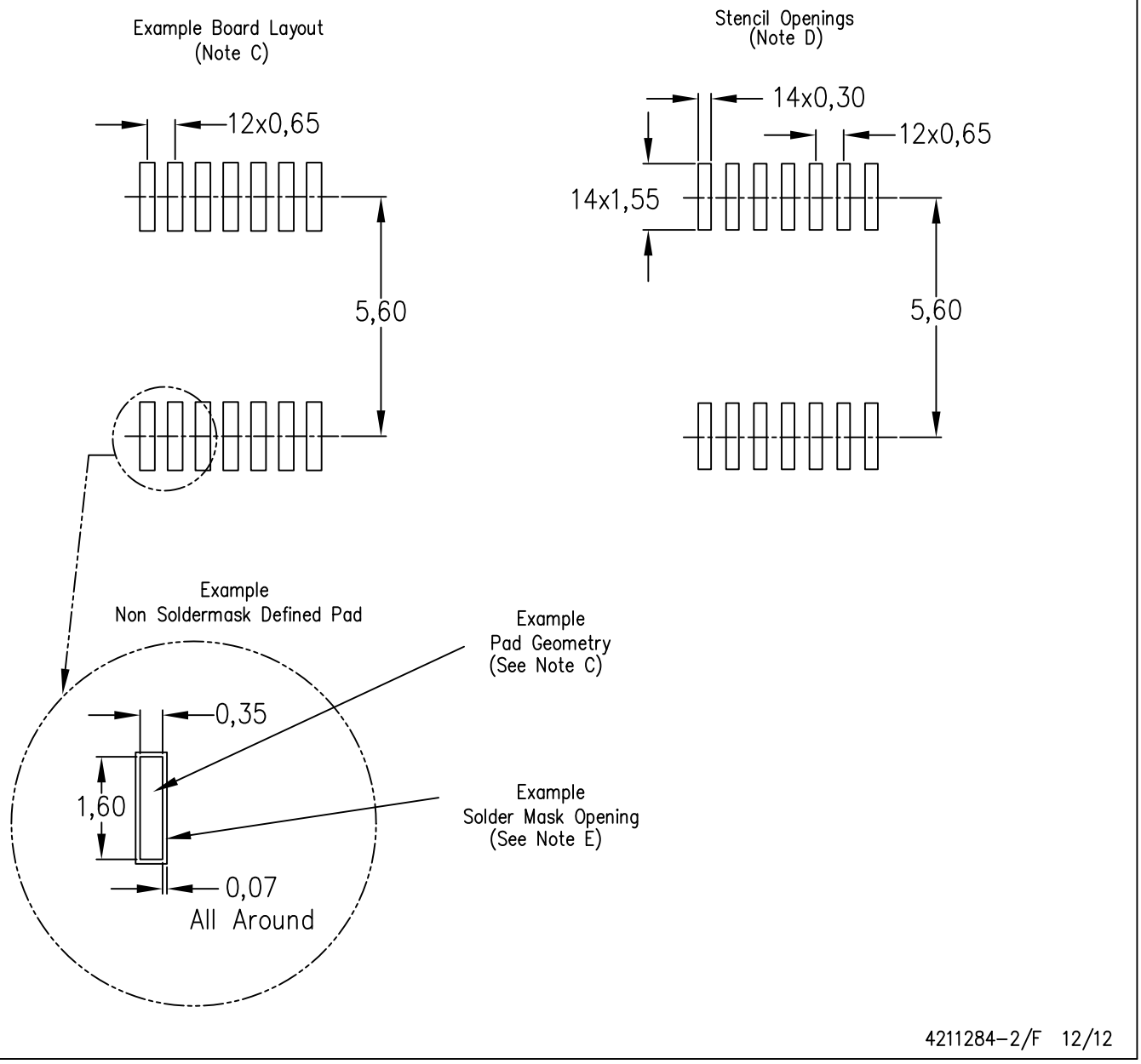
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

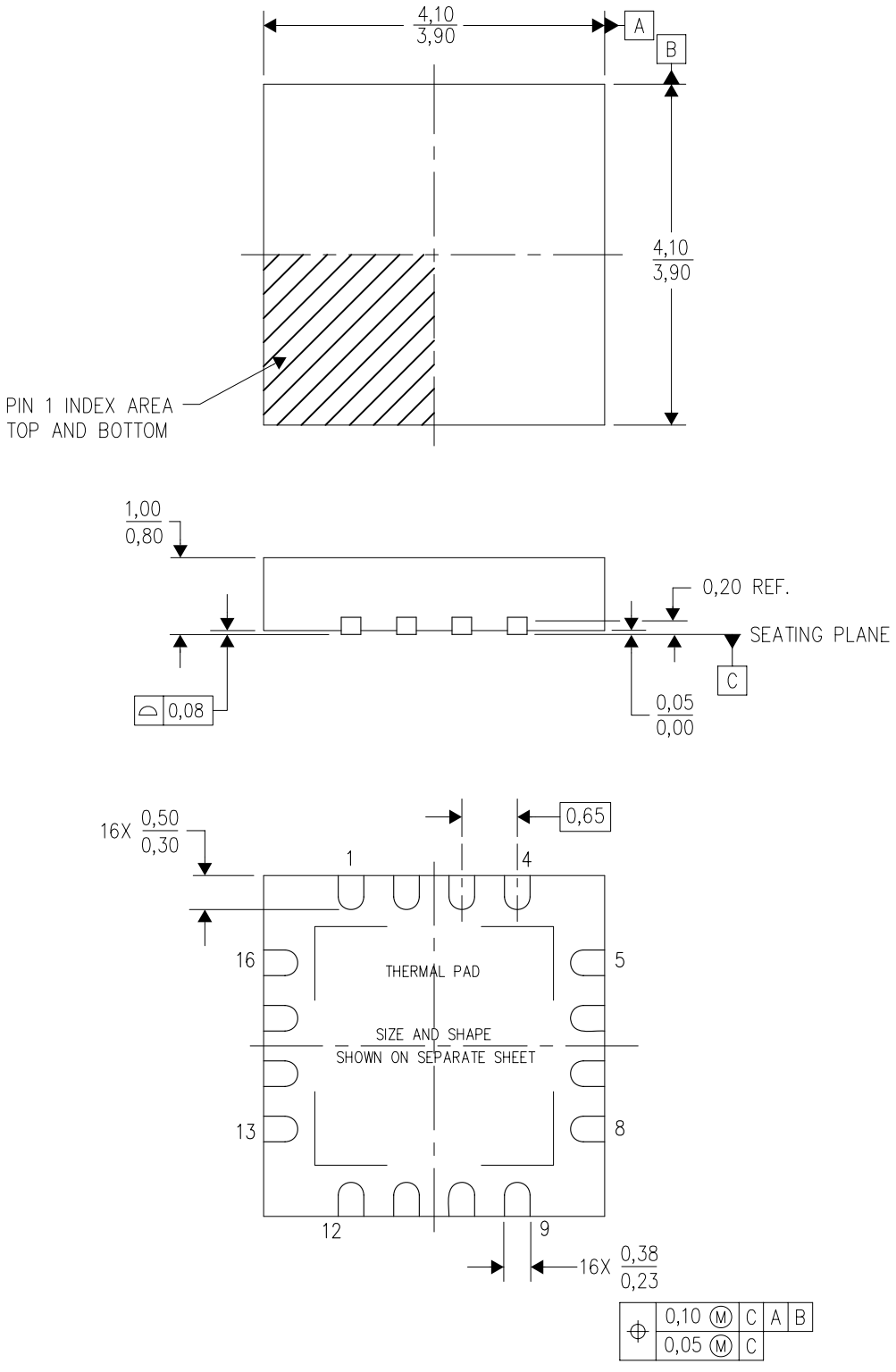
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

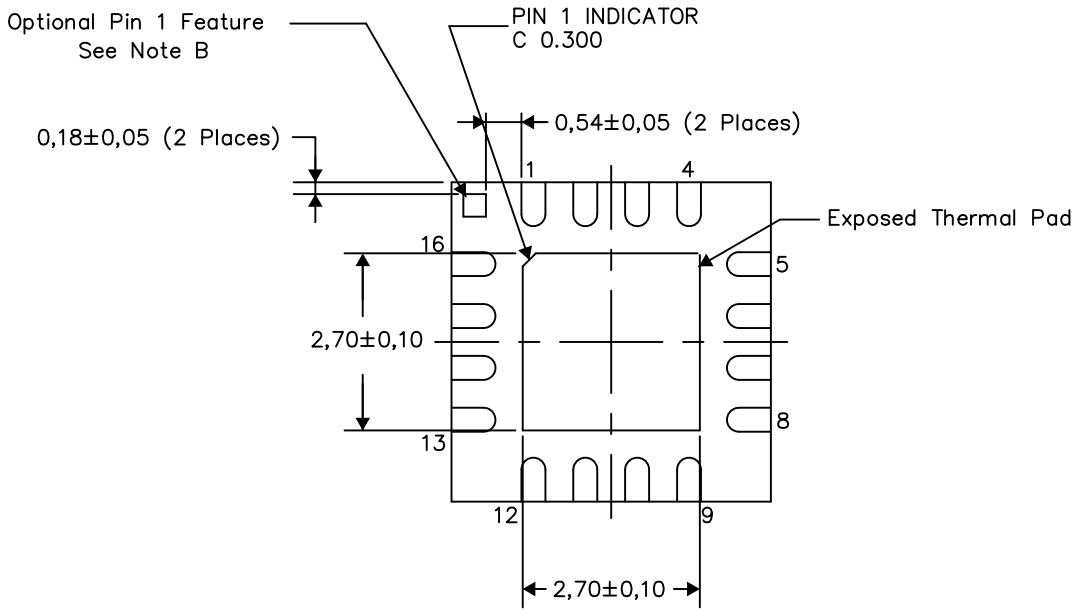
RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

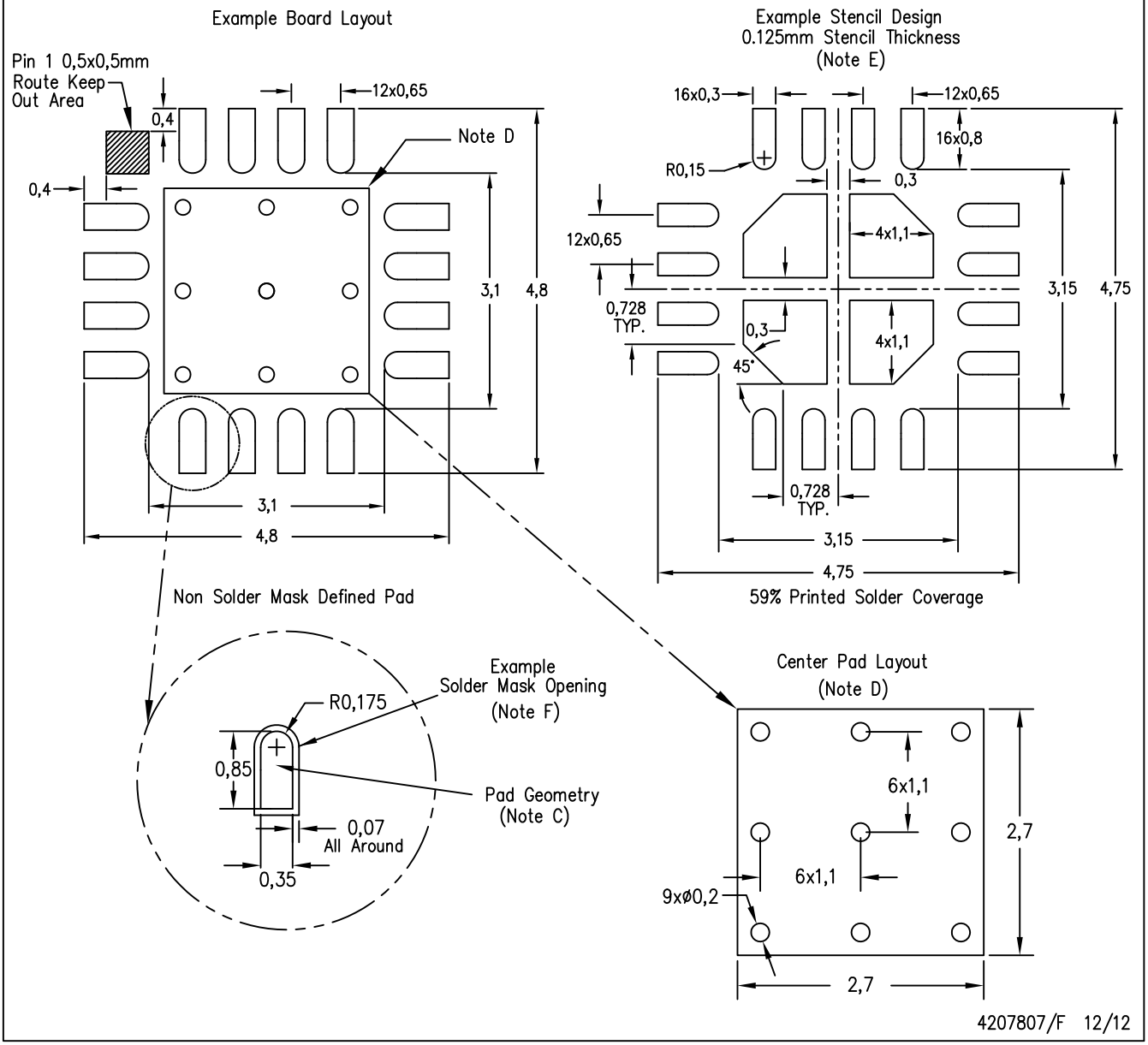
4206364/M 12/12

NOTES:

A. All linear dimensions are in millimeters

B. The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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