

MSP432P401R, MSP432P401M Mixed-Signal Microcontrollers

1 Device Overview

1.1 Features

- Core
 - ARM® 32-Bit Cortex® M4F CPU With Floating-Point Unit and Memory Protection Unit
 - Frequency up to 48 MHz
 - UI PBench™ Benchmark
 - 192.3 UI PBench™-CP
 - Performance Benchmark
 - 3.41 CoreMark/MHz
 - 1.22 DMIPS/MHz (Dhrystone 2.1)
- Memories
 - Up to 256KB of Flash Main Memory (Organized Into Two Banks Enabling Simultaneous Read/Execute During Erase)
 - 16KB of Flash Information Memory (Used for BSL, TLV, and Flash Mailbox)
 - Up to 64KB of SRAM (Including 8KB of Backup Memory)
 - 32KB of ROM With MSP432™ Peripheral Driver Libraries
- Operating Characteristics
 - Wide Supply Voltage Range: 1.82 V to 3.7 V
 - Temperature Range (Ambient): -40°C to 85°C
- Ultra-Low-Power Operating Modes
 - Active: 80 µA/MHz
 - Low-Frequency Active: 83 µA at 128 kHz (Typical)
 - LPM3 (With RTC): 600 nA (Typical)
 - LPM3.5 (With RTC): 630 nA (Typical)
 - LPM4: 500 nA (Typical)
 - LPM4.5: 25 nA (Typical)
- Flexible Cloning Features
 - Tunable Internal DCO (up to 48 MHz)
 - 32.768-kHz Low-Frequency Crystal Support (LFXT)
 - High-Frequency Crystal Support (HFXT) up to 48 MHz
 - Low-Frequency Internal Reference Oscillator (RLFO)
 - Very Low-Power Low-Frequency Internal Oscillator (VLO)
 - Module Oscillator (MODOSC)
 - System Oscillator (SYSOSC)
- Code Security Features
 - JTAG and SWD Lock
 - IP Protection (up to Four Secure Flash Zones, Each With Configurable Start Address and Size)
- Enhanced System Features
 - Programmable Supervision and Monitoring of Supply Voltage
 - Multiple-Class Resets for Better Control of Application and Debug
 - 8-Channel DMA
 - RTC With Calendar and Alarm Functions
- Timing and Control
 - Up to Four 16-Bit Timers, Each With up to Five Capture, Compare, PWM Capability
 - Two 32-Bit Timers, Each With Interrupt Generation Capability
- Serial Communication
 - Up to Four eUSCIA Modules
 - UART With Automatic Baud-Rate Detection
 - IrDA Encode and Decode
 - SPI (up to 16 Mbp/s)
 - Up to Four eUSCLB Modules
 - I²C (With Multiple-Slave Addressing)
 - SPI (up to 16 Mbp/s)
- Flexible I/O Features
 - Ultra-Low-Leakage I/Os (120 nA Maximum)
 - All I/Os With Capacitive-Touch Capability
 - Up to 48 I/Os With Interrupt and Wake-up Capability
 - Up to 24 I/Os With Port Mapping Capability
 - Eight I/Os With Glitch Filtering Capability
- Advanced Low-Power Analog Features
 - 14-Bit 1-MSPS SAR ADC With Differential and Single-Ended Inputs
 - Internal Voltage Reference With 10-ppm/°C Typical Stability
 - Two Analog Comparators
- Encryption and Data Integrity Accelerators
 - 128-, 192-, or 256-Bit AES Encryption and Decryption Accelerator
 - 32-Bit Hardware CRC Engine
- JTAG and Debug Support
 - Support for 4-Pin JTAG and 2-Pin SWD Debug Interfaces
 - Support for Serial Wire Traces
 - Support for Power Debug and Profiling of Applications



NOT RECOMMENDED FOR USE IN THE NEW OR HIGH-CRITICAL-APPLICATIONS, AUTOMOTIVE, AEROSPACE, OR MEDICAL-VERIFIED APPLICATIONS. INTO LOCAL PROPERTY REGULATIONS AND OTHER IMPORTANT DISCLOSURES. PRODUCTION DATA.

1.2 Applications

- Industrial and Automation
 - Home Automation
 - Smoke Detectors
 - Barcode Scanners
 - Access Panels
- Health and Fitness
 - Watches
 - Activity Monitors
 - Fitness Accessories
 - Blood Glucose Meters
- Metering
 - Electric Meters
 - Flow Meters
 - Communication Modules
- Consumer Electronics
 - Mobile Devices
 - Sensor Hubs

1.3 Description

The MSP432P401x microcontroller (MCU) family is TI's latest addition to its portfolio of efficient ultra-low-power mixed-signal MCUs. The MSP432P401x MCUs feature the ARM Cortex-M4 processor in a wide configuration of device options including a rich set of analog, timing, and communication peripherals, thereby catering to a large number of application scenarios where both efficient data processing and enhanced low-power operation are paramount.

Overall, the MSP432P401x is an ideal combination of the TI MSP430™ low-power DNA, advanced mixed-signal features, and the processing capabilities of the ARM 32-bit Cortex-M4 RISC engine. The devices ship with bundled peripheral driver libraries and are compatible with standard components of the ARM ecosystem.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE ⁽²⁾
MSP432P401R-REZ MS M432P401M12	LQFP (100)	14 mm × 14 mm
MSP432P401R-REZ01 MS M432P401M204	WFPA (50)	5 mm × 5 mm
MSP432P401R-REZ0C MS M432P401M300	VQFN (54)	5 mm × 5 mm

(1) For the most current part, package, and ordering information for all TI analog devices, see the Package Option Addendum in Section 9, or see the TI website.

(2) The sizes shown here are approximate. For the package dimensions with tolerances, see the Mechanical Data in Section 8.

1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the MSP432P401R and MSP432P401M devices.

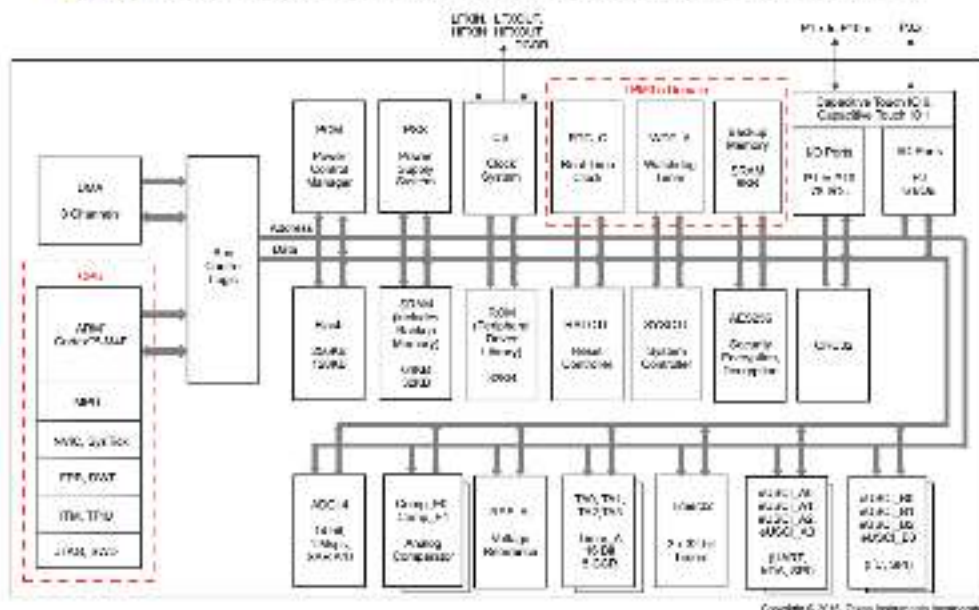


Figure 1-1. MSP432P401R, MSP432P401M Functional Block Diagram

The CPU and all of the peripherals in the device interact with each other through a common AHB matrix. In some cases, there are bridges between the AHB ports and the peripherals. These bridges are transparent to the application from a memory map perspective and, therefore, are not shown in the block diagram.

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2 Revision History

NOTE: Page numbers for previous editions may differ from page numbers in the current version.

Changes from June 20, 2016 to July 25, 2016	Page
• Corrected C6.7 signal type (changed IO to I) in Table 4-1 , Pin Attributes	12
• Corrected C6.7 signal type (changed IO to I) in Table 4-2 , Signal Descriptions	18
• Added "HSMCLK, and SMDCLK" to note (3) of Section 5-12 , Current Consumption in Low-Frequency Active Modes – Chrysalis 2.1 Program	32
• Added "HSMCLK, and SMDCLK" to note (3) of Section 5-20 , Current Consumption in Low-Frequency LPM0 Modes	38
• Changed the ADC Gain Factor, ADC Offset, REF 1.2V Reference, REF 1.45V Reference, REF 2.5V Reference	
Taps to Reserved in Table B-86 , Device Descriptor Table	177
• Added Section 6.14.1 , Revision Identification	178
• Added Section 6.14.2 , Device Identification	178

3 Device Comparison

Table 3-1 summarizes the features of the MSP432P401x microcontrollers.

Table 3-1. Device Comparison⁽¹⁾

DEVICE	FLASH (KB)	SRAM (KB)	ADC14 (channels)	COMP ₀ (channels)	COMP ₁ (channels)	Timer_A ⁽²⁾	USCI CHANNEL A: UART, I2C, SPI	CHANNEL B: SPI, I ² C	20-mA DRIVE I/O	TOTAL I/Os	PACKAGE
MSP432P401R1PZ	256	64	24 ext, 2 int	0	0	0, 0, 0, 0	4	4	4	64	100-PZ
MSP432P401M1PZ	256	32	24 ext, 2 int	0	0	0, 0, 0, 0	4	4	4	64	100-PZ
MSP432P401R2ZRH	256	64	16 ext, 2 int	0	0	0, 0, 0	3	4	4	64	80-ZRH
MSP432P401M2ZRH	256	32	16 ext, 2 int	0	0	0, 0, 0	3	4	7	64	80-ZRH
MSP432P401R0002	256	64	16 ext, 2 int	2	4	0, 0, 0	3	3	4	40	84-B00
MSP432P401M0002	256	32	16 ext, 2 int	2	4	0, 0, 0	3	3	4	40	84-B00

(1) For the most current part numbers and pricing information for all available devices, see the Pricing Order Assemblies in Section 5, or see the TI website at www.ti.com.

(2) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 0, 0 would represent two instantiations of Timer_A, the first instantiation having 0 capture/compare registers and PWM output generators, respectively.

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

Products for MSP 16-Bit and 32-Bit MCUs Low-power mixed-signal processors with smart analog and digital peripherals for a wide range of industrial and consumer applications.

Products for MSP432 Low Power + Performance MCUs MSP low-power and performance microcontrollers from TI provide designers with increased processing capability, smart analog, advanced security, and display and communication peripherals while using less watts than ever before for the development of "always on" embedded applications.

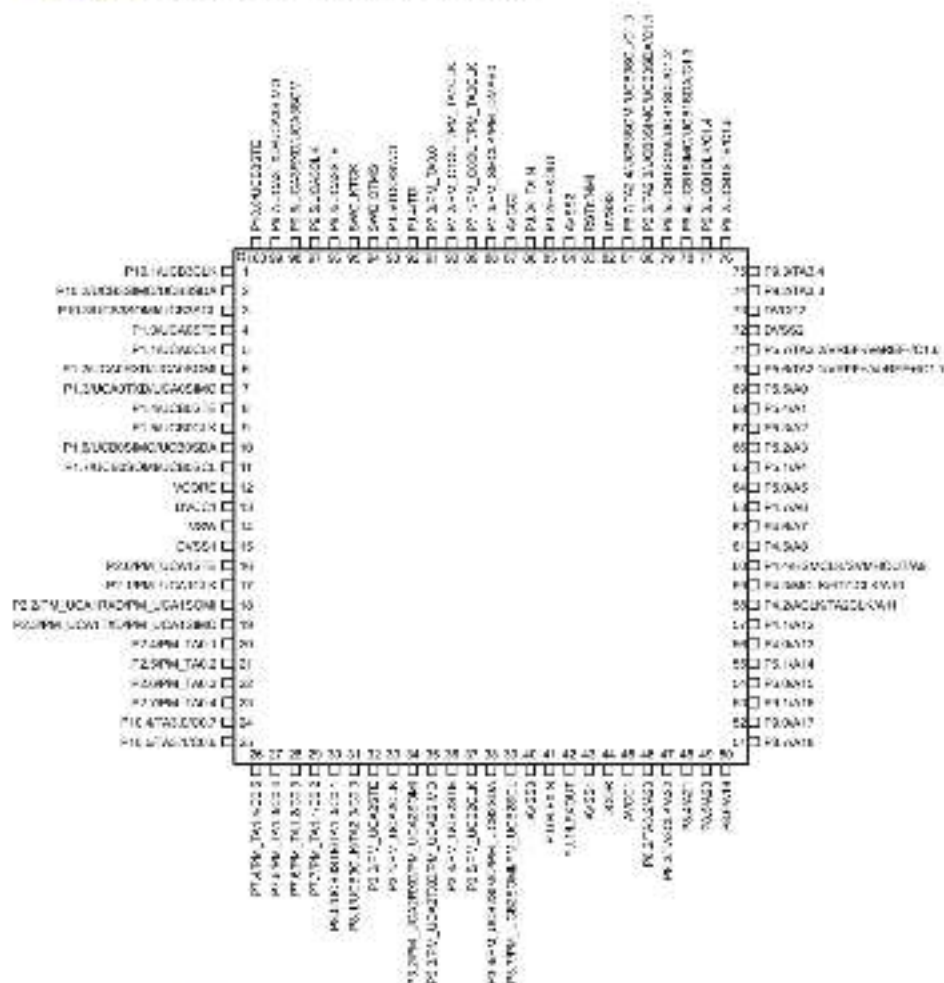
Companion Products for MSP432P401R Review products that are frequently purchased or used with this product.

Reference Designs for MSP432P401R The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the pinout of the 100-pin PZ package.



- A. The secondary digital functions on Pins P0, P1, and P2 are fully responsive. The pinout shows only the default mapping. See [Section 8.5.2](#) for details.
- B. A pull-up is implemented on these digital I/Os: P10, P14, P15, P30, P34, P35, P36, P37.
- C. UART RS485 pins: P17 – RS485D, P18 – RS485C.
- D. SPI CS0 pin: P14 – CS0, P15 – CS0, P16 – CS0, P17 – CS0, P18 – CS0.
- E. I2C CS0 pin: P10 – CS0, P11 – CS0, P12 – CS0, P13 – CS0, P14 – CS0, P15 – CS0, P16 – CS0, P17 – CS0, P18 – CS0.

Figure 4-1. 100-Pin PZ Package (Top View)

Figure 4-2 shows the pinout of the 80-pin ZXH package.

P1.0 SWDIO/CK	P1.1	P2.0	P2.1	P2.2	P2.3	P2.4	P2.5	P2.6
(A7)	(A8)	(A9)	(A6)	(A5)	(A4)	(A3)	(A2)	(A1)
P3.1 SWDIOTMS	P3.0	P7.0	P7.1	RESERVED	P4.0	P4.1	P4.2	P4.3
(D4)	(D3)	(D6)	(D5)	(D6)	(D7)	(D8)	(D9)	(D0)
P1.5 VCCRT		P1.2	P1.3	DAVDD1	DAVDD0	P5.0	P5.1	P5.2
(C1)	(C2)	(C4)	(C5)	(C6)	(C7)	(C8)	(C9)	(C0)
P1.6 DAVDD1	P1.4	P1.7	AVDD2	AVDD3	P5.3	P5.4	P5.5	P5.6
(B1)	(B2)	(B4)	(B5)	(B6)	(B7)	(B8)	(B9)	(B0)
P1.7 VDDH	P2.2	P2.0	AVDD2	DVDD2	P5.0	P5.1	P5.2	
(F1)	(F2)	(F3)	(F4)	(F5)	(F6)	(F7)	(F8)	(F9)
P2.3 DAVDD1	P2.4	P2.1	AVDD1	AVDD0	P4.0	P4.1	P4.2	P4.3
(F1)	(F2)	(F3)	(F4)	(F5)	(F6)	(F7)	(F8)	(F9)
P2.5	P2.6	P2.7	P6.0	P6.1	P6.2	P6.3	P6.4	P6.5
(G1)	(G2)	(G3)	(G4)	(G5)	(G6)	(G7)	(G8)	(G9)
P2.7	P7.0	P5.0	P5.1	P5.2	P5.3	P5.4	P5.5	P5.6
(H1)	(H2)	(H3)	(H4)	(H5)	(H6)	(H7)	(H8)	(H9)
P7.1	P7.2	P7.3	P7.4	P7.5	P7.6	P7.7	P7.8	P7.9
(J1)	(J2)	(J3)	(J4)	(J5)	(J6)	(J7)	(J8)	(J9)

- A. A glitch filter is implemented on these digital I/Os: P1.0, P1.1, P1.2, P2.0, P2.1, P2.2, P2.3, P2.4, P2.5, P2.6, P2.7.
 B. UART I/Os are: P1.2 – ESI/RXD, P1.3 – ESI/TXD.
 C. SPI I/Os are: P1.4 – SS/STB, P1.5 – SCLK, P1.6 – SS/SMO, P1.7 – SS/SDI.
 D. I²C I/Os are: P2.5 – SCL/SCL, P2.7 – SDA/SDA.

Figure 4-2. 80-Pin ZXH Package (Top View)

4.2 Pin Attributes

Table 4-1 describes the attributes of the pins.

Table 4-1. Pin Attributes

PIN NO. ⁽¹⁾			SIGNAL NAME ^(1, 2)	SIGNAL TYPE ⁽⁴⁾	BUFFER TYPE ⁽⁵⁾	POWER SOURCE ⁽⁶⁾	RESET STATE AFTER POR ⁽⁷⁾
PZ	ZX0	RGC					
1	N/A	N/A	P10.1 (RD)	IO	LVCMOS	DVDD	OFF
			EX0001K	IO	LVCMOS	LVDD	N/A
2	N/A	N/A	P10.2 (RD)	IO	LVCMOS	DVDD	OFF
			EX0000M0	IO	LVCMOS	LVDD	N/A
3	N/A	N/A	EX0000M0	IO	LVCMOS	LVDD	N/A
			EX0000M0	IO	LVCMOS	LVDD	N/A
4	A1	1	P1.0 (RD)	IO	LVCMOS	DVDD	OFF
			U00000E	IO	LVCMOS	LVDD	N/A
5	D1	2	P1.1 (RD)	IO	LVCMOS	DVDD	OFF
			EX0001K	IO	LVCMOS	LVDD	N/A
6	D1	3	P1.2 (RD)	IO	LVCMOS	DVDD	OFF
			EX0000M0	IO	LVCMOS	LVDD	N/A
7	D1	4	P1.3 (RD)	IO	LVCMOS	DVDD	OFF
			EX0000M0	IO	LVCMOS	LVDD	N/A
8	D3	5	P1.4 (RD)	IO	LVCMOS	DVDD	OFF
			U00000E	IO	LVCMOS	LVDD	N/A
9	D1	6	P1.5 (RD)	IO	LVCMOS	DVDD	OFF
			EX0001K	IO	LVCMOS	LVDD	N/A
10	D1	7	P1.6 (RD)	IO	LVCMOS	DVDD	OFF
			EX0000M0	IO	LVCMOS	LVDD	N/A
11	F1	8	P1.7 (RD)	IO	LVCMOS	DVDD	OFF
			EX0000M0	IO	LVCMOS	LVDD	N/A
12	C2	9	VCORE	—	Power	DVDD	N/A
13	C2	10	DVDD1	—	Power	N/A	N/A
14	E2	11	VEW	—	Power	N/A	N/A
15	D2	12	DVDD2	—	Power	N/A	N/A
16	F1	13	P1.8 (RD)	IO	LVCMOS	DVDD	OFF
			RM1000STT	IO	LVCMOS	LVDD	N/A

(1) N/A = not available on this package.

(2) (RD) indicates the reset default signal name for that pin.

(3) To determine the pin mode attributes for each pin, see Section 5.12, Input/Output Properties.

(4) Signal Type: I = Input, O = Output, IO = Input or Output, P = power.

(5) Buffer Type: see Table 4-2 for details.

(6) The power source shown in this table is the I/O power source, which may differ from the module power source.

(7) Reset States:

OFF = Input impedance with Schmitt trigger and pull-up or pull-down (if available) enabled.

PD = High-impedance input with pull-down enabled.

PU = High-impedance input with pull-up enabled.

N/A = Not applicable.

Table 4-1. Pin Attributes (continued)

PIN NO. ⁽¹⁾			SIGNAL NAME ⁽²⁾	SIGNAL TYPE ⁽³⁾	BUFFER TYPE ⁽⁴⁾	POWER SOURCE ⁽⁵⁾	RESET STATE AFTER POR ⁽⁶⁾
PT	TXR	RGS					
17	F1	14	P2.1 (RD)	IO	LVCMOS	DVDD	OFF
			PM1VCA2CLK	IO	LVCMOS	DVDD	N/A
18	E3	10	P2.2 (RD)	IO	LVCMOS	DVDD	OFF
			PM1UCM0RXD	I	LVCMOS	DVDD	N/A
			PM1UCM0RXM	IO	LVCMOS	DVDD	N/A
19	F4	16	P2.3 (RD)	IO	LVCMOS	DVDD	OFF
			PM1UCM0XD	IO	LVCMOS	DVDD	N/A
			PM1UCM0RND	IO	LVCMOS	DVDD	N/A
20	F3	N/A	P2.4 (RD)	IO	LVCMOS	DVDD	OFF
			PM1TA0.1	IO	LVCMOS	DVDD	N/A
21	G4	N/A	P2.5 (RD)	IO	LVCMOS	DVDD	OFF
			PM1TA0.2	IO	LVCMOS	DVDD	N/A
22	G2	N/A	P2.6 (RD)	IO	LVCMOS	DVDD	OFF
			PM1TA0.3	IO	LVCMOS	DVDD	N/A
23	H1	N/A	P2.7 (RD)	IO	LVCMOS	DVDD	OFF
			PM1TA0.4	IO	LVCMOS	DVDD	N/A
24	N/A	N/A	P0B.1 (RH)	IO	LVCMOS	DVDD	DI
			TA0.0	IO	LVCMOS	DVDD	N/A
			CA0.7	I	Analog	DVDD	N/A
			P0B.5 (RH)	IO	LVCMOS	DVDD	DI
25	N/A	N/A	TA0.1	IO	LVCMOS	DVDD	N/A
			CA0.6	I	Analog	DVDD	N/A
26	J1	N/A	P2.8 (RD)	IO	LVCMOS	DVDD	OFF
			PM1TA0.4	IO	LVCMOS	DVDD	N/A
			CA0.5	I	Analog	DVDD	N/A
27	J2	N/A	P2.9 (RD)	IO	LVCMOS	DVDD	OFF
			PM1TA0.3	IO	LVCMOS	DVDD	N/A
			CA0.4	I	Analog	DVDD	N/A
28	J2	N/A	P2.0 (RD)	IO	LVCMOS	DVDD	OFF
			PM1TA0.2	IO	LVCMOS	DVDD	N/A
			CA0.3	I	Analog	DVDD	N/A
29	G3	N/A	P2.7 (RD)	IO	LVCMOS	DVDD	OFF
			PM1TA0.1	IO	LVCMOS	DVDD	N/A
			CA0.2	I	Analog	DVDD	N/A
			P2.0 (RD)	IO	LVCMOS	DVDD	OFF
30	H5	17	UCS98TE	IO	LVCMOS	DVDD	N/A
			TA0.0	IO	LVCMOS	DVDD	N/A
			CA0.1	I	Analog	DVDD	N/A
31	G4	18	P0.1 (RD)	IO	LVCMOS	DVDD	OFF
			UCS98CLK	IO	LVCMOS	DVDD	N/A
			TA0.0	IO	LVCMOS	DVDD	N/A
			CA0.0	I	Analog	DVDD	N/A
32	J3	19	P3.0 (RD)	IO	LVCMOS	DVDD	OFF
			PM1UCM0STE	IO	LVCMOS	DVDD	N/A
33	H4	20	P3.1 (RD)	IO	LVCMOS	DVDD	OFF
			PM1UCM0CLK	IO	LVCMOS	DVDD	N/A

Table 4-1. Pin Attributes (continued)

PIN NO. ⁽¹⁾			SIGNAL NAME ⁽¹⁾	SIGNAL TYPE ⁽¹⁾	BUFFER TYPE ⁽¹⁾	POWER SOURCE ⁽¹⁾	RESET STATE AFTER POR ⁽²⁾
PIN	FXR	RG0					
34	A5	24	FS.2 (RD)	IO	LVCMOS	DVDD	OFF
			FM_FXCRX1	I	LVCMOS	DVDD	N/A
			FM_UC2800H	IO	LVCMOS	DVDD	N/A
35	A6	25	FS.3 (RD)	IO	LVCMOS	DVDD	OFF
			FM_FXCRX2	I	LVCMOS	DVDD	N/A
			FM_UC2800	IO	LVCMOS	DVDD	N/A
36	A5	26	FS.4 (RD)	IO	LVCMOS	DVDD	DI
			FM_UC2801E	IO	LVCMOS	DVDD	N/A
37	A6	24	FS.5 (RD)	IO	LVCMOS	DVDD	OFF
			FM_FXCRX3	IO	LVCMOS	DVDD	N/A
38	A5	25	FS.6 (RD)	IO	LVCMOS	DVDD	OFF
			FM_FXCRX4	IO	LVCMOS	DVDD	N/A
			FM_UC2805	IO	LVCMOS	DVDD	N/A
39	A6	26	FS.7 (RD)	IO	LVCMOS	DVDD	OFF
			FM_FXCRX5	IO	LVCMOS	DVDD	N/A
			FM_UC2806	I	LVCMOS	DVDD	N/A
40	A5	27	AVSS1	–	Power	N/A	N/A
41	A6	28	FS.8 (RD)	IO	LVCMOS	DVDD	OFF
			UFXIN	I	Analog	DVDD	N/A
			FS.9 (RD)	IO	LVCMOS	DVDD	DI
42	A7	29	UFXOUT	O	Analog	DVDD	N/A
43	A5	30	AVSS1	–	Power	N/A	N/A
44	A8	31	DOCK	–	Analog	N/A	N/A
45	A0	32	AVCC1	–	Power	N/A	N/A
			FS.1 (RD)	IO	LVCMOS	DVDD	DI
			FS.2	IO	LVCMOS	DVDD	N/A
46	N/A	N/A	A20	I	Analog	DVDD	N/A
			FS.3 (RD)	IO	LVCMOS	DVDD	DI
			TAC10H	I	LVCMOS	DVDD	N/A
47	N/A	N/A	A21	I	Analog	DVDD	N/A
			FS.4 (RD)	IO	LVCMOS	DVDD	OFF
			A21	I	Analog	DVDD	N/A
48	N/A	N/A	FS.5 (RD)	IO	LVCMOS	DVDD	OFF
			A20	I	Analog	DVDD	N/A
			FS.6 (RD)	IO	LVCMOS	DVDD	DI
49	N/A	N/A	A19	I	Analog	DVDD	N/A
			FS.7 (RD)	IO	LVCMOS	DVDD	DI
			A18	I	Analog	DVDD	N/A
50	N/A	N/A	FS.8 (RD)	IO	LVCMOS	DVDD	OFF
			A17	I	Analog	DVDD	N/A
51	N/A	N/A	FS.9 (RD)	IO	LVCMOS	DVDD	OFF
			A16	I	Analog	DVDD	N/A
52	A0	N/A	FS.10 (RD)	IO	LVCMOS	DVDD	OFF
			A15	I	Analog	DVDD	N/A
			FS.11 (RD)	IO	LVCMOS	DVDD	DI
53	A7	N/A	A14	I	Analog	DVDD	N/A

Table 4-1. Pin Attributes (continued)

PIN NO. ⁽¹⁾			SIGNAL NAME ⁽¹⁾	SIGNAL TYPE ⁽¹⁾	BUFFER TYPE ⁽¹⁾	POWER SOURCE ⁽¹⁾	RESET STATE AFTER POR ⁽²⁾
PT	TXR	RGS					
56	H5	N/A	P4.0 (RD)	IO	LVCMOS	DVDD	OFF
			A13	I	Analog	DVDD	N/A
57	H5	N/A	P4.1 (RD)	IO	LVCMOS	DVDD	OFF
			A12	I	Analog	DVDD	N/A
58	D7	D3	P4.2 (RD)	IO	LVCMOS	DVDD	OFF
			ADCLK	O	LVCMOS	DVDD	N/A
			TA0CLK	I	LVCMOS	DVDD	N/A
			A11	I	Analog	DVDD	N/A
59	C8	S4	P4.3 (RD)	IO	LVCMOS	DVDD	OFF
			MD1K	O	LVCMOS	DVDD	N/A
			RTCLK	O	LVCMOS	DVDD	N/A
			A10	I	Analog	DVDD	N/A
60	C9	S5	P4.4 (RD)	IO	LVCMOS	DVDD	OFF
			HSCLK	O	LVCMOS	DVDD	N/A
			SVMDMA1	O	LVCMOS	DVDD	N/A
			A9	I	Analog	DVDD	N/A
61	F7	D6	P4.5 (RD)	IO	LVCMOS	DVDD	DI
			A8	I	Analog	DVDD	N/A
62	F8	D7	P4.6 (RD)	IO	LVCMOS	DVDD	OFF
			A7	I	Analog	DVDD	N/A
63	F9	30	P4.7 (RD)	IO	LVCMOS	DVDD	OFF
			A6	I	Analog	DVDD	N/A
64	E7	30	P5.0 (RD)	IO	LVCMOS	DVDD	OFF
			A5	I	Analog	DVDD	N/A
65	E8	40	P5.1 (RD)	IO	LVCMOS	DVDD	OFF
			A4	I	Analog	DVDD	N/A
66	F4	41	P5.2 (RD)	IO	LVCMOS	DVDD	DI
			A3	I	Analog	DVDD	N/A
67	D7	42	P5.3 (RD)	IO	LVCMOS	DVDD	OFF
			A2	I	Analog	DVDD	N/A
68	D8	43	P5.4 (RD)	IO	LVCMOS	DVDD	OFF
			A1	I	Analog	DVDD	N/A
69	C8	44	P5.5 (RD)	IO	LVCMOS	DVDD	OFF
			A0	I	Analog	DVDD	N/A
			P5.6 (RD)	IO	LVCMOS	DVDD	OFF
			TQ2.1	IO	LVCMOS	DVDD	N/A
70	D9	45	VBATT	O	Analog	DVDD	N/A
			VBATT+I	I	Analog	DVDD	N/A
			Cl. 7	I	Analog	DVDD	N/A
			P5.7 (RD)	IO	LVCMOS	DVDD	DI
71	C9	46	TQ2.2	IO	LVCMOS	DVDD	N/A
			VBREF	O	Analog	DVDD	N/A
			VBREFP	I	Analog	DVDD	N/A
			Cl. 6	I	Analog	DVDD	N/A
72	F6	47	DVDD2	—	Power	N/A	N/A
73	C5	48	DVDD2	—	Power	N/A	N/A

Table 4-1. Pin Attributes (continued)

PIN NO. ⁽¹⁾			SIGNAL NAME ⁽²⁾	SIGNAL TYPE ⁽³⁾	BUFFER TYPE ⁽⁴⁾	POWER SOURCE ⁽⁵⁾	RESET STATE AFTER POR ⁽⁶⁾
P7	PXH	FG0					
74	N/A	N/A	P0.2 (RD)	IO	LVCMOS	DVDD	OFF
			TAL3	IO	LVCMOS	DVDD	N/A
75	N/A	N/A	P0.3 (RD)	IO	LVCMOS	DVDD	OFF
			TAL4	IO	LVCMOS	DVDD	N/A
76	N/A	N/A	P0.4 (RD)	IO	LVCMOS	DVDD	OFF
			UC0P0STE	IO	LVCMOS	DVDD	N/A
77	N/A	N/A	CT5	I	Analog	LVDD	N/A
			P0.5 (RD)	IO	LVCMOS	DVDD	OFF
78	N/A	N/A	UC0CLK	IO	LVCMOS	DVDD	N/A
			CT7	I	Analog	LVDD	N/A
79	A0	N/A	P0.4 (RD)	IO	LVCMOS	DVDD	OFF
			UC0P0SMD	IO	LVCMOS	DVDD	N/A
80	A2	N/A	UC0P0S0A	IO	LVCMOS	DVDD	N/A
			CT3	I	Analog	DVDD	N/A
81	A7	N/A	P0.5 (RD)	IO	LVCMOS	DVDD	OFF
			UC0P0S0M	IO	LVCMOS	DVDD	N/A
82	B0	40	P0.7 (RD)	IO	LVCMOS	DVDD	OFF
			TAL7	IO	LVCMOS	DVDD	N/A
83	B7	50	UC0P0S0M	IO	LVCMOS	DVDD	N/A
			CT0	I	Analog	DVDD	N/A
84	C7	51	P0.7 (RD)	IO	LVCMOS	DVDD	OFF
			TAL8	IO	LVCMOS	DVDD	N/A
85	B6	52	UC0P0S0M	IO	LVCMOS	DVDD	N/A
			CT1	I	Analog	DVDD	N/A
86	D5	53	P0.8 (RD)	IO	LVCMOS	DVDD	OFF
			HEXOUT	O	Analog	DVDD	N/A
87	A4	54	P0.9 (RD)	IO	LVCMOS	DVDD	OFF
			HEXIN	I	Analog	DVDD	N/A
88	D5	55	P0.9 (RD)	IO	LVCMOS	DVDD	OFF
			HEXIN	I	Analog	DVDD	N/A
89	B7	57	P0.10 (RD)	IO	LVCMOS	DVDD	OFF
			FM_SMCCLK	O	LVCMOS	DVDD	N/A
90	D5	58	P0.11 (RD)	IO	LVCMOS	DVDD	OFF
			FM_SMCCLK	O	LVCMOS	DVDD	N/A
91	B4	59	P0.12 (RD)	IO	LVCMOS	DVDD	OFF
			FM_SMCCLK	O	LVCMOS	DVDD	N/A
92	B4	59	P0.13 (RD)	IO	LVCMOS	DVDD	OFF
			FM_SMCCLK	O	LVCMOS	DVDD	N/A

Table 4-1. Pin Attributes (continued)

PIN NO. ⁽¹⁾			SIGNAL NAME ⁽¹⁾	SIGNAL TYPE ⁽¹⁾	BUFFER TYPE ⁽¹⁾	POWER SOURCE ⁽¹⁾	RESET STATE AFTER POR ⁽²⁾
PT	TXR	RGS					
0	A4	00	PT2 (RD)	IO	LVCNOS	DVDD	OFF
			PM-TAG0	IO	LVCNOS	DVDD	N/A
02	B3	01	P24	IO	LVCNOS	DVDD	N/A
			TD1 (RD)	I	LVCNOS	DVDD	PU
			P25	IO	LVCNOS	DVDD	N/A
03	A3	02	TD0 (RD)	O	LVCNOS	DVDD	N/A
			SW0	I	LVCNOS	DVDD	N/A
04	B2	03	SW1 (RD)	IO	LVCNOS	DVDD	PU
05	A2	04	SW0-KTCH	I	LVCNOS	DVDD	PD
06	N/A	N/A	PR4 (RD)	IO	LVCNOS	DVDD	DX
08	N/A	N/A	UC98STE	IO	LVCNOS	DVDD	N/A
09	N/A	N/A	PR5 (RD)	IO	LVCNOS	DVDD	OFF
			UC98CLK	IO	LVCNOS	DVDD	N/A
10	N/A	N/A	PR0 (RD)	IO	LVCNOS	DVDD	OFF
			UC98RX0	I	LVCNOS	DVDD	N/A
			UC98RX1	IO	LVCNOS	DVDD	N/A
11	N/A	N/A	PR7 (RD)	IO	LVCNOS	DVDD	DX
			UC98RX2	O	LVCNOS	DVDD	N/A
			UC98RX3	IO	LVCNOS	DVDD	N/A
100	N/A	N/A	PR10 (RD)	IO	LVCNOS	DVDD	DX
			UC98STE	IO	LVCNOS	DVDD	N/A
N/A	N/A	Pnd	QTM-Pnd	–	–	N/A	–

4.3 Signal Descriptions

Table 4-2 describes the signals for all device variants and package options.

Table 4-2. Signal Descriptions

FUNCTION	SIGNAL NAME	SIGNAL NO. (1)			SIGNAL TYPE (2)	DESCRIPTION
		P2	ZXH	R00		
ADC	A0	70	C0	44	I	ADC analog input A0
	A1	68	D8	43	I	ADC analog input A1
	A2	67	D7	42	I	ADC analog input A2
	A3	66	E2	41	I	ADC analog input A3
	A4	65	E8	40	I	ADC analog input A4
	A5	64	F7	39	I	ADC analog input A5
	A6	63	F6	38	I	ADC analog input A6
	A7	62	F5	37	I	ADC analog input A7
	A8	61	F7	36	I	ADC analog input A8
	A9	60	G0	35	I	ADC analog input A9
	A10	59	G0	34	I	ADC analog input A10
	A11	58	G7	33	I	ADC analog input A11
	A12	57	H8	N/A	I	ADC analog input A12
	A13	56	H9	N/A	I	ADC analog input A13
	A14	55	H7	N/A	I	ADC analog input A14
	A15	54	J4	N/A	I	ADC analog input A15
	A16	53	J4	N/A	I	ADC analog input A16
	A17	52	J5	N/A	I	ADC analog input A17
	A18	51	J4	N/A	I	ADC analog input A18
	A19	50	J5	N/A	I	ADC analog input A19
	A20	49	J6	N/A	I	ADC analog input A20
	A21	48	J6	N/A	I	ADC analog input A21
	A22	47	J5	N/A	I	ADC analog input A22
	A23	46	J4	N/A	I	ADC analog input A23
Clock	ACLK	18	G7	33	O	ACLK clock output
	DC2DR	17	J1	31	—	DC2 external resistor pin
	HFXIN	58	A5	55	I	Input to high-frequency crystal oscillator (HFX)
	HFXOUT	55	A5	54	O	Output for high-frequency crystal oscillator (HFX)
	LFXTCLK	70	D8	36	O	LFXTCLK clock output
	LFXTIN	41	J5	28	I	Input for low-frequency crystal oscillator (LFXT)
	LFXTOUT	42	J7	29	O	Output of low-frequency crystal oscillator (LFXT)
	RLCLK	19	D8	34	O	RLCLK clock output

(1) N/A = not available

(2) I = input, O = output

Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO. ⁽¹⁾			SIGNAL TYPE ⁽²⁾	DESCRIPTION
		P2	ZMH	R00		
Comparator	CO0	31	14	10	I	Comparator_E0 input 0
	CO1	29	15	11	I	Comparator_E0 input 1
	CO2	28	16	12A	I	Comparator_E0 input 2
	CO3	30	17	12A	I	Comparator_E0 input 3
	CO4	27	12	13A	I	Comparator_E0 input 4
	CO5	26	11	13A	I	Comparator_E0 input 5
	CO6	25	14A	14A	I	Comparator_E0 input 6
	CO7	24	14A	14A	I	Comparator_E0 input 7
	CO8	31	16	16	I	Comparator_E1 input 0
	CO9	30	15	17	I	Comparator_E1 input 1
	CO10	29	16	17A	I	Comparator_E1 input 2
	CO11	28	17	17A	I	Comparator_E1 input 3
	CO12	27	12	18A	I	Comparator_E1 input 4
	CO13	26	11	18A	I	Comparator_E1 input 5
Debug	SWCLK/IOCLK	28	A7	24	I	Serial-wire clock input (SWCLK/IOCLK clock input (IOCLK))
	SWDIO/IOCS	29	D2	23	IO	Serial-wire data input/output (SWDIO/IOCS test mode select (TMS))
	SWO	30	A5	22	O	Serial-wire trace output
	TDI	32	E3	61	I	JTAG test data input
	TDO	33	A3	62	O	JTAG test data output
GPIO	P1.0	4	A4	1	IO	General-purpose digital I/O with port interrupt, wake-up, and glitch-filtering capability
	P1.1	5	P4	2	IO	General-purpose digital I/O with port interrupt and wake-up capability
	P1.2	6	C6	3	IO	General-purpose digital I/O with port interrupt and wake-up capability
	P1.3	7	D6	4	IO	General-purpose digital I/O with port interrupt and wake-up capability
	P1.4	8	LS	5	IO	General-purpose digital I/O with port interrupt, wake-up, and glitch-filtering capability
	P1.5	9	UT	6	IO	General-purpose digital I/O with port interrupt, wake-up, and glitch-filtering capability
	P1.6	10	DT	7	IO	General-purpose digital I/O with port interrupt and wake-up capability
	P1.7	11	FT	8	IO	General-purpose digital I/O with port interrupt and wake-up capability

Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO. ⁽¹⁾			SIGNAL TYPE ⁽²⁾	DESCRIPTION
		P2	ZMH	R00		
GPIO (continued)	P2.0	15	F4	13	IO	General-purpose digital I/O with port interrupt and wake-up capability, and with reconfigurable port mapping secondary function. This I/O can be configured for high-drive operation with up to 20-mA drive capability.
	P2.1	17	F1	14	IO	General-purpose digital I/O with port interrupt and wake-up capability, and with reconfigurable port mapping secondary function. This I/O can be configured for high-drive operation with up to 20-mA drive capability.
	P2.2	18	F5	15	IO	General-purpose digital I/O with port interrupt and wake-up capability, and with reconfigurable port mapping secondary function. This I/O can be configured for high-drive operation with up to 20-mA drive capability.
	P2.3	19	F4	16	IO	General-purpose digital I/O with port interrupt and wake-up capability, and with reconfigurable port mapping secondary function. This I/O can be configured for high-drive operation with up to 20-mA drive capability.
	P2.4	20	F3	N/A	IO	General-purpose digital I/O with port interrupt and wake-up capability, and with reconfigurable port mapping secondary function.
	P2.5	21	G0	N/A	IO	General-purpose digital I/O with port interrupt and wake-up capability, and with reconfigurable port mapping secondary function.
	P2.6	22	F2	N/A	IO	General-purpose digital I/O with port interrupt and wake-up capability, and with reconfigurable port mapping secondary function.
	P2.7	23	H1	N/A	IO	General-purpose digital I/O with port interrupt and wake-up capability, and with reconfigurable port mapping secondary function.
	P3.0	32	J3	19	IO	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability, and with reconfigurable port mapping secondary function.
	P3.1	33	I0	20	IO	General-purpose digital I/O with port interrupt and wake-up capability, and with reconfigurable port mapping secondary function.
	P3.2	34	I6	21	IO	General-purpose digital I/O with port interrupt and wake-up capability, and with reconfigurable port mapping secondary function.
	P3.3	35	J4	22	IO	General-purpose digital I/O with port interrupt and wake-up capability, and with reconfigurable port mapping secondary function.
	P3.4	36	I5	23	IO	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability, and with reconfigurable port mapping secondary function.
	P3.5	37	I2	24	IO	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability, and with reconfigurable port mapping secondary function.
	P3.6	38	J2	25	IO	General-purpose digital I/O with port interrupt and wake-up capability, and with reconfigurable port mapping secondary function.
	P3.7	39	I6	26	IO	General-purpose digital I/O with port interrupt and wake-up capability, and with reconfigurable port mapping secondary function.

Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO. ⁽¹⁾			SIGNAL TYPE ⁽²⁾	DESCRIPTION
		P2	ZOH	ROC		
C1001 (continued)	PT.0	36	E5	67	IO	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	PT.1	39	O5	68	IO	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	PT.2	39	E4	69	IO	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	PT.3	34	A4	60	IO	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	PT.4	38	J1	70A	IO	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	PT.5	37	L2	70A	IO	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	PT.6	36	J1	70A	IO	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	PT.7	38	A3	70A	IO	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	PE.0	70	L3	17	IO	General-purpose digital I/O
	PE.1	31	L4	18	IO	General-purpose digital I/O
	PE.2	46	N/A	N/A	IO	General-purpose digital I/O
	PE.3	47	N/A	N/A	IO	General-purpose digital I/O
	PE.4	48	N/A	N/A	IO	General-purpose digital I/O
	PE.5	46	N/A	N/A	IO	General-purpose digital I/O
	PE.6	50	N/A	N/A	IO	General-purpose digital I/O
	PE.7	51	N/A	N/A	IO	General-purpose digital I/O
	PE.8	52	N/A	N/A	IO	General-purpose digital I/O
	PE.9	53	N/A	N/A	IO	General-purpose digital I/O
	PE.0	54	N/A	N/A	IO	General-purpose digital I/O
	PE.1	55	N/A	N/A	IO	General-purpose digital I/O
	PE.2	56	N/A	N/A	IO	General-purpose digital I/O
	PE.3	57	N/A	N/A	IO	General-purpose digital I/O
	PE.4	58	N/A	N/A	IO	General-purpose digital I/O
	PE.5	59	N/A	N/A	IO	General-purpose digital I/O
	PE.6	58	N/A	N/A	IO	General-purpose digital I/O
	PE.7	59	N/A	N/A	IO	General-purpose digital I/O
	PE.8	60	N/A	N/A	IO	General-purpose digital I/O
	PE.9	1	N/A	N/A	IO	General-purpose digital I/O
	PE.10	2	N/A	N/A	IO	General-purpose digital I/O
	PE.11	3	N/A	N/A	IO	General-purpose digital I/O
	PE.12	34	N/A	N/A	IO	General-purpose digital I/O
	PE.13	35	N/A	N/A	IO	General-purpose digital I/O
	PE.14	41	J0	20	IO	General-purpose digital I/O
	PE.15	42	J0	24	IO	General-purpose digital I/O
	PE.16	55	A0	64	IO	General-purpose digital I/O
	PE.17	56	A0	65	IO	General-purpose digital I/O
	PE.18	62	B3	61	IO	General-purpose digital I/O
	PE.19	63	A3	62	IO	General-purpose digital I/O

Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO. ⁽¹⁾			SIGNAL TYPE ⁽²⁾	DESCRIPTION
		P2	ZMH	R00		
PC	FX040K0	11	11	5	IO	PC clock – w/FX040 PC mode
	UCS080A	10	01	7	IO	PC data – w/UC080 PC mode
	FX015C0	29	A7	2A	IO	PC clock – w/FX015 PC mode
	FX015B0A	28	A6	2A	IO	PC clock – w/FX015 PC mode
	UC030C0	3	N/A	N/A	IO	PC clock – w/UC030 PC mode
	FX020C0	14	07	50	IO	PC clock – w/FX020 PC mode
	UC090A	2	N/A	N/A	IO	PC data – w/UC090 PC mode
	UC030A	50	E6	40	IO	PC data – w/UC030 PC mode

Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO. ⁽¹⁾			SIGNAL TYPE ⁽²⁾	DESCRIPTION
		P2	ZMH	R00		
I/Os/Mem	EM_CICUI	19	15	50	I	Default mapping: Comparator 10 output
	EM_CICUI	20	16	50	O	Default mapping: Comparator 10 output
	EM_DACD0	16	15	57	I	Default mapping: DMA channel 0 input
	EM_SMCLK	10	15	57	I	Default mapping: SMCLK clock output
	EM_IAD0	01	A4	50	I/O	Default mapping: TAO GCR0 capture: CCH0 input, compare: 0.0
	EM_IAD1	01	15	50A	I/O	Default mapping: TAO GCR1 capture: CCH1 input, compare: 0.0
	EM_IAD2	01	12	50A	I/O	Default mapping: IAD GCR2 capture: CCH2 input, compare: 0.0
	EM_IAD3	02	12	50A	I/O	Default mapping: IAD GCR3 capture: CCH3 input, compare: 0.0
	EM_TA0_4	23	11	50A	I/O	Default mapping: IAD GCR4 capture: CCH4 input, compare: 0.0
	EM_IADCLK	19	15	50	I	Default mapping: IAD clock output
	EM_IAD2	01	12	50A	I/O	Default mapping: IAD GCR2 capture: CCH2 input, compare: 0.0
	EM_TA0_3	27	12	50A	I/O	Default mapping: IAD GCR3 capture: CCH3 input, compare: 0.0
	EM_TA0_4	28	11	50A	I/O	Default mapping: IAD GCR4 capture: CCH4 input, compare: 0.0
	EM_TA0CLK	19	15	50	I	Default mapping: TA0 clock output
	EM_UCG0CLK	17	F1	14	I/O	Default mapping: Clock signal input – eUSC0_A0 SPI slave mode Clock signal output – eUSC0_A0 SPI master mode
	EM_UCG0RXD	10	15	15	I	Default mapping: Receive data – eUSC0_A0 UART mode
	EM_UCG0TXD	19	15	16	I/O	Default mapping: Slave tx, master out – eUSC0_A0 SPI mode
	EM_UCG0SMD	10	15	15	I/O	Default mapping: Slave tx, master in – eUSC0_A0 SPI mode
	EM_UCG0SMD	10	15	15	I/O	Default mapping: Slave tx, master in – eUSC0_A0 SPI mode
	EM_UCG0SMD	10	15	15	I/O	Default mapping: Slave tx, master in – eUSC0_A0 SPI mode
	EM_UCG0SMD	10	15	15	I/O	Default mapping: Slave tx, master in – eUSC0_A0 SPI mode
	EM_UCG0SMD	10	15	15	I/O	Default mapping: Slave tx, master in – eUSC0_A0 SPI mode
	EM_UCG0SMD	10	15	15	I/O	Default mapping: Slave tx, master in – eUSC0_A0 SPI mode
	EM_UCG0SMD	10	15	15	I/O	Default mapping: Slave tx, master in – eUSC0_A0 SPI mode
	EM_UCG0SMD	10	15	15	I/O	Default mapping: Slave tx, master in – eUSC0_A0 SPI mode
	EM_UCG0SMD	10	15	15	I/O	Default mapping: Slave tx, master in – eUSC0_A0 SPI mode
	EM_UCG0SMD	10	15	15	I/O	Default mapping: Slave tx, master in – eUSC0_A0 SPI mode
	EM_UCG0SMD	10	15	15	I/O	Default mapping: Slave tx, master in – eUSC0_A0 SPI mode
	EM_UCG0SMD	10	15	15	I/O	Default mapping: Slave tx, master in – eUSC0_A0 SPI mode
	EM_UCG0SMD	10	15	15	I/O	Default mapping: Slave tx, master in – eUSC0_A0 SPI mode
	EM_UCG0SMD	10	15	15	I/O	Default mapping: Slave tx, master in – eUSC0_A0 SPI mode
	EM_UCG0SMD	10	15	15	I/O	Default mapping: Slave tx, master in – eUSC0_A0 SPI mode

Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO. ⁽¹⁾			SIGNAL TYPE ⁽²⁾	DESCRIPTION
		P2	ZMH	R00		
I/O: Master (continued)	FM_US02CLK	37	06	24	I/O	Lowest mapping: Clock signal input = 40000 Hz 10% duty cycle mode Clock signal output = at 150/100 SPI master mode
	FM_US02SCL	39	H0	26	I	Default mapping: I/O clock = iUSCI_E2 I/O mode
	FM_US02SDA	38	J5	25	I/O	Default mapping: I/O data = iUSCI_E2 I/O mode
	FM_US02SMO	36	J5	25	I/O	Lowest mapping: Slave rx, master out = 40000 Hz SPI mode
	FM_US02SMI	39	H0	26	I/O	Lowest mapping: Slave rx, master in = 40000 Hz SPI mode
	FM_US02STE	36	H0	26	I/O	Default mapping: Slave transmit enable = iUSCI_E2 SPI mode
Power	AVCC1	45	F5	32	—	Analog power supply
	AVCLL2	51	05	36	—	Analog power supply
	AVSS1	43	F5	30	—	Analog ground supply
	AVSS2	51	06	31	—	Analog ground supply
	AVSS3	49	05	27	—	Analog ground supply
	DVCC1	45	09	16	—	Digital power supply
	DVCC2	25	08	10	—	Digital power supply
	DVSS1	45	F2	12	—	Digital ground supply
	DVSS2	25	F5	17	—	Digital ground supply
	DVSS3	52	07	31	—	Must be connected to ground
	VCCORE ⁽³⁾	12	02	5	—	Regulated core power supply (internal use only; no external current loading)
RTC	VSM	14	E2	11	—	DC to DC converter switching output
	RTTCLK	59	06	35	I	RTC clock calibration output
Reference	VREF+	70	D9	45	I	Internal shunt reference voltage positive terminal
	VREF	71	C9	46	O	Internal shunt reference voltage negative terminal
	VREFH+	70	09	45	I	External terminal of external reference voltage for ADC
	VREFH-	71	09	46	I	Negative terminal of external reference voltage to ADC (external resistor needed to convert to unipolar potential)

⁽³⁾ VCCORE is for internal use only. No external current loading is needed. VCCORE should only be connected to the two recommended capacitors.

Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO. ⁽¹⁾			SIGNAL TYPE ⁽²⁾	DESCRIPTION
		P2	ZMH	R00		
SPI	UCW0CLK	0	E1	2	IO	Clock signal input – eUSCI_A0 SPI slave mode Clock signal output – eUSCI_A0 SPI master mode
	UCW0SMD	7	D0	4	IO	Slave in, master out – eUSCI_A0 SPI mode
	UCW0S0M0	8	D4	5	IO	Slave out, master in – eUSCI_A0 SPI mode
	UCW0STT	4	A4	1	IO	Slave transmit enable – eUSCI_A0 SPI mode
	UCW0CLK	27	N/A	N/A	IO	Clock signal input – eUSCI_A1 SPI slave mode Clock signal output – eUSCI_A1 SPI master mode
	UCW0SMD	28	N/A	N/A	IO	Slave in, master out – eUSCI_A1 SPI mode
	UCW0S0M0	29	N/A	N/A	IO	Slave out, master in – eUSCI_A1 SPI mode
	UCW0STT	25	N/A	N/A	IO	Slave transmit enable – eUSCI_A1 SPI mode
	UCW0CLK	8	D3	6	IO	Clock signal input – eUSCI_B0 SPI slave mode Clock signal output – eUSCI_B0 SPI master mode
	UCW0SMD	10	D1	7	IO	Slave in, master out – eUSCI_B0 SPI mode
	UCW0S0M0	11	E1	8	IO	Slave out, master in – eUSCI_B0 SPI mode
	UCW0STT	0	D0	5	IO	Slave transmit enable – eUSCI_B0 SPI mode
	UCW0CLK	27	FR	N/A	IO	Clock signal input – eUSCI_B1 SPI slave mode Clock signal output – eUSCI_B1 SPI master mode
	UCW0SMD	26	A0	N/A	IO	Slave in, master out – eUSCI_B1 SPI mode
	UCW0S0M0	29	A7	N/A	IO	Slave out, master in – eUSCI_B1 SPI mode
	UCW0STT	26	A6	N/A	IO	Slave transmit enable – eUSCI_B1 SPI mode
	UCW0CLK	1	N/A	N/A	IO	Clock signal input – eUSCI_C0 SPI slave mode Clock signal output – eUSCI_C0 SPI master mode
	UCW0CLK	14	B4	10	IO	Clock signal input – eUSCI_C1 SPI slave mode Clock signal output – eUSCI_C1 SPI master mode
	UCW0SMD	7	N/A	N/A	IO	Slave in, master out – eUSCI_C1 SPI mode
	UCW0S0M0	20	B5	49	IO	Slave out, master in – eUSCI_C1 SPI mode
	UCW0S0M0	3	N/A	N/A	IO	Slave out, master in – eUSCI_B3 SPI mode
	UCW0S0M0	51	B7	50	IO	Slave out, master in – eUSCI_C3 SPI mode
	UCW0STT	20	B6	17	IO	Slave transmit enable – eUSCI_B3 SPI mode
	UCW0STT	101	N/A	N/A	IO	Slave transmit enable – eUSCI_C3 SPI mode
System	NMI	55	B5	52	I	External non-maskable interrupt
	RST#	53	D5	57	I	External master reset (active low)
	DSM1[OUT]	20	FA	26	O	DSM1 output
Thermal	TEMP1[OUT]	N/A	N/A	1 bit	–	QFN package exposed thermal pad. TI recommends connection to VDD.

Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO. ⁽¹⁾			SIGNAL TYPE ⁽²⁾	DESCRIPTION
		P2	ZMH	R00		
T/Q2	RM_TAF1	29	G0	NA	IO	Reset/trigger for IAT CCR1 capture. CCR1A input, compare Out1
	IA1_0	30	IA	17	IO	IA1 CCR0 capture. CCR0A input, compare Out0
	IA2_0	31	IA	18	IO	IA2 CCR0 capture. CCR0A input, compare Out0
	TA2_1	79	TA	15	IO	TA2 CCR1 capture. CCR1A input, compare Out1
	TA2_2	71	TA	16	IO	TA2 CCR2 capture. CCR2A input, compare Out2
	TA2_3	59	EA	49	IO	TA2 CCR3 capture. CCR3A input, compare Out3
	TA2_4	14	ET	50	IO	TA2 CCR4 capture. CCR4A input, compare Out4
	T/Q2CLK	28	Q7	33	I	T/Q2 input clock
	TA3_0	24	NA	NA	IO	TA3 CCR0 capture. CCR0A input, compare Out0
	IA3_1	25	NA	NA	IO	IA3 CCR0 capture. CCR0A input, compare Out0
	TA3_2	40	NA	NA	IO	TA3 CCR2 capture. CCR2A input, compare Out2
	IA3_3	77	NA	NA	IO	IA3 CCR3 capture. CCR3A input, compare Out3
	IA3_4	75	NA	NA	IO	IA3 CCR4 capture. CCR4A input, compare Out4
	TA3TCLK	17	NA	NA	I	TA3 input mode
	LOCKEVAL	6	LO	31	I	lockstep eval – all I/Os, all UARTs mode
UART	UC0RXD	7	EA	4	O	Transmit data – eUSCI_A0 UART mode
	UC0TXD	50	NA	NA	I	Receive data – all I/Os, all UARTs mode
	UC0RXD	29	NA	NA	O	Transmit data – eUSCI_A3 UART mode

4.4 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and diagrams of the multiplexed parts, see [Section 5.12](#).

4.5 Buffer Types

[Table 4-3](#) describes the buffer types that are referenced in [Table 4-1](#).

Table 4-3. Buffer Type

BUFFER TYPE (STANDARD)	NOMINAL VOLTAGE	HYSTERESIS	PULL-UP/PD	NOMINAL PU OR PD STRENGTH (μ A)	OUTPUT DRIVE STRENGTH (mA)	OTHER CHARACTERISTICS
Analog ⁽¹⁾	0.0 V	N	N/A	N/A	N/A	See analog module in Specifications for details
HVCMOS	1.30 V	Y	N/A	N/A	See Typical Characteristics	
LVCMOS	0.0 V	Y/R	Programmable	See Typical Characteristics	See Typical Characteristics	
Tri-state (LVCMOS) ⁽²⁾	0.0 V	N	N/A	N/A	N/A	SVSHH enables hysteresis on LVCMOS
Tri-state (LVCMOS) ⁽²⁾	0.0 V	N	N/A	N/A	N/A	
Power-TWSS and AVSS ⁽³⁾	0.0 V	N	N/A	N/A	N/A	

(1) This is a switch, not a buffer.

(2) Only for input pins.

(3) This is a supply rail, not a buffer.

4.5 Connection for Unused Pins

[Table 4-4](#) lists the correct termination of all unused pins.

Table 4-4. Connection for Unused Pins⁽¹⁾

PIN	POTENTIAL	COMMENT
AVSS	DVSS	
AVSS	DVSS	
Px0 to Px7	Open	Set to port function, output direction, and leave unconnected on the PC board.
TEST/SM	DVSS or VDD	4-k Ω pulldown with 1.5-k Ω pullup.
UART0	Open	The UART0 pin is shared with general-purpose I/O function (PJ.4). If not being used, this pin should be set to port function and pulled down.
PJ.4/TD/SWD	DVSS or VDD	The PJ.4/TD/SWD pin is shared with general-purpose I/O function (PJ.4). If not being used, this pin should be set to port function, output direction, and pulled down externally.
RAMO/TVSS	DVSS or VDD	This pin should be pulled up externally.
RAMO/KICK	DVSS or VDD	This pin should be pulled down externally.

(1) For any unused pin with a secondary function that is shared with general-purpose I/O, follow the guidelines for the Px0 to Px7 pins.

5 Specifications

5.1 Absolute Maximum Ratings⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	MIN	MAX	UNIT
Voltage applied at DVDD and AVDD pins to V_{DD}	-0.3	+17	V
Voltage difference between DVDD and AVDD pins ⁽²⁾		±0.3	V
Voltage applied to any pin ⁽³⁾	-0.3	$V_{DD} + 0.3$ V (+17 V MAX)	V
Diode current at any diode pin ⁽⁴⁾		±2	mA
Storage temperature, T_{STG} ⁽⁵⁾	-40	125	°C
Maximum junction temperature, T_J		95	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.
- (2) Voltage difference between DVDD and AVDD exceeding the specified limits may cause malfunction of the device.
- (3) All voltages referenced to V_{SS} .
- (4) High-temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak solder temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

Type of electrostatic discharge	Human body model (HBM) per ANSI/ESD S8.1E-1987 ⁽¹⁾	VALUE	UNIT
	Charged device model (CDM) per JEDEC specification JESD22-C10 ⁽²⁾	+1000	V
		±200	

- (1) JEDEC document JEP155 states that 100-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
- (2) All pins except DVSS3 pass HBM up to ±1000 V. The DVSS3 pin is used for TI internal test purposes. Control the DVSS3 pin to supply current on the customer application board.
- (3) JEDEC document JEP157 states that 200-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±200 V may actually have higher performance.

5.3 Recommended Operating Conditions

Typical data are based on $V_{CC} = 3.0$ V, $T_A = 25^\circ\text{C}$ (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V _{DD}	Supply voltage (applied at DVDD and AVDD pins) ⁽¹⁾	1.7		3.7	V
	At power up (with normal V _{DD} support) ⁽²⁾	1.7		3.7	
	Normal operation with minimal V _{DD} support ⁽³⁾	1.55		3.7	
V _{SS}	Supply voltage on all I/O pins and AVSS pins		0		V
I _{DDSD}	Standby current into the V _{DD} pins ⁽⁴⁾			100	µA
f _{CLK}	Frequency of the CPU and all I/O clocks in the system ⁽⁵⁾	0		48	MHz
T _A	Operating free-air temperature	-40		85	°C
T _J	Operating junction temperature	-40		85	°C

- (1) TI recommends providing AV_{DD} and DV_{DD} from the same source. A maximum difference of 100 mV between AV_{DD} and DV_{DD} can be tolerated during power up and operation. See Section 5.4 for decoupling capacitor recommendations.
- (2) Supply voltage must not decrease faster than 150 mV/µs. Excess decrease can cause the MUX2 pin to trigger a reset even with the recommended supply voltage range.
- (3) Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.
- (4) Does not include I/O currents driven by application-specific loads.
- (5) Operating frequency may require the device to be screened with wall clock. See Section 5.6 for further details.

5.6 Operating Mode CPU Frequency Ranges⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	OPERATING MODE	DESCRIPTION	F_CPU		UNIT
			MIN	MAX	
f _{clk_LDO_VCORE0}	AM_LDO_VCORE0	Normal performance mode with LDO as the active regulator	0	24	MHz
f _{clk_LDO_VCORE1}	AM_LDO_VCORE1	High performance mode with LDO as the active regulator	0	40	MHz
f _{clk_DCO_VCORE0}	AM_DCO_VCORE0	Normal performance mode with DCO as the active regulator	0	24	MHz
f _{clk_DCO_VCORE1}	AM_DCO_VCORE1	High performance mode with DCO as the active regulator	0	40	MHz
f _{clk_LP_VCORE0}	AM_LP_VCORE0	Low frequency mode with LDO as the active regulator	0	128	KHz
f _{clk_LP_VCORE1}	AM_LP_VCORE1	Low frequency mode with LDO as the active regulator	0	128	KHz

(1) LDO can be operated at the same frequency as DCO.

5.7 Operating Mode Peripheral Frequency Ranges

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	OPERATING MODE	DESCRIPTION	MIN	MAX	UNIT
f _{clk_per_VCORE0}	AM_LDO_VCORE0	Peripheral frequency range in LDO or DCO based active or LPNO modes for VCORE0	0	12	MHz
	AM_DCO_VCORE0				
	LPNO_LDO_VCORE0				
f _{clk_per_VCORE1}	AM_LDO_VCORE1	Peripheral frequency range in LDO or DCO based active or LPNO modes for VCORE1	0	24	MHz
	AM_DCO_VCORE1				
	LPNO_DCO_VCORE1				
f _{clk_per_LP}	AM_LP_VCORE0	Peripheral frequency range in low-frequency active or low frequency LPNO modes for VCORE0 and VCORE1	0	128	KHz
	AM_LP_VCORE1				
	LPNO_LP_VCORE0				
f _{clk_RTCT} ⁽¹⁾	LPNO_VCORE0	Peripheral frequency in RTCT mode in VCORE0 and VCORE1	0	32,768	KHz
f _{clk_WDT} ⁽¹⁾	LPNO_VCORE1	Peripheral frequency in WDT mode	0	32,768	KHz

(1) Only RTCT and WDT can be active.

5.8 Operating Mode Execution Frequency vs Flash Wait-State Requirements

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	NUMBER OF FLASH WAIT STATES	FLASH READ MODE	MAXIMUM SUPPORTED MCLK FREQUENCY ⁽¹⁾ (4)		UNIT
			AM_LDO_VDDREF, AM_DCCDC_VDDREF	AM_LDO_VDDREF, AM_DCCDC_VDDREF	
Flash APP WAIT	0	Normal read mode	16	24	KHz
Flash APP WAIT	1	Normal read mode	24	48	KHz
Flash APP WAIT	0	Other read modes ⁽²⁾	8	32	KHz
Flash APP WAIT	1	Other read modes ⁽²⁾	16	24	KHz
Flash APP WAIT	2	Other read modes ⁽²⁾	24	36	KHz
Flash APP WAIT	3	Other read modes ⁽²⁾	24	48	KHz

- (1) Violation of the maximum frequency limitation for a given wait state configuration results in nondeterministic data on instruction fetches from the flash memory.
(2) In low frequency active modes, the flash can always be accessed with zero wait states, because the maximum MCLK frequency is limited to 175 kHz.
(3) Other read modes refer to Read Mode 0, Read Mode 1, Program Verify, and Erase Verify.

5.9 Current Consumption During Device Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)^{(1) (2) (3)}

PARAMETER		V _{CC}	MIN	TYP	MAX	UNIT
I _{CC} (1)	Current through device reset	1.7 V		5.10		μA
		3.0 V		620	850	μA

- (1) Device held in reset through RSTnM pin.
(2) Current measured into V_{CC}.
(3) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sink any current.

5.10 Current Consumption in LDO-Based Active Modes – Dhrystone 2.1 Program

over recommended operating free-air temperature (unless otherwise noted)^{(1) (2) (3) (4) (5)}

PARAMETER	EXECUTION MODE ⁽¹⁾	V _{CC}	MCLK = 1 MHz				MCLK = 5 MHz				MCLK = 10 MHz				MCLK = 20 MHz				MCLK = 40 MHz				UNIT
			TYP	MIN	TYP	MAX	TYP	MIN	TYP	MAX	TYP	MIN	TYP	MAX	TYP	MIN	TYP	MAX	TYP	MIN	TYP	MAX	
I _{CC} (2) (3) (4) (5)	Flash	1.8 V	240	100	240	300	240	100	240	300	240	100	240	300	240	100	240	300	240	100	240	300	μA
I _{CC} (2) (3) (4) (5)	Flash	1.8 V	410	100	410	500	410	100	410	500	410	100	410	500	410	100	410	500	410	100	410	500	μA
I _{CC} (2) (3) (4) (5)	SRAM	1.8 V	240	100	240	300	240	100	240	300	240	100	240	300	240	100	240	300	240	100	240	300	μA
I _{CC} (2) (3) (4) (5)	SRAM	3.0 V	420	100	420	500	420	100	420	500	420	100	420	500	420	100	420	500	420	100	420	500	μA

- (1) MCLK sourced by HCC0.
(2) Current measured into V_{CC}.
(3) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sink any current.
(4) All SRAM banks kept active.
(5) All peripherals are inactive.
(6) Device executing the Dhrystone 2.1 program. Code execution from both flash and SRAM is allowed.
(7) Flash configured to minimum wait states required to support operation at given frequency and core voltage level.
(8) Instructions and data cache sizes are 64KB (BL0) + 64KB (BL1) = 128KB.
(9) Device executing the Dhrystone 2.1 program. Code execution from SRAM. Stack and data in SRAM.

5.11 Current Consumption in DC-DC-Based Active Modes – Dhrystone 2.1 Program

over recommended operating free-air temperature (unless otherwise noted) ⁽¹⁾ ⁽²⁾ ⁽³⁾ ⁽⁴⁾ ⁽⁵⁾

PARAMETER	EXECUTION MEMORY	V _{CC}	MCLK = 1 MHz		MCLK = 0 MHz		MCLK = 7.68 MHz		MCLK = 24 MHz		MCLK = 24 MHz		MCLK = 32 MHz		MCLK = 40 MHz		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I _{DD} (no outputs, I/O ⁽⁶⁾)	Flash	3.0 V	40	475	20	100	0.5	170	200	200							μA
I _{DD} (no outputs, I/O ⁽⁶⁾)	Flash	3.0 V	40	500	10	100	0.5	210	200	200	300	170	600	600	470	500	μA
I _{DD} (no outputs, I/O ⁽⁶⁾)	SRAM	3.0 V	270	150	50	50	100	100	100	100							μA
I _{DD} (no outputs, I/O ⁽⁶⁾)	SRAM	3.0 V	280	170	100	60	100	100	100	100	100	100	100	100	100	100	μA

- (1) MCLK sourced by DCO.
- (2) Current measured into V_{CC}.
- (3) All other I/O pins tied to 0 V or V_{CC}. Outputs do not source or sink any current.
- (4) All GR/IO modules are active.
- (5) All peripherals are inactive.
- (6) Device executing the Dhrystone 2.1 program. Code execution from Flash. Stack and data in SRAM.
- (7) Flash configured to minimum wait states required for support operation at given frequency and core voltage level.
- (8) Flash instruction and data buffers are enabled (BUF1 = BUF0 = 1).
- (9) Device executing the Dhrystone 2.1 program. Code execution from SRAM. Stack and data in SRAM.

5.12 Current Consumption in Low-Frequency Active Modes – Dhrystone 2.1 Program

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) ⁽¹⁾ ⁽²⁾ ⁽³⁾ ⁽⁴⁾ ⁽⁵⁾

PARAMETER	EXECUTION MEMORY	V _{CC}	-40°C		25°C		55°C		85°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I _{DD} (no outputs, I/O ⁽⁶⁾)	Flash	2.2 V	75		80		95		115		μA
I _{DD} (no outputs, I/O ⁽⁶⁾)		3.0 V	75		80	100	95		115	200	
I _{DD} (no outputs, I/O ⁽⁶⁾)	Flash	2.2 V	70		85		105		125		μA
I _{DD} (no outputs, I/O ⁽⁶⁾)		3.0 V	80		85	100	105		115	200	
I _{DD} (no outputs, I/O ⁽⁶⁾)	SRAM	2.2 V	60		70		90		100		μA
I _{DD} (no outputs, I/O ⁽⁶⁾)		3.0 V	70		75	90	90		105	180	
I _{DD} (no outputs, I/O ⁽⁶⁾)	SRAM	2.2 V	70		77		95		117		μA
I _{DD} (no outputs, I/O ⁽⁶⁾)		3.0 V	70		90	100	100		120	200	

- (1) Current measured into V_{CC}.
- (2) All other I/O pins tied to 0 V or V_{CC}. Outputs do not source or sink any current.
- (3) MCLK is 100 kHz, wait states 0, execution by DCO at 100 kHz.
- (4) All peripherals are inactive.
- (5) SRAM banks 0 and 1 enabled for execution from Flash, and SRAM bank 2 to 3 enabled for execution from SRAM.
- (6) Flash configured to 0 wait states.
- (7) Device executing the Dhrystone 2.1 program. Code execution from Flash. Stack and data in SRAM.
- (8) Flash instruction and data buffers are enabled (BUF1 = BUF0 = 1).
- (9) Device executing the Dhrystone 2.1 program. Code execution from SRAM. Stack and data in SRAM.

5.13 Typical Characteristics of Active Mode Currents for CoreMark Program

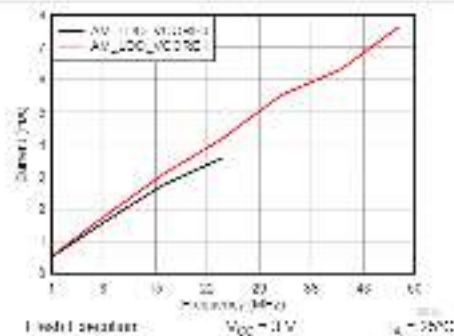


Figure 5-1. Frequency vs. Current Consumption

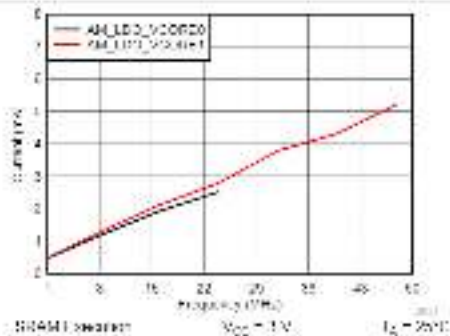


Figure 5-2. Frequency vs. Current Consumption

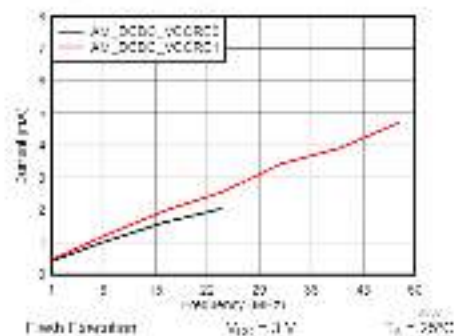


Figure 5-3. Frequency vs. Current Consumption

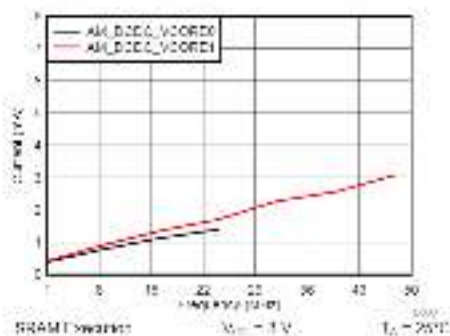


Figure 5-4. Frequency vs. Current Consumption

5.14 Typical Characteristics of Active Mode Currents for Prime Number Program

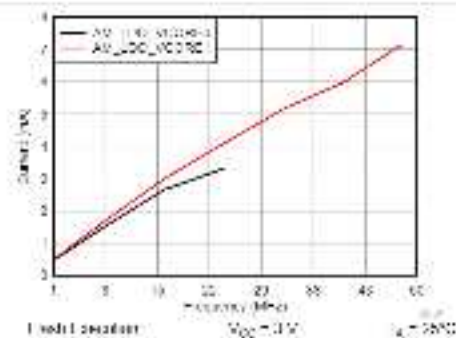


Figure 5-5. Frequency vs. Current Consumption

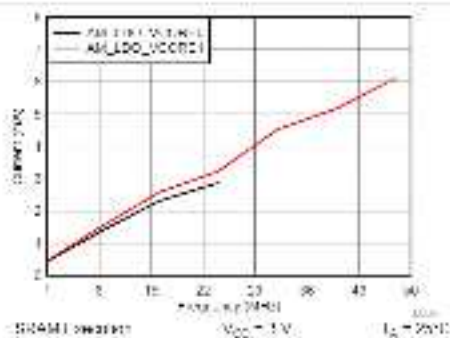


Figure 5-6. Frequency vs. Current Consumption

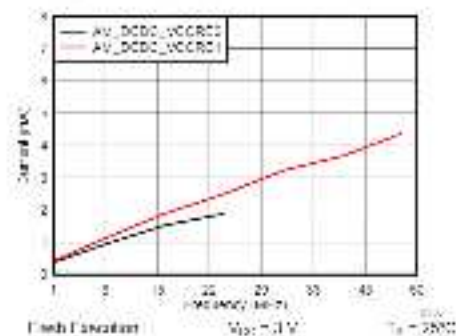


Figure 5-7. Frequency vs. Current Consumption

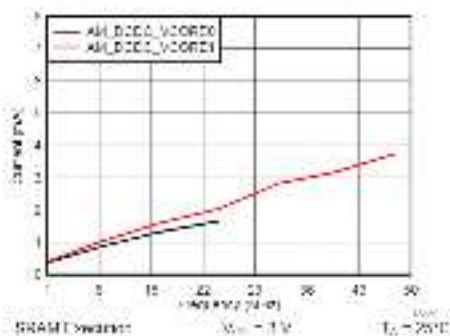


Figure 5-8. Frequency vs. Current Consumption

5.15 Typical Characteristics of Active Mode Currents for Fibonacci Program

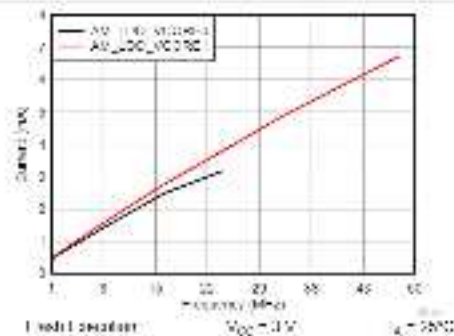


Figure 5-8. Frequency vs Current Consumption

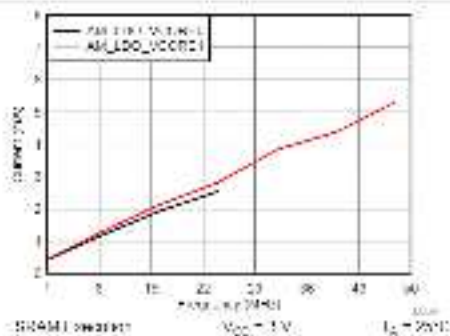


Figure 5-9. Frequency vs Current Consumption

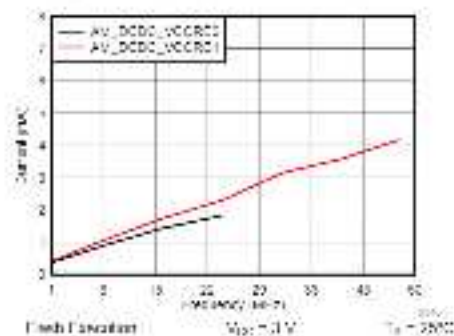


Figure 5-10. Frequency vs Current Consumption

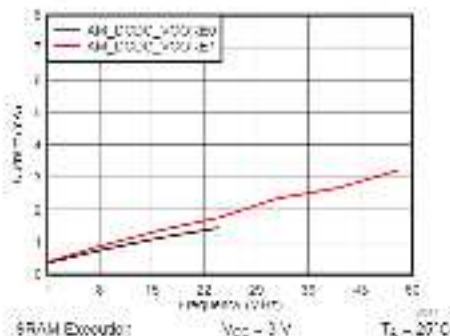


Figure 5-11. Frequency vs Current Consumption

5.16 Typical Characteristics of Active Mode Currents for While[1] Program

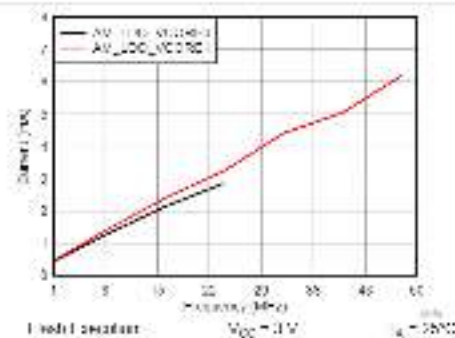


Figure 5-13. Frequency vs Current Consumption

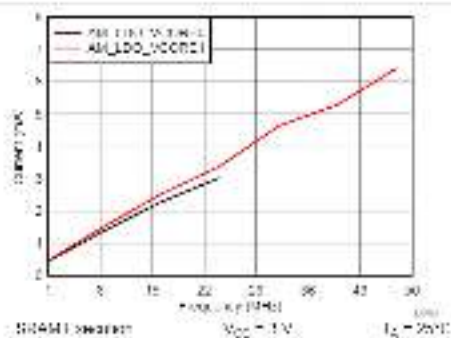


Figure 5-14. Frequency vs Current Consumption

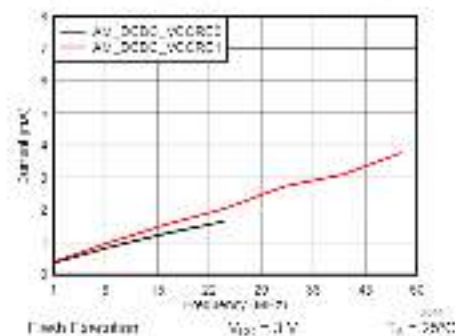


Figure 5-15. Frequency vs Current Consumption

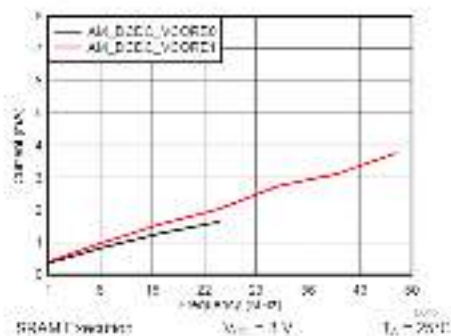


Figure 5-16. Frequency vs Current Consumption

5.17 Typical Characteristics of Low-Frequency Active Mode Currents for CoreMark Program

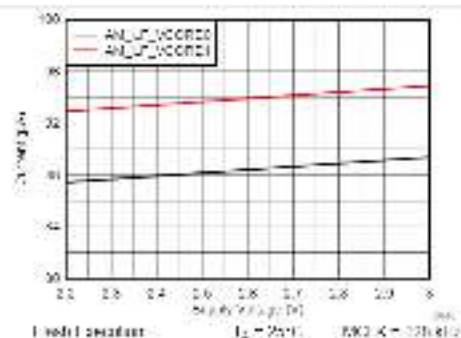


Figure 5-17. Supply Voltage vs. Current Consumption

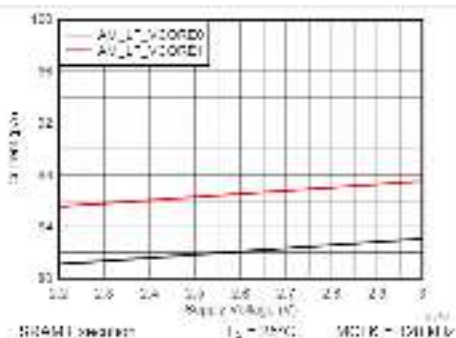


Figure 5-18. Supply Voltage vs. Current Consumption

5.18 Current Consumption in LDO-Based LPM0 Modes

 over recommended operating free-air temperature (unless otherwise noted)⁽¹⁾ (2) (3) (4) (5) (6)

PARAMETER	V _{DD}	MCLK = 1 MHz		MCLK = 5 MHz		MCLK = 12 MHz		MCLK = 24 MHz		MCLK = 32 MHz		MCLK = 40 MHz		MCLK = 48 MHz		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I _{DD} (typical)	2.2 V	290	400	400	500	500	720	720	800							μA
	3.0 V	290	400	400	500	500	720	720	800							
I _{DD} (maximum)	2.2 V	800	800	800	800	800	800	800	800	800	800	800	800	800	800	μA
	3.0 V	900	900	900	900	900	900	900	900	900	900	900	900	900	900	

(1) MCLK sourced by HCLK.

 (2) Current measured into V_{DD}.

 (3) All other inputs tied to 0 V or V_{DD}. Outputs do not source or sink any current.

(4) CPU is off. Flash and SRAM not accessed.

(5) All I/O pins are in high-impedance.

(6) All peripherals are inactive.

5.19 Current Consumption in DC-DC-Based LPM0 Modes

 over recommended operating free-air temperature (unless otherwise noted)⁽¹⁾ (2) (3) (4) (5) (6)

PARAMETER	V _{DD}	MCLK = 1 MHz		MCLK = 5 MHz		MCLK = 12 MHz		MCLK = 24 MHz		MCLK = 32 MHz		MCLK = 40 MHz		MCLK = 48 MHz		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I _{DD} (typical)	2.2 V	290	400	400	500	500	800	800	800							μA
	3.0 V	300	400	400	500	500	800	800	800							
I _{DD} (maximum)	2.2 V	900	900	900	900	900	900	900	900	900	900	900	900	900	900	μA
	3.0 V	900	900	900	900	900	900	900	900	900	900	900	900	900	900	

(1) MCLK sourced by DCDC.

 (2) Current measured into V_{DD}.

 (3) All other inputs tied to 0 V or V_{DD}. Outputs do not source or sink any current.

(4) CPU is off. Flash and SRAM not accessed.

(5) All I/O pins are in high-impedance.

(6) All peripherals are inactive.

5.20 Current Consumption in Low-Frequency LPM0 Modes

 over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾ (2) (3) (4) (5) (6)

PARAMETER	V _{DD}	-40°C		0°C		60°C		85°C		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I _{DD} (typical)	2.2 V	35		60		70		94		μA
	3.0 V	64		66	72	81		97	107	
I _{DD} (typical)	2.2 V	60		60		84		104		μA
	3.0 V	60		60	80	87		107	220	

 (1) Current measured into V_{DD}.

 (2) All other inputs tied to 0 V or V_{DD}. Outputs do not source or sink any current.

(3) MCLK, HREF, K, and HREF, K sourced by HREF at 1 MHz.

(4) All peripherals are inactive.

(5) Bank 0 and SRAM0 are powered down.

(6) CPU is off. Flash and SRAM not accessed.

5.21 Current Consumption in LPM3, LPM4 Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾ (2) (3) (4) (5) (6)

PARAMETER	V _{CC}	-40°C		25°C		80°C		85°C		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I _{core} (wake-up) (4) (5)	2.2 V	0.52		0.61		1.11		1.43		μA
	3.0 V	0.54		0.60	0.85	1.13		2.40	5	
I _{core} (power awake) (4) (5)	2.2 V	0.65		1.07		1.55		1.85		μA
	3.0 V	0.66		1.16	1.39	1.54		2.95	5.0	
I _{core} (mode Lpm3) (4) (5)	2.2 V	0.72		0.93		1.47		2.03		μA
	3.0 V	0.75		0.95	1.28	1.5		2.94	5	
I _{core} (mode Lpm4) (4) (5)	2.2 V	1.04		1.3		1.87		3.34		μA
	3.0 V	1.14		1.4	1.7	1.95		3.44	6.5	
I _{core} (mode TM) (4)	2.2 V	0.57		0.45		0.60		2.15		μA
	3.0 V	0.4		0.7	0.65	0.8		2.3	1.0	
I _{core} (wake) (4)	2.2 V	0.55		0.7		1.2		1.54		μA
	3.0 V	0.56		0.72	0.98	1.23		2.0	5.0	

- (1) Current measured into V_{CC}.
 (2) All other inputs tied to 0 V or V_{CC}. Outputs do not source or sink any current.
 (3) CPU is off and flash is powered down.
 (4) Bank 0 of SRAM retained, all other banks are powered down.
 (5) See Table 3-47 for details on additional current consumed for each extra Bank that is enabled for retention.
 (6) SRAM is disabled.
 (7) RTC sourced by LPM3. Effective load capacitance of LF crystal is 3.7 pF.
 (8) WDT module is disabled.
 (9) RTC sourced by REF0.
 (10) LPTC and WDT modules disabled.

5.22 Current Consumption in LPM3.5, LPM4.5 Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾ (2)

PARAMETER	V _{CC}	-40°C		25°C		80°C		85°C		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I _{core} (wake) (4) (5) (6) (7)	2.2 V	0.48		0.6		1.07		1.35		μA
	3.0 V	0.5		0.63	0.87	1.1		2.34	4.8	
I _{core} (power awake) (4) (5) (6) (7)	2.2 V	0.52		1.03		1.52		2.01		μA
	3.0 V	0.60		1.13	1.3	1.51		3.4	5.5	
I _{core} (PM3)	2.2 V	10		20		45		120		μA
	3.0 V	10		20	30	50		100	100	

- (1) Current measured into V_{CC}.
 (2) All other inputs tied to 0 V or V_{CC}. Outputs do not source or sink any current.
 (3) CPU is off and flash is powered down.
 (4) Bank 0 of SRAM retained, all other banks powered down.
 (5) LPTC sourced by LPM3. Effective load capacitance of LF crystal is 3.7 pF.
 (6) WDT module is disabled.
 (7) SRAM is disabled.
 (8) RTC sourced by REF0.
 (9) No core wakeup, CPU, flash, and all banks of SRAM are powered down.

5.23 Current Consumption of Digital Peripherals

 (see recommended ranges of supply voltage and operating frequency (unless otherwise noted))⁽¹⁾

PARAMETER	TEST CONDITIONS	TYP	MAX	UNIT
I _{mpu_A}	Timer_A configured as PWM timer with 50% duty cycle	5		µA/V _{DD}
I _{mpu_B}	TimerB2 enabled	1.5		µA/V _{DD}
I _{uwr}	US0C_A configured in URT mode	0.5		µA/V _{DD}
I _{uwr}	US0C_A configured in RPT mode (no data)	5		µA/V _{DD}
I _{uwr}	US0C_B configured in RPT mode (no data)	2		µA/V _{DD}
I _{uwr_A}	WOT_A configured in interrupt mode	6		µA/V _{DD}
I _{uwr_B}	WOT_B enabled and disabled from 0.4MHz (10K)	100		nA
I _{uwr_C}	WOT_C enabled	10		µA/V _{DD}
I _{uwr_D}	WOT_D enabled	2		µA/V _{DD}

 (1) Measured with V_{DDIOH} = 1.2 V

5.24 Thermal Resistance Characteristic

PARAMETER	TEST CONDITIONS	PACKAGE	VALUE ⁽¹⁾	UNIT
R _{ja}	Junction-to-ambient thermal resistance: still air ⁽²⁾	LQFP-100 (PZ)	90.0	°C/W
R _{ja(top)}	Junction-to-board (top) thermal resistance ⁽³⁾		9.7	°C/W
R _{ja(b)}	Junction-to-board thermal resistance ⁽³⁾		27.2	°C/W
Ψ _{jt}	Junction-to-board thermal characterization parameter		37.8	°C/W
Ψ _{jt}	Junction-to-top thermal characterization parameter		3.3	°C/W
R _{junction}	Junction-to-case (bottom) thermal resistance ⁽⁴⁾		NA	°C/W
R _{jc}	Junction-to-case thermal resistance: still air ⁽⁵⁾		51.1	°C/W
R _{junction}	Junction-to-case (top) thermal resistance ⁽⁶⁾		26.7	°C/W
R _{jb}	Junction-to-board thermal resistance ⁽⁷⁾		22.6	°C/W
Ψ _{jt}	Junction-to-board thermal characterization parameter		27.0	°C/W
R _{ja}	Junction-to-ambient thermal characterization parameter	VQFN (64) (RSC)	0.5	°C/W
R _{ja(top)}	Junction-to-board (bottom) thermal resistance ⁽⁸⁾		NA	°C/W
R _{ja(b)}	Junction-to-board thermal resistance: still air ⁽⁹⁾		20.4	°C/W
R _{ja(top)}	Junction-to-case (top) thermal resistance ⁽¹⁰⁾		1.0	°C/W
R _{jc}	Junction-to-case thermal resistance ⁽¹¹⁾		5.5	°C/W
Ψ _{jt}	Junction-to-board thermal characterization parameter		8.2	°C/W
Ψ _{jt}	Junction-to-top thermal characterization parameter		0.2	°C/W
R _{junction}	Junction-to-case (bottom) thermal resistance ⁽¹²⁾		1.2	°C/W

 (1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Annot.](#)

(2) NA = not applicable

(3) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC standard High K board, as specified in J-ESD1-7, in an environment described in J-ESD1-7.

(4) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI-STD-4 standard G33444.

(5) The junction-to-board thermal resistance is obtained by simulating it on a reference without any cold plate boards to control the PCB temperature. No reference is JEDEC14-0.

(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed bottom pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI-STD-4 standard G33444.

5.25 Timing and Switching Characteristics

5.25.1 Reset Timing

Table 5-1 lists the latencies to recover from different types of resets.

Table 5-1. Reset Recovery Latencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) ⁽¹⁾

PARAMETER	MIN	TYP	MAX	UNIT
t_{wakeup}	Latency from release of soft reset to first CPU instruction fetch	5		KCLK cycles
t_{wakeup}	Latency from release of hard reset to release of soft reset	20		KCLK cycles
t_{wakeup}	Latency from release of device POR to release of hard reset	15	35	µs
$t_{wakeup,por}$	Latency from cold power-up condition to release of device POR, $C_{boot} = 100$ nF	500	910	µs
$t_{wakeup,por}$	Latency from cold power-up condition to release of device POR, $C_{boot} = 4.7$ µF	500	910	µs

(1) See Section 6.6.1 for details on the various classes of resets on the device.

Table 5-2 lists the latencies to recover from an external reset applied on RSTn pin.

Table 5-2. External Reset Recovery Latencies⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{wakeup}	External reset applied when device is in LDO or LDO-DC based active modes, KCLK = 1 to 48 MHz		5	µs
$t_{wakeup,125kHz}$	External reset applied when device is in low-frequency active modes, KCLK = 125 kHz		5.5	µs
$t_{wakeup,30dB}$	External reset applied when device is in low-frequency active modes, KCLK = 32 MHz ± 3%		6.0	µs
t_{wakeup}	External reset applied when device is in LDO or DC-DC based LPM0 modes, KCLK = 1 to 48 MHz		5	µs
$t_{wakeup,125kHz}$	External reset applied when device is in low-frequency LPM0 modes, KCLK = 125 kHz		5.5	µs
$t_{wakeup,30dB}$	External reset applied when device is in low-frequency LPM0 modes, KCLK = 32 MHz ± 3%		6.5	µs
$t_{wakeup,active}$	External reset applied when device is in LPM3 or LPM4 modes, KCLK = 24 or 48 MHz while entering LPM3 or LPM4 modes		5	µs
t_{wakeup}	External reset applied when device is in LPM3 or LPM4 modes		5	µs

(1) External reset is applied on RSTn pin, and the latency is measured from release of external reset to start of user application code.

5.2.5.2 Mode Transition Timing

Table 5-3 lists the latencies required to change between different active modes.

Table 5-3. Active Mode Transition Latencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	ORIGINAL OPERATING MODE	FINAL OPERATING MODE	TEST CONDITIONS	TYP	MAX	UNIT
t_{PM_WakeUp}	Power Off	AM_LDO_VCORE0	From V_{DD} reaching 1.71 V to start of core register access		0	ms
t_{WakeUp_LDO}	AM_LDO_VCORE0	AM_LDO_VCORE1	Transition from AM_LDO_VCORE0 to AM_LDO_VCORE1 MCLK frequency = 24 MHz	100	150	μ s
t_{WakeUp_LDO2}	AM_LDO_VCORE0	AM_LDO_VCORE2	Transition from AM_LDO_VCORE0 to AM_LDO_VCORE2 MCLK frequency = 24 MHz	4	5	μ s
t_{WakeUp_VDDIO0}	AM_LDO_VCORE0	AM_DDC0_VCORE0	Transition from AM_LDO_VCORE0 to AM_DDC0_VCORE0 MCLK frequency = 24 MHz	20	30	μ s
t_{WakeUp_VDDIO1}	AM_DDC0_VCORE0	AM_LDO_VCORE0	Transition from AM_DDC0_VCORE0 to AM_LDO_VCORE0 MCLK frequency = 24 MHz	10	15	μ s
t_{WakeUp_VDDIO1}	AM_LDO_VCORE1	AM_DDC0_VCORE1	Transition from AM_LDO_VCORE1 to AM_DDC0_VCORE1 MCLK frequency = 48 MHz	20	30	μ s
t_{WakeUp_VDDIO1}	AM_DDC0_VCORE1	AM_LDO_VCORE1	Transition from AM_DDC0_VCORE1 to AM_LDO_VCORE1 MCLK frequency = 48 MHz	10	15	μ s
t_{WakeUp_LDO2}	AM_LDO_VCORE0	AM_LF_VCORE0	Transition from AM_LDO_VCORE0 to AM_LF_VCORE0 SELN = 2, REFCLK frequency = 128 kHz	20	100	μ s
t_{WakeUp_LDO1}	AM_LF_VCORE0	AM_LF_VCORE1	Transition from AM_LF_VCORE0 to AM_LF_VCORE1 SELN = 2, REFCLK frequency = 128 kHz	50	100	μ s
t_{WakeUp_LDO1}	AM_LF_VCORE1	AM_LF_VCORE0	Transition from AM_LF_VCORE1 to AM_LF_VCORE0 SELN = 2, REFCLK frequency = 128 kHz	50	100	μ s
t_{WakeUp_LDO1}	AM_LF_VCORE1	AM_LF_VCORE1	Transition from AM_LF_VCORE1 to AM_LF_VCORE1 SELN = 2, REFCLK frequency = 128 kHz	50	100	μ s

Table 5-4 lists the latencies required to change between different active and LPM0 modes.

Table 5-4. LPM0 Mode Transition Latencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	ORIGINAL OPERATING MODE	FINAL OPERATING MODE	TEST CONDITIONS	TYPE	MAX	UNIT
$t_{wake_core0}^{(1)}$	AM_LDO_VCORE0	LPM0_LDO_VCORE0	Transition from AM_LDO_VCORE0 or AM_LDO_VCORE1 to LPM0_LDO_VCORE0 or LPM0_LDO_VCORE1	1		WOLK cycles
$t_{wake_core1}^{(1)}$	LPM0_LDO_VCORE0	AM_LDO_VCORE0	Transition from LPM0_LDO_VCORE0 to AM_LDO_VCORE0 or AM_LDO_VCORE1 through D1 interrupt	2	4	WOLK cycles
$t_{wake_core0}^{(1)}$	AM_DDC0_VCORE0	LPM0_DDC0_VCORE0	Transition from AM_DDC0_VCORE0 or AM_DDC0_VCORE1 to LPM0_DDC0_VCORE0 or LPM0_DDC0_VCORE1	1		WOLK cycles
$t_{wake_core1}^{(1)}$	LPM0_DDC0_VCORE0	AM_DDC0_VCORE0	Transition from LPM0_DDC0_VCORE0 to AM_DDC0_VCORE0 or AM_DDC0_VCORE1 through D0 interrupt	2	4	WOLK cycles
$t_{wake_core0}^{(1)}$	AM_LF_VCORE0	LPM0_LF_VCORE0	Transition from AM_LF_VCORE0 or AM_LF_VCORE1 to LPM0_LF_VCORE0 or LPM0_LF_VCORE1	1		WOLK cycles
$t_{wake_core1}^{(1)}$	LPM0_LF_VCORE0	AM_LF_VCORE0	Transition from LPM0_LF_VCORE0 or AM_LF_VCORE1 through I/O interrupt	2	4	WOLK cycles

(1) This is the latency between assertion of VTI interrupt by CPU1 to assertion of SLEEPING signal at CPU0 output.
(2) This is the latency between I/O interrupt event to deassertion of SLEEPING signal at CPU0 output.

Table 5-5 lists the latencies required to change between different active modes and LPM3 or LPM4 modes.

Table 5-5. LPM3, LPM4 Mode Transition Latencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	ORIGINAL OPERATING MODE	FINAL OPERATING MODE	TEST CONDITIONS	TYPE	MAX.	UNIT
$t_{wake_up_lpm3}^{(1)}$	AM_LDO_VDDREF	LPM3_LPM4_VDDREF	Transition from AM_LDO_VDDREF to LPM3 or LPM4 at VDDREF	SEV = 1 OSC frequency = 24 MHz	20	µs
$t_{wake_up_lpm3}^{(2)}$	LPM3_LPM4_VDDREF	AM_LDO_VDDREF	Transition from LPM3 or LPM4 at VDDREF to AM_LDO_VDDREF through wake-up event from any pin (see type A)	SEV = 2 OSC frequency = 24 MHz	8	µs
$t_{wake_up_lpm3}^{(2)}$	LPM3_LPM4_VDDREF	AM_LDO_VDDREF	Transition from LPM3 or LPM4 at VDDREF to AM_LDO_VDDREF through wake-up event from any pin (see type A) $GLUT1.DN = 1$	SEV = 2 OSC frequency = 24 MHz	9	µs
$t_{wake_up_lpm4}^{(1)}$	AM_LDO_VDDREF	LPM3_LPM4_VDDREF	Transition from AM_LDO_VDDREF to LPM3 or LPM4 at VDDREF	SEV = 2 OSC frequency = 48 MHz	21	µs
$t_{wake_up_lpm4}^{(2)}$	LPM3_LPM4_VDDREF	AM_LDO_VDDREF	Transition from LPM3 or LPM4 at VDDREF to AM_LDO_VDDREF through wake-up event from any pin (see type A)	SEV = 1 OSC frequency = 48 MHz	7.5	µs
$t_{wake_up_lpm4}^{(2)}$	LPM3_LPM4_VDDREF	AM_LDO_VDDREF	Transition from LPM3 or LPM4 at VDDREF to AM_LDO_VDDREF through wake-up event from any pin (see type A) $GLUT1.DN = 1$	SEV = 1 OSC frequency = 48 MHz	8	µs
$t_{wake_up_lpm4}^{(2)}$	AM_LDO_VDDREF	LPM3_LPM4_VDDREF	Transition from AM_LDO_VDDREF to LPM3 or LPM4 at VDDREF	SEV = 2, 9640 frequency = 125 kHz	210	µs
$t_{wake_up_lpm4}^{(2)}$	AM_LDO_VDDREF	LPM3_LPM4_VDDREF	Transition from AM_LDO_VDDREF to LPM3 or LPM4 at VDDREF	SEV = 2, 9640 frequency = 52.155 kHz	300	µs
$t_{wake_up_lpm4}^{(2)}$	LPM3_LPM4_VDDREF	AM_LDO_VDDREF	Transition from LPM3 or LPM4 at VDDREF to AM_LDO_VDDREF through wake-up event from any pin (see type A)	SEV = 1, 9640 frequency = 125 kHz	49	µs
$t_{wake_up_lpm4}^{(2)}$	LPM3_LPM4_VDDREF	AM_LDO_VDDREF	Transition from LPM3 or LPM4 at VDDREF to AM_LDO_VDDREF through wake-up event from any pin (see type A)	SEV = 1, 9640 frequency = 52.155 kHz	100	µs

- (1) This is the latency from VREF initialization executed by GPM to LPM3 or LPM4 and μ .
 (2) This is the latency from IO wake-up event to MCLK clock start at device pin.

Table 5-3 lists the latencies required to change to and from LPM3.5 and LPM4.5 modes.

Table 5-6. LPM3.5, LPM4.5 Mode Transition Latencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	ORIGINAL OPERATING MODE	FINAL OPERATING MODE	TEST CONDITIONS	TYP	MAX	UNIT
$t_{WFI_to_LPM3.5}^{(1)}$	AM_LDO_VDDIOHx	LPM3.5	Transition from AM_LDO_VDDIOHx to LDO_VDDIOHx in LPM3.5	25	30	μ s
$t_{WFI_to_LPM4.5}^{(1)}$	AM_LDO_VDDIOHx	LPM4.5	Transition from AM_LDO_VDDIOHx to LDO_VDDIOHx in LPM4.5	25	30	μ s
$t_{LPM3.5_to_WFI}^{(2)}$	AM_LDO_VDDIOHx	LPM3.5	Transition from AM_LDO_VDDIOHx to AM_LDO_VDDIOHx in LPM3.5	25	30	μ s
$t_{LPM4.5_to_WFI}^{(2)}$	AM_LDO_VDDIOHx	LPM4.5	Transition from AM_LDO_VDDIOHx to AM_LDO_VDDIOHx in LPM4.5	25	30	μ s
$t_{LPM3.5_to_LPM4.5}^{(3)}$	AM_LDO_VDDIOHx	LPM4.5	Transition from AM_LDO_VDDIOHx to AM_LDO_VDDIOHx in LPM4.5	25	30	μ s
$t_{LPM4.5_to_LPM3.5}^{(3)}$	AM_LDO_VDDIOHx	LPM3.5	Transition from AM_LDO_VDDIOHx to AM_LDO_VDDIOHx in LPM3.5	25	30	μ s
$t_{LPM3.5_to_LPM4.5_with_SWSM}^{(4)}$	LPM3.5	AM_LDO_VDDIOHx	Transition from LPM3.5 to AM_LDO_VDDIOHx SWSM enabled while in LPM3.5 C _{SWSM} = 100 nF	0.7	0.8	μ s
$t_{LPM4.5_to_LPM3.5_with_SWSM}^{(4)}$	LPM4.5	AM_LDO_VDDIOHx	Transition from LPM4.5 to AM_LDO_VDDIOHx SWSM enabled while in LPM4.5 C _{SWSM} = 100 nF	0.7	0.8	μ s
$t_{LPM3.5_to_LPM4.5_with_SWSM_and_LPM4.5}^{(4)}$	LPM3.5	AM_LDO_VDDIOHx	Transition from LPM3.5 to AM_LDO_VDDIOHx SWSM enabled while in LPM4.5 C _{SWSM} = 100 nF	1	1.1	μ s
$t_{LPM4.5_to_LPM3.5_with_SWSM_and_LPM3.5}^{(4)}$	LPM4.5	AM_LDO_VDDIOHx	Transition from LPM4.5 to AM_LDO_VDDIOHx SWSM enabled while in LPM3.5 C _{SWSM} = 100 nF	1	1.1	μ s

(1) This is the latency from WFI instruction execution by CPU to LPM3.5 mode entry.

(2) This is the latency from WFI instruction execution by CPU to LPM4.5 mode entry.

(3) This is the latency from WFI instruction execution to start of user application code.

(4) This is the latency from WFI instruction execution to start of user application code.

5.25.3 Clock Specifications

Table 5-7 lists the input requirement for the low-frequency crystal oscillator, LFXT.

Table 5-7. Low-Frequency Crystal Oscillator, LFXT, Recommended Operating Conditions

over operating free air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ESR	Crystal equivalent series resistance $f_{osc} = 32,768$ kHz	18	40	85	Ω
C_{load}	Capacitance from LFXT input to ground and from LFXT output to ground ⁽¹⁾	14	12	24	pF
C_{start}	Crystal start capacitance	0.0	0.5	1.0	pF
f_{osc}	Crystal nominal frequency	1	1	10	1

(1) Does not include board parasitics. This type also tested with additional capacitance for C_{load} .

Table 5-8 lists the characteristics of the low-frequency crystal oscillator, LFXT.

Table 5-8. Low-Frequency Crystal Oscillator, LFXT

over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{cc} (typ)	Current consumption ⁽¹⁾	f _{osc} = 32,768 kHz, LFXTRM = 0, LFXTRMSE = (1), C _{load} = 32 pF, Typical ESR and C _{start}	3.0 V	100		nA	
		f _{osc} = 32,768 kHz, LFXTRM = 0, LFXTRMSE = (1), C _{load} = 0 pF, Typical ESR and C _{start}		100			
		f _{osc} = 32,768 kHz, LFXTRM = 0, LFXTRMSE = (2), C _{load} = 8 pF, Typical ESR and C _{start}		150			
		f _{osc} = 32,768 kHz, LFXTRM = 0, LFXTRMSE = (1), C _{load} = 12 pF, Typical ESR and C _{start}		170			
f _{osc}	LFXT oscillator crystal frequency	LFXTBYPASS = 0 ⁽²⁾	32,768		kHz		
D _{LFXT}	LFXT oscillator duty cycle	f _{osc} = 32,768 kHz ⁽²⁾	30%		70%		
f _{osc,20k}	LFXT oscillator nominal square-wave output frequency	LFXTBYPASS = (1) (4)	10	32,768	50	kHz	
D _{LFXT,20k}	LFXT oscillator nominal square-wave output duty cycle	LFXTBYPASS = 1	30%		70%		
U _{A_osc}	Oscillator allowance for LF crystals ⁽³⁾	LFXTBYPASS = 0, LFXTRMSE = (1), f _{osc} = 32,768 kHz, C _{load} = 0 pF	200	240		mV	
		LFXTBYPASS = 0, LFXTRMSE = (3), f _{osc} = 32,768 kHz, C _{load} = 12 pF	300	340			

(1) Total current measured on both AVCC and DVCC supplies.

(2) Measured at 25°C.

(3) When LFXTBYPASS is set, LFXT outputs are automatically powered down. Input signal is a digital square wave with parameters defined in the 5-pin input/output timing section of this data sheet. Duty cycle may vary from 30% to 70%.

(4) Maximum frequency of operation of the entire device cannot be exceeded.

(5) Oscillator allowance is based on a safety factor of 5 for recommended crystals. The oscillator allowance is a function of the LFXT output voltage and the effective load. In general, capacitor oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:

- For LFXTRM = (0), $C_{load} = 0$ pF
- For LFXTRM = (1), 0.0 pF $\leq C_{load} \leq 0$ pF
- For LFXTRM = (2), 0 pF $\leq C_{load} \leq 10$ pF
- For LFXTRM = (3), 0.0 pF $\leq C_{load} \leq 12$ pF

Low-Frequency Crystal Oscillator, LFXT (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
C _{LOAD}	Intended load capacitance at LFXT1 terminal ⁽¹⁾ (1)			2		pF
C _{OUT}	Intended load capacitance at LFXTOUT terminal ⁽¹⁾ (2)			2		pF
t _{STARTUP}	Startup time ⁽³⁾	0.0 V		11		s
				1.0		s
f _{OSC}	Oscillator full frequency ⁽⁴⁾ (5)		1		0.1	MHz

- (1) This represents all the parasitic capacitance present at the LFXT1 and LFXTOUT terminals, respectively, including pads to bond and package capacitance. The effective load capacitance (C_L) can be computed as C_L = C_{OUT} + (C_{IN} + C_{OUT}) / 2, where C_{IN} and C_{OUT} are the total capacitance at the LFXT1 and LFXTOUT terminals, respectively.
- (2) Intended external capacitance at both terminals to meet the effective load capacitance specified by crystal manufacturer. Recommended effective load capacitance values supported are 5.1 pF, 6 pF, 9 pF, and 12 pF. Maximum shunt capacitance of 1.0 pF. Because the PCD adds additional capacitance, it must also be considered in the overall capacitance. TI recommends verifying that the recommended effective load capacitance of the selected crystal is met.
- (3) Does not include programmable start-up counter.
- (4) Frequencies above the MAX specified here do not set the fault flag. Frequencies in between the MIN and MAX specifications may set the flag. A static condition or stuck-at-fault condition will set the fault flag.
- (5) Measured with approved input frequency but also applies to operation with crystals.

Table 5-3 lists the input requirements for the high-frequency crystal oscillator, HFXT.

Table 5-3. High-Frequency Crystal Oscillator, HFXT, Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{OSC}	Crystal resonant frequency (resonance)	f _{osc} = 1 MHz to 60 MHz		75	150	°C
		f _{osc} = 14 MHz to 18 MHz		75	100	
		f _{osc} = 20 MHz to 26 MHz		70	80	
		f _{osc} = 30 MHz to 34 MHz		30	80	
		f _{osc} = 39 MHz to 42 MHz		20	70	
		f _{osc} = 42 MHz to 48 MHz		15	50	
V _{IN}	Capacitance from HFXT ⁺ input to ground and from HFXT ⁻ input to ground	f _{osc} = 1 MHz to 40 MHz	25	10	30	pF
C _{LOAD}	Crystal shunt capacitance	f _{osc} = 1 MHz to 40 MHz	1	3	6	pF
C _{EXT}	Crystal external capacitance	f _{osc} = 1 MHz to 40 MHz	1	7	20	pF

Table 5-10 lists the characteristics of the high-frequency crystal oscillator, HFXT.

Table 5-10. High-Frequency Crystal Oscillator, HFXT

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
Oscillator	f _{osc} = 1 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFXTRQ = 1, C _{load} = 10 pF, Typical ESR and Capacitance	0.9 V		40		µA
	f _{osc} = 4 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFXTRQ = 1, C _{load} = 10 pF, Typical ESR and Capacitance			60		
	f _{osc} = 8 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFXTRQ = 1, C _{load} = 10 pF, Typical ESR and Capacitance			100		
	f _{osc} = 10 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFXTRQ = 1, C _{load} = 10 pF, Typical ESR and Capacitance			180		
	f _{osc} = 20 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFXTRQ = 1, C _{load} = 10 pF, Typical ESR and Capacitance			280		
	f _{osc} = 32 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFXTRQ = 1, C _{load} = 10 pF, Typical ESR and Capacitance			320		
	f _{osc} = 40 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFXTRQ = 1, C _{load} = 10 pF, Typical ESR and Capacitance			400		
	f _{osc} = 48 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFXTRQ = 1, C _{load} = 10 pF, Typical ESR and Capacitance			500		
F _{osc}	HFXTBYPASS = 0, HFXTDRIVE = 0 ⁽¹⁾		1		4	MHz
	HFXTBYPASS = 0, HFXTRQ = 1 ⁽¹⁾		4.0 ⁽²⁾		8	
	HFXTBYPASS = 0, HFXTRQ = 2 ⁽¹⁾		8.0 ⁽²⁾		16	
	HFXTBYPASS = 0, HFXTRQ = 4 ⁽¹⁾		16.0 ⁽²⁾		34	
	HFXTBYPASS = 0, HFXTRQ = 4 ⁽¹⁾		24.0 ⁽²⁾		32	
	HFXTBYPASS = 0, HFXTRQ = 4 ⁽¹⁾		32.0 ⁽²⁾		40	
	HFXTBYPASS = 0, HFXTRQ = 0 ⁽¹⁾		40.0 ⁽²⁾		45	
D _{osc} (%)	HFXT oscillator duty cycle Measured at MCLK or HSMCLK f _{osc} = 1.5 MHz to 48 MHz		40%	60%	60%	
I _{osc} (µA)	HFXT oscillator logic level ACRSH-DIVSEL input impedance, bypass mode	HFXTBYPASS = 1 (H2)	0.0		45	µA
	HFXTBYPASS = 1 External clock used as a direct source for MCLK or HSMCLK with no divider (DIVSEL = 0 or DIVSEL = 0)		45%		50%	
D _{osc} (%)	HFXT oscillator logic level ACRSH-DIVSEL input duty cycle	HFXTBYPASS = 1 External clock used as a direct source for MCLK or HSMCLK with divider (DIVSEL > 0 or DIVSEL > 0) must meet specified source to MCLK or HSMCLK	40%		60%	

(1) Maximum frequency of operation of the entire device cannot be exceeded.

(2) When HFXTBYPASS = 0, HFXTDRIVE is not terminated to ground. Input signal is a digital square wave with period T_{osc} defined in the Bottom Trigger Input section of this data sheet. Duty cycle requirements are defined by D_{osc}(%).

High-Frequency Crystal Oscillator, HFXT (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
Oscillator Oscillator is known as HFXT crystal ⁽¹⁾	HFXTBYPASS = 0, HFXTDIRM = 0, HFFREQ = 0, f _{osc,typ} = 10 MHz, C _{load} = 15 pF		1229	5000		Ω
	HFXTBYPASS = 0, HFXTDIRM = 1, HFFREQ = 0, f _{osc,typ} = 4 MHz, C _{load} = 18 pF		940	1200		
	HFXTBYPASS = 0, HFXTDIRM = 1, HFFREQ = 1, f _{osc,typ} = 8 MHz, C _{load} = 18 pF		589	690		
	HFXTBYPASS = 0, HFXTDIRM = 1, HFFREQ = 0, f _{osc,typ} = 0 MHz, C _{load} = 16 pF		200	420		
	HFXTBYPASS = 0, HFXTDIRM = 1, HFFREQ = 0, f _{osc,typ} = 24 MHz, C _{load} = 18 pF		130	270		
	HFXTBYPASS = 0, HFXTDIRM = 1, HFFREQ = 1, f _{osc,typ} = 32 MHz, C _{load} = 18 pF		110	220		
	HFXTBYPASS = 0, HFXTDIRM = 1, HFFREQ = 0, f _{osc,typ} = 40 MHz, C _{load} = 16 pF		100	180		
	HFXTBYPASS = 0, HFXTDIRM = 1, HFFREQ = 0, f _{osc,typ} = 60 MHz, C _{load} = 18 pF		80	140		

(1) Oscillator tolerance is based on a safety factor of 5 for recommended crystals.

High-Frequency Crystal Oscillator, HFXT (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
STARTUP ⁽¹⁾ - Start-up time ⁽²⁾	f _{osc} = 1 MHz, HFXTBYPASS = 0, HFXTDRIVE = 0, HFXTRNG = 0, C _{OUT} = 10 pF, Typical ESR and Capacitance F0NTHF_JEN = 0	3.0 V		1		ms
	f _{osc} = 1 MHz, HFXTBYPASS = 0, HFXTRNG = 1, HFXTRNG = 0, C _{OUT} = 10 pF, Typical ESR and Capacitance F0NTHF_JEN = 0			1.5		
	f _{osc} = 5 MHz, HFXTBYPASS = 0, HFXTRNG = 1, HFXTRNG = 1, C _{OUT} = 10 pF, Typical ESR and Capacitance F0NTHF_JEN = 0			0.7		
	f _{osc} = 10 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFXTRNG = 2, C _{OUT} = 10 pF, Typical ESR and Capacitance F0NTHF_JEN = 0			0.0		ms
	f _{osc} = 20 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFXTRNG = 3, C _{OUT} = 10 pF, Typical ESR and Capacitance F0NTHF_JEN = 0			400		
	f _{osc} = 10 MHz, HFXTBYPASS = 0, HFXTRNG = 1, HFXTRNG = 1, C _{OUT} = 10 pF, Typical ESR and Capacitance F0NTHF_JEN = 0			200		
	f _{osc} = 40 kHz, HFXTBYPASS = 0, HFXTRNG = 1, HFXTRNG = 1, C _{OUT} = 10 pF, Typical ESR and Capacitance F0NTHF_JEN = 0			250		
	f _{osc} = 48 kHz, HFXTBYPASS = 0, HFXTRNG = 1, HFXTRNG = 0, C _{OUT} = 10 pF, Typical ESR and Capacitance F0NTHF_JEN = 0			200		
CapIN	Integrated load capacitance at HFXTN terminal ⁽³⁾			2		pF
CapOUT	Integrated load capacitance at HFXTOUT terminal ⁽³⁾			2		pF
FreqOUT	Oscillator fault frequency ⁽⁴⁾		400		700	Hz

(1) Does not include programmable start-up counter.

(2) This represents all the parasitic capacitance present at the HFXTN and HFXTOUT terminals, respectively, including package, board and package capacitance. The effective load capacitance, CL_{eff} can be computed as CL_{eff} = C_{IN} × C_{OUT} / (C_{IN} + C_{OUT}), where C_{IN} and C_{OUT} is the load capacitance at the HFXTN and HFXTOUT terminals, respectively.

(3) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitor values are specified as 10 pF, 15 pF, and 20 pF. Minimum external capacitance of 7 pF. These are for AC loads; additional capacitance, if used, also be considered in the overall capacitance. The recommendation is only that the recommended effective load capacitance of the selected crystal is met.

(4) Frequencies above the 60 Hz specification do not set the fault flag. Frequencies in between the MIN and MAX might set the flag. A static load condition or fault condition will set the flag.

(5) Measured with typical rated crystal frequency but also applies to specification with crystals.

Table 5-11 lists the characteristics of the DCO.

Table 5-11. DCO

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} , T _A	MIN	TYP	MAX	UNIT
f _{DCO_LF1}	DCO center frequency accuracy for range 1 with calibrated factory settings	Internal resistor mode, DCO _{RSEL} = 0, DCO _{TUNE} = 0	1.443	1.5	1.557	MHz
	External resistor mode, DCO _{RSEL} = 0, DCO _{TUNE} = 0		1.482	1.5	1.518	
f _{DCO_LF2}	DCO center frequency accuracy for range 2 with calibrated factory settings	Internal resistor mode, DCO _{RSEL} = 1, DCO _{TUNE} = 0	2.885	3	3.115	MHz
	External resistor mode, DCO _{RSEL} = 1, DCO _{TUNE} = 0		2.904	3	3.096	
f _{DCO_LF3}	DCO center frequency accuracy for range 3 with calibrated factory settings	Internal resistor mode, DCO _{RSEL} = 2, DCO _{TUNE} = 0	5.77	6	6.23	MHz
	External resistor mode, DCO _{RSEL} = 2, DCO _{TUNE} = 0		5.835	6	6.065	
f _{DCO_LF4}	DCO center frequency accuracy for range 4 with calibrated factory settings	Internal resistor mode, DCO _{RSEL} = 3, DCO _{TUNE} = 0	11.541	12	12.459	MHz
	External resistor mode, DCO _{RSEL} = 3, DCO _{TUNE} = 0		11.655	12	12.345	
f _{DCO_LF5}	DCO center frequency accuracy for range 5 with calibrated factory settings	Internal resistor mode, DCO _{RSEL} = 4, DCO _{TUNE} = 0	23.084	24	24.916	MHz
	External resistor mode, DCO _{RSEL} = 4, DCO _{TUNE} = 0		23.174	24	24.826	
f _{DCO_LF6}	DCO center frequency accuracy for range 6 with calibrated factory settings	Internal resistor mode, DCO _{RSEL} = 5, DCO _{TUNE} = 0	46.164	48	49.836	MHz
	External resistor mode, DCO _{RSEL} = 5, DCO _{TUNE} = 0		47.404	48	48.596	
df _{DCO} /dT	DCO frequency shift with temperature ⁽¹⁾	Internal resistor mode, f ₀ fixed voltage	1.02 V to 3.7 V		250	ppm/°C
	External resistor mode, f ₀ fixed voltage	1.02 V to 3.7 V			-40	
df _{DCO} /dV _{CC}	DCO frequency voltage shift with voltage ⁽²⁾	f ₀ fixed temperature, applicable for both DCO internal and External resistor mode	40°C to 85°C		0.1	%/V
f _{DCO_0}	DCO frequency range 0	DCO _{RSEL} = 0 DCO internal or external resistor mode	3.0 V, 25°C	0.98	0.96	MHz
f _{DCO_1}	DCO frequency range 1	DCO _{RSEL} = 1 DCO internal or external resistor mode	3.0 V, 25°C	1.95	1.9	MHz
f _{DCO_2}	DCO frequency range 2	DCO _{RSEL} = 2 DCO internal or external resistor mode	3.0 V, 25°C	3.92	3.8	MHz
f _{DCO_3}	DCO frequency range 3	DCO _{RSEL} = 3 DCO internal or external resistor mode	3.0 V, 25°C	7.84	7.6	MHz
f _{DCO_4}	DCO frequency range 4	DCO _{RSEL} = 4 DCO internal or external resistor mode	3.0 V, 25°C	15.68	15.2	MHz
f _{DCO_5}	DCO frequency range 5	DCO _{RSEL} = 5 DCO internal or external resistor mode	3.0 V, 25°C	31.36	30	MHz
f _{DCO_6}	DCO frequency range 6			-47.5	26.5	MHz

(1) Calculated using the following method: (500ppm/°C) × (85°C) - (80ppm/°C) × (0°C) = (40°C) × (80ppm/°C) × (85°C) = (40°C) × (3400ppm/°C)

(2) Does not include temperature coefficient of external resistor

Recommended value of external resistor is 100kΩ per 80kΩ, 0.1% ±25ppm/°C

(3) Calculated using the following method: (500ppm/°C) × (1.02 V to 3.7 V) - (40ppm/°C) × (1.02 V to 3.7 V) / (3.7 V - 1.02 V)

DCO (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} , T _A	MIN	TYP	MAX	UNIT
F _{osc, DCO}	DCORSEL = 5, DCOPLIM = 0	1.8 V to 3.7 V		50	50	Hz
	DCORSEL = 4, DCOPLIM = 0			80	120	
	DCORSEL = 3, DCOPLIM = 0			110	170	
	DCORSEL = 2, DCOPLIM = 0			160	270	
	DCORSEL = 1, DCOPLIM = 0			220	340	
	DCORSEL = 0, DCOPLIM = 0			450	550	
F _{osc, DCO}	Stop state	Stop state of the DCO		0.2%		
F _{osc, wake, worst}	DCO settling from worst case DCOSEL to DCOSELm	DCO settled to within 10% of steady state frequency			10	Hz
F _{osc, VDDm, best}	DCO settling from worst case DCOPLIM to within very DCOSEL settling	DCO settled to within 10% of steady state frequency			10	Hz
t _{start}	DCO start-up time ⁽⁴⁾	DCO settled to within 10% of steady state frequency		5		ms

(4) The maximum parasitic capacitance at the DCO external resistance pin (DCCR) should not exceed 5 pF to ensure the specified DCO start-up time.

Table 5-12 lists the overall tolerance of the DCO.

Table 5-12. DCO Overall Tolerance

over operating free-air temperature range (unless otherwise noted)

RESISTOR OPTION	TEMPERATURE RANGE	TEMPERATURE OFFSET (°C)	VOL. TOLER. CHANDEL (°C)	VOL. TOLER. DMS-1 (°C)	OVERALL DMS-1 (°C)	OVERALL ACCURACY (°C)
resistor network	-40°C to 85°C	±0.150	1.00 V to 3.7 V	±0.4	±0.550	±0.801
	10°C	0	1.60 V to 3.7 V	±0.3	±0.3	±0.7
	-40°C to 85°C	±0.155	0 V	0	±0.125	±0.625
Control resistor with 25ppm/°C	-40°C to 85°C	±0.1	1.60 V to 3.7 V	±0.3	±0.7	±1.2
	10°C	0	1.60 V to 3.7 V	±0.2	±0.2	±0.1
	-40°C to 85°C	±0.1	0 V	0	±0.1	±1

Table 5-13 lists the characteristics of the internal very-low-power low-frequency oscillator (VLO).

Table 5-13. Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VLO}	VLO current consumption ⁽¹⁾		50		nA
f_{VLO}	VLO frequency	8	8.4	14	kHz
$\frac{df_{VLO}}{dT}$	VLO frequency temperature drift ⁽²⁾		0.1		%/°C
$\frac{df_{VLO}}{dV_{DD}}$	VLO frequency supply voltage drift ⁽³⁾		0.2		%/V
DC _{VLO}	Duty cycle	40%	55%	60%	

(1) Current measured in PMOS supply.

(2) Calculated using the box method: (MAX: 40°C to 85°C) - (MIN: 40°C to 85°C) / (MIN: 40°C to 85°C) - (85°C - (-40°C)).

(3) Calculated using the box method: (MAX: 3.0 V to 3.7 V) - (MIN: 3.0 V to 3.7 V) / (MAX: 3.0 V to 3.7 V) - (3.7 V - 3.0 V).

Table 5-14 lists the characteristics of the internal-reference low-frequency oscillator (REFO) in 32.768-kHz mode.

Table 5-14. Internal-Reference Low-Frequency Oscillator (REFO) in 32.768-kHz Mode⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{DD}	MIN	TYP	MAX	UNIT
I_{REFO}	REFO current consumption ⁽²⁾			10		μA
f_{REFO}	REFO frequency calibrated			32.768		kHz
f_{REFO}	REFO absolute tolerance calibrated	$T_A = -40^{\circ}\text{C}$ to 85°C $T_A = 25^{\circ}\text{C}$			±1%	
$\frac{df_{REFO}}{dT}$	REFO frequency temperature drift ⁽³⁾			0.0.2		%/°C
$\frac{df_{REFO}}{dV_{DD}}$	REFO frequency supply voltage drift ⁽⁴⁾			0.2		%/V
DC _{REFO}	REFO duty cycle		40%	60%	60%	

(1) REFO is configured in 32.768-kHz mode with REFOSEL = 0.

(2) Total current measured on both AVDD and DVDD supplies.

(3) Calculated using the box method: (MAX: 40°C to 85°C) - (MIN: 40°C to 85°C) / (MAX: 40°C to 85°C) - (85°C - (-40°C)).

(4) Calculated using the box method: (MAX: 3.0 V to 3.7 V) - (MIN: 3.0 V to 3.7 V) / (MAX: 3.0 V to 3.7 V) - (3.7 V - 3.0 V).

Table 5-15 lists the characteristics of the internal-reference low-frequency oscillator (REFO) in 128-kHz mode.

Table 5-15. Internal-Reference Low-Frequency Oscillator (REFO) in 128-kHz Mode⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{DD}	MIN	TYP	MAX	UNIT
REFO	REFO current consumption ⁽²⁾			1		μA
f_{REFO}	REFO frequency calibrated			128		kHz
f_{REFO}	REFO absolute tolerance calibrated	$T_A = -40^{\circ}\text{C}$ to 85°C $T_A = 25^{\circ}\text{C}$			±0%	
$\frac{df_{REFO}}{dT}$	REFO frequency temperature drift ⁽³⁾			0.018		%/°C
$\frac{df_{REFO}}{dV_{DD}}$	REFO frequency supply voltage drift ⁽⁴⁾			0.4		%/V
DC _{REFO}	REFO duty cycle		40%	50%	60%	

(1) REFO is configured in 128-kHz mode with REFOSEL = 1.

(2) Total current measured on both AVDD and DVDD supplies.

(3) Calculated using the box method: (MAX: 40°C to 85°C) - (MIN: 40°C to 85°C) / (MIN: 40°C to 85°C) - (85°C - (-40°C)).

(4) Calculated using the box method: (MAX: 3.0 V to 3.7 V) - (MIN: 3.0 V to 3.7 V) / (MAX: 3.0 V to 3.7 V) - (3.7 V - 3.0 V).

Table 5-16 Lists the characteristics of the module oscillator (MODOSC).**Table 5-16. Module Oscillator (MODOSC)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{MODOSC}	Current consumption ⁽¹⁾			50		µA
f _{MODOSC}	MODOSC frequency		25	25	27	MHz
df _{MODOSC} /dT	MODOSC frequency temperature coefficient			0.02		ppm/°C
df _{MODOSC} /dV _{CC}	MODOSC frequency supply voltage coefficient			0.5		ppm/V
MODOSC _{test}	Duty cycle		40%	50%	60%	

(1) Total current measured on both AVCC and DVCC supplies.

(2) Calculated using the box method: (MAX=40°C to 85°C) + (MIN=40°C to 85°C) + (MIN=40°C to 85°C) + (85°C to 125°C) + (125°C to 150°C).

(3) Calculated using the box method: (MIN) 0.2 V to 0.7 V; (MIN) 0.2 V to 0.7 V; (MIN) 0.2 V to 0.7 V; (13.7 V to 62 V).

Table 5-17 Lists the characteristics of the system oscillator (SYSOSC).**Table 5-17. System Oscillator (SYSOSC)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{SYSOSC}	Current consumption ⁽¹⁾			50		µA
f _{SYSOSC}	SYSOSC frequency		4.75	5.0	5.25	MHz
df _{SYSOSC} /dT	SYSOSC frequency temperature coefficient			0.03		ppm/°C
df _{SYSOSC} /dV _{CC}	SYSOSC frequency supply voltage coefficient			0.5		ppm/V
SYSOSC _{test}	Duty cycle		40%	50%	60%	

(1) Current measured on AVCC supply.

(2) Calculated using the box method: (MAX=40°C to 85°C) + (MIN=40°C to 85°C) + (MIN=40°C to 85°C) + (85°C to 125°C) + (125°C to 150°C).

(3) Calculated using the box method: (MIN) 0.2 V to 0.7 V; (MIN) 0.2 V to 0.7 V; (MIN) 0.2 V to 0.7 V; (13.7 V to 62 V).

5.25.4 Power Supply System

Table 5-18 lists the LDO V_{DDREG} regulator characteristics.

Table 5-18. V_{DDREG} Regulator (LDO) Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DDREG0}	Static V_{DDREG} voltage Level 0 in active and LPM0 modes	1.12	1.2	1.25	V
$V_{DDREG10}$	Static V_{DDREG} voltage Level 1 in active and LPM0 modes	1.2	1.4	1.45	V
V_{DDREG1}	Static V_{DDREG} voltage Level 1 in low-frequency active and the frequency LPM0 modes	1.12	1.2	1.25	V
$V_{DDREG1F}$	Static V_{DDREG} voltage Level 1 in low-frequency active and the frequency LPM0 modes	1.3	1.4	1.45	V
$V_{DDREG1+2+4}$	Static V_{DDREG} voltage Level 0 in LPM1 and LPM1+ modes	1.16	1.2	1.12	V
$V_{DDREG1+2+4F}$	Static V_{DDREG} voltage Level 1 in LPM1 and LPM1+ modes	1.27	1.4	1.51	V
$V_{DDREG1+2+4F}$	Static V_{DDREG} voltage Level 1 in LPM1+ mode	1.00	1.2	1.12	V
I_{DDREG0}	Initial current at start-up			200	mA
I_{DDREG1}	Peak current drawn by LDO from V_{DD}			250	mA
$I_{DDREG1+2+4}$	Static current and initial LDO			300	mA

Table 5-19 lists the DC-DC V_{DDREG} regulator characteristics.

Table 5-19. V_{DDREG} Regulator (DC-DC) Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OV_{DDREG}	Allowed V_{DDREG} range in LDO-III operation	0		0.7	V
$V_{DDREG1+2+4}$	DC-DC to LDO switch-over voltage	0		2.0	V
$V_{DDREG1+2+4}$	Static V_{DDREG} voltage Level 0 in DC-DC independent mode	1.12	1.2	1.25	V
$V_{DDREG1+2+4F}$	Static V_{DDREG} voltage Level 1 in DC-DC independent mode	1.31	1.4	1.45	V
I_{DDREG1}	Peak current drawn by DC-DC from V_{DD}			200	mA
$I_{DDREG1+2+4}$	Static current and initial DC-DC			200	mA

(1) When V_{DDREG} falls below the voltage, the regulator switches over to LDO from DC-DC.

Table 5-20 lists the VCCDET characteristics.

Table 5-20. PSS, VCCDET

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{CCDET} _{down}	VCCDET1 power-down level (up point with rising V _{CC}) ID(A _{DD}) ≤ 5 mA ⁽¹⁾	0.04	1.12	1.99	V
V _{CCDET} _{up}	VCCDET power-up level (up point with rising V _{CC}) ID(A _{DD}) ≤ 5 mA ⁽¹⁾	0.70	1.18	1.99	V
V _{CCDET} _{hys}	VCCDET hysteresis	30	65	100	mV

(1) The VCCDET1 levels are measured with a 5-kHz square-wave supply. Load slopes are noted in 0.1mA/100µs.

Table 5-21 lists the SVSMH characteristics.

Table 5-21. PSS, SVSMH

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{SVSMH}	SVSMH current consumption (low power mode)	SVSMHCT = 0, SVSMHLP = 1	200	400	nA
	SVSMH current consumption (high performance mode)	SVSMHCT = 0, SVSMHLP = 0	7	10	µA
V _{SVSMH} _{low}	SVSMH threshold level during high performance mode (falling DV _{DD})	SVSMHCT = 0, SVSMHLP = 0, SVSMHTH = 0 DC (ID(A _{DD}) ≤ 10µA)	1.59	1.64	1.71
		SVSMHCT = 0, SVSMHLP = 0, SVSMHTH = 1 DC (ID(A _{DD}) ≤ 10µA)	1.59	1.64	1.71
		SVSMHCT = 0, SVSMHLP = 0, SVSMHTH = 2 DC (ID(A _{DD}) ≤ 10µA)	1.59	1.64	1.71
		SVSMHCT = 0, SVSMHLP = 0, SVSMHTH = 3 DC (ID(A _{DD}) ≤ 10µA)	2.0	2.06	2.13
		SVSMHCT = 0, SVSMHLP = 0, SVSMHTH = 4 DC (ID(A _{DD}) ≤ 10µA)	2.2	2.26	2.33
		SVSMHCT = 0, SVSMHLP = 0, SVSMHTH = 5 DC (ID(A _{DD}) ≤ 10µA)	2.4	2.47	2.54
		SVSMHCT = 0, SVSMHLP = 0, SVSMHTH = 6 DC (ID(A _{DD}) ≤ 10µA)	2.7	2.70	2.83
		SVSMHCT = 0, SVSMHLP = 0, SVSMHTH = 7 DC (ID(A _{DD}) ≤ 10µA)	2.9	3.0	3.1
		SVSMHCT = 0, SVSMHLP = 0, SVSMHTH = 0 DC (ID(A _{DD}) ≤ 10µA)	1.8	1.88	1.93
		SVSMHCT = 0, SVSMHLP = 0, SVSMHTH = 1 DC (ID(A _{DD}) ≤ 10µA)	1.8	1.88	1.93
V _{SVSMH} _{high}	SVSMH threshold level, High Performance Mode (rising DV _{DD})	SVSMHCT = 0, SVSMHLP = 0, SVSMHTH = 3 DC (ID(A _{DD}) ≤ 10µA)	2.02	2.07	2.14
		SVSMHCT = 0, SVSMHLP = 0, SVSMHTH = 4 DC (ID(A _{DD}) ≤ 10µA)	2.22	2.27	2.34
		SVSMHCT = 0, SVSMHLP = 0, SVSMHTH = 5 DC (ID(A _{DD}) ≤ 10µA)	2.42	2.48	2.60
		SVSMHCT = 0, SVSMHLP = 0, SVSMHTH = 6 DC (ID(A _{DD}) ≤ 10µA)	2.72	2.8	2.8
		SVSMHCT = 0, SVSMHLP = 0, SVSMHTH = 7 DC (ID(A _{DD}) ≤ 10µA)	2.92	3.01	3.13
		SVSMHCT = 0, SVSMHLP = 0, SVSMHTH = 0 DC (ID(A _{DD}) ≤ 10µA)	1.8	1.88	1.93
		SVSMHCT = 0, SVSMHLP = 0, SVSMHTH = 1 DC (ID(A _{DD}) ≤ 10µA)	1.8	1.88	1.93

PSS, SVSMH (continued)

over recommended ranges of supply voltage and operating fresh-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{SWMR} (1)	SVSMH:CE = 0, SVSMH:IE = 1, SVSMH:II = 0 DC (dV _{CO} /dt > 1V/s)	1.55	1.57	1.71	V
	SVSMH:CE = 0, SVSMH:IE = 1, SVSMH:II = 1 DC (dV _{CO} /dt > 1V/s)	1.55	1.62	1.71	
	SVSMH:FF = 0, SVSMH:LP = 1, SVSMH:TH = 2 DC (dV _{CO} /dt > 1V/s)	1.55	1.62	1.71	
	SVSMH:FF = 0, SVSMH:LP = 1, SVSMH:TH = 3 DC (dV _{CO} /dt > 1V/s)	2.0	2.09	2.18	
	SVSMH:FF = 0, SVSMH:LP = 1, SVSMH:TH = 4 DC (dV _{CO} /dt > 1V/s)	2.2	2.3	2.4	
	SVSMH:FF = 0, SVSMH:LP = 1, SVSMH:TH = 5 DC (dV _{CO} /dt > 1V/s)	3.0	2.81	3.67	
	SVSMH:CE = 0, SVSMH:IE = 1, SVSMH:II = 8 DC (dV _{CO} /dt > 1V/s)	3.7	2.63	3.84	
	SVSMH:CE = 0, SVSMH:IE = 1, SVSMH:II = 7 DC (dV _{CO} /dt > 1V/s)	2.67	3.0	3.13	
V _{SWMR} (2)	SVSMH: hardware		15	37	mV
t _{SVSMH}	SVSMH propagation delay (high-performance mode)	SVSMH:CE = 0, SVSMH:IE = 0 any fast dV _{CO} /dt	3	5	ns
	SVSMH propagation delay (low-power mode)	SVSMH:CE = 0, SVSMH:IE = 1 any fast dV _{CO} /dt	25	100	ns
t _{SVSMH}	SVSMH on-reset delay time	SVSMH:CE = 1 & 0, SVSMH:LP = 0 (3)	1.7	60	ns

(1) If the SVSMH is kept disabled in active mode and enabled while entering a deep-power mode of the device (LPM3, LPM4, LPM5, or LPM5.5) then should be known that software time has elapsed since enabling of the module before entry into the device low-power mode to allow for successful wake up of the SVSMH module per the SVSMH on-reset delay time specification. Otherwise, SVSMH may trip, causing the device to reset and wake up from the low-power mode.

5.25.5 Digital I/Os

Table 5-22 lists the characteristics of the digital inputs.

Table 5-22. Digital Inputs (Applies to Both Normal and High-Drive I/Os)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{DD}	MIN	TYP	MAX	UNIT
V _{IH}	Positive-going input threshold voltage	2.4 V	0.98		1.65	V
		3 V	1.95		2.25	
V _{IL}	Negative-going input threshold voltage	2.4 V	0.55		1.11	V
		3 V	0.75		1.65	
V _{OL}	Input voltage hysteresis (V _{IH} = V _{IL} + 1)	2.2 V	0.20		0.71	V
		3 V	0.4		1.0	
I _{leak}	Full-scale pull-down current	For pull-up: V _{DD} = V _{DD} For pull-down: V _{DD} = V _{DD}		20	30	40
C _{in}	Input capacitance, digital-only port pins	V _{DD} = V _{DD} or V _{DD}		3		pF
C _{in}	Input capacitance, port pins driven with analog functions	V _{DD} = V _{DD} or V _{DD}		7		pF
I _{in}	Normal I/O high-impedance input leakage current	base (100)	2.0 V, 3 V		500	nA
I _{in}	High-drive I/O high-impedance input leakage current	base (100)	2.0 V, 3 V		500	nA
t _{tr}	External interrupt timing (external trigger pulse duration for set interrupt flag)	Ports with interrupt capability and without pin driver (1)	2.0 V, 3 V	20		ns
		Ports with interrupt capability and with pin driver but pin driver disabled (GCLKEN = 0) (2)	2.2 V, 3 V	20		
		Ports with interrupt capability and with pin driver enabled (GCLKEN = 1) (3)	2.2 V, 3 V	0.25	1	ps
t _{tr}	External noise pulse duration on RSTn pin (4)	2.2 V, 3 V		1		ps

(1) The input leakage current is measured with V_{DD} or V_{SS} applied to the corresponding pin, unless otherwise noted.

(2) The input leakage of the digital-only pins is measured individually. The port pin is selected for input and the pull-up/down resistor is disabled.

(3) An external signal sets the interrupt flag every time the minimum interrupt pulse duration is not. It may be set by trigger signals shorter than t_{tr}.

(4) A trigger pulse duration less than the MIN value is always filtered, and a trigger pulse duration more than the MAX value is always present. The trigger pulse may or may not be filtered if the duration is between the MIN and MAX values.

(5) Not applicable if I/O is not pin configured as I/O.

Table 5-23 lists the characteristics of the normal-drive digital outputs. See Figure 5-19 through Figure 5-22 for the typical characteristics graphs.

Table 5-23. Digital Outputs, Normal I/Os

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
V _{OH}	High-level output voltage	2.2 V	V _{OH} = 0.25	V _{OH}	V
			V _{OH} = 0.60	V _{CC}	
		3.0 V	V _{OH} = 0.25	V _{CC}	
			V _{OH} = 0.80	V _{CC}	
V _{OL}	Low-level output voltage	2.2 V	V _{OL}	V _{OL} + 0.25	V
			V _{OL}	V _{OL} + 0.80	
		3.0 V	V _{OL}	V _{OL} + 0.25	
			V _{OL}	V _{OL} + 0.80	
f _{OUT}	Max output frequency (with 10- Ω load) ⁽¹⁾	1.62 V	24		MHz
		2.2 V	24		
		3.0 V	24		
d _{OUT}	Max output duty cycle (with 10- Ω load)	1.62 V	40%	60%	
		2.2 V	40%	60%	
		3.0 V	40%	60%	
f _{OUT,CLK}	Clock output frequency ⁽²⁾	1.62 V	24		MHz
		2.2 V	24		
		3.0 V	24		
d _{OUT,CLK}	Clock output duty cycle	1.62 V	40%	60%	
		2.2 V	40%	60%	
		3.0 V	40%	60%	
t _{rise}	Rise time, 50% to 90% ⁽³⁾	1.62 V	8		ns
		2.2 V	9		
		3.0 V	11		
t _{fall}	Fall time, 90% to 50% ⁽³⁾	1.62 V	8		ns
		2.2 V	9		
		3.0 V	11		
t _{rise,drv}	Rise time, 50% to 90%, per pin with driver and lag functions ⁽⁴⁾	1.62 V	8		ns
		2.2 V	9		
		3.0 V	9		
t _{fall,drv}	Fall time, 90% to 50%, per pin with driver and lag functions ⁽⁴⁾	1.62 V	8		ns
		2.2 V	9		
		3.0 V	9		

(1) The maximum total current, I_{OH(max)} and I_{OL(max)}, for all outputs in a defined state of not asserted +45 mA to limit the maximum voltage drop specified.

(2) The maximum total current, I_{OH(max)} and I_{OL(max)}, for all outputs in a defined state of not asserted +120 mA to limit the maximum voltage drop specified.

(3) The maximum output frequency (measured at 50% to 90% of the specified limit), if multiple outputs happen two outputs.

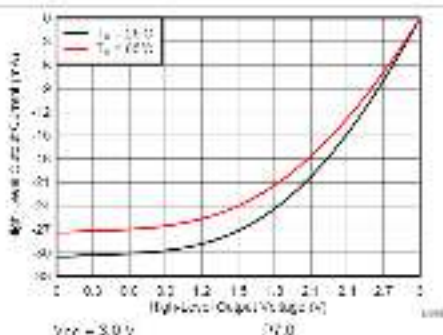
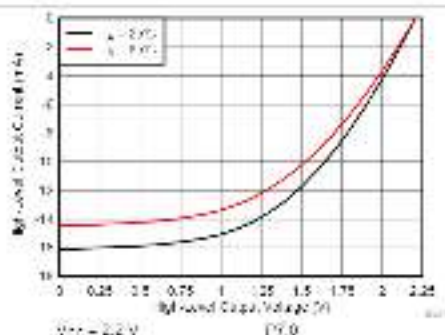
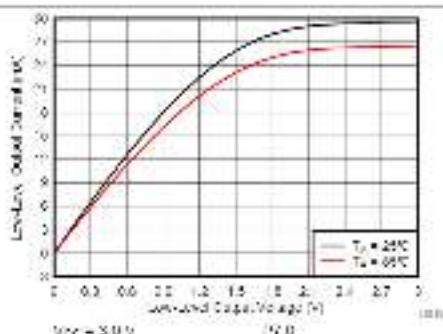
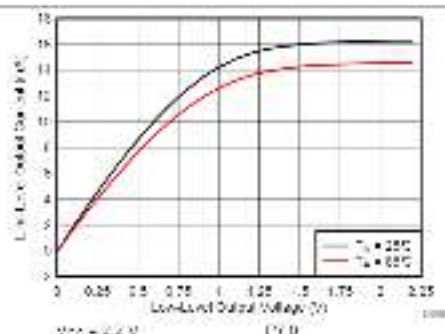
(4) A resistor divider with R = 10 Ω and (2) = 2.2 k Ω between V_{CC} and V_{OL} is used as load. The output is connected to the center tap of the divider. C_L = 20 pF is connected to the output to V_{CC}.

(5) The output voltage measured at load 20 Ω and 80 Ω at f_{OUT} at the specified supply frequency.

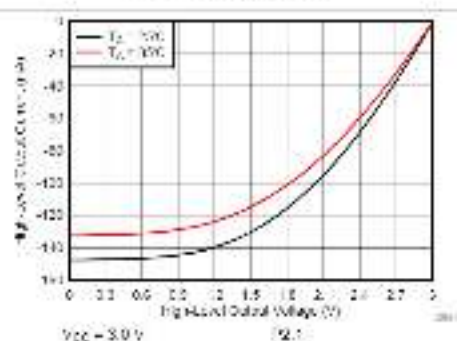
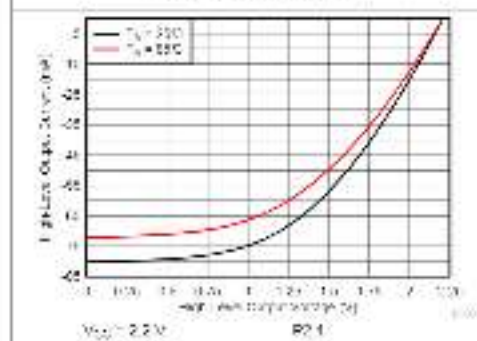
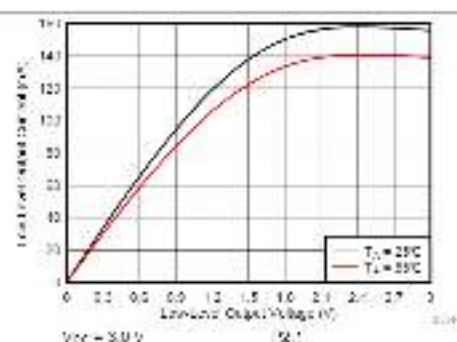
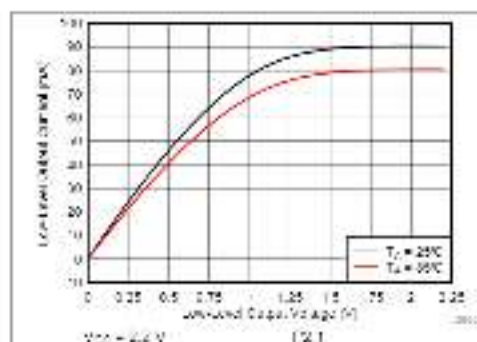
(6) Measured between 20% of V_{CC} to 50% of V_{CC}.

(7) Measured between 80% of V_{CC} to 90% of V_{CC}.

5.25.5.1 Typical Characteristics, Normal-Drive I/O Outputs at 3.0 V and 2.2 V



5.25.5.2 Typical Characteristics, High-Drive I/O Outputs at 3.0 V and 2.2 V



5.26.5.3 Typical Characteristics, Pin-Oscillator Frequency

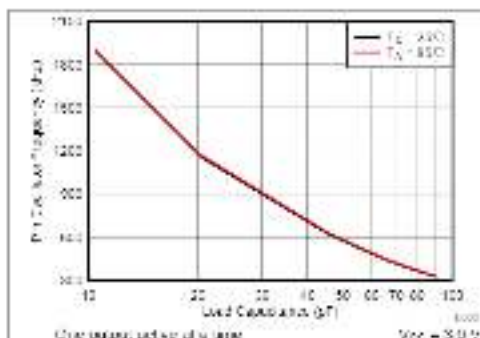


Figure 5-27. Load Capacitance vs Pin Oscillator Frequency

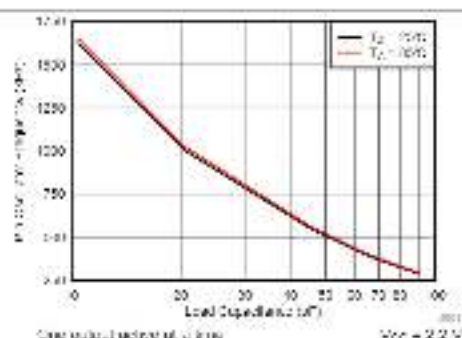


Figure 5-28. Load Capacitance vs Pin Oscillator Frequency

5.25.6 14-Bit ADC

Table 5-26 lists the power supply and input range conditions for the ADC.

Table 5-26. 14-Bit ADC: Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{DD}	MIN	NOM	MAX	UNIT
A _{VDD}	Analog supply voltage AVDD and DVDD are connected together, V _{AVDD} = V _{DVDD} = 0 V, ADC14PWRMD = 2		1.62		3.7	V
A _{VDD}	Analog supply voltage AVDD and DVDD are connected together, V _{AVDD} = V _{DVDD} = 0 V, ADC14PWRMD = 0		1.4		3.7	V
V _{IN(1)}	Analog input voltage (range 1)	At ADC analog input pin A _N	0		V _{DDC}	V
V _{IN(2)}	Input common-mode voltage	At ADC analog input pin A _N (ADC14DF = 1)	0	V _{REF} / 2	V _{DDSP}	V
I _{DD(1)} Sleep-mode current	Operating supply current into AVDD and DVDD terminals ⁽¹⁾	f _{APCLK1} = 25 MHz, 1 Mbps (ADC14PWRMD = 0), ADC14ON = 1, ADC14SH = 0, ADC14M2SEL = 0b0, ADC14ON = 0, ADC14SH TX = 0b0, ADC14SH TX = 0b0	3.0 V	400	640	μA
			2.2 V	450	590	
		f _{APCLK1} = 2 MHz, 200 kbps (ADC14PWRMD = 0), ADC14ON = 1, ADC14DF = 0, ADC14M2SEL = 0b0, ADC14ON = 0, ADC14SH TX = 0b0, ADC14SH TX = 0b0	3.0 V	210	270	
			2.2 V	240	260	
I _{DD(2)} Active-mode current	Operating supply current into AVDD and DVDD terminals ⁽¹⁾	f _{APCLK1} = 25 MHz, 1 Mbps (ADC14PWRMD = 0), ADC14ON = 1, ADC14DF = 1, ADC14M2SEL = 0b0, REPON = 0, ADC14SH TX = 0b0, ADC14SH TX = 0b0	3.0 V	650	675	μA
			2.2 V	650	675	
		f _{APCLK1} = 2 MHz, 200 kbps (ADC14PWRMD = 2), ADC14ON = 1, ADC14DF = 1, ADC14M2SEL = 0b0, REPON = 0, ADC14SH TX = 0b0, ADC14SH TX = 0b0	3.0 V	375	385	
			2.2 V	380	390	
C _I	Input capacitance and a single terminal ⁽²⁾			12	15	pF
R _I	Input Miller capacitance ⁽³⁾	0 V < V _{IN(1)} < V _{DDC}	1.5 V to 3.7 V	0.45	1	fF
		1.5 V to 3.7 V	1.5 V to 3.7 V	0.45	1.7	fF

(1) The allowed input voltage range must be within the selected reference voltage range (V_{REF} to V_{DD}) for valid conversion results.

(2) The allowed power-supply pin and terminal is included in current-consumption parameter I_{DD(1)}.

(3) Represents only the ADC switching capacitance. See the digital input/output electrical specifications for internal measured capacitance.

Table 5-22 lists the dynamic parameters of the ADC.

Table 5-29. 14-Bit ADC, Dynamic Parameters⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR ⁽²⁾	Signal-to-noise and distortion	1 kHz, AUC140E = 0, AUC14VREF = 0 2.5 V reference, 20 kHz input sine, EOC based operation	91	75		
		1 kHz, AUC140E = 0, AUC14VREF = 0 2.5 V reference, 20 kHz input sine, EOC based operation	62	70		dB
		1 kHz, AUC140E = 1, AUC14VREF = 0 2.5 V reference, 20 kHz input sine	68	81		
ENOB ⁽¹⁾	Effective number of bits	1 kHz, AUC140E = 0, AUC14VREF = 0 2.5 V reference, 20 kHz input sine, EOC based operation	11.5	11.6		
		1 kHz, AUC140E = 0, AUC14VREF = 0 2.5 V reference, 20 kHz input sine, EOC based operation	10	11.3		LSB
		1 kHz, AUC140E = 1, AUC14VREF = 0 2.5 V reference, 20 kHz input sine	10.9	10.2		
CMRR _{DC}	Common mode rejection ratio, DC	Common mode input signal = 0 to VREF pp at AUC140E = 1	70	80		dB
CMRR _{AC}	Common mode rejection ratio, AC	Common mode input signal = 0 to VREF pp at 1 kHz, AUC140E = 1	60	66		dB
PSRR _{CM}	Power supply rejection ratio, CM	$V_{REF} = V_{REF} \text{ (avg) to } V_{REF} \text{ (max)}$ AUC140E = 0, AUC14VREF = 0	1	2.5		mV/V
		$V_{REF} = V_{REF} \text{ (avg) to } V_{REF} \text{ (max)}$ AUC140E = 1, AUC14VREF = 0	50	150		mV/V
PSRR _{CM}	Power supply rejection ratio, CM	$V_{REF} = 0.1 \text{ V to } 1 \text{ mV}$ AUC140E = 0, AUC14VREF = 0	1			mV/V
		$V_{REF} = 0.1 \text{ V to } 1 \text{ mV}$ AUC140E = 1, AUC14VREF = 0	50			mV/V

(1) $9481 \cdot 1$ is a prime number; moreover, $9481 \cdot 1$ is a prime number.

(2) ΔE_C value determined by HF-KT calculation.

Table 5-30 lists the characteristics of the temperature sensor and built-in V_{TSEN} .

Table 5-30. 14-Bit ADC, Temperature Sensor and Built-In V_{TSEN}

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{DD}	MIN	TYP	MAX	UNIT
V_{TSEN}	See 10.21	ADC14ON = 1, ADC14TCONMAP = 1, $I_A = 0\mu A$		550		mV
$T_{OSensor}$	See 10.21	ADC14ON = 1, ADC14TCONMAP = 1		1.0		mV/°C
t_{Sensor} (max)	Sample time required if ADC14TCONMAP = 1 and channel 3 (P3C_1) is selected ⁽¹⁾	ADC14ON = 1, ADC14TCONMAP = 1, End of conversion result 0.1 LSB		5		μs
V_{IN}	ADC voltage divider for ADC14TCONMAP = 1 on 140K input 0.00001	ADC14ON = 1, ADC14TCONMAP = 1	93%	96%	97%	
t_{IN} (max)	Sample time required if ADC14TCONMAP = 1 and channel 3 (P3C_1) is selected ⁽¹⁾	ADC14ON = 1, ADC14TCONMAP = 1		1		μs

- (1) The temperature sensor value can be expressed as $0.001^\circ C$. If recommended sample-and-hold device is used, the clock rate of the built-in temperature sensor.
- (2) The mV that are obtained when values in 0.01%, 0.01% and 0.01% are used of the variable reference voltage levels. The sensor voltage can be computed as $V_{TSEN} = T_{OSensor} \times (\text{Temperature}/^\circ C) + V_{TSEN}$ where $T_{OSensor}$ and V_{TSEN} are 1.00 computed from the calibration values for better accuracy.
- (3) The typical equivalent impedance of the sensor is 250k Ω . The sample time required includes the sensor settling time for accuracy.
- (4) The clock f_{CLK} is indicated in the sample time t_{IN} (5 sample). No additional on time is needed.

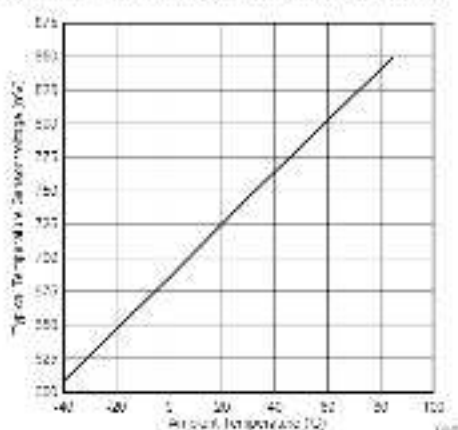


Figure 5-29. Typical Temperature Sensor Voltage

Table 5-31 lists the characteristics of the internal reference buffers of the ADC.

Table 5-31. 14-Bit ADC, Internal Reference Buffers

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{REF}	Operating supply current into ADC internal ⁽¹⁾	ADC ON, REFOUT = 0, ADC14PWRMD = 0, REFVSEL = (0, 1, 2)	3 V		600	800	μA
		ADC ON, REFOUT = 0, ADC14PWRMD = 2, REFVSEL = (0, 1, 2)			200	300	
		ADC ON, REFOUT = 1, ADC14PWRMD = 2, REFVSEL = (0, 1, 2)			650	850	
t _{tr}	Turn-on time		3 V			2	μs

(1) The internal reference current is supplied through bandgaps.

Table 5-32 lists the characteristics of the ADC external reference.

Table 5-32. 14-Bit ADC, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

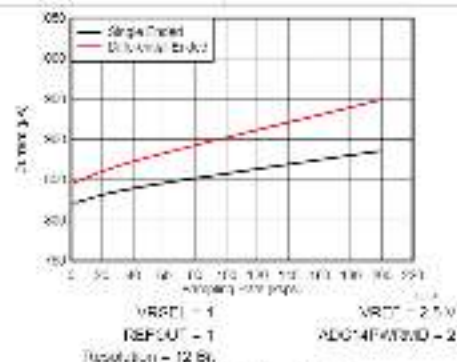
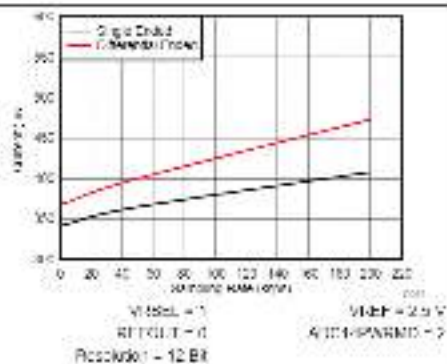
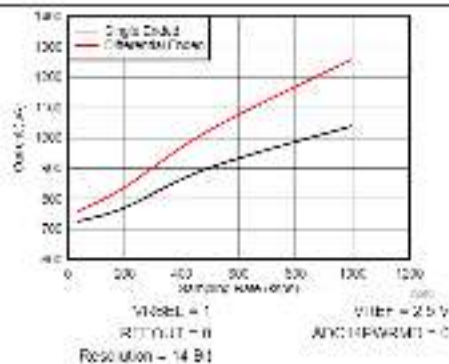
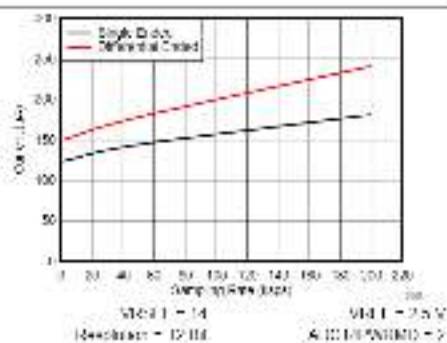
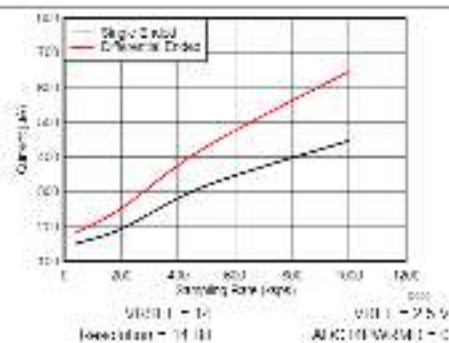
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{REFP}	Positive external reference voltage input ⁽¹⁾		1.45	V _{VCC}		V
V _{REFM}	Negative external reference voltage input			0		V
(V _{REFP} - V _{REFM})	Differential external reference voltage input ⁽¹⁾		1.45	V _{VCC}		V
I _{INP} , I _{INM}	Static input current in single-ended input mode	1.45 V < V _{REFP} , V _{REFM} , V _{REFD} = 0 V, I _{INP} max = 75 nA in ADC14S110x = 0x1, ADC14SHT1x = 0x1, ADC14OP = 0 1.45 V < V _{REFP} , V _{REFM} , V _{REFD} = 0 V, I _{INM} max = 5 nA in ADC14S110x = 0x1, ADC14SHT1x = 0x1, ADC14OP = 0 1.45 V < V _{REFP} , V _{REFM} , V _{REFD} = 0 V, I _{INP} max = 25 nA in ADC14S110x = 0x1, ADC14SHT1x = 0x1, ADC14OP = 1 1.45 V < V _{REFP} , V _{REFM} , V _{REFD} = 0 V, I _{INM} max = 5 nA in ADC14S110x = 0x1, ADC14SHT1x = 0x1, ADC14OP = 1		±75		μA
I _{INP} , I _{INM}	Static input current in differential input mode	1.45 V < V _{REFP} , V _{REFM} , V _{REFD} = 0 V, I _{INP} max = 75 nA in ADC14S110x = 0x1, ADC14SHT1x = 0x1, ADC14OP = 0 1.45 V < V _{REFP} , V _{REFM} , V _{REFD} = 0 V, I _{INM} max = 5 nA in ADC14S110x = 0x1, ADC14SHT1x = 0x1, ADC14OP = 0 1.45 V < V _{REFP} , V _{REFM} , V _{REFD} = 0 V, I _{INP} max = 25 nA in ADC14S110x = 0x1, ADC14SHT1x = 0x1, ADC14OP = 1 1.45 V < V _{REFP} , V _{REFM} , V _{REFD} = 0 V, I _{INM} max = 5 nA in ADC14S110x = 0x1, ADC14SHT1x = 0x1, ADC14OP = 1		±150		
C _{OUT}	Capacitance of V _{REF} terminals	See (2)		5		pF

(1) Lower reference voltage down to 1.2 V can be supplied for 1-Mbps sampling rate with reduced accuracy requirements of binary partitions.

(2) Two recommended operations, 5 nA and 10 nA, should be considered to V_{REF} terminal to decrease the dynamic current required to an external reference source if it is used by the ADC14. See also the MSP432P401R/MSP432P401M User's Guide for additional information.

5.26.6.1 Typical Characteristics of ADC

typical characteristics at 3 V, 25°C, and 1-Msp/s sampling rate of ADC (unless otherwise specified)



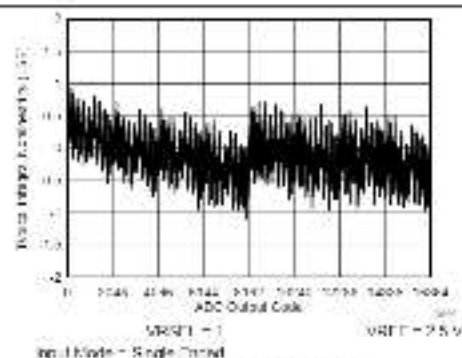


Figure 5-35. INL vs ADC Output Code

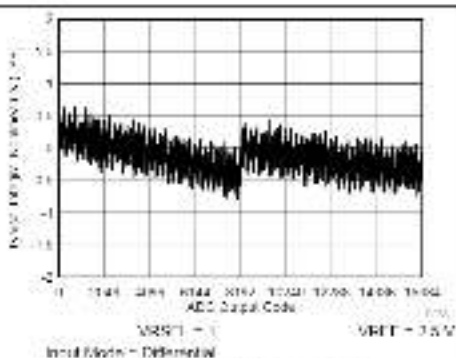


Figure 5-36. INL vs ADC Output Code

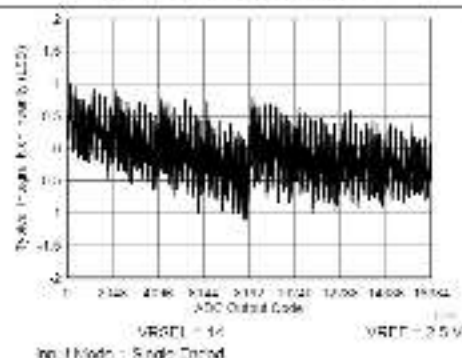


Figure 5-37. INL vs ADC Output Code

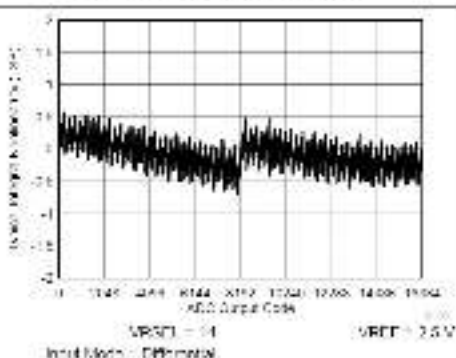


Figure 5-38. INL vs ADC Output Code

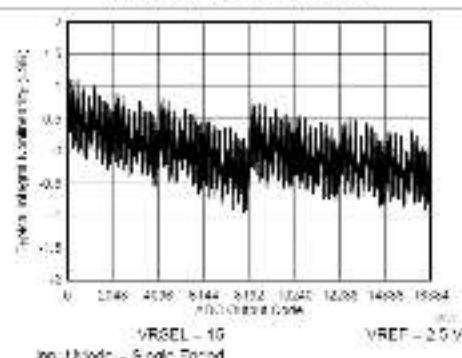


Figure 5-39. INL vs ADC Output Code

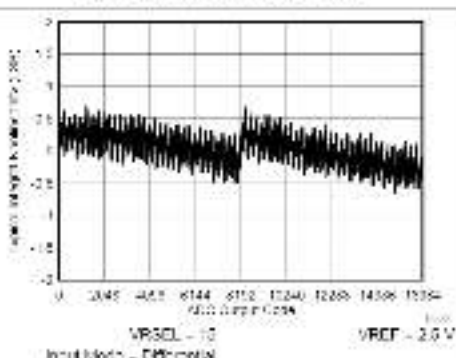
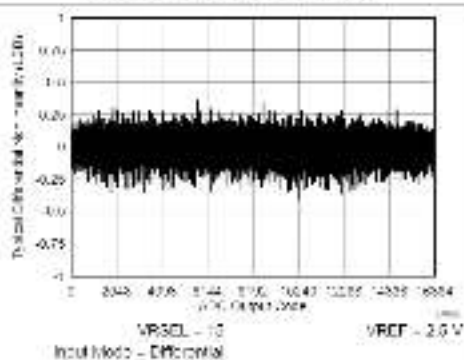
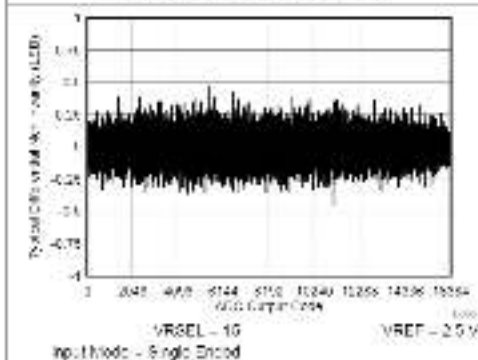
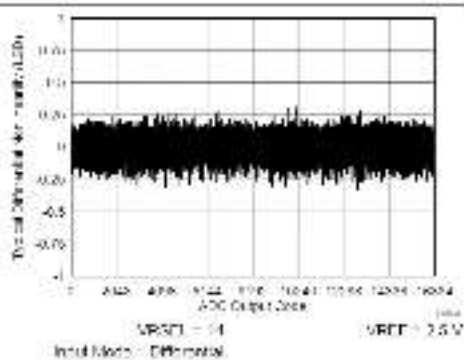
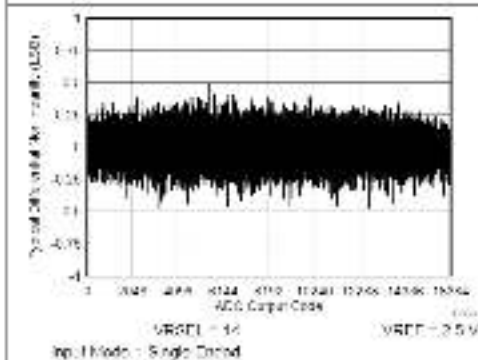
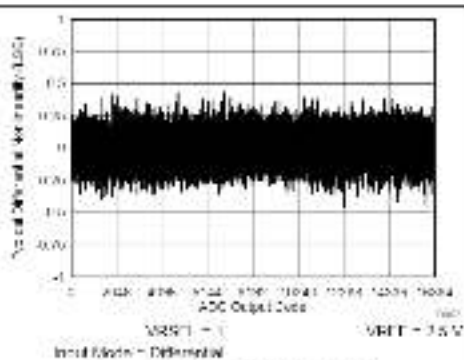
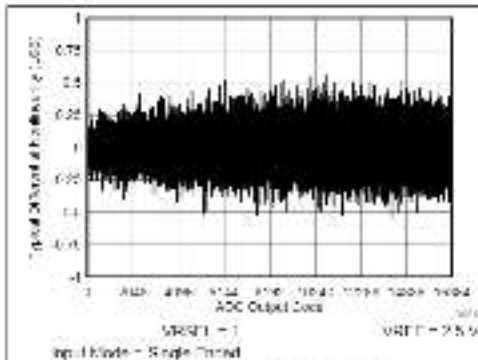
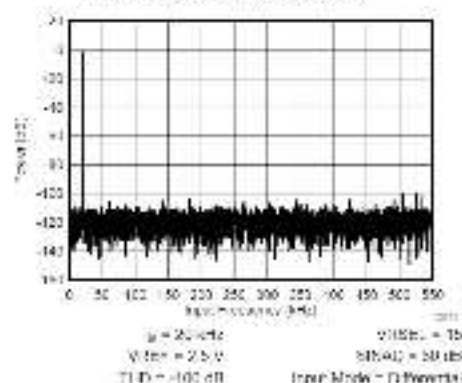
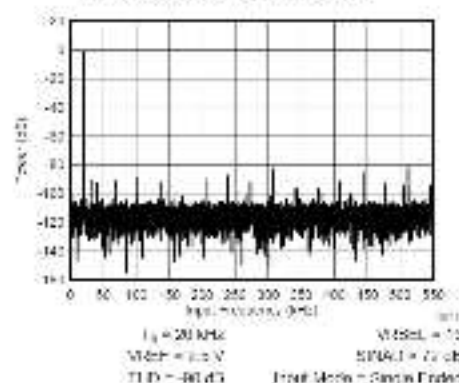
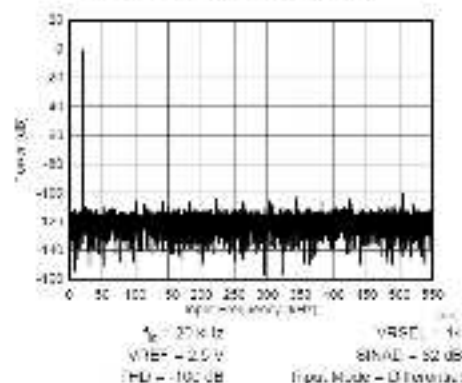
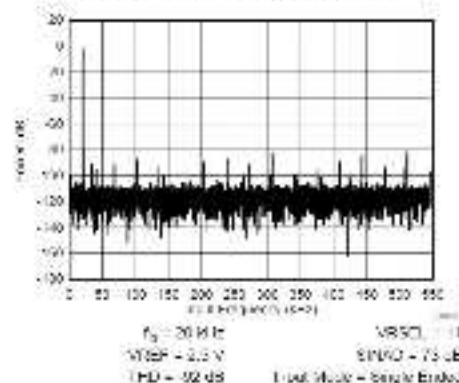
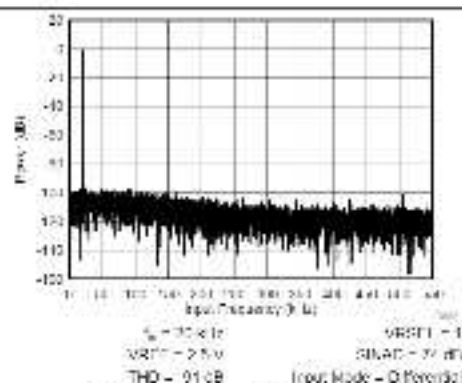
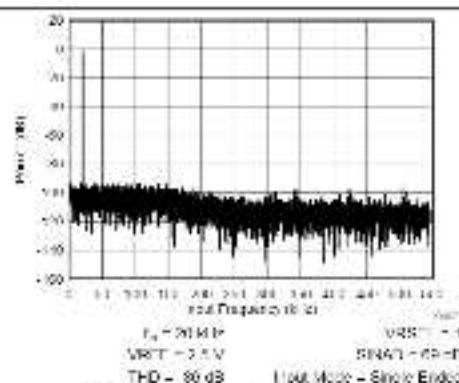


Figure 5-40. INL vs ADC Output Code





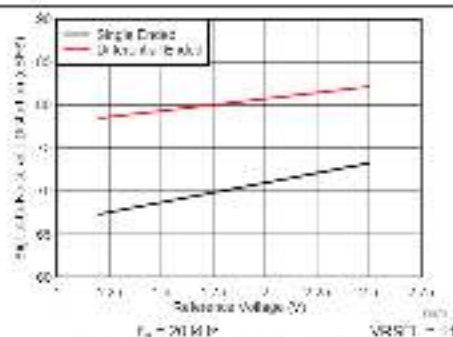


Figure 6-63. SINAD vs Reference Voltage

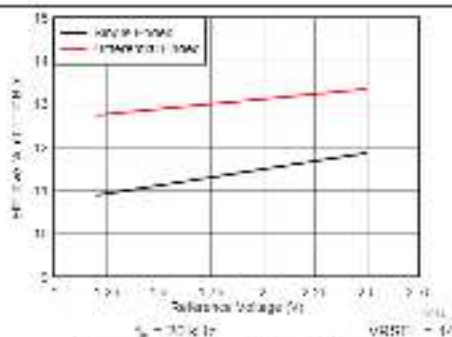


Figure 6-64. ENOB vs Reference Voltage

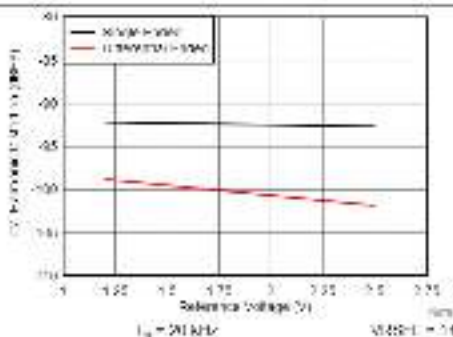


Figure 6-65. THD vs Reference Voltage

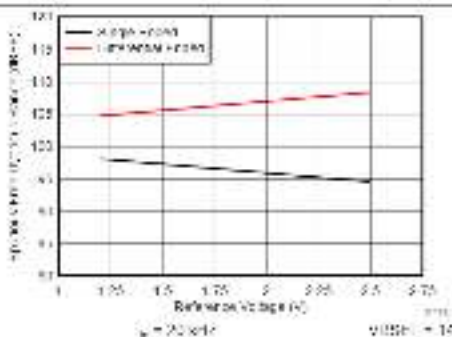
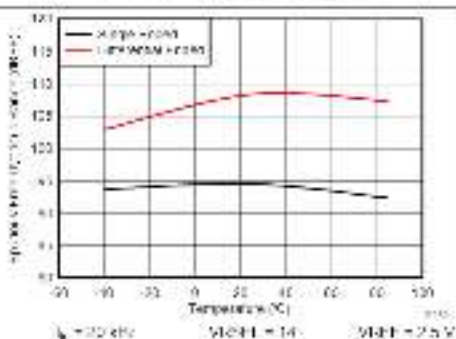
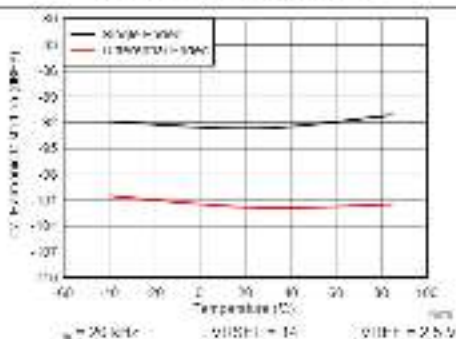
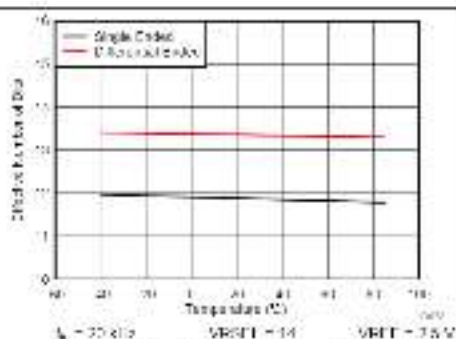
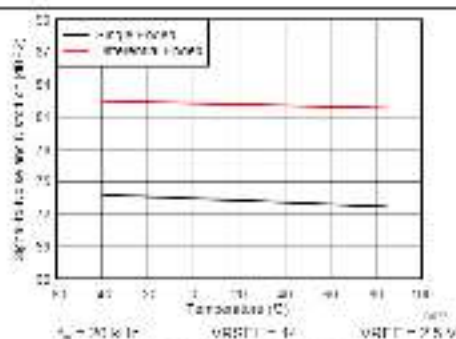


Figure 6-66. SFDR vs Reference Voltage



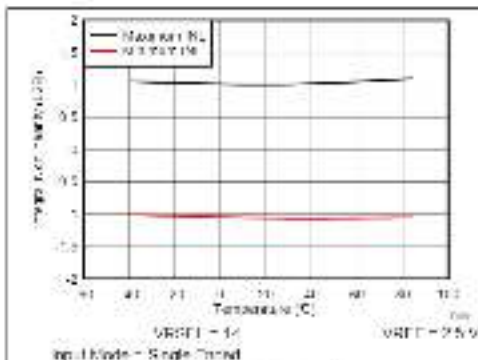


Figure 5-61: INL vs Temperature

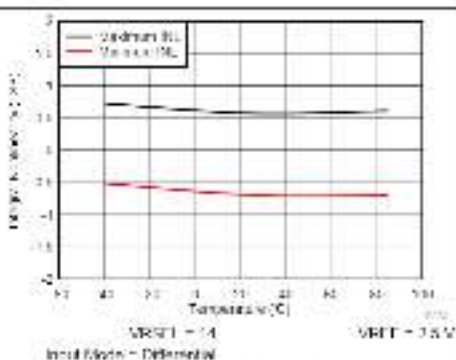


Figure 5-62: INL vs Temperature

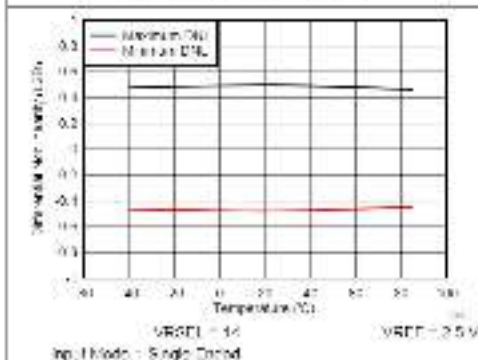


Figure 5-63: DNL vs Temperature

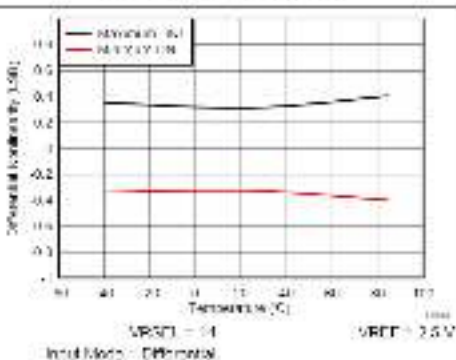


Figure 5-64: DNL vs Temperature

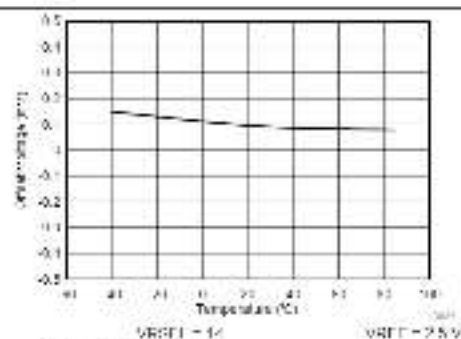


Figure 5-85. Offset Voltage vs Temperature

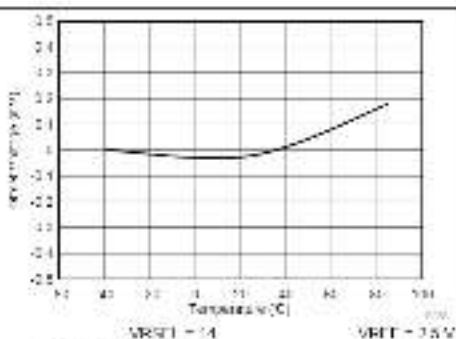


Figure 5-86. Offset Voltage vs Temperature

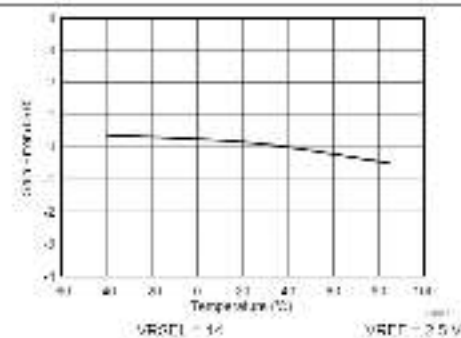


Figure 5-87. Gain Error vs Temperature

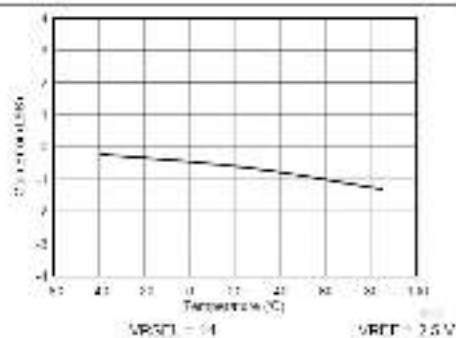


Figure 5-88. Gain Error vs Temperature

5.25.7 REF_A

Table 5-33 lists the characteristics of the REF_A built-in reference.

Table 5-33. REF_A, Built-In Reference (LDO Operation)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{DD}	MIN	TYP	MAX	UNIT
V _{REF} ⁽¹⁾	REFVSEL = (0) for 1.2 V, REFON = 1	1.02 V	1.2	±1%		V
	REFVSEL = (1) for 1.45 V, REFON = 1	1.75 V	1.45	±1%		
	REFVSEL = (2) for 1.5 V, REFON = 1	2.5 V	1.5	±1%		
V _{DD(boot)}	REFVSEL = (0) for 1.2 V		1.02			V
	REFVSEL = (1) for 1.45 V		1.75			
	REFVSEL = (2) for 1.5 V		2.5			
I _{DDA}	Operating supply current into ADC (internal)	REFON = 1	3 V	15	10	µA
I _{DDREF} ⁽²⁾	Max. maximum load current VREF+ terminal	REFVSEL = (0, 1, 2) A _{DDREF} = A _{DDREF} (for each reference level) REFON = REFOUT = 1		±1000	10	µA
I _{DDREF} ⁽²⁾	Load-current regulation, VREF+ terminal	REFVSEL = (0, 1, 2) V _{DDREF} = +10 µA or -1000 µA A _{DDREF} = A _{DDREF} (for each reference level) REFON = REFOUT = 1			2000	µV/mA
C _{LOAD} ⁽³⁾	Capacitance of VREF+, VREF+ terminal	REFON = REFOUT = 1		0	100	pF
PSRR _{DC} (DCL) after ADC buffer	Power supply rejection ratio (DCL) after ADC buffer	A _{DDREF} = A _{DDREF} (for each reference level) REFVSEL = (0, 1, 2), REFON = 1 REFOUT = 0		50	250	µV/V
PSRR _{DC} (DCL) after ADC buffer	Power supply rejection ratio (DCL) after ADC buffer	A _{DDREF} = A _{DDREF} (for each reference level) REFVSEL = (0, 1, 2), REFON = 1 REFOUT = 1		50	250	µV/V
PSRR _{AC} (DCL) after ADC buffer	Power supply rejection ratio (AC) after ADC buffer	A _{DDREF} = A _{DDREF} (for each reference level) f _{SWDCL} = 0.1 V at 1 kHz REFVSEL = (0, 1, 2), REFON = 1 REFOUT = 0		9	10	mV/V
PSRR _{AC} (DCL) after ADC buffer	Power supply rejection ratio (AC) after ADC buffer	A _{DDREF} = A _{DDREF} (for each reference level) f _{SWDCL} = 0.1 V at 1 kHz REFVSEL = (0, 1, 2), REFON = 1 REFOUT = 1		9	5	mV/V
TC _{VREF} ⁽²⁾	Temperature coefficient of built-in reference	REFVSEL = (0, 1, 2), REFON = 1 T _A = -40°C to 125°C		70	25	ppm/°C
I _{DDREF} ⁽²⁾	Settling time of reference voltage ⁽³⁾	A _{DDREF} = A _{DDREF} (for each reference level) REFVSEL = (0, 1, 2), REFON = 0 → 1		20	10	µs

(1) The reference voltage current is supplied from internal VDD.

(2) Calculated using the box method: MAX: -40°C to 25°C; MIN: -40°C to 25°C; MIN: -40°C to 25°C; MAX: -40°C to 25°C; 25°C to 125°C.

(3) The condition is that the error of a ADC converter calculated due to I_{DDREF} is less than 0.5 LSB.

5.25.8 Comparator_E

Table 5-34 lists the characteristics of the comparator.

Table 5-34. Comparator_E

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT	
V _{DD}	Supply voltage		1.8		3.7	V	
I _{quiescent}	Comparator operating with supply current into AVCC. Includes reference resistor loading.	CEPWIND = 00, CEON = 1, CDRSX = 00 (idle)	2.2 V, 3 V	10	19	µA	
		CEPWIND = 01, CEON = 1, CDRSX = 00 (medium)	2.2 V, 3 V	8	10		
		CEPWIND = 10, CEON = 1, CDRSX = 00 (slow), T _A = 50°C	2.2 V, 3 V		0.5		
		CEPWIND = 10, CEON = 1, CDRSX = 00 (slow), T _A = 50°C	2.2 V, 3 V		0.5		
I _{quiescent}	Quiescent current of resistor loaded into AVCC. Includes I _{REF} and I _{REF} current.	CEPWIND = 0, CDRSX = 01, CDRSX = 10, REFON = 0, CEON = 0	2.2 V, 3 V	25	30	µA	
		CEPWIND = 1, CDRSX = 01, CDRSX = 10, REFON = 0, CEON = 0	2.2 V, 3 V	10	15		
V _{REF}	Reference voltage level	CDRSX = 11, CDRSX = 01, CDRSX = 0	1.63 V	1.17	1.2	1.20	V
		CDRSX = 11, CDRSX = 10, CDRSX = 0	2.2 V	1.95	2.0	2.00	
		CDRSX = 11, CDRSX = 11, CDRSX = 0	2.2 V	2.40	2.5	2.60	
		CDRSX = 11, CDRSX = 01, CDRSX = 1	1.62 V	1.15	1.2	1.20	
		CDRSX = 11, CDRSX = 10, CDRSX = 1	2.2 V	1.95	2.0	2.00	
		CDRSX = 11, CDRSX = 11, CDRSX = 1	2.2 V	2.5	2.5	2.6	
V _{CM}	Common-mode input range			0	V _{DD} - 1	V	
V _{offset}	Input offset voltage	CEPWIND = 10		-10	+10	mV	
		CEPWIND = 01		25	100		
C _{in}	Input capacitance	CEPWIND = 00 or CEPWIND = 01		8		pF	
		CEPWIND = 10		8			
R _{on}	Series input resistance	On (switch closed)		4	4	Ω	
		Off (switch open)		20		MΩ	
t _{pd}	Propagation delay response (100%)	CEPWIND = 10, CDRSX = 0, CDRSX > 20 mV		300	500	ns	
		CEPWIND = 01, CDRSX = 0, CDRSX > 20 mV		410	500		
		CEPWIND = 10, CDRSX = 0, CDRSX > 20 mV			90	µs	
t _{rise}	Rise time delay with 100% swing	CEPWIND = 00 or 01, CDRSX = 1, CDRSX > 20 mV, CDRSX = 10		1.5	1.8	µs	
		CEPWIND = 00 or 01, CDRSX = 1, CDRSX > 20 mV, CDRSX = 10		1.1	1.6		
		CEPWIND = 10 or 01, CDRSX = 1, CDRSX > 20 mV, CDRSX = 10		1	1		
		CEPWIND = 10 or 01, CDRSX = 1, CDRSX > 20 mV, CDRSX = 10		1	1		

Comparator_E (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{CC_COMP}	C _{COMP} = 0 to 1, C _{COMP} = 10 nF V _{INP} = V _{IN} from 0V to V _{CC} Overdrive > 20 mV			0.5		μA
	C _{COMP} = 0 to 1, C _{COMP} = 10 nF V _{INP} = V _{IN} from 0V to V _{CC} Overdrive > 20 mV			0.5	1.2	μA
	C _{COMP} = 0 to 1, C _{COMP} = 10 nF V _{INP} = V _{IN} from 0V to V _{CC} Overdrive > 20 mV			15	25	μA
	C _{COMP} = 0 to 1, C _{COMP} = 10 nF C _{REFLX} = 10, C _{REFLX} = 11 REFON = 0, Overdrive > 20 mV			50	120	μA
	C _{COMP} = 0 to 1, C _{COMP} = 10 nF C _{REFLX} = 10, C _{REFLX} = 11 REFON = 0, Overdrive > 20 mV			50	120	μA
I _{CC_COMP_REF}	C _{COMP} = 0 to 1, C _{COMP} = 10 nF C _{REFLX} = 10, C _{REFLX} = 11 REFON = 0, Overdrive > 20 mV			50	120	μA
	C _{COMP} = 0 to 1, C _{COMP} = 10 nF C _{REFLX} = 10, C _{REFLX} = 11 REFON = 0, C _{REFLX} = 0x0F, Overdrive > 20 mV			50	100	μA
	C _{COMP} = 0 to 1, C _{COMP} = 10 nF C _{REFLX} = 10, C _{REFLX} = 11 REFON = 0, C _{REFLX} = 0x0F, Overdrive > 20 mV			50	100	μA
	C _{COMP} = 0 to 1, C _{COMP} = 10 nF C _{REFLX} = 10, C _{REFLX} = 11 REFON = 0, C _{REFLX} = 0x0F, Overdrive > 20 mV			50	100	μA
I _{CC_COMP_REF}	C _{COMP} = 0 to 1, C _{COMP} = 10 nF C _{REFLX} = 10, C _{REFLX} = 11 REFON = 0, C _{REFLX} = 0x0F, Overdrive > 20 mV			1.5	2	μA
	C _{COMP} = 0 to 1, C _{COMP} = 10 nF C _{REFLX} = 10, C _{REFLX} = 11 REFON = 0, C _{REFLX} = 0x0F, Overdrive > 20 mV			1.5	2	μA
	C _{COMP} = 0 to 1, C _{COMP} = 10 nF C _{REFLX} = 10, C _{REFLX} = 11 REFON = 0, C _{REFLX} = 0x0F, Overdrive > 20 mV			15	25	μA
V _{CM_REF}	V _{IN} = reference voltage to 0V to 1V V _{CC} = 0 to 1V		V _{IN} = 0V to 1V V _{CC} = 0V to 1V	V _{IN} = 0V to 1V V _{CC} = 0V to 1V	V _{IN} = 0V to 1V V _{CC} = 0V to 1V	V

5.25.9 eUSCI

Table 5-35 lists the supported clock frequencies of the eUSCI in UART mode.

Table 5-35. eUSCI (UART Mode) Clock Frequency

PARAMETER	TEST CONDITIONS	VCORE	VDD	MIN	MAX	UNIT
f _{UART}	eUSCI input clock frequency Internal: BRCLK External: LCLK Data rate = BRCLK * 10%	1.2 V		11		kHz
		1.4 V		24		
f _{STOP}	Baud rate mode frequency (equals baud rate in full rate)	1.2 V		5		kHz
		1.4 V		7		

Table 5-36 lists the characteristics of the eUSCI in UART mode.

Table 5-36. eUSCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{DD}	MIN	TYP	MAX	UNIT
t _{UART receive depth time} ⁽¹⁾	UC0LUTx = 0		5		20	ns
	UC0LUTx = 1		20		60	
	UC0LUTx = 2		30		100	
	UC0LUTx = 3		50		100	

(1) Pulses on the UART receive input (UC0RX) that are shorter than the UART receive depth time are suppressed. Thus, the extended depth time does not limit the maximum possible baud rate. To ensure that pulses are correctly recognized, the duration should exceed the maximum specification of the depth time.

Table 5-37 lists the supported clock frequencies of the eUSCI in SPI master mode.

Table 5-37. eUSCI (SPI Master Mode) Clock Frequency

PARAMETER	CONDITIONS	V _{DD}	MIN	TYP	MAX	UNIT
f _{UART}	eUSCI input clock frequency BRCLK * Data rate = 0% - 10%	VCORE = 1.2 V			12	kHz
		VCORE = 1.4 V			17	

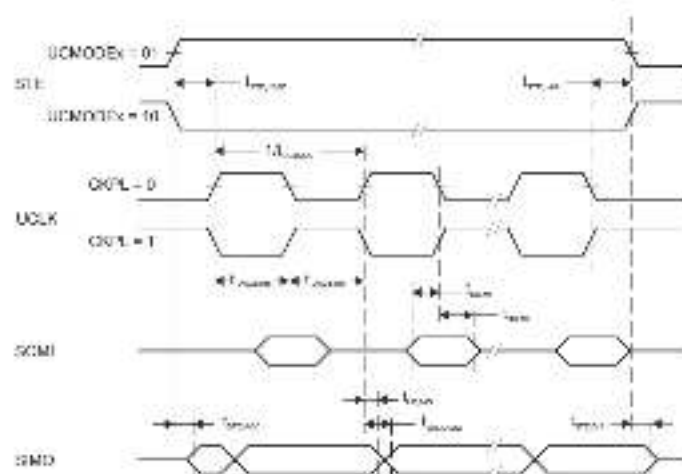


Figure 5-69. SPI Master Mode, CKPH = 0

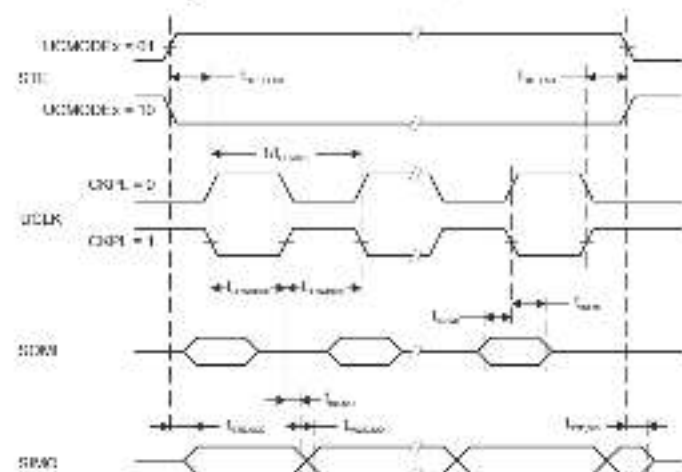


Figure 5-70. SPI Master Mode, CKPH = 1

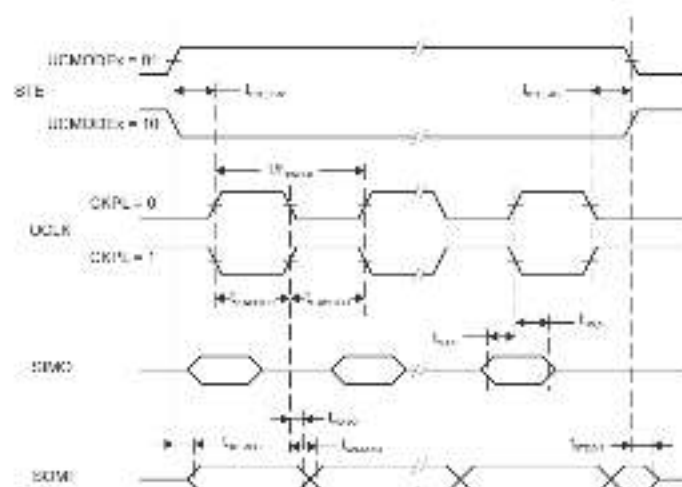


Figure 5-72. SPI Slave Mode, CKPH = 1

5.25.10 Timers

Table 5-42 lists the characteristics of Timer_A.

Table 5-42. Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{DD}	V _{DD}	MIN	MAX	UNIT
f _{TA} Timer_A input clock frequency	Internal TACLK External TACLK Duty cycle = 50% ± 0%	1.2 V			12	MHz
		1.4 V			24	
f _{UPDATE} Timer_A update period	All capture inputs, Minimum input duration required for capture			35	44	ns

Table 5-43 lists the characteristics of Timer32.

Table 5-43. Timer32

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{DD}	V _{DD}	MIN	MAX	UNIT
f _{TA} Timer32 operating clock frequency ⁽¹⁾		1.2 V			24	MHz
		1.4 V			48	

(1) Timer32 operates on the same clock as the Cortex-M3 CPU.

5.25.11 Memories

Table 5-44 lists the general characteristics of the flash memory.

Table 5-44. Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	MIN	MAX	UNIT
UVAC _{Program}	Supply voltage for program or erase	1.82	V
I _{Program} , max	Peak supply current from DVCC during program or erase	10	mA
Retention	Program or erase endurance ⁽¹⁾	10000	cycles
Reads	Data read time delay	20	ns

(1) Program or erase cycle for a bit is defined as the value of bit changing from 1 to 0 or 0 to 1.

Table 5-45 lists the characteristics of the flash operations using MSP432 peripheral driver libraries.

Table 5-45. Flash Operations Using MSP432 Peripheral Driver Libraries⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Prog_Acc_Wait	Program time for 32-bit data using ROM_FlashCtrl_programMemory() API VDDIO = 1.4 V, DVCC = 40 MHz	40		275	µs
Prog_Acc_Read	Program time for 32-bit data (data reading) using ROM_FlashCtrl_programMemory() API VDDIO = 1.4 V, DVCC = 40 MHz	65		71	ns
Prog_Acc_Erase	Erase erase time using ROM_FlashCtrl_eraseSector() API VDDIO = 1.4 V, DVCC = 40 MHz Number of erase or program cycles: 10x and 425x	9	350 ⁽²⁾		ns
Prog_Acc_Program	Mass erase time using ROM_FlashCtrl_performMassErase() API VDDIO = 1.4 V, DVCC = 40 MHz Number of erase or program cycles: 10x MSP432P401R devices with 256 KiB of flash memory	12	1000 ⁽²⁾		ns
	VDDIO = 1.4 V, DVCC = 40 MHz Number of erase or program cycles: 10x MSP432P401M devices with 128 KiB of flash memory	12	900 ⁽²⁾		ns
I _{Program} , av	Average supply current from DVCC during program using ROM_FlashCtrl_programMemory() API VDDIO = 1.2 V, DVCC = 30 MHz	5		7	mA
I _{Program} , av	Average supply current from DVCC during erase using ROM_FlashCtrl_eraseSector() API VDDIO = 1.2 V, DVCC = 30 MHz	2		3	mA

(1) MSP432 peripheral driver libraries accessed from ROM.

(2) The maximum value is theoretically calculated by multiplying the typical value by 1000 for the average erase or program cycles.

(3) The maximum value is theoretically calculated by multiplying the typical value by 1000 for the average erase or program cycles and the total number of sectors in the flash main memory.

Table 5-16 lists the characteristics of the flash stand-alone operations.

Table 5-16. Flash Stand-Alone Operations

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Flash Erase Latency	Asynchronous for 16K/32K-bit erase using immediate write mode	V _{DD} = 1.4V, V _{DD} PS = 1	70		µs
	Serial JTAG = 1, V _{DD} PS = 1		80		
Flash Program Latency	Asynchronous for 16K/32K-bit word using full word write mode	V _{TR_PRC} = 0, V _{TR_PST} = 1	40		µs
	V _{DD} = 1.4V, V _{DD} PS = 1		50		
Flash Read Latency	Program time for 16/32-bit word using burst write mode	AUTO_PRC = 0, AUTO_PST = 1	65		µs
	AUTO_PRC = 1, AUTO_PST = 1		65		
Flash	Time for sector erase or mass erase		9		ms
Flash _{prog}	Maximum number of pulses to complete program operations			2	
Flash _{erase}	Maximum number of pulses to complete erase operation	Number of erase or program cycles < 1K		24	
		Number of erase or program cycles < 1K and 10Ks		104	

Table 5-17 lists the characteristics of the SRAM.

Table 5-17. SRAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{DDQ} _{SRAM}	Current consumption of one SRAM bank when enabled	V _{DD} = 1.2 V	100	550	nA
	V _{DD} = 1.4 V		100	550	
I _{DDQ} _{SRAM}	Current consumption of one SRAM bank when disabled	V _{DD} = 1.2 V	30	125	nA
	V _{DD} = 1.4 V		30	120	
t _{SRAM} _{en}	Time taken to enable one SRAM bank		4	5	µs
t _{SRAM} _{dis}	Time taken to disable one SRAM bank		4	5	µs
t _{SRAM} _{en}	Time taken to enable all SRAM banks except Bank 0		7	8	µs
t _{SRAM} _{dis}	Time taken to disable all SRAM banks except Bank 0		8	9	µs

5.25.12 Emulation and Debug

Table 5-48 lists the characteristics of the JTAG interface.

Table 5-48. JTAG

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
f_{TCK} TCK clock frequency	0		10	MHz
t_{TCK} TCK clock period	100			ns
t_{TCK_iso} TCK clock low time		$t_{TCK}/2$		ns
t_{TCK_ohg} TCK clock high time		$t_{TCK}/2$		ns
t_{TCK_rise} TCK rise time	0		10	ns
t_{TCK_fall} TCK fall time	0		10	ns
t_{TMS_su} TMS setup time to TCK rise	20			ns
t_{TMS_ho} TMS hold time from TCK rise	0			ns
t_{TDI_su} TDI setup time to TCK rise	20			ns
t_{TDI_ho} TDI hold time from TCK rise	7			ns
t_{TDO_dv} TCK fall to data valid from high impedance		0	44	ns
t_{TDO_dr} TCK fall to data valid from drive valid		0	44	ns
t_{TDO_oh} TCK fall to high impedance from drive valid		0	50	ns



Figure 5-74. JTAG Test Clock Input Timing

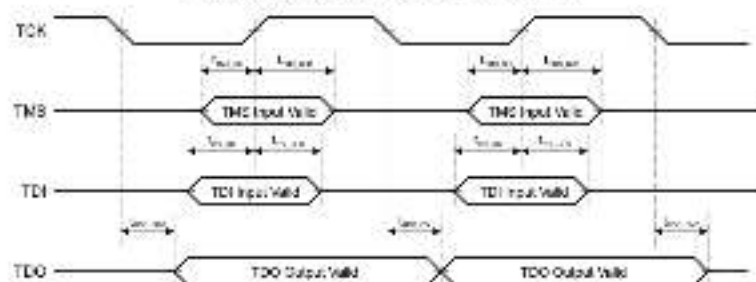


Figure 5-75. JTAG Test Access Port (TAP) Timing

6 Detailed Description

6.1 Overview

The MSP432P401x microcontroller is an ideal combination of the TI MSP430 low-power DNA, advanced mixed-signal features, and the processing capabilities of the ARM 32-bit Cortex-M4 RISC engine. The microcontrollers ship with bundled driver libraries and are compatible with standard components of the ARM ecosystem.

6.2 Processor and Execution Features

The Cortex-M4 processor provides a high-performance low-cost platform that meets system requirements of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts. The Thumb[®]-2 mixed 16- and 32-bit instruction set of this processor delivers the high performance that is expected of a 32-bit ARM core in a compact memory size usually associated with 8- and 18-bit devices (typically in the range of a few kilobytes of memory needed for microcontroller-class applications).

In the MSP432P401x MCUs, the Cortex-M4 processor can run up to 48 MHz, delivering high performance for the targeted class of applications, while at the same time maintaining ultra-low active power consumption.

6.2.1 Floating-Point Unit

The Cortex-M4 processor on the MSP432P401x MCUs includes a tightly coupled floating-point unit (FPU). The FPU is an IEEE 754 compliant single precision floating point module supporting add, subtract, multiply, divide, square-root, and square operations. It also provides conversion between fixed-point and floating-point data formats and floating point constant instructions.

6.2.2 Memory Protection Unit

The Cortex-M4 processor on the MSP432P401x MCUs includes a tightly coupled memory protection unit (MPU) that supports up to eight protection regions. Applications can use the MPU to enforce memory privilege rules that isolate processes from each other or enforce memory access rules. These features are typically required for operating system handling purposes.

6.2.3 Nested Vectored Interrupt Controller (NVIC)

The NVIC supports up to 84 interrupts with eight levels of interrupt priority. The Cortex-M4 NVIC architecture allows for low latency, efficient interrupt and event handling, and seamless integration to device-level power-control strategies.

6.2.4 SysTick

The Cortex-M4 includes an integrated system timer, SysTick, which provides a simple, 24-bit, clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used in several different ways, and it is typically deployed either for operating system related purposes or as a general-purpose alarm mechanism.

6.2.5 Debug and Trace Features

The Cortex-M4 processor implements a complete hardware debug solution and provides high system visibility of the processor and memory through either a traditional 4-pin JTAG port or a 2-pin Serial Wire Debug (SWD) port, which is local for microcontrollers and other small-package devices. The SWD-DP interface combines the SWD and JTAG debug ports into one module, which allows a seamless switch between the 2-pin and 4-pin modes of operation, depending on application needs.

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Figure 6-2. Code Zone Memory Map

6.3.1.1 Flash Memory Region

The 4MB region from 0x0000_0000 to 0x000F_FFFF is defined as the flash memory region. This region is further divided into different types of flash memory regions, which are explained in [Section 6.4.1](#).

6.3.1.2 SRAM Region

The 1MB region from 0x0100_0000 to 0x010F_FFFF is defined as the SRAM region. This region is also placed in the SRAM zone of the device, thereby allowing efficient access to the SRAM, both for instruction fetches and data reads. See [Section 6.4.2](#) for more details.

6.3.1.3 ROM Region

The 1MB region from 0x0200_0000 to 0x020F_FFFF is defined as the ROM region. See [Section 6.4.3](#) for details about the ROM.

6.3.2 SRAM Zone Memory Map

The SRAM zone of the device lies in the address range of 0x2000_0000 to 0x3FFF_FFFF. [Figure 6-3](#) shows how this zone is divided.



Figure 6-3. SRAM Zone Memory Map

6.3.2.1 SRAM Region

The 1MB region from 0x2000_0000 to 0x2000_FFFF is defined as the SRAM region. The SRAM accessible in this region is also aliased in the Code zone of the device, thereby allowing efficient access to the SRAM, both for instruction fetches and data reads. See [Section 6.4.2](#) for details about the SRAM.

6.3.2.2 SRAM Bit-Band Alias Region

The 32MB region from 0x2000_0000 through 0x23FF_FFFF forms the bit-band alias region for the 1-MB SRAM region. Bit-banding is a feature of the Cortex-M4 processor and allows the application to set or clear individual bits throughout the SRAM space without using the pipeline bandwidth of the processor to carry out an exclusive read-modify-write sequence.

6.3.3 Peripheral Zone Memory Map

The Peripheral zone of this device lies in the address range of 0x4000_0000 to 0x5FFF_FFFF. [Figure 6-4](#) shows how this range is further divided.



Figure 6-4. Peripheral Zone Memory Map

6.3.3.1 Peripheral Region

The 1MB region from 0x4000_0000 to 0x400F_FFFF is dedicated to the system and application control peripherals of the device. On the MSP432P401x MCUs, a total of 128KB of this region is dedicated for peripherals, while the rest is reserved. Table 6-1 lists the peripheral allocation within this 128-KB space. Note that all peripherals may not be available in all devices of the family (details in the REMARKS column). If a peripheral is listed as N/A for a particular device, treat the corresponding address space as reserved.

NOTE

Peripherals that are marked as 16-bit should be accessed through byte or half-word read or write only. Any 32-bit access to these peripherals results in a bus error response.

Table 6-1. Peripheral Address Offsets

ADDRESS RANGE	PERIPHERAL	TABLE	REMARKS
0x4000_0000-0x4000_03FF	Timer_A0	Table 6-2	16-bit peripheral
0x4000_0400-0x4000_07FF	Timer_A1	Table 6-3	16-bit peripheral
0x4000_0800-0x4000_0BFF	Timer_A2	Table 6-4	16-bit peripheral
0x4000_0C00-0x4000_0FFF	Timer_A3	Table 6-5	16-bit peripheral
0x4000_1000-0x4000_13FF	GPIO_A0	Table 6-6	16-bit peripheral
0x4000_1400-0x4000_17FF	GPIO_A1	Table 6-7	16-bit peripheral
0x4000_1800-0x4000_1BFF	GPIO_A2	Table 6-8	16-bit peripheral
0x4000_1C00-0x4000_1FFF	USQL_A3	Table 6-9	16-bit peripheral
0x4000_2000-0x4000_23FF	GPIO_B0	Table 6-10	16-bit peripheral
0x4000_2400-0x4000_27FF	USQL_B1	Table 6-11	16-bit peripheral

Table 6-1. Peripheral Address Offsets (continued)

Table 6-3. Timer_A1 Registers (Base Address: 0x4000_0400)

REGISTER NAME	ACRONYM	OFFSET
Timer_A1 Control	TA1CTL	0x0
Timer_A1 Capture/Compare Control 0	TA1CC0R	0x10
Timer_A1 Capture/Compare Control 1	TA1CC1R	0x14
Timer_A1 Capture/Compare Control 2	TA1CC2R	0x18
Timer_A1 Capture/Compare Control 3	TA1CC3R	0x1C
Timer_A1 Capture/Compare Control 4	TA1CC4R	0x20
Timer_A1 Counter	TA1CR	0x24
Timer_A1 Capture/Compare 0	TA1CCR0	0x28
Timer_A1 Capture/Compare 1	TA1CCR1	0x2C
Timer_A1 Capture/Compare 2	TA1CCR2	0x30
Timer_A1 Capture/Compare 3	TA1CCR3	0x34
Timer_A1 Capture/Compare 4	TA1CCR4	0x38
Timer_A1 Interrupt Vector	TA1IV	0x3C
Timer_A1 Expansion 0	TA1EX0	0x40

Table 6-4. Timer_A2 Registers (Base Address: 0x4000_0800)

REGISTER NAME	ACRONYM	OFFSET
Timer_A2 Control	TA2CTL	0x0
Timer_A2 Capture/Compare Control 0	TA2CC0R	0x10
Timer_A2 Capture/Compare Control 1	TA2CC1R	0x14
Timer_A2 Capture/Compare Control 2	TA2CC2R	0x18
Timer_A2 Capture/Compare Control 3	TA2CC3R	0x1C
Timer_A2 Capture/Compare Control 4	TA2CC4R	0x20
Timer_A2 Counter	TA2CR	0x24
Timer_A2 Capture/Compare 0	TA2CCR0	0x28
Timer_A2 Capture/Compare 1	TA2CCR1	0x2C
Timer_A2 Capture/Compare 2	TA2CCR2	0x30
Timer_A2 Capture/Compare 3	TA2CCR3	0x34
Timer_A2 Capture/Compare 4	TA2CCR4	0x38
Timer_A2 Interrupt Vector	TA2IV	0x3C
Timer_A2 Expansion 0	TA2EX0	0x40

Table 6-5. Timer_A3 Registers (Base Address: 0x4000_0C00)

REGISTER NAME	ACRONYM	OFFSET
Timer_A3 Control	TA3CTL	0x0
Timer_A3 Capture/Compare Control 0	TA3CC0R	0x10
Timer_A3 Capture/Compare Control 1	TA3CC1R	0x14
Timer_A3 Capture/Compare Control 2	TA3CC2R	0x18
Timer_A3 Capture/Compare Control 3	TA3CC3R	0x1C
Timer_A3 Capture/Compare Control 4	TA3CC4R	0x20
Timer_A3 Counter	TA3CR	0x24
Timer_A3 Capture/Compare 0	TA3CCR0	0x28
Timer_A3 Capture/Compare 1	TA3CCR1	0x2C
Timer_A3 Capture/Compare 2	TA3CCR2	0x30
Timer_A3 Capture/Compare 3	TA3CCR3	0x34
Timer_A3 Capture/Compare 4	TA3CCR4	0x38
Timer_A3 Interrupt Vector	TA3IV	0x3C

Table 6-5. Timer_A3 Registers (Base Address: 0x4000_0C00) (continued)

REGISTER NAME	ACRONYM	OFFSET
Timer_A3 Expansion 0	TAEK0	20h

Table 6-6. eUSCI_A0 Registers (Base Address: 0x4000_1000)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_A0 Control Word 0	UCA0CTLW0	00h
eUSCI_A0 Control Word 1	UCA0CTLW1	02h
eUSCI_A0 Basic Mode Control	UCA0B0MW	08h
eUSCI_A0 Modulation Control	UCA0M0CTW	09h
eUSCI_A0 Status	UCA0S0ATW	0Ah
eUSCI_A0 Receive Buffer	UCA0RXBUF	0Ch
eUSCI_A0 Transmit Buffer	UCA0TXBUF	0Dh
eUSCI_A0 Auto-Baud Rate Control	UCA0ABCTL	0Eh
eUSCI_A0 I/OA Control	UCA0IOCTL	10h
eUSCI_A0 Interrupt Enable	UCA0IE	1Ah
eUSCI_A0 Interrupt Flag	UCA0IFG	1Ch
eUSCI_A0 Interrupt Vector	UCA0IN	1Eh

Table 6-7. eUSCI_A1 Registers (Base Address: 0x4000_1400)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_A1 Control Word 0	UCA1CTLW0	00h
eUSCI_A1 Control Word 1	UCA1CTLW1	02h
eUSCI_A1 Basic Mode Control	UCA1B1MW	08h
eUSCI_A1 Modulation Control	UCA1M1CTW	09h
eUSCI_A1 Status	UCA1S1ATW	0Ah
eUSCI_A1 Receive Buffer	UCA1RXBUF	0Ch
eUSCI_A1 Transmit Buffer	UCA1TXBUF	0Dh
eUSCI_A1 Auto-Baud Rate Control	UCA1ABCTL	0Eh
eUSCI_A1 I/OA Control	UCA1IOCTL	10h
eUSCI_A1 Interrupt Enable	UCA1IE	1Ah
eUSCI_A1 Interrupt Flag	UCA1IFG	1Ch
eUSCI_A1 Interrupt Vector	UCA1IN	1Eh

Table 6-8. eUSCI_A2 Registers (Base Address: 0x4000_1800)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_A2 Control Word 0	UCA2CTLW0	00h
eUSCI_A2 Control Word 1	UCA2CTLW1	02h
eUSCI_A2 Basic Mode Control	UCA2B2MW	08h
eUSCI_A2 Modulation Control	UCA2M2CTW	09h
eUSCI_A2 Status	UCA2S2ATW	0Ah
eUSCI_A2 Receive Buffer	UCA2RXBUF	0Ch
eUSCI_A2 Transmit Buffer	UCA2TXBUF	0Dh
eUSCI_A2 Auto-Baud Rate Control	UCA2ABCTL	0Eh
eUSCI_A2 I/OA Control	UCA2IOCTL	10h
eUSCI_A2 Interrupt Enable	UCA2IE	1Ah
eUSCI_A2 Interrupt Flag	UCA2IFG	1Ch
eUSCI_A2 Interrupt Vector	UCA2IN	1Eh

Table 6-9. eUSCI_A3 Registers (Base Address: 0x4000_1C00)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_A3 Control Word 0	UCA3CTLW0	0Ch
eUSCI_A3 Control Word 1	UCA3CTLW1	01h
eUSCI_A3 Baud Rate Control	UCA3BRW	02h
eUSCI_A3 Modem Control	UCA3MCTLW	03h
eUSCI_A3 Status	UCA3STATW	04h
eUSCI_A3 Receive Buffer	UCA3RXBUF	0Ch
eUSCI_A3 Transmitt Buffer	UCA3TXBUF	07h
eUSCI_A3 Auto Baud Rate Control	UCA3ABCTL	10h
eUSCI_A3 I/OA Control	UCA3IOCTL	12h
eUSCI_A3 Interrupt Enable	UCA3IE	16h
eUSCI_A3 Interrupt Flag	UCA3IFG	1Ch
eUSCI_A3 Interrupt Vector	UCA3IV	1Eh

Table 6-10. eUSCI_B0 Registers (Base Address: 0x4000_2000)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_B0 Control Word 0	UCB0CTLW0	0Ch
eUSCI_B0 Control Word 1	UCB0CTLW1	01h
eUSCI_B0 Baud Rate Control Word	UCB0BRW	02h
eUSCI_B0 Status Word	UCB0STATW	03h
eUSCI_B0 Byte Counter Threshold	UCB0TCN1	04h
eUSCI_B0 Receive Buffer	UCB0RXBUF	0Ch
eUSCI_B0 Transmitt Buffer	UCB0TXBUF	07h
eUSCI_B0 I2C Own Address 0	UCB0I2COA0	14h
eUSCI_B0 I2C Own Address 1	UCB0I2COA1	1Ch
eUSCI_B0 I2C Own Address 2	UCB0I2COA2	18h
eUSCI_B0 I2C Own Address 3	UCB0I2COA3	1Ah
eUSCI_B0 I2C Slave Address	UCB0I2ADR0	1Ch
eUSCI_B0 Acknowledge Mask	UCB0ACKMASK	1Bh
eUSCI_B0 I2C Slave Address	UCB0I2SRA	17h
eUSCI_B0 Interrupt Enable	UCB0IE	24h
eUSCI_B0 Interrupt Flag	UCB0IFG	2Ch
eUSCI_B0 Interrupt Vector	UCB0IV	27h

Table 6-11. eUSCI_B1 Registers (Base Address: 0x4000_2400)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_B1 Control Word 0	UCB1CTLW0	0Ch
eUSCI_B1 Control Word 1	UCB1CTLW1	02h
eUSCI_B1 Baud Rate Control Word	UCB1BRW	03h
eUSCI_B1 Status Word	UCB1STATW	04h
eUSCI_B1 Byte Counter Threshold	UCB1TCN1	09h
eUSCI_B1 Receive Buffer	UCB1RXBUF	0Ch
eUSCI_B1 Transmitt Buffer	UCB1TXBUF	07h
eUSCI_B1 I2C Own Address 0	UCB1I2COA0	14h
eUSCI_B1 I2C Own Address 1	UCB1I2COA1	1Ch
eUSCI_B1 I2C Own Address 2	UCB1I2COA2	18h
eUSCI_B1 I2C Own Address 3	UCB1I2COA3	1Ah
eUSCI_B1 I2C Slave Address	UCB1I2ADR0	1Ch

Table 6-11. eUSCI_B1 Registers (Base Address: 0x4000_2400) (continued)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_B1 Address Mask	UCB1ADDRMASK	12h
eUSCI_B1 TX Data Base Address	UCB1PDATA	20h
eUSCI_B1 Interrupt Enable	UCB1IE	24h
eUSCI_B1 Interrupt Flag	UCB1IFG	2Ch
eUSCI_B1 Interrupt Vector	UCB1IV	28h

Table 6-12. eUSCI_B2 Registers (Base Address: 0x4000_2800)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_B2 Control Word 0	UCB2CTRLW0	00h
eUSCI_B2 Control Word 1	UCB2CTRLW1	04h
eUSCI_B2 Clock Rate Control Word	UCB2CRW	0Ch
eUSCI_B2 Status Word	UCB2STATUS	08h
eUSCI_B2 Byte Counter Threshold	UCB2TCNT	0Ah
eUSCI_B2 Receive Buffer	UCB2RXBUF	0Ch
eUSCI_B2 Transmit Buffer	UCB2TXBUF	0Eh
eUSCI_B2 I2C Own Address 0	UCB2IOCA0	14h
eUSCI_B2 I2C Own Address 1	UCB2IOCA1	18h
eUSCI_B2 I2C Own Address 2	UCB2IOCA2	1Ch
eUSCI_B2 I2C Own Address 3	UCB2IOCA3	1Eh
eUSCI_B2 Received Address	UCB2ADRESA	1Ch
eUSCI_B2 Address Mask	UCB2ADDRMASK	12h
eUSCI_B2 TX Data Base Address	UCB2PDATA	20h
eUSCI_B2 Interrupt Enable	UCB2IE	24h
eUSCI_B2 Interrupt Flag	UCB2IFG	2Ch
eUSCI_B2 Interrupt Vector	UCB2IV	28h

Table 6-13. eUSCI_B3 Registers (Base Address: 0x4000_2C00)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_B3 Control Word 0	UCB3CTRLW0	00h
eUSCI_B3 Control Word 1	UCB3CTRLW1	04h
eUSCI_B3 Clock Rate Control Word	UCB3CRW	0Ch
eUSCI_B3 Status Word	UCB3STATUS	08h
eUSCI_B3 Byte Counter Threshold	UCB3TCNT	0Ah
eUSCI_B3 Receive Buffer	UCB3RXBUF	0Ch
eUSCI_B3 Transmit Buffer	UCB3TXBUF	0Eh
eUSCI_B3 I2C Own Address 0	UCB3IOCA0	14h
eUSCI_B3 I2C Own Address 1	UCB3IOCA1	18h
eUSCI_B3 I2C Own Address 2	UCB3IOCA2	1Ch
eUSCI_B3 I2C Own Address 3	UCB3IOCA3	1Eh
eUSCI_B3 Received Address	UCB3ADRESA	1Ch
eUSCI_B3 Address Mask	UCB3ADDRMASK	12h
eUSCI_B3 TX Data Base Address	UCB3PDATA	20h
eUSCI_B3 Interrupt Enable	UCB3IE	24h
eUSCI_B3 Interrupt Flag	UCB3IFG	2Ch
eUSCI_B3 Interrupt Vector	UCB3IV	28h

Table 6-14. REF_A Registers (Base Address: 0x4000_3000)

REGISTER NAME	ACRONYM	OFFSET
REF_A Control 0	REFCTL0	0Ch

Table 6-15. COMP_E0 Registers (Base Address: 0x4000_3400)

REGISTER NAME	ACRONYM	OFFSET
Comparator_E0 Control 0	CECTL0	0Ch
Comparator_E0 Control 1	CECTL1	02h
Comparator_E0 Control 2	CECTL2	04h
Comparator_E0 Control 3	CECTL3	06h
Comparator_E0 Interrupt	CEINT	0Ch
Comparator_E0 Interrupt Vector Word	CEIM	0Ch

Table 6-16. COMP_E1 Registers (Base Address: 0x4000_3800)

REGISTER NAME	ACRONYM	OFFSET
Comparator_E1 Control 0	CECTL0	0Ch
Comparator_E1 Control 1	CECTL1	02h
Comparator_E1 Control 2	CECTL2	04h
Comparator_E1 Control 3	CECTL3	06h
Comparator_E1 Interrupt	CEINT	0Ch
Comparator_E1 Interrupt Vector Word	CEIM	0Ch

Table 6-17. AES256 Registers (Base Address: 0x4000_3C00)

REGISTER NAME	ACRONYM	OFFSET
AES Accelerator Control 0	AESACTL0	0Ch
AES Accelerator Control 1	AESACTL1	02h
AES Accelerator Status	AESASVAL	04h
AES Accelerator Key	AESKEY	06h
AES Accelerator Data In	AESADIN	08h
AES Accelerator Data Out	AESADOUT	0Ah
AES Accelerator Xored Data In	AESAXIN	0Ch
AES Accelerator Xored Data In (on trigger)	AESAXIN	0Bh

Table 6-18. CRC32 Registers (Base Address: 0x4000_4000)

REGISTER NAME	ACRONYM	OFFSET
CRC32 Data Input Low	CRC32DI_L	000h
CRC32 Data In Reverse Low	CRC32DIR_L	004h
CRC32 Initialization and Result Low	CRC32NIRS_L0	008h
CRC32 Initialization and Result High	CRC32NIRS_H	00Ch
CRC32 Result Reverse Low	CRC32RESR_L0	00Ch
CRC32 Result Reverse High	CRC32RESR_H	00Fh
CRC32 Data Input Low	CRC32DI	010h
CRC32 Data In Reverse Low	CRC32DIR	014h
CRC32 Initialization and Result	CRC32NIRS	018h
CRC32 Result Reverse	CRC32RESR	01Ch

Table 6-19. RTC_C Registers (Base Address: 0x4000_4400)

REGISTER NAME	ACRONYM	OFFSET
Real-Time Clock Control 0	RTCCCTL0	0x0
Real-Time Clock Control 1, 2	RTCCCTL1	0x1
Real-Time Clock Offset Calibration	RTCCCAL	0x2
Real-Time Clock Temperature Compensation	RTCCTMP	0x3
Real-Time Prescaler Timer 0 Control	RTCCPRCTL	0x4
Real-Time Prescaler Timer 1 Control	RTCCPRCTL	0x5
Real-Time Prescaler Timer 0, 1 Counter	RTCCPR	0x6
Real-Time Clock Interrupt Vector	RTCCIV	0x7
Real-Time Clock Seconds/Minutes	RTCCSEC	0x8
Real-Time Clock Hour/Day of Week	RTCCHR	0x9
Real-Time Clock Date	RTCCDATE	0xA
Real-Time Clock Year	RTCCYR	0xB
Real-Time Clock Minutes/Hours Alarm	RTCCMINHR	0xC
Real-Time Clock Day of Week/Day of Month Alarm	RTCCDOWDAY	0xD
Real-Time Clock Comparison	RTCCCMPVAL	0xE
RTC to Binary Converter	RTCCO2BIN	0xF

Table 6-20. WDT_A Registers (Base Address: 0x4000_4800)

REGISTER NAME	ACRONYM	OFFSET
Watchdog Timer Control	WDTCTL	0x0

Table 6-21. Port Registers (Base Address: 0x4000_4C00)

REGISTER NAME	ACRONYM	OFFSET
Port 1 Input	P1IN	0x0
Port 2 Input	P2IN	0x1
Port 1 Output	P1OUT	0x2
Port 2 Output	P2OUT	0x3
Port 1 Direction	P1DIR	0x4
Port 2 Direction	P2DIR	0x5
Port 1 Register Enable	P1REN	0x6
Port 2 Register Enable	P2REN	0x7
Port 1 Drive Strength	P1DS	0x8
Port 2 Drive Strength	P2DS	0x9
Port 1 Slew Rate	P1SLW	0xA
Port 2 Slew Rate	P2SLW	0xB
Port 1 Interrupt Vector	P1IV	0xC
Port 1 Complement Selection	P1SEL0	0xD
Port 2 Complement Selection	P2SEL0	0xE
Port 1 Interrupt Edge Select	P1IES	0xF
Port 2 Interrupt Edge Select	P2IES	0x10
Port 1 Interrupt Enable	P1IE	0x11
Port 2 Interrupt Enable	P2IE	0x12
Port 1 Interrupt Flag	P1IFG	0x13
Port 2 Interrupt Flag	P2IFG	0x14
Port 1 Interrupt Vector	P1IV	0x15
Port 2 Interrupt Vector	P2IV	0x16
Port 1 Input	P1IN	0x17

Table 6-21. Port Registers (Base Address: 0x4000_4C00) (continued)

REGISTER NAME	ACRONYM	OFFSET
Port 4 Input	PAIN	021h
Port 4 Output	PAOUT	022h
Port 4 Output	PAOUT	023h
Port 4 Direction	PAIR	024h
Port 4 Direction	PAIR	025h
Port 4 Resistor Enable	PAREN	026h
Port 4 Resistor Enable	PAREN	027h
Port 4 Select 0	PASEL0	028h
Port 4 Select 0	PASEL0	029h
Port 4 Select 1	PASEL1	02Ah
Port 4 Interrupt Vector	PAIV	02Bh
Port 4 Complement Selection	PASEL0	02Ch
Port 4 Complement Selection	PASEL0	02Dh
Port 4 Interrupt Edge Select	PAIES	02Eh
Port 4 Interrupt Enable	PAIE	02Fh
Port 4 Interrupt Enable	PAIE	030h
Port 4 Interrupt Flag	PAIFS	031h
Port 4 Interrupt Flag	PAIFS	032h
Port 4 Interrupt Vector	PAIV	033h
Port 4 Input	PAIN	034h
Port 4 Input	PAIN	035h
Port 4 Output	PAOUT	036h
Port 4 Output	PAOUT	037h
Port 4 Direction	PAIR	038h
Port 4 Direction	PAIR	039h
Port 4 Resistor Enable	PAREN	03Ah
Port 4 Resistor Enable	PAREN	03Bh
Port 4 Select 0	PASEL0	03Ch
Port 4 Select 1	PASEL1	03Dh
Port 4 Select 1	PASEL1	03Eh
Port 4 Interrupt Vector	PAIV	03Fh
Port 4 Complement Selection	PASEL0	040h
Port 4 Complement Selection	PASEL0	041h
Port 4 Interrupt Edge Select	PAIES	042h
Port 4 Interrupt Enable	PAIE	043h
Port 4 Interrupt Enable	PAIE	044h
Port 4 Interrupt Flag	PAIFS	045h
Port 4 Interrupt Flag	PAIFS	046h
Port 4 Interrupt Vector	PAIV	047h
Port 4 Input	PAIN	048h
Port 4 Input	PAIN	049h
Port 4 Output	PAOUT	04Ah
Port 4 Output	PAOUT	04Bh

Table 6-22. PMAP Registers (Base Address: 0x4000_5000)

REGISTER NAME	ACRONYM	OFFSET
Port Mapping Key	PMKEYID	0Ch
Port Mapping Control	PMCTRL	0Th
Port Mapping M0	PMMA0	10h
Port Mapping M1	PMMA1	14h
Port Mapping M2	PMMA2	18h
Port Mapping M3	PMMA3	1Ch
Port Mapping M4	PMMA4	1Eh
Port Mapping M5	PMMA5	20h
Port Mapping M6	PMMA6	24h
Port Mapping M7	PMMA7	28h
Port Mapping M8	PMMA8	2Ch
Port Mapping M9	PMMA9	30h
Port Mapping M10	PMMA10	34h
Port Mapping M11	PMMA11	38h
Port Mapping M12	PMMA12	3Ch
Port Mapping M13	PMMA13	40h
Port Mapping M14	PMMA14	44h
Port Mapping M15	PMMA15	48h
Port Mapping M16	PMMA16	4Ch
Port Mapping M17	PMMA17	50h
Port Mapping M18	PMMA18	54h
Port Mapping M19	PMMA19	58h
Port Mapping M20	PMMA20	5Ch
Port Mapping M21	PMMA21	60h
Port Mapping M22	PMMA22	64h
Port Mapping M23	PMMA23	68h
Port Mapping M24	PMMA24	6Ch
Port Mapping M25	PMMA25	70h
Port Mapping M26	PMMA26	74h
Port Mapping M27	PMMA27	78h

Table 6-23. Capacitive Touch I/O 0 Registers (Base Address: 0x4000_5400)

REGISTER NAME	ACRONYM	OFFSET
Capacitive Touch I/O 0 Control	CAT0CTRL	0Ch

Table 6-24. Capacitive Touch I/O 1 Registers (Base Address: 0x4000_5800)

REGISTER NAME	ACRONYM	OFFSET
Capacitive Touch I/O 1 Control	CAT1CTRL	0Ch

Table 6-25. Timer32 Registers (Base Address: 0x4000_C000)

REGISTER NAME	ACRONYM	OFFSET
Timer 1 Load	T32LOAD1	0Ch
Timer 1 Current Value	T32VAL1	0Eh
Timer 1 Timer Control	T32CONTROL1	0Fh
Timer 1 Interrupt Clear	T32INTCLR	10h
Timer 1 Interrupt Status	T32INTS1	12h
Timer 1 Interrupt Status	T32INTS1	14h
Timer 1 Interrupt Load	T32INTLOAD1	16h
Timer 2 Load	T32LOAD2	20h
Timer 2 Current Value	T32VAL2	22h

Table 6-25. Timer32 Registers (Base Address: 0x4000_C000) (continued)

REGISTER NAME	ACRONYM	OFFSET
Timer2 Timer Control	TS2CONTROL2	28h
Timer2 Interrupt Status	TS2INTSTAT	2Ch
Timer2 Timer Interrupt Status	TS2TINT	30h
Timer2 Interrupt Status	TS2INTS	34h
Timer2 Interrupt Flag	TS2XCHGINT	38h

Table 6-26. DMA Registers (Base Address: 0x4000_E000)

REGISTER NAME	ACRONYM	OFFSET
Device Configuration Status	DMA_DEVCFG_STAT	000h
Software Channel Trigger	DMA_SWCHTRIG	004h
Channel 0 Source Configuration	DMA_CH0_SRCCFG	008h
Channel 1 Source Configuration	DMA_CH1_SRCCFG	00Ch
Channel 2 Source Configuration	DMA_CH2_SRCCFG	010h
Channel 3 Source Configuration	DMA_CH3_SRCCFG	014h
Channel 4 Source Configuration	DMA_CH4_SRCCFG	018h
Channel 5 Source Configuration	DMA_CH5_SRCCFG	01Ch
Channel 6 Source Configuration	DMA_CH6_SRCCFG	020h
Channel 7 Source Configuration	DMA_CH7_SRCCFG	024h
Channel 8 Source Configuration	DMA_CH8_SRCCFG	028h
Channel 9 Source Configuration	DMA_CH9_SRCCFG	02Ch
Channel 10 Source Configuration	DMA_CH10_SRCCFG	030h
Channel 11 Source Configuration	DMA_CH11_SRCCFG	034h
Channel 12 Source Configuration	DMA_CH12_SRCCFG	038h
Channel 13 Source Configuration	DMA_CH13_SRCCFG	03Ch
Channel 14 Source Configuration	DMA_CH14_SRCCFG	040h
Channel 15 Source Configuration	DMA_CH15_SRCCFG	044h
Channel 16 Source Configuration	DMA_CH16_SRCCFG	048h
Channel 17 Source Configuration	DMA_CH17_SRCCFG	04Ch
Channel 18 Source Configuration	DMA_CH18_SRCCFG	050h
Channel 19 Source Configuration	DMA_CH19_SRCCFG	054h
Channel 20 Source Configuration	DMA_CH20_SRCCFG	058h
Channel 21 Source Configuration	DMA_CH21_SRCCFG	05Ch
Channel 22 Source Configuration	DMA_CH22_SRCCFG	060h
Channel 23 Source Configuration	DMA_CH23_SRCCFG	064h
Channel 24 Source Configuration	DMA_CH24_SRCCFG	068h
Channel 25 Source Configuration	DMA_CH25_SRCCFG	06Ch
Channel 26 Source Configuration	DMA_CH26_SRCCFG	070h
Channel 27 Source Configuration	DMA_CH27_SRCCFG	074h
Channel 28 Source Configuration	DMA_CH28_SRCCFG	078h
Channel 29 Source Configuration	DMA_CH29_SRCCFG	07Ch
Channel 30 Source Configuration	DMA_CH30_SRCCFG	080h
Channel 31 Source Configuration	DMA_CH31_SRCCFG	084h
Channel 32 Source Configuration	DMA_CH32_SRCCFG	088h
Channel 33 Source Configuration	DMA_CH33_SRCCFG	08Ch
Channel 34 Source Configuration	DMA_CH34_SRCCFG	090h
Channel 35 Source Configuration	DMA_CH35_SRCCFG	094h
Channel 36 Source Configuration	DMA_CH36_SRCCFG	098h
Channel 37 Source Configuration	DMA_CH37_SRCCFG	09Ch
Channel 38 Source Configuration	DMA_CH38_SRCCFG	0A0h
Channel 39 Source Configuration	DMA_CH39_SRCCFG	0A4h
Channel 40 Source Configuration	DMA_CH40_SRCCFG	0A8h
Channel 41 Source Configuration	DMA_CH41_SRCCFG	0ACh
Channel 42 Source Configuration	DMA_CH42_SRCCFG	0B0h
Channel 43 Source Configuration	DMA_CH43_SRCCFG	0B4h
Channel 44 Source Configuration	DMA_CH44_SRCCFG	0B8h
Channel 45 Source Configuration	DMA_CH45_SRCCFG	0BCh
Channel 46 Source Configuration	DMA_CH46_SRCCFG	0C0h
Channel 47 Source Configuration	DMA_CH47_SRCCFG	0C4h
Channel 48 Source Configuration	DMA_CH48_SRCCFG	0C8h
Channel 49 Source Configuration	DMA_CH49_SRCCFG	0CCh
Channel 50 Source Configuration	DMA_CH50_SRCCFG	0D0h
Channel 51 Source Configuration	DMA_CH51_SRCCFG	0D4h
Channel 52 Source Configuration	DMA_CH52_SRCCFG	0D8h
Channel 53 Source Configuration	DMA_CH53_SRCCFG	0DCh
Channel 54 Source Configuration	DMA_CH54_SRCCFG	0E0h
Channel 55 Source Configuration	DMA_CH55_SRCCFG	0E4h
Channel 56 Source Configuration	DMA_CH56_SRCCFG	0E8h
Channel 57 Source Configuration	DMA_CH57_SRCCFG	0ECh
Channel 58 Source Configuration	DMA_CH58_SRCCFG	0F0h
Channel 59 Source Configuration	DMA_CH59_SRCCFG	0F4h
Channel 60 Source Configuration	DMA_CH60_SRCCFG	0F8h
Channel 61 Source Configuration	DMA_CH61_SRCCFG	0FCh
Channel 62 Source Configuration	DMA_CH62_SRCCFG	100h
Channel 63 Source Configuration	DMA_CH63_SRCCFG	104h
Channel 64 Source Configuration	DMA_CH64_SRCCFG	108h
Channel 65 Source Configuration	DMA_CH65_SRCCFG	10Ch
Channel 66 Source Configuration	DMA_CH66_SRCCFG	110h
Channel 67 Source Configuration	DMA_CH67_SRCCFG	114h
Channel 68 Source Configuration	DMA_CH68_SRCCFG	118h
Channel 69 Source Configuration	DMA_CH69_SRCCFG	11Ch
Channel 70 Source Configuration	DMA_CH70_SRCCFG	120h
Channel 71 Source Configuration	DMA_CH71_SRCCFG	124h
Channel 72 Source Configuration	DMA_CH72_SRCCFG	128h
Channel 73 Source Configuration	DMA_CH73_SRCCFG	12Ch
Channel 74 Source Configuration	DMA_CH74_SRCCFG	130h
Channel 75 Source Configuration	DMA_CH75_SRCCFG	134h
Channel 76 Source Configuration	DMA_CH76_SRCCFG	138h
Channel 77 Source Configuration	DMA_CH77_SRCCFG	13Ch
Channel 78 Source Configuration	DMA_CH78_SRCCFG	140h
Channel 79 Source Configuration	DMA_CH79_SRCCFG	144h
Channel 80 Source Configuration	DMA_CH80_SRCCFG	148h
Channel 81 Source Configuration	DMA_CH81_SRCCFG	14Ch
Channel 82 Source Configuration	DMA_CH82_SRCCFG	150h
Channel 83 Source Configuration	DMA_CH83_SRCCFG	154h
Channel 84 Source Configuration	DMA_CH84_SRCCFG	158h
Channel 85 Source Configuration	DMA_CH85_SRCCFG	15Ch
Channel 86 Source Configuration	DMA_CH86_SRCCFG	160h
Channel 87 Source Configuration	DMA_CH87_SRCCFG	164h
Channel 88 Source Configuration	DMA_CH88_SRCCFG	168h
Channel 89 Source Configuration	DMA_CH89_SRCCFG	16Ch
Channel 90 Source Configuration	DMA_CH90_SRCCFG	170h
Channel 91 Source Configuration	DMA_CH91_SRCCFG	174h
Channel 92 Source Configuration	DMA_CH92_SRCCFG	178h
Channel 93 Source Configuration	DMA_CH93_SRCCFG	17Ch
Channel 94 Source Configuration	DMA_CH94_SRCCFG	180h
Channel 95 Source Configuration	DMA_CH95_SRCCFG	184h
Channel 96 Source Configuration	DMA_CH96_SRCCFG	188h
Channel 97 Source Configuration	DMA_CH97_SRCCFG	18Ch
Channel 98 Source Configuration	DMA_CH98_SRCCFG	190h
Channel 99 Source Configuration	DMA_CH99_SRCCFG	194h
Channel 100 Source Configuration	DMA_CH100_SRCCFG	198h
Channel 101 Source Configuration	DMA_CH101_SRCCFG	19Ch
Channel 102 Source Configuration	DMA_CH102_SRCCFG	1A0h
Channel 103 Source Configuration	DMA_CH103_SRCCFG	1A4h
Channel 104 Source Configuration	DMA_CH104_SRCCFG	1A8h
Channel 105 Source Configuration	DMA_CH105_SRCCFG	1AC

Table 6-27. PCM Registers (Base Address: 0x4001_0000)

REGISTER NAME	ACRONYM	OFFSET
Control 0	PCMCTL0	00h
Control 1	PCMCTL1	04h
Interrupt Enable	PCMCIE	08h
Interrupt Flag	PCMFIF	0Ch

Table 6-27. PCM Registers (Base Address: 0x4001_0000) (continued)

REGISTER NAME	ACRONYM	OFFSET
Clear Interrupt Flag	PCWOLRIFG	1Ch

Table 6-28. CS Registers (Base Address: 0x4001_0400)

REGISTER NAME	ACRONYM	OFFSET
Key	CSKEY	0Ch
Control 0	CSCTL0	04h
Control 1	CSCTL1	05h
Control 2	CSCTL2	0Ch
Control 3	CSCTL3	1Ch
Clock Prescaler	CSCLKEN	1Ch
Status	CSSTAT	34h
Interrupt Enable	CSE	4Ch
Interrupt Flag	CSIFG	4Ch
Clear Interrupt Flag	CSCLRIFG	5Ch
Self-Interrupt Flag	CSSEIFG	5Ch
DDC External Resistor Calibration 0	CSDCOEPRCAL0	6Ch
DDC External Resistor Calibration 1	CSDCOEPRCAL1	6Ch

Table 6-29. PSS Registers (Base Address: 0x4001_0800)

REGISTER NAME	ACRONYM	OFFSET
Key	PSSKEY	07h
Control 0	PSSCTL0	04h
Interrupt Enable	PSSIE	34h
Interrupt Flag	PSSIFG	34h
Clear Interrupt Flag	PSSCLRIFG	3Ch

Table 6-30. FLCTL Registers (Base Address: 0x4001_1000)

REGISTER NAME	ACRONYM	OFFSET
Power Mode	FLCTL_POWER_MODE	010h
Bank 0 Read Control	FLCTL_BANK0_READCTL	010h
Bank 1 Read Control	FLCTL_BANK1_READCTL	014h
Read Burst/Compare Control and Status	FLCTL_READBST_CTLSTAT	020h
Read Burst/Compare Start Address	FLCTL_READBST_STARTADDR	024h
Read Burst/Compare Length	FLCTL_READBST_LEN	028h
Read Burst/Compare End Address	FLCTL_READBST_ENDADDR	02Ch
Read Burst/Compare Use Counter	FLCTL_READBST_COUNTER	030h
Program Burst Control and Status	FLCTL_PROGBST_CTLSTAT	034h
Program Burst Start Address	FLCTL_PROGBST_STARTADDR	038h
Program Burst Data 0	FLCTL_PROGBST_DATA0_0	0C0h
Program Burst Data 1	FLCTL_PROGBST_DATA0_1	0C4h
Program Burst Data 2	FLCTL_PROGBST_DATA0_2	0C8h
Program Burst Data 3	FLCTL_PROGBST_DATA0_3	0CCh
Program Burst Data 0	FLCTL_PROGBST_DATA1_0	0D0h
Program Burst Data 1	FLCTL_PROGBST_DATA1_1	0D4h
Program Burst Data 2	FLCTL_PROGBST_DATA1_2	0D8h

Table 6-30. FLCTL Registers (Base Address: 0x4001_1000) (continued)

REGISTER NAME	ACRONYM	OFFSET
Program Burst Data0 3	FLCTL_PRGBURST_DATA0_3	07Ch
Program Burst Data0 0	FLCTL_PRGBURST_DATA0_0	07Dh
Program Burst Data0 1	FLCTL_PRGBURST_DATA0_1	07Eh
Program Burst Data0 2	FLCTL_PRGBURST_DATA0_2	07Fh
Program Burst Data0 3	FLCTL_PRGBURST_DATA0_3	080h
Program Burst Data0 0	FLCTL_PRGBURST_DATA0_0	081h
Program Burst Data0 1	FLCTL_PRGBURST_DATA0_1	082h
Program Burst Data0 2	FLCTL_PRGBURST_DATA0_2	083h
Program Burst Data0 3	FLCTL_PRGBURST_DATA0_3	084h
Erase Control and Status	FLCTL_ERASE_CTLSTAT	090h
Erase Sector Address	FLCTL_ERASE_SECTADDR	094h
Information Memory Bank 0 Write Enable Protection	FLCTL_BANK0_INFOWRPROT	0A0h
Main Memory Bank 0 Write Enable Protection	FLCTL_BANK0_MAINWRPROT	0A4h
Information Memory Bank 1 Write Enable Protection	FLCTL_BANK1_INFOWRPROT	0C0h
Main Memory Bank 1 Write Enable Protection	FLCTL_BANK1_MAINWRPROT	0C4h
Benchmark Control and Status	FLCTL_BNKR_CTLSTAT	0D0h
Benchmark Instruction Fetch Count	FLCTL_BNKR_FETCH	0D4h
Benchmark Data Read Count	FLCTL_BNKR_DREAD	0D8h
Benchmark Control Compare	FLCTL_BNKR_CMP	0DCh
Interrupt Flag	FLCTL_IFG	0E0h
Interrupt Enable	FLCTL_IE	0F4h
Clear Interrupt Flag	FLCTL_CLRIFG	0F8h
Set Interrupt Flag	FLCTL_SETIFG	0FCh
Real Time Control	FLCTL_RTAN_TMCNT	100h
Device Monitor Timing Control	FLCTL_DEVMONSTR_TMCNT	104h
Program Watch Timing Control	FLCTL_PROGWR_TMCNT	108h
Eraser Watch Timing Control	FLCTL_ERASWR_TMCNT	10Ch
Program Timing Control	FLCTL_PROGVAL_TMCNT	114h
Eraser Timing Control	FLCTL_ERASE_TMCNT	118h
Eraser Watch Timing Control	FLCTL_ERASEWR_TMCNT	11Ch
Burst Program Timing Control	FLCTL_BURSTPRO_TMCNT	120h

Table 6-31. ADC14 Registers (Base Address: 0x4001_2000)

REGISTER NAME	ACRONYM	OFFSET
Control 0	ADC14CTL0	02h
Control 1	ADC14CTL1	04h
Window Comparator Low Threshold 0	ADC14W0	08h
Window Comparator High Threshold 0	ADC14H0	0Ch
Window Comparator Low Threshold 1	ADC14W1	10h
Window Comparator High Threshold 1	ADC14H1	14h
Memory Control 0	ADC14MCTL0	18h
Memory Control 1	ADC14MCTL1	1Ch
Memory Control 2	ADC14MCTL2	20h
Memory Control 3	ADC14MCTL3	24h
Memory Control 4	ADC14MCTL4	28h
Memory Control 5	ADC14MCTL5	2Ch
Memory Control 6	ADC14MCTL6	30h

Table 6-31. ADC14 Registers (Base Address: 0x4001_2000) (continued)

REGISTER NAME	ACRONYM	OFFSET
Memory Control 7	ADC14/CTL7	34h
Memory Control 8	ADC14/CTL8	35h
Memory Control 9	ADC14/CTL9	36h
Memory Control 10	ADC14/CTL10	37h
Memory Control 11	ADC14/CTL11	38h
Memory Control 12	ADC14/CTL12	39h
Memory Control 13	ADC14/CTL13	3Ah
Memory Control 14	ADC14/CTL14	3Bh
Memory Control 15	ADC14/CTL15	3Ch
Memory Control 16	ADC14/CTL16	3Dh
Memory Control 17	ADC14/CTL17	3Eh
Memory Control 18	ADC14/CTL18	3Fh
Memory Control 19	ADC14/CTL19	40h
Memory Control 20	ADC14/CTL20	41h
Memory Control 21	ADC14/CTL21	42h
Memory Control 22	ADC14/CTL22	43h
Memory Control 23	ADC14/CTL23	44h
Memory Control 24	ADC14/CTL24	45h
Memory Control 25	ADC14/CTL25	46h
Memory Control 26	ADC14/CTL26	47h
Memory Control 27	ADC14/CTL27	48h
Memory Control 28	ADC14/CTL28	49h
Memory Control 29	ADC14/CTL29	4Ah
Memory Control 30	ADC14/CTL30	4Bh
Memory Control 31	ADC14/CTL31	4Ch
Memory 0	ADC14/EM0	60h
Memory 1	ADC14/EM1	61h
Memory 2	ADC14/EM2	62h
Memory 3	ADC14/EM3	63h
Memory 4	ADC14/EM4	64h
Memory 5	ADC14/EM5	65h
Memory 6	ADC14/EM6	66h
Memory 7	ADC14/EM7	67h
Memory 8	ADC14/EM8	68h
Memory 9	ADC14/EM9	69h
Memory 10	ADC14/EM10	6Ah
Memory 11	ADC14/EM11	6Bh
Memory 12	ADC14/EM12	6Ch
Memory 13	ADC14/EM13	6Dh
Memory 14	ADC14/EM14	6Eh
Memory 15	ADC14/EM15	6Fh
Memory 16	ADC14/EM16	70h
Memory 17	ADC14/EM17	71h
Memory 18	ADC14/EM18	72h
Memory 19	ADC14/EM19	73h
Memory 20	ADC14/EM20	74h
Memory 21	ADC14/EM21	75h

Table 6-31. ADC14 Registers (Base Address: 0x4001_2000) (continued)

REGISTER NAME	ACRONYM	OFFSET
Memory 22	ADC14MEM22	F0h
Memory 23	ADC14MEM23	F1h
Memory 24	ADC14MEM24	F2h
Memory 25	ADC14MEM25	F3h
Memory 26	ADC14MEM26	F4h
Memory 27	ADC14MEM27	F5h
Memory 28	ADC14MEM28	F6h
Memory 29	ADC14MEM29	F7h
Memory 30	ADC14MEM30	F8h
Memory 31	ADC14MEM31	F9h
Interrupt Block 0	ADC14EB0	13Ch
Interrupt Block 1	ADC14EB1	14Ch
Interrupt Flag 0	ADC14IFCR0	14Ah
Interrupt Flag 1	ADC14IFCR1	14Bh
Clear Interrupt Flag 0	ADC14CLRIFCR0	14Ch
Clear Interrupt Flag 1	ADC14CLRIFCR1	14Dh
Interrupt Vector	ADC14IV	14Eh

6.3.3.2 Peripheral Bit Band Alias Region

The 32MB region from 0x4200_0000 through 0x43FF_FFFF forms the bit-band alias region for the 1MB peripheral region. Bit banding is a feature of the Cortex M4 processor and allows the application to set or clear individual bits throughout the peripheral memory space without using the pipeline bandwidth of the processor to carry out an exclusive read-modify-write sequence.

NOTE

The restriction of accessing 16-bit peripherals only through byte or half-word accesses also applies to the corresponding bit-band region of these peripherals. In other words, writes to the bit-band alias region for these peripherals must be in the form of byte or half-word accesses only.

6.3.4 Debug and Trace Peripheral Zone

This zone maps the internal and external PPB regions of the Cortex-M4 (see [Table 6-32](#)). The following peripherals are mapped to this zone:

- Core and System debug control registers (internal PPB)
- NVIC and other registers in the System Control space of the Cortex-M4 (internal PPB)
- TPU, DWT, ITM (internal PPB)
- TPIU (Debug ROM table) (external PPB)
- Reset Controller (external PPB)
- System Controller (external PPB)

Table 6-32. Debug Zone Memory Map

ADDRESS RANGE	MODULE OR PERIPHERAL	REMARKS
0xE000_0000-0xE000_0FFF	ITM	Internal PPB
0xE000_1000-0xE000_1FFF	DWT	Internal PPB
0xE000_2000-0xE000_2FFF	TPU	Internal PPB
0xE000_3000-0xE000_3FFF	Reserved	Internal PPB
0xE000_4000-0xE000_4FFF	Cortex-M4 System Control Space	Internal PPB
0xE000_5000-0xE000_5FFF	Reserved	Internal PPB
0xE004_0000-0xE004_0FFF	TPIU	External PPB
0xE004_1000-0xE004_1FFF	Reserved	External PPB
0xE004_2000-0xE004_2FFF	Reset Controller (see Table 6-93)	External PPB
0xE004_3000-0xE004_3FFF	Reserved	External PPB
0xE004_4000-0xE004_4FFF	System Controller (see Table 6-94)	External PPB
0xE004_5000-0xE004_5FFF	Reserved	External PPB
0xE004_6000-0xE004_6FFF	System Controller	External PPB
0xE004_7000-0xE004_7FFF	Reserved	External PPB
0xE004_8000-0xE004_8FFF	Reserved	External PPB
0xE004_9000-0xE004_9FFF	ROM Table (External PPB)	External PPB
0xE004_A000-0xE004_AFFF	Reserved	External PPB

NOTE

For the address maps of the ARM modules listed in [Table 6-32](#), see the Cortex-M4 technical reference manual at www.arm.com.

Table 6-93. RSTCTL Registers

REGISTER NAME	ACRONYM	OFFSET
Reset Request	RSTCTL_RESET_REQ	000h
Hard Reset Status	RSTCTL_HARDRESET_STAT	004h
Hard Reset Status Clear	RSTCTL_HARDRESET_CLR	008h
Hard Reset Status Set	RSTCTL_HARDRESET_SET	00Ch
Soft Reset Status	RSTCTL_SOFTRESET_STAT	010h
Soft Reset Status Clear	RSTCTL_SOFTRESET_CLR	014h
Soft Reset Status Set	RSTCTL_SOFTRESET_SET	018h
PSR Reset Status	RSTCTL_PSRRESET_STAT	0C0h
PSR Reset Status Clear	RSTCTL_PSRRESET_CLR	0C4h
PCN Reset Status	RSTCTL_PCNRESET_STAT	0C8h
PCN Reset Status Clear	RSTCTL_PCNRESET_CLR	0CCh
Pin Reset Status	RSTCTL_PINRESET_STAT	0D0h

Table 6-33. RSTCTL Registers (continued)

REGISTER NAME	ACRONYM	OFFSET
Pin Reset Status Clear	RSTCTL_PINRESET_CLR	114h
Internal Reset Status	RSTCTL_INTERNAL_RESET_STAT	116h
Internal Reset Status Clear	RSTCTL_INTERNAL_RESET_CLR	118h
CPU Reset Status	RSTCTL_CPU_RESET_STAT	120h
CPU Reset Status Clear	RSTCTL_CPU_RESET_CLR	122h

Table 6-34. SYSCTL Registers

REGISTER NAME	ACRONYM	OFFSET
Reset Control	SYS_RESET_CTL	0000h
NMI Control and Status	SYS_NMI_CTLSTA	0004h
Watchdog Reset Control	SYS_WDTRESET_CTL	0008h
Peripheral Lock Control	SYS_PERIPH_LOCK	000Ch
SRAM Size	SYS_SRAM_SIZE	0010h
SRAM Bank Enable	SYS_SRAM_BANKEN	0014h
SRAM Bank Individual Control	SYS_SRAM_BANKSEL	0018h
Flash Size	SYS_FLASH_SIZE	0020h
Debug/ICE Control and Status	SYS_DBG_ICESTAT	0024h
ITF Protected Secure Zone User Access Unlock	SYS_SECURITY_UNLOCK	0040h
Master Unlock	SYS_MASTER_UNLOCK	0044h
Power Downmode Request 0	SYS_POWERDOWNREQ0	0048h
Power Downmode Request 1	SYS_POWERDOWNREQ1	004Ch
Power Downmode Acknowledge	SYS_POWERDOWNACK	0050h
Reset Request	SYS_RESET_REQ	0054h
Reset Status and Overwrite	SYS_RESET_STATOVR	0058h
System Status	SYS_SYSTEM_STAT	005Ch

6.4 Memories on the MSP432P401x

The MSP432P401x MCUs include flash memory and SRAM for general application purposes. In addition, the devices include a backup memory (a portion of total available SRAM) that is retained in low-power modes.

6.4.1 Flash Memory

The MSP432P401x MCUs include a high-endurance, low-power flash memory that supports up to a minimum of 20000 write or erase cycles. The flash memory is 128 bits wide, thereby enabling high code execution performance by virtue of each fetch returning up to four 32-bit instructions (or up to eight 16-bit instructions). The flash is further divided into two types of subregions: main memory and information memory.

From a physical perspective, the flash memory comprises two banks, with the main and information memory regions divided equally between the two banks. This permits an application to carry out a simultaneous read or execute operation from one bank while the other bank may be undergoing a program or erase operation.

Figure 8-3 shows the memory map of the flash on MSP432P401x MCUs.

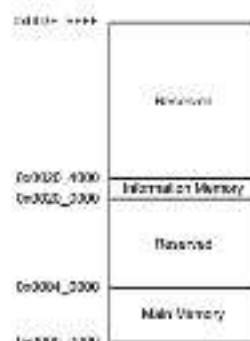


Figure 6-5. Flash Memory Map

6.4.1.1 Flash Main Memory (0x0000_0000 to 0x0003_FFFF)

The flash main memory on MSP432P401x MCUs can be up to 256KB. Flash main memory consists of up to 64 sectors of 4KB each, with a minimum erase granularity of 4KB (1 sector). The main memory can be viewed as two independent identical banks of up to 128KB each, allowing simultaneous read or execute from one bank while the other bank is undergoing a program or erase operation.

6.4.1.2 Flash Information Memory (0x0020_0000 to 0x0020_3FFF)

The flash information memory region is 16KB. Flash information memory consists of four sectors of 4KB each, with a minimum erase granularity of 4KB (1 sector). [Table 6-35](#) details the different regions of flash information memory and the contents of each of the regions. The flash information memory region that contains the device descriptor (TLV) is factory configured for protection against write and erase operations.

Table 6-35. Flash Information Memory Regions

REGION	ADDRESS RANGE	CONTENTS	WRITE AND ERASE PROTECTED?
Bank 0, Sector 0	0x0020_0000-0x0020_0FFF	Flash descriptor table (FDT)	No
Bank 0, Sector 1	0x0020_1000-0x0020_1FFF	Device Descriptor (TLV)	Yes
Bank 1, Sector 0	0x0020_2000-0x0020_2FFF	TLV	No
Bank 1, Sector 1	0x0020_3000-0x0020_3FFF	TLV	No

6.4.1.3 Flash Operation

The flash memory provides multiple read and program modes of operation that the application can deploy. Up to 128 bits (memory word width) can be programmed (set from 1 to 0) in a single program operation. Although the CPU data buses are 32 bits wide, the flash can buffer 128-bit write data before initiating flash programming, thereby making it more seamless and power efficient for software to program large blocks of data at a time. In addition, the flash memory also supports a burst write mode that takes less time when compared to programming words individually. See [Table 6-44](#) for information on timing parameters.

The flash main and information memory regions offer write/erase protection control at a sector granularity to enable software to optimize operations like mass erase while protecting certain regions of the flash. In low power modes of operation, the flash memory is disabled and put in a power down state to minimize leakage.

For details on the flash memory and its various modes of operation and configuration, see the *Flash Controller (FLCTL)* chapter in the *MSP432P4xx Family Technical Reference Manual*.

NOTE

Depending on the CPU (MCU) frequency and the active mode in use, the flash may need to be accessed with single/multiple wait states. Whenever there is a change required in the operating frequency, it is the responsibility of the application to ensure that the flash access wait states are configured correctly before the frequency change is effected. See the electrical specification for details on flash wait state requirements.

6.4.2 SRAM

The MSP432P401x MCUs support up to 64KB of SRAM, with the rest of the 1MB SRAM region reserved. The SRAM is aliased in both Code and SRAM zones. This enables fast single-cycle execution of code from the SRAM, as the Cortex-M4 processor pipelines instruction fetches to memory zones other than the Code space. As with the flash memory, the SRAM can be powered down or placed in a low-leakage retention state in low-power modes of operation.

Figure 6-6 shows the memory map of SRAM on MSP432P401x MCUs.

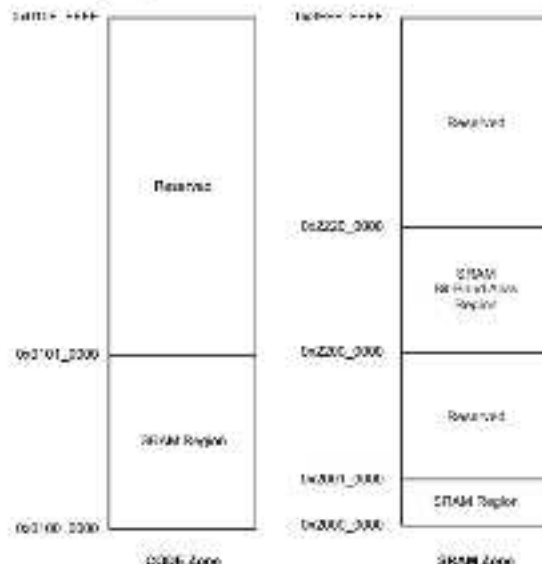


Figure 6-6. SRAM Map

6.4.2.1 SRAM Bank Enable Configuration

The application can optimize the power consumption of the SRAM. To enable this, the SRAM is divided into 8-KB banks that can be individually powered down. Banks that are powered down remain powered down in both active and low-power modes of operation, thereby limiting any unnecessary inrush current when the device transitions between active and retention-based low-power modes. The application can also disable one (or more) banks for a certain stage in the processing and enable it for another stage.

When a particular bank is disabled, reads to its address space return 0h, and writes are discarded. To prevent holes in the memory map, if a particular bank is enabled, all the lower banks are also forced to enabled state. This ensures a contiguous memory map through the set of enabled banks instead of a showing a disabled bank to appear between enabled banks. For example,

- If there are eight banks in the device, values of 00111111 and 00000111 are acceptable.
- Values like 00010111 are not valid, and the resultant bank configuration is automatically set to 00011111.
- For example, for a 4-bank SRAM, the only allowed values are 0001, 0011, 0111, and 1111.

Bank 0 of SRAM is always enabled and cannot be disabled. For all other banks, any enable or disable change results in the SRAM RDY bit of the SYS SRAM BANKEN register being set to 0 until the configuration change is effective. Any accesses to the SRAM is stalled during this time, and access resumes only after the SRAM banks are ready for read or write operations. This is handled transparently and does not require any code intervention. See the SRAM characteristics in the electrical specification for the SRAM bank enable or disable latency.

6.4.2.2 SRAM Bank Retention Configuration and Backup Memory

The application can optimize the leakage power consumption of the SRAM in LPM3 and LPM4 modes of operation. To enable this, each SRAM bank can be individually configured for retention. Banks that are enabled for retention retain their data through the LPM3 and LPM4 modes. The application can also retain a subset of the enabled banks.

For example, the application may need 32KB of SRAM for its processing needs (four banks are kept enabled). However, of these four banks, only one bank may contain critical data that must be retained in LPM3 or LPM4, while the rest are powered off completely to minimize power consumption.

Bank 0 of SRAM is always retained and cannot be powered down. Therefore, it also operates up as a possible backup memory in the LPM3, LPM4, and LPM3.5 modes of operation. In the case of LPM3 and LPM4 modes the full 8KB of SRAM bank 0 is retained but in the case of LPM3.5 mode only 8KB of SRAM bank 0 is retained. The 2KB of SRAM bank 0 over the address range 0x2000_0000 to 0x2000_00FF is not retained in LPM3.5 mode.

6.4.3 ROM

The MSP432P401x MCUs support 32KB of ROM, with the rest of the 1MB region reserved (for future upgrades). The lower 2KB of the ROM is reserved for TI internal purposes and accesses to this space returns an error response. The rest of the ROM is used for driver libraries.

NOTE

The entire ROM region returns an error response for write accesses. The lower 2KB of the ROM always returns an error response for any access.

6.5 DMA

The MSP432P401x MCUs implement an 8-channel ARM uDMA. This allows eight simultaneously active channels for data transfer between memory and peripherals without needing to use the bandwidth of the CPU (thereby reducing power by idling the CPU when there is no data processing required). In addition, the DMA remains active in multiple low-power modes of operation, allowing for a very low power state in which data can be transferred at low rates.

For maximum flexibility, up to eight DMA event sources can map to any of the eight channels. This is controlled through configuration registers in the DMA. In addition, the DMA can generate up to four interrupt requests (described in Section 6.6.2). For details regarding configuration of the DMA, see the DMA chapter in the *MSP432P401x Family Technical Reference Manual*.

6.5.1 DMA Source Mapping

Each channel of the eight available channels has a control register that can select any of the device-level DMA sources as the first source for that corresponding channel. Table 6-38 lists the sources available for mapping to each channel, based on the value of the Source Configuration (SRCCFG) register. The DMA transfers are initiated upon rising edge of the selected DMA source.

Table 6-38. DMA Sources

	M032P401R	M032P401M	M032P401R	M032P401M	M032P401R	M032P401M	M032P401R	M032P401M
Channel 0	Reserved	4US0_00 TX	4US0_00 TX	4US0_00 TX	4US0_00 TX	4US0_00 TX	4US0_00 TX	4US0_00 TX
Channel 1	Reserved	4US0_00 RX	4US0_00 RX	4US0_00 RX	4US0_00 RX	4US0_00 RX	4US0_00 RX	4US0_00 RX
Channel 2	Reserved	4US0_01 TX	4US0_01 TX	4US0_01 TX	4US0_01 TX	4US0_01 TX	4US0_01 TX	4US0_01 TX
Channel 3	Reserved	4US0_01 RX	4US0_01 RX	4US0_01 RX	4US0_01 RX	4US0_01 RX	4US0_01 RX	4US0_01 RX
Channel 4	Reserved	4US0_02 TX	4US0_02 TX	4US0_02 TX	4US0_02 TX	4US0_02 TX	4US0_02 TX	4US0_02 TX
Channel 5	Reserved	4US0_02 RX	4US0_02 RX	4US0_02 RX	4US0_02 RX	4US0_02 RX	4US0_02 RX	4US0_02 RX
Channel 6	Reserved	4US0_03 TX	4US0_03 TX	4US0_03 TX	4US0_03 TX	4US0_03 TX	4US0_03 TX	4US0_03 TX
Channel 7	Reserved	4US0_03 RX	4US0_03 RX	4US0_03 RX	4US0_03 RX	4US0_03 RX	4US0_03 RX	4US0_03 RX

NOTE

Any source marked as Reserved is unused. It may be used for software-controlled DMA transfer, but typically it is reserved for enhancement purposes on future devices.

6.5.2 DMA Completion Interrupts

In the case of the ARM μ DMA controller, it is usually the responsibility of software to maintain a list of channels that have completed their operation. To provide further flexibility, the MSP432P401x DMA supports four DMA completion interrupts, which are mapped in the following way:

- DMA_INT0: Logical OR of all completion events except those that are already mapped to DMA_INT1, DMA_INT2, or DMA_INT3.
- DMA_INT1, DMA_INT2, DMA_INT3: Can be mapped to the DMA completion event of any of the eight channels.

NOTE

Software must make sure that DMA_INT1, DMA_INT2, and DMA_INT3 are mapped to different channels, so that the same channel does not result in multiple interrupts at the NVIC.

6.5.3 DMA Access Privileges

The DMA has access to all of the memories and peripheral configuration interfaces of the device. If the device is configured for IP protection, DMA access to the flash is restricted to only the lower half (second bank) of the flash main and information memory regions. This prevents the DMA from being used as an unauthorized access source into the top half (first bank) of the flash, where secure data regions are housed.

6.6 Memory Map Access Details

The bus system on the MSP432P401x MCUs incorporates four masters, which can initiate various types of transactions:

- ICODE: Cortex-M4 instruction fetch bus. Accesses the Code zone only.
- DICODE: Cortex-M4 data and literal load/store bus. Accesses the Code zone only. Debugger accesses to Code zone also appear on this bus.

- **SBUS:** Cortex-M4 data read and write bus. Accesses to all zones except Code zones and PDB memory space only. Debugger accesses to this space also appear on this bus.
- **DMA:** Access to all zones except the PDB memory space.

NOTE

The MPU space is dedicated only to the Cortex-M4 Private Peripheral Bus.

8.6.1 Master and Slave Access Priority Settings

Table 8-37 lists all of the available masters (rows) and their access permissions to slaves (columns). If multiple masters can access one slave, the table lists access priorities if arbitration is required. A lower number in the table indicates a higher prioritization (note the priority is always fixed).

Table G-37. Master and Slave Access Priority

	FLASH MEMORY	ROM	SRAM	PERIPHERALS
MCU	5	4	4	NA
DCDC	21 ¹	1	1	NA
SD-S	NA	NA	1	2
DMA	11 ²	NA	11 ³	1

- (1) Access from the ECC/CE1 to Bank 0 memory may be needed if the device is operating in a secure mode.
- (2) Access from L2A to Bank 0 memory are needed to Bank 1 if the device is operating in a secure mode with L1 protection enabled. In such cases, access to Bank 0 returns an error response.
- (3) Although the SRAM is mapped to both Code and System spaces, accesses from DMA to SRAM must use only the System space. L2A and access to SRAMs in Code space will result in an error.

6.6.2 Memory Map Access Response

Table 6-39 summarizes the access responses to the entire memory map of the MSP432P401x MCUs.

Table 6-38. Member Map Accession Requirements

ADDRESS RANGE	DESCRIPTION	READ (R)	WRITE (W)	INSTRUCTION FETCH (IF)
0x0000_0000-0x0003_FFFF	Flash Memory Memory	OK	OK (1)	OK
0x0004_0000-0x000F_FFFF	Reserved	Error	Error	Error
0x0010_0000-0x001F_FFFF	Flash Memory Memory	OK	OK (2)	OK
0x0020_0000-0x00FF_FFFF	Reserved	Error	Error	Error
0x0100_0000-0x01FF_FFFF	SRAM	OK	OK	OK
0x0101_0000-0x01FF_FFFF	Reserved	Error	Error	Error
0x0200_0000-0x02FF_FFFF	ROM (Reserved)	Error	Error	Error
0x0201_0000-0x02FF_FFFF	ROM	OK	Error	OK
0x0202_8000-0xFFFF_FFFF	Reserved	Error	Error	Error
0x0300_0000-0x03FF_FFFF	SRAM	OK	OK	OK
0x0301_0000-0x03FF_FFFF	Reserved	Error	Error	Error
0x0302_0000-0x03FF_FFFF	SRAM bit band alias	OK (3)	OK	Error
0x0400_0000-0x04FF_FFFF	Reserved	Error	Error	Error
0x0401_0000-0x04FF_FFFF	Reserved	Error	Error	Error
0x0402_0000-0x04FF_FFFF	Reserved	Error	Error	Error

- (12) A reserved memory region returns 0 on reads and instruction fetches. Writes to this region are ignored.

Table 6-39. NVIC Interrupts (continued)

NVIC INTERRUPT INPUT	SOURCE	FLAGS IN SOURCE
INTSR[0]	WDT_A	
INTSR[1]	INTEN[0]	Combined interrupt from flags in the INTEN[0] part of CoreDev1[0]
INTSR[2]	ECCTL	Flash Controller interrupt flags
INTSR[3]	COMP_0	Comparator 0 interrupt flag
INTSR[4]	COMP_1	Comparator 1 interrupt flag
INTSR[5]	Timer_00	TACCTL0COFIFG
INTSR[6]	Timer_01	TACCTL0COFIFG (x = 1 through 4), TACCTL1TIFG
INTSR[10]	Timer_07	TACCTL0COFIFG
INTSR[11]	Timer_01	TACCTL0COFIFG (x = 1 through 4), TACCTL1TIFG
INTSR[12]	Timer_02	TACCTL0COFIFG
INTSR[13]	Timer_02	TACCTL0COFIFG (x = 1 through 4), TACCTL1TIFG
INTSR[14]	Timer_03	TACCTL0COFIFG
INTSR[15]	Timer_03	TACCTL0COFIFG (x = 1 through 4), TACCTL1TIFG
INTSR[16]	USART_A0	UART or SPI mode TX, RX, and Status flags
INTSR[17]	USART_A1	UART or SPI mode TX, RX, and Status flags
INTSR[18]	USART_A2	UART or SPI mode TX, RX, and Status flags
INTSR[19]	USART_A3	UART or SPI mode TX, RX, and Status flags
INTSR[20]	USART_B0	SP or PC mode TX, RX, and Status flags (PC in multiple slave mode)
INTSR[21]	USART_0	SP or PC mode TX, RX, and Status flags (PC in multiple slave mode)
INTSR[22]	USART_02	SP or PC mode TX, RX, and Status flags (PC in multiple slave mode)
INTSR[23]	USART_B9	SP or PC mode TX, RX, and Status flags (PC in multiple slave mode)
INTSR[24]	ADC17	ADC17[0], ADC17[1], ADC17[2], ADC17[3], ADC17[4], ADC17[5], ADC17[6], ADC17[7]
INTSR[25]	Timer32_T0T1	Timer32 interrupt for timer 0
INTSR[26]	Timer32_T0T2	Timer32 interrupt for timer 2
INTSR[27]	Timer32_T0T3	Timer32 Combined interrupt
INTSR[28]	AE8256	AE8256VIFG
INTSR[29]	RTC_0	DRIFG, RHYFIFG, TTIMEF, ALFIFG, RSTRTFIFG, RSTRTIFG
INTSR[30]	DMA_B0R0	DMA error interrupt
INTSR[31]	DMA_INT0	DMA completion interrupt
INTSR[32]	DMA_IN_0	DMA completion interrupt
INTSR[33]	DMA_INT1	DMA completion interrupt
INTSR[34]	DMA_IN_0[2]	DMA completion interrupt
INTSR[35]	IO Port P0	PIF0[x] (x = 0 through 7)
INTSR[36]	IO Port P0	PIF0[x] (x = 0 through 7)
INTSR[37]	IO Port P1	PIF1[x] (x = 0 through 7)
INTSR[38]	IO Port P0	PIF0[x] (x = 0 through 7)
INTSR[39]	IO Port P0	PIF0[x] (x = 0 through 7)
INTSR[40]	IO Port P0	PIF0[x] (x = 0 through 7)
INTSR[41]	Reserved	
INTSR[42]	Reserved	
INTSR[43]	Reserved	
INTSR[44]	Reserved	
INTSR[45]	Reserved	
INTSR[46]	Reserved	
INTSR[47]	Reserved	

(2) The CPU of the Cortex-M3 can generate interrupts due to multiple floating point exceptions. It is the responsibility of software to process and clear the interrupt flags in the FPU registers.

(3) DMA_INT0 has a different functionality from DMA_INT1, DMA_INT2, or DMA_INT3. See Section 6.3.2 for more details.

Table 6-39. NVIC Interrupts (continued)

NVIC INTERRUPT INPUT	SOURCE	FLAGS IN SOURCE
INT_SRQ48	Reserved	
INT_SRQ49	Reserved	
INT_SRQ50	Reserved	
INT_SRQ51	Reserved	
INT_SRQ52	Reserved	
INT_SRQ53	Reserved	
INT_SRQ54	Reserved	
INT_SRQ55	Reserved	
INT_SRQ56	Reserved	
INT_SRQ57	Reserved	
INT_SRQ58	Reserved	
INT_SRQ59	Reserved	
INT_SRQ60	Reserved	
INT_SRQ61	Reserved	
INT_SRQ62	Reserved	
INT_SRQ63	Reserved	

NOTE

The Interrupt Service Routine (ISR) must ensure that the pending interrupt flag in the source peripheral is cleared before returning from the ISR. If this is not done, the same interrupt may be incorrectly triggered again as a new event, even though the event has already been processed by the ISR. As there may be a few cycles of delay between the execution of the write command and the act of write reflecting in the interrupt flag register of the peripheral, the recommendation is to carry out the write and wait for a few cycles before exiting the ISR. Alternatively, the application can do an explicit read to ensure that the flag is cleared before exiting the ISR.

6.8 System Control

System Control comprises the modules that govern the overall behavior of the device, including power management, operating modes, clocks, reset handling, and user configuration settings.

6.8.1 Device Resets

The MSP432P401x MCUs support multiple classes of reset. Each class results in a different level of initiation of device logic, thus allowing the application developer to initiate different resets based reset requirements during code development and debug. The following subsections cover the classes of reset in the device.

6.8.1.1 Power On/Off Reset (POR)

The POR initiates a complete initialization of the application settings and device configuration information. This class of reset may be initiated either by the FSS, the PDM, the RSTn pin, the Clock System upon DCO external resistor short circuit fault, or the device emulator logic (through the debugger). From an application perspective, all sources of POR return the device to the same state of initialization.

NOTE

Depending on the source of the reset, the device may exhibit different wake-up latencies from the POR. This implementation enables optimization of the reset recovery time.

6.8.1.4 Soft Reset

The Soft Reset resets only the execution component of the system, which is the nondebug logic in the Cortex-M4 and the WDT-A. This reset remains noninvasive to all other peripherals and system components. The MSP432P401x MCUs support up to 16 sources of Soft Reset. Table 6-41 lists the reset source allocation. The Reset Controller registers can be used to identify the source of reset in the design. For further details, see the Reset Controller chapter in the *MSP432P4xx Family Technical Reference Manual*.

Table 6-41. MSP432P401x Soft Reset Sources

RESET SOURCE NUMBER	SOURCE
0	CPU LOCKUP Condition (LOCKUP output of Cortex-M4)
1	WDT-A Timeout [1]
2	WDT-A Nonword Violation [2]
3	Reserved [3]
4	Reserved [3]
5	Reserved [3]
6	Reserved [3]
7	Reserved [3]
8	Reserved [3]
9	Reserved [3]
10	Reserved [3]
11	Reserved [3]
12	Reserved [3]
13	Reserved [3]
14	Reserved [3]
15	Reserved [3]

[1] The WDT-A timeout resets can be masked when an L1 Errata Reset or a Soft Reset. Reserved indicates that the source of Soft Reset is currently unused and left for future expansion.

NOTE

To support and enhance debug of reset conditions, the Reset Controller is located on the PPB of the device. This allows the Reset Controller to remain accessible even if the device is stuck in a Hard or Soft reset state. The Reset Controller permits overrides for Hard and Soft resets, thereby allowing an application to regain control of the device and isolate the cause of the stuck reset.

6.8.2 Power Supply System (PSS)

The PSS controls all the power supply related functionality of the device. It consists of the following components:

6.8.2.1 VCCDET

The VCCDET monitors the input voltage applied at the DVCC and AVCC pins of the device. When the V_{IN} is found to be below the operating range of the VCCDET trip points, it generates a brownout condition, thereby initiating a device reset (POR class reset).

6.8.2.2 Supply Supervisor and Monitor for High Side (SVSMH)

The SVSMH supervises and monitors the V_{DD} . SVSMH has a programmable threshold setting and can be used by the application to generate a reset or an interrupt if the V_{DD} dips below the desired threshold. In supervisor mode, the SVSMH generates a device reset (POR/blank reset). In monitor mode, the SVSMH generates an interrupt. The SVSMH can also be disabled if monitoring and supervision of the supply voltage are not required (offers further power savings).

6.8.2.3 Core Voltage Regulator

The MSP432P401x MCUs can be programmed to operate either with an LDO or with a DC-DC as the voltage regulator for the digital logic in the core domain of the device. The DC-DC offers significant boost in power efficiency for high-current, high-performance applications. The LDO is a highly efficient regulator that offers power advantages at lower V_{DD} ranges and in the ultra-low-power modes of operation.

The core operating voltage (output of the LDO or DC-DC) is automatically set by the device depending on the selected operating mode of the device (see Table 6-42 for further details). The device offers seamless switching between LDO and DC-DC operating modes and also implements a seamless DC-DC fail-safe mechanism.

6.8.3 Power Control Manager (PCM)

The PCM controls the operating modes of the device and the switching between the modes. This is controlled by the application, which can choose modes to meet its power and performance requirements. Table 6-42 lists the operating modes of the device.

Table 6-42. MSP432P401x Operating Modes

OPERATING MODE	DESCRIPTION
AM_LDO_VCORE0	LDO-based active mode, normal performance, core voltage level 0
LPMS_LDO_VCORE0	Same as above, except that CPU is OFF (no code execution)
AM_LDO_VCORE1	LDO-based active mode, maximum performance, core voltage level 1
LPMS_LDO_VCORE1	Same as above, except that CPU is OFF (no code execution)
AM_DCDC_VCORE0	DC-DC-based active mode, normal performance, core voltage level 0
LPMS_DCDC_VCORE0	Same as above, except that CPU is OFF (no code execution)
AM_DCDC_VCORE1	DC-DC-based active mode, maximum performance, core voltage level 1
LPMS_DCDC_VCORE1	Same as above, except that CPU is OFF (no code execution)
AM_LF_VCORE0	LDO-based low-frequency active mode, core voltage level 0
LPMS_LF_VCORE0	Same as above, except that CPU is OFF (no code execution)
AM_LF_VCORE1	LDO-based low-frequency active mode, core voltage level 1
LPMS_LF_VCORE1	Same as above, except that CPU is OFF (no code execution)
LPMS_VCORE0	LDO-based low-power mode with full static retention, core voltage level 0. RTC and WDT can be active.
LPMS_VCORE1	LDO-based low-power mode with full static retention, core voltage level 1. RTC and WDT can be active.
LPMS_VCORE0	LDO-based deep-power mode with full static retention, core voltage level 0, all peripherals disabled.
LPMS_VCORE1	LDO-based deep-power mode with full static retention, core voltage level 1, all peripherals disabled.
LPMS0	DC-DC-based deep-power mode, core voltage level 0, no retention or peripheral registers, WDT and WOT can be active.
LPMS1	Core voltage turned off, wake up only through pin reset or wake up capable I/Os.

6.8.4 Clock System (CS)

The CS contains the sources of the various clocks in the device. It also controls the mapping between the sources and the different clocks in the device.

6.8.4.1 LFXT

The LFXT supports 32.768 kHz low-frequency crystals.

6.8.4.2 HFXT

The HFXT supports high-frequency crystals up to 48 MHz.

6.8.4.3 DCO

The DCO is a power-efficient, tunable internal oscillator that generates up to 48 MHz. The DCO also supports a high-precision mode when using an external precision resistor.

6.8.4.4 Very Low-Power Low-Frequency Oscillator (VLO)

The VLO is an ultra-low-power internal oscillator that generates a low-accuracy clock at typical frequency of 8.1 kHz.

6.8.4.5 Low-Frequency Reference Oscillator (REFO)

The REFO can be used as an alternate, low-power, lower-accuracy source of a 32.768 kHz clock instead of the LFXT. The REFO can also be programmed to generate a 128 kHz clock.

6.8.4.6 Module Oscillator (MODOSC)

The MODOSC is an internal clock source that has a very low latency wake-up time. It is factory-calibrated to a frequency of 25 MHz. The MODOSC is typically used to supply a 'clock on request' to different modules. It can be used as a clock source for ADC operation at 1 Msps sampling rate.

6.8.4.7 System Oscillator (SYSOSC)

The SYSOSC is an internal clock source that is factory calibrated to a frequency of 5 MHz. It can be used as a clock source for ADC operation at 200 kps sampling rate. In addition, the SYSOSC is also used for timing of various system-level control and management operations.

6.8.4.8 Fail-Safe Mechanisms

All clock sources that operate with external components have a built-in fail-safe mechanism that automatically switches to the relevant backup source, thereby ensuring that spurious or unstable clocks never impact the device operation. Table 6-43 shows the different types of clock source faults and the corresponding fail-safe clocks.

Table 6-43. Fail-Safe Clocks

Fault Type	Fail-Safe Clock
LFXT oscillator fault	REFO clock
HFXT oscillator fault	SYSOSC clock
DCO external resistor open/short fault	DCO clock in internal mode

6.9.2 Port Mapping Controller (PMAPCTL)

The port mapping controller allows flexible and reconfigurable mapping of digital functions.

6.9.2.1 Port Mapping Definitions

The port mapping controller on MSP432P401x MCUs allows reconfigurable mapping of digital functions on ports P2, P3, and P7. Table 6-44 lists the available mappings. Table 6-45 lists the default settings for all pins that support port mapping.

Table 6-44. Port Mapping Mnemonics and Functions

VALUE	PMAP MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
0	PM_NMI	NMI	NMI
1	PM_UC0CLK	UC0CLK clock input/output (direction controlled by UC0C1)	
2	PM_UC0RXD	UC0C1_A0 UART RXD (direction controlled by UC0C1 – Input)	
	PM_UC0SD0B	UC0C1_A0 SPI slave bit master in (direction controlled by UC0C1)	
3	PM_UC0TXD	UC0C1_A0 UART TXD (direction controlled by UC0C1 – Output)	
	PM_UC0SD0A	UC0C1_A0 SPI slave bit master out (direction controlled by UC0C1)	
4	PM_UC0CLK	UC0C1_B0 clock input/output (direction controlled by UC0C1)	
5	PM_UC0P0A	UC0C1_B0 P0 mode (open drain and direction controlled by UC0C1)	
	PM_UC0SD0B	UC0C1_B0 SPI slave bit master in (direction controlled by UC0C1)	
6	PM_UC0P0A	UC0C1_B0 P0 mode (open drain and direction controlled by UC0C1)	
	PM_UC0SD0A	UC0C1_B0 SPI slave bit master out (direction controlled by UC0C1)	
7	PM_UC0STE	UC0C1_A1 SPI slave transmit enable (direction controlled by UC0C1)	
8	PM_UC0CLK	UC0C1_A1 clock input/output (direction controlled by UC0C1)	
9	PM_UC0TXD	UC0C1_A1 UART RXD (direction controlled by UC0C1 – Input)	
	PM_UC0SD0B	UC0C1_A1 SPI slave bit master in (direction controlled by UC0C1)	
10	PM_UC0TXD	UC0C1_A1 UART TXD (direction controlled by UC0C1 – Output)	
	PM_UC0SD0A	UC0C1_A1 SPI slave bit master out (direction controlled by UC0C1)	
11	PM_UC0STE	UC0C1_A1 SPI slave transmit enable (direction controlled by UC0C1)	
12	PM_UC0CLK	UC0C1_A2 clock input/output (direction controlled by UC0C1)	
	PM_UC0RXD	UC0C1_A2 UART RXD (direction controlled by UC0C1 – Input)	
	PM_UC0SD0B	UC0C1_A2 SPI slave bit master in (direction controlled by UC0C1)	
14	PM_UC0TXD	UC0C1_A2 UART TXD (direction controlled by UC0C1 – Output)	
	PM_UC0SD0A	UC0C1_A2 SPI slave bit master out (direction controlled by UC0C1)	
15	PM_UC0SD0B	UC0C1_B2 SPI slave bit master in (direction controlled by UC0C1)	
16	PM_UC0CLK	UC0C1_B2 clock input/output (direction controlled by UC0C1)	
17	PM_UC0P0A	UC0C1_B2 P0 mode (open drain and direction controlled by UC0C1)	
	PM_UC0SD0A	UC0C1_B2 SPI slave bit master out (direction controlled by UC0C1)	
18	PM_UC0SD0B	UC0C1_B2 P0 mode (open drain and direction controlled by UC0C1)	
19	PM_UC0SD0A	UC0C1_B2 SPI slave bit master in (direction controlled by UC0C1)	
20	PM_TA0_0	TA0_CCR0 capture input CCR0A	TA0_CCR0 compare output Out0
21	PM_TA0_1	TA0_CCR1 capture input CCR1A	TA0_CCR1 compare output Out1
22	PM_TA0_2	TA0_CCR2 capture input CCR2A	TA0_CCR2 compare output Out2
23	PM_TA0_3	TA0_CCR3 capture input CCR3A	TA0_CCR3 compare output Out3
24	PM_TA0_4	TA0_CCR4 capture input CCR4A	TA0_CCR4 compare output Out4
25	PM_TA1_1	TA1_CCR1 capture input CCR1A	TA1_CCR1 compare output Out1
26	PM_TA1_2	TA1_CCR2 capture input CCR2A	TA1_CCR2 compare output Out2
27	PM_TA1_3	TA1_CCR3 capture input CCR3A	TA1_CCR3 compare output Out3
28	PM_TA1_7	TA1_CCR4 capture input CCR4A	TA1_CCR4 compare output Out4

Table 6-44. Port Mapping Mnemonics and Functions (continued)

VALUE	PRIMARY MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
28	PM_TA0CLK	Timer _{TA0} external clock input	None
	PM_TA0IO1	None	Compass/IO-2 output
29	PM_TA0CLK	Timer _{TA0} external clock input	None
	PM_TA0IO2	None	Compass/IO-1 output
30	PM_TA0IO1	IOVREF input	None
	PM_TA0CLK	None	SMCLK
31 (GPIO ⁽¹⁾)	PM_GPIO0G	Disable the output driver and the input Schmitt trigger to prevent excessive current when applying analog signals.	

(1) The value of the PM_GPIO0G mnemonic is 31. This port mapping implies any 5-bit wide, and the upper bits are ignored, which means 0x1000000000000000.

Table 6-45. Default Mapping

PIN NAME	PRIMARY MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
P2.0/PM_UC0A15TE	PM_UC0A15TE	eUSCI_A1 SPI slave transmit enable (direction controlled by eUSCI)	
P2.0/PM_UC0A15C	PM_UC0A15C	eUSCI_A1 clock input/output direction controlled by eUSCI	
P2.2/PM_UC0A15RXD ⁽¹⁾ PM_UC0A15M	PM_UC0A15RXD ⁽¹⁾ PM_UC0A15M	eUSCI_A1 UART RXD (direction controlled by eUSCI) Input eUSCI_A1 SPI slave output master in (direction controlled by eUSCI)	
P2.3/PM_UC0A15TXD ⁽¹⁾ PM_UC0A15M	PM_UC0A15TXD ⁽¹⁾ PM_UC0A15M	eUSCI_A1 UART TXD (direction controlled by eUSCI) Output eUSCI_A1 SPI slave in master out (direction controlled by eUSCI)	
P2.4/PM_TA0IO1 ⁽²⁾	PM_TA0IO1	TAC_CCR1 capture input CCR1A	TA0_CCR1 compare output Out1
P2.5/PM_TA0IO2 ⁽²⁾	PM_TA0IO2	TAC_CCR2 capture input CCR2A	TA0_CCR2 compare output Out2
P2.6/PM_TA0IO3 ⁽²⁾	PM_TA0IO3	TAC_CCR3 capture input CCR3A	TA0_CCR3 compare output Out3
P2.7/PM_TA0IO4 ⁽²⁾	PM_TA0IO4	TAC_CCR4 capture input CCR4A	TA0_CCR4 compare output Out4
P3.0/PM_UC0B15TE	PM_UC0B15TE	eUSCI_B1 SPI slave transmit enable (direction controlled by eUSCI)	
P3.0/PM_UC0B15C	PM_UC0B15C	eUSCI_B1 clock input/output direction controlled by eUSCI	
P3.2/PM_UC0B15RXD ⁽¹⁾ PM_UC0B15M	PM_UC0B15RXD ⁽¹⁾ PM_UC0B15M	eUSCI_B1 UART RXD (direction controlled by eUSCI) Input eUSCI_B1 SPI slave output master in (direction controlled by eUSCI)	
P3.3/PM_UC0B15TXD ⁽¹⁾ PM_UC0B15M	PM_UC0B15TXD ⁽¹⁾ PM_UC0B15M	eUSCI_B1 UART TXD (direction controlled by eUSCI) Output eUSCI_B1 SPI slave in master out (direction controlled by eUSCI)	
P3.4/PM_UC0B15TE	PM_UC0B15TE	eUSCI_B2 SPI slave transmit enable (direction controlled by eUSCI)	
P3.5/PM_UC0B15C	PM_UC0B15C	eUSCI_B2 clock input/output direction controlled by eUSCI	
P3.6/PM_UC0B15RXD ⁽¹⁾ PM_UC0B15M	PM_UC0B15RXD ⁽¹⁾ PM_UC0B15M	eUSCI_B2 UART RXD (direction controlled by eUSCI) Input eUSCI_B2 SPI slave output master in (direction controlled by eUSCI)	
P3.7/PM_UC0B15TXD ⁽¹⁾ PM_UC0B15M	PM_UC0B15TXD ⁽¹⁾ PM_UC0B15M	eUSCI_B2 UART TXD (direction controlled by eUSCI) Output eUSCI_B2 SPI slave in master out (direction controlled by eUSCI)	
P7.0/PM_SMCLK ⁽¹⁾ PM_TA0IO1	PM_SMCLK ⁽¹⁾ PM_TA0IO1	DRIVE0 Input	SMCLK
P7.1/PM_G0OUT ⁽¹⁾ PM_TA0IO2	PM_G0OUT ⁽¹⁾ PM_TA0IO2	Timer _{TA0} external clock input	Compass/IO-2 output
P7.2/PM_G1OUT ⁽¹⁾ PM_TA0IO3	PM_G1OUT ⁽¹⁾ PM_TA0IO3	Timer _{TA1} external clock input	Compass/IO-1 output
P7.3/PM_TA0IO1 ⁽²⁾	PM_TA0IO1	TAC_CCR1 capture input CCR1A	TA0_CCR1 compare output Out1
P7.4/PM_TA0IO2 ⁽²⁾	PM_TA0IO2	TAC_CCR2 capture input CCR2A	TA0_CCR2 compare output Out2
P7.5/PM_TA0IO3 ⁽²⁾	PM_TA0IO3	TAC_CCR3 capture input CCR3A	TA0_CCR3 compare output Out3
P7.6/PM_TA0IO4 ⁽²⁾	PM_TA0IO4	TAC_CCR4 capture input CCR4A	TA0_CCR4 compare output Out4

(1) Not available on the 64-pin TQFP package.

6.9.3 Timer_A

Timers TA0, TA1, TA2 and TA3 are 16-bit timers/counters (Timer_A type) with five capture/compare registers each. Each timer supports multiple capture/compares, PWM outputs, and interval timing. Each has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

6.9.3.1 Timer_A Signal Connection Tables

Table 6-46 through Table 6-49 list the interface signals of the Timer_A modules on the device and connections of the interface signals to the corresponding pins or internal signals. The following rules apply to the naming conventions used:

- The first column lists the device-level pin or internal signal that sources the clocks and/or triggers into the Timer. The default assumption is that these are pins, unless specifically marked as internal. Nomenclature used for internal signals is as follows:
 - CxOUT: output from Comparator x.
 - TAx_Cy: Output from Timer x, Capture/Compare module y.
- The second column lists the input signals of the Timer module.
- The third column lists the submodule of the Timer and also implies the functionality (Timer, Capture (Inputs or Triggers), or Compare (Outputs or PWM)).
- The fourth column lists the output signals of the Timer module.
- The fifth column lists the device-level pin or internal signal that is driven by the outputs of the Timer. The default assumption is that these are pins, unless specifically marked as internal.

NOTE

The pin names listed in the tables are the complete names. It is the responsibility of the software to ensure that the pin is used in the intended mode for the targeted Timer functionality.

NOTE

Internal signals that are sourced by the Timer outputs may connect to other modules (for example, other timers or the ADC) in the device (as trigger sources).

Table 6-46. TAO Signal Connections

DEVICE INPUT PIN OR INTERNAL SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT PIN OR INTERNAL SIGNAL
P1.0P1.0 (Output Pin) TAO0_K	TA00K	Timer	NA	NA
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
UCCLK (internal)	UCCLK			
P1.3P1.3 TAO0	OC0A5	CCR0	TA0	P1.3P1.3 TAO0 (AO_C0 (internal))
DVss	OC0B5			
DVss	GND			
DVss	Vcc			
P1.4P1.4 TAO1	OC1A	CCR1	TA1	P1.4P1.4 TAO1 TA0_C1 (internal) ADC14 (internal) ADC14HSx – (?)
ACLK (internal)	OC1B			
DVss	GND			
DVss	Vcc			
P2.5P2.5 TAO2	OC2A	CCR2	TA2	P2.5P2.5 TAO2 (AO_C2 (internal) ADC14 (internal) ADC14HS (Set = 0))
UCCLK (internal)	OC2B			
DVss	GND			
DVss	Vcc			
P2.6P2.6 TAO3	OC3A	CCR3	TA3	P2.6P2.6 TAO3 TA0_C3 (internal)
UCCLK (internal)	OC3B			
DVss	GND			
DVss	Vcc			
P2.7P2.7 TAO4	OC4A	CCR4	TA4	P2.7P2.7 TAO4 (AO_C4 (internal))
TA1_C4 (internal)	OC4B			
DVss	GND			
DVss	Vcc			

Table 6-47. TA1 Signal Connections

DEVICE INPUT PIN OR INTERNAL SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT PIN OR INTERNAL SIGNAL
P7.1P01 (GPIO/PWM TA102_K)	TA0101	Timer	NA	NA
ACLK (internal)	ACLK			
SMCLK (Normal)	SMCLK			
UTCLK (Normal)	UTCLK			
PS.WUCBSSTBTA10V0.1	OC0A5	C030	TA0	PS.WUCBSSTBTA10V0.1 (TA1_C0 (internal))
DVDD	OC0B5			
DVDD	CND			
DVDD	VDD			
P7.1P01 (TA1_0V0.2)	OC01A	CCR0	TA1	P7.1P01 (TA1_0V0.2) (TA1_C1 (internal)) ADC14 (Normal) ADC14S (Set-C)
ACLK (internal)	OC01B			
DVDD	GND			
DVDD	VDD			
P7.1P01 (TA1_0V0.3)	OC02A	C032	TA0	P7.1P01 (TA1_0V0.3) (TA1_C2 (internal)) ADC14 (Normal) ADC14S (Set-C)
UTCLK (Normal)	OC02B			
DVDD	CND			
DVDD	VDD			
P7.1P01 (TA1_0V0.4)	OC03A	CCR0	TA1	P7.1P01 (TA1_0V0.4) (TA1_C3 (internal))
UTCLK (Normal)	OC03B			
DVDD	CND			
DVDD	VDD			
P7.1P01 (TA1_0V0.5)	OC04A	CCR4	TA4	P7.1P01 (TA1_0V0.5) (TA1_C4 (internal))
TA0_C4 (Normal)	OC04B			
DVDD	GND			
DVDD	VDD			

Table 6-49. TA3 Signal Connections

DEVICE INPUT PIN OR INTERNAL SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT PIN OR INTERNAL SIGNAL
P0.3/TA3T1/0477	TA3T1	Timer	NA	NA
P0.4/0404/0406	ACLK			
SMCLK (Internal)	SMCLK			
From Capacitive Touch IO 1 (Internal)	BT3TX	CCR0	TA0	P10.4/AS0402 / TA3_C0 (Internal)
P10.4/TA3T003/4	EX03A			
OVSS	OVSS			
P10.5/TA3T004/6	EX04A	CCR1	TA1	P10.5/AS1004/6 TA3_C1 (Internal) APO14 (Internal) ADUT48MSK = 0
OVSS	OVSS			
OVSS	OVSS			
P10.2/0402/0402	EX02A	CCR2	TA2	P10.2/AS0402/5 TA3_C2 (Internal)
COOUT (Internal)	CO2B			
OVSS	OVSS			
P0.2/TA3T1	EX01A	CCR3	TA3	P0.2/TA3T3/4 TA3_C3 (Internal)
TA3T3 (Internal)	EX03A			
OVSS	OVSS			
P0.3/TA3T4	EX04A	CCR4	TA4	P0.3/TA3T7 TA3_C4 (Internal)
From Capacitive Touch IO (Internal)	CO4B			
OVSS	OVSS			

6.9.4 Timer32

Timer32 is an ARM dual 32-bit timer module. It contains two 32-bit timers, each of which can be configured as two independent 16-bit timers. The two timers can generate independent events or a combined event, which can be processed according to application requirements. Timer32 runs out of the same clock as the Cortex-M4 CPU.

6.9.5 Enhanced Universal Serial Communication Interface (eUSCI)

The eUSCI modules are used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3-pin or 4-pin) and I²C, and asynchronous communication protocols such as UART, enhanced UART with automatic baud-rate detection, and IrDA.

The eUSCI_A module provides support for SPI (3-pin or 4-pin), UART, enhanced UART, and IrDA.

The eUSCI_B module provides support for SPI (3-pin or 4-pin) and I²C.

The MSP432P401x MCUs offer up to four eUSCI_A and four eUSCI_B modules.

6.9.6 Real-Time Clock (RTC_C)

The RTC_C module contains an integrated real-time clock. It integrates an internal calendar which compensates for months with less than 31 days and includes leap year correction. The RTC_C also supports flexible alarm functions, offset calibration, and temperature compensation. The RTC_C operation is available in LPM3 and LPM3.5 modes to minimize power consumption.

6.9.7 Watchdog Timer (WDT_A)

The primary function of the WDT_A module is to perform a controlled system restart if a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

CAUTION

The WDT must be set to interval mode before transitioning into the LPM3 or LPM3.5 modes of operation. This allows the WDT event to wake the device and return it to active modes of operation. Using the WDT in watchdog mode may result in nondeterministic behavior due to the generated reset.

The watchdog can generate a reset on either a time-out or a password violation. This reset can be configured to generate either a Hard Reset or a Soft Reset into the system. See the [MSP432P4xx Family Technical Reference Manual](#) for more details. The WDT should typically be configured to generate a Hard reset into the system. A Soft reset resets the CPU but leaves the rest of the system and peripherals unaffected. As a result, if the WDT is configured to generate a Soft reset, the application should assume responsibility for the fact that a Soft reset can corrupt an ongoing transaction from the CPU into the system.

Table 6-50 lists the clocks that can be selected as the source for the WDT_A module.

Table 6-50. WDT_A Clocks

WDTSEL	NORMAL OPERATION (WATCHDOG AND INTERVAL TIMER MODE)
00	SMCLK
01	ACLK
10	SMCLK
11	BCLK

6.9.8 ADC14

The ADC14 module supports 14-bit analog-to-digital conversions up to 1 Msps sampling rate with differential and single-ended inputs. The module implements a 14-bit SAR core, sample and hold circuit, reference generator and a conversion result buffer. The window comparators with a lower and upper limit allow CPU independent result monitoring through different window comparator interrupt flags.

The available ADC14 external trigger sources are summarized in Table 6-51.

Table 6-51. ADC14 Trigger Signal Connections

ADC14SSELx		CONNECTED TRIGGER SOURCE
BINARY	DECIMAL	
000	0	Software (ADC14SC)
001	1	AD1_C0
010	2	TAD_C0
011	3	TAD_C1
100	4	TAD_C2
101	5	TAD_C3
110	6	AD2_C0
111	7	TAD_C0

Table 6-52, Table 6-53, and Table 6-54 list the available multiplexing between internal and external analog inputs of ADC14.

Table 6-52. ADC14 Channel Mapping on 100-Pin PZ Devices

ADC14 CHANNEL	EXTERNAL CHANNEL SOURCE (CONTROL BIT = 0)	INTERNAL CHANNEL SOURCE (CONTROL BIT = 1) ⁽¹⁾	CONTROL BIT ⁽²⁾
Channel 20	A20	Battery Monitor	ADC14BATMP
Channel 21	A21	Temperature Sensor	ADC14TCMP
Channel 22	A22	N/A (Reserved)	ADC14CH0MP
Channel 23	A23	N/A (Reserved)	ADC14CH1MP
Channel 19	A19	N/A (Reserved)	ADC14CH2MP
Channel 18	A18	N/A (Reserved)	ADC14CH3MP

- (1) If an internal source is marked as N/A (Reserved), it indicates that only the external source is available for that channel.
(2) See the ADC14 chapter in the [MSP432Pxx Family Technical Reference Manual](#) for details on the registers that contain the control bits listed in the table.

Table 6-53. ADC14 Channel Mapping on 80-Pin ZXH Devices

ADC14 CHANNEL	EXTERNAL CHANNEL SOURCE (CONTROL BIT = 0)	INTERNAL CHANNEL SOURCE (CONTROL BIT = 1) ⁽¹⁾	CONTROL BIT ⁽²⁾
Channel 10	A10	Battery Monitor	ADC14BATMP
Channel 14	A14	Temperature Sensor	ADC14TCMP
Channel 13	A13	N/A (Reserved)	ADC14CH0MP
Channel 12	A12	N/A (Reserved)	ADC14CH1MP
Channel 11	A11	N/A (Reserved)	ADC14CH2MP
Channel 16	A16	N/A (Reserved)	ADC14CH3MP

- (1) If an internal source is marked as N/A (Reserved), it indicates that only the external source is available for that channel.
(2) See the ADC14 chapter in the [MSP432Pxx Family Technical Reference Manual](#) for details on the registers that contain the control bits listed in the table.

In 2-pin SWD mode, the TDO pin can be used to export serial wire trace output (SWO) data. In addition, the TDI and TDO pins of the device can be reassigned as user I/Os. See [Section 6.12.22](#) and [Section 6.12.23](#) for more details.

NOTE

If the device has activated debug security, debugger accesses into the device is completely disabled. The debugger, however, is still able to scan the run-time state of the CPU. Further control of and visibility into the device is possible only after initiating a mass-erase of the device flash contents.

6.10.2 Peripheral Halt Control

The Peripheral Halt Control register in the System Controller module allows the user independent control over the functionality of device peripherals during code development and debug. When the CPU is halted, the bits in this register can control whether the corresponding peripheral freezes its operation (such as incrementing, increment, and receive) or continues its operation (debug remains non-intrusive). The registers of the peripheral remain accessible without regard to the values in the Peripheral Halt Control register.

6.10.3 Bootloader (BSL)

The BSL enables users to program flash or SRAM on the device using a UART or I²C or SPI serial interface. Access to the device memory through the BSL is protected by a user-defined password. [Table 6-55](#) lists the device pins that are required to use the BSL.

Table 6-55. BSL Pins and Functions

DEVICE PIN	BSL FUNCTION
P1.2	UART BSL TXD
P1.3	UART BSL RXD
P1.4	SPI BSL SCK
P1.5	SPI BSL CS0
P1.8	SPI BSL SS0
P1.7	SPI BSL CS1
P0.6	I ² C BSL SDA
P0.7	I ² C BSL SCL

The BSL is invoked under any of the following conditions:

- Flash main memory is erased
- Hardware invocation of BSL
- Software-based API calls to BSL functions

The user can perform hardware invocation of BSL using any pin of ports P1, P2, or P3. The pin selected for this purpose should not be same as the ones used for BSL. The user can configure the device pin and its polarity through the flash boot-override mailbox. The BSL can then be invoked upon a power cycle or POR reset event with the configured pin.

For the complete description of the BSL features and its implementation, see the [MSP432P401R Bootloader \(BSL\) User's Guide](#).

6.11.2 CoreMark/MHz Performance: 3.41

Table 6-58 shows the software configuration for this performance benchmark. Table 6-59 shows the profile configuration.

Table 6-58. Software Configuration

ITEMS	DETAILS
Compiler Name and Version	ARM Compiler v5.0.3
Compiler Flags	-mcpu=cortex-m4 -mfloat-abi=hardfloat -mthumb -mcpu=cortex-m4 -mfloat-abi=hardfloat
CoreMark Profile and Version	v1.0

Table 6-59. Profile Configuration

CONFIGURATION	DETAILS
Active Power Mode Name	Active Mode
Active Mode Clock Configuration	CPU: 3 MHz
Active Mode Voltage Integrity	1.02 V

6.11.3 DMIPS/MHz (Dhrystone 2.1) Performance: 1.22

Table 6-60 shows the software configuration for this performance benchmark. Table 6-61 shows the profile configuration.

Table 6-60. Software Configuration

ITEMS	DETAILS
Compiler Name and Version	ARM Compiler v5.0.3
Compiler Flags	-mcpu=cortex-m4 -mfloat-abi=hardfloat -mthumb -mcpu=cortex-m4 -mfloat-abi=hardfloat
Dhrystone Profile and Version	v2.1

Table 6-61. Profile Configuration

CONFIGURATION	DETAILS
Active Power Mode Name	Active Mode
Active Mode Clock Configuration	CPU: 3 MHz
Active Mode Voltage Integrity	1.02 V

Table 6-62. Port P1 (P1.0 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P1DIR.x	P1SEL1.x	P1SEL2.x
P1.0 UC0A0EVT	0	P1.0 (IO)	I/O, O:1	0	0
		UC0A0EVT	x ⁽²⁾	0	1
		NA	0		
		DVSS	1	1	0
		NA	0	1	1
P1.1 UC0A0CLK	1	P1.1 (IO)	I/O, O:1	0	0
		UC0A0CLK	x ⁽²⁾	0	1
		NA	0		
		DVSS	1	1	0
		NA	0	1	1
P1.2 UC0A0RX/UC0A0SDA	2	P1.2 (IO)	I/O, O:1	0	0
		UC0A0RX/UC0A0SDA	x ⁽²⁾	0	1
		NA	0		
		DVSS	1	1	0
		NA	0	1	1
P1.3 UC0A0RX/UC0A0SDA	3	P1.3 (IO)	I/O, O:1	0	0
		UC0A0RX/UC0A0SDA	x ⁽²⁾	0	1
		NA	0		
		DVSS	1	1	0
		NA	0	1	1
P1.4 UC0A0STE	4	P1.4 (IO)	I/O, O:1	0	0
		UC0A0STE	x ⁽²⁾	0	1
		NA	0		
		DVSS	1	1	0
		NA	0	1	1
P1.5 UC0A0CLK	5	P1.5 (IO)	I/O, O:1	0	0
		UC0A0CLK	x ⁽²⁾	0	1
		NA	0		
		DVSS	1	1	0
		NA	0	1	1
P1.6 UC0A0M0/UC0A0SDA	6	P1.6 (IO)	I/O, O:1	0	0
		UC0A0M0/UC0A0SDA	x ⁽²⁾	0	1
		NA	0		
		DVSS	1	1	0
		NA	0	1	1

(1) x = configuration

(2) Direction controlled by UC0A0_AD module

(3) Direction controlled by UC0A0_BQ module

Table 6-82. Port P1 (P1.0 to P1.7) Pin Functions (continued)

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ^{1,2}		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1-P1.0 (P1.0 to P1.0)	0	P1.7 (STN)	1 0 0 1	0	0
		UCB0SDMAUCB0SDC	x ³	0	1
		MA	0	1	0
		DA20	1		
		MA	0	1	1
P1-P1.1 (P1.1 to P1.1)	1	DA20	1		
		MA	0	1	1
		DA20	1		
		MA	0	1	1
		DA20	1		

6.12.2 Port P2 (P2.0 to P2.3) Input/Output With Schmitt Trigger

Figure 8-7 shows the port diagram. Table 8-63 summarizes the selection of the pin functions.

Table 8-63. Port P2 (P2.0 to P2.3) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
			P2DIR.x	P2SEL1.x	P2SEL0.x	P2MAPx
P2.0PM_UCAMST ⁽²⁾	0	P2.0 (IO)	I/O, 0	0	0	X
		UCAMSTE	X ⁽²⁾	0	1	default
		NA	0	1	0	X
		DVSS	1	1	0	X
		NA	0	1	1	X
P2.1PM_UCAMCLK	1	P2.1 (IO)	I/O, 0, 1	0	0	X
		UCAMCLK	X ⁽²⁾	0	1	default
		NA	0	1	0	X
		DVSS	1	1	0	X
		NA	0	1	1	X
P2.2PM_UCAMQNTM_U_CAMQNTM	2	P2.2 (IO)	I/O, 0	0	0	X
		UCAMQNTM_U_CAMQNTM	X ⁽²⁾	0	1	default
		NA	0	1	0	X
		DVSS	1	1	0	X
		NA	0	1	1	X
P2.3PM_UCAMTXDRM_U_CAMTXDRM	3	P2.3 (IO)	I/O, 0, 1	0	0	X
		UCAMTXDRM_U_CAMTXDRM	X ⁽²⁾	0	1	default
		NA	0	1	0	X
		DVSS	1	1	0	X
		NA	0	1	1	X

(1) X = don't care

(2) Function controlled by UCAMQNTM module

6.12.3 Port P3 (P3.0 to P3.7) Input/Output With Schmitt Trigger

Figure 8-7 shows the port diagram. Table 8-64 summarizes the selection of the pin functions.

Table 8-64. Port P3 (P3.0 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
			P3DIR.x	P3SEL1.x	P3SEL0.x	P3MAPx
P3.0PM_UCAS2ET	0	P3.0 (IO)	1 0 0 1	0	0	X
		UCAS2E	X ⁽²⁾	0	1	default
		NA	0			
		DVSS	1	1	0	X
		NA	0			
P3.1PM_UCAS2CLK	1	P3.1 (IO)	1 0 0 1	0	0	X
		UCAS2CLK	X ⁽²⁾	0	1	default
		NA	0			
		DVSS	1	1	0	X
		NA	0			
P3.2PM_UCAS2QEM0_UCA230M0	2	P3.2 (IO)	1 0 0 1	0	0	X
		UCAS2QEM0/UCAS2QEM0	X ⁽²⁾	0	1	default
		NA	0			
		DVSS	1	1	0	X
		NA	0			
P3.3PM_UCAS2TXD0PM_UCA230M0	3	P3.3 (IO)	1 0 0 1	0	0	X
		UCAS2TXD0/UCAS2TXD0	X ⁽²⁾	0	1	default
		NA	0			
		DVSS	1	1	0	X
		NA	0			
P3.4PM_UCAS2STE	4	P3.4 (IO)	1 0 0 1	0	0	X
		UCAS2STE	X ⁽²⁾	0	1	default
		NA	0			
		DVSS	1	1	0	X
		NA	0			
P3.5PM_UCAS2CLK	5	P3.5 (IO)	1 0 0 1	0	0	X
		UCAS2CLK	X ⁽²⁾	0	1	default
		NA	0			
		DVSS	1	1	0	X
		NA	0			
P3.6PM_UCAS2CLK	6	P3.6 (IO)	1 0 0 1	0	0	X
		UCAS2CLK	X ⁽²⁾	0	1	default
		NA	0			
		DVSS	1	1	0	X
		NA	0			

(1) X = don't care.

(2) Direction controlled by UCAS2E module.

(3) Direction controlled by UCAS2E module.

Table 6-84. Port P3 (P3.0 to P3.7) Pin Functions (continued)

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
			P3DIR.x	P3SEL1.x	P3SEL0.x	P3MAPx
P3.0/MI_UCE2600H/MI_UCE250A	0	P3.0 (IO)	1, 0, 0, 1	0	0	X
		UC2600H/MI_UCE250A	X ⁽²⁾	0	1	default
		NA	0			
		DVSS	1	1	0	X
		NA	0			
P3.1/MI_UCE2600H/MI_UCE250A	1	P3.1 (IO)	1, 0, 0, 1	0	0	X
		UC2600H/MI_UCE250A	X ⁽²⁾	0	1	default
		NA	0			
		DVSS	1	1	0	X
		NA	0			
P3.2/MI_UCE2600H/MI_UCE250A	2	P3.2 (IO)	1, 0, 0, 1	0	0	X
		UC2600H/MI_UCE250A	X ⁽²⁾	0	1	default
		NA	0			
		DVSS	1	1	0	X
		NA	0			
P3.3/MI_UCE2600H/MI_UCE250A	3	P3.3 (IO)	1, 0, 0, 1	0	0	X
		UC2600H/MI_UCE250A	X ⁽²⁾	0	1	default
		NA	0			
		DVSS	1	1	0	X
		NA	0			
P3.4/MI_UCE2600H/MI_UCE250A	4	P3.4 (IO)	1, 0, 0, 1	0	0	X
		UC2600H/MI_UCE250A	X ⁽²⁾	0	1	default
		NA	0			
		DVSS	1	1	0	X
		NA	0			
P3.5/MI_UCE2600H/MI_UCE250A	5	P3.5 (IO)	1, 0, 0, 1	0	0	X
		UC2600H/MI_UCE250A	X ⁽²⁾	0	1	default
		NA	0			
		DVSS	1	1	0	X
		NA	0			
P3.6/MI_UCE2600H/MI_UCE250A	6	P3.6 (IO)	1, 0, 0, 1	0	0	X
		UC2600H/MI_UCE250A	X ⁽²⁾	0	1	default
		NA	0			
		DVSS	1	1	0	X
		NA	0			
P3.7/MI_UCE2600H/MI_UCE250A	7	P3.7 (IO)	1, 0, 0, 1	0	0	X
		UC2600H/MI_UCE250A	X ⁽²⁾	0	1	default
		NA	0			
		DVSS	1	1	0	X
		NA	0			

6.12.4 Port P9 (P9.4 to P9.7) Input/Output With Schmitt Trigger

Figure 8-7 shows the port diagram. Table 8-65 summarizes the selection of the pin functions.

Table 8-65. Port P9 (P9.4 to P9.7) Pin Functions

PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			PMR x	PSR1 x	PSR2 x
P9.4UCACSTE ⁽²⁾	4	P9.4 (IO)	1 0, 0 1	0	0
		UCACSTE	X ⁽³⁾	0	1
		NA	0	1	0
		DVSS	1		
		NA	0	1	1
		DVSS	1		
P9.5UCACQCLK ⁽³⁾	5	P9.5 (IO)	1 0, 0 1	0	0
		UCACQCLK	X ⁽³⁾	0	1
		NA	0	1	0
		DVSS	1		
		NA	0	1	1
		DVSS	1		
P9.6UCACQCLKUCACSSQNC ⁽³⁾	6	P9.6 (IO)	1 0, 0 1	0	0
		UCACQCLKUCACSSQNC	X ⁽³⁾	0	1
		NA	0	1	0
		DVSS	1		
		NA	0	1	1
		DVSS	1		
P9.7UCACSTX0UCACSSW0 ⁽²⁾	7	P9.7 (IO)	1 0, 0 1	0	0
		UCACSTX0UCACSSW0	X ⁽³⁾	0	1
		NA	0	1	0
		DVSS	1		
		NA	0	1	1
		DVSS	1		

(1) X = don't care

(2) Not available on STACTH and STACTD packages.

(3) Divider controlled by UCACLAS module.

6.12.5 Port P10 (P10.0 to P10.3) Input/Output With Schmitt Trigger

Figure 8-7 shows the port diagram. Table 8-66 summarizes the selection of the pin functions.

Table 8-66. Port P10 (P10.0 to P10.3) Pin Functions

PIN NAME (P10.X)	X	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P10DIR.x	P10SEL1.x	P10SEL0.x
P10IN0COST[1R]	0	P10.0 (IN)	1 0, 0 1	0	0
		UCSSTE	X ⁽²⁾	0	1
		NA	0		
		DVSS	1	1	0
		NA	0		
		DVSS	1	1	1
P10.1UCSCLK[1]	1	P10.1 (Q)	1 0, 0 1	0	0
		UCSCLK	X ⁽²⁾	0	1
		NA	0		
		DVSS	1	1	0
		NA	0		
		DVSS	1	1	1
P10.2UCSMDK[1]UCSQA[2]	2	P10.2 (Q)	1 0, 0 1	0	0
		UCSMDKUCSQA	X ⁽²⁾	0	1
		NA	0		
		DVSS	1	1	0
		NA	0		
		DVSS	1	1	1
P10.3UCSMDKUCSQA[2]	3	P10.3 (Q)	1 0, 0 1	0	0
		UCSMDKUCSQA	X ⁽²⁾	0	1
		NA	0		
		DVSS	1	1	0
		NA	0		
		DVSS	1	1	1

(1) X = don't care

(2) NA: not available on STACTH and 94-pin packages

(3) Divider controlled by UCSQ_B3 module.

6.12.6 Port P2 (P2.4 to P2.7) Input/Output With Schmitt Trigger

Figure 6-8 shows the port diagram. Table 6-67 summarizes the selection of the pin functions.

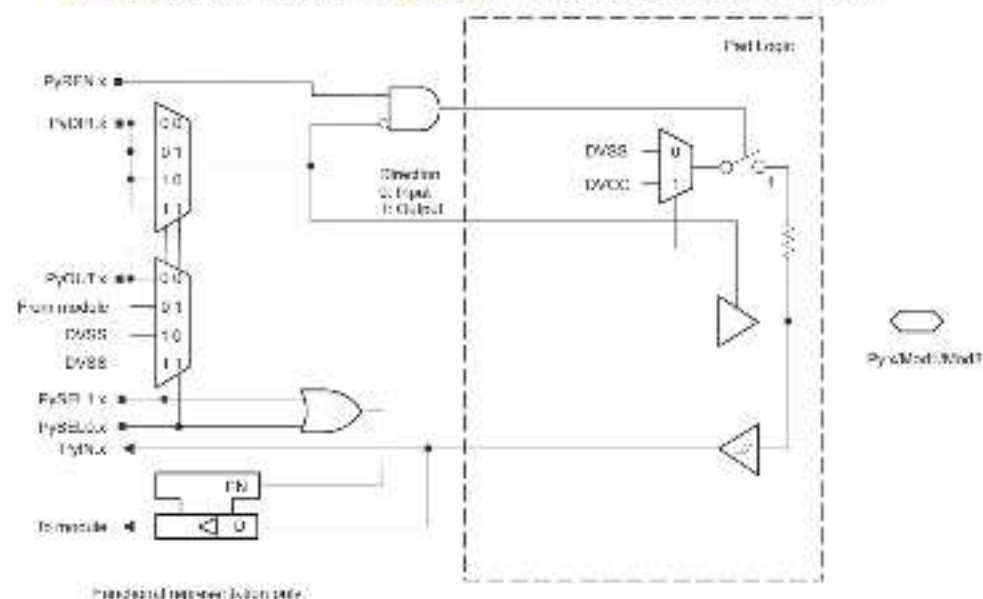


Figure 6-8. Py.x/Mod1/Mod2 Pin Diagram

Table 6-67. Port P2 (P2.4 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
			P2DIR.x	P2SEL1.x	P2SEL0.x	P2NAP.x
P2.4 (P2A_1A0) ⁽²⁾	4	P2.4 (IO)	1 0 1 1	0	0	X
		TAN(CC1A)	0	0	1	default
		TAN 1	1			
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P2.5 (P2A_1A1) ⁽²⁾	5	P2.5 (IO)	1 0 0 0 1	0	0	X
		TAN(CC2A)	0	0	1	default
		TAN 2	1			
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P2.6 (P2A_1A2) ⁽²⁾	6	P2.6 (IO)	1 0 0 0 1	0	0	X
		TAN(CC3A)	0	0	1	default
		TAN 3	1			
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			
P2.7 (P2A_1A3) ⁽²⁾	7	P2.7 (IO)	1 0 0 0 1	0	0	X
		TAN(CC4A)	0	0	1	default
		TAN 4	1			
		N/A	0	1	0	X
		DVSS	1			
		N/A	0	1	1	X
		DVSS	1			

(1) X = don't care

(2) Not available on the 64-pin RGC package

6.12.7 Port P7 (P7.0 to P7.3) Input/Output With Schmitt Trigger

Figure 8-8 shows the port diagram. Table 8-68 summarizes the selection of the pin functions.

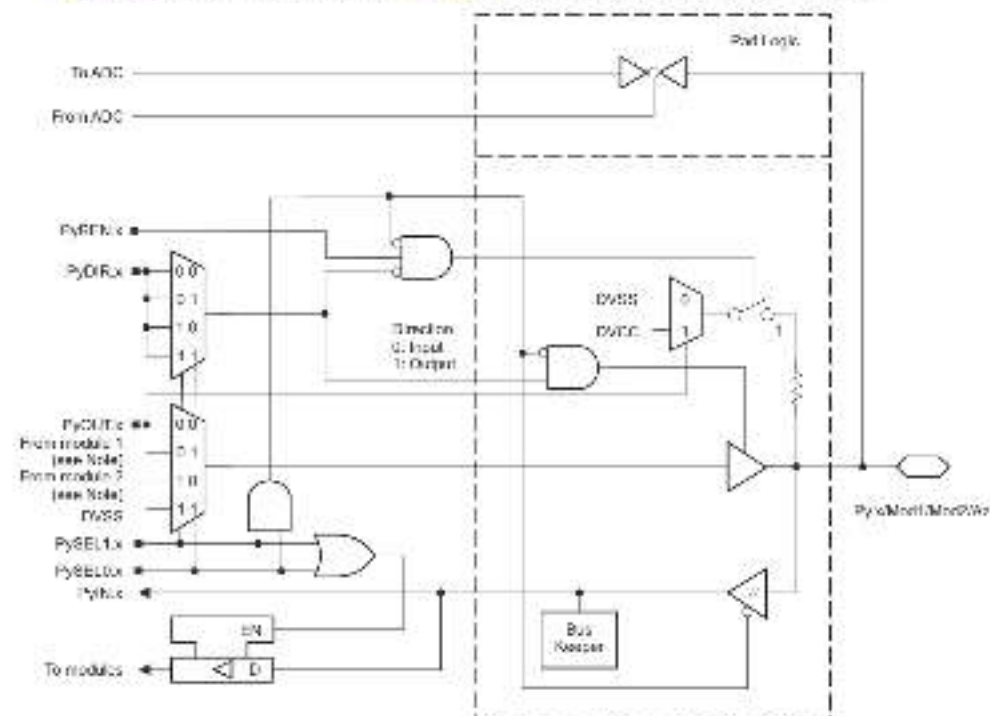
Table 8-68. Port P7 (P7.0 to P7.3) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
			P7MR.x	P7SE1.x	P7SE0.x	P7MAPx
P7.0P(L_BWCLK) PM_TWDIO	0	P7.0(C)	0:0,1	0	0	X
		DMAC0	0	0	1	default
		SWCLK	1	0	0	X
		N/A	1	1	1	X
		DVSS	1	1	1	X
		N/A	1	1	1	X
P7.1P(L_C0OUT) PM_TWDIO	1	P7.1(C)	0:0,1	0	0	X
		TACLK	0	0	1	default
		C0OUT	1	0	0	X
		N/A	1	1	0	X
		DVSS	1	1	1	X
		N/A	1	1	1	X
P7.2P(L_C0OUT) PM_TA1CLK	2	P7.2(C)	0:0,1	0	0	X
		TACLK	0	0	1	default
		C0OUT	1	1	0	X
		N/A	1	1	1	X
		DVSS	1	1	1	X
		N/A	1	1	1	X
P7.3P(L_TA0.0)	3	P7.3(C)	0:0,1	0	0	X
		TA0_C0IN	0	0	1	default
		TA0.0	1	1	0	X
		N/A	1	1	1	X
		DVSS	1	1	1	X
		N/A	1	1	1	X

(1) X = configurable

6.12.9 Port P4 (P4.0 to P4.7) Input/Output With Schmitt Trigger

Figure 6-6 shows the port diagram. Table 6-70 summarizes the selection of the pin functions.



Note: Output is DVSS if module 1 or module 2 function is not available. See the pin function table.
 Functional representation only.

Figure 6-6. Py.x/Mod1/Mod2/Ax Pin Diagram

Table 6-70. Port P4 (P4.0 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P4DIR.x	P4SEL1.x	P4SEL2.x
P4.0A15 ⁽²⁾	0	P4.0 (IO)	1, 0, 0, 1	0	0
		N/A	0		
		DVSS	1	0	1
		N/A	0		
		DVSS	1	1	0
		A15 ⁽²⁾	X	1	1
P4.1A12 ⁽²⁾	1	P4.1 (IO)	1, 0, 0, 1	0	0
		N/A	0		
		DVSS	1	0	1
		N/A	0		
		DVSS	1	1	0
		A12 ⁽²⁾	X	1	1
P4.2A10 (K7A2CLKA1)	2	P4.2 (IO)	1, 0, 0, 1	0	0
		N/A	0		
		ACLK	1	0	1
		TAPCLK	0		
		DVSS	1	1	0
		A11 ⁽²⁾	X	1	1
P4.3A00 (K4100-K1A1)	3	P4.3 (IO)	1, 0, 0, 1	0	0
		N/A	0		
		MCLK	1	0	1
		N/A	0		
		RTCLK ⁽²⁾	1	1	0
		A10 ⁽²⁾	X	1	1
P4.4A00 (MCLK3A10UT/AD)	4	P4.4 (IO)	1, 0, 0, 1	0	0
		N/A	0		
		EMCLK	1	0	1
		N/A	0		
		SMCLK3A1	1	1	0
		A9 ⁽²⁾	X	1	1
P4.5A1	5	P4.5 (IO)	1, 0, 0, 1	0	0
		N/A	0		
		DVSS	1	0	1
		N/A	0		
		DVSS	1	1	0
		A8 ⁽²⁾	X	1	1
P4.6A2	6	P4.6 (IO)	1, 0, 0, 1	0	0
		N/A	0		
		DVSS	1	0	1
		N/A	0		
		DVSS	1	1	0
		A7 ⁽²⁾	X	1	1

(1) X = don't care

(2) Not available on the 01-pin RSC package

(3) Setting MCLK1 to 0 and MCLK2 to 0 enables the output driver and the input buffer. To power the peripheral, connect the output driver to ground.

Table 6-70. Port P4 (P4.0 to P4.7) Pin Functions (continued)

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ^{1,2}		
			P4DIR.x	P4SEL1.x	P4SEL0.x
P4.0/NA6	0	TM / (0/0)	1 0, 0/1	0	0
		NA	0	0	1
		D/S5	1		
		NA	0	1	0
		D/S5	1		
		NA	X	1	1

6.12.10 Port P5 (P5.0 to P5.5) Input/Output With Schmitt Trigger

Figure 6-6 shows the port diagram. Table 6-71 summarizes the selection of the pin functions.

Table 6-71. Port P5 (P5.0 to P5.5) Pin Functions

PIN NAME (P5.x)	X	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P5DIR.x	P5SEL1.x	P5SEL0.x
P5.0/40	0	P5.0 (IO)	1 0 0 1	0	0
		N/A	0		
		TVSS	1	0	1
		N/A	0		
		DVSS	1		0
		AG2 ⁽²⁾	X	1	1
P5.1/41	1	P5.1 (IO)	1 0 0 1	0	0
		N/A	0		
		TVSS	1	0	1
		N/A	0		
		TVSS	1	1	0
		AG2 ⁽²⁾	X	1	1
P5.2/42	2	P5.2 (IO)	1 0 0 1	0	0
		N/A	0		
		DVSS	1	0	1
		N/A	0		
		DVSS	1	1	0
		AG2 ⁽²⁾	X	1	1
P5.3/43	3	P5.3 (IO)	1 0 0 1	0	0
		N/A	0		
		TVSS	1	0	1
		N/A	0		
		TVSS	1	1	0
		AG2 ⁽²⁾	X	1	1
P5.4/44	4	P5.4 (IO)	1 0 0 1	0	0
		N/A	0		
		DVSS	1	0	1
		N/A	0		
		TVSS	1	1	0
		AG2 ⁽²⁾	X	1	1
P5.5/45	5	P5.5 (IO)	1 0 0 1	0	0
		N/A	0		
		TVSS	1	0	1
		N/A	0		
		DVSS	1	1	0
		AG2 ⁽²⁾	X	1	1

(1) X = don't care.

(2) Setting P5AG1 to 0 and P5AG2 to 0 enables the output driver and the input internal trigger, as power pins do not connect when operating on a single supply.

6.12.11 Port P6 (P6.0 and P6.1) Input/Output With Schmitt Trigger

Figure 6-6 shows the port diagram. Table 6-72 summarizes the selection of the pin functions.

Table 6-72. Port P6 (P6.0 and P6.1) Pin Functions

PIN NAME (P6.x)	X	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P6DIR.x	P6PSEL1.x	P6PSEL0.x
P6.0/4 (N ⁽²⁾)	0	P6.0 (I/O)	1, 0, 0, 1	0	0
		N/A	0		
		DVSS	1	0	1
		N/A	0		
		DVSS	1	1	0
		Alt5 ⁽³⁾	X	1	1
P6.1/5 (4/5)	1	P6.1 (I/O)	1, 0, 0, 1	0	0
		N/A	0		
		DVSS	1	0	1
		N/A	0		
		DVSS	1	1	0
		Alt4 ⁽³⁾	X	1	1

(1) X = don't care.

(2) Not available on the 64-pin TQFP package.

(3) Selects P6PSEL1.x and P6PSEL0.x to enable the output driver and the input if Schmitt trigger is present (in power pin mode), more currently when [MSP432P401R](#) or [MSP432P401M](#).

6.12.12 Port P8 (P8.2 to P8.7) Input/Output With Schmitt Trigger

Figure 6-6 shows the port diagram. Table 6-73 summarizes the selection of the pin functions.

Table 6-73. Port P8 (P8.2 to P8.7) Pin Functions

PIN NAME (P&x)	X	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P8DIR x	P8SEL1 x	P8SEL0 x
P8.2(A0/A20) ⁽²⁾	2	M1.2 (IO)	I (0) D (1)	0	0
		TAG0CQ2A	0	0	0
		TAT1.2	1	0	0
		N/A	0	0	0
		DVSS	1	1	0
		A20 ⁽³⁾	X	1	1
P8.3(TA0C1/KA22/0)	3	P8.3 (IO)	I (0) O (1)	0	0
		TAT0C1K	0	0	0
		KA22/0	1	0	0
		N/A	0	1	0
		KA22/0	1	1	0
		A22 ⁽³⁾	X	1	1
P8.4(A1) ⁽²⁾	4	P8.4 (IO)	I (0) O (1)	0	0
		N/A	0	0	0
		DVSS	1	0	1
		N/A	0	1	0
		DVSS	1	1	0
		A0/A1	X	1	1
P8.5(A20) ⁽²⁾	5	P8.5 (IO)	I (0) D (1)	0	0
		N/A	0	0	0
		KA20/0	1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		A20 ⁽³⁾	X	1	1
P8.6(A10) ⁽²⁾	6	P8.6 (IO)	I (0) O (1)	0	0
		N/A	0	0	0
		DVSS	1	0	1
		N/A	0	1	0
		KA10/0	1	1	0
		A10 ⁽³⁾	X	1	1
P8.7(A10) ⁽²⁾	7	M1.7 (IO)	I (0) D (1)	0	0
		N/A	0	0	0
		DVSS	1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		A10 ⁽³⁾	X	1	1

(1) X = don't care

(2) Not available on M4301 and M4302 packages

(3) Setting P8SEL1x and P8SEL0x enables the output driver and the input Schmitt trigger to prevent possible cross currents when applying analog voltage

6.12.14 Port P5 (P5.6 and P5.7) Input/Output With Schmitt Trigger

Figure 6-10 shows the port diagram. Table 6-75 summarizes the selection of the pin functions.

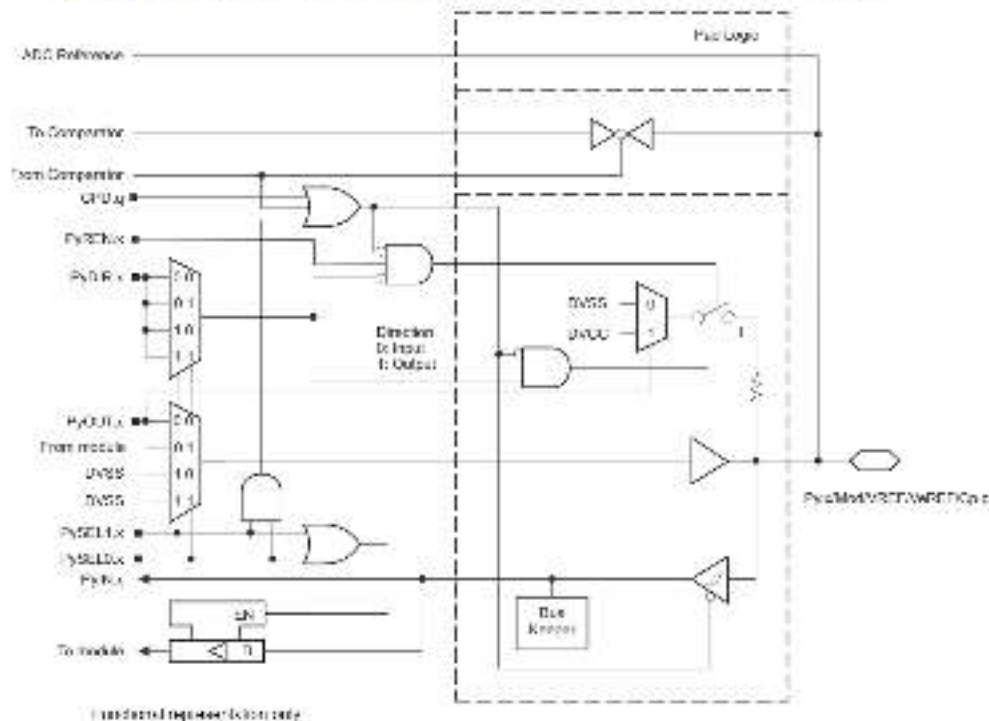


Figure 6-10. Py.x/Mod/VREF/VeREF/Cp.q Pin Diagram

Table 6-75. Port P5 (P5.6 and P5.7) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			PSDRx	PESELx	PESEL3x
P5.6(A2) (VREF) (VREF) (VREF) (VREF)	6	PS.DR0	1, 0, 0, 1	0	0
		TA2.CC1A	0	0	1
		TA2.1	1		
		N/A	0	1	0
		OVSS	1		
P5.7(TA2.DVREF) (VREF) (VREF) (VREF)	7	WRT0 + WRT0 (OUT2(2))	X	1	1
		PS.T(0)	1, 0, 0, 1	0	0
		TA2.CC1A	0	0	1
		TA2.2	1		
		N/A	0	1	0
		OVSS	1		
P5.7(TA2.DVREF) (VREF) (VREF) (VREF)	7	WRT0 + WRT0 (OUT2(2))	X	1	1

(1) X = don't care.

- (2) Setting PSDR0 to 1 and PSDR0 to 0 enables the output driver and the input buffer, respectively, in power-preserving mode when applying analog signals.
- (3) Setting the PS.T(0) bit in the comparator disables the output driver and the input buffer, together, to prevent excessive currents when applying analog signals. Selecting the OUT1 input pin to the comparator multiplexer with the CEMPSEL or CEMPSEL bits permanently disables the output driver and input buffer for that pin, regardless of the value of the associated PS.DR bit.

6.12.15 Port P6 (P6.2 to P6.5) Input/Output With Schmitt Trigger

Figure 6-11 shows the port diagram. Table 8-76 summarizes the selection of the pin functions.

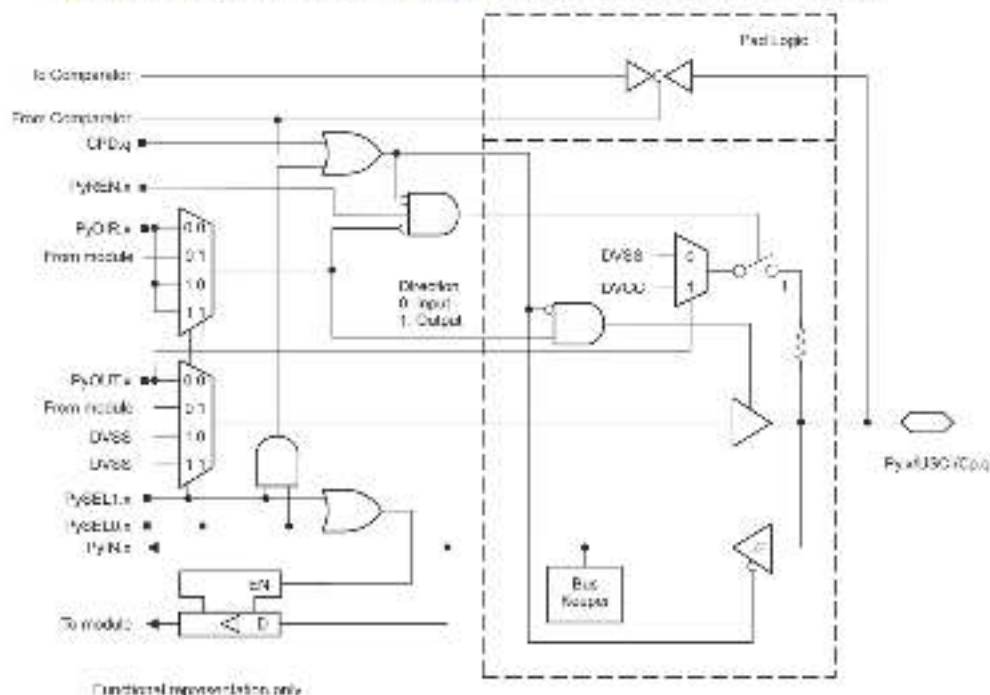


Figure 6-11. Py.x/USC/Cp.q Pin Diagram

Table 6-76. Port P6 (P6.2 to P6.5) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			PSDIR.x	PESEL1.x	PESEL0.x
P6.2(UCE18TCLK/SPI)	2	P6.2 (0x0)	1 (0, 0: 1)	0	0
		UCB18TCLK	X ⁽²⁾	0	1
		N/A	0		
		UVSS	1	1	0
		C1.2(4M)	X	1	1
P6.3(UCE10CLK/SPI)	3	P6.3 (0x0)	1 (0, 0: 1)	0	0
		UCB10CLK	X ⁽²⁾	0	1
		N/A	0		
		UVSS	1	1	0
		C1.4(4M)	X	1	1
P6.4(UCB18MDUCLB18UA)	4	P6.4 (0x0)	1 (0, 0: 1)	0	0
		UCB18MDUCLB18UA	X ⁽²⁾	0	1
		N/A	0		
		UVSS	1	1	0
		C1.2(4M)	X	1	1
P6.5(UCB180VBUCLB180L)	5	P6.5 (0x0)	1 (0, 0: 1)	0	0
		UCB180VBUCLB180L	X ⁽²⁾	0	1
		N/A	0		
		UVSS	1	1	0
		C1.2(4M)	X	1	1

(1) X = don't care

(2) Not available on the 64-pin TQFP package

(3) Direction controlled by the SCL04 module

(4) Setting PESEL1.x and PESEL0.x disables the output driver and the input Schmitt trigger to prevent possible cross currents when applying analog signals

(5) Setting the CH12G bit in the comparator disables the output driver and the input Schmitt trigger to prevent cross currents when applying analog signals. Selecting the C1.4 input pin to the comparator multiplexer with the CEPSSEL or CEINSEL bits automatically disables the output driver and input buffer for that pin, regardless of the state of the associated UCB180VBUCLB180L

6.12.16 Port P6 (P6.6 and P6.7) Input/Output With Schmitt Trigger

Figure 6-12 shows the port diagram. Table 8-77 summarizes the selection of the pin functions.

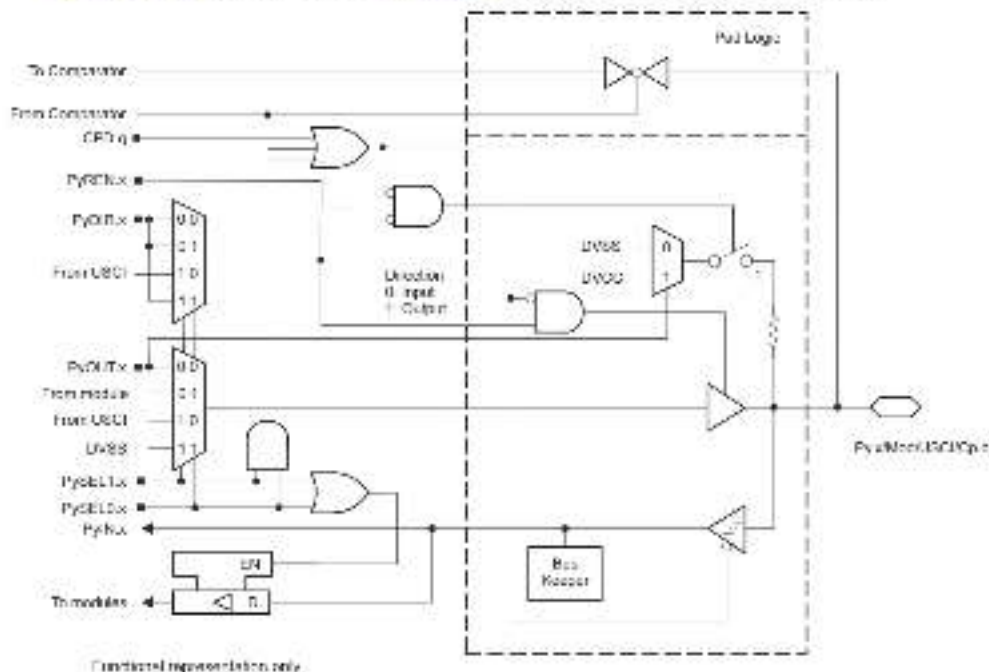


Figure 6-12. Py.x/Mod/USCI/Cp.q Pin Diagram

Table 6-77. Port P6 (P6.6 and P6.7) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P6DIR.x	P6SEL1.x	P6SEL2.x
P6.6 (P6.6) (P6.6) (P6.6)	6	P6.6 (VCC)	1 (0, 0: 1)	0	0
		P6.6 (VCC)	0	0	1
		TA2.7	1	0	0
		UCB0000000000000000	x ⁽²⁾	1	0
		Q1.1 (VCC)	x	1	1
P6.7 (P6.7) (P6.7) (P6.7)	7	P6.7 (VCC)	1 (0, 0: 1)	0	0
		TA2.8 (VCC)	0	0	1
		TA2.8	1	0	0
		UCB0000000000000000	x ⁽²⁾	1	0
		Q1.0 (VCC)	x	1	1

(1) X = don't care.

(2) Direction controlled by UCB0000000000000000.

(3) Setting P6SEL1.x and P6SEL2.x disables the output driver and the input Schmitt trigger to prevent possible cross currents when applying a logic signal.

(4) Setting the CEPS0 bit of the comparator disables the output driver and the input Schmitt trigger to prevent possible cross currents when applying a logic signal. Selecting the CEPS0 input pin to the comparator multiplexer with the CEPS0 bit in CEPS0H1, then automatically enables the output driver and input buffer for that pin, regardless of the state of the associated CEPS0 bit.

Figure 8-13 shows the port diagram. Table 8-78 summarizes the selection of the pin functions.



Table 6-78. Port P8 (P8.0 and P8.1) Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P8DIR.x	P8SEL1.x	P8SEL2.x
P8.0(UCC2STAT/TA1/IOC0.1)	0	IN0.0 (V _{CC})	1 (0, 0: 1)	0	0
		UCB0S1B	x ⁽²⁾	0	1
		TA1.CC0A	0		
		TA1.0	1	1	0
		OC0.0SR	X	1	1
P8.1(UCC0CLK/TA2/IOC0.0)	1	PW1.0 (V _{CC})	1 (0, 0: 1)	0	0
		UCB0CLK	x ⁽²⁾	0	1
		TA2.CC0A	0		
		TA2.0	1	1	0
		OC0.0SR	X	1	1

(1) X = don't care.

(2) Direction controlled by UCB0L_B0 module.

(3) Setting P8SEL1.x and P8SEL2.x disables the output driver and the input Schmitt trigger to prevent possible cross currents when applying a logic signal.

(4) Setting the CERP0 bit of the non-comparator disables the output driver and the input Schmitt trigger to prevent possible cross currents when applying a logic signal. Selecting the C0 input pin to the comparator multiplexer with the C0 input pin C0SEL0.0x, automatically enables the output driver and input buffer for that pin, regardless of the state of the associated CERP0 bit.

6.12.18 Port P10 (P10.4 and P10.5) Input/Output With Schmitt Trigger

Figure 6-14 shows the port diagram. Table 6-79 summarizes the selection of the pin functions.

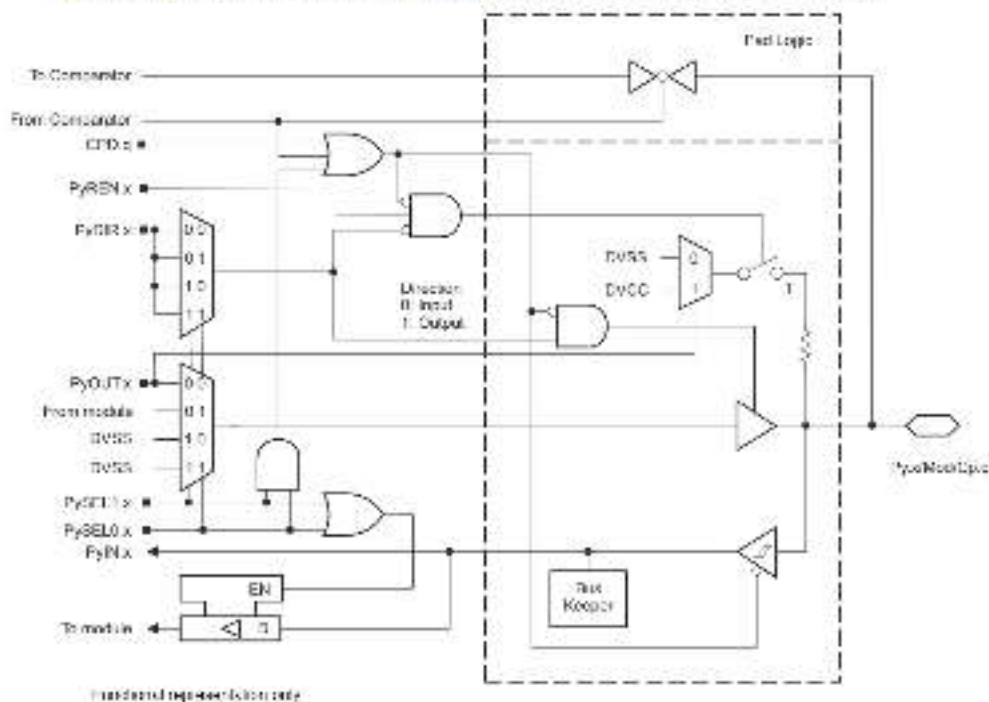


Figure 6-14. Py.x/Mod/Cp.q Pin Diagram

Table 6-79. Port P10 (P10.4 and P10.5) Pin Functions

PIN NAME (P10.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P10DIR.x	P10SEL1.x	P10SEL0.x
P10.4 (TA10T0.4) ⁽²⁾	4	P10.4 (IO)	1, 0, 0, 1	0	0
		WAKEUP	0	0	1
		TA10.0	1		
		N/A	0	1	0
		OVSS	1		
		COMP1OUT	X		
P10.5 (TA10T0.5) ⁽²⁾	5	P10.5 (IO)	1, 0, 0, 1	0	0
		TA10.0CHA	0	0	1
		WAKE	1		
		N/A	0	1	0
		OVSS	1		
		COMP1OUT	X		

(1) X = don't care.

(2) Not available on MSP432P401R and MSP432P401M packages.

(3) Setting P10SEL1.x and P10SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when switching analog signals.

(4) Setting the CERP0 bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying periodic signals. Selecting the C0 input pin to the comparator multiplexer with the C0SEL1 or C0SEL0 bits simultaneously disables the output driver and input buffer for that pin, regardless of the state of the associated C0SEL bit.

6.12.19 Port P7 (P7.4 to P7.7) Input/Output With Schmitt Trigger

Figure 6-15 shows the port diagram. Table 8-80 summarizes the selection of the pin functions.

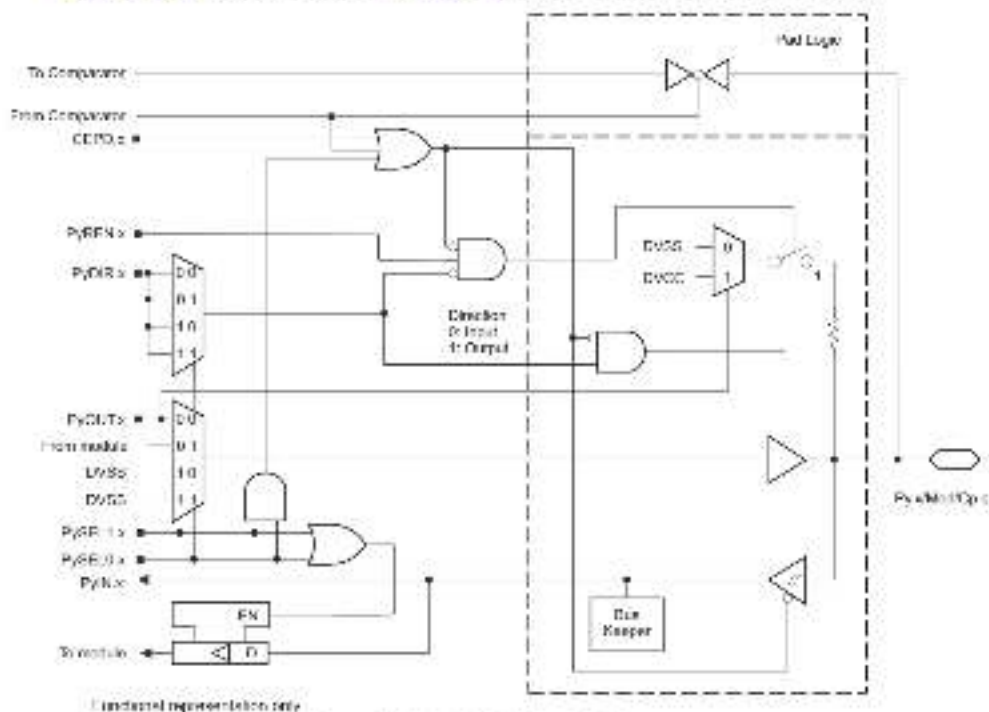


Figure 6-15. Py.xModiCp.q Pin Diagram

Table 6-80. Port P7 (P7.4 to P7.7) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
			P7DIR.x	P7SEL1.x	P7SEL0.x	P7MAP.x
P7.4(PM, IAT.0)5 ⁽²⁾	4	P7.4(0)	I/O, O ⁽³⁾	0	0	X
		IAT.0(3A)	0	0	1	default
		TAI.1	1			
		N/A	0			
		DVSS	1	1	0	X
P7.5(PM, IAT.3)0,4 ⁽²⁾	5	CO.0(3A)	X	1	1	X
		P7.5(0)	I/O, O ⁽³⁾	0	0	X
		TAI.0(3A)	0			
		IAT.3	1	0	1	default
		N/A	0			
P7.6(PM, TAI.2)0,3 ⁽²⁾	6	DVSS	1	1	0	X
		CO.0(3A)	X	1	1	X
		P7.6(0)	I/O, O ⁽³⁾	0	0	X
		IAT.0(3A)	0			
		TAI.2	1	0	1	default
P7.7(PM, IAT.0)3 ⁽²⁾	7	N/A	0			
		DVSS	1	1	0	X
		CO.0(3A)	X	1	1	X
		P7.7(0)	I/O, O ⁽³⁾	0	0	X
		TAI.0(3A)	0			
P7.7(PM, IAT.0)3 ⁽²⁾	7	IAT.1	1	0	1	default
		N/A	0			
		DVSS	1	1	0	X
		CO.0(3A)	X	1	1	X
		P7.7(0)	I/O, O ⁽³⁾	0	0	X

(1) X = configurable

(2) Not available on the 64-pin MSP432 package

(3) Setting P7SEL1.x and P7SEL0.x disables the output driver and the input buffer, to prevent parasitic cross currents when applying analog signals

(4) Setting the CEMSEL bit of the comparator disables the output driver and the input buffer, to prevent parasitic cross currents when applying analog signals. Selecting the CEMSEL bit to the comparator multiplies with the CEMSEL or CEMSEL bit, so internally disables the output driver and input buffer for that pin, regardless of the value of the associated CEMSEL bit

Figure 8-16 and Figure 8-17 show the port diagram. Table 8-81 summarizes the selection of the pin functions.



Figure 5-16. Port PJ (PJ.0) Diagram

Table 6-81. Port PJ (PJ.0 and PJ.1) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾					LFX1 BYPASS
			PJDIR.x	PJSEL1.1	PJSEL0.1	PJSEL1.0	PJSEL0.0	
PJ.0S+XIN	0	PJ.0 (IO)	0, 0, 0, 1	X	X	0	0	X
		NA	0	X	X	1	X	X
		IOVSS	1					
		LFX1N crystal mode ⁽²⁾	X	X	X	0	1	0
		LFX1N bypass mode ⁽²⁾	X	X	X	0	1	1
PJ.1S+XOUT	1	PJ.1 (IO)	0, 0, 0, 1	0	0	0	0	0
						1	X	
						X	X	IO
		NA	0	see ⁽³⁾	see ⁽³⁾	0	0	0
						1	X	
						X	X	1 ⁽⁴⁾
		IOVSS	1	see ⁽³⁾	see ⁽³⁾	0	0	0
						1	X	
						X	X	1 ⁽⁴⁾
		LFX1N crystal mode ⁽²⁾	X	X	X	0	1	0

(1) X = 00011100

(2) Selecting PJSEL1.0 = 0 and PJSEL0.0 = 1 causes the general-purpose IO to be disabled. When LFX1N/BYPASS = 0, PJ.0 and PJ.1 are configured for crystal operation and PJSEL1.1 and PJSEL0.1 are don't care. When LFX1N/BYPASS = 1, PJ.0 is configured for bypass operation and PJ.1 is configured as general-purpose IO.

(3) When PJ.0 is configured in bypass mode, PJ.1 is configured as general-purpose IO.

(4) With PJSEL0.1 = 1 or PJSEL1.1 = 1, the general-purpose IO functionality is disabled. No input function is available. When configured as output, the pin is always pulled down.

6.12.21 Port PJ (PJ.2 and PJ.3) Input/Output With Schmitt Trigger

Figure 6-18 and Figure 6-19 show the port diagrams. Table 6-82 summarizes the selection of the pin functions.

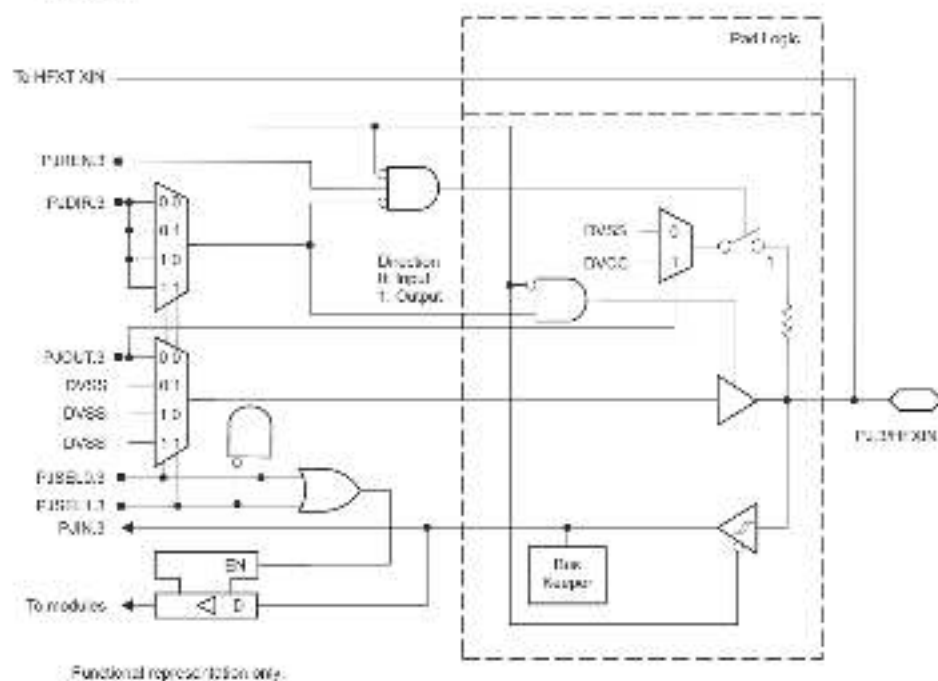


Figure 6-18. Port PJ (PJ.2) Diagram

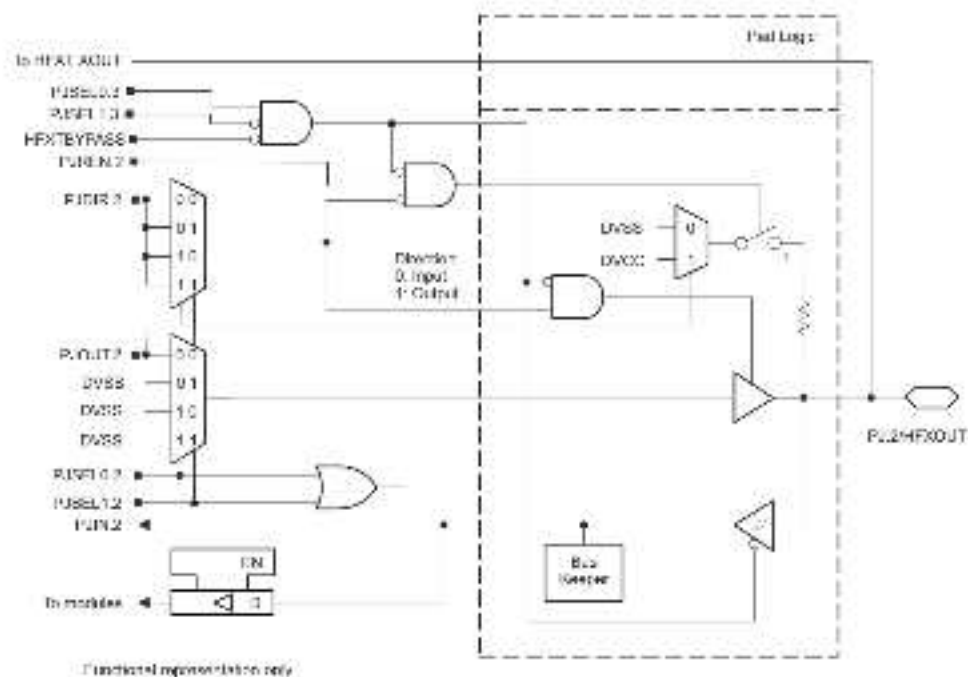


Figure 6-19. Port PJ (PJ.3) Diagram

Table 6-82. Port PJ (PJ.2 and PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾					HFX1 BYPASS
			PJDIR.x	PJSEL1.2	PJSEL0.2	PJSEL1.3	PJSEL0.3	
PJ.2H+XIN	3	PJ.2 (I/O)	0, 0, 0, 1	X	X	0	0	X
		NA	0	X	X	1	X	X
		Unuse	1					
		HFX1 crystal mode ⁽²⁾	X	X	X	0	1	0
		LF XIN bypass mode ⁽³⁾	X	X	X	0	1	1
PJ.2H+XOUT	2	PJ.2 (I/O)	0, 0, 0, 1	0	0	0	0	0
						1	X	0
						X	X	1 ⁽⁴⁾
		NA	0	non ⁽⁴⁾	non ⁽⁴⁾	0	0	0
						1	X	0
						X	X	1 ⁽⁴⁾
		Unuse	1	non ⁽⁴⁾	non ⁽⁴⁾	0	0	0
						1	X	0
						X	X	1 ⁽⁴⁾
		LF XIN crystal mode ⁽³⁾	X	X	X	0	1	0

(1) X = 000 000

(2) Selecting PJSEL1.1, 1, 1 = 0 and PJSEL0.1 = 1 causes the general-purpose I/O to be disabled. When HFX1BYPASS = 0, PJ.2 and PJ.3 are configured for crystal operation and PJSEL1.2 and PJSEL0.2 are don't care. When HFX1BYPASS = 1, PJ.3 is configured for bypass operation and PJ.2 is configured as general-purpose I/O.

(3) When PJ.3 is configured in bypass mode, PJ.2 is configured as general-purpose I/O.

(4) With PJSEL0.2 = 1 or PJSEL1.2 = 1, the general-purpose I/O functionality is disabled. No input function is available. When configured as output, the pin is always pulled down.

6.12.22 Port PJ (PJ.4 and PJ.5) Input/Output With Schmitt Trigger

Table 6-83 summarizes the selection of the pin functions.

Table 6-83. Port PJ (PJ.4 to PJ.5) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			SWJ MODE OF OPERATION ⁽¹⁾
			PJDIR.x	PJSEL1.x	PJSEL0.x	
PJ.4(TDI) ⁽²⁾	4	PJ.4(BC)	1 (0/1) ⁽³⁾	0	0	X
		TDI	X	0	1	JTAG (4 wires)
		DVDD	X	0	1	SWD (2 wires)
		DVSS	X	1	X	X
PJ.5(DVSSW) ⁽²⁾	5	PJ.5(BC)	1 (0/1) ⁽³⁾	0	0	X
		DVSS	X	0	1	JTAG (4 wires)
		SWD	X	0	1	SWD (2 wires)
		TRST	X	1	X	X

(1) X indicates that the value of the control signal or mode of operation may be either set or the function is disabled.

(2) This pin is internally pulled up to DVDD (0 = X, 1 = 1).

(3) When used in debug configuration, this pin must be pulled to ground through an external pull-down resistor.

6.12.23 Ports SWCLKTCK and SWDIOTMS With Schmitt Trigger

Table 6-84 summarizes the selection of the pin functions.

Table 6-84. Ports SWCLKTCK and SWDIOTMS Pin Functions

PIN NAME	FUNCTION	SWJ MODE OF OPERATION
SWCLKTCK ⁽¹⁾	TCK (input)	JTAG (4 wires)
	SWCLK (input)	SWD (2 wires)
SWDIOTMS ⁽²⁾	TMS (input)	JTAG (4 wires)
	SWDIO(BC)	SWD (2 wires)

(1) This pin is internally pulled to DVDD.

(2) This pin is internally pulled to DVDD.

6.13 Device Descriptors (TLV)

Table 6-85 summarizes the Device IDs of the MSP432P401x MCUs. Table 6-86 lists the contents of the device descriptor (TLV) structure for the MSP432P401x MCUs.

Table 6-85. Device IDs

DEVICE	DEVICE ID
MSP432P401R1Z	00000001h
MSP432P401M1PZ	00000001h
MSP432P401M1PZ-XH	00000001h
MSP432P401M1PZRH	00000001h
MSP432P401M1PZRC	00000001h
MSP432P401M1PZRC	00000001h

Table 6-86. Device Descriptor Table⁽¹⁾

	DESCRIPTION	ADDRESS	VALUE
Info Block	Device Info Tag	00010001h	per unit
	Device Info Length	00010001h	00000001h
	Device ID	00000001h	See Table 6-85
	Manufacturer Revision	00010001h	per unit
	Part Code Revision	00010001h	per unit
	ROM Error Library Revision	00010001h	per unit
	Die Record Tag	00000001h	00000001h
Die Record	Die Record Length	00010001h	00000001h
	Die X Position	00010001h	per unit
	Die Y Position	00010001h	per unit
	Wafer ID	00000001h	per unit
	Lot ID	00010001h	per unit
	Reserved	00010001h	per unit
	Reserved	00010001h	per unit
	Reserved	00000001h	per unit
	Test Results	00010001h	per unit
	Device System Calibration Tag	00010001h	00000001h
	Device System Calibration Length	00010001h	00000001h
	DCO-R Mode Frequency calibration for DCO-RSEL 0 to 4	00000001h	per unit
	DCO-R Mode Frequency calibration for DCO-RSEL 5	00010001h	per unit
	Reserved	00010001h	not defined
	Reserved	00010001h	not defined
	Reserved	00000001h	not defined
	Reserved	00010001h	not defined
Device System Calibration	DCO-R Mode DCO Current (I _{DCO}) for DCO-RSEL 0 to 4	00010001h	per unit
	DCO-R Mode DCO Current (I _{DCO}) for DCO-RSEL 5	00010001h	per unit
	DCO-R Mode Frequency calibration for DCO-RSEL 0 to 4	00000001h	per unit
	DCO-R Mode Frequency calibration for DCO-RSEL 5	00010001h	per unit
	Reserved	00010001h	not defined
	Reserved	00010001h	not defined
	Reserved	00000001h	not defined
	Reserved	00010001h	not defined
	DCO-R Mode DCO Current (I _{DCO}) for DCO-RSEL 0 to 4	00010001h	per unit
	DCO-R Mode DCO Current (I _{DCO}) for DCO-RSEL 5	00010001h	per unit

(1) – per unit = contents valid for this device to device.

Table 8-86. Device Descriptor Table⁽¹⁾ (continued)

DESCRIPTION	ADDRESS	VALUE
ADC14 Calibration	ADC14 Calibration Tag	00000000h
	ADC14 Calibration Length	00000000h
	Reserved	00000000h
	Reserved	00000000h
	Reserved	00000000h
	Reserved	00000000h
	Reserved	00000000h
	Reserved	00000000h
	Reserved	00000000h
	Reserved	00000000h
	Reserved	00000000h
	Reserved	00000000h
	Reserved	00000000h
	Reserved	00000000h
	Reserved	00000000h
	Reserved	00000000h
	Reserved	00000000h
	Reserved	00000000h
	Reserved	00000000h
	Reserved	00000000h
	Reserved	00000000h
Flash Calibration	ADC11.5-V Reference Temperature Sensor 30°C	per unit
	ADC11.5-V Reference Temperature Sensor 60°C	per unit
	ADC11.5-V Reference Temperature Sensor 90°C	per unit
	ADC11.5-V Reference Temperature Sensor 120°C	per unit
	ADC11.5-V Reference Temperature Sensor 150°C	per unit
	ADC11.5-V Reference Temperature Sensor 180°C	per unit
	ADC11.5-V Reference Temperature Sensor 210°C	per unit
	ADC11.5-V Reference Temperature Sensor 240°C	per unit
	ADC11.5-V Reference Temperature Sensor 270°C	per unit
	ADC11.5-V Reference Temperature Sensor 300°C	per unit
Flash Info	Flash Calibration Tag	00000000h
	Flash Calibration Length	00000000h
	Reserved	not defined
	Reserved	not defined
	Flash Info Tag	00000000h
	Flash Info Length	00000000h
	Flash Memory Programming Failure	00000000h
	Flash Memory Erase Failure	00000000h
	128-Bit Random Number Tag	00000000h
	Random Number Length	00000000h
Random Number	Reserved	per unit
	128-Bit Random Number ⁽²⁾	per unit
	Reserved	per unit
	Reserved	per unit
	Reserved	per unit
RTC Configuration	RTC Configuration Tag	00000000h
	RTC Configuration Length	00000000h
	RTC Periodic Interrupt Schedule	00000000h
	RTC Periodic Interrupt Configuration for L490	00000000h
	RTC Periodic Interrupt Configuration for L491	00000000h
	RTC Periodic Interrupt Configuration for L492	00000000h
T1V Prod	T1V Test Word	00000000h
	Reserved	00000000h

(2) 128-Bit Random Number: The random number is generated during production test using the CryptGenRandom() function from Windows®.

6.14 Identification

6.14.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to the errata sheets for the devices in this data sheet, see [Section 8.4](#).

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the Hardware Revision entry in the Device Descriptor structure (see [Section 6.13](#)).

6.14.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to the errata sheets for the devices in this data sheet, see [Section 8.4](#).

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the Device ID entry in the Device Descriptor structure (see [Section 6.13](#)).

6.14.3 ARM Cortex-M4F ROM Table Based Part Number

The MSP432P4xx family of MCUs incorporates a part number for the device for the IDEs to recognize the device, in addition to the device IDs specified in the device descriptors (TLV). This section describes how this information is organized on the device.

IEEE 1149.1 defines the use of a JIDCODE register in the JTAG chain to provide the fields in [Table 6-87](#).

Table 6-87. Structure of Device Identification Code

Bit Position	Field Description
31:28	Version
27:12	Part Number of the device
11:1	Manufacturer Identity
0	Reserved (Mapped to 1)

On MSP432P4xx MCUs, all these fields are implemented on the ARM Cortex-M4 ROM table. The part number can be read by the IDE tools (TI internal or third party) to determine the device. [Figure 6-20](#) shows the Peripheral ID register bit descriptions from the ARM Cortex-M4 specifications. See the *ARM Debug Interface V5 Architecture Specification* for bit-level details on the ARM Cortex-M4 Peripheral ID registers.

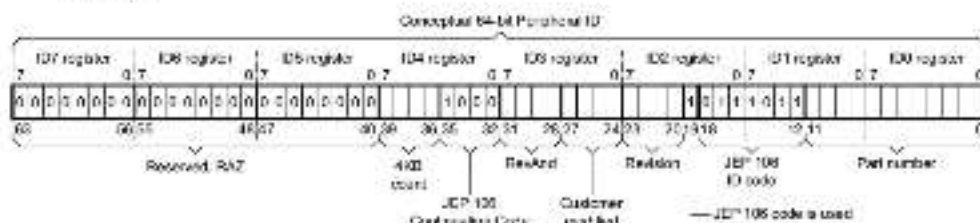


Figure 6-20. ARM Cortex-M4 Peripheral ID Register Description

[Figure 6-20](#) shows that a one-to-one mapping is not possible for the following fields from [Table 6-97](#):

1. Version: IEEE 1149.1 defines a 4-bit field where as the CoreSight compliant PID registers have 4 bits each for Revision (major revision) and RevAnd (minor revision).

2. Part Number: IEEE 1149.1 defines a 16-bit entity. However, the PID registers in the ROM table have only 12 bits reserved for this purpose (Part number – PID1 and PID0 registers).

For the MSP432P4xx MCUs, the Revision and RevAnd fields are used for tracking the major and minor revisions. Also, the Customer modified (4-bit) field is used for extending the Part number to 16 bits, to accommodate all of the fields needed by IEEE 1149.1 in the ROM table.

As an example, the ROM table with IEEE 1149.1 compliant device ID00DC for the MSP432P401xx MCU is 0000-1011-1001-1010-1111-0000-0010-1111 (see Figure 6-21).

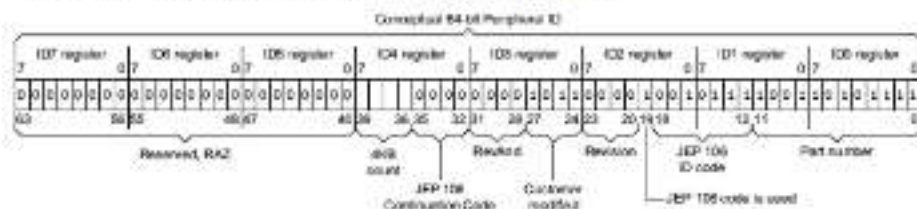


Figure 6-21. Example of ROM PID Entries for MSP432P401xx MCU

7 Applications, Implementation, and Layout

NOTE

Information in this following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. The customer is responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Device Connection and Layout Fundamentals

This section discusses the recommended guidelines when designing with the MSP432 microcontrollers. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

7.1.1 Power Supply Decoupling and Bulk Capacitors

TI recommends connecting a combination of a 4.7- μ F plus a 100-nF low-ESR ceramic decoupling capacitor to each AVCC and DVCC pin (see Figure 7-1). Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters). Additionally, TI recommends separated grounds with a single point connection for better noise isolation from signal-to-analog circuits on the board and for high analog accuracy.

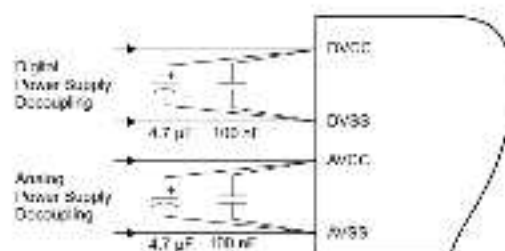


Figure 7-1. Power Supply Decoupling

7.1.2 External Oscillator

The device supports a low frequency crystal (32.768 kHz) on the LFXT pins and a high frequency crystal on the HFXT pins. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the LFXIN and HFXIN input pins that meet the specifications of the respective oscillator if the appropriate LFXTBYPASS or HFXTBYPASS mode is selected. In this case, the associated LFXOUT and HFXOUT pins can be used for other purposes.

Figure 7-2 shows a typical connection diagram.

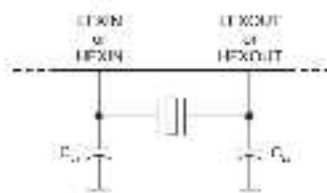


Figure 7-2. Typical Crystal Connection

See [MSP430 32kHz Crystal Oscillators](#) for more information on selecting, testing, and designing a crystal oscillator with the MSP432 devices.

7.1.3 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See [MSP430 32kHz Crystal Oscillators](#) for recommended layout guidelines.
- Proper bypass capacitors on DVCC, AVCC, and reference pins if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or UART signals away from the oscillator circuit.
- See [Circuit Board Layout Techniques](#) for a detailed discussion on printed-circuit-board (PCB) layout considerations. This document is written primarily about op amps, but the guidelines are generally applicable for all mixed-signal applications.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See [MSP430 System-Level ESD Considerations](#) for guidelines.

7.1.4 Do's and Don'ts

TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in *Absolute Maximum Ratings*. Exceeding the specified limits may cause malfunction of the device.

7.2 Peripheral and Interface-Specific Design Information

7.2.1 ADC14 Peripheral

7.2.1.1 Partial Schematic

Figure 7-3 shows a partial schematic of the ADC14 external connections.

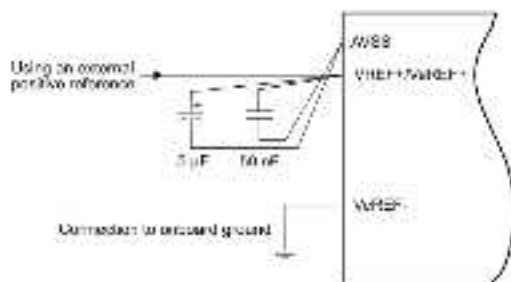


Figure 7-3. ADC14 Grounding and Noise Considerations

7.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate PCB layout and grounding techniques should be followed to minimize ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in [Section 7.1.3](#) combined with the connections shown in [Section 7.2.1.1](#) prevent this.

In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. A noise-free design using separate analog and digital ground planes with a single-point connection is recommended to achieve high accuracy.

Figure 7-8 shows the recommended decoupling circuit when an external voltage reference is used.

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 5- μ F capacitor is used to buffer the reference pin and filter any low-frequency ripple. A 50-nF bypass capacitor is used to filter out any high-frequency noise.

7.2.1.3 Layout Guidelines

Components that are shown in the partial schematic (see Figure 7-3) should be placed as close as possible to the respective device pins. Avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

If differential mode is used for the ADC14, the analog differential input signals must be routed close together to minimize the effect of noise on the resulting signal.

8 Device and Documentation Support

8.1 Getting Started and Next Steps

For more information on the MSP432 family of microcontrollers and the tools and libraries that are available to help with your development, visit [Getting Started with MSP432P4x](#).

8.2 Device and Development Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP432 MCU devices and support tools. Each MSP432 MCU commercial family member has one of three prefixes: MSP, PMS, or XMS (for example, MSP432P401R). TI recommends two of three possible prefix designators for its support tools: MSP and MSPX. These prefixes represent evolutionary stages of product development from engineering prototypes (with XMS for devices and MSPX for tools) through fully-qualified production devices and tools (with MSP for devices and MSP for tools).

Device development evolutionary flow:

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications.

PMS – First silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

MSP – Fully-qualified production device.

Support tool development evolutionary flow:

MSPX – Development-support product that has not yet completed Texas Instruments internal qualification testing.

MSP – Fully-qualified development-support product.

XMS and PMS devices and MSPX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices and MSP development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS and PMS) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate (EOL) is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, P2P) and temperature range (for example, T). [Figure 8-1](#) provides a legend for reading the complete device name for any family member.



Processor Family	MSP = Mixed-Signal Processor XMS = eXtreme Micro-System			
Platform	432 – TI's 32-Bit Low-Power Microcontroller Platform			
Series	P = Performance and Low-Power Series			
Feature Set	First Digit 4 – Flash-based devices up to 40 MB	Second Digit 0 – General purpose	Third Digit 1 – ADC14	Fourth Digit R – 256KB of Flash 512KB of SRAM M – 128KB of Flash 32KB of SRAM
Optional: Temperature Range	S = 0°C to 55°C I = -40°C to 85°C T = -40°C to 105°C			
Packaging	http://www.ti.com/package			
Optional: Distribution Format	T = Tape and Reel R = Large Reel No marking = Tube or Tray			
Optional: Additional Features	-E0 = Enhanced Product (-40°C to 105°C) -HT = Extended Temperature Range (-55°C to 150°C) -Q1 = Automotive Q100 Qualified			

Figure 8-1. Device Nomenclature

8.3 Tools and Software

All MSP microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at [TI 32-bit MSP432 microcontrollers](#).

Table 8-1 lists the supported debug features. See the *Code Composer Studio 6.1 for MSP432 User's Guide* for details on the available hardware features. See *Advanced Debugging Using the Enhanced Emulation Module (EEM) With Code Composer Studio Version 6* and *MSP432™ Advanced Power Optimizations: ULP Advisor™ and EnergyTrace™ Technology* for further usage information.

Table 8-1. Hardware Debug Features

FAMILY	JTAG	SWD	NUMBER OF BREAKPOINTS	ITM	DWT	FPB
MSP432P401x	Yes	Yes	4	Yes	Yes	Yes

EnergyTrace technology is supported with Code Composer Studio version 6.0 and newer. It requires specialized debugger circuitry, which is supported with the second-generation onboard eZ-FET flash emulation tool and second-generation stand-alone MSP-FET JTAG emulator. See *MSP432 Advanced Power Optimizations: ULP Advisor™ and EnergyTrace™ Technology*, the *Code Composer Studio 6.1 for MSP432 User's Guide*, and the *MSP432 Hardware Tools User's Guide* for more detailed information.

Design Kits and Evaluation Modules

100-Pin Target Development Board for MSP432P4x MCUs The MSP-TS432PZ100 is a stand-alone ZIF socket target board used to program and debug the MSP432 in-system through the JTAG interface or the Serial Wire Debug (SWD, 2-wire JTAG) protocol. This development board supports all MSP432P401x flash parts in a 100-pin LQFP package (TI package code: PZ).

MSP432P401R LaunchPad™ Development Kit The MSP432P401R LaunchPad development kit enables you to develop high-performance applications that benefit from low-power operation. The kit features the MSP432P401R MCU, which includes a 48-MHz ARM Cortex M4F, 55-µW/MHz active power, and 650 nA RTC operation, a 14-bit 1 MSPS differential SAR ADC, and an AES256 accelerator.

Software

MSP432P401x Code Examples C Code examples are available for every MSP device that configures each of the integrated peripherals for various application needs.

MSP432 Capacitive Touch Software Library Free libraries for enabling capacitive touch capabilities on MSP432 MCUs.

MSP EnergyTrace™ Technology EnergyTrace technology for MSP432 microcontrollers is an energy-based code analysis tool that measures and displays the application's energy profile and helps to optimize it for ultra-low-power consumption.

ULP (Ultra-Low Power) Advisor ULP (Ultra Low Power) Advisor is a tool for guiding developers to write more efficient code to fully utilize the unique ultra low power features of MSP and MSP432 microcontrollers. Aimed at both experienced and new microcontroller developers, ULP Advisor checks your code against a thorough ULP checklist to squeeze every last nano amp out of your application.

RTOS for MSP432 MSP432 MCUs offer compatibility with several TI and third party Real-Time Operating Systems (RTOS). Visit this link to learn about the key features of each to suit your design needs.

Ti-RTOS: Real-Time Operating System (RTOS) Ti-RTOS accelerates development schedules by eliminating the need to create basic system software functions from scratch. Ti-RTOS scales from a minimal footprint real-time multitasking kernel – Ti-RTOS Kernel (formerly known as SYSBIOS) – to a complete RTOS solution including protocol stacks, multicore communications, device drivers and power management. By providing essential system software components prebuilt and preintegrated, Ti-RTOS enables developers to focus on differentiating their application.

MSP Driver Library Driver Library's abstracted API keeps you above the bits and bytes of the MSP430 and MSP432 hardware by providing easy-to-use function calls. Thorough documentation is delivered through a helpful API Guide, which includes details on each function call and the recognized parameters. Developers can use Driver Library functions to write complete projects with minimal overhead.

MSP Graphics Library The MSP Graphics Library is a royalty-free set of graphics primitives for creating graphical user interfaces on MSP430 and MSP432 microcontroller-based boards that have a graphical display. The graphics library consists of two building layers of functionality: the display driver layer, specific to the display in use, and the graphics primitives layer, which draws points, lines, rectangles, circles, text, and bitmap images.

Digital Signal Processing Library The Texas Instruments™ Digital Signal Processing library is a set of highly optimized functions to perform many common signal processing operations on fixed-point numbers for MSP430™ and MSP432™ microcontrollers. This function set is typically utilized for applications where processing-intensive transforms are done in real-time for minimal energy and with very high accuracy. This library's optimal utilization of the MSP families' intrinsic hardware for fixed-point math allows for significant performance gains.

Development Tools

Code Composer Studio Integrated Development Environment for MSP Microcontrollers Code Composer Studio is an integrated development environment (IDE) that supports all MSP microcontroller devices. Code Composer Studio comprises a suite of embedded software utilities used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. For more information, see the *Code Composer Studio 5.1 for MSP432 User's Guide*.

ARM® Keil® MDK – Free 32KB IDE The ARM Keil MDK is a complete debugger and C/C++ compiler toolchain for building and debugging embedded applications. Keil MDK supports the low-power and high-performance MSP432 MCU family, and includes a fully integrated debugger for source and disassembly level debugging with support for complex code and data breakpoint. For more information, see the *ARM Keil MDK Version 5 for MSP432 User's Guide*.

IAR Embedded Workbench Kickstart IAR Embedded Workbench Kickstart for MSP is a complete debugger and C/C++ compiler toolchain for building and debugging embedded applications based on MSP430 and MSP432 microcontrollers. The code size limitation of C/C++ compiler is set to 8 KB for MSP430 devices and 32KB for MSP432 devices. For more information, see the *IAR Embedded Workbench for ARM 7.x for MSP432 User's Guide*.

Debuggers for MSP432 MSP432 MCUs are designed to work with a variety of debuggers from Texas Instruments and third-party vendors.

MSP MCU Programmer and Debugger The MSP-FET is a powerful emulation development tool – often called a debug probe – that allows users to quickly begin application development on MSP low-power microcontrollers.

MSP-GANG Production Programmer The MSP Gang Programmer is an MSP430 and MSP432 device programmer that can program up to eight identical MSP430 or MSP432 flash or FRAM devices at the same time. The MSP Gang Programmer connects to a host PC using a standard RS-232 or USB connection and provides flexible programming options that allow the user to fully customize the process.

Pin Mux Tool The Pin MUX Utility is a software tool that provides a graphical user interface for configuring pin multiplexing settings, resolving conflicts, and specifying I/O cell characteristics for 11 MPUs. Results are output as C header and code files that can be imported into software development kits or used to configure customer's custom software. Version 3 of the Pin Mux utility can automatically selecting a mux configuration that satisfies the requirements entered by the user.

8.4 Documentation Support

The following documents describe the MSP432P401x MCUs. Copies of these documents are available on the TI website.

Receiving Notification of Document Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on [ti.com](http://www.ti.com) (see [Section 8.5](#) for links to product folders). In the upper right corner, click the "Alert me!" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

Errata

MSP432P401R Device Erratasheet Describes the known exceptions to the functional specifications for each silicon revision of this device.

MSP432P401M Device Erratasheet Describes the known exceptions to the functional specifications for each silicon revision of this device.

User's Guides

MSP432P4xx Family Technical Reference Manual Detailed description of all modules and peripherals available in this device family.

Code Composer Studio 6.1 for MSP432 User's Guide This manual describes the use of the TI Code Composer Studio IDE (CCS) version 6.1 with the MSP432 low-power microcontrollers.

IAR Embedded Workbench for ARM 7.x for MSP432 User's Guide This manual describes the use of IAR Embedded Workbench for ARM (EWARM) version 7.x with the MSP432 low-power microcontrollers.

ARM Keil MDK Version 5 for MSP432 User's Guide This user's guide describes the use of the ARM Keil MDK version 5 with the MSP432 low-power microcontrollers.

GCC ARM Embedded Toolchain for MSP432 User's Guide This manual describes the setup and basic operation of the MSP432 programming and debug using GCC ARM compiler and the GDB debugger.

MSP432P401R Bootloader (BSL) User's Guide The MSP432 BSL enables users to communicate with embedded memory in the MSP432 microcontroller during the prototyping phase, final production, and in service. Both the programmable memory (flash memory) and the data memory (RAM) can be modified as required.

MSP432 Capacitive Touch Software Library Programmer's Guide MSP432 microcontrollers are equipped with the peripherals needed to perform a capacitance measurement. The purpose of the capacitive touch software library is to create a single interface that can be integrated with the peripheral set found in MSP432 devices. This document explains the capacitive touch library configuration and use with MSP432 devices.

Application Reports

MSP432 Platform Porting The goal for this porting guide is to help developers accurately assess the effort to port an existing application from one MSP platform to another, ultimately to derive a porting strategy with complete hardware and software coverage that properly ports the existing application without introducing bugs due to platform differences yet taking advantage of the unique features or performance improvements introduced in the new platform.

Designing an Ultra-Low-Power (ULP) Application With MSP432™ Microcontrollers With the growing system complexity in ultra-low-power microcontroller applications, minimizing the overall energy consumption is one of the most difficult problems to solve. Multiple aspects including silicon, other onboard hardware components, and application software must be considered. There are some obvious generic techniques that can be used to reduce energy consumption such as reducing operating voltage or frequency. Many of these generic techniques may not greatly reduce energy consumption independently, but taken as a whole, the results can be significant, as there are many interdependencies across these components.

Maximizing MSP432P4xx Voltage Regulator Efficiency This application report describes the relationship of the MSP432P4xx DC-DC and LDO, provides guidelines on choosing which is most efficient for your application, and gives board layout considerations for the DC-DC.

Leveraging Low-Frequency Power Modes on MSP432P4xx Microcontrollers Low power consumption is very important in all battery-powered embedded applications. But the operating frequency of these embedded applications can be diverse based on the needs of the application. Some applications might require operating at higher frequencies, in the order of several megahertz, while some other applications might require operating at lower frequencies, in the order of a few tens or a few hundreds of kilohertz. There are several microcontrollers in the market that offer good active mode power consumption when the operating frequency is in the order of several megahertz. But it is a challenge to get the power consumption low when the operating frequency is in the order of kilohertz. The low-frequency power modes available on the MSP432P4xx microcontrollers offer very low power consumption when low frequency of operation is used by the target application.

Software IP Protection on MSP432P4xx Microcontrollers Differentiation in embedded software applications enable differentiated products. Companies invest significant money in building differentiated software application. Hence, protecting this investment (application or portions of the application) is extremely important. This application note describes how to protect software intellectual property (IP) running on the Texas Instruments MSP432P401x family of microcontrollers.

Code Conversion Application for MSP432P401R This application note describes the use of the code conversion application delivered with version 2.0.0 (and above) of the MSP432P401R device header files. In these revisions of the MSP432P401R device header files, the coding style has been adapted to CMSIS. This may lead to compilation errors in user code if the code is not converted. MSP430 style register definitions have also been removed with exception of legacy 18-bit IPs (see msp432p401r.h classisht).

8.5 Related Links

Table 8-2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
MSP432P401R	Click here	Click here	Click here	Click here	Click here
MSP432P401M	Click here	Click here	Click here	Click here	Click here

8.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Community

TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki

Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.7 Trademarks

MSP432, MSP430, ULP, Advisor, EnergyTrace, LaunchPad, Texas Instruments, E2E are trademarks of Texas Instruments.

ARM, Cortex, Thumb, Keil are registered trademarks of ARM Ltd.

ULPBench, ULPMark are trademarks of EEMBC.

All other trademarks are the property of their respective owners.

8.8 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation practices may cause damage.

1. All personnel concerned with static-sensitive devices should be aware that even integrated circuits may be more susceptible to damage because very small quantities of charge could cause the device not to meet its published specifications.

8.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations; received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

8.10 Glossary

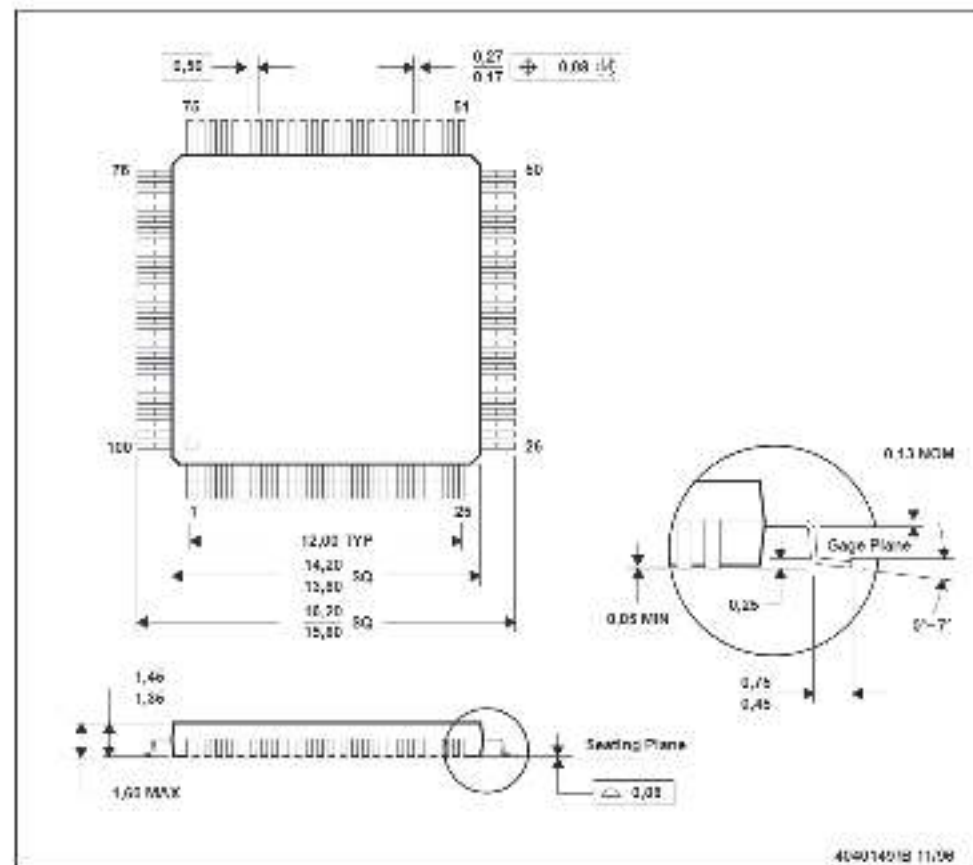
T Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PZ (S-PQFP-G100)

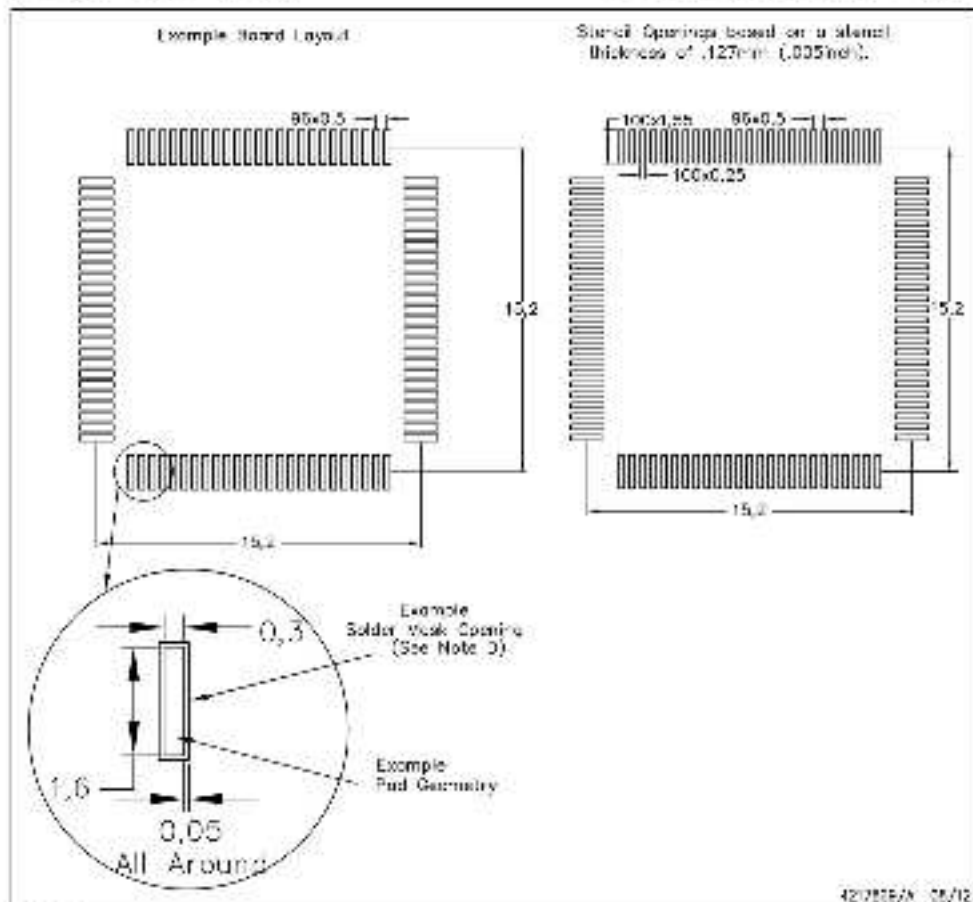
PLASTIC QUAD FLATPACK



- NOTES:
- Pin lead dimensions are in millimeters.
 - Pin dimensions are in inches.
 - Pin lead dimensions are in inches.

PZ (S-PQFP-G100)

PLASTIC QUAD FLAT PACK



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



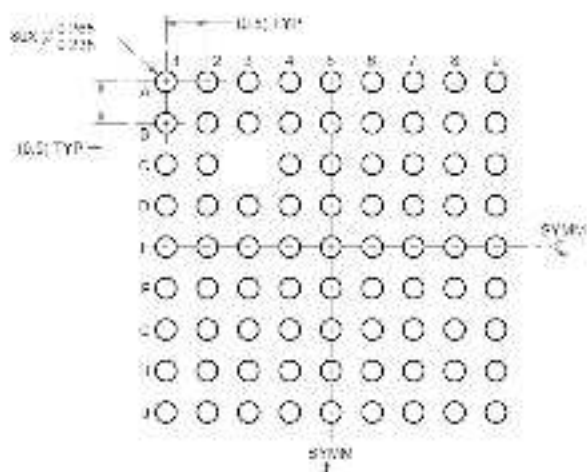
TABLE 1. Continued



1. All linear dimensions are in millimeters. Any dimensions in parentheses is for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This is a Ph-true order ball design.

ZXH0080A

DALL GREN ABBEY



LAND PATTERN EXAMPLE
SCALE 1:100



SOLDER MASK DETAILS
NO. 010411

422 EP'S & HENNING

NOTES continued

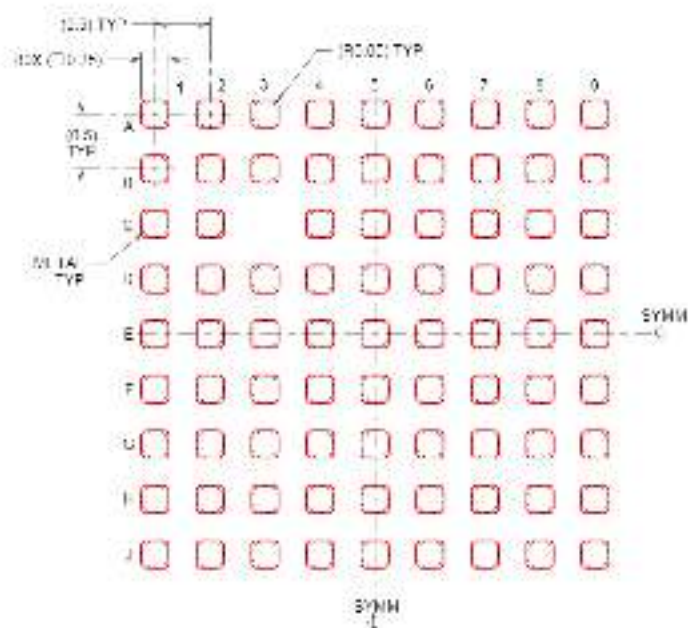
3. Final dimensions may vary due to manufacturing tolerances considerations and distributing constraints.
See <http://www.hubbell.com/hubbell/catalog/Products/Products%20List%20-%202017.pdf>

EXAMPLE STENCIL DESIGN

ZXH0080A

NFBGA - 1 mm max height

BALL GRID ARRAY



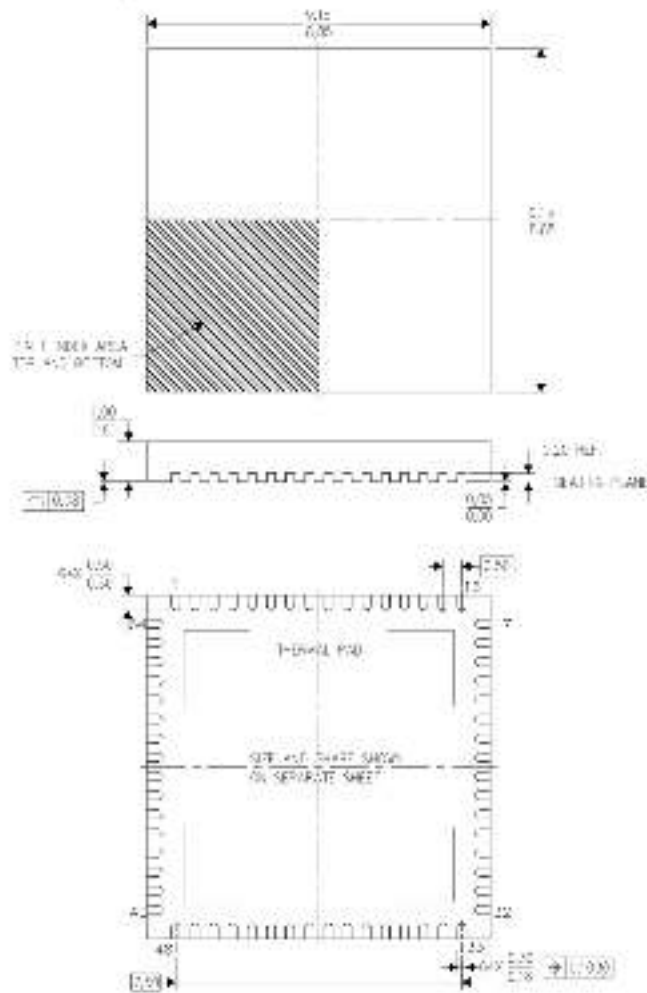
SOLDER PASTE EXAMPLE
 MAXIMUM 1mm EPOXY STENCIL
 (100% TYP)

402-00796-01/0001

NOTES: (continued)

4. Laser cutting operations with trapezoidal walls and rounded corners may offer better paste release.

R30(S-HVQFN-NS4) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO-LEAD



402408/ 11/01

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - The drawing is subject to change without notice.
 - Lead 1 clock, No leads (QFN) per-pin configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional notes in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

RGC (S-PVQFN-N64)

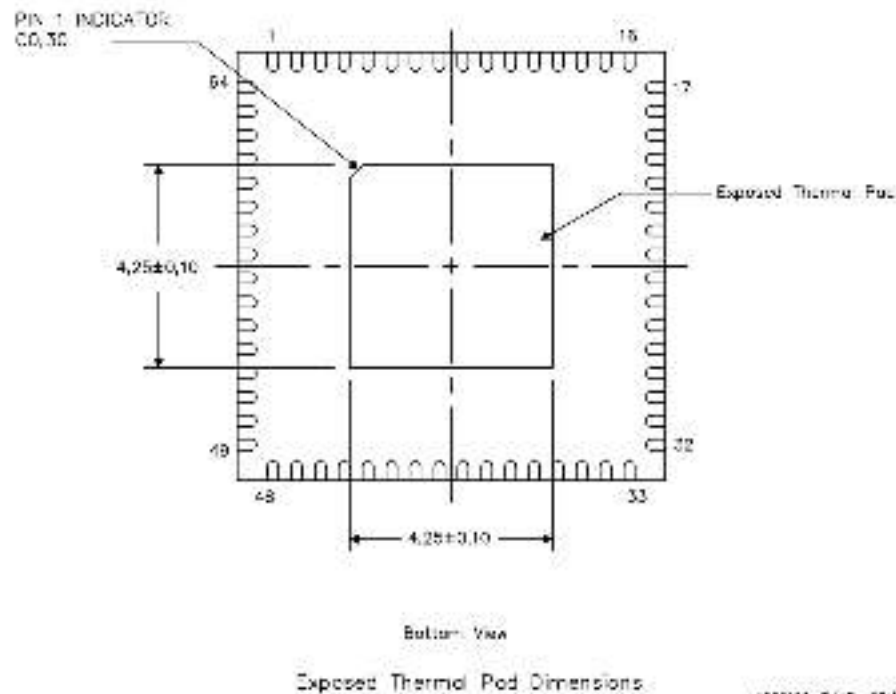
ELASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SQFN PCB Attachment, Texas Instruments Literature No. SLA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: A. All linear dimensions are in millimeters.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (3)	MSL, Peak Temp (4)	Op Temp (°C)	Device Marking (15)	Samples
MSP432P401MIF2	PREVIEW	LQFP	PZ	100	90	TBD	CuNiTi	CuNiTi	40 to 85	MSP432P401M	
MSP432P401MRZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br) (16)	CuNiPdAu	Level 3 2000 100 HR	40 to 85		
MSP432P401KIF00	PREVIEW	VQFN	R30	64	100	TBD	CuNiTi	CuNiTi	40 to 85		
MSP432P401MR50R	PREVIEW	VQFN	R30	64	2000	TBD	CuNiTi	CuNiTi	40 to 85		
MSP432P401MR50T	LIFE BUY (14)	VQFN	R30	64	250	(14)	CuNiTi	CuNiTi	40 to 85		
MS1432P401M2XH	(15)VIEW	NFBGA	ZAH	50	250	(16)	CuNiTi	CuNiTi	40 to 85		
MSP432P401M2XHR	PREVIEW	NFBGA	ZAH	50	2500	TBD	CuNiTi	CuNiTi	40 to 85		
MS1432P401M2XHT	(15)VIEW	NFBGA	ZAH	50	250	(16)	CuNiTi	CuNiTi	40 to 85		
MSP432P401RIF2R	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br) (16)	CuNiPdAu	Level 3 2000 100 HR	40 to 85	MSP432P401R	
MSP432P401RIF00	PREVIEW	VQFN	R30	64	100	TBD	CuNiTi	CuNiTi	40 to 85		
MSP432P401R50R	PREVIEW	VQFN	R30	64	2000	TBD	CuNiTi	CuNiTi	40 to 85		
MSP432P401R50T	PREVIEW	VQFN	R30	64	250	(14)	CuNiTi	CuNiTi	40 to 85		
MSP432P401R70T	LIFE BUY (14)	NFBGA	ZAH	50	250	(14)	CuNiTi	CuNiTi	40 to 85		
MS1432P401R2XHT	(15)VIEW	NFBGA	ZAH	50	2500	(16)	CuNiTi	CuNiTi	40 to 85		
MSP432P401R2XHT	PREVIEW	NFBGA	ZAH	50	250	TBD	CuNiTi	CuNiTi	40 to 85		
XM5432P401MRZR	PREVIEW	LQFP	PZ	100	1000	TBD	CuNiTi	CuNiTi	40 to 85		
XM5432P401RIF2R	PREVIEW	LQFP	PZ	100	1000	TBD	CuNiTi	CuNiTi	40 to 85		
XM5432P401R50T	PREVIEW	VQFN	R30	64	250	(14)	CuNiTi	CuNiTi	40 to 85		
XM5432P401R70T	LIFE BUY (14)	NFBGA	ZAH	50	1000	(14)	CuNiTi	CuNiTi	40 to 85		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a final buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan – The planned eco-friendly substitution: Pb-free (Pb (RoHS Exempt)), or Green (RoHS & no Sb/Br) – please check <http://www.ti.com/epd/interim> for the latest available information and additional product-related details.

TBD: The Pb-free (RoHS) compliant plan has not been defined.

Pb-Free (RoHS): Unless otherwise noted, all TI parts meet RoHS compliance and are compatible with the current, for US customers, lead (Pb)-free soldering and reflow processes, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-free products may contain a limited amount of lead to meet these high-temperature requirements.

Pb-Free (RoHS Compliant): These components have had Pb removed from the entire TI lead-based solderable surface, except between the device pins (leads or 2) located on the bottom side of the device. The reference used for these devices is the solderability of these components. For leaded TI components, see the leaded solderability test.

Green (RoHS & no Sb/Br): TI defines "Green" to mean halogen-free (Pb-free and antimony-free), and also bromine-free. TI defines "halogen-free" to mean the total halogen content (Br and Cl) does not exceed 0.1% by weight in homogeneous materials.

¹⁷ **MSL Peak Temp.** The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

¹⁸ There may be additional marking, which relates to the logo, Marking code information on the environmental category on the device.

¹⁹ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "+" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

²⁰ **Lead/Ball Profile:** Underline Devices may have multiple measured linear profiles. Profile spaces are separated by a vertical ruled line. Lead/Ball Profile values may wrap for two lines if the total value exceeds the maximum column width.

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