DDR2 SDRAM Mini-RDIMM

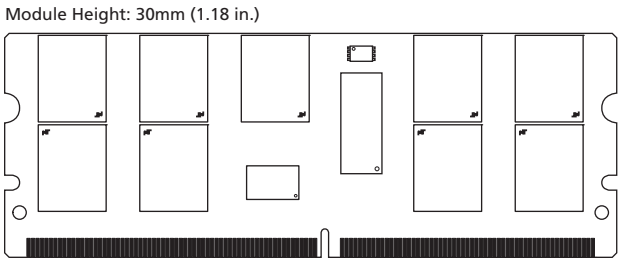
MT18HTF25672PKZ – 2GB

For component data sheets, refer to Micron's Web site: www.micron.com

Features

- 244-pin, mini registered dual in-line memory module (Mini-RDIMM)
- Fast data transfer rates: PC2-3200, PC2-4200, PC2-5300, or PC2-6400
- Supports ECC error detection and correction
- $V_{DD} = V_{DDQ} = +1.8V$
- $V_{DDSPD} = +1.7V$ to $+3.6V$
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Dual rank
- Multiple internal device banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8192-cycle refresh
- On-die termination (ODT)
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts
- Halogen-free

Figure 1: 244-Pin Mini-RDIMM (MO-244)



Options — Marking

- Operating temperature
  - Commercial ($0°C \le T_A \le +70°C$)
  - Industrial ($–40°C \le T_A \le +85°C$)[1,2] — I
- Parity — P
- Package
  - 244-pin Mini-RDIMM (halogen-free) — Z
- Frequency/CAS latency[3]
  - 2.5ns at CL = 5 (DDR2-800) — -80E
  - 2.5ns at CL = 6 (DDR2-800) — -800
  - 3.0ns at CL = 5 (DDR2-667) — -667

Notes: 1. Industrial temperature rating applies to DRAM only.
2. Contact Micron for product availability.
3. CL = CAS (READ) latency; registered mode will add one clock cycle to CL.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)				^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
		CL = 6	CL = 5	CL = 4	CL = 3			
-80E	PC2-6400	800	800	533	400	12.5	12.5	55
-800	PC2-6400	800	667	533	400	15	15	55
-667	PC2-5300	–	667	533	400	15	15	55
-53E	PC2-4200	–	–	533	400	15	15	55
-40E	PC2-3200	–	–	400	400	15	15	55

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2009 Micron Technology, Inc. All rights reserved.
Products and specifications discussed herein are subject to change by Micron without notice.

Table 2: Addressing

	2GB
Refresh count	8K
Row address	16K A[13:0]
Device bank address	8 BA[2:0]
Device configuration	1Gb (128 Meg x 8)
Column address	1K A[9:0]
Module rank address	2 S#[1:0]

Table 3: Part Numbers and Timing Parameters Not Used Modules

Base device: MT47H128M8,[1] 1Gb DDR2 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL - ^{t}RCD - ^{t}RP)
MT18HTF25672PK(I)Z-80E__	2GB	256 Meg x72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT18HTF25672PK(I)Z-800__	2GB	256 Meg x72	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT18HTF25672PK(I)Z-667__	2GB	256 Meg x72	5.3 GB/s	3.0ns/667MT/s	5-5-5

Notes: 1. The data sheets for the base devices can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT18HTF25672PKZ-667**G1**.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2009 Micron Technology, Inc. All rights reserved.

Pin Assignments and Descriptions

Table 4: Pin Assignments

244-Pin Mini-RDIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{REF}	32	V_{SS}	63	V_{DDQ}	94	DQS5#
2	V_{SS}	33	DQ24	64	A2	95	DQS5
3	DQ0	34	DQ25	65	V_{DD}	96	V_{SS}
4	DQ1	35	V_{SS}	66	V_{SS}	97	DQ42
5	V_{SS}	36	DQS3#	67	V_{SS}	98	DQ43
6	DQS0#	37	DQS3	68	Par_In	99	V_{SS}
7	DQS0	38	V_{SS}	69	V_{DD}	100	DQ48
8	V_{SS}	39	DQ26	70	A10/AP	101	DQ49
9	DQ2	40	DQ27	71	BA0	102	V_{SS}
10	DQ3	41	V_{SS}	72	V_{DD}	103	SA2
11	V_{SS}	42	CB0	73	WE#	104	NC
12	DQ8	43	CB1	74	V_{DDQ}	105	V_{SS}
13	DQ9	44	V_{SS}	75	CAS#	106	DQS6#
14	V_{SS}	45	DQS8#	76	V_{DDQ}	107	DQS6
15	DQS1#	46	DQS8	77	S1#	108	V_{SS}
16	DQS1	47	V_{SS}	78	ODT1	109	DQ50
17	V_{SS}	48	CB2	79	V_{DDQ}	110	DQ51
18	RESET#	49	CB3	80	NC	111	V_{SS}
19	NC	50	V_{SS}	81	V_{SS}	112	DQ56
20	V_{SS}	51	NC	82	DQ32	113	DQ57
21	DQ10	52	V_{DDQ}	83	DQ33	114	V_{SS}
22	DQ11	53	CKE0	84	V_{SS}	115	DQS7#
23	V_{SS}	54	V_{DD}	85	DQS4#	116	DQS7
24	DQ16	55	BA2	86	DQS4	117	V_{SS}
25	DQ17	56	Err_Out	87	V_{SS}	118	DQ58
26	V_{SS}	57	V_{DDQ}	88	DQ34	119	DQ59
27	DQS2#	58	A11	89	DQ35	120	V_{SS}
28	DQS2	59	A7	90	V_{SS}	121	SA0
29	V_{SS}	60	V_{DD}	91	DQ40	122	SA1
30	DQ18	61	A5	92	DQ41		
31	DQ19	62	A4	93	V_{SS}		

244-Pin Mini-RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
123	V_{SS}	154	DQ28	185	A3	216	NF/ RDQS5#
124	DQ4	155	DQ29	186	A1	217	V_{SS}
125	DQ5	156	V_{SS}	187	V_{DD}	218	DQ46
126	V_{SS}	157	DM3/ RDQS3	188	CK0	219	DQ47
127	DM0/ RDQS0	158	NF/ RDQS3#	189	CK0#	220	V_{SS}
128	NF/ RDQS0#	159	V_{SS}	190	V_{DD}	221	DQ52
129	V_{SS}	160	DQ30	191	A0	222	DQ53
130	DQ6	161	DQ31	192	BA1	223	V_{SS}
131	DQ7	162	V_{SS}	193	V_{DD}	224	NC
132	V_{SS}	163	CB4	194	RAS#	225	NC
133	DQ12	164	CB5	195	V_{DDQ}	226	V_{SS}
134	DQ13	165	V_{SS}	196	S0#	227	DM6/ RDQS6
135	V_{SS}	166	DM8/ RDQS8	197	V_{DDQ}	228	NF/ RDQS6#
136	DM1/ RDQS1	167	NF/ RDQS8#	198	ODT0	229	V_{SS}
137	NF/ RDQS1#	168	V_{SS}	199	A13	230	DQ54
138	V_{SS}	169	CB6	200	V_{DD}	231	DQ55
139	NF	170	CB7	201	NC	232	V_{SS}
140	NF	171	V_{SS}	202	V_{SS}	233	DQ60
141	V_{SS}	172	NC	203	DQ36	234	DQ61
142	DQ14	173	V_{DDQ}	204	DQ37	235	V_{SS}
143	DQ15	174	CKE1	205	V_{SS}	236	DM7/ RDQS7
144	V_{SS}	175	V_{DD}	206	DM4/ RDQS4	237	NF/ RDQS7#
145	DQ20	176	A15	207	NF/ RDQS4#	238	V_{SS}
146	DQ21	177	A14	208	V_{SS}	239	DQ62
147	V_{SS}	178	V_{DDQ}	209	DQ38	240	DQ63
148	DM2/ RDQS2	179	A12	210	DQ39	241	V_{SS}
149	NF/ RDQS2#	180	A9	211	V_{SS}	242	SDA
150	V_{SS}	181	V_{DD}	212	DQ44	243	SCL
151	DQ22	182	A8	213	DQ45	244	V_{DDSPD}
152	DQ23	183	A6	214	V_{SS}		
153	V_{SS}	184	V_{DDQ}	215	DM5/ RDQS5		

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2009 Micron Technology, Inc. All rights reserved.

Table 5: Pin Descriptions

Symbol	Type	Description
A[15:0]	Input (SSTL_18)	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA[2:0]) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. A[13:0] 2GB. A[15:14] are connected for parity.
BA[2:0]	Input (SSTL_18)	**Bank address inputs:** BA[2:0] define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR, EMR1, EMR2, and EMR3) is loaded during the LOAD MODE command.
CK0, CK0#	Input (SSTL_18)	**Clock:** CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKE[1:0]	Input (SSTL_18)	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DDR2 SDRAM.
DM[8:0] RDQS[8:0] RDQS#[8:0]	Input (SSTL_18)	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data, during a write access. DM is sampled on both edges of DQS. Although the DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins. If RDQS is disabled, RDQS[8:0] become DM[8:0] and RDQS#[8:0] are no function.
ODT[1:0]	Input (SSTL_18)	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR2 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	**Parity input:** Parity bit for the address, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input (SSTL_18)	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input	**Reset:** Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQ are High-Z.
S#[1:0]	Input (SSTL_18)	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA[2:0]	Input	**Serial address inputs:** These pins are used to configure the SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for SPD EEPROM:** SCL is used to synchronize communication to and from the SPD EEPROM.
CB[7:0]	I/O	Check bits.
DQ[63:0]	I/O (SSTL_18)	**Data input/output:** Bidirectional data bus.
DQS[8:0], DQS#[8:0]	I/O (SSTL_18)	**Data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
SDA	I/O	**Serial data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the SPD EEPROM on the module on the I^2C bus.
Err_Out	Output (open drain)	**Parity error output:** Parity error found on the command and address bus.
V_{DD}/V_{DDQ}	Supply	**Power supply:** 1.8V ±0.1V. The component V_{DD} and V_{DDQ} are connected to the module V_{DD}.
V_{DDSPD}	Supply	**SPD EEPROM power supply:** +1.7V to +3.6V.
V_{REF}	Supply	**Reference voltage:** $V_{DD}/2$.
V_{SS}	Supply	Ground.
NC	–	**No connect:** These pins are not connected on the module.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2009 Micron Technology, Inc. All rights reserved.

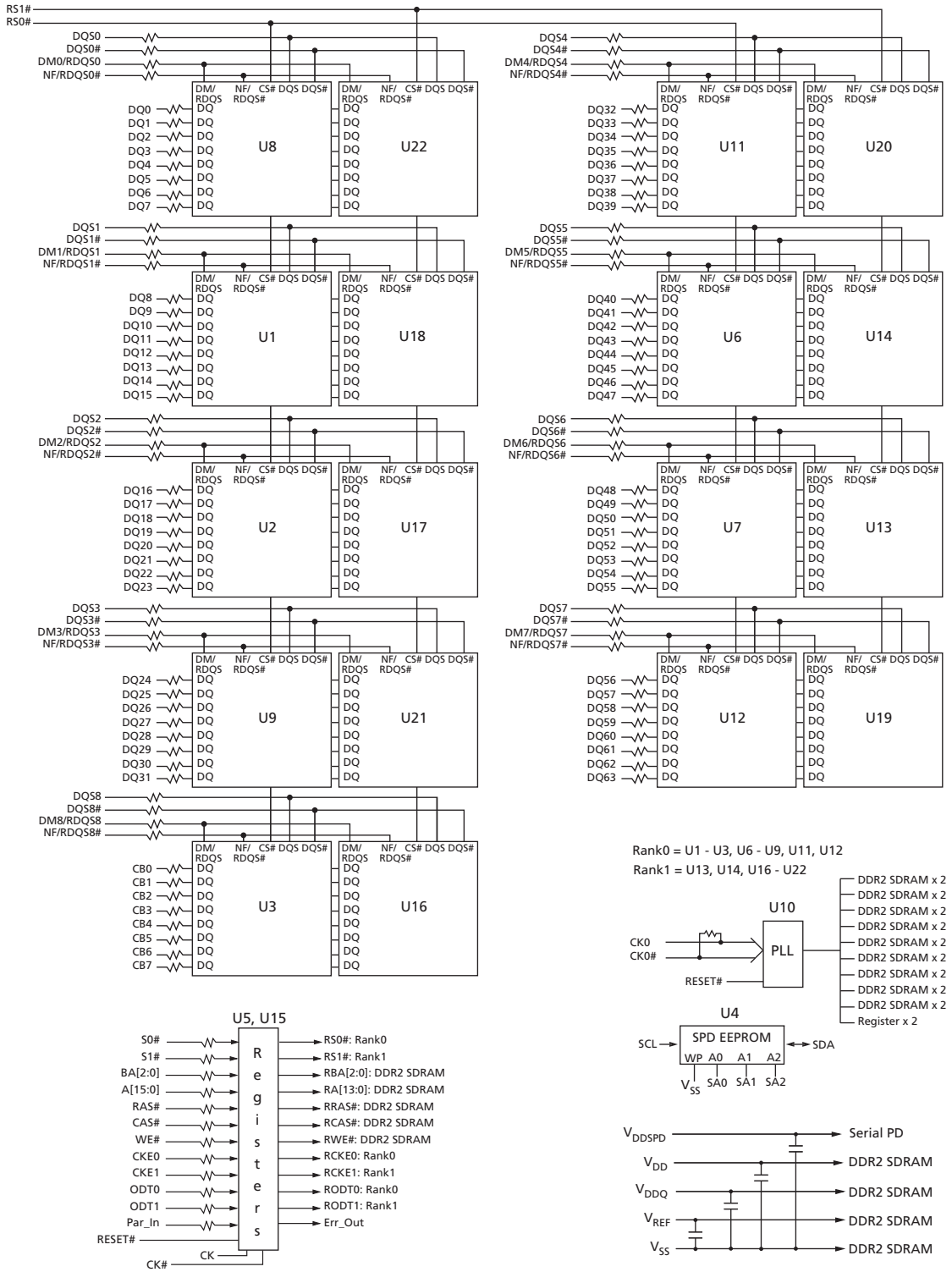
Table 5: Pin Descriptions (continued)

Symbol	Type	Description
NF	–	**No function:** These pins are connected within the module but provide no functionality.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2009 Micron Technology, Inc. All rights reserved.

Functional Block Diagram

Figure 2: Functional Block Diagram



Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2009 Micron Technology, Inc. All rights reserved.

General Description

The MT18HTF25672PK(I)Z DDR2 SDRAM module is a high-speed, CMOS, dynamic random-access 2GB memory module, organized in x72 configuration. This DDR2 SDRAM module uses internally configured eight-bank 1Gb DDR2 SDRAM devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

These DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Register and PLL EEPROM Operation

DDR2 SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR2 SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR2 SDRAM devices. The register(s) and PLL reduce clock, control, command, and address signals loading by isolating DRAM from the system controller. PLL clock timing is defined by JEDEC specifications and ensured by use of the JEDEC clock reference board. Registered mode will add one clock cycle to CL.

Parity Operations

The registering clock driver can accept a parity bit from the system's memory controller, providing even parity for the control, command, and address bus. Parity errors are flagged on the Err_Out pin. Systems not using parity are expected to function without issue if Par_In and Err_Out are left as no connects to the system.

Serial Presence-Detect EEPROM Operation

DDR2 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA[2:0], which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is connected to V_{SS}, permanently disabling hardware write protection.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2009 Micron Technology, Inc. All rights reserved.

Electrical Specifications

Stresses greater than those listed in Table 6 may cause permanent damage to the DRAM devices on the module. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 6: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}		–1.0	2.3	V
V_{DDQ}	V_{DDQ} supply voltage relative to V_{SS}		–0.5	2.3	V
V_{DDL}	V_{DDL} supply voltage relative to V_{SS}		–0.5	2.3	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		–0.5	2.3	V
I_I	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤0.95V; (All other pins not under test = 0V)	RAS#, CAS#, WE# S#, CKE, ODT	–5	5	µA
		CK, CK#	–250	+250	
		DM	–10	10	
I_{OZ}	Output leakage current; 0V ≤ V_{OUT} ≤ V_{DDQ}; DQs and ODT are disabled	DQ, DQS, DQS#	–10	10	µA
I_{VREF}	V_{REF} leakage current; V_{REF} = Valid V_{REF} level		–36	36	µA
T_{CASE}	DDR2 SDRAM device operating temperature (case)[1]	Commercial	0	+85	°C
		Industrial[2]	–40	+95	°C

Notes: 1. For further information, refer to technical note TN-00-08: Thermal Applications, available on Micron's Web site at www.micron.com/technotes.
2. Refresh rate must double when T_{CASE} exceeds 85°C.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2009 Micron Technology, Inc. All rights reserved.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 7.

Table 7: Module and Component Speed Grades
DDR2 components may exceed the listed module speed grades

Module Speed Grade	Component Speed Grade
-80E	-25E
-800	-25
-667	-3
-53E	-37E
-40E	-5E

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2009 Micron Technology, Inc. All rights reserved.

I_{DD} Specifications

Table 8: DDR2 I_{DD} Specifications and Conditions – 2GB

Values shown for MT47H128M8 DDR2 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter/Condition		Symbol	-80E -800	-667	Units
Operating one bank active-precharge current: $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RC = {}^{t}RC (I_{DD})$, $^{t}RAS = {}^{t}RAS\ MIN (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD0}[1]	873	828	mA
Operating one bank active-read-precharge current: I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RC = {}^{t}RC (I_{DD})$, $^{t}RAS = {}^{t}RAS\ MIN (I_{DD})$, $^{t}RCD = {}^{t}RCD (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as I_{DD4W}		I_{DD1}[1]	1053	963	mA
Precharge power-down current: All device banks idle; $^{t}CK = {}^{t}CK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		I_{DD2P}[2]	126	126	mA
Precharge quiet standby current: All device banks idle; $^{t}CK = {}^{t}CK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		I_{DD2Q}[2]	900	720	mA
Precharge standby current: All device banks idle; $^{t}CK = {}^{t}CK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD2N}[2]	900	720	mA
Active power-down current: All device banks open; $^{t}CK = {}^{t}CK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	I_{DD3P}[2]	720	540	mA
	Slow PDN exit MR[12] = 1		180	180	mA
Active standby current: All device banks open; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RAS = {}^{t}RAS\ MAX (I_{DD})$, $^{t}RP = {}^{t}RP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD3N}[2]	1080	990	mA
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (I_{DD}), AL = 0; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RAS = {}^{t}RAS\ MAX (I_{DD})$, $^{t}RP = {}^{t}RP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD4W}[1]	1503	1278	mA
Operating burst read current: All device banks open; Continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RAS = {}^{t}RAS\ MAX (I_{DD})$, $^{t}RP = {}^{t}RP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD4R}[1]	1503	1278	mA
Burst refresh current: $^{t}CK = {}^{t}CK (I_{DD})$; REFRESH command at every $^{t}RFC (I_{DD})$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD5}[2]	4230	3870	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		I_{DD6}[2]	126	126	mA
Operating bank interleave read current: All device banks interleaving reads, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = $^{t}RCD (I_{DD})$ -1 x $^{t}CK (I_{DD})$; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RC = {}^{t}RC (I_{DD})$, $^{t}RRD = {}^{t}RRD (I_{DD})$, $^{t}RCD = {}^{t}RCD (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during DESELECTs; Data bus inputs are switching		I_{DD7}[1]	3078	2583	mA

Notes: 1. Value calculated as one module rank in this operating condition, all other module ranks in I_{DD2P} (CKE LOW) mode.
2. Value calculated reflects all module ranks in this operating condition.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2009 Micron Technology, Inc. All rights reserved.

Register and PLL Specifications

Table 9: Register Specifications
SSTU32866 devices or equivalent

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	$V_{IH(DC)}$	Control, command, address	SSTL_18	$V_{REF(DC)}$ + 125	V_{DDQ} + 250	mV
DC low-level input voltage	$V_{IL(DC)}$	Control, command, address	SSTL_18	0	$V_{REF(DC)}$ - 125	mV
AC high-level input voltage	$V_{IH(AC)}$	Control, command, address	SSTL_18	$V_{REF(DC)}$ + 250	V_{DD}	mV
AC low-level input voltage	$V_{IL(AC)}$	Control, command, address	SSTL_18	0	$V_{REF(DC)}$ - 250	mV
Output high voltage	V_{OH}	Parity output	LVCMOS	1.2	–	V
Output low voltage	V_{OL}	Parity output	LVCMOS	–	0.5	V
Input current	I_I	All pins	$V_I = V_{DDQ}$ or V_{SSQ}	–5	+5	µA
Static standby	I_{DD}	All pins	RESET# = V_{SSQ} (I_O = 0)	–	100	µA
Static operating	I_{DD}	All pins	RESET# = V_{SSQ}; $V_I = V_{IH(AC)}$ or $V_{IL(DC)}$ I_O = 0	–	40	mA
Dynamic operating (clock tree)	I_{DDD}	n/a	RESET# = V_{DD}, $V_I = V_{IH(DC)}$ or $V_{IL(AC)}$, I_O = 0; CK and CK# switching 50% duty cycle	–	Varies by manufacturer	µA
Dynamic operating (per each input)	I_{DDD}	n/a	RESET# = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, I_O = 0; CK and CK# switching 50% duty cycle; One data input switching at $^tCK/2$, 50% duty cycle	–	Varies by manufacturer	µA
Input capacitance (per device, per pin)	C_I	All inputs except RESET#	$V_I = V_{REF}$ ±250mV; V_{DDQ} = 1.8V	2.5	3.5	pF
Input capacitance (per device, per pin)	C_I	RESET#	$V_I = V_{DDQ}$ or V_{SSQ}	–	Varies by manufacturer	pF

Notes: 1. Timing and switching specifications for the register listed above are critical for proper operation of the DDR2 SDRAM RDIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this register is available in JEDEC standard JESD82.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2009 Micron Technology, Inc. All rights reserved.

Table 10: PLL Specifications
CU877 device or equivalent JESD82-8.01

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	V_{IH}	RESET#	LVCMOS	0.65 × V_{DD}	–	V
DC low-level input voltage	V_{IL}	RESET#	LVCMOS	–	0.35 × V_{DD}	V
Input voltage (limits)	V_{IN}	RESET#, CK, CK#	–	–0.3	V_{DDQ} + 0.3	V
DC high-level input voltage	V_{IH}	CK, CK#	Differential input	0.65 × V_{DD}	–	V
DC low-level input voltage	V_{IL}	CK, CK#	Differential input	–	0.35 × V_{DD}	V
Input differential-pair cross voltage	V_{IX}	CK, CK#	Differential input	(V_{DDQ}/2) - 0.15	(V_{DDQ}/2) + 0.15	V
Input differential voltage	$V_{ID(DC)}$	CK, CK#	Differential input	0.3	V_{DDQ} + 0.4	V
Input differential voltage	$V_{ID(AC)}$	CK, CK#	Differential input	0.6	V_{DDQ} + 0.4	V
Input current	I_I	RESET#	V_I = V_{DDQ} or V_{SSQ}	–10	+10	µA
		CK, CK#	V_I = V_{DDQ} or V_{SSQ}	–250	+250	µA
Output disabled current	I_{ODL}		RESET# = V_{SSQ}; V_I = $V_{IH(AC)}$ or $V_{IL(DC)}$	100	–	µA
Static supply current	I_{DDLD}		CK = CK# = LOW	–	500	µA
Dynamic supply	I_{DD}	n/a	CK, CK# = 270 MHz, all outputs open (not connected to PCB)	–	300	mA
Input capacitance	C_{IN}	Each input	V_I = V_{DDQ} or V_{SSQ}	2	3	pF

Table 11: PLL Clock Driver Timing Requirements and Switching Characteristics

Parameter	Symbol	Min	Max	Units
Stabilization time	^tL	–	15	µs
Input clock slew rate	SLR_I	1.0	4.0	V/ns
SSC modulation frequency	–	30	33	kHz
SSC clock input frequency deviation	–	0.0	–0.5	%
PLL loop bandwidth (–3dB from unity gain)	–	2.0	–	MHz

Notes: 1. PLL timing and switching specifications are critical for proper operation of the DDR2 DIMM. This is a subset of parameters for the specific PLL used. Detailed PLL information is available in JEDEC standard JESD82.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2009 Micron Technology, Inc. All rights reserved.

Table 12: PLL Specifications
CU877 device or equivalent JESD82-8.01

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	V_{IH}	RESET#	LVCMOS	0.65 × V_{DD}	–	V
DC low-level input voltage	V_{IL}	RESET#	LVCMOS	–	0.35 × V_{DD}	V
Input voltage (limits)	V_{IN}	RESET#, CK, CK#	–	–0.3	V_{DDQ} + 0.3	V
DC high-level input voltage	V_{IH}	CK, CK#	Differential input	0.65 × V_{DD}	–	V
DC low-level input voltage	V_{IL}	CK, CK#	Differential input	–	0.35 × V_{DD}	V
Input differential-pair cross voltage	V_{IX}	CK, CK#	Differential input	(V_{DDQ}/2) - 0.15	(V_{DDQ}/2) + 0.15	V
Input differential voltage	$V_{ID(DC)}$	CK, CK#	Differential input	0.3	V_{DDQ} + 0.4	V
Input differential voltage	$V_{ID(AC)}$	CK, CK#	Differential input	0.6	V_{DDQ} + 0.4	V
Input current	I_I	RESET#	V_I = V_{DDQ} or V_{SSQ}	–10	+10	µA
		CK, CK#	V_I = V_{DDQ} or V_{SSQ}	–250	+250	µA
Output disabled current	I_{ODL}		RESET# = V_{SSQ}; V_I = $V_{IH(AC)}$ or $V_{IL(DC)}$	100	–	µA
Static supply current	I_{DDLD}		CK = CK# = LOW	–	500	µA
Dynamic supply	I_{DD}	n/a	CK, CK# = 270 MHz, all outputs open (not connected to PCB)	–	300	mA
Input capacitance	C_{IN}	Each input	V_I = V_{DDQ} or V_{SSQ}	2	3	pF

Table 13: PLL Clock Driver Timing Requirements and Switching Characteristics

Parameter	Symbol	Min	Max	Units
Stabilization time	^tL	–	15	µs
Input clock slew rate	SLR_I	1.0	4.0	V/ns
SSC modulation frequency	–	30	33	kHz
SSC clock input frequency deviation	–	0.0	–0.5	%
PLL loop bandwidth (–3dB from unity gain)	–	2.0	–	MHz

Notes: 1. PLL timing and switching specifications are critical for proper operation of the DDR2 DIMM. This is a subset of parameters for the specific PLL used. Detailed PLL information is available in JEDEC standard JESD82.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2009 Micron Technology, Inc. All rights reserved.

Serial Presence-Detect

Table 14: Serial Presence-Detect EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	1.7	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.6	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.1	3.0	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	3.0	µA
Standby current	I_{SB}	1.6	4.0	µA
Power supply current, READ: SCL clock frequency = 100 kHz	I_{CCR}	0.4	1.0	mA
Power supply current, WRITE: SCL clock frequency = 100 kHz	I_{CCW}	2.0	3.0	mA

Table 15: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^{t}BUF	1.3	–	µs	
Data-out hold time	^{t}DH	200	–	ns	
SDA fall time	^{t}F	–	300	ns	2
SDA rise time	^{t}R	–	300	ns	2
Data-in hold time	^{t}HD:DAT	0	–	µs	
Start condition hold time	^{t}H:STA	0.6	–	µs	
Clock HIGH period	^{t}HIGH	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I	–	50	ns	
Clock LOW period	^{t}LOW	1.3	–	µs	
SCL clock frequency	^{f}SCL	–	400	kHz	
Data-in setup time	^{t}SU:DAT	100	–	ns	
Start condition setup time	^{t}SU:STA	0.6	–	µs	3
Stop condition setup time	^{t}SU:STO	0.6	–	µs	
WRITE cycle time	^{t}WRC	–	10	ms	4

Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

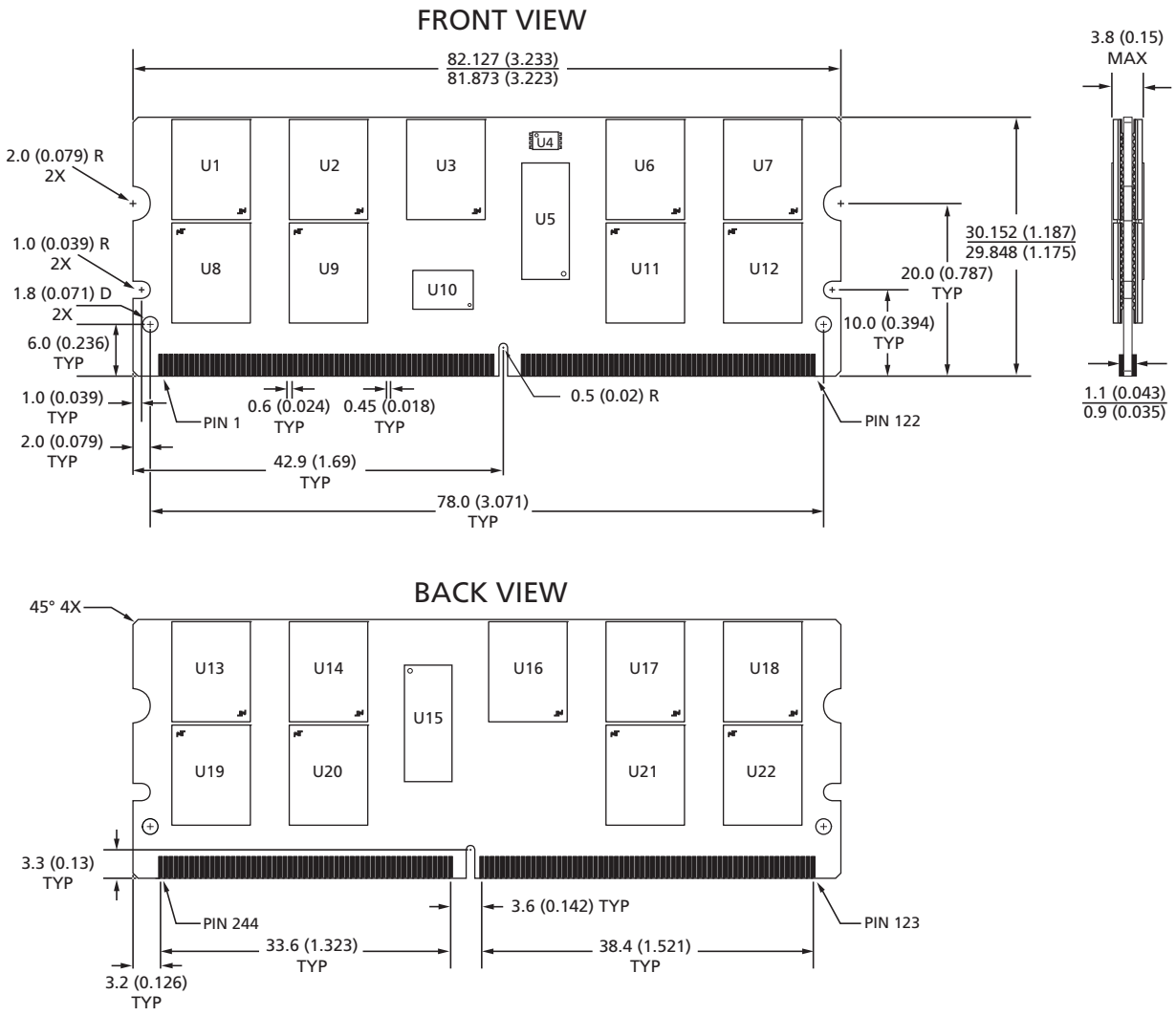
Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2009 Micron Technology, Inc. All rights reserved.

Module Dimensions

Figure 3: 244-Pin DDR2 Mini-RDIMM



Notes: 1. All dimensions are in millimeters (inches), MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for complete design dimensions.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
www.micron.com/productsupport Customer Comment Line: 800-932-4992
Micron and the Micron logo are trademarks of Micron Technology, Inc.
All other trademarks are the property of their respective owners.
This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2009 Micron Technology, Inc. All rights reserved.