DDR3 SDRAM RDIMM

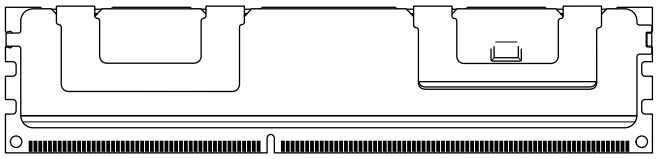
MT36JSZF51272PZ – 4GB
MT36JSZF1G72PZ – 8GB

Features

- DDR3 functionality and operations supported as defined in the component data sheet
- 240-pin, registered dual in-line memory module (RDIMM)
- Fast data transfer rates: PC3-12800, PC3-10600, PC3-8500, or PC3-6400
- Heat spreader
- 4GB (512 Meg x 72), 8GB (1 Gig x 72)
- V_{DD} = 1.5V ±0.075V
- V_{DDSPD} = +3.0V to +3.6V
- Supports ECC error detection and correction
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Dual rank
- On-board I^2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- 8 internal device banks
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

Figure 1: 240-Pin RDIMM (MO-269 R/C J)

Module height: 30.0mm (1.181in)



Options	Marking
• Operating temperature[1]	
– Commercial (0°C ≤ T_A ≤ +70°C)	None
– Industrial (–40°C ≤ T_A ≤ +85°C)	I
• Package	
– 240-pin DIMM (halogen-free)	Z
• Frequency/CAS latency	
– 1.25ns @ CL = 11 (DDR3-12800)	-1G6
– 1.5ns @ CL = 9 (DDR3-1333)	-1G4
– 1.87ns @ CL = 7 (DDR3-1066)	-1G1

Note: 1. Contact Micron for industrial temperature module offerings.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)							^tRCD (ns)	^tRP (ns)	^tRC (ns)
		CL = 11	CL = 10	CL = 9	CL = 8	CL = 7	CL = 6	CL = 5			
-1G6	PC3-12800	1600	1333	1333	1066	1066	800	667	13.125	13.125	48.125
-1G4	PC3-10600	–	1333	1333	1066	1066	800	667	13.125	13.125	49.125
-1G1	PC3-8500	–	–	–	1066	1066	800	667	13.125	13.125	50.625
-1G0	PC3-8500	–	–	–	1066	–	800	667	15	15	52.5
-80B	PC3-6400	–	–	–	–	–	800	667	15	15	52.5

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Table 2: Addressing

Parameter	4GB	8GB
Refresh count	8K	8K
Row address	16K A[13:0]	32K A[14:0]
Device bank address	8 BA[2:0]	8 BA[2:0]
Device configuration	1Gb (256 Meg x 4)	2Gb (512 Meg x 4)
Column address	2K A[11, 9:0]	2K A[11, 9:0]
Module rank address	2 S#[1:0]	2 S#[1:0]

Table 3: Part Numbers and Timing Parameters – 4GB Modules

Base device: MT41J256M4,[1] 1Gb DDR3 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT36JSZF51272P(I)Z-1G6__	4GB	512 Meg x 72	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT36JSZF51272P(I)Z-1G4__	4GB	512 Meg x 72	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT36JSZF51272P(I)Z-1G1__	4GB	512 Meg x 72	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

Table 4: Part Numbers and Timing Parameters – 8GB Modules

Base device: MT41J512M4,[1] 2Gb DDR3 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT36JSZF1G72P(I)Z-1G6__	8GB	1 Gig x 72	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT36JSZF1G72P(I)Z-1G4__	8GB	1 Gig x 72	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT36JSZF1G72P(I)Z-1G1__	8GB	1 Gig x 72	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

Notes:
1. The data sheet for the base device can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT36JSZF1G72PZ-1G1D1.

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Pin Assignments

Table 5: Pin Assignments

240-Pin DDR3 RDIMM Front								240-Pin DDR3 RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{REFDQ}	31	DQ25	61	A2	91	DQ41	121	V_{SS}	151	V_{SS}	181	A1	211	V_{SS}
2	V_{SS}	32	V_{SS}	62	V_{DD}	92	V_{SS}	122	DQ4	152	DQS12	182	V_{DD}	212	DQS14
3	DQ0	33	DQS3#	63	NF	93	DQS5#	123	DQ5	153	DQS12#	183	V_{DD}	213	DQS14#
4	DQ1	34	DQS3	64	NF	94	DQS5	124	V_{SS}	154	V_{SS}	184	CK0	214	V_{SS}
5	V_{SS}	35	V_{SS}	65	V_{DD}	95	V_{SS}	125	DQS9	155	DQ30	185	CK0#	215	DQ46
6	DQS0#	36	DQ26	66	V_{DD}	96	DQ42	126	DQS9#	156	DQ31	186	V_{DD}	216	DQ47
7	DQS0	37	DQ27	67	V_{REFCA}	97	DQ43	127	V_{SS}	157	V_{SS}	187	EVENT#	217	V_{SS}
8	V_{SS}	38	V_{SS}	68	Par_In	98	V_{SS}	128	DQ6	158	CB4	188	A0	218	DQ52
9	DQ2	39	CB0	69	V_{DD}	99	DQ48	129	DQ7	159	CB5	189	V_{DD}	219	DQ53
10	DQ3	40	CB1	70	A10	100	DQ49	130	V_{SS}	160	V_{SS}	190	BA1	220	V_{SS}
11	V_{SS}	41	V_{SS}	71	BA0	101	V_{SS}	131	DQ12	161	DQS17	191	V_{DD}	221	DQS15
12	DQ8	42	DQS8#	72	V_{DD}	102	DQS6#	132	DQ13	162	DQS17#	192	RAS#	222	DQS15#
13	DQ9	43	DQS8	73	WE#	103	DQS6	133	V_{SS}	163	V_{SS}	193	S0#	223	V_{SS}
14	V_{SS}	44	V_{SS}	74	CAS#	104	V_{SS}	134	DQS10	164	CB6	194	V_{DD}	224	DQ54
15	DQS1#	45	CB2	75	V_{DD}	105	DQ50	135	DQS10#	165	CB7	195	ODT0	225	DQ55
16	DQS1	46	CB3	76	S1#	106	DQ51	136	V_{SS}	166	V_{SS}	196	A13	226	V_{SS}
17	V_{SS}	47	V_{SS}	77	ODT1	107	V_{SS}	137	DQ14	167	NU	197	V_{DD}	227	DQ60
18	DQ10	48	V_{TT}	78	V_{DD}	108	DQ56	138	DQ15	168	RESET#	198	NC	228	DQ61
19	DQ11	49	V_{TT}	79	NC	109	DQ57	139	V_{SS}	169	CKE1	199	V_{SS}	229	V_{SS}
20	V_{SS}	50	CKE0	80	V_{SS}	110	V_{SS}	140	DQ20	170	V_{DD}	200	DQ36	230	DQS16
21	DQ16	51	V_{DD}	81	DQ32	111	DQS7#	141	DQ21	171	A15	201	DQ37	231	DQS16#
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	V_{SS}	172	A14	202	V_{SS}	232	V_{SS}
23	V_{SS}	53	Err_Out#	83	V_{SS}	113	V_{SS}	143	DQS11	173	V_{DD}	203	DQS13	233	DQ62
24	DQS2#	54	V_{DD}	84	DQS4#	114	DQ58	144	DQS11#	174	A12	204	DQS13#	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQ59	145	V_{SS}	175	A9	205	V_{SS}	235	V_{SS}
26	V_{SS}	56	A7	86	V_{SS}	116	V_{SS}	146	DQ22	176	V_{DD}	206	DQ38	236	V_{DDSPD}
27	DQ18	57	V_{DD}	87	DQ34	117	SA0	147	DQ23#	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	V_{SS}	178	A6	208	V_{SS}	238	SDA
29	V_{SS}	59	A4	89	V_{SS}	119	SA2	149	DQ28	179	V_{DD}	209	DQ44	239	V_{SS}
30	DQ24	60	V_{DD}	90	DQ40	120	V_{TT}	150	DQ29	180	A3	210	DQ45	240	V_{TT}

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Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for all DDR3 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

Table 6: Pin Descriptions

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments Table for density-specific addressing information.
BAx	Input	**Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command.
CKx, CKx#	Input	**Clock:** Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKEx	Input	**Clock enable:** Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DMx	Input	**Data mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODTx	Input	**On-die termination:** Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	**Parity input:** Parity bit for Ax, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** RESET# is an active LOW asychronous input that is connected to each DRAM and the registering clock driver. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed.
Sx#	Input	**Chip select:** Enables (registered LOW) and disables (registered HIGH) the command decoder.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I^2C bus.
CBx	I/O	**Check bits:** Used for system error detection and correction.
DQx	I/O	**Data input/output:** Bidirectional data bus.
DQSx, DQSx#	I/O	**Data strobe:** Differential data strobes. Output with read data; edge-aligned with read data; input with write data; center-aligned with write data.

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Table 6: Pin Descriptions (Continued)

Symbol	Type	Description
SDA	I/O	**Serial data:** Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the I^2C bus.
TDQSx, TDQSx#	Output	**Redundant data strobe (x8 devices only):** TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance; otherwise, TDQS# are no function.
Err_Out#	Output (open drain)	**Parity error output:** Parity error found on the command and address bus.
EVENT#	Output (open drain)	**Temperature event:**The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V. The component V_{DD} and V_{DDQ} are connected to the module V_{DD}.
V_{DDSPD}	Supply	**Temperature sensor/SPD EEPROM power supply:** 3.0–3.6V.
V_{REFCA}	Supply	**Reference voltage:** Control, command, and address $V_{DD}/2$.
V_{REFDQ}	Supply	**Reference voltage:** DQ, DM $V_{DD}/2$.
V_{SS}	Supply	Ground.
V_{TT}	Supply	**Termination voltage:** Used for control, command, and address $V_{DD}/2$.
NC	–	**No connect:** These pins are not connected on the module.
NF	–	**No function:** These pins are connected within the module, but provide no functionality.

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DQ Map

Table 7: Component-to-Module DQ Map, Front

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	2	9	U2	0	10	18
	1	0	3		1	8	12
	2	3	10		2	11	19
	3	1	4		3	9	13
U3	0	18	27	U4	0	26	36
	1	16	21		1	24	30
	2	19	28		2	27	37
	3	17	22		3	25	31
U5	0	CB2	45	U8	0	34	87
	1	CB0	39		1	32	81
	2	CB3	46		2	35	88
	3	CB1	40		3	33	82
U9	0	42	96	U10	0	50	105
	1	40	90		1	48	99
	2	43	97		2	51	106
	3	41	91		3	49	100
U11	0	58	114	U12	0	5	123
	1	56	108		1	6	128
	2	59	115		2	4	122
	3	57	109		3	7	129
U13	0	13	132	U14	0	21	141
	1	14	137		1	22	146
	2	12	131		2	20	140
	3	15	138		3	23	147
U15	0	29	150	U16	0	CB5	159
	1	30	155		1	CB6	164
	2	28	149		2	CB4	158
	3	31	156		3	CB7	165
U17	0	37	201	U18	0	45	210
	1	38	206		1	46	215
	2	36	200		2	44	209
	3	39	207		3	47	216

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Table 7: Component-to-Module DQ Map, Front (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U19	0	53	219	U20	0	61	228
	1	54	224		1	62	233
	2	52	218		2	60	227
	3	55	225		3	63	234

Table 8: Component-to-Module DQ Map, Back

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U21	0	56	108	U22	0	48	99
	1	58	114		1	50	105
	2	57	109		2	49	100
	3	59	115		3	51	106
U23	0	40	90	U24	0	32	81
	1	42	96		1	34	87
	2	41	91		2	33	82
	3	43	97		3	35	88
U25	0	CB0	39	U26	0	24	30
	1	CB2	45		1	26	36
	2	CB1	40		2	25	31
	3	CB3	46		3	27	37
U27	0	16	21	U28	0	8	12
	1	18	27		1	9	18
	2	17	22		2	10	13
	3	19	28		3	11	19
U29	0	0	3	U30	0	62	233
	1	2	9		1	61	228
	2	1	4		2	63	234
	3	3	10		3	60	227
U31	0	54	224	U32	0	46	215
	1	53	219		1	45	210
	2	55	225		2	47	216
	3	52	218		3	44	209

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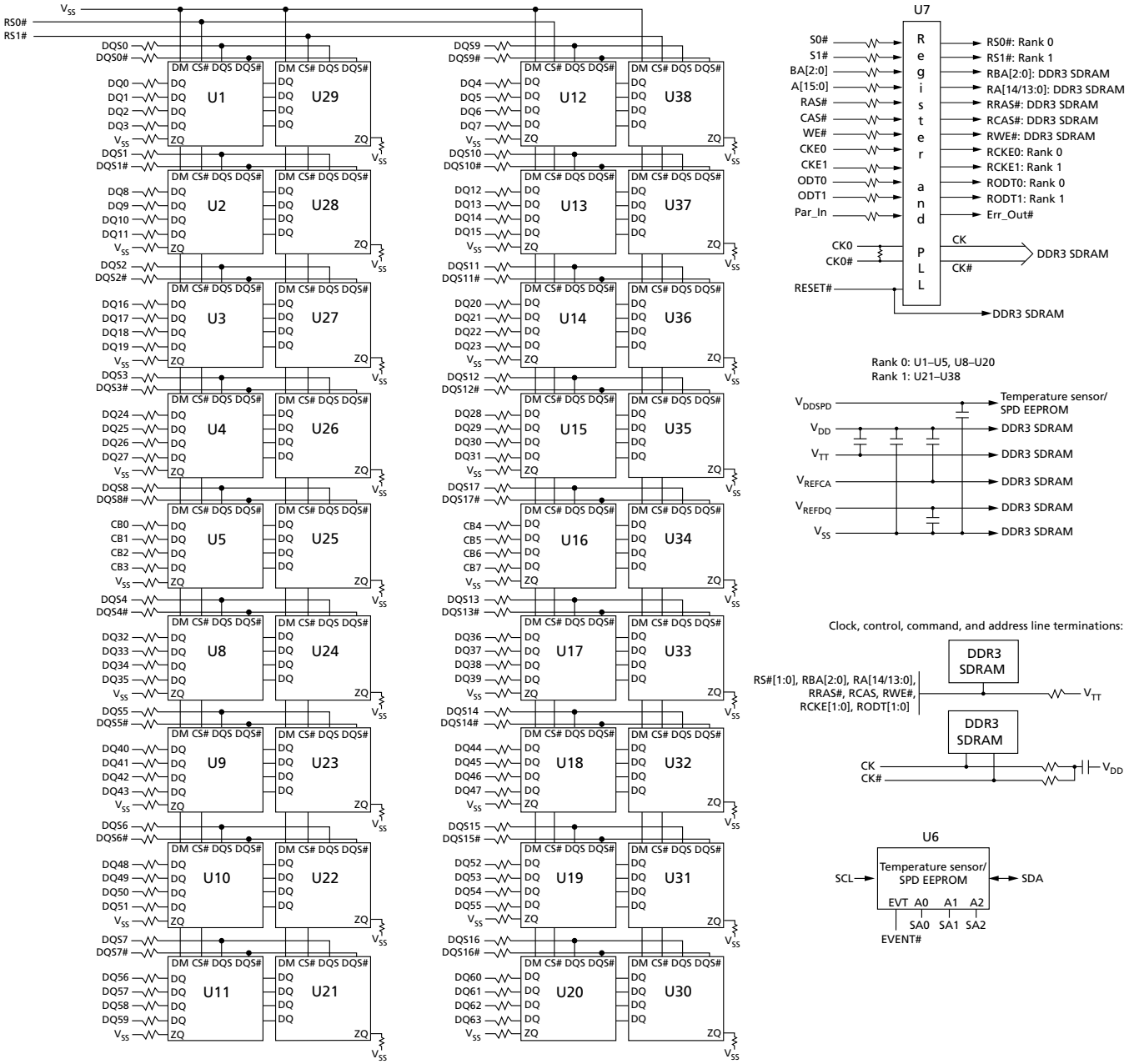
Table 8: Component-to-Module DQ Map, Back (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U33	0	38	206	U34	0	CB6	164
	1	37	201		1	CB5	159
	2	39	207		2	CB7	165
	3	36	200		3	CB4	158
U35	0	30	155	U36	0	22	146
	1	29	150		1	21	141
	2	31	156		2	23	147
	3	28	149		3	20	140
U37	0	14	137	U38	0	6	128
	1	13	132		1	5	123
	2	15	138		2	7	129
	3	12	131		3	4	122

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Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

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General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially a 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

Registering Clock Driver Operation

Registered DDR3 SDRAM modules use a registering clock driver device consisting of a register and a phase-lock loop (PLL). The device complies with the JEDEC standard "Definition of the SSTE32882 Registering Clock Driver with Parity and Quad Chip Selects for DDR3 RDIMM Applications."

The register section of the registering clock driver latches command and address input signals on the rising clock edge. The PLL section of the registering clock driver receives and redrives the differential clock signals (CK, CK#) to the DDR3 SDRAM devices. The register(s) and PLL reduce clock, control, command, and address signals loading by isolating DRAM from the system controller.

Parity Operations

The registering clock driver includes an even parity function for checking parity. The memory controller accepts a parity bit at the Par_In input and compares it with the data received on A[15:0], BA[2:0], RAS#, CAS#, and WE#. Valid parity is defined as an even number of ones (1s) across the address and command inputs (A[15:0], BA[2:0], RAS#, CAS#, and WE#) combined with Par_In. Parity errors are flagged on Err_Out#.

Address and command parity is checked during all DRAM operations and during control word WRITE operations to the registering clock driver. For SDRAM operations, the address is still propagated to the SDRAM even when there is a parity error. When writing to the internal control words of the registering clock driver, the write will be ignored if parity is not valid. For this reason, systems must connect the Par_In pins on the DIMM and provide correct parity when writing to the registering clock driver control word configuration registers.

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Temperature Sensor with Serial Presence-Detect EEPROM

Thermal Sensor Operations

The temperature from the integrated thermal sensor is monitored and converts into a digital word via the I^2C bus. System designers can use the user-programmable registers to create a custom temperature-sensing solution based on system requirements. Programming and configuration details comply with JEDEC standard No. 21-C page 4.7-1, "Definition of the TSE2002av, Serial Presence Detect with Temperature Sensor."

Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR3 SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to V_{SS}, permanently disabling hardware write protection. For further information refer to Micron technical note TN-04-42, "Memory Module Serial Presence-Detect."

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Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 9: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	1.975	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	1.975	V

Table 10: Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units	Notes
V_{DD}	V_{DD} supply voltage		1.425	1.5	1.575	V	
$V_{REFCA(DC)}$	Input reference voltage command/address bus		0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V	
$V_{REFDQ(DC)}$	I/O reference voltage DQ bus		0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V	
I_{VTT}	Termination reference current from V_{TT}		–600	–	+600	mA	
V_{TT}	Termination reference voltage (DC) – command/address bus		0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V	1
I_I	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, S#, CKE, ODT, BA, CK, CK#	TBD	TBD	TBD	µA	
		DM	–4	0	+4		
I_{OZ}	Output leakage current; 0V ≤ V_{OUT} ≤ V_{DD}; DQ and ODT are disabled; ODT is HIGH	DQ, DQS, DQS#	–10	0	+10	µA	
I_{VREF}	V_{REF} supply leakage current; V_{REFDQ} = V_{DD}/2 or V_{REFCA} = V_{DD}/2 (All other pins not under test = 0V)		–36	0	+36	µA	
T_A	Module ambient operating temperature	Commercial	0	–	+70	°C	2, 3
		Industrial	–40	–	+85	°C	
T_C	DDR3 SDRAM component case operating temperature	Commercial	0	–	+85	°C	2, 3, 4
		Industrial	–40	–	+95	°C	

Notes:
1. V_{TT} termination voltage in excess of the stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
2. T_A and T_C are simultaneous requirements.
3. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.
4. The refresh rate is required to double when 85°C < T_C ≤ 95°C.

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DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR3 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown below.

Table 11: Module and Component Speed Grades

DDR3 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
-1G9	-107
-1G6	-125
-1G4	-15E
-1G1	-187E
-1G0	-187
-80C	-25E
-80B	-25

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

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I_{DD} Specifications

Table 12: DDR3 I_{DD} Specifications and Conditions – 4GB

Values are for the MT41J256M4 DDR3 SDRAM only and are computed from values specified in the 1Gb (256 Meg x 4) component data sheet

Parameter	Symbol	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRE-CHARGE	I_{DD0}[1]	1926	1746	1566	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}[1]	2286	2106	1926	mA
Precharge power-down current: Slow exit	I_{DD2P0}[2]	432	432	432	mA
Precharge power-down current: Fast exit	I_{DD2P1}[2]	1620	1440	1260	mA
Precharge quiet standby current	I_{DD2Q}[2]	2412	2160	1908	mA
Precharge standby current	I_{DD2N}[2]	2520	2340	1980	mA
Precharge standby ODT current	I_{DD2NT}[2]	1926	1746	1566	mA
Active power-down current	I_{DD3P}[2]	1620	1440	1260	mA
Active standby current	I_{DD3N}[2]	2412	2232	2052	mA
Burst read operating current	I_{DD4R}[1]	4716	3816	3096	mA
Burst write operating current	I_{DD4W}[1]	4716	4176	3636	mA
Refresh current	I_{DD5B}[2]	9360	8640	7920	mA
Self refresh temperature current: MAX T_C = 85°C	I_{DD6}[2]	216	216	216	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{DD6ET}[2]	324	324	324	mA
All banks interleaved read current	I_{DD7}[1]	7416	5886	4716	mA
Reset current	I_{DD8}[1]	504	504	504	mA

Notes: 1. One module rank in the active I_{DD}, the other rank in I_{DD2P0} (slow exit).
2. All ranks in this I_{DD} condition.

Table 13: DDR3 I_{DD} Specifications and Conditions – 8GB

Values are for the MT41J512M4 DDR3 SDRAM only and are computed from values specified in the 2Gb (512 Meg x 4) component data sheet, die rev D

Parameter	Symbol	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRE-CHARGE	I_{DD0}[1]	1926	1746	1566	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}[1]	2106	2016	1926	mA
Precharge power-down current: Slow exit	I_{DD2P0}[2]	432	432	432	mA
Precharge power-down current: Fast exit	I_{DD2P1}[2]	1260	1080	900	mA
Precharge quiet standby current	I_{DD2Q}[2]	1440	1260	1080	mA
Precharge standby current	I_{DD2N}[2]	1512	1332	1152	mA
Precharge standby ODT current	I_{DD2NT}[2]	1116	1026	936	mA
Active power-down current	I_{DD3P}[2]	1440	1260	1080	mA

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Table 13: DDR3 I_{DD} Specifications and Conditions – 8GB (Continued)

Values are for the MT41J512M4 DDR3 SDRAM only and are computed from values specified in the 2Gb (512 Meg x 4) component data sheet, die rev D

Parameter	Symbol	1600	1333	1066	Units
Active standby current	I_{DD3N}[2]	1620	1440	1260	mA
Burst read operating current	I_{DD4R}[1]	3186	2826	2466	mA
Burst write operating current	I_{DD4W}[1]	3276	3006	2646	mA
Refresh current	I_{DD5B}[2]	7740	7200	6840	mA
Self refresh temperature current: MAX T_C = 85°C	I_{DD6}[2]	432	432	432	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{DD6ET}[2]	540	540	540	mA
All banks interleaved read current	I_{DD7}[1]	8046	7146	6246	mA
Reset current	I_{DD8}[1]	504	504	504	mA

Notes:
1. One module rank in the active I_{DD}, the other rank in I_{DD2P0} (slow exit).
2. All ranks in this I_{DD} condition.

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Registering Clock Driver Specifications

Table 14: Registering Clock Driver Electrical Characteristics

SSTE32882 devices or equivalent

Parameter	Symbol	Pins	Min	Nom	Max	Units
DC supply voltage	V_{DD}	–	1.425	1.5	1.575	V
DC reference voltage	V_{REF}	–	0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V
DC termination voltage	V_{TT}	–	0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V
AC high-level input voltage	$V_{IH(AC)}$	Control, command, address	V_{REF} + 175mV	–	V_{DD} + 400mV	V
AC low-level input voltage	$V_{IL(AC)}$	Control, command, address	–0.4	–	V_{REF} - 175mV	V
DC high-level input voltage	$V_{IH(DC)}$	Control, command, address	V_{REF} + 100mV	–	V_{DD} + 0.4	V
DC low-level input voltage	$V_{IL(DC)}$	Control, command, address	–0.4	–	V_{REF} - 100mV	V
High-level input voltage	$V_{IH(CMOS)}$	RESET#, MIRROR	0.65 × V_{DD}	–	V_{DD}	V
Low-level input voltage	$V_{IL(CMOS)}$	RESET#, MIRROR	0	–	0.35 × V_{DD}	V
Differential input crosspoint voltage range	$V_{IX(AC)}$	CK, CK#, FBIN, FBIN#	0.5 × V_{DD} - 175mV	0.5 × V_{DD}	0.5 × V_{DD} + 175mV	V
Differential input voltage	$V_{ID(AC)}$	CK, CK#	350	–	V_{DD} + TBD	mV
High-level output current	I_{OH}	Err_Out#	–	–	TBD	mA
Low-level output current	I_{OL}	Err_Out#	TBD	–	TBD	mA

Note: 1. Timing and switching specifications for the register listed are critical for proper operation of the DDR3 SDRAM RDIMMs. These are meant to be a subset of the parameters for the specific device used on the module.

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Temperature Sensor with Serial Presence-Detect EEPROM

The temperature sensor continuously monitors the module's temperature and can be read back at any time over the I^2C bus shared with the SPD EEPROM.

Serial Presence-Detect

For the latest SPD data, refer to Micron's SPD page: www.micron.com/SPD.

Table 15: Temperature Sensor with SPD EEPROM Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	3.0	3.6	V
Supply current: V_{DD} = 3.3V	I_{DD}	–	2.0	mA
Input high voltage: Logic 1; SCL, SDA	V_{IH}	1.45	V_{DDSPD} + 1	V
Input low voltage: Logic 0; SCL, SDA	V_{IL}	–	0.55	V
Output low voltage: I_{OUT} = 2.1mA	V_{OL}	–	0.4	V
Input current	I_{IN}	–5.0	5.0	µA
Temperature sensing range	–	–40	125	°C
Temperature sensor accuracy (class B)	–	–1.0	1.0	°C

Table 16: Temperature Sensor and EEPROM Serial Interface Timing

Parameter/Condition	Symbol	Min	Max	Units
Time bus must be free before a new transition can start	^tBUF	4.7	–	µs
SDA fall time	^tF	20	300	ns
SDA rise time	^tR	–	1000	ns
Data hold time	$^tHD:DAT$	200	900	ns
Start condition hold time	$^tH:STA$	4.0	–	µs
Clock HIGH period	^tHIGH	4.0	50	µs
Clock LOW period	^tLOW	4.7	–	µs
SCL clock frequency	^tSCL	10	100	kHz
Data setup time	$^tSU:DAT$	250	–	ns
Start condition setup time	$^tSU:STA$	4.7	–	µs
Stop condition setup time	$^tSU:STO$	4.0	–	µs

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EVENT# Pin

The temperature sensor also adds the EVENT# pin (open-drain). Not used by the SPD EEPROM, EVENT# is a temperature sensor output used to flag critical events that can be set up in the sensor's configuration register.

EVENT# has three defined modes of operation: interrupt mode, compare mode, and critical temperature mode. Event thresholds are programmed in the 0x01 register using a hysteresis. The alarm window provides a comparison window, with upper and lower limits set in the alarm upper boundary register and the alarm lower boundary register, respectively. When the alarm window is enabled, EVENT# will trigger whenever the temperature is outside the MIN or MAX values set by the user.

The interrupt mode enables software to reset EVENT# after a critical temperature threshold has been detected. Threshold points are set in the configuration register by the user. This mode triggers the critical temperature limit and both the MIN and MAX of the temperature window.

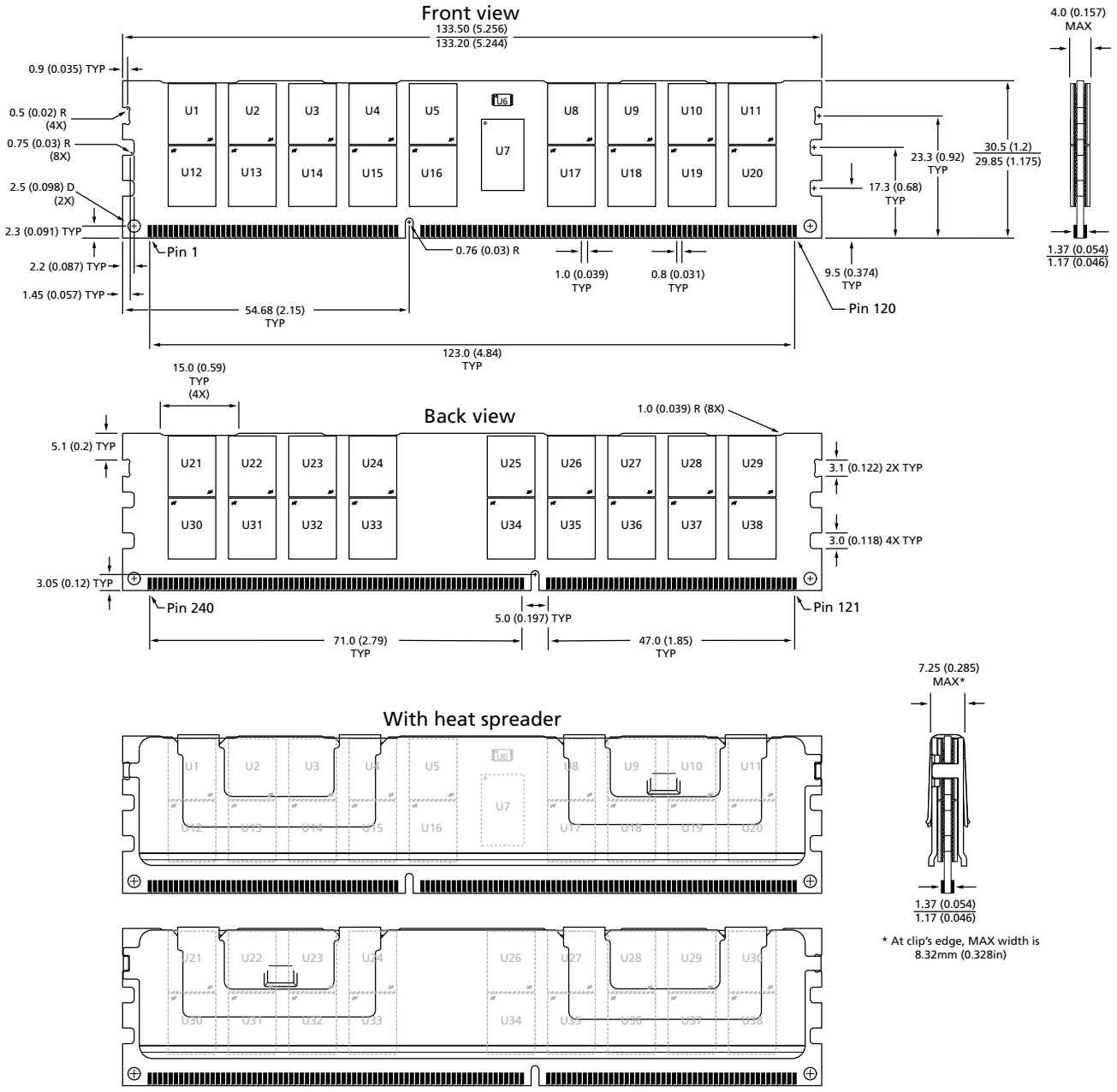
The compare mode is similar to the interrupt mode, except EVENT# cannot be reset by the user and returns to the logic HIGH state only when the temperature falls below the programmed thresholds.

Critical temperature mode triggers EVENT# only when the temperature has exceeded the programmed critical trip point. When the critical trip point has been reached, the temperature sensor goes into comparator mode, and the critical EVENT# cannot be cleared through software.

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Module Dimensions

Figure 3: 240-Pin DDR3 RDIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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