TwinDie™ 1.35V DDR3L SDRAM

MT41K512M16 – 32 Meg x 16 x 8 Banks x 2 Ranks

Description

The 8Gb (TwinDie™) 1.35V DDR3L SDRAM is a low-voltage version of the 1.5V DDR3 SDRAM device. It uses two Micron 4Gb DDR3L SDRAM x16 die for essentially two ranks of 4Gb DDR3L SDRAM. Unless stated otherwise, the DDR3L meets the functional and timing specifications listed in the equivalent-density DDR3 SDRAM data sheets. Refer to Micron's 4Gb DDR3 SDRAM data sheet for the specifications not included in this document. Specifications for base part number MT41K256M16 (monolithic) correlate to manufacturing part number MT41K512M16.

Features

- Uses two 4Gb x16 Micron die in one package
- Two ranks (includes dual CS#, ODT, CKE, and ZQ balls)
- $V_{DD} = V_{DDQ}$ = 1.35V (1.283–1.425V); backward compatible to 1.5V operation
- 1.35V center-terminated push/pull I/O
- JEDEC-standard ballout
- Low-profile package
- T_C of 0°C to 95°C
  - 0°C to 85°C: 8192 refresh cycles in 64ms
  - 85°C to 95°C: 8192 refresh cycles in 32ms

Options	Marking
• Configuration	
– 32 Meg x 16 x 8 banks x 2 ranks	512M16
• FBGA package (Pb-free)	
– 96-ball FBGA (10mm x 14mm x 1.2mm)	TNA
• Timing – cycle time[1]	
– 1.071ns @ CL = 13 (DDR3L-1866)	-107
– 1.25ns @ CL = 11 (DDR3L-1600)	-125
– 1.5ns @ CL = 9 (DDR3L-1333)	-15E
– 1.87ns @ CL = 7 (DDR3L-1066)	-187E
• Operating temperature	
– Commercial (0°C ≤ T_C ≤ 95°C)	None
– Industrial (-40°C ≤ T_C ≤ 95°C)	IT
• Revision	:E

Note: 1. CL = CAS (READ) latency.

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-107[1, 2,3]	1866	13-13-13	13.91	13.91	13.91
-125[1, 2]	1600	11-11-11	13.75	13.75	13.75
-15E[1]	1333	9-9-9	13.5	13.5	13.5
-187E	1066	7-7-7	13.1	13.1	13.1

Notes: 1. Backward compatible to 1066, CL = 7 (-187E).
2. Backward compatible to 1333, CL = 9 (-15E).
3. Backward compatible to 1600, CL = 11 (-125).

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Table 2: Addressing

Parameter	512 Meg x 16
Configuration	32 Meg x 16 x 8 banks x 2 ranks
Refresh count	8K
Row address	32K A[14:0]
Bank address	8 BA[2:0]
Column address	1K A[9:0]
Page size	2KB

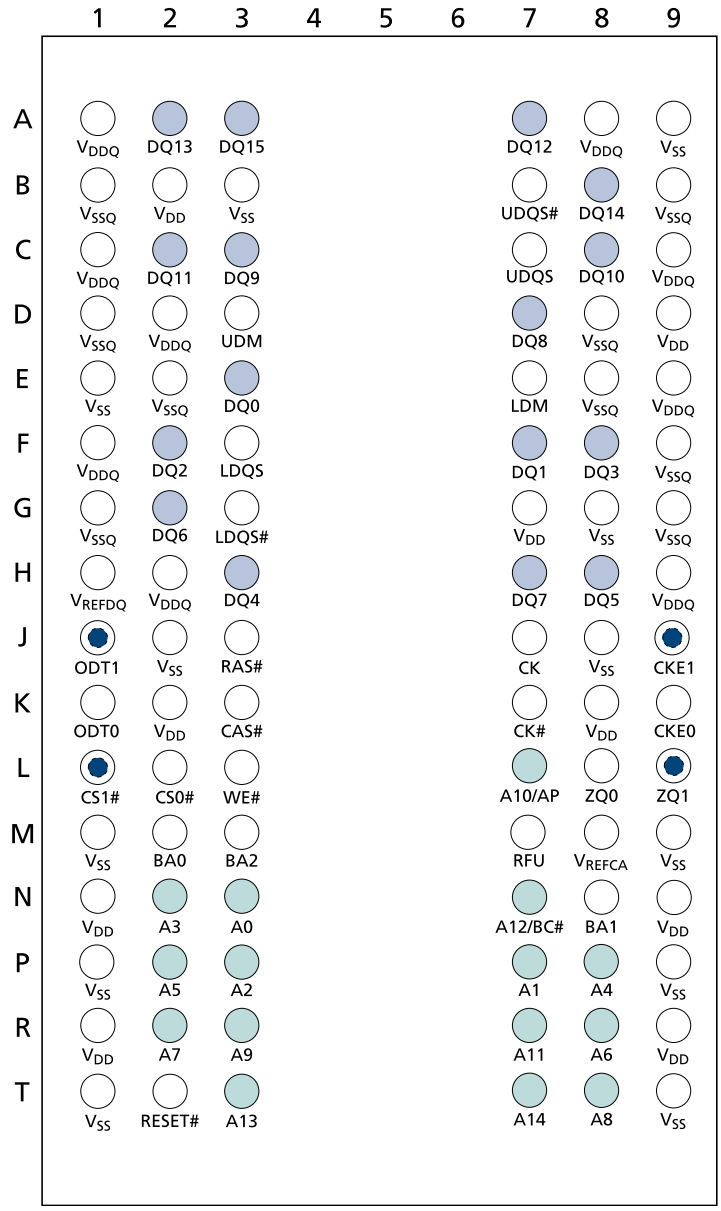
FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

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Ball Assignments and Descriptions

Figure 1: 96-Ball FBGA – x16 (Top View)



Note: 1. Dark balls (with rings) designate balls that differ from the monolithic versions.

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Table 3: 96-Ball FBGA – x16 Ball Descriptions

Symbol	Type	Description
A[14:13], A12/BC#, A11, A10/AP, A[9:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA}. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4). See Truth Table – Command in the DDR3 SDRAM data sheet.
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA}.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE[1:0]	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle),or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.
CS#[1:0]	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to V_{REFCA}.
LDM	Input	**Input data mask:** LDM is a lower-byte, input mask signal for write data. Lower-byte input data is masked when LDM is sampled HIGH along with the input data during a write access. Although the LDM ball is input-only, the LDM loading is designed to match that of the DQ and DQS balls. LDM is referenced to V_{REFDQ}.
ODT[0:1]	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[15:0], LDQS, LDQS#, UDQS, UDQS#, LDM, and UDM for the x16; DQ0[7:0], DQS, DQS#, DM/TDQS, and NF/TDQS# (when TDQS is enabled) for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA}.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA}.

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Table 3: 96-Ball FBGA – x16 Ball Descriptions (Continued)

Symbol	Type	Description
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DD} and DC LOW ≤ 0.2 × V_{DDQ}. RESET# assertion and de-assertion are asynchronous.
UDM	Input	**Input data mask:** UDM is an upper-byte input mask signal for write data. Upper-byte input data is masked when UDM is sampled HIGH along with that input data during a WRITE access. Although the UDM ball is input-only, the UDM loading is designed to match that of the DQ and DQS balls. UDM is referenced to V_{REFDQ}.
DQ[7:0]	I/O	**Data input/output:** Lower byte of bidirectional data bus for the x16 configuration. DQ[7:0] are referenced to V_{REFDQ}.
DQ[15:8]	I/O	**Data input/output:** Upper byte of bidirectional data bus for the x16 configuration. DQ[15:8] are referenced to V_{REFDQ}.
LDQS, LDQS#	I/O	**Lower byte data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
UDQS, UDQS#	I/O	**Upper byte data strobe:** Output with read data. Edge-aligned with read data. Input with write data. DQS is center-aligned to write data.
V_{DD}	Supply	**Power supply:** 1.35V, 1.283–1.45V.
V_{DDQ}	Supply	**DQ power supply:** 1.35V, 1.283–1.45V.
V_{REFCA}	Supply	**Reference voltage for control, command, and address:** V_{REFCA} must be maintained at all times (including self refresh) for proper device operation.
V_{REFDQ}	Supply	**Reference voltage for data:** V_{REFDQ} must be maintained at all times (excluding self refresh) for proper device operation.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ[1:0]	Reference	**External reference ball for output drive calibration:** This lower byte ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}.
NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).

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Functional Description

The TwinDie DDR3L SDRAM is a high-speed, CMOS dynamic random access memory device internally configured as two 8-bank DDR3L SDRAM devices.

Although each die is tested individually within the dual-die package, some TwinDie test results may vary from a like die tested within a monolithic die package.

The DDR3L SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR3L SDRAM input receiver. DQS is center-aligned with data for WRITEs. The read data is transmitted by the DDR3L SDRAM and edge-aligned to the data strobes.

Read and write accesses to the DDR3L SDRAM are burst-oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits (including CS*n*#, BA*n*, and A*n*) registered coincident with the READ or WRITE command are used to select the rank, bank, and starting column location for the burst access.

This data sheet provides a general description, package dimensions, and the package ballout. Refer to the Micron monolithic DDR3L data sheet for complete information regarding individual die initialization, register definition, command descriptions, and die operation.

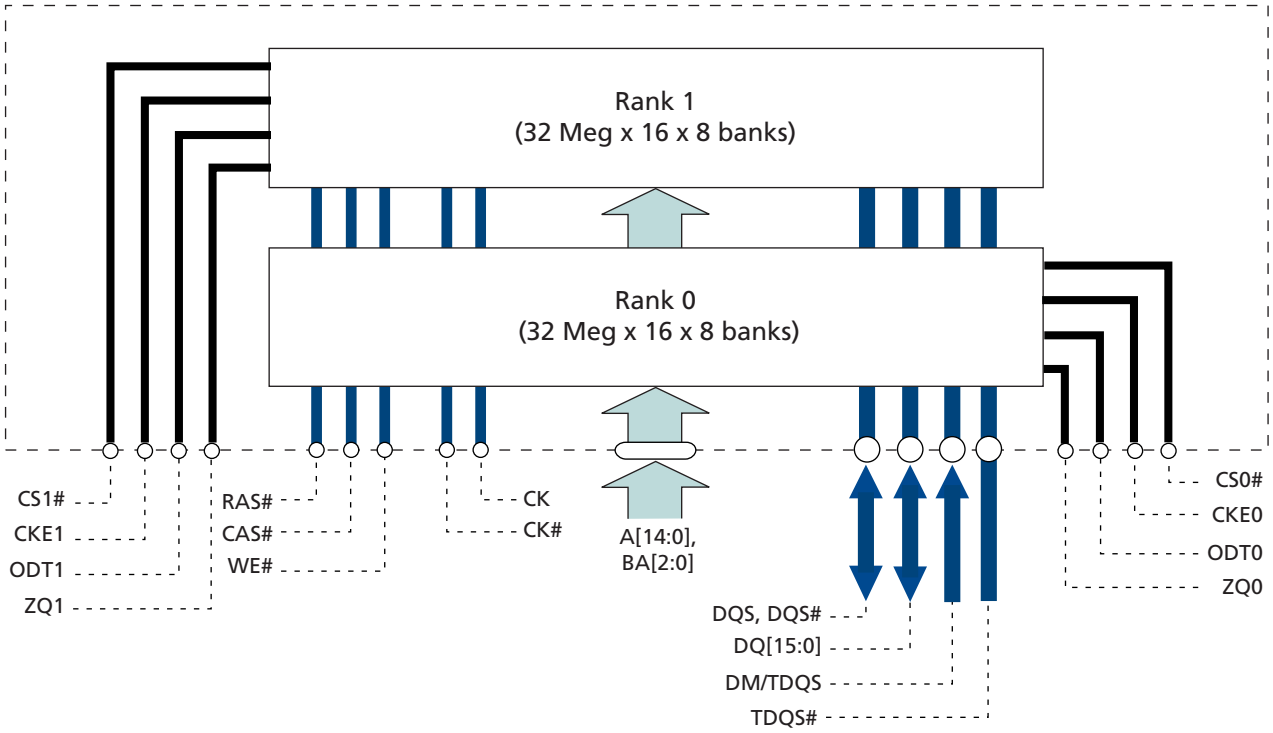
Industrial Temperature

The industrial temperature (IT) option, if offered, requires that the case temperature not exceed –40°C or 95°C. JEDEC specifications require the refresh rate to double when T_C exceeds 85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance, I_{DD} values, some IDD specifications and the input/output impedance must be derated when T_C is < 0°C or > 95°C. See the DDR3 monolithic data sheet for details.

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Functional Block Diagram

Figure 2: Functional Block Diagram (32 Meg x 16 x 8 Banks x 2 Ranks)



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Electrical Specifications

Absolute Rating

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the device data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 4: Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
V_{DD} supply voltage relative to V_{SS}	V_{DD}	–0.4	1.975	V	1
V_{DD} supply voltage relative to V_{SSQ}	V_{DDQ}	–0.4	1.975	V	
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	–0.4	1.975	V	
Input leakage current Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.1V (All other pins not under test = 0V)	I_I	–4	4	µA	
V_{REF} supply leakage current V_{REFDQ} = V_{DD}/2 or V_{REFCA} = V_{DD}/2 (All other pins not under test = 0V)	I_{VREF}	–2	2	µA	2
Operating case temperature	T_C	0	95	°C	3, 4
Storage temperature	T_{STG}	–55	150	°C	

Notes:
1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times, and V_{REF} must not be greater than 0.6 × V_{DDQ}. When V_{DD} and V_{DDQ} are less than 500mV, V_{REF} may be ≤ 300mV.
2. The minimum limit requirement is for testing purposes. The leakage current on the V_{REF} pin should be minimal.
3. MAX operating case temperature. T_C is measured in the center of the package (see the Temperature Test Point Location figure).
4. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.

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Input/Output Capacitance

The lump capacitance values are not listed. Simulations should use actual models and not lumped capacitance.

Temperature and Thermal Impedance

It is imperative that the DDR3L SDRAM device's temperature specifications, shown in the following table, be maintained in order to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. Thermal impedances listed in the Thermal Characteristics table apply to the current die revision and packages.

Incorrectly using thermal impedances can produce significant errors. Read Micron technical note TN-00-08, "Thermal Applications," prior to using the values listed in the thermal impedance table. For designs that are expected to last several years and require the flexibility to use several DRAM die shrinks, consider using final target theta values (rather than existing values) to account for increased thermal impedances from the die size reduction.

The DDR3 SDRAM device's safe junction temperature range can be maintained when the T_C specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required to satisfy the case temperature specifications.

Table 5: Thermal Characteristics

Notes 1–3 apply to entire table

Parameter	Symbol	Value	Units	Notes
Operating temperature	T_C	0 to 85	°C	
		0 to 95	°C	4

Notes:
1. MAX operating case temperature T_C is measured in the center of the package, as shown below.
2. A thermal solution must be designed to ensure that the device does not exceed the maximum T_C during operation.
3. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2x refresh, which is a 3.9µs interval refresh rate. The use of self refresh temperature (SRT) or automatic self refresh (ASR), if available, must be enabled.

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Figure 3: Temperature Test Point Location

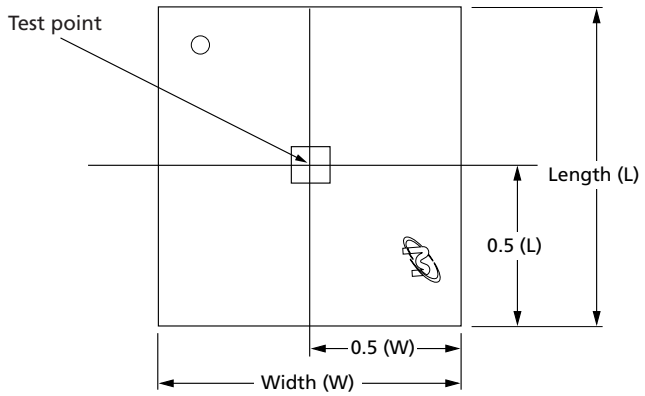


Table 6: Thermal Impedance

Die Rev	Package	Substrate	ΘJA (°C/W) Airflow = 0m/s	ΘJA (°C/W) Airflow = 1m/s	ΘJA (°C/W) Airflow = 2m/s	ΘJB (°C/W)	ΘJC (°C/W)	Notes
E	96-ball	Low conductivity	48.0	36.4	31.9	n/a	1.8	1
		High conductivity	28.6	23.4	21.6	16.5	n/a	

Note: 1. Thermal resistance data is based on a number of samples from multiple lots and should be viewed as a typical number.

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Electrical Specifications – I_{CDD} Parameters

Table 7: DDR3L I_{CDD} Specifications and Conditions (Die Revision E)

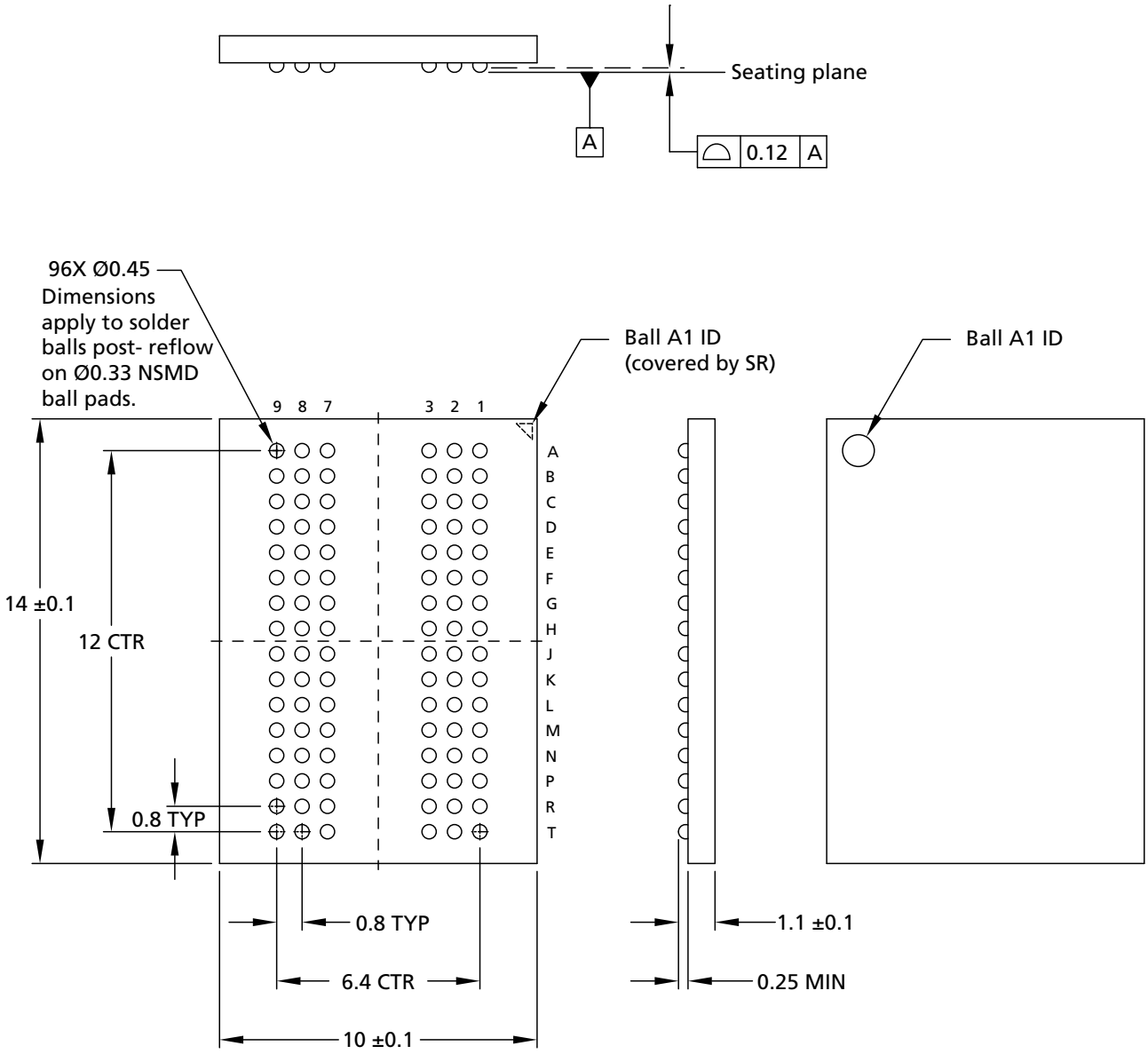
Combined Symbol	Individual Die Status	Bus Width	-187E	-15E	-125	-107	Units
I_{CDD0}	$I_{CDD0} = I_{DD0} + I_{DD2P0} + 5$	x16	78	81	89	96	mA
I_{CDD1}	$I_{CDD1} = I_{DD1} + I_{DD2P0} + 5$	x16	103	107	110	114	mA
I_{CDD2P0} (slow exit)	$I_{CDD2P0} = I_{DD2P0} + I_{DD2P0}$	x16	36	36	36	36	mA
I_{CDD2P1} (fast exit)	$I_{CDD2P1} = I_{DD2P1} + I_{DD2P0}$	x16	44	46	50	55	mA
I_{CDD2Q}	$I_{CDD2Q} = I_{DD2Q} + I_{DD2P0}$	x16	45	46	50	53	mA
I_{CDD2N}	$I_{CDD2N} = I_{DD2N} + I_{DD2P0}$	x16	46	47	50	53	mA
$I_{CDD2N\ T}$	$I_{CDD2NT} = I_{DD2NT} + I_{DD2P0}$	x16	53	57	60	63	mA
I_{CDD3P}	$I_{CDD3P} = I_{DD3P} + I_{DD2P0}$	x16	50	53	56	59	mA
I_{CDD3N}	$I_{CDD3N} = I_{DD3N} + I_{DD2P0}$	x16	59	63	65	67	mA
I_{CDD4R}	$I_{CDD4R} = I_{DD4R} + I_{DD2P0} + 5$	x16	208	225	258	275	mA
I_{CDD4W}	$I_{CDD4W} = I_{DD4W} + I_{DD2P0} + 5$	x16	160	175	194	213	mA
I_{CDD5B}	$I_{CDD5B} = I_{DD5B} + I_{DD2P0}$	x16	242	246	253	257	mA
I_{CDD6} (room temperature)	$I_{CDD6} = I_{DD6} + I_{DD6}$	x16	40	40	40	40	mA
I_{CDD6ET} (extended temperature)	$I_{CDD6ET} = I_{DD6ET} + I_{DD6ET}$	x16	50	50	50	50	mA
I_{CDD7}	$I_{CDD7} = I_{DD7} + I_{DD2P0} + 5$	x16	221	240	266	297	mA
I_{CDD8}	$I_{CDD8} = 2 \times I_{DD2P0} + 4$	x16	40	40	40	40	mA

Note: 1. I_{CDD} values reflect the combined current of both individual die. I_{DDx} represents individual die values.

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Package Dimensions

Figure 4: 96-Ball FBGA – Die Revision E (Package Code TNA)



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

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Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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