1.35V DDR3L SDRAM Addendum

MT41K256M4 – 32 Meg x 4 x 8 banks
MT41K128M8 – 16 Meg x 8 x 8 banks
MT41K64M16 – 8 Meg x 16 x 8 banks

Description

DDR3L SDRAM (1.35V) is a low voltage version of the DDR3 SDRAM (1.5V). Unless stated otherwise, DDR3L SDRAM meets the functional and timing specifications listed in the equivalent density DDR3 SDRAM data sheet located on www.micron.com.

Features

- $V_{DD} = V_{DDQ}$ = +1.35V (1.283V to 1.45V)
- Backward compatible to $V_{DD} = V_{DDQ}$ = 1.5V ±0.075V
- Differential bidirectional data strobe
- 8*n*-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS (READ) latency (CL)
- Programmable CAS additive latency (AL)
- Programmable CAS (WRITE) latency (CWL)
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- T_C of 0°C to 95°C
  - 64ms, 8192-cycle refresh at 0°C to 85°C
  - 32ms at 85°C to 95°C
- Self refresh temperature (SRT)
- Automatic self refresh (ASR)
- Write leveling
- Multipurpose register
- Output driver calibration

Options[1] — Marking

- Configuration
  - 256 Meg x 4 — 256M4
  - 128 Meg x 8 — 128M8
  - 64 Meg x 16 — 64M16
- FBGA package (Pb-free) – x4, x8
  - 78-ball FBGA (8mm x 11.5mm) Rev. F, G — JP
- FBGA package (Pb-free) – x16
  - 96-ball FBGA (8mm x 14mm) Rev. G — JT
- Timing – cycle time
  - 1.25ns @ CL = 11 (DDR3-1600) — -125
  - 1.5ns @ CL = 9 (DDR3-1333) — -15E
- Revision — :F, :G

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL (ns)	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-125[1]	1600	11-11-11	13.75	13.75	13.75
-15E[1]	1333	9-9-9	13.5	13.5	13.5
-187E	1066	7-7-7	13.1	13.1	13.1

Note: 1. Backward compatible to 1066, CL = 7 (-187E).

Table 2: Addressing

Parameter	256 Meg x 4	128 Meg x 8	64 Meg x 16
Configuration	32 Meg x 4 x 8 banks	16 Meg x 8 x 8 banks	4 Meg x 16 x 8 banks
Refresh count	8K	8K	8K
Row address	16K A[13:0]	16K A[13:0]	8K A[12:0]

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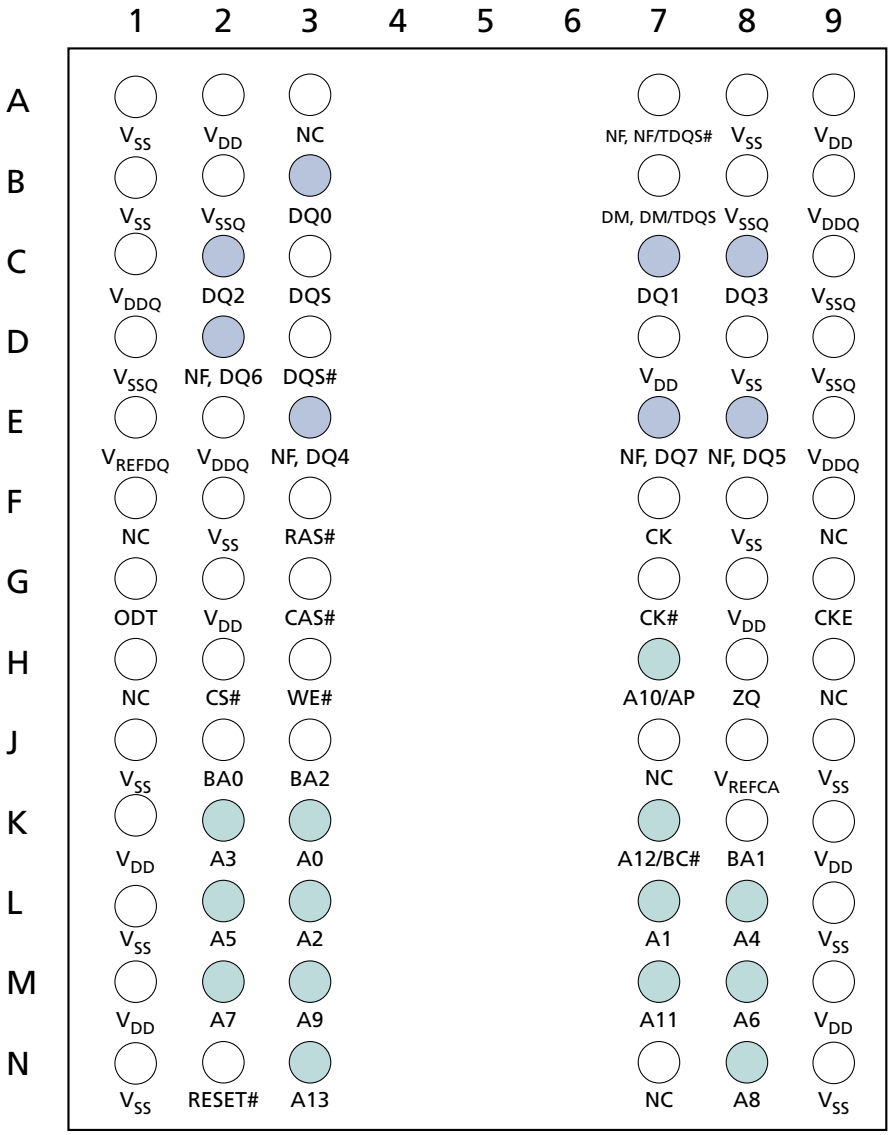
Table 2: Addressing (Continued)

Parameter	256 Meg x 4	128 Meg x 8	64 Meg x 16
Bank address	8 BA[2:0]	8 BA[2:0]	8 BA[2:0]
Column address	2K A[11, 9:0]	1K A[9:0]	1K A[9:0]
Page Size	1KB	1KB	2KB

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Ball Assignments and Descriptions

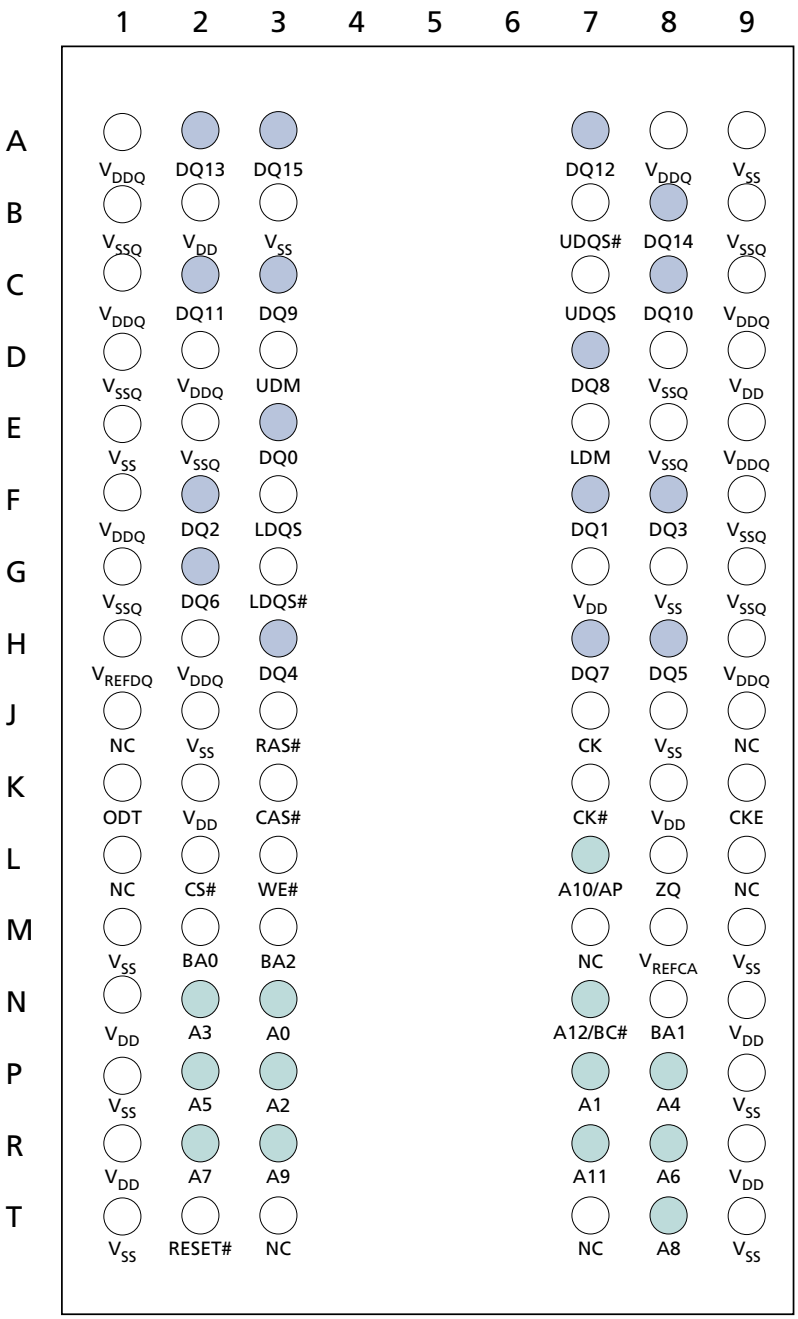
Figure 1: 78-Ball FBGA – x4, x8 Ball Assignments (Top View)



Notes:
1. Ball descriptions listed in Table 3 (page 5) are listed as x4, x8 if unique; otherwise, x4 and x8 are the same.
2. A comma separates the configuration; a slash defines a selectable function. Example: D7 = NF, NF/TDQS#. NF applies to the x4 configuration only. NF/TDQS# applies to the x8 configuration only—selectable between NF or TDQS# via MRS (symbols are defined in Table 3).

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Figure 2: 96-Ball FBGA – x16 Ball Assignments (Top View)



Notes:
1. Ball descriptions listed in Table 3 (page 5) are listed as x16.
2. A comma separates the configuration; a slash defines a selectable function.

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Table 3: 78-Ball FBGA – x4, x8 Ball Descriptions

Symbol	Type	Description
A[9:0], A10/AP, A11, A12/BC#, A13	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA}. A12/BC#: when enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4 burst chop).
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define to which bank an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA}.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle) or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to V_{REFCA}.
DM	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a write access. Although the DM ball is input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is referenced to V_{REFDQ}. DM has an optional use as TDQS on the x8 device.
ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[7:0], DQS, DQS#, and DM for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA}.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA}.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DD} and DC LOW ≤ 0.2 × V_{DDQ}. RESET# assertion and de-assertion are asynchronous.
DQ[3:0]	I/O	**Data input/output:** Bidirectional data bus for the x4 configuration. DQ[3:0] are referenced to V_{REFDQ}.

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Table 3: 78-Ball FBGA – x4, x8 Ball Descriptions (Continued)

Symbol	Type	Description
DQ[7:0]	I/O	**Data input/output:** Bidirectional data bus for the x8 configuration. DQ[7:0] are referenced to V_{REFDQ}.
DQS, DQS#	I/O	**Data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
TDQS, TDQS#	I/O	**Termination data strobe:** Applies to the x8 configuration only. When TDQS is enabled, DM is disabled, and the TDQS and TDQS# balls provide termination resistance.
V_{DD}	Supply	**Power supply:** 1.35V, 1.2825V to 1.45V operational; compatible with 1.5V operation.
V_{DDQ}	Supply	**DQ power supply:** 1.35V, 1.2825V to 1.45V operational; compatible with 1.5V operation.
V_{REFCA}	Supply	**Reference voltage for control, command, and address:** V_{REFCA} must be maintained at all times (including self refresh) for proper device operation.
V_{REFDQ}	Supply	**Reference voltage for data:** V_{REFDQ} must be maintained at all times (including self refresh) for proper device operation.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}.
NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).
NF	–	**No function:** When configured as a x4 device, these balls are NF. When configured as a x8 device, these balls are defined as TDQS#, DQ[7:4].

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Table 4: 96-Ball FBGA – x16 Ball Descriptions

Symbol	Type	Description
A[9:0], A10/AP, A11, A12/BC#	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA}. A12/BC#: when enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4).
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA}.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle) or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to V_{REFCA}.
LDM	Input	**Input data mask:** LDM is a lower byte, input mask signal for write data. Lower-byte input data is masked when LDM is sampled HIGH along with the input data during a write access. Although the LDM ball is input-only, the LDM loading is designed to match that of the DQ and DQS balls. LDM is referenced to V_{REFDQ}.
ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[15:0], LDQS, LDQS#, UDQS, UDQS#, LDM, and UDM for the x16; DQ0[7:0], DQS, DQS#, DM/TDQS, and NF/TDQS# (when TDQS is enabled) for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA}.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA}.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DD} and DC LOW ≤ 0.2 × V_{DDQ}. RESET# assertion and de-assertion are asynchronous.

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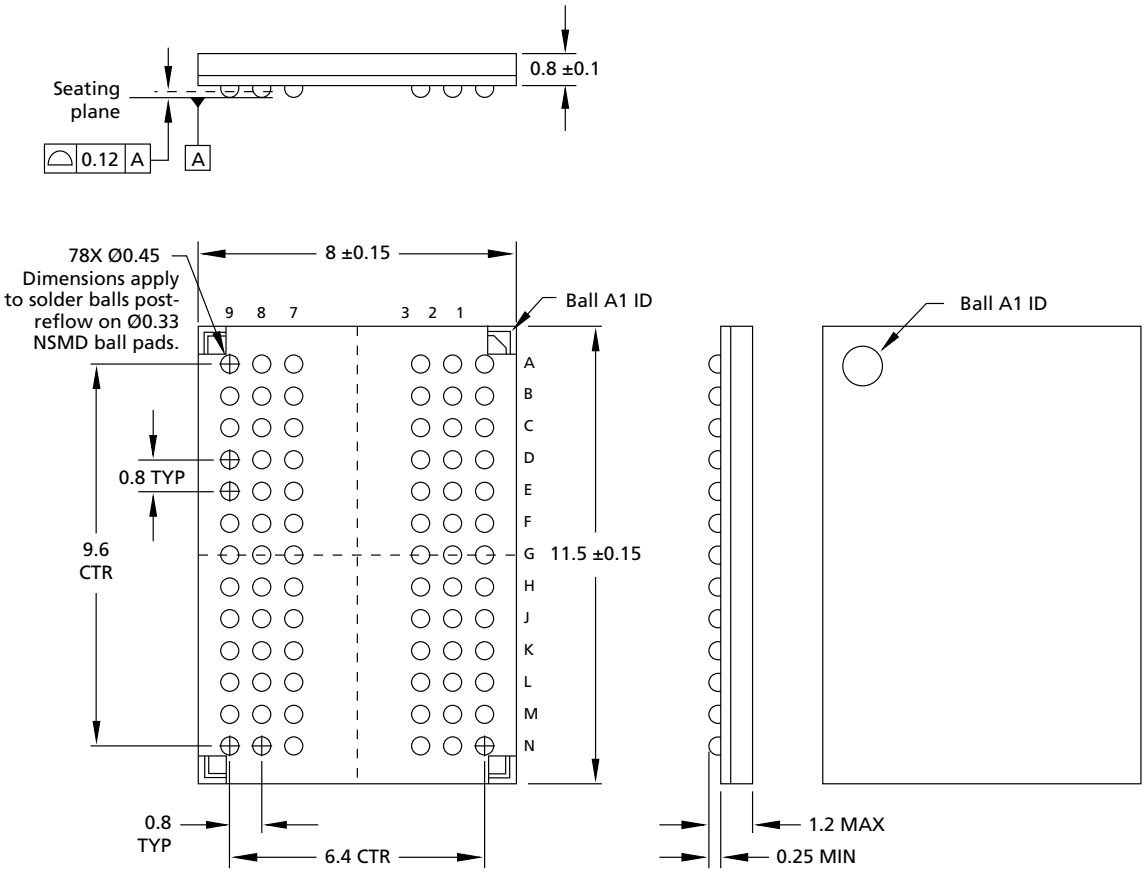
Table 4: 96-Ball FBGA – x16 Ball Descriptions (Continued)

Symbol	Type	Description
UDM	Input	**Input data mask:** UDM is an upper-byte, input mask signal for write data. Upper-byte input data is masked when UDM is sampled HIGH along with that input data during a WRITE access. Although the UDM ball is input-only, the UDM loading is designed to match that of the DQ and DQS balls. UDM is referenced to V_{REFDQ}.
DQ[7:0]	I/O	**Data input/output:** Lower byte of bidirectional data bus for the x16 configuration. DQ[7:0] are referenced to V_{REFDQ}.
DQ[15:8]	I/O	**Data input/output:** Upper byte of bidirectional data bus for the x16 configuration. DQ[15:8] are referenced to V_{REFDQ}.
LDQS, LDQS#	I/O	**Lower byte data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
UDQS, UDQS#	I/O	**Upper byte data strobe:** Output with read data. Edge-aligned with read data. Input with write data. DQS is center-aligned to write data.
V_{DD}	Supply	**Power supply:** 1.35V, 1.2825V to 1.45V.
V_{DDQ}	Supply	**DQ power supply:** 1.35V, 1.2825V to 1.45V.
V_{REFCA}	Supply	**Reference voltage for control, command, and address:** V_{REFCA} must be maintained at all times (including self refresh) for proper device operation.
V_{REFDQ}	Supply	**Reference voltage for data:** V_{REFDQ} must be maintained at all times (excluding self refresh) for proper device operation.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}.
NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).

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Package Dimensions

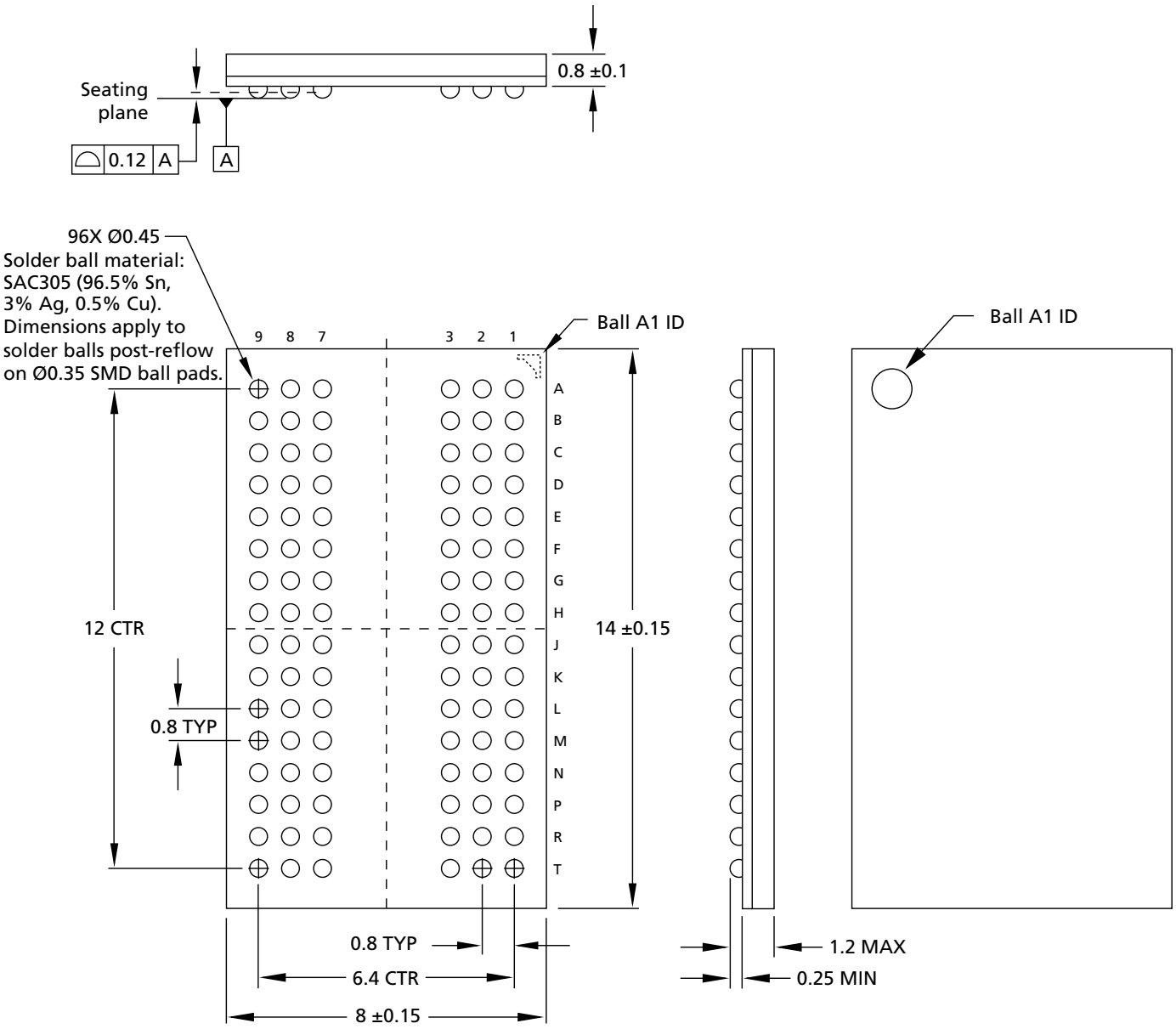
Figure 3: 78-Ball FBGA – x4, x8; (JP)



Note: 1. All dimensions are in millimeters.

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Figure 4: 96-Ball FBGA – x16 (JT)



Note: 1. All dimensions are in millimeters.

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Electrical Characteristics – I_{DD} Specifications

Table 5: I_{DD} Maximum Limits – Rev. F

Speed Bin				
I_{DD}	Width	DDR3L-1066	DDR3L-1333	Units
I_{DD0}	x4	65	75	mA
	x8	85	95	mA
I_{DD1}	x4	80	90	mA
	x8	100	110	mA
I_{DD2PO}	All	8	10	mA
I_{DD2P1}	All	25	30	mA
I_{DD2Q}	All	45	55	mA
I_{DD2N}	All	45	55	mA
I_{DD2NT}	All	65	75	mA
I_{DD3P}	All	30	37	mA
I_{DD3N}	x4, x8	50	60	mA
I_{DD4R}	x4	120	145	mA
	x8	120	145	mA
I_{DD4W}	x4	120	145	mA
	x8	120	145	mA
I_{DD5B}	All	175	185	mA
I_{DD6}	All	6	6	mA
I_{DD6ET}	All	9	9	mA
I_{DD7}	x4	230	300	mA
	x8	290	360	mA
I_{DD8}	All	I_{DD2P0} + 2mA	I_{DD2P0} + 2mA	mA

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Table 6: I_{DD} Maximum Limits – Die Rev G

Speed Bin					
I_{DD}	Width	DDR3-1066	DDR3-1333	DDR3-1600	Unit
I_{DD0}	x4	65	70	75	mA
	x8	65	70	75	mA
	x16	80	85	90	mA
I_{DD1}	x4	80	85	90	mA
	x8	80	85	90	mA
	x16	110	115	120	mA
I_{DD2P0} (Slow)	All	12	12	12	mA
I_{DD2P1} (Fast)	All	25	30	35	mA
I_{DD2Q}	All	40	45	45	mA
I_{DD2N}	All	40	45	45	mA
I_{DD2NT}	x4, x8	50	50	55	mA
	x16	60	65	70	mA
I_{DD3P}	All	30	35	35	mA
I_{DD3N}	x4, x8	40	45	45	mA
	x16	50	50	50	mA
I_{DD4R}	x4	110	130	145	mA
	x8	110	130	145	mA
	x16	150	175	200	mA
I_{DD4W}	x4	115	135	150	mA
	x8	115	135	150	mA
	x16	165	190	215	mA
I_{DD5B}	All	165	170	175	mA
I_{DD6}	All	8	8	8	mA
I_{DD6ET}	All	10	10	10	mA
I_{DD7}	x4	200	245	250	mA
	x8	200	245	250	mA
	x16	250	275	310	mA
I_{DD8}	All	I_{DD2P0} + 2mA	I_{DD2P0} + 2mA	I_{DD2P0} + 2mA	mA

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Electrical Specifications

Table 7: Input/Output Capacitance

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

Capacitance Parameters	Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Single-end I/O: DQ, DM	C_{IO}	1.5	2.5	1.5	2.5	1.5	2.3	1.5	2.3	pF
Differential I/O: DQS, DQS#, TDQS, TDQS#	C_{IO}	1.5	2.5	1.5	2.5	1.5	2.3	1.5	2.3	pF
Inputs (CTRL, CMD,ADDR)	C_I	0.75	1.3	0.75	1.3	0.75	1.3	0.75	1.3	pF

Table 8: DC Electrical Characteristics and Operating Conditions – 1.35V Operation

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Nom	Max	Units	Notes
Supply voltage	V_{DD}	1.283	1.35	1.45	V	1, 2, 3, 4
I/O supply voltage	V_{DDQ}	1.283	1.35	1.45	V	1, 2, 3, 4

Notes:
1. Maximum DC value may not be greater than 1.425V. The DC value is the linear average of $V_{DD}/V_{DDQ}(t)$ over a very long period of time (e.g., 1 sec).
2. If the maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
3. Under these supply voltages, the device operates to this DDR3L specification.
4. Once initialized for DDR3L operation, DDR3 operation may only be used if the device is in reset while V_{DD} and V_{DDQ} are changed for DDR3 operation (see Figure 5 (page 21)).

Table 9: DC Electrical Characteristics and Operating Conditions – 1.5V Operation

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Nom	Max	Units	Notes
Supply voltage	V_{DD}	1.425	1.5	1.575	V	1, 2, 3
I/O supply voltage	V_{DDQ}	1.425	1.5	1.575	V	1, 2, 3

Notes:
1. If the minimum limit is exceeded, input levels shall be governed by DDR3L specifications.
2. Under 1.5V operation, this DDR3L device operates in accordance with the DDR3 specifications under the same speed timings as defined for this device.
3. Once initialized for DDR3 operation, DDR3L operation may only be used if the device is in reset while V_{DD} and V_{DDQ} are changed for DDR3L operation (see Figure 5 (page 21)).

Table 10: Input Switching Conditions – Command and Address

Parameter/Condition	Symbol	DDR3L-800/1066	DDR3L-1333/1600	Units
Input high AC voltage: Logic 1	$V_{IH(AC160)min}$	160	160	mV
Input high AC voltage: Logic 1	$V_{IH(AC135)min}$	135	135	mV
Input high DC voltage: Logic 1	$V_{IH(DC90)min}$	90	90	mV
Input low AC voltage: Logic 0	$V_{IL(AC160)min}$	–160	–160	mV
Input low AC voltage: Logic 0	$V_{IL(AC135)min}$	–135	–135	mV

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Table 10: Input Switching Conditions – Command and Address (Continued)

Parameter/Condition	Symbol	DDR3L-800/1066	DDR3L-1333/1600	Units
Input low DC voltage: Logic 0	$V_{IL(DC90)min}$	–90	–90	mV

Table 11: Input Switching Conditions – DQ and DM

Parameter/Condition	Symbol	DDR3L-800/1066	DDR3L-1333/1600	Units
Input high AC voltage: Logic 1	$V_{IH(AC160)min}$	160	–	mV
Input high AC voltage: Logic 1	$V_{IH(AC135)min}$	135	135	mV
Input high DC voltage: Logic 1	$V_{IH(DC90)min}$	90	90	mV
Input low AC voltage: Logic 0	$V_{IL(AC160)min}$	–160	–	mV
Input low AC voltage: Logic 0	$V_{IL(AC135)min}$	–135	–135	mV
Input low DC voltage: Logic 0	$V_{IL(DC90)min}$	–90	–90	mV

Table 12: Differential Input Operating Conditions (CK, CK# and DQS, DQS#)

Parameter/Condition	Symbol	Min	Max	Units
Differential input logic high – slew	$V_{IH,diff(AC)slew}$	180	N/A	mV
Differential input logic low – slew	$V_{IL,diff(AC)slew}$	N/A	–180	mV
Differential input logic high	$V_{IH,diff(AC)}$	$2 \times (V_{IH(AC)} - V_{REF})$	V_{DD}/V_{DDQ}	mV
Differential input logic low	$V_{IL,diff(AC)}$	V_{SS}/V_{SSQ}	$2 \times (V_{REF} - V_{IL(AC)})$	mV
Single-ended high level for strobes	V_{SEH}	$V_{DDQ}/2 + 160$	V_{DDQ}	mV
Single-ended high level for CK, CK#		$V_{DD}/2 + 160$	V_{DD}	mV
Single-ended low level for strobes	V_{SEL}	V_{SSQ}	$V_{DDQ}/2 - 160$	mV
Single-ended low level for CK, CK#		V_{SS}	$V_{DD}/2 - 160$	mV

Table 13: Required Time ^{t}DVAC for CK/CK#, DQS/DQS# Differential for AC Ringback

Slew Rate (V/ns)	^{t}DVAC at 320mV (ps)	^{t}DVAC at 270mV (ps)
>4.0	70	209
4.0	53	198
3.0	47	194
2.0	35	186
1.8	31	184
1.6	26	181
1.4	20	177
1.2	12	171
1.0	0	164
<1.0	0	164

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Table 14: R_{TT} Effective Impedance

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

MR1 [9, 6, 2]	R_{TT}	Resistor	V_{OUT}	Min	Nom	Max	Units
0, 1, 0	120Ω	$R_{TT,120PD240}$	0.2 × V_{DDQ}	0.6	1.0	1.15	$R_{ZQ}/1$
			0.5 × V_{DDQ}	0.9	1.0	1.15	$R_{ZQ}/1$
			0.8 × V_{DDQ}	0.9	1.0	1.45	$R_{ZQ}/1$
		$R_{TT,120PU240}$	0.2 × V_{DDQ}	0.9	1.0	1.45	$R_{ZQ}/1$
			0.5 × V_{DDQ}	0.9	1.0	1.15	$R_{ZQ}/1$
			0.8 × V_{DDQ}	0.6	1.0	1.15	$R_{ZQ}/1$
	120Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	$R_{ZQ}/2$
0, 0, 1	60Ω	$R_{TT,60PD120}$	0.2 × V_{DDQ}	0.6	1.0	1.15	$R_{ZQ}/2$
			0.5 × V_{DDQ}	0.9	1.0	1.15	$R_{ZQ}/2$
			0.8 × V_{DDQ}	0.9	1.0	1.45	$R_{ZQ}/2$
		$R_{TT,60PU120}$	0.2 × V_{DDQ}	0.9	1.0	1.45	$R_{ZQ}/2$
			0.5 × V_{DDQ}	0.9	1.0	1.15	$R_{ZQ}/2$
			0.8 × V_{DDQ}	0.6	1.0	1.15	$R_{ZQ}/2$
	60Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	$R_{ZQ}/4$
0, 1, 1	40Ω	$R_{TT,40PD80}$	0.2 × V_{DDQ}	0.6	1.0	1.15	$R_{ZQ}/3$
			0.5 × V_{DDQ}	0.9	1.0	1.15	$R_{ZQ}/3$
			0.8 × V_{DDQ}	0.9	1.0	1.45	$R_{ZQ}/3$
		$R_{TT,40PU80}$	0.2 × V_{DDQ}	0.9	1.0	1.45	$R_{ZQ}/3$
			0.5 × V_{DDQ}	0.9	1.0	1.15	$R_{ZQ}/3$
			0.8 × V_{DDQ}	0.6	1.0	1.15	$R_{ZQ}/3$
	40Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	$R_{ZQ}/6$
1, 0, 1	30Ω	$R_{TT,30PD60}$	0.2 × V_{DDQ}	0.6	1.0	1.15	$R_{ZQ}/4$
			0.5 × V_{DDQ}	0.9	1.0	1.15	$R_{ZQ}/4$
			0.8 × V_{DDQ}	0.9	1.0	1.45	$R_{ZQ}/4$
		$R_{TT,30PU60}$	0.2 × V_{DDQ}	0.9	1.0	1.45	$R_{ZQ}/4$
			0.5 × V_{DDQ}	0.9	1.0	1.15	$R_{ZQ}/4$
			0.8 × V_{DDQ}	0.6	1.0	1.15	$R_{ZQ}/4$
	30Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	$R_{ZQ}/8$
1, 0, 0	20Ω	$R_{TT,20PD40}$	0.2 × V_{DDQ}	0.6	1.0	1.15	$R_{ZQ}/6$
			0.5 × V_{DDQ}	0.9	1.0	1.15	$R_{ZQ}/6$
			0.8 × V_{DDQ}	0.9	1.0	1.45	$R_{ZQ}/6$
		$R_{TT,20PU40}$	0.2 × V_{DDQ}	0.9	1.0	1.45	$R_{ZQ}/6$
			0.5 × V_{DDQ}	0.9	1.0	1.15	$R_{ZQ}/6$
			0.8 × V_{DDQ}	0.6	1.0	1.15	$R_{ZQ}/6$
	20Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	$R_{ZQ}/12$

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Table 15: Reference Settings for ODT Timing Measurements

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

Measured Parameter	$R_{TT,nom}$ Setting	$R_{TT(WR)}$ Setting	V_{SW1}	V_{SW2}
^{t}AON	R_{ZQ}/4 (60Ω)	N/A	50mV	100mv
	R_{ZQ}/12 (20Ω)	N/A	100mV	200mV
^{t}AOF	R_{ZQ}/4 (60Ω)	N/A	50mV	100mv
	R_{ZQ}/12 (20Ω)	N/A	100mV	200mV
^{t}AONPD	R_{ZQ}/4 (60Ω)	N/A	50mV	100mv
	R_{ZQ}/12 (20Ω)	N/A	100mV	200mV
^{t}AOFPD	R_{ZQ}/4 (60Ω)	N/A	50mV	100mv
	R_{ZQ}/12 (20Ω)	N/A	100mV	200mV
^{t}ADC	R_{ZQ}/12 (20Ω)	R_{ZQ}/2 (20Ω)	200mV	250mV

Table 16: 34Ω Driver Impedance Characteristics

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

MR1 [5, 1]	R_{ON}	Resistor	V_{OUT}	Min	Nom	Max[1]	Units
0, 1	34.3Ω	$R_{ON,34PD}$	0.2 × V_{DDQ}	0.6	1.0	1.15	R_{ZQ}/7
			0.5 × V_{DDQ}	0.9	1.0	1.15	R_{ZQ}/7
			0.8 × V_{DDQ}	0.9	1.0	1.45	R_{ZQ}/7
		$R_{ON,34PU}$	0.2 × V_{DDQ}	0.9	1.0	1.45	R_{ZQ}/7
			0.5 × V_{DDQ}	0.9	1.0	1.15	R_{ZQ}/7
			0.8 × V_{DDQ}	0.6	1.0	1.15	R_{ZQ}/7
Pull-up/pull-down mismatch (MM_{PUPD})			$V_{IL(AC)}$ to $V_{IH(AC)}$	–10	N/A	10	%

Note: 1. A larger maximum limit will result in slightly lower minimum currents.

Table 17: 40Ω Driver Impedance Characteristics

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

MR1 [5, 1]	R_{ON}	Resistor	V_{OUT}	Min	Nom	Max[1]	Units
0, 0	40Ω	$R_{ON,40PD}$	0.2 × V_{DDQ}	0.6	1.0	1.15	R_{ZQ}/6
			0.5 × V_{DDQ}	0.9	1.0	1.15	R_{ZQ}/6
			0.8 × V_{DDQ}	0.9	1.0	1.45	R_{ZQ}/6
		$R_{ON,40PU}$	0.2 × V_{DDQ}	0.9	1.0	1.45	R_{ZQ}/6
			0.5 × V_{DDQ}	0.9	1.0	1.15	R_{ZQ}/6
			0.8 × V_{DDQ}	0.6	1.0	1.15	R_{ZQ}/6
Pull-up/pull-down mismatch (MM_{PUPD})			$V_{IL(AC)}$ to $V_{IH(AC)}$	–10	N/A	10	%

Note: 1. A larger maximum limit will result in slightly lower minimum currents.

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Table 18: Single-Ended Output Driver Characteristics

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

Parameter/Condition	Symbol	Min	Max	Units
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)} = V_{REF} - 0.09 \times V_{DDQ}$ and $V_{OH(AC)} = V_{REF} + 0.09 \times V_{DDQ}$	SRQ_{se}	1.75	6	V/ns

Table 19: Differential Output Driver Characteristics

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

Parameter/Condition	Symbol	Min	Max	Units
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)} = -0.18 \times V_{DDQ}$ and $V_{OH,diff(AC)} = +0.18 \times V_{DDQ}$	SRQ_{diff}	3.5	12	V/ns
Output differential crosspoint voltage	$V_{OX(AC)}$	V_{REF} - 135	V_{REF} + 135	mV

Table 20: Electrical Characteristics and AC Operating Conditions

Parameter		Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
DQ Input Timing											
Data setup time to DQS, DQS#	Base (specification)	^{t}DS (AC160)	90	–	40	–	N/A	–	N/A	–	ps
	V_{REF} @ 1 V/ns		250	–	200	–	N/A	–	N/A	–	ps
Data setup time to DQS, DQS#	Base (specification)	^{t}DS (AC135)	140	–	90	–	45	–	25	–	ps
	V_{REF} @ 1 V/ns		275	–	225	–	180	–	160	–	ps
Data hold time from DQS, DQS#	Base (specification)	^{t}DH (DC90)	160	–	110	–	75	–	55	–	ps
	V_{REF} @ 1 V/ns		250	–	200	–	165	–	145	–	ps
Command and Address Timing											
CTRL, CMD, ADDR setup to CK, CK#	Base (specification)	^{t}IS (AC160)	215	–	140	–	80	–	60	–	ps
	V_{REF} @ 1 V/ns		375	–	300	–	240	–	220	–	ps
CTRL, CMD, ADDR setup to CK, CK#	Base (specification)	^{t}IS (AC135)	365	–	290	–	205	–	185	–	ps
	V_{REF} @ 1 V/ns		500	–	425	–	340	–	320	–	ps
CTRL, CMD, ADDR hold from CK, CK#	Base (specification)	^{t}IH (DC90)	285	–	210	–	150	–	130	–	ps
	V_{REF} @ 1 V/ns		375	–	300	–	240	–	220	–	ps

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Table 21: Derating Values for $^{t}IS/^{t}IH$ – AC160/DC90-Based

$\Delta^{t}IS$, $\Delta^{t}IH$ Derating (ps) – AC/DC-Based																
CMD/ADDR Slew Rate V/ns	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$
2.0	80	45	80	45	80	45	88	53	96	61	104	69	112	79	120	95
1.5	53	30	53	30	53	30	61	38	69	46	77	54	85	64	93	80
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	–1	–3	–1	–3	–1	–3	7	5	15	13	23	21	31	31	39	47
0.8	–3	–8	–3	–8	–3	–8	5	1	13	9	21	17	29	27	37	43
0.7	–5	–13	–5	–13	–5	–13	3	–5	11	3	19	11	27	21	35	37
0.6	–8	–20	–8	–20	–8	–20	0	–12	8	–4	16	4	24	14	32	30
0.5	–20	–30	–20	–30	–20	–30	–12	–22	–4	–14	4	–6	12	4	20	20
0.4	–40	–45	–40	–45	–40	–45	–32	–37	–24	–29	–16	–21	–8	–11	0	5

Table 22: Derating Values for $^{t}IS/^{t}IH$ – AC135/DC90-Based

$\Delta^{t}IS$, $\Delta^{t}IH$ Derating (ps) – AC/DC-Based																
CMD/ADDR Slew Rate V/ns	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$
2.0	68	45	68	45	45	45	76	53	84	61	92	69	100	79	108	95
1.5	45	30	45	30	30	30	53	38	61	46	69	54	77	64	85	80
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	2	–3	2	–3	2	–3	10	5	18	13	26	21	34	31	42	47
0.8	3	–8	3	–8	3	–8	11	1	19	9	27	17	35	27	43	43
0.7	6	–13	6	–13	6	–13	14	–5	22	3	30	11	38	21	46	37
0.6	9	–20	9	–20	9	–20	17	–12	25	–4	33	4	41	14	49	30
0.5	5	–30	5	–30	5	–30	13	–22	21	–14	29	–6	37	4	45	20
0.4	–3	–45	–3	–45	–3	–45	6	–37	14	–29	22	–21	30	–11	38	5

Table 23: Required Time ^{t}VAC Above $V_{IH(AC)}$ (Below $V_{IL[AC]}$) for Valid ADD/CMD Transition

Slew Rate (V/ns)	^{t}VAC at 160mV (ps)	^{t}VAC at 135mV (ps)
>2.0	70	209
2.0	53	198
1.5	47	194
1.0	35	186
0.9	31	184
0.8	26	181

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Table 23: Required Time ^{t}VAC Above $V_{IH(AC)}$ (Below $V_{IL[AC]}$) for Valid ADD/CMD Transition (Continued)

Slew Rate (V/ns)	^{t}VAC at 160mV (ps)	^{t}VAC at 135mV (ps)
0.7	20	177
0.6	12	171
0.5	0	164
<0.5	0	164

Table 24: Derating Values for $^{t}DS/^{t}DH$ – AC160/DC90-Based

$\Delta^{t}DS$, $\Delta^{t}DH$ Derating (ps) – AC/DC-Based																
DQ Slew Rate V/ns	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	$\Delta^{t}DS$	$\Delta^{t}DH$	$\Delta^{t}DS$	$\Delta^{t}DH$	$\Delta^{t}DS$	$\Delta^{t}DH$	$\Delta^{t}DS$	$\Delta^{t}DH$	$\Delta^{t}DS$	$\Delta^{t}DH$	$\Delta^{t}DS$	$\Delta^{t}DH$	$\Delta^{t}DS$	$\Delta^{t}DH$	$\Delta^{t}DS$	$\Delta^{t}DH$
2.0	80	45	80	45	80	45										
1.5	53	30	53	30	53	30	61	38								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			–1	–3	–1	–3	7	5	15	13	23	21				
0.8					–3	–8	5	1	13	9	21	17	29	27		
0.7							–3	–5	11	3	19	11	27	21	35	37
0.6									8	–4	16	4	24	14	32	30
0.5											4	6	12	4	20	20
0.4													–8	–11	0	5

Table 25: Derating Values for $^{t}DS/^{t}DH$ – AC135/DC90-Based

$\Delta^{t}DS$, $\Delta^{t}DH$ Derating (ps) – AC/DC-Based																
DQ Slew Rate V/ns	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	$\Delta^{t}DS$	$\Delta^{t}DH$	$\Delta^{t}DS$	$\Delta^{t}DH$	$\Delta^{t}DS$	$\Delta^{t}DH$	$\Delta^{t}DS$	$\Delta^{t}DH$	$\Delta^{t}DS$	$\Delta^{t}DH$	$\Delta^{t}DS$	$\Delta^{t}DH$	$\Delta^{t}DS$	$\Delta^{t}DH$	$\Delta^{t}DS$	$\Delta^{t}DH$
2.0	68	45	68	45	68	45										
1.5	45	30	45	30	45	30	53	38								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			2	–3	2	–3	10	5	18	13	26	21				
0.8					3	–8	11	1	19	9	27	17	35	27		
0.7							14	–5	22	3	30	11	38	21	46	37
0.6									25	–4	33	4	41	14	49	30
0.5											39	–6	37	4	45	20
0.4													30	–11	38	5

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Table 26: Required Time ^{t}VAC Above $V_{IH(AC)}$ (Below $V_{IL(AC)}$) for Valid DQTransition

Slew Rate (V/ns)	^{t}VAC at 160mV (ps)	^{t}VAC at 135mV (ps)
>2.0	70	109
2.0	53	98
1.5	47	94
1.0	35	86
0.9	31	84
0.8	26	81
0.7	20	77
0.6	12	71
0.5	0	64
<0.5	0	64

Initialization

If the SDRAM is powered up and initialized for the 1.35V operating voltage range, voltage can be increased to the 1.5V operating range provided that:

- Just prior to increasing the 1.35V operating voltages, no further commands are issued, other than NOPs or COMMAND INHIBITs, and all banks are in the precharge state.
- The 1.5V operating voltages are stable prior to issuing new commands, other than NOPs or COMMAND INHIBITs.
- The DLL is reset and relocked after the 1.5V operating voltages are stable and prior to any READ command.
- The ZQ calibration is performed. ^{t}ZQinit must be satisfied after the 1.5V operating voltages are stable and prior to any READ command.

If the SDRAM is powered up and initialized for the 1.5V operating voltage range, voltage can be reduced to the 1.35V operation range provided that:

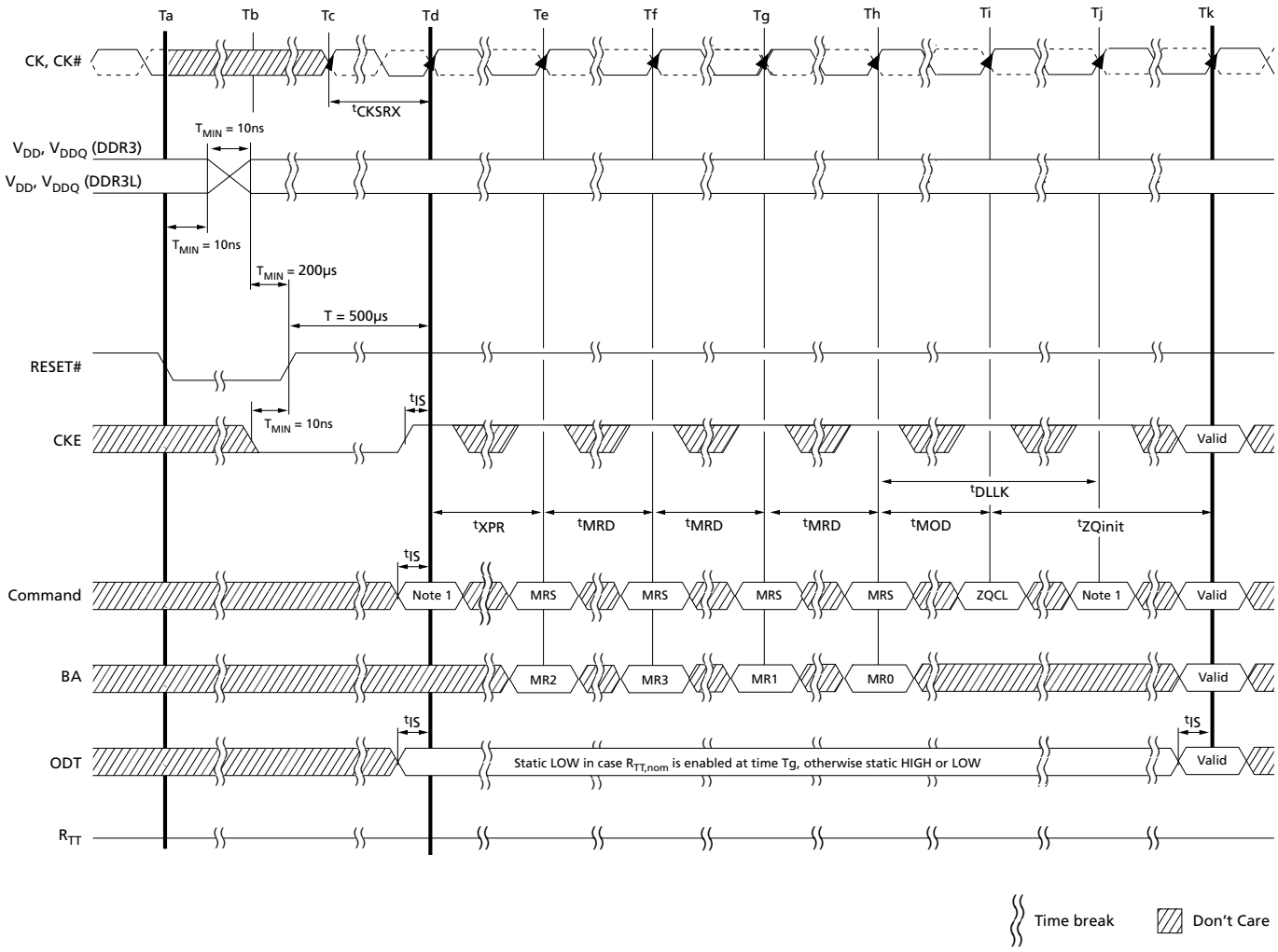
- Just prior to reducing the 1.5V operating voltages, no further commands are issued, other than NOPs or COMMAND INHIBITs, and all banks are in the precharge state.
- The 1.35V operating voltages are stable prior to issuing new commands, other than NOPs or COMMAND INHIBITs.
- The DLL is reset and relocked after the 1.35V operating voltages are stable and prior to any READ command.
- The ZQ calibration is performed. ^{t}ZQinit must be satisfied after the 1.35V operating voltages are stable and prior to any READ command.

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V_{DD} Voltage Switching

After the DDR3L DRAM is powered up and initialized, the power supply can be altered between the DDR3L and DDR3 levels, provided the sequence in Figure 5 is maintained.

Figure 5: V_{DD} Voltage Switching



Note: 1. From time point Td until Tk, NOP or DES commands must be applied between MRS and ZQCL commands.

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