# DDR SDRAM UDIMM

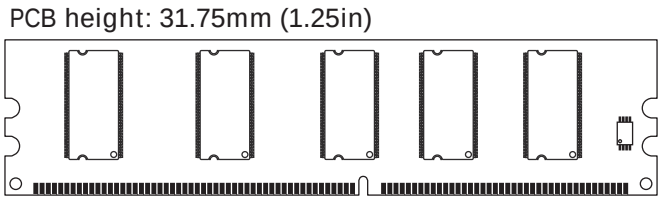
## MT5VDDT872A – 64MB[1]
## MT5VDDT1672A – 128MB[2]
## MT5VDDT3272A – 256MB[2]

For component data sheets, refer to Micron's Web site: www.micron.com

## Features

- 184-pin, unbuffered dual in-line memory module (UDIMM)
- Fast data transfer rates: PC2100, PC2700, or PC3200
- 64MB (8 Meg x 72), 128MB (16 Meg x 72), and 256MB (32 Meg x 72)
- Supports ECC error detection and correction
- $V_{DD} = V_{DD}Q = +2.5V$ (-40B: $V_{DD} = V_{DD}Q = +2.6V$)
- $V_{DDSPD} = +2.3V$ to $+3.6V$
- 2.5V I/O (SSTL_2-compatible)
- Internal, pipelined double data rate (DDR) 2*n*-prefetch architecture
- Bidirectional data strobe (DQS) transmitted/ received with data—that is, source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Multiple internal device banks for concurrent operation
- Single rank
- Selectable burst lengths (BL): 2, 4, or 8
- Auto precharge option
- Auto refresh and self refresh modes: 64MB = 15.625µs and 128MB, 256MB = 7.8125µs maximum average periodic refresh interval
- Serial presence-detect (SPD) with EEPROM
- Selectable CAS latency (CL) for maximum compatibility
- Gold edge contacts

**Figure 1: 184-Pin UDIMM (MO-206 R/C C)**




## Options — Marking

- Operating temperature[3]
  - Commercial ($0°C \le T_A \le +70°C$) — None
  - Industrial ($–40°C \le T_A \le +85°C$) — I
- Package
  - 184-pin DIMM (standard) — G
  - 184-pin DIMM (Pb-free) — Y
- Memory clock, speed, CAS latency
  - 5.0ns (200 MHz), 400 MT/s, CL = 3.0 — -40B
  - 6.0ns (167 MHz), 333 MT/s, CL = 2.5 — -335
  - 7.5ns (133 MHz), 266 MT/s, CL = 2.0 — -262
  - 7.5ns (133 MHz), 266 MT/s, CL = 2.0 — -26A
  - 7.5ns (133 MHz), 266 MT/s, CL = 2.5 — -265

Notes: 1. End of life.
2. Not recommended for new designs.
3. Contact Micron for industrial temperature module offerings.

**Table 1: Key Timing Parameters**

| Speed Grade | Industry Nomenclature | Data Rate (MT/s) | | | $^tRCD$ (ns) | $^tRP$ (ns) | $^tRC$ (ns) | Notes |
|---|---|---|---|---|---|---|---|---|
| | | CL = 3 | CL = 2.5 | CL = 2 | | | | |
| -40B | PC3200 | 400 | 333 | 266 | 15 | 15 | 55 | |
| -335 | PC2700 | – | 333 | 266 | 18 | 18 | 60 | 1 |
| -262 | PC2100 | – | 266 | 266 | 15 | 15 | 60 | |
| -26A | PC2100 | – | 266 | 266 | 20 | 20 | 65 | |
| -265 | PC2100 | – | 266 | 200 | 20 | 20 | 65 | |

Notes: 1. The values of $^tRCD$ and $^tRP$ for -335 modules show 18ns to align with industry specifications; actual DDR SDRAM device specifications are 15ns.


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**Table 2: Addressing**

| Parameter | 64MB | 128MB | 256MB |
|---|---|---|---|
| Refresh count | 4K | 8K | 8K |
| Row address | 4K (A0–A11) | 8K (A0–A12) | 8K (A0–A12) |
| Device bank address | 4 (BA0, BA1) | 4 (BA0, BA1) | 4 (BA0, BA1) |
| Device configuration | 128Mb (8 Meg x 16) | 256Mb (16 Meg x 16) | 512Mb (32 Meg x 16) |
| Column address | 512 (A0–A8) | 512 (A0–A8) | 1K (A0–A9) |
| Module rank address | 1 (S0#) | 1 (S0#) | 1 (S0#) |

**Table 3: Part Numbers and Timing Parameters – 64MB Modules**

Base device: MT46V8M16,[1] 128Mb DDR SDRAM

| Part Number[2] | Module Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Clock Cycles (CL-$^{t}$RCD-$^{t}$RP) |
|---|---|---|---|---|---|
| MT5VDDT872AG-335__ | 64MB | 8 Meg x 72 | 2.7 GB/s | 6.0ns/333 MT/s | 2.5-3-3 |
| MT5VDDT872AG-262__ | 64MB | 8 Meg x 72 | 2.1 GB/s | 7.5ns/266 MT/s | 2-2-2 |
| MT5VDDT872AG-26A__ | 64MB | 8 Meg x 72 | 2.1 GB/s | 7.5ns/266 MT/s | 2-3-3 |
| MT5VDDT872AG-265__ | 64MB | 8 Meg x 72 | 2.1 GB/s | 7.5ns/266 MT/s | 2.5-3-3 |

**Table 4: Part Numbers and Timing Parameters – 128MB Modules**

Base device: MT46V16M16,[1] 256Mb DDR SDRAM

| Part Number[2] | Module Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Clock Cycles (CL-$^{t}$RCD-$^{t}$RP) |
|---|---|---|---|---|---|
| MT5VDDT1672AG-40B__ | 128MB | 16 Meg x 72 | 3.2 GB/s | 5.0ns/400 MT/s | 3-3-3 |
| MT5VDDT1672AG-335__ | 128MB | 16 Meg x 72 | 2.7 GB/s | 6.0ns/333 MT/s | 2.5-3-3 |
| MT5VDDT1672AY-335__ | 128MB | 16 Meg x 72 | 2.7 GB/s | 6.0ns/333 MT/s | 2.5-3-3 |
| MT5VDDT1672AG-262__ | 128MB | 16 Meg x 72 | 2.1 GB/s | 7.5ns/266 MT/s | 2-2-2 |
| MT5VDDT1672AG-26A__ | 128MB | 16 Meg x 72 | 2.1 GB/s | 7.5ns/266 MT/s | 2-3-3 |
| MT5VDDT1672AG-265__ | 128MB | 16 Meg x 72 | 2.1 GB/s | 7.5ns/266 MT/s | 2.5-3-3 |

**Table 5: Part Numbers and Timing Parameters – 256MB Modules**

Base device: MT46V32M16,[1] 512Mb DDR SDRAM

| Part Number[2] | Module Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Clock Cycles (CL-$^{t}$RCD-$^{t}$RP) |
|---|---|---|---|---|---|
| MT5VDDT3272AG-40B__ | 256MB | 32 Meg x 72 | 3.2 GB/s | 5.0ns/400 MT/s | 3-3-3 |
| MT5VDDT3272AY-40B__ | 256MB | 32 Meg x 72 | 3.2 GB/s | 5.0ns/400 MT/s | 3-3-3 |
| MT5VDDT3272AG-335__ | 256MB | 32 Meg x 72 | 2.7 GB/s | 6.0ns/333 MT/s | 2.5-3-3 |
| MT5VDDT3272AY-335__ | 256MB | 32 Meg x 72 | 2.7 GB/s | 6.0ns/333 MT/s | 2.5-3-3 |
| MT5VDDT3272AG-265__ | 256MB | 32 Meg x 72 | 2.1 GB/s | 7.5ns/266 MT/s | 2.5-3-3 |

Notes:
1. Data sheets for the base devices can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT5VDDT1672AY-335F3.


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# Pin Assignments and Descriptions

**Table 6: Pin Assignments**

| 184-Pin DDR UDIMM Front | | | | | | | |
|---|---|---|---|---|---|---|---|
| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
| 1 | VREF | 24 | DQ17 | 47 | DQS8 | 70 | VDD |
| 2 | DQ0 | 25 | DQS2 | 48 | A0 | 71 | NC |
| 3 | VSS | 26 | VSS | 49 | CB2 | 72 | DQ48 |
| 4 | DQ1 | 27 | A9 | 50 | VSS | 73 | DQ49 |
| 5 | DQS0 | 28 | DQ18 | 51 | CB3 | 74 | VSS |
| 6 | DQ2 | 29 | A7 | 52 | BA1 | 75 | CK2# |
| 7 | VDD | 30 | VDDQ | 53 | DQ32 | 76 | CK2 |
| 8 | DQ3 | 31 | DQ19 | 54 | VDDQ | 77 | VDDQ |
| 9 | NC | 32 | A5 | 55 | DQ33 | 78 | DQS6 |
| 10 | NC | 33 | DQ24 | 56 | DQS4 | 79 | DQ50 |
| 11 | VSS | 34 | VSS | 57 | DQ34 | 80 | DQ51 |
| 12 | DQ8 | 35 | DQ25 | 58 | VSS | 81 | VSS |
| 13 | DQ9 | 36 | DQS3 | 59 | BA0 | 82 | NC |
| 14 | DQS1 | 37 | A4 | 60 | DQ35 | 83 | DQ56 |
| 15 | VDDQ | 38 | VDD | 61 | DQ40 | 84 | DQ57 |
| 16 | CK1 | 39 | DQ26 | 62 | VDDQ | 85 | VDD |
| 17 | CK1# | 40 | DQ27 | 63 | WE# | 86 | DQS7 |
| 18 | VSS | 41 | A2 | 64 | DQ41 | 87 | DQ58 |
| 19 | DQ10 | 42 | VSS | 65 | CAS# | 88 | DQ59 |
| 20 | DQ11 | 43 | A1 | 66 | VSS | 89 | VSS |
| 21 | CKE0 | 44 | CB0 | 67 | DQS5 | 90 | NC |
| 22 | VDDQ | 45 | CB1 | 68 | DQ42 | 91 | SDA |
| 23 | DQ16 | 46 | VDD | 69 | DQ43 | 92 | SCL |

| 184-Pin DDR UDIMM Back | | | | | | | |
|---|---|---|---|---|---|---|---|
| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
| 93 | VSS | 116 | VSS | 139 | VSS | 162 | DQ47 |
| 94 | DQ4 | 117 | DQ21 | 140 | DM8/ DQS17 | 163 | NC |
| 95 | DQ5 | 118 | A11 | 141 | A10 | 164 | VDDQ |
| 96 | VDDQ | 119 | DM2/ DQS11 | 142 | CB6 | 165 | DQ52 |
| 97 | DM0/ DQS9 | 120 | VDD | 143 | VDDQ | 166 | DQ53 |
| 98 | DQ6 | 121 | DQ22 | 144 | CB7 | 167 | NC |
| 99 | DQ7 | 122 | A8 | 145 | VSS | 168 | VDD |
| 100 | VSS | 123 | DQ23 | 146 | DQ36 | 169 | DM6/ DQS15 |
| 101 | NC | 124 | VSS | 147 | DQ37 | 170 | DQ54 |
| 102 | NC | 125 | A6 | 148 | VDD | 171 | DQ55 |
| 103 | NC | 126 | DQ28 | 149 | DM4/ DQS13 | 172 | VDDQ |
| 104 | VDDQ | 127 | DQ29 | 150 | DQ38 | 173 | NC |
| 105 | DQ12 | 128 | VDDQ | 151 | DQ39 | 174 | DQ60 |
| 106 | DQ13 | 129 | DM3/ DQS12 | 152 | VSS | 175 | DQ61 |
| 107 | DM1/ DQS10 | 130 | A3 | 153 | DQ44 | 176 | VSS |
| 108 | VDD | 131 | DQ30 | 154 | RAS# | 177 | DM7/ DQS16 |
| 109 | DQ14 | 132 | VSS | 155 | DQ45 | 178 | DQ62 |
| 110 | DQ15 | 133 | DQ31 | 156 | VDDQ | 179 | DQ63 |
| 111 | NC | 134 | CB4 | 157 | S0# | 180 | VDDQ |
| 112 | VDDQ | 135 | CB5 | 158 | NC | 181 | SA0 |
| 113 | NC | 136 | VDDQ | 159 | DM5/ DQS14 | 182 | SA1 |
| 114 | DQ20 | 137 | CK0 | 160 | VSS | 183 | SA2 |
| 115 | A12 | 138 | CK0# | 161 | DQ46 | 184 | VDDSPD |


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**Table 7: Pin Descriptions**

| Symbol | Type | Description |
|---|---|---|
| A0–A12 | Input | **Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command. A0–A11 (64MB) and A0–A12 (128MB, 256MB). |
| BA0, BA1 | Input | **Bank address:** BA0 and BA1 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. |
| CK0, CK0#,<br>CK1, CK1#,<br>CK2, CK2# | Input | **Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#. |
| CKE1 | Input | **Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates the internal clock, input buffers, and output drivers. |
| DM0–DM8<br>(DQS9–DQS17) | Input | **Data input mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. |
| RAS#, CAS#, WE# | Input | **Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered. |
| S0# | Input | **Chip selects:** S# (registered LOW) enables and (registered HIGH) disables the command decoder. |
| SA0–SA2 | Input | **Presence-detect address inputs:** These pins are used to configure the presence-detect device. |
| SCL | Input | **Serial clock for presence-detect:** SCL is used to synchronize the presence-detect data transfer to and from the module. |
| CB0–CB7 | I/O | Check bits. |
| DQ0–DQ63 | I/O | **Data input/output:** Data bus. |
| DQS0–DQS7 | I/O | **Data strobe:** Output with read data, input with write data. DQS is edge-aligned with read data, center-aligned with write data. Used to capture data. |
| SDA | I/O | **Serial presence-detect data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module. |
| $V_{DD}$/$V_{DD}Q$ | Supply | **Power supply:** +2.5V ±0.2V (-40B: +2.6V ±0.1V). |
| $V_{DDSPD}$ | Supply | **Serial EEPROM positive power supply:** +2.3V to +3.6V. |
| $V_{REF}$ | Supply | SSTL_2 reference voltage ($V_{DD}$/2). |
| $V_{SS}$ | Supply | Ground. |
| NC | – | **No connect:** These pins are not connected on the module. |


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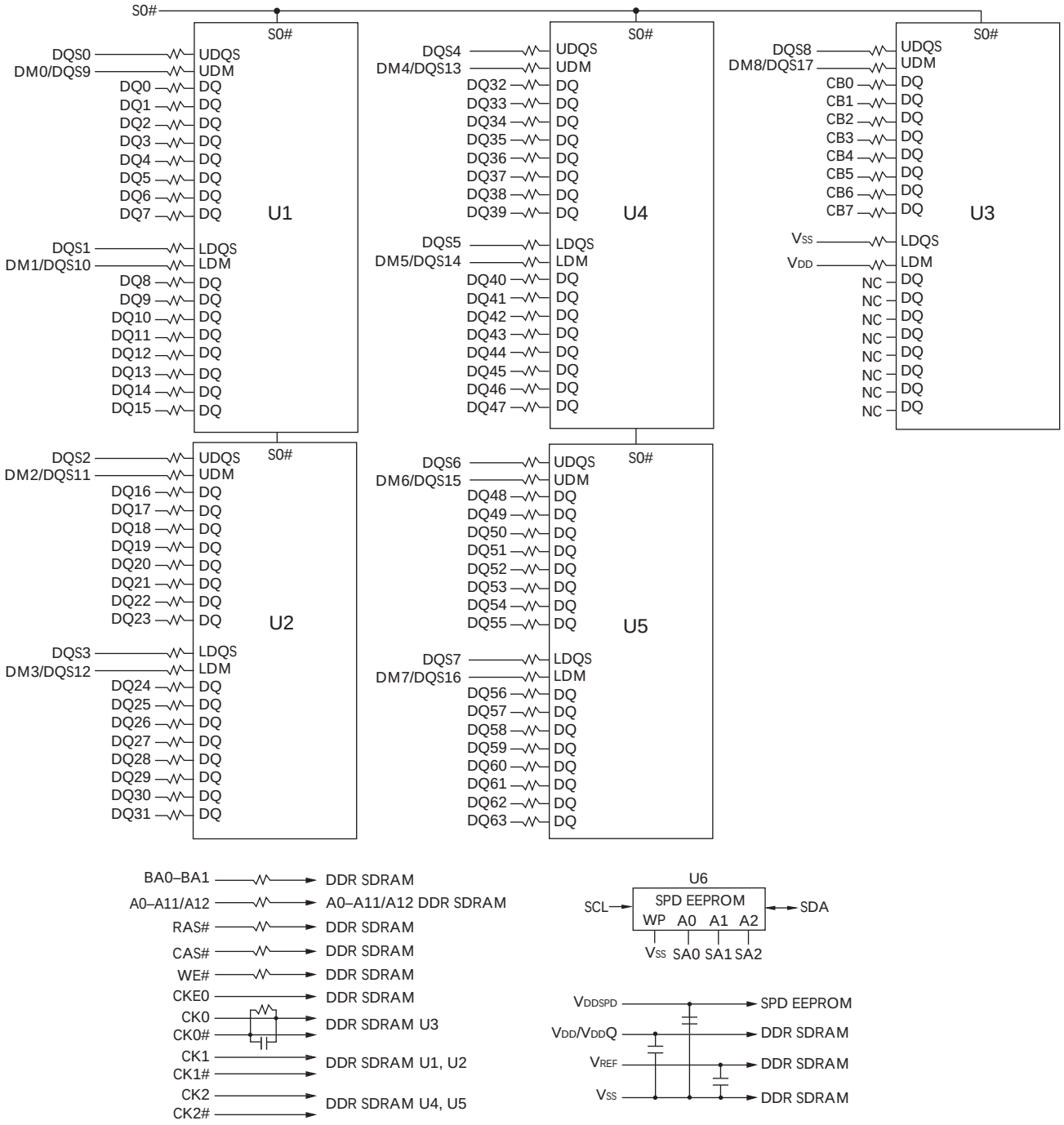
# Functional Block Diagram

**Figure 2: Functional Block Diagram**





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# General Description

The MT5VDDT872A, MT5VDDT1672A, and MT5VDDT3272A are high-speed CMOS, dynamic random access 64MB, 128MB, and 256MB memory modules organized in a x72 configuration. These modules use DDR SDRAM devices with four internal banks.

DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for DDR SDRAM modules effectively consists of a single 2*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR SDRAM modules operate from differential clock inputs (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

## Serial Presence-Detect Operation

DDR SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard $I^2C$ bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to $V_{SS}$ on the module, permanently disabling hardware write protect.


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# Electrical Specifications

Stresses greater than those listed in Table 8 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated on the device data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

**Table 8: Absolute Maximum Ratings**

| Symbol | Parameter | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{DD}/V_{DDQ}$ | $V_{DD}/V_{DDQ}$ supply voltage relative to $V_{SS}$ | | –1.0 | +3.6 | V |
| $V_{IN}$, $V_{OUT}$ | Voltage on any pin relative to $V_{SS}$ | | –0.5 | +3.2 | V |
| $I_I$ | Input leakage current; Any input $0V \le V_{IN} \le V_{DD}$; $V_{REF}$ input $0V \le V_{IN} \le 1.35V$ (All other pins not under test = 0V) | Address inputs, RAS#, CAS#, WE#, BA, S#, CKE | –10 | +10 | µA |
| | | CK0, CK0# | –2 | +2 | |
| | | CK1, CK1#, CK2, CK2# | –4 | +4 | |
| | | DM | –2 | +2 | |
| $I_{OZ}$ | Output leakage current; $0V \le V_{OUT} \le V_{DDQ}$; DQ are disabled | DQ, DQS | –5 | +5 | µA |
| $T_A$ | DRAM ambient operating temperature[1] | Commercial | 0 | +70 | °C |
| | | Industrial | –40 | +85 | °C |

Notes: 1. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.

## Input Capacitance

Micron encourages designers to simulate the performance of the module to achieve optimum values. Simulations are significantly more accurate and realistic than a gross estimation of module capacitance when inductance and delay parameters associated with trace lengths are used in simulations. JEDEC modules are currently designed using simulations to close timing budgets.

## Component AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 9.

**Table 9: Module and Component Speed Grades**

| Module Speed Grade | Component Speed Grade |
|---|---|
| -40B | -5B |
| -335 | -6 |
| -262 | -75E |
| -26A | -75Z |
| -265 | -75 |


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## IDD Specifications

**Table 10: IDD Specifications and Conditions – 64MB**
Values are shown for the MT46V8M16 DDR SDRAM only and are computed from values specified in the 128Mb (8 Meg x 16) component data sheet

| Parameter/Condition | | Symbol | -335 | -262 | -26A/ -265 | Units |
|---|---|---|---|---|---|---|
| **Operating one bank active-precharge current:** $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles | | IDD0 | 625 | 575 | 550 | mA |
| **Operating one bank active-read-precharge current:** BL = 2; $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle | | IDD1 | 675 | 675 | 625 | mA |
| **Precharge power-down standby current:** All device banks idle; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = LOW | | IDD2P | 15 | 15 | 15 | mA |
| **Idle standby current:** CS# = HIGH; All device banks idle; $^{t}CK = {}^{t}CK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; VIN = VREF for DQ, DQS, and DM | | IDD2F | 225 | 225 | 200 | mA |
| **Active power-down standby current:** One device bank active; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = LOW | | IDD3P | 125 | 125 | 100 | mA |
| **Active standby current:** CS# = HIGH; CKE = HIGH; One device bank active; $^{t}RC = {}^{t}RAS$ (MAX); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle | | IDD3N | 250 | 250 | 225 | mA |
| **Operating burst read current:** BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); IOUT = 0mA | | IDD4R | 725 | 700 | 675 | mA |
| **Operating burst write current:** BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle | | IDD4W | 775 | 675 | 650 | mA |
| **Auto refresh current** | $^{t}REFC = {}^{t}RFC$ (MIN) | IDD5 | 1,325 | 1,250 | 1,250 | mA |
| | $^{t}REFC$ = 15.625µs | IDD5A | 25 | 25 | 25 | mA |
| **Self refresh current:** CKE ≤ 0.2V | | IDD6 | 15 | 15 | 10 | mA |
| **Operating bank interleave read current:** Four device bank interleaving reads; BL = 4 with auto precharge; $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); Address and control inputs change only during active READ or WRITE commands | | IDD7 | 1,925 | 1,875 | 1,875 | mA |


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**Table 11: IDD Specifications and Conditions – 128MB**

Values are shown for the MT46V16M16 DDR SDRAM only and are computed from values specified in the 256Mb (16 Meg x 16) component data sheet

| Parameter/Condition | | Symbol | -40B | -335 | -262 | -26A/ -265 | Units |
|---|---|---|---|---|---|---|---|
| **Operating one bank active-precharge current:** $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles | | IDD0 | 675 | 625 | 625 | 600 | mA |
| **Operating one bank active-read-precharge current:** BL = 2; $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle | | IDD1 | 925 | 900 | 850 | 775 | mA |
| **Precharge power-down standby current:** All device banks idle; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = LOW | | IDD2P | 20 | 20 | 20 | 20 | mA |
| **Idle standby current:** CS# = HIGH; All device banks idle; $^{t}CK = {}^{t}CK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; VIN = VREF for DQ, DQS, and DM | | IDD2F | 300 | 250 | 225 | 225 | mA |
| **Active power-down standby current:** One device bank active; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = LOW | | IDD3P | 200 | 150 | 125 | 125 | mA |
| **Active standby current:** CS# = HIGH; CKE = HIGH; One device bank active; $^{t}RC = {}^{t}RAS$ (MAX); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle | | IDD3N | 350 | 300 | 250 | 250 | mA |
| **Operating burst read current:** BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); IOUT = 0mA | | IDD4R | 1,300 | 1,100 | 925 | 925 | mA |
| **Operating burst write current:** BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle | | IDD4W | 1,075 | 975 | 800 | 800 | mA |
| **Auto refresh current** | $^{t}REFC = {}^{t}RFC$ (MIN) | IDD5 | 1,300 | 1,275 | 1,175 | 1,175 | mA |
| | $^{t}REFC$ = 7.8125µs | IDD5A | 30 | 30 | 30 | 30 | mA |
| **Self refresh current:** CKE ≤ 0.2V | | IDD6 | 20 | 20 | 20 | 20 | mA |
| **Operating bank interleave read current:** Four device bank interleaving reads; BL = 4 with auto precharge; $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); Address and control inputs change only during active READ or WRITE commands | | IDD7 | 2,550 | 2,200 | 1,900 | 1,900 | mA |


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**Table 12: IDD Specifications and Conditions – 256MB**

Values are shown for the MT46V32M16 DDR SDRAM only and are computed from values specified in the 512Mb (32 Meg x 16) component data sheet

| Parameter/Condition | | Symbol | -40B | -335 | -265 | Units |
|---|---|---|---|---|---|---|
| **Operating one bank active-precharge current:** $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles | | IDD0 | 775 | 650 | 575 | mA |
| **Operating one bank active-read-precharge current:** BL = 2; $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle | | IDD1 | 975 | 800 | 725 | mA |
| **Precharge power-down standby current:** All device banks idle; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = LOW | | IDD2P | 25 | 25 | 25 | mA |
| **Idle standby current:** CS# = HIGH; All device banks idle; $^{t}CK = {}^{t}CK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; VIN = VREF for DQ, DQS, and DM | | IDD2F | 275 | 225 | 200 | mA |
| **Active power-down standby current:** One device bank active; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = LOW | | IDD3P | 225 | 175 | 150 | mA |
| **Active standby current:** CS# = HIGH; CKE = HIGH; One device bank active; $^{t}RC = {}^{t}RAS$ (MAX); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle | | IDD3N | 300 | 250 | 225 | mA |
| **Operating burst read current:** BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); IOUT = 0mA | | IDD4R | 1,050 | 825 | 725 | mA |
| **Operating burst write current:** BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle | | IDD4W | 1,075 | 975 | 675 | mA |
| **Auto refresh current** | $^{t}REFC = {}^{t}RFC$ (MIN) | IDD5 | 1,725 | 1,450 | 1,400 | mA |
| | $^{t}REFC$ = 7.8125µs | IDD5A | 55 | 50 | 50 | mA |
| **Self refresh current:** CKE ≤ 0.2V | | IDD6 | 30 | 25 | 25 | mA |
| **Operating bank interleave read current:** Four device bank interleaving reads; BL = 4 with auto precharge; $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); Address and control inputs change only during active READ or WRITE commands | | IDD7 | 2,400 | 2,025 | 1,750 | mA |


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# Serial Presence-Detect

**Table 13: Serial Presence-Detect EEPROM DC Operating Conditions**

| Parameter/Condition | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Supply voltage | $V_{DDSPD}$ | 2.3 | 3.6 | V |
| Input high voltage: Logic 1; All inputs | $V_{IH}$ | $V_{DDSPD}$ × 0.7 | $V_{DDSPD}$ + 0.5 | V |
| Input low voltage: Logic 0; All inputs | $V_{IL}$ | –1.0 | $V_{DDSPD}$ × 0.3 | V |
| Output low voltage: $I_{OUT}$ = 3mA | $V_{OL}$ | – | 0.4 | V |
| Input leakage current: $V_{IN}$ = GND to $V_{DD}$ | $I_{LI}$ | – | 10 | µA |
| Output leakage current: $V_{OUT}$ = GND to $V_{DD}$ | $I_{LO}$ | – | 10 | µA |
| Standby current: SCL = SDA = $V_{DD}$ - 0.3V; All other inputs = $V_{SS}$ or $V_{DD}$ | $I_{SB}$ | – | 30 | µA |
| Power supply current: SCL clock frequency = 100 kHz | $I_{CC}$ | – | 2.0 | mA |

**Table 14: Serial Presence-Detect EEPROM AC Operating Conditions**

| Parameter/Condition | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| SCL LOW to SDA data-out valid | $^{t}AA$ | 0.2 | 0.9 | µs | 1 |
| Time the bus must be free before a new transition can start | $^{t}BUF$ | 1.3 | – | µs | |
| Data-out hold time | $^{t}DH$ | 200 | – | ns | |
| SDA and SCL fall time | $^{t}F$ | – | 300 | ns | 2 |
| Data-in hold time | $^{t}HD:DAT$ | 0 | – | µs | |
| Start condition hold time | $^{t}HD:STA$ | 0.6 | – | µs | |
| Clock HIGH period | $^{t}HIGH$ | 0.6 | – | µs | |
| Noise suppression time constant at SCL, SDA inputs | $^{t}I$ | – | 50 | ns | |
| Clock LOW period | $^{t}LOW$ | 1.3 | – | µs | |
| SDA and SCL rise time | $^{t}R$ | – | 0.3 | µs | 2 |
| SCL clock frequency | $^{f}SCL$ | – | 400 | kHz | |
| Data-in setup time | $^{t}SU:DAT$ | 100 | – | ns | |
| Start condition setup time | $^{t}SU:STA$ | 0.6 | – | µs | 3 |
| Stop condition setup time | $^{t}SU:STO$ | 0.6 | – | µs | |
| WRITE cycle time | $^{t}WRC$ | – | 10 | ms | 4 |

Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time ($^{t}WRC$) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

## Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.


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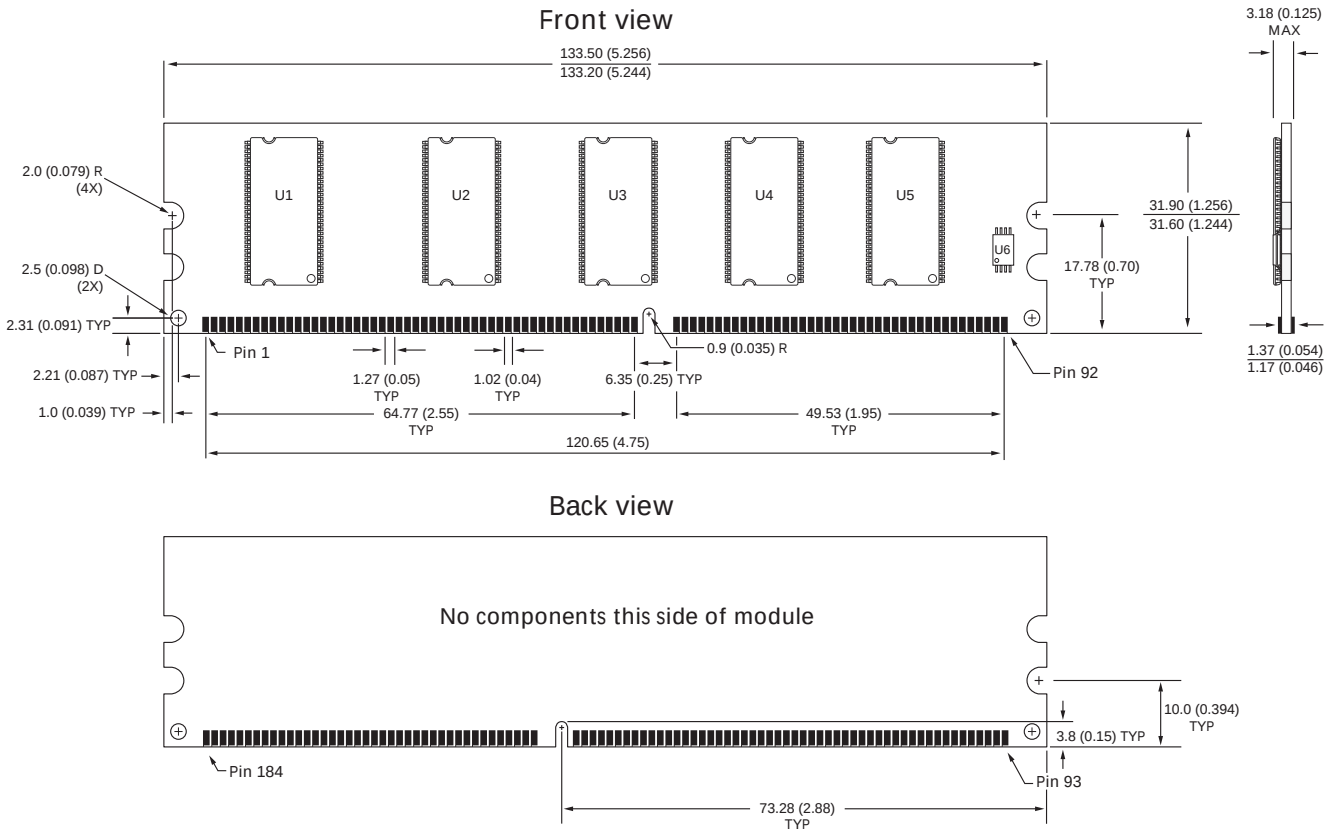
# Module Dimensions

**Figure 3: 184-Pin DDR UDIMM**




Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.

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**This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.**


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