DDR3 SDRAM UDIMM

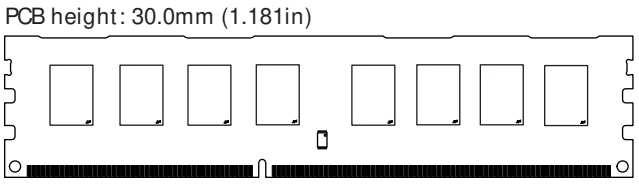
MT8JTF12864A – 1GB
MT8JTF25664A – 2GB

For component data sheets, refer to Micron's Web site: www.micron.com

Features

- DDR3 functionality and operations supported as defined in the component data sheet
- 240-pin, unbuffered dual in-line memory module (UDIMM)
- Fast data transfer rates: PC3-12800, PC3-10600 PC3-8500 or PC3-6400
- 1GB (128 Meg x 64), 2GB (256 Meg x 64)
- Vdd = Vddq = +1.5V ±0.075V
- Vddspd = +3.0V to +3.6V
- Reset pin for improved system stability
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Single rank
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Adjustable data-output drive strength
- Serial presence-detect (SPD) EEPROM
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

Figure 1: 240-Pin UDIMM (MO-269 R/C A)



Options	Marking
• Operating temperature[1]	
– Commercial (0°C ≤ T_A ≤ +70°C)	None
– Industrial (–40°C ≤ T_A ≤ +85°C)	I
• Package	
– 240-pin DIMM (halogen-free)	Z
• Frequency/CAS latency	
– 1.25ns @CL = 11 (DDR3-1600)[3]	-1G6
– 1.5ns @CL = 9 (DDR3-1333)	-1G4
– 1.87ns @CL = 7 (DDR3-1066)	-1G1
– 1.87ns @CL = 8 (DDR3-1066)[2]	-1G0
– 2.5ns @CL = 5 (DDR3-800)[2]	-80C
– 2.5ns @CL = 6 (DDR3-800)[2]	-80B

Notes: 1. Contact Micron for industrial temperature module offerings.
2. Not recommended for new designs.
3. Not available for 2GB modules.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)							^tRCD (ns)	^tRP (ns)	^tRC (ns)
		CL=11	CL = 10	CL = 9	CL = 8	CL = 7	CL = 6	CL = 5			
-1G6	PC3-12800	1600	1333	–	1066	–	800	–	13.75	13.75	48.75
-1G4	PC3-10600		1333	1333	1066	1066	800	–	13.5	13.5	49.5
-1G1	PC3-8500		–	–	1066	1066	800	–	13.125	13.125	50.625
-1G0	PC3-8500		–	–	1066	–	800	–	15	15	52.5
-80C	PC3-6400		–	–	–	–	800	800	12.5	12.5	50
-80B	PC3-6400		–	–	–	–	800	–	15	15	52.5

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Table 2: Addressing

Parameter	1GB	2GB
Refresh count	8K	8K
Row address	16K A[13:0]	32K A[14:0]
Device bank address	8 BA[2:0]	8 BA[2:0]
Device configuration	1Gb (128 Meg x 8)	2Gb (256 Meg x 8)
Column address	1K A[9:0]	1K A[9:0]
Module rank address	1 (S0#)	1 (S0#)

Table 3: Part Numbers and Timing Parameters – 1GB Modules

Base device: MT41J128M8,[1] 1Gb DDR3 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT8JTF12864A(I)Z-1G6__	1GB	128 Meg x 64	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT8JTF12864A(I)Z-1G4__	1GB	128 Meg x 64	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT8JTF12864A(I)Z-1G1__	1GB	128 Meg x 64	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

Table 4: Part Numbers and Timing Parameters – 2GB Modules

Base device: MT41J256M8,[1] 2Gb DDR3 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT8JTF25664A(I)Z-1G4__	2GB	256 Meg x 64	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT8JTF25664A(I)Z-1G1__	2GB	256 Meg x 64	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

Notes:
1. Data sheets for the base device parts can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT8JTF12864AY-1G1D1.

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Pin Assignments and Descriptions

Table 5: Pin Assignments

240-Pin DDR3 UDIMM Front								240-Pin DDR3 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vrefdq	31	DQ25	61	A2	91	DQ41	121	Vss	151	Vss	181	A1	211	Vss
2	Vss	32	Vss	62	Vdd	92	Vss	122	DQ4	152	DM3	182	Vdd	212	DM5
3	DQ0	33	DQS3#	63	NU	93	DQS5#	123	DQ5	153	NC	183	Vdd	213	NC
4	DQ1	34	DQS3	64	NU	94	DQS5	124	Vss	154	Vss	184	CK0	214	Vss
5	Vss	35	Vss	65	Vdd	95	Vss	125	DM0	155	DQ30	185	CK0#	215	DQ46
6	DQS0#	36	DQ26	66	Vdd	96	DQ42	126	NC	156	DQ31	186	Vdd	216	DQ47
7	DQS0	37	DQ27	67	Vrefca	97	DQ43	127	Vss	157	Vss	187	NC	217	Vss
8	Vss	38	Vss	68	NC	98	Vss	128	DQ6	158	NC	188	A0	218	DQ52
9	DQ2	39	NC	69	Vdd	99	DQ48	129	DQ7	159	NC	189	Vdd	219	DQ53
10	DQ3	40	NC	70	A10	100	DQ49	130	Vss	160	Vss	190	BA1	220	Vss
11	Vss	41	Vss	71	BA0	101	Vss	131	DQ12	161	NC	191	Vdd	221	DM6
12	DQ8	42	NC	72	Vdd	102	DQS6#	132	DQ13	162	NC	192	RAS#	222	NC
13	DQ9	43	NC	73	WE#	103	DQS6	133	Vss	163	Vss	193	S0#	223	Vss
14	Vss	44	Vss	74	CAS#	104	Vss	134	DM1	164	NC	194	Vdd	224	DQ54
15	DQS1#	45	NC	75	Vdd	105	DQ50	135	NC	165	NC	195	ODT0	225	DQ55
16	DQS1	46	NC	76	NC	106	DQ51	136	Vss	166	Vss	196	A13	226	Vss
17	Vss	47	Vss	77	NC	107	Vss	137	DQ14	167	NC	197	Vdd	227	DQ60
18	DQ10	48	NC	78	Vdd	108	DQ56	138	DQ15	168	RESET#	198	NC	228	DQ61
19	DQ11	49	NC	79	NC	109	DQ57	139	Vss	169	NC	199	Vss	229	Vss
20	Vss	50	CKE0	80	Vss	110	Vss	140	DQ20	170	Vdd	200	DQ36	230	DM7
21	DQ16	51	Vdd	81	DQ32	111	DQS7#	141	DQ21	171	NC	201	DQ37	231	NC
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	Vss	172	NC/A14[1]	202	Vss	232	Vss
23	Vss	53	NC	83	Vss	113	Vss	143	DM2	173	Vdd	203	DM4	233	DQ62
24	DQS2#	54	Vdd	84	DQS4#	114	DQ58	144	NC	174	A12	204	NC	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQ59	145	Vss	175	A9	205	Vss	235	Vss
26	Vss	56	A7	86	Vss	116	Vss	146	DQ22	176	Vdd	206	DQ38	236	Vddspd
27	DQ18	57	Vdd	87	DQ34	117	SA0	147	DQ23	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	Vss	178	A6	208	Vss	238	SDA
29	Vss	59	A4	89	Vss	119	SA2	149	DQ28	179	Vdd	209	DQ44	239	Vss
30	DQ24	60	Vdd	90	DQ40	120	Vtt	150	DQ29	180	A3	210	DQ45	240	Vtt

Notes: 1. Pin 172 is NC for 1GB modules and A14 for 2GB modules.

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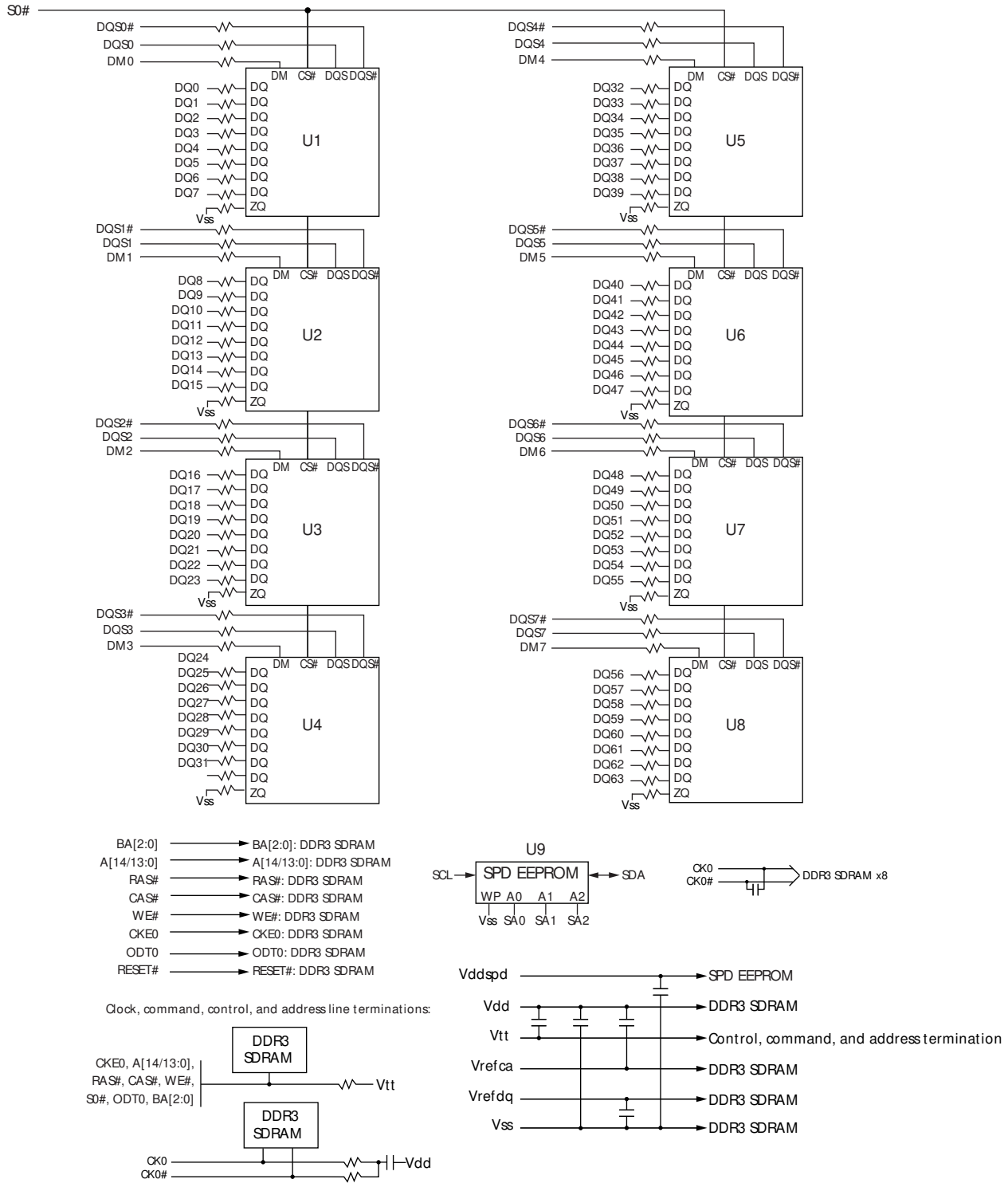
Table 6: Pin Descriptions

Symbol	Type	Description
A[14:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also used for BC4/BL8 identification as "BL on-the-fly" during CAS commands. The address inputs also provide the op-code during the mode register command set. A[13:0] address the 1GB devices; A[14:0] address the 2GB devices.
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the device bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command.
CK0, CK0#	Input	**Clock:** CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKE0	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DM[7:0]	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of the DQ and DQS pins.
ODT0	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to Vss. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 x Vdd and DC LOW ≤ 0.2 x Vdd.
SA[2:0]	Input	**Serial address inputs:** These pins are used to configure the SPD EEPROM address range.
SCL	Input	**Serial clock for presence-detect:** SCL is used to synchronize communication to and from the SPD EEPROM.
S0#	Input	Chip select: S# enables (registered LOW) and disables (registered HIGH) the command decoder.
DQ[63:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[7:0], DQS#[7:0]	I/O	**Data strobe:** DQS and DQS# are differential data strobes. Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data. DQS# is only used when the differential data strobe mode is enabled via the LOAD MODE command.
SDA	I/O	**Serial data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the SPD EEPROM on the module.
Vdd	Supply	**Power supply:** 1.5V ±0.075V. The component Vdd and Vddq are connected to the module Vdd.
Vddspd	Supply	**Temperature sensor/SPD EEPROM power supply:** +3.0V to +3.6V.
Vrefdq	Supply	**Reference voltage:** DQ, DM (Vdd/2).
Vrefca	Supply	**Reference voltage:** Control, command, and address (Vdd/2).
Vss	Supply	Ground.
Vtt	Supply	**Termination voltage:** Used for control, command, and address (Vdd/2).
NC	–	**No connect:** These pins are not connected on the module.
NU	–	**Not used:** These pins are not used in specific module configuration/operations.

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Functional Block Diagram

Figure 2: Functional Block Diagram



Notes: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

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General Description

The MT8JTF12864A and MT8JTF25664A DDR3 SDRAM modules are high-speed, CMOS dynamic random access 1GB and 2GB memory modules organized in a x64 configuration. These DDR3 SDRAM modules use internally configured, 8-bank 1Gb and 2Gb DDR3 SDRAM devices.

DDR3 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR3 SDRAM input receiver. DQS is center-aligned with data for WRITEs. The read data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes.

DDR3 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Fly-By Topology

These DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by utilizing the write-leveling feature of DDR3.

Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC standard JC-45 "Appendix X: Serial Presence Detect (SPD) for DDR3 SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. User-specific information can be written into the remaining 128 bytes of storage. READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA[2:0], which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is connected to Vss, permanently disabling hardware write protect.

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Electrical Specifications

Stresses greater than those listed in Table 7, may cause permanent damage to the DRAM devices on the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 7: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Units
Vdd[1]	Vdd supply voltage relative to Vss		–0.4	+1.975	V
Vin, Vout	Voltage on any pin relative to Vss		–0.4	+1.975	V
Ii	Input leakage current; Any input 0V ≤ Vin ≤ Vdd; Vref input 0V ≤ Vin ≤ 0.95V (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, S#, CKE, ODT, BA, CK, CK#	–16	+16	µA
		DM	–2	+2	
Ioz	Output leakage current; 0V ≤ Vout ≤ Vddq; DQ and ODT are disabled	DQ, DQS, DQS#	–5	+5	µA
Ivref	Vref leakage current; Vref = valid Vref level		–8	+8	µA

Notes: 1. Vref must not be greater than 0.6 x Vdd. When Vdd is less than 500mV, Vref may be equal to or less than 300mV.

Table 8: Operating Conditions

Symbol	Parameter		Min	Max	Units
Ivtt	Termination reference current from Vtt		–600	+600	mA
Vtt[1]	Termination reference voltage – command address bus		–0.483 × Vdd	+0.517 × Vdd	V
T_A[2,4]	Module ambient operating temperature	Commercial	0	+70	°C
		Industrial	–40	+85	°C
T_C[2,4]	DDR3 SDRAM component case operating temperature[3]	Commercial	0	+85	°C
		Industrial	–40	+95	°C

Notes:
1. Vtt termination voltage in excess of stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
2. T_A and T_C are simultaneous requirements.
3. The refresh rate is required to double when 85°C < T_C ≤ 95°C.
4. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.

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DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR3 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 9.

Table 9: Module and Component Speed Grades
DDR3 components may exceed the listed module speed grades

Module Speed Grade	Component Speed Grade
-1G6	-125
-1G4	-15E
-1G1	-187E
-1G0	-187
-80C	-25E
-80B	-25

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

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Idd Specifications

Table 10: DDR3 Idd Specifications and Conditions – 1GB
Values are for the MT41J128M8 DDR3 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter	Symbol	1600	1333	1066	800	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	Idd0	960	880	800	720	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	Idd1	1120	1040	960	880	mA
Precharge power-down current: Slow exit	Idd2P	80	80	80	80	mA
Precharge power-down current: Fast exit	Idd2P	200	200	200	200	mA
Precharge quiet standby current	Idd2Q	440	400	360	320	mA
Precharge standby current	Idd2N	480	440	400	360	mA
Active power-down current	Idd3P	320	280	240	200	mA
Active standby current	Idd3N	520	480	440	400	mA
Burst read operating current	Idd4R	2000	1600	1280	1040	mA
Burst write operating current	Idd4W	1800	1520	1280	1040	mA
Refresh current	Idd5B	2080	1920	1760	1600	mA
Self refresh temperature current: MAX T_C = 85°C	Idd6	48	48	48	48	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	Idd6ET	72	72	72	72	mA
All banks interleaved read current	Idd7	4800	3920	3120	2800	mA

Table 11: DDR3 Idd Specifications and Conditions – 2GB
Values are for the MT41J256M8 DDR3 SDRAM only and are computed from values specified in the 2Gb (256 Meg x 8) component data sheet

Parameter	Symbol	1333	1066	800	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	Idd0	1040	960	800	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	Idd1	1240	1080	920	mA
Precharge power-down current: Slow exit	Idd2P	80	80	80	mA
Precharge power-down current: Fast exit	Idd2P	200	200	200	mA
Precharge quiet standby current	Idd2Q	560	480	400	mA
Precharge standby current	Idd2N	560	480	400	mA
Active power-down current	Idd3P	480	400	360	mA
Active standby current	Idd3N	720	600	520	mA
Burst read operating current	Idd4R	2040	1800	1560	mA
Burst write operating current	Idd4W	2400	2120	1840	mA
Refresh current	Idd5B	2440	2320	2200	mA
Self refresh temperature current: MAX T_C = 85°C	Idd6	72	72	72	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	Idd6ET	96	96	96	mA
All banks interleaved read current	Idd7	3680	3440	3200	mA

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Serial Presence-Detect

Table 12: Serial Presence-Detect EEPROM DC Operating Conditions
All voltages referenced to Vss

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	Vddspd	3.0	3.6	V
Input high voltage: Logic 1; All inputs	Vih	Vddspd × 0.7	Vddspd + 0.5	V
Input low voltage: Logic 0; All inputs	Vil	–0.6	Vddspd × 0.3	V
Output low voltage: Iout = 3mA	Vol	–	0.4	V
Input leakage current: Vin = GND to Vdd	Ili	0.10	3	µA
Output leakage current: Vout = GND to Vdd	Ilo	0.05	3	µA
Standby current	Isb	1.6	4	µA
Power supply current, READ: SCL clock frequency = 100 kHz	Iccr	0.4	1	mA
Power supply current, WRITE: SCL clock frequency = 100 kHz	Iccw	2	3	mA

Table 13: Serial Presence-Detect EEPROM AC Operating Conditions
All voltages referenced to Vss

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^{t}BUF	1.3	–	µs	
Data-out hold time	^{t}DH	200	–	ns	
SDA and SCL fall time	^{t}F	–	300	ns	2
Data-in hold time	^{t}HD:DAT	0	–	µs	
Start condition hold time	^{t}HD:STA	0.6	–	µs	
Clock HIGH period	^{t}HIGH	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I	–	50	ns	
Clock LOW period	^{t}LOW	1.3	–	µs	
SDA and SCL rise time	^{t}R	–	0.3	µs	2
SCL clock frequency	^{f}SCL	–	400	kHz	
Data-in setup time	^{t}SU:DAT	100	–	ns	
Start condition setup time	^{t}SU:STA	0.6	–	µs	3
Stop condition setup time	^{t}SU:STO	0.6	–	µs	
WRITE cycle time	^{t}WRC	–	10	ms	4

Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

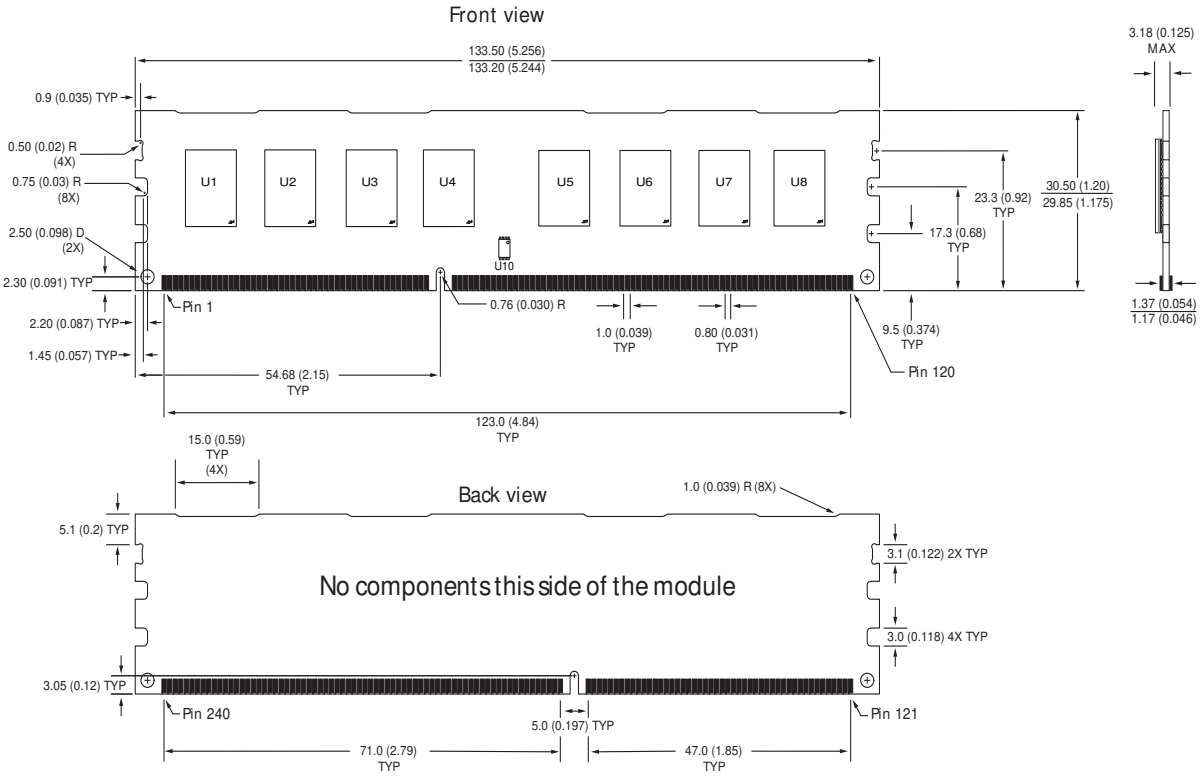
Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.

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Module Dimensions

Figure 3: 240-Pin DDR3 UDIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

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