DDR2 SDRAM FBDIMM

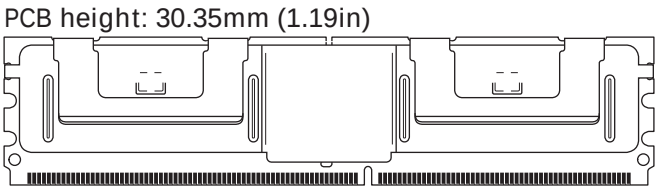
MT9HTF6472F – 512MB
MT9HTF12872F – 1GB

For the component data sheet, refer to Micron's Web site: www.micron.com

Features

- 240-pin, DDR2 fully-buffered dual in-line memory module (FBDIMM)
- Fast data transfer rates: PC2-4200, PC2-5300, or PC2-6400
- 512MB (64 Meg x 72), 1GB (128 Meg x 72)
- 3.2 Gb/s, 4.0 Gb/s, and 4.8 Gb/s link transfer rates
- High-speed, 1.5V differential, point-to-point link between the host controller and advanced memory buffer (AMB)
- Fault tolerant; can work around a bad bit lane in each direction
- High-density scaling with up to eight FBDIMMs per channel
- SMBus interface to AMB for configuration register access
- In-band and out-of-band command access
- Deterministic protocol
  - Enables memory controller to optimize DRAM accesses for maximum performance
  - Delivers precise control and repeatable memory behavior
- Automatic DDR2 SDRAM bus and channel calibration
- Transmitter de-emphasis to reduce ISI
- MBIST and IBIST test functions
- Transparent mode for DRAM test support

Figure 1: 240-Pin FBDIMM (MO-256 R/C A)



Features (continued)

- V_{DD} = $V_{DD}Q$ = +1.8V for DRAM
- V_{REF} = 0.9V SDRAM command and address termination
- V_{CC} = 1.5V for AMB
- V_{DDSPD} = +3.0V to +3.6V for AMB and EEPROM
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts
- Single rank
- Supports 95°C operation with 2X refresh

Options	Marking
• Package	
– 240-pin DIMM (Pb-free)	Y
• Frequency/CAS latency	
– 2.5ns @ CL = 5 (DDR2-800)	-80E
– 3.0ns @ CL = 5 (DDR2-667)	-667
– 3.75ns @ CL = 4 (DDR2-533)[1]	-53E

Notes: 1. Not recommended for new designs.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)			t_{RCD} (ns)	t_{RP} (ns)	t_{RC} (ns)
		CL = 5	CL = 4	CL = 3			
-80E	PC2-6400	800	533	–	12.5	12.5	55
-667	PC2-5300	667	533	400	15	15	55
-53E	PC2-4200	–	533	400	15	15	55

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Table 2: Addressing

Parameter	512MB	1GB
Refresh count	8K	8K
Device bank address	4 (BA0, BA1)	8 (BA0–BA2)
Device page size per bank	1KB	1KB
Device configuration	512Mb (64 Meg x 8)	1Gb (128 Meg x 8)
Row address	16K (A0–A13)	16K (A0–A13)
Column address	1K (A0–A9)	1K (A0–A9)
Module rank address	1 (S0#)	1 (S0#)

Table 3: Part Numbers and Timing Parameters – 512MB

Base device: MT47H64M8,[1] 512Mb DDR2 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)	Link Transfer Rate
MT9HTF6472FY-80E__	512MB	64 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5	4.8 GT/s
MT9HTF6472FY-667__	512MB	64 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5	4.0 GT/s
MT9HTF6472FY-53E__	512MB	64 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4	3.2 GT/s

Table 4: Part Numbers and Timing Parameters – 1GB

Base device: MT47H128M8,[1] 1Gb DDR2 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)	Link Transfer Rate
MT9HTF12872FY-80E__	1GB	128 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5	4.8 GT/s
MT9HTF12872FY-667__	1GB	128 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5	4.0 GT/s
MT9HTF12872FY-53E__	1GB	128 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4	3.2 GT/s

Notes:
1. Data sheets for the base devices can be found on Micron's Web page.
2. All part numbers end with a four-place code (not shown) that designates component, PCB, and AMB revisions. Consult factory for current revision codes. Example: MT9HTF12872FY-667E1D4.

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Pin Assignments and Descriptions

Table 5: Pin Assignments

240-Pin FBDIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VDD	31	PN3	61	PN9#	91	PS9#[1]
2	VDD	32	PN3#	62	VSS	92	VSS
3	VDD	33	VSS	63	PN10	93	PS5
4	VSS	34	PN4	64	PN10#	94	PS5#
5	VDD	35	PN4#	65	VSS	95	VSS
6	VDD	36	VSS	66	PN11	96	PS6
7	VDD	37	PN5	67	PN11#	97	PS6#
8	VSS	38	PN5#	68	VSS	98	VSS
9	VCC	39	VSS	69	VSS	99	PS7
10	VCC	40	PN13[1]	70	PS0	100	PS7#
11	VSS	41	PN13#[1]	71	PS0#	101	VSS
12	VCC	42	VSS	72	VSS	102	PS8
13	VCC	43	VSS	73	PS1	103	PS8#
14	VSS	44	DNU	74	PS1#	104	VSS
15	VTT	45	DNU	75	VSS	105	DNU
16	DNU	46	VSS	76	PS2	106	DNU
17	RESET#	47	VSS	77	PS2#	107	VSS
18	VSS	48	PN12[1]	78	VSS	108	VDD
19	DNU	49	PN12#[1]	79	PS3	109	VDD
20	DNU	50	VSS	80	PS3#	110	VSS
21	VSS	51	PN6	81	VSS	111	VDD
22	PN0	52	PN6#	82	PS4	112	VDD
23	PN0#	53	VSS	83	PS4#	113	VDD
24	VSS	54	PN7	84	VSS	114	VSS
25	PN1	55	PN7#	85	VSS	115	VDD
26	PN1#	56	VSS	86	DNU	116	VDD
27	VSS	57	PN8	87	DNU	117	VTT
28	PN2	58	PN8#	88	VSS	118	SA2
29	PN2#	59	VSS	89	VSS	119	SDA
30	VSS	60	PN9	90	PS9[1]	120	SCL

240-Pin FBDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
121	VDD	151	SN3	181	SN9#	211	SS9#[1]
122	VDD	152	SN3#	182	VSS	212	VSS
123	VDD	153	VSS	183	SN10	213	SS5
124	VSS	154	SN4	184	SN10#	214	SS5#
125	VDD	155	SN4#	185	VSS	215	VSS
126	VDD	156	VSS	186	SN11	216	SS6
127	VDD	157	SN5	187	SN11#	217	SS6#
128	VSS	158	SN5#	188	VSS	218	VSS
129	VCC	159	VSS	189	VSS	219	SS7
130	VCC	160	SN13[1]	190	SS0	220	SS7#
131	VSS	161	SN13#[1]	191	SS0#	221	VSS
132	VCC	162	VSS	192	VSS	222	SS8
133	VCC	163	VSS	193	SS1	223	SS8#
134	VSS	164	DNU	194	SS1#	224	VSS
135	VTT	165	DNU	195	VSS	225	DNU
136	DNU	166	VSS	196	SS2	226	DNU
137	M_TEST (DNU)	167	VSS	197	SS2#	227	VSS
138	VSS	168	SN12[1]	198	VSS	228	SCK
139	DNU	169	SN12#[1]	199	SS3	229	SCK#
140	DNU	170	VSS	200	SS3#	230	VSS
141	VSS	171	SN6	201	VSS	231	VDD
142	SN0	172	SN6#	202	SS4	232	VDD
143	SN0#	173	VSS	203	SS4#	233	VDD
144	VSS	174	SN7	204	VSS	234	VSS
145	SN1	175	SN7#	205	VSS	235	VDD
146	SN1#	176	VSS	206	DNU	236	VDD
147	VSS	177	SN8	207	DNU	237	VTT
148	SN2	178	SN8#	208	VSS	238	VDDSPD
149	SN2#	179	VSS	209	VSS	239	SA0
150	VSS	180	SN9	210	SS9[1]	240	SA1

Notes: 1. The following signals are cyclical redundancy code (CRC) bits and thus appear out of the normal sequence: PN12/PN12#, SN12/SN12#, PN13/PN13#, SN13/SN13#, PS9/PS9#, SS9/SS9#.

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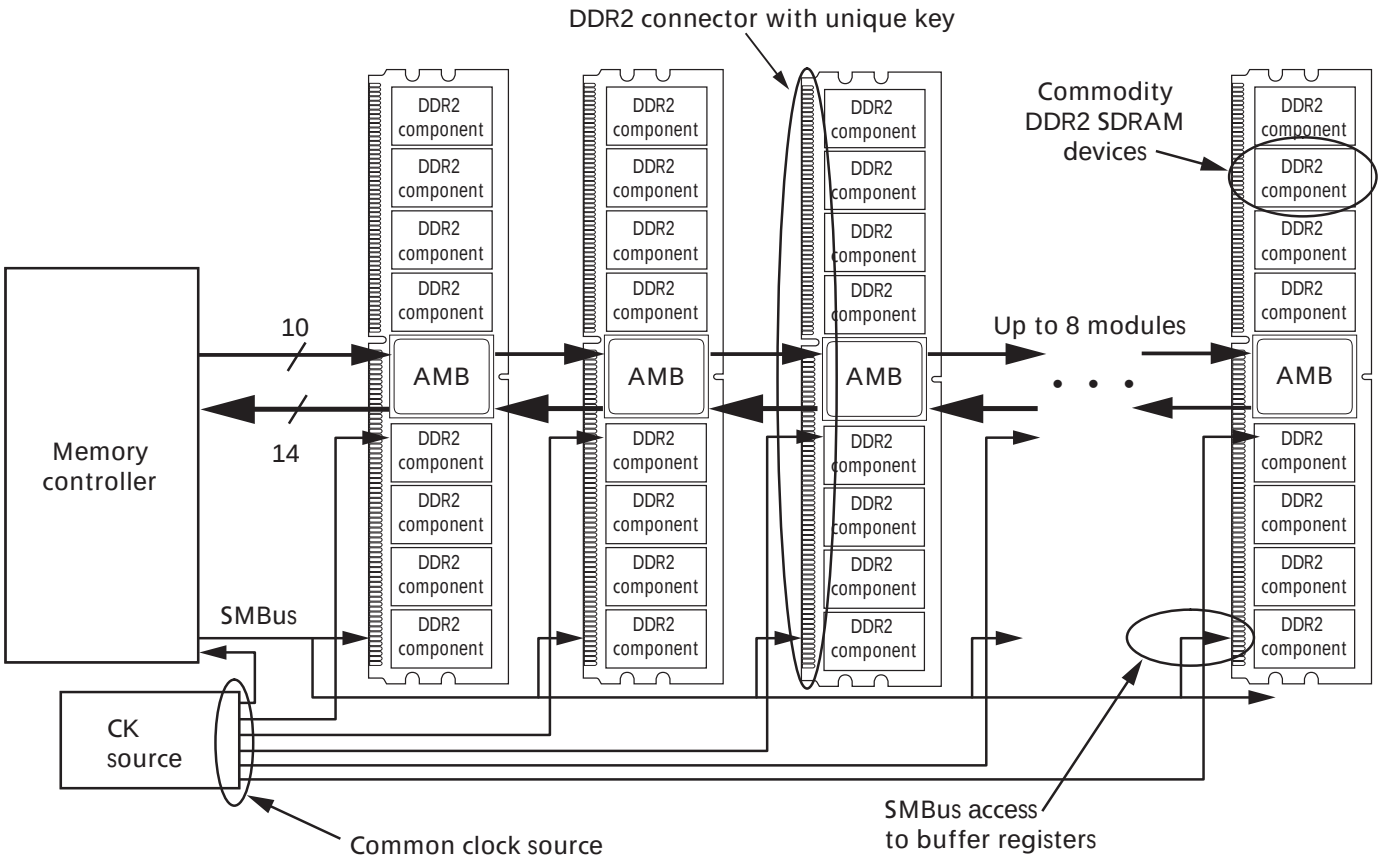
Table 6: Pin Descriptions

Symbol	Type	Description
PS0–PS9	Input	Primary southbound data, positive lines.
PS0#–PS9#	Input	Primary southbound data, negative lines.
SCK	Input	System clock input, positive line.
SCK#	Input	System clock Input, negative line.
SCL	Input	Serial presence-detect (SPD) clock input.
SS0–SS9	Input	Secondary southbound data, positive lines.
SS0#–SS9#	Input	Secondary southbound data, negative lines.
PN0–PN13	Output	Primary northbound data, positive lines.
PN0#–PN13#	Output	Primary northbound data, negative lines.
SN0–SN13	Output	Secondary northbound data, positive lines.
SN0#–SN13#	Output	Secondary northbound data, negative lines.
SA0–SA2	I/O	SPD address inputs, also used to select the FBDIMM number in the AMB.
SDA	I/O	SPD data input/output.
RESET#	Supply	AMB reset signal.
V_{CC}	Supply	AMB core power and AMB channel interface power (1.5V).
V_{DD}	Supply	DRAM power and AMB DRAM I/O power (1.8V).
V_{DDSPD}	Supply	SPD/AMB SMBUS power (3.3V).
V_{SS}	Supply	Ground.
V_{TT}	Supply	DRAM address/command/clock termination power (V_{DD}/2).
M_TEST	–	The M_Test pin provides an external connection for testing the margin of V_{REF}, which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system. This test pin may have other features on future card designs and will be included in this specification at that time.
DNU	–	Do not use.

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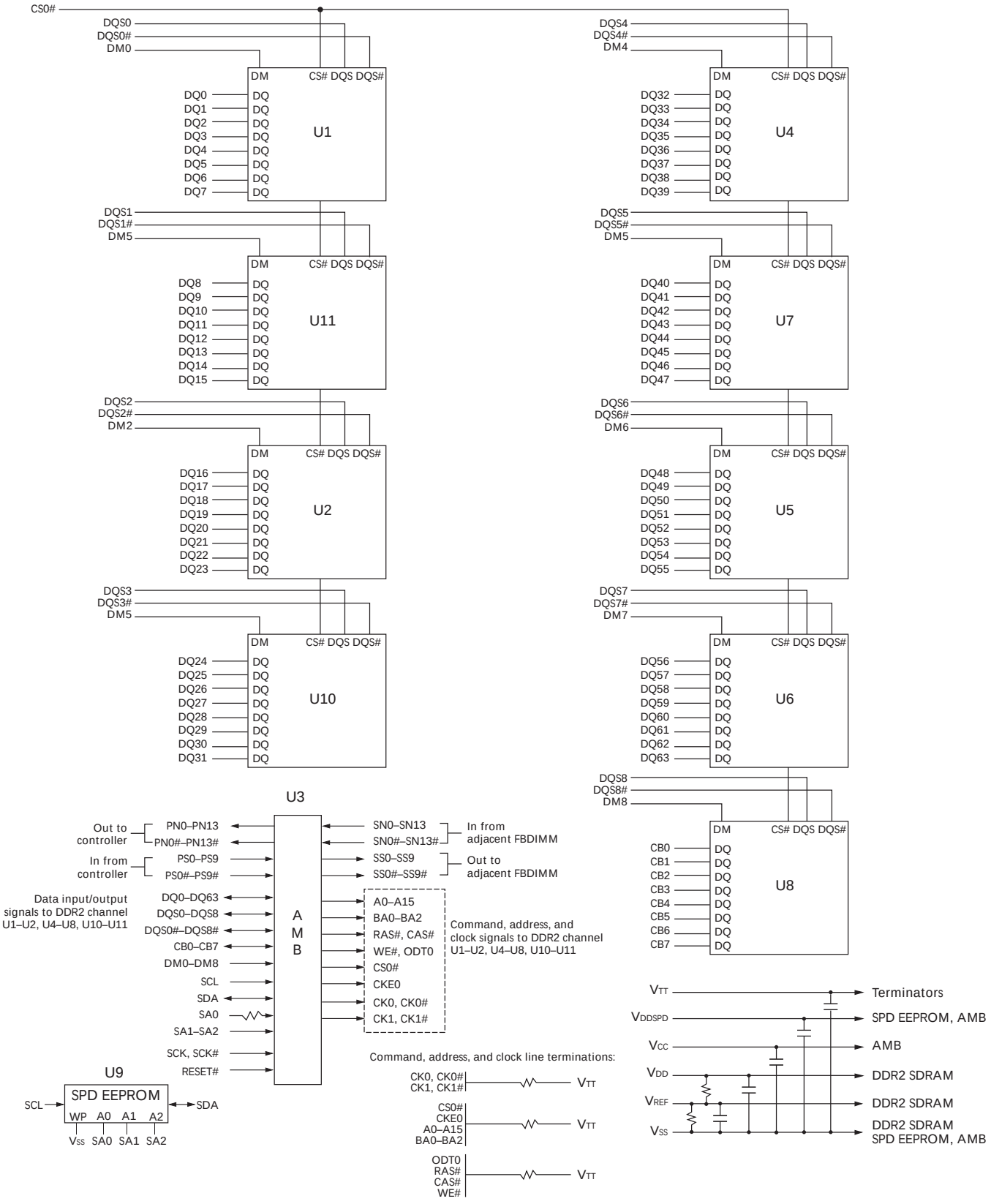
Block Diagrams

Figure 2: System Block Diagram



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Figure 3: Functional Block Diagram



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General Description

The Micron® FBDIMM adheres to the currently proposed industry specifications for FBDIMMs. The following specifications contain detailed information on FBDIMM design, interfaces, and theory of operation, and are listed here for the system designers convenience. Refer to the JEDEC Web site for available specifications.

- FBDIMM Design Specification – pending JEDEC approval
- FBDIMM: Architecture and Protocol – JESD206
- FBDIMM: Advanced Memory Buffer (AMB) Specification – JESD82-20
- Design for Test, Design for Validation (DF*x*) Specification
- Serial Presence-Detect (SPD) for Fully Buffered DIMM – JEDEC Standard No. 21-C page 4.1.2.7-1

The MT9HTF6472F and MT9HTF12872F DDR2 SDRAM modules are high-bandwidth, large-capacity channel solutions that have a narrow host interface. FBDIMMs use DDR2 SDRAM devices isolated from the channel behind an AMB buffer on the FBDIMM. Memory-device capacity remains high and total memory capacity scales with DDR2 SDRAM bit density.

As shown in Figure 2 on page 5, the FBDIMM channel provides a communication path from a host controller to an array of DDR2 SDRAM devices, with the DDR2 SDRAM devices buffered behind an AMB device. The physical isolation of the DDR2 SDRAM devices from the channel provides the flexibility needed to enhance the communication path and significantly increase the reliability and availability of the memory subsystem.

Advanced Memory Buffer

The AMB isolates the DDR2 SDRAM devices from the channel. This single-chip AMB component, located in the center of each FBDIMM, acts as a repeater and buffer for all signals and commands exchanged between the host controller and DDR2 SDRAM devices, including data input and output. The AMB communicates with the host controller and adjacent FBDIMMs on a system board using an industry-standard, high-speed, differential, point-to-point interface at 1.5V. The AMB also allows buffering of memory traffic to support large memory capacities. Refer to the JEDEC AMB FBDIMM: JESD82-20 specification for further information.

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Electrical Specifications

Stresses greater than those listed in Table 7 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in the device data sheet are not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 7: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	–0.3	+1.75	V	1
Voltage on V_{CC} pin relative to V_{SS}	V_{CC}	–0.3	+1.75	V	
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	–0.5	+2.3	V	
Voltage on V_{TT} pin relative to V_{SS}	V_{TT}	–0.5	+2.3	V	
DDR2 SDRAM device operating case temperature	T_C	0	+95	°C	2, 3
AMB device operating case temperature		0	+110	°C	

Notes:
1. V_{IN} should not be greater than V_{CC}.
2. T_C is specified at 95°C only when using 2X refresh timing (^tREFI = 7.8µs at or below 85°C; ^tREFI = 3.9µs above 85°C); refer to the DDR2 SDRAM component data sheet.
3. See applicable DDR2 SDRAM component data sheet for ^tREFI and extended mode register settings. The ^tREFI parameter is used to specify the doubled refresh interval necessary to sustain <85°C operation.

Table 8: Input DC Voltage and Operating Conditions

Parameter	Symbol	Min	Nom	Max	Units	Notes
AMB supply voltage	V_{CC}	1.46	1.5	1.54	V	
DDR2 SDRAM supply voltage	V_{DD}	1.7	1.8	1.9	V	
Termination voltage	V_{TT}	0.48 × V_{DD}	0.50 × V_{DD}	0.52 × V_{DD}	V	
EEPROM supply voltage	V_{DDSPD}	3.0	3.3	3.6	V	1
SPD input HIGH (logic 1) voltage	$V_{IH(DC)}$	2.1	–	V_{DDSPD}	V	2
SPD input LOW (logic 0) voltage	$V_{IL(DC)}$	–	–	0.8	V	2
RESET input HIGH (logic 1) voltage	$V_{IH(DC)}$	1.0	–	–	V	3
RESET input LOW (logic 0) voltage	$V_{IL(DC)}$	–	–	0.5	V	2
Leakage current (RESET)	I_L	–90	–	+90	µA	3
Leakage current (link)	I_L	–5	–	+5	µA	4

Notes:
1. Applies to AMB and SPD.
2. Applies to SMB and SPD bus signals.
3. For all other AMB-related DC parameters, please refer to the high-speed differential link interface specification.
4. For all other AMB-related DC parameters, please refer to the high-speed differential link interface specification.

Table 9: Clock Rates

FBDIMM Link Data Rate	Reference Clock	DRAM Clock	DRAM Data Rate
3.2 Gb/s	133 MHz	266 MHz	533 Mb/s
4.0 Gb/s	167 MHz	333 MHz	666 Mb/s
4.8 Gb/s	200 MHz	400 MHz	800 Mb/s

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IDD Conditions and Specifications

Table 10: IDD Conditions

Symbol	Condition
IDD_Idle_0	**Idle current, single or last DIMM:** L0 state; Idle (0 percent bandwidth); Primary channel enabled; Secondary channel disabled; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active
IDD_Idle_1	**Idle current, first DIMM:** L0 state; Idle (0 percent bandwidth); Primary and secondary channels enabled; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active
IDD_Active_1	**Active power:** L0 state; 50 percent DRAM bandwidth; 67 percent READ; 33 percent WRITE; Primary and secondary channels enabled; DDR2 SDRAM clock active; CKE HIGH
IDD_Active_2	**Active power, data pass through:** L0 state; 50 percent DRAM bandwidth to downstream DIMM; 67 percent READ; 33 percent WRITE; Primary and secondary channels enabled; DDR2 SDRAM clock active; CKE HIGH; Command and address lines stable
IDD_Training	**Training:** Primary and secondary channels enabled; 100 percent toggle on all channel lanes; DRAMs idle; 0 percent bandwidth; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active
IDD_IBIST	**IBIST over all IBIST modes:** DRAM idle (0 percent bandwidth); Primary channel enabled; Secondary channel enabled; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active
IDD_EI	**Electrical idle:** DRAM idle (0 percent bandwidth); Primary channel disabled; Secondary channel disabled; CKE LOW; Command and address lines floated; DDR2 SDRAM clock active; ODT and CKE driven LOW

Notes: 1. Actual test conditions may vary from published JEDEC test conditions.

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Table 11: IDD Specifications – 512MB DDR2-533

Symbol	IDD_Idle_0	IDD_Idle_1	IDD_Active_1	IDD_Active_2	IDD_Training	IDD_IBIST	IDD_EI	Units
ICC	2,200	3,000	3,400	3,200	3,500	3,800	2,000	mA
IDD	1,060	1,060	2,185	1,060	1,060	1,060	263	mA
Total power[1]	5.5	6.7	9.5	7.1	7.5	8.0	3.6	W

Table 12: IDD Specifications – 512MB DDR2-667

Symbol	IDD_Idle_0	IDD_Idle_1	IDD_Active_1	IDD_Active_2	IDD_Training	IDD_IBIST	IDD_EI	Units
ICC	2,600	3,400	3,900	3,700	4,000	4,500	2,500	mA
IDD	1,105	1,105	2,372	1,105	1,105	1,105	263	mA
Total power[1]	6.2	7.5	14.6	7.9	8.4	9.2	4.4	W

Table 13: IDD Specifications – 512MB DDR2-800

Symbol	IDD_Idle_0	IDD_Idle_1	IDD_Active_1	IDD_Active_2	IDD_Training	IDD_IBIST	IDD_EI	Units
ICC	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
IDD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
Total power[1]	TBD	TBD	TBD	TBD	TBD	TBD	TBD	W

Table 14: IDD Specifications – 1GB DDR2-533

Symbol	IDD_Idle_0	IDD_Idle_1	IDD_Active_1	IDD_Active_2	IDD_Training	IDD_IBIST	IDD_EI	Units
ICC	2,200	3,000	3,400	3,200	3,500	3,800	2,000	mA
IDD	1,060	1,060	2,065	1,060	1,060	1,060	263	mA
Total power[1]	5.5	6.7	9.3	7.1	7.5	8.0	3.6	W

Table 15: IDD Specifications – 1GB DDR2-667

Symbol	IDD_Idle_0	IDD_Idle_1	IDD_Active_1	IDD_Active_2	IDD_Training	IDD_IBIST	IDD_EI	Units
ICC	2,600	3,400	3,900	3,700	4,000	4,500	2,500	mA
IDD	1,060	1,060	2,155	1,060	1,060	1,060	263	mA
Total power[1]	6.1	7.4	10.2	7.8	8.3	9.1	4.4	W

Table 16: IDD Specifications – 1GB DDR2-800

Symbol	IDD_Idle_0	IDD_Idle_1	IDD_Active_1	IDD_Active_2	IDD_Training	IDD_IBIST	IDD_EI	Units
ICC	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
IDD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
Total power[1]	TBD	TBD	TBD	TBD	TBD	TBD	TBD	W

Notes: 1. Total power is based on maximum voltage levels, ICC @ 1.575V and IDD @ 1.9V.

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Serial Presence-Detect

Table 17: Serial Presence-Detect EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
EEPROM and AMB supply voltage	V_{DDSPD}	3.0	3.6	V
Input high voltage: logic 1; all inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: logic 0; all inputs	V_{IL}	–0.6	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.10	3.0	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	3.0	µA
Standby current	I_{SB}	1.6	4.0	µA
Power supply current, READ: SCL clock frequency = 100 kHz	ICC_R	0.4	1.0	mA
Power supply current, WRITE: SCL clock frequency = 100 kHz	ICC_W	2.0	3.0	mA

Table 18: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^tAA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^tBUF	1.3	–	µs	
Data-out hold time	^tDH	200	–	ns	
SDA and SCL fall time	^tF	–	300	ns	2
Data-in hold time	$^tHD:DAT$	0	–	µs	
Start condition hold time	$^tHD:STA$	0.6	–	µs	
Clock HIGH period	^tHIGH	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^tI	–	50	ns	
Clock LOW period	^tLOW	1.3	–	µs	
SDA and SCL rise time	^tR	–	0.3	µs	2
SCL clock frequency	^fSCL	–	400	kHz	
Data-in setup time	$^tSU:DAT$	100	–	ns	
Start condition setup time	$^tSU:STA$	0.6	–	µs	3
Stop condition setup time	$^tSU:STO$	0.6	–	µs	
WRITE cycle time	^tWRC	–	10	ms	4

Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

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Table 19: Serial Presence-Detect Matrix – DRAM Device and Module

Byte	Description	Entry	512MB	1GB
0	CRC range/SPD bytes total/bytes used	Bytes 0–116/ 256 bytes/ 176 bytes	92	92
1	SPD revision	1.1	11	11
2	Key byte/DRAM device type	DDR2 FBDIMM	09	09
3	Voltage levels of this assembly	DRAM/AMB	12	12
4	SDRAM addressing: Device rows/columns/banks	14 rows/ 10 columns/ 4 banks or 8 banks	44	45
5	Module physical attributes: Height/thickness	30.35mm/ 7.16mm	23	23
6	Module type	FBDIMM	07	07
7	Module organization: Module ranks/SDRAM device width (I/O)	Single rank/x8	09	09
8	Fine time-base dividend and divisor	5.0ps	51	51
9	Medium time-base dividend	1/4 = 0.25ns	01	01
10	Medium time-base divisor	1/4 = 0.25ns	04	04
11	SDRAM MIN cycle time (^{t}CK [MIN])	2.5ns (-80E) 3.0ns (-667) 3.75ns (-53E)	0A 0C 0F	0A 0C 0F
12	SDRAM MAX cycle time (^{t}CK [MAX])	8ns	20	20
13	SDRAM CAS latencies supported	5, 4 (-80E) 5, 4, 3 (-667) 4, 3 (-53E)	24 33 23	24 33 23
14	SDRAM MIN CL time (^{t}CAS)	12.5ns (-80E) 15ns (-667/-53E)	32 3C	32 3C
15	SDRAM WRITE recovery times supported	Range, MIN	22	22
16	SDRAM WRITE recovery time (^{t}WR)	15ns	3C	3C
17	SDRAM WRITE latencies supported	Range, MIN	42	42
18	SDRAM additive latencies supported	Range, MIN	40	40
19	SDRAM MIN RAS-to-CAS delay (^{t}RCD)	12.5ns (-80E) 15ns (-667/-53E)	32 3C	32 3C
20	SDRAM MIN row active-to-row active delay (^{t}RRD)	7.5ns	1E	1E
21	SDRAM MIN row precharge time (^{t}RP)	12.5ns (-80E) 15ns (-667/-53E)	32 3C	32 3C
22	SDRAM upper nibbles for ^{t}RAS and ^{t}RC	–	00	00
23	SDRAM MIN active to precharge time (^{t}RAS)	40ns	B4	B4
24	SDRAM MIN auto refresh-to-active/auto refresh time (^{t}RC)	55ns	DC	DC
25	SDRAM MIN AUTO REFRESH-to-ACTIVE/AUTO REFRESH command period (^{t}RFC-LSB)	105ns (512MB) 127.5ns (1GB)	A4	FE
26	SDRAM MIN AUTO REFRESH-to-ACTIVE/AUTO REFRESH command period (^{t}RFC-MSB)		01	01
27	SDRAM internal WRITE-to-READ command delay (^{t}WTR)	7.5ns	1E	1E
28	SDRAM internal READ-to-PRECHARGE command delay (^{t}RTP)	–	1E	1E
29	SDRAM burst lengths supported	4, 8	03	03
30	SDRAM drivers/terminations supported: 03 = 75Ω and 100Ω; 07 = 50Ω, 75Ω, and 100Ω	-80E/-667 -53E	07 03	07 03
31	Drivers supported	Weak drivers	01	01
32	SDRAM refresh rate (^{t}REFI) and 95°C self refresh	7.8µs	C2	C2

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Table 19: Serial Presence-Detect Matrix – DRAM Device and Module (continued)

Byte	Description	Entry	512MB	1GB
33	Bits 7:4: ΔT_C (MAX) (DRAM case temperature difference between MAX case temperature and baseline MAX case temperature), the baseline MAX case temperature is 85°C; Bits 3:0: DT4R4W Δ (case temperature rise difference between IDD4R/page open burst READ and IDD4W/page open burst WRITE operations)	–	52	51
34	Thermal resistance of DRAM device package from top (case) to ambient (PSI T-A DRAM) at still air condition based on JESD51-2 standard	–	32	31
35	DT0/T_C mode bits: Bits 7:2: Case temperature rise from ambient due to IDD0/ACTIVATE PRECHARGE operation minus 2.8°C offset temperature; Bit 1: Double refresh mode bit; Bit 0: High temperature self refresh rate support indication	–	04	04
36	DT2N/DT2Q: Case temperature rise from ambient due to IDD2N precharge STANDBY operation for UDIMM and due to IDD2Q/precharge quiet STANDBY operation for RDIMM	–	0E	0F
37	DT2P: Case temperature rise from ambient due to IDD2P/ PRECHARGE power-down operation	–	0A	0A
38	DT3N: Case temperature rise from ambient due to IDD3N/ACTIVE STANDBY operation	–	0D	0B
39	DT4R/mode bit, bits 7:1: Case temperature rise from ambient due to IDD4R/page open BURST READ operation; Bit 0: Mode bit to specify if DT4W is greater or less than DT4R	–	18	18
40	DT5B: Case temperature rise from ambient due to IDD5B/BURST REFRESH operation	–	0F	12
41	DT7: Case temperature rise from ambient due to IDD7/bank interleave READ MODE operation	–	12	15
42–78	FBDIMM reserved bytes	–	00	00
79	FBDIMM ODT definition	–	01	01
117	Module ID: Module manufacturer's JEDEC ID code	MICRON	80	80
118	Module ID: Module manufacturer's JEDEC ID code	MICRON	2C	2C
119	Module ID: Module manufacturing location	1–12	01–0C	01–0C
120–121	Module ID: Module manufacturing date	–	Variable data	Variable data
122–125	Module ID: Module serial number	–	Variable data	Variable data
128–145	Module part number	–	Variable data	Variable data
146–147	Module revision code	–	Variable data	Variable data
148–149	DRAM manufacturer's JEDEC ID code	MICRON	802C	802C
152–175	Reserved for manufacturer-specific data	–	FF	FF
176–255	Reserved for customer-specific data	–	FF	FF

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Table 20: Serial Presence-Detect Matrix – AMB and CRC

Byte	Description	Entry	E4	D4	N6	N7
80	FBDIMM reserved byte	–	00	00	00	00
81	Channel protocol supported (lower byte)	–	02	02	02	02
82	Channel protocol supported (upper byte)	–	00	00	00	00
83	Back-to-back turnaround clock cycles	–	10	10	15	15
84	Buffer read access at ^{t}CK for MAX CL	–	56	36	44	40
85	Buffer read access at ^{t}CK for MAX CL - 1	–	40	34	36	36
86	Buffer read access at ^{t}CK for MAX CL - 2	–	36	32	30	30
87	PSI T-A AMB	–	30	2A	2B	2B
88	DT AMB idle_0	-80E -667 -53E	– 60 52	56 56 4C	– 55 4C	5F 55 –
89	DT AMB idle_1	-80E -667 -53E	– 7A 66	6B 6B 61	– 73 69	7B 73 –
90	DT AMB idle_2	-80E -667 -53E	– 6E 60	5C 5C 50	– 73 69	7B 73 –
91	DT AMB active_1	-80E -667 -53E	– A1 84	91 91 82	– 92 87	92 92 –
92	DT AMB active_2	-80E -667 -53E	– 7F 6A	76 76 69	– 73 69	84 73 –
93	DT AMB LOS	-80E -667 -53E	– 00 00	00 00 00	– 73 69	84 73 –
94	PSI T-A DRAM-AF	–	00	00	00	00
95	PSIT-A AMB-AF	–	00	00	00	00
96	PSI D-A	–	00	00	00	00
97	PSI A-D	–	00	00	00	00
98	AMB T_J (MAX)	–	00	1F	1F	1F
99	Airflow impedance/DRAM/heat spreader types	–	0A	0A	0A	0A
100	Reserved	0	00	00	00	00
101	AMB preinitialization bytes	–	80	00	8F	6B
102	AMB preinitialization bytes	–	20	E2	2C	18
103	AMB preinitialization bytes	–	00	62	00	00
104	AMB preinitialization bytes	–	44	20	01	00
105	AMB preinitialization bytes	–	04	80	00	00
106	AMB preinitialization bytes	–	80	9C	00	00
107	AMB postinitialization bytes	–	48	00	00	43
108	AMB postinitialization bytes	–	53	00	00	00
109	AMB postinitialization bytes	–	B3	F0	02	00
110	AMB postinitialization bytes	512MB 1GB	43 41	70 70	00 00	00 00
111	AMB postinitialization bytes	–	65	60	00	00
112	AMB postinitialization bytes	–	4C	60	00	00
113	AMB postinitialization bytes	–	00	60	00	00

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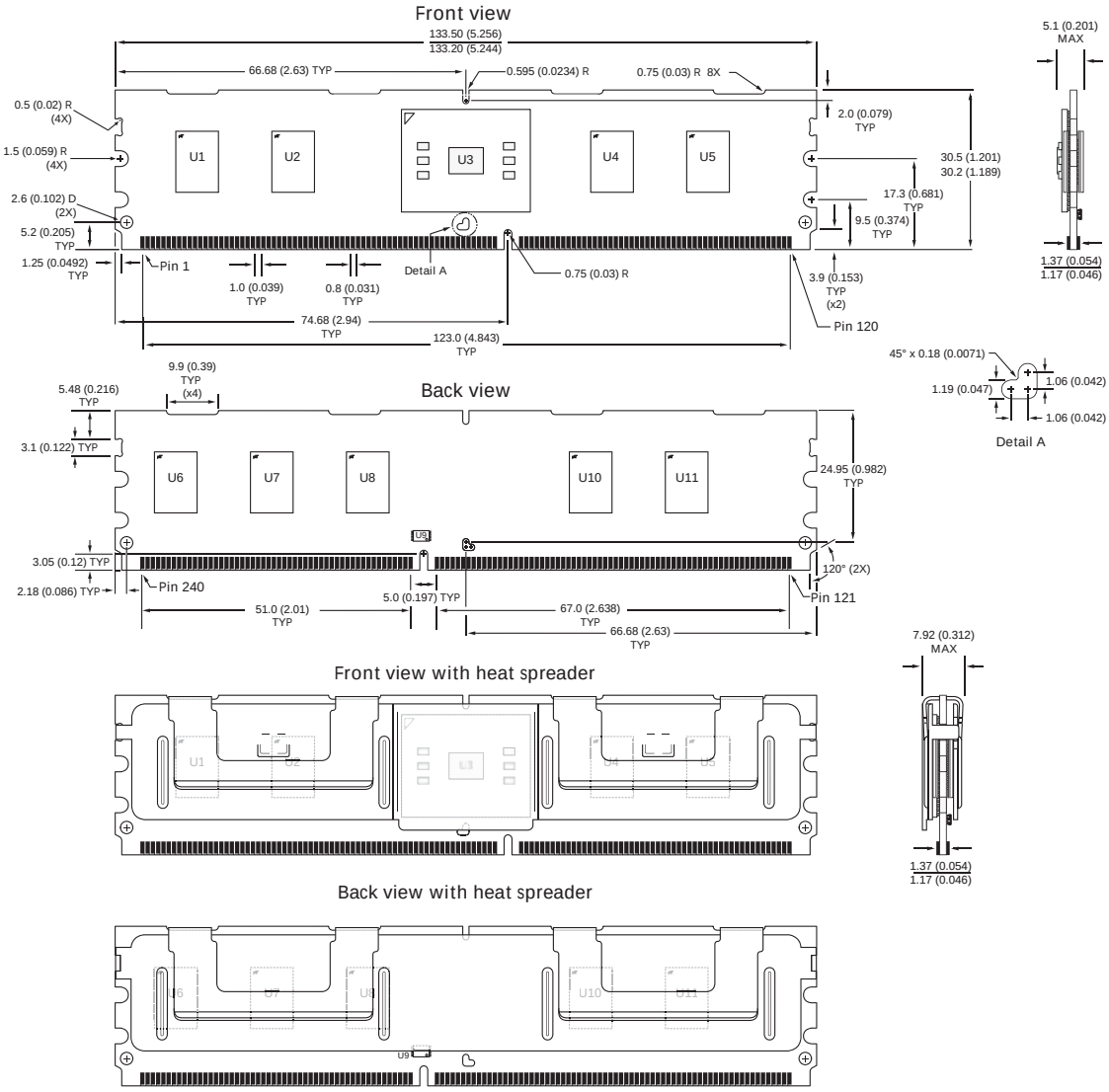
Table 20: Serial Presence-Detect Matrix – AMB and CRC (continued)

Byte	Description	Entry	E4	D4	N6	N7
114	AMB postinitialization bytes	–	10	60	00	10
115	AMB manufacturer's ID code (lower byte)	–	80	7F	80	80
116	AMB manufacturer's ID code (upper byte)	–	89	B3	10	10
126–127	CRC for bytes 0–116 (512MB/1GB)	-80E -667 -53E	– 818A/0477 9A44/1FB9	3C24/5AB9 B437/D2AA B08F/D612	– 6CE8/0A75 781D/1E80	8716/E188 9EBF/F822 –
150	Informal AMB revision tag (MSB)	–	01	00	–	00
151	Informal AMB revision tag (LSB)	–	09	00	–	00

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Module Dimensions

Figure 4: 240-Pin DDR2 FBDIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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