DDR3 SDRAM UDIMM

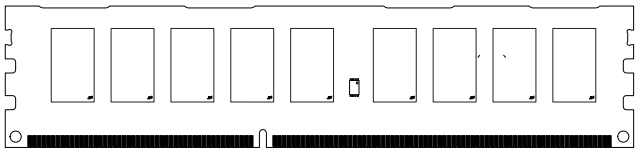
MT9JSF12872AZ – 1GB
MT9JSF25672AZ – 2GB
MT9JSF51272AZ – 4GB

Features

- DDR3 functionality and operations supported as defined in the component data sheet
- 240-pin, unbuffered dual in-line memory module (UDIMM)
- Fast data transfer rates: PC3-12800, PC3-10600, PC3-8500, or PC3-6400
- 1GB (128 Meg x 72), 2GB (256 Meg x 72), and 4GB (512 Meg x 72)
- V_{DD} = 1.5V ±0.075V
- V_{DDSPD} = +3.0V to +3.6V
- Supports ECC error detection and correction
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Single rank
- On-board I^2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

Figure 1: 240-Pin UDIMM (MO-269 R/C D)

Module height: 30mm (1.18in)



Options	Marking
• Operating temperature[1]	
– Commercial (0°C ≤ T_A ≤ +70°C)	None
– Industrial (–40°C ≤ T_A ≤ +85°C)	I
• Package	
– 240-pin DIMM (halogen-free)	Z
• Frequency/CAS latency	
– 1.25ns @ CL = 11 (DDR3-1600)	-1G6
– 1.5ns @ CL = 9 (DDR3-1333)	-1G4
– 1.87ns @ CL = 7 (DDR3-1066)	-1G1

Note: 1. Contact Micron for industrial temperature module offerings.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)							^tRCD (ns)	^tRP (ns)	^tRC (ns)
		CL = 11	CL = 10	CL = 9	CL = 8	CL = 7	CL = 6	CL = 5			
-1G6	PC3-12800	1600	1333	1333	1066	1066	800	667	13.125	13.125	48.125
-1G4	PC3-10600	–	1333	1333	1066	1066	800	667	13.125	13.125	49.125
-1G1	PC3-8500	–	–	–	1066	1066	800	667	13.125	13.125	50.625
-1G0	PC3-8500	–	–	–	1066	–	800	667	15	15	52.5
-80C	PC3-6400	–	–	–	–	–	800	800	12.5	12.5	50
-80B	PC3-6400	–	–	–	–	–	800	667	15	15	52.5

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Table 2: Addressing

Parameter	1GB	2GB	4GB
Refresh count	8K	8K	8K
Row address	16K A[13:0]	32K A[14:0]	64K A[15:0]
Device bank address	8 BA[2:0]	8 BA[2:0]	8 BA[2:0]
Device configuration	1Gb (128 Meg x 8)	2Gb (256 Meg x 8)	4Gb (512 Meg x 8)
Column address	1K A[9:0]	1K A[9:0]	1K A[9:0]
Module rank address	1 (S0#)	1 (S0#)	1 (S0#)

Table 3: Part Numbers and Timing Parameters – 1GB Modules

Base device: MT41J128M8,[1] 1Gb DDR3 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT9JSF12872A(I)Z-1G6__	1GB	128 Meg x 72	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT9JSF12872A(I)Z-1G4__	1GB	128 Meg x 72	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT9JSF12872A(I)Z-1G1__	1GB	128 Meg x 72	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

Notes:
1. The data sheet for the base device can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT9JSF12872AZ-1G1F1.

Table 4: Part Numbers and Timing Parameters – 2GB Modules

Base device: MT41J256M8,[1] 2Gb DDR3 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT9JSF25672A(I)Z-1G6__	2GB	256 Meg x 72	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT9JSF25672A(I)Z-1G4__	2GB	256 Meg x 72	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT9JSF25672A(I)Z-1G1__	2GB	256 Meg x 72	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

Notes:
1. The data sheet for the base device can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT9JSF25672AZ-1G1D1.

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Table 5: Part Numbers and Timing Parameters – 4GB Modules

Base device: MT41J512M8,[1] 4Gb DDR3 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT9JSF51272A(I)Z-1G6__	4GB	512 Meg x 72	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT9JSF51272A(I)Z-1G4__	4GB	512 Meg x 72	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT9JSF51272A(I)Z-1G1__	4GB	512 Meg x 72	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

Notes:
1. The data sheet for the base device can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT9JSF51272AZ-1G1A1.

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Pin Assignments and Descriptions

Table 6: Pin Assignments

240-Pin DDR3 UDIMM Front								240-Pin DDR3 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{REFDQ}	31	DQ25	61	A2	91	DQ41	121	V_{SS}	151	V_{SS}	181	A1	211	V_{SS}
2	V_{SS}	32	V_{SS}	62	V_{DD}	92	V_{SS}	122	DQ4	152	DM3	182	V_{DD}	212	DM5
3	DQ0	33	DQS3#	63	NC	93	DQS5#	123	DQ5	153	NC	183	V_{DD}	213	NC
4	DQ1	34	DQS3	64	NC	94	DQS5	124	V_{SS}	154	V_{SS}	184	CK0	214	V_{SS}
5	V_{SS}	35	V_{SS}	65	V_{DD}	95	V_{SS}	125	DM0	155	DQ30	185	CK0#	215	DQ46
6	DQS0#	36	DQ26	66	Vdd	96	DQ42	126	NC	156	DQ31	186	V_{DD}	216	DQ47
7	DQS0	37	DQ27	67	V_{REFCA}	97	DQ43	127	V_{SS}	157	V_{SS}	187	EVENT#	217	V_{SS}
8	V_{SS}	38	V_{SS}	68	NC	98	V_{SS}	128	DQ6	158	CB4	188	A0	218	DQ52
9	DQ2	39	CB0	69	V_{DD}	99	DQ48	129	DQ7	159	CB5	189	V_{DD}	219	DQ53
10	DQ3	40	CB1	70	A10	100	DQ49	130	V_{SS}	160	V_{SS}	190	BA1	220	V_{SS}
11	V_{SS}	41	V_{SS}	71	BA0	101	V_{SS}	131	DQ12	161	DM8	191	V_{DD}	221	DM6
12	DQ8	42	DQS8#	72	V_{DD}	102	DQS6#	132	DQ13	162	NC	192	RAS#	222	NC
13	DQ9	43	DQS8	73	WE#	103	DQS6	133	V_{SS}	163	V_{SS}	193	S0#	223	V_{SS}
14	V_{SS}	44	V_{SS}	74	CAS#	104	V_{SS}	134	DM1	164	CB6	194	V_{DD}	224	DQ54
15	DQS1#	45	CB2	75	V_{DD}	105	DQ50	135	NC	165	CB7	195	ODT0	225	DQ55
16	DQS1	46	CB3	76	NC	106	DQ51	136	V_{SS}	166	V_{SS}	196	A13	226	V_{SS}
17	V_{SS}	47	V_{SS}	77	NC	107	V_{SS}	137	DQ14	167	NC	197	V_{DD}	227	DQ60
18	DQ10	48	NC	78	V_{DD}	108	DQ56	138	DQ15	168	RESET#	198	NC	228	DQ61
19	DQ11	49	NC	79	NC	109	DQ57	139	V_{SS}	169	NC	199	V_{SS}	229	V_{SS}
20	V_{SS}	50	CKE0	80	V_{SS}	110	V_{SS}	140	DQ20	170	V_{DD}	200	DQ36	230	DM7
21	DQ16	51	V_{DD}	81	DQ32	111	DQS7#	141	DQ21	171	NF/A15	201	DQ37	231	NC
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	V_{SS}	172	NF/A14	202	V_{SS}	232	V_{SS}
23	V_{SS}	53	NC	83	V_{SS}	113	V_{SS}	143	DM2	173	V_{DD}	203	DM4	233	DQ62
24	DQS2#	54	V_{DD}	84	DQS4#	114	DQ58	144	NC	174	A12	204	NC	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQ59	145	V_{SS}	175	A9	205	V_{SS}	235	V_{SS}
26	V_{SS}	56	A7	86	V_{SS}	116	V_{SS}	146	DQ22	176	V_{DD}	206	DQ38	236	V_{DDSPD}
27	DQ18	57	V_{DD}	87	DQ34	117	SA0	147	DQ23	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	V_{SS}	178	A6	208	V_{SS}	238	SDA
29	V_{SS}	59	A4	89	V_{SS}	119	SA2	149	DQ28	179	V_{DD}	209	DQ44	239	V_{SS}
30	DQ24	60	V_{DD}	90	DQ40	120	V_{TT}	150	DQ29	180	A3	210	DQ45	240	V_{TT}

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Table 7: Pin Descriptions

Symbol	Type	Description
A[15:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also used for BC4/BL8 identification as "BL on-the-fly" during CAS commands. The address inputs also provide the op-code during the mode register command set. A[13:0] address 1Gb DDR3 devices; A[14:0] address 2Gb devices, and [15:0] address 4Gb devices.
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the device bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, and MR3) is loaded during the LOAD MODE command.
CK0, CK0#	Input	**Clock:** CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKE0	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DM[8:0]	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data, during a write access. DM is sampled on both edges of the DQS. Although the DM pins are input-only, the DM loading is designed to match that of the DQ and DQS pins.
ODT0	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DD} and DC LOW ≤ 0.2 × V_{DD}.
S0#	Input	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA[2:0]	Input	**Serial address inputs:** These pins are used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** SCL is used to synchronize communication to and from the temperature sensor/SPD EEPROM.
CB[7:0]	I/O	**Check bits:** Data used for ECC.
DQ[63:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[8:0] DQS#[8:0]	I/O	**Data strobe:** DQS and DQS# are differential data strobes. Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data.
SDA	I/O	**Serial data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the module on the I^2C bus.

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Table 7: Pin Descriptions (Continued)

Symbol	Type	Description
EVENT#	Output (open drain)	**Temperature event:** The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V. The component V_{DD} and V_{DDQ} are connected to the module V_{DD}.
V_{DDSPD}	Supply	**Temperature sensor/SPD EEPROM power supply:** +3.0V to +3.6V.
V_{REFCA}	Supply	**Reference voltage:** Control, command, and address (V_{DD}/2).
V_{REFDQ}	Supply	**Reference voltage:** DQ, DM (V_{DD}/2).
V_{SS}	Supply	Ground.
V_{TT}	Supply	**Termination voltage:** Used for control, command, and address (V_{DD}/2).
NC	–	**No connect:** These pins are not connected on the module.
NF	–	**No function**: Connected within the module, but provides no functionality.

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DQ Map

Table 8: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	2	9	U2	0	10	18
	1	5	123		1	13	132
	2	7	129		2	15	138
	3	0	3		3	8	12
	4	6	128		4	14	137
	5	4	122		5	12	131
	6	3	10		6	11	19
	7	1	4		7	9	13
U3	0	18	27	U4	0	26	36
	1	21	141		1	29	150
	2	23	147		2	31	156
	3	16	21		3	24	30
	4	22	146		4	30	155
	5	20	140		5	28	149
	6	19	28		6	27	37
	7	17	22		7	25	31
U5	0	CB2	45	U6	0	34	87
	1	CB5	159		1	37	201
	2	CB7	165		2	39	207
	3	CB0	39		3	32	81
	4	CB6	164		4	38	206
	5	CB4	158		5	36	200
	6	CB3	46		6	35	88
	7	CB1	40		7	33	82
U7	0	42	96	U8	0	50	105
	1	45	210		1	53	219
	2	47	216		2	55	225
	3	40	90		3	48	99
	4	46	215		4	54	224
	5	44	209		5	52	218
	6	43	97		6	51	106
	7	41	91		7	49	100

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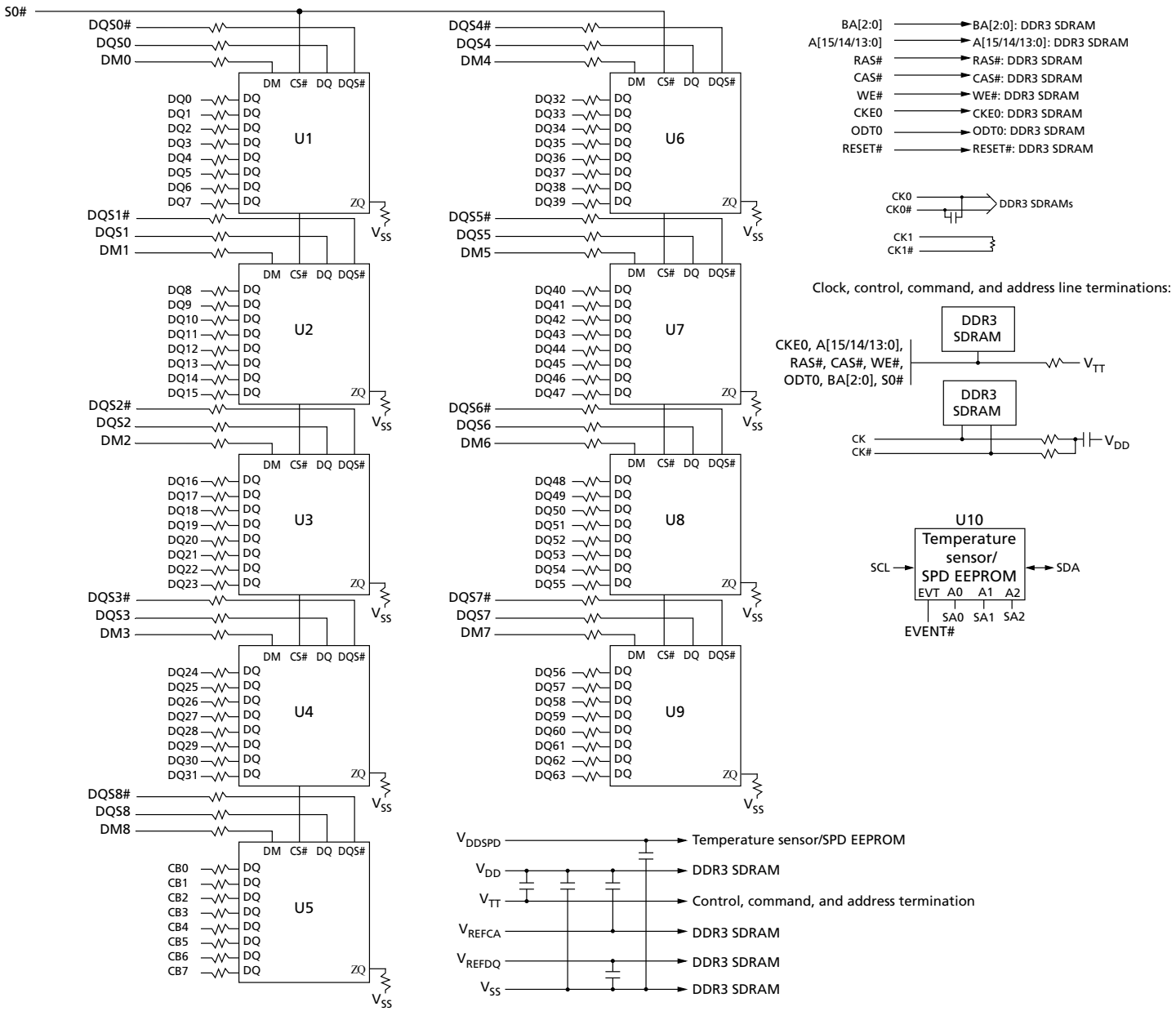
Table 8: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U9	0	58	114				
	1	61	228				
	2	63	234				
	3	56	108				
	4	62	233				
	5	60	227				
	6	59	115				
	7	57	109				

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Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

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General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

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Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 9: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	+1.975	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	+1.975	V

Table 10: Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units	Notes
V_{DD}	V_{DD} supply voltage		1.425	1.5	1.575	V	
I_{VTT}	Termination reference current from V_{TT}		–600	–	+600	mA	
V_{TT}	Termination reference voltage (DC) – command/address bus		0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V	1
I_I	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, BA, S#, CKE, ODT, CK, CK#	–18	0	+18	µA	
		DM	–2	0	+2		
I_{OZ}	Output leakage current; 0V ≤ V_{OUT} ≤ V_{DDQ}; DQ and ODT are disabled; ODT is HIGH	DQ, DQS, DQS#	–5	0	+5	µA	
I_{VREF}	V_{REF} supply leakage current; V_{REFDQ} = V_{DD}/2 or V_{REFCA} = V_{DD}/2 (All other pins not under test = 0V)		–9	0	+9	µA	
T_A	Module ambient operating temperature	Commercial	0	–	+70	°C	2, 3
		Industrial	–40	–	+85	°C	
T_C	DDR3 SDRAM component case operating temperature	Commercial	0	–	+85	°C	2, 3, 4
		Industrial	–40	–	+95	°C	

Notes:
1. V_{TT} termination voltage in excess of the stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
2. T_A and T_C are simultaneous requirements.
3. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.
4. The refresh rate is required to double when 85°C < T_C ≤ 95°C.

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DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR3 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown below.

Table 11: Module and Component Speed Grades

DDR3 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
-1G6	-125
-1G4	-15E
-1G1	-187E
-1G0	-187
-80C	-25E
-80B	-25

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

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I_{DD} Specifications

Table 12: DDR3 I_{DD} Specifications and Conditions – 1GB

Values are for the MT41J128M8 DDR3 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter	Symbol	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{DD0}	1080	990	900	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	1260	1170	1080	mA
Precharge power-down current: Slow exit	I_{DD2P0}	108	108	108	mA
Precharge power-down current: Fast exit	I_{DD2P1}	405	360	315	mA
Precharge quiet standby current	I_{DD2Q}	603	540	477	mA
Precharge standby current	I_{DD2N}	630	585	495	mA
Precharge standby ODT current	I_{DD2NT}	855	765	675	mA
Active power-down current	I_{DD3P}	405	360	315	mA
Active standby current	I_{DD3N}	603	558	513	mA
Burst read operating current	I_{DD4R}	2250	1800	1440	mA
Burst write operating current	I_{DD4W}	2250	1980	1710	mA
Refresh current	I_{DD5B}	2340	2160	1980	mA
Self refresh temperature current: MAX T_C = 85°C	I_{DD6}	54	54	54	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{DD6ET}	81	81	81	mA
All banks interleaved read current	I_{DD7}	5400	4410	3510	mA
Reset current	I_{DD8}	126	126	126	mA

Table 13: DDR3 I_{DD} Specifications and Conditions – 2GB

Values are for the MT41J256M8 DDR3 SDRAM only and are computed from values specified in the 2Gb (256 Meg x 8) component data sheet

Parameter	Symbol	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{DD0}	TBD	810	720	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	TBD	1035	900	mA
Precharge power-down current: Slow exit	I_{DD2P0}	TBD	108	108	mA
Precharge power-down current: Fast exit	I_{DD2P1}	TBD	315	270	mA
Precharge quiet standby current	I_{DD2Q}	TBD	585	495	mA
Precharge standby current	I_{DD2N}	TBD	585	495	mA
Precharge standby ODT current	I_{DD2NT}	TBD	765	675	mA
Active power-down current	I_{DD3P}	TBD	405	360	mA
Active standby current	I_{DD3N}	TBD	675	540	mA
Burst read operating current	I_{DD4R}	TBD	1800	1440	mA
Burst write operating current	I_{DD4W}	TBD	2160	1800	mA
Refresh current	I_{DD5B}	TBD	2295	2205	mA
Self refresh temperature current: MAX T_C = 85°C	I_{DD6}	TBD	81	81	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{DD6ET}	TBD	108	108	mA

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Table 13: DDR3 I_{DD} Specifications and Conditions – 2GB (Continued)

Values are for the MT41J256M8 DDR3 SDRAM only and are computed from values specified in the 2Gb (256 Meg x 8) component data sheet

Parameter	Symbol	1600	1333	1066	Units
All banks interleaved read current	IDD7	TBD	3285	2880	mA
Reset current	IDD8	TBD	126	126	mA

Table 14: DDR3 I_{DD} Specifications and Conditions – 4GB

Values are for the MT41J512M8 DDR3 SDRAM only and are computed from values specified in the 4Gb (512 Meg x 8) component data sheet

Parameter	Symbol	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{DD0}	TBD	990	900	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	TBD	1215	1035	mA
Precharge power-down current: Slow exit	I_{DD2P0}	TBD	108	108	mA
Precharge power-down current: Fast exit	I_{DD2P1}	TBD	225	225	mA
Precharge quiet standby current	I_{DD2Q}	TBD	585	495	mA
Precharge standby current	I_{DD2N}	TBD	585	495	mA
Precharge standby ODT current	I_{DD2NT}	TBD	765	630	mA
Active power-down current	I_{DD3P}	TBD	450	405	mA
Active standby current	I_{DD3N}	TBD	720	585	mA
Burst read operating current	I_{DD4R}	TBD	2070	1755	mA
Burst write operating current	I_{DD4W}	TBD	2385	2070	mA
Refresh current	I_{DD5B}	TBD	3285	3150	mA
Self refresh temperature current: MAX T_C = 85°C	I_{DD6}	TBD	99	99	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{DD6ET}	TBD	135	135	mA
All banks interleaved read current	I_{DD7}	TBD	3735	3375	mA
Reset current	I_{DD8}	TBD	126	126	mA

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Temperature Sensor with Serial Presence-Detect EEPROM

The temperature from the integrated thermal sensor is monitored and converts into a digital word via the I^2C bus. System designers can use the user-programmable registers to create a custom temperature-sensing solution based on system requirements. Programming and configuration details comply with JEDEC standard No. 21-C page 4.7-1, "Definition of the TSE2002av, Serial Presence Detect with Temperature Sensor."

Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR3 SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. User-specific information can be written into the remaining 128 bytes of storage. READ/WRITE operations between the system (master) and the EEPROM (slave) device occur via an I^2C bus. Write protect (WP) is connected to Vss, permanently disabling hardware write protect. For further information please refer to Micron technical note TN-04-42, "Memory Module Serial Presence-Detect."

Table 15: Temperature Sensor with Serial Presence-Detect EEPROM Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	+3.0	+3.6	V
Supply current: V_{DD} = 3.3V	I_{DD}	–	+2.0	mA
Input high voltage: Logic 1; SCL, SDA	V_{IH}	+1.45	V_{DDSPD} + 1	V
Input low voltage: Logic 0; SCL, SDA	V_{IL}	–	+0.55	V
Output low voltage: I_{OUT} = 2.1mA	V_{OL}	–	+0.4	V
Input current	I_{IN}	–5.0	+5.0	µA
Temperature sensing range	–	–40	+125	°C
Temperature sensor accuracy (initial release)	–	–2.0	+2.0	°C
Temperature sensor accuracy (class B)	–	–1.0	+1.0	°C

Table 16: Sensor and EEPROM Serial Interface Timing

Parameter/Condition	Symbol	Min	Max	Units
Time bus must be free before a new transition can start	^tBUF	4.7	–	µs
SDA fall time	^tF	20	300	ns
SDA rise time	^tR	–	1,000	ns
Data hold time	$^tHD:DAT$	200	900	ns
Start condition hold time	$^tH:STA$	4.0	–	µs
Clock HIGH period	^tHIGH	4.0	50	µs
Clock LOW period	^tLOW	4.7	–	µs
SCL clock frequency	^tSCL	10	100	kHz
Data setup time	$^tSU:DAT$	250	–	ns

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Table 16: Sensor and EEPROM Serial Interface Timing (Continued)

Parameter/Condition	Symbol	Min	Max	Units
Start condition setup time	^{t}SU:STA	4.7	–	µs
Stop condition setup time	^{t}SU:STO	4.0	–	µs

EVENT# Pin

The temperature sensor also adds the EVENT# pin (open drain). Not used by the SPD EEPROM, EVENT# is a temperature sensor output used to flag critical events that can be set up in the sensor's configuration register.

EVENT# has three defined modes of operation: interrupt mode, compare mode, and critical temperature mode. The open-drain output of EVENT# under the three separate operating modes is illustrated below. Event thresholds are programmed in the 0x01 register using a hysteresis. The alarm window provides a comparison window, with upper and lower limits set in the alarm upper boundary register and the alarm lower boundary register, respectively. When the alarm window is enabled, EVENT# will trigger whenever the temperature is outside the MIN or MAX values set by the user.

The interrupt mode enables software to reset EVENT# after a critical temperature threshold has been detected. Threshold points are set in the configuration register by the user. This mode triggers the critical temperature limit and both the MIN and MAX of the temperature window.

The compare mode is similar to the interrupt mode, except EVENT# cannot be reset by the user and only returns to the logic HIGH state when the temperature falls below the programmed thresholds.

Critical temperature mode triggers EVENT# only when the temperature has exceeded the programmed critical trip point. When the critical trip point has been reached, the temperature sensor goes into comparator mode, and the critical EVENT# cannot be cleared through software.

SM Bus Slave Subaddress Decoding

The temperature sensor's physical address differs from the SPD EEPROM's physical address: binary 0011 for A0, A1, A2, and RW#, where A2, A1, and A0 are the three slave subaddress pins and the RW# bit is the READ/WRITE flag.

If the slave base address is fixed for the temperature sensor/SPD EEPROM, then the pins set the subaddress bits of the slave address, enabling the devices to be located anywhere within the eight slave address locations. For example, they could be set from 30h to 3Eh.

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Figure 3: EVENT# Pin Functionality

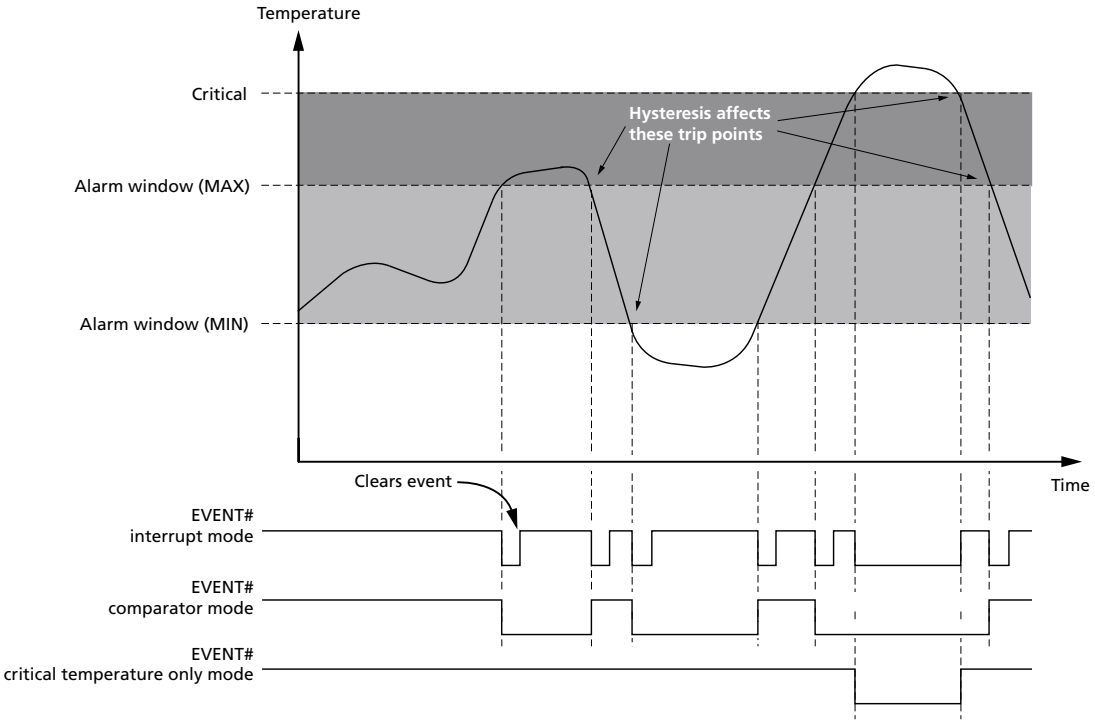


Table 17: Temperature Sensor Registers

Name	Address	Power-on Default
Pointer register	Not applicable	Undefined
Capability register	0x00	0x0001
Configuration register	0x01	0x0000
Alarm temperature upper boundary register	0x02	0x0000
Alarm temperature lower boundary register	0x03	0x0000
Critical temperature register	0x04	0x0000
Temperature register	0x05	Undefined

Pointer Register

The pointer register selects which of the 16-bit registers is being accessed in subsequent READ and WRITE operations. This register is a write-only register.

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Table 18: Pointer Register Bits 0–7

Bit							
7	6	5	4	3	2	1	0
0	0	0	0	Register select	Register select	Register select	Register select

Table 19: Pointer Register Bits 0–2 Descriptions

Bit			Register
2	1	0	
0	0	0	Capability register
0	0	1	Configuration register
0	1	0	Alarm temperature upper boundary register
0	1	1	Alarm temperature lower boundary register
1	0	0	Critical temperature register
1	0	1	Temperature register

Capability Register

The capability register indicates the features and functionality supported by the temperature sensor. This register is a read-only register.

Table 20: Capability Register (Address: 0x00)

Bit							
15	14	13	12	11	10	9	8
RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Bit							
7	6	5	4	3	2	1	0
RFU	RFU	RFU	Temperature resolution		Wider range	Precision	Has alarm and critical temperature

Table 21: Capability Register Bit Description

Bit	Description
0	Basic capability 1: Has alarm and critical trip point capabilities
1	Accuracy 0: ±2°C over the active range and ±3°C over the monitor range 1: ±1°C over the active range and ±2°C over the monitor range
2	Wider range 0: Temperatures lower than 0°C are clamped to a binary value of 0 1: Temperatures below 0°C can be read

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Table 21: Capability Register Bit Description (Continued)

Bit	Description
4:3	Temperature resolution 00: 0.5°C LSB 01: 0.25°C LSB 10: 0.125°C LSB 11: 0.0625°C LSB
15:5	0: Must be set to zero

Configuration Register

Table 22: Configuration Register (Address: 0x01)

Bit							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RFU	RFU	RFU	RFU	RFU	Hysteresis		Shutdown mode
Bit							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Critical lock bit	Alarm lock bit	Clear event	Event output status	Event output control	Critical event only	Event polarity	Event mode

Table 23: Configuration Register Bit Descriptions

Bit	Description	Notes
0	Event mode 0: Comparator mode 1: Interrupt mode	Event mode cannot be changed if either of the lock bits is set.
1	EVENT# polarity 0: Active LOW 1: Active HIGH	EVENT# polarity cannot be changed if either of the lock bits is set.
2	Critical event only 0: EVENT# trips on alarm or critical temperature event 1: EVENT# trips only if critical temperature is reached	
3	Event output control 0: Event output disabled 1: Event output enabled	
4	Event status 0: EVENT# has not been asserted by this device 1: EVENT# is being asserted due to an alarm window or critical temperature condition	This is a read-only field in the register. The event causing the event can be determined from the read temperature register.
5	Clear event 0: No effect 1: Clears the event when the temperature sensor is in the interrupt mode	

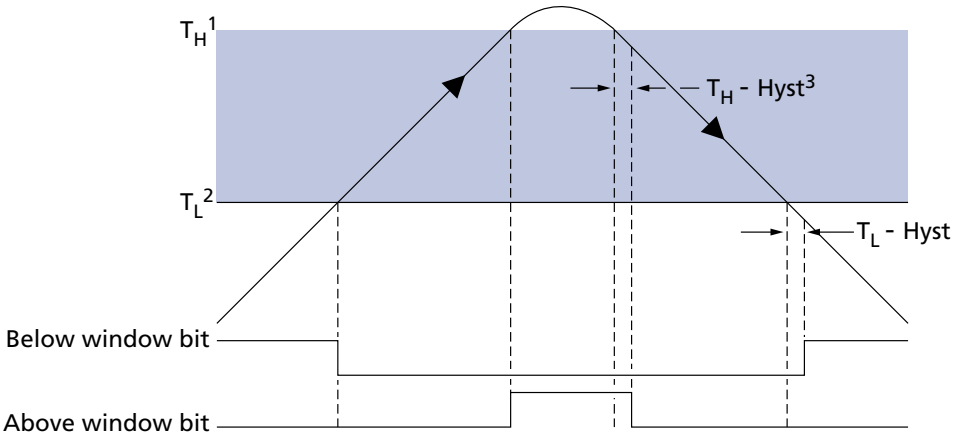
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Table 23: Configuration Register Bit Descriptions (Continued)

Bit	Description	Notes
6	Alarm window lock bit 0: Alarm trips are not locked and can be changed 1: Alarm trips are locked and cannot be changed	
7	Critical trip lock bit 0: Critical trip is not locked and can be changed 1: Critical trip is locked and cannot be changed	
8	Shutdown mode 0: Enabled 1: Shutdown	The shutdown mode is a power-saving mode that disables the temperature sensor.
10:9	Hysteresis enable 00: Disable 01: Enable at 1.5°C 10: Enable at 3°C 11: Enable at 6°C	When enabled, a hysteresis is applied to temperature movement around the trip points (see Figure 4 (page 21)). As an example, if the hysteresis register is enabled to a delta of 6°C, the preset trip points will toggle when the temperature reaches the programmed value. These values will reset when the temperature drops below the trip points minus the set hysteresis level. In this case, this would be critical temperature minus 6°C. The hysteresis is applied to both the above alarm window and the below alarm window bits found in the read-only temperature register (see Table 24 (page 21)). EVENT# is also affected by this register.

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Figure 4: Hysteresis Applied to Temperature Around Trip Points



Notes:
1. T_H is the value set in the alarm temperature upper boundary trip register.
2. T_L is the value set in the alarm temperature lower boundary trip register.
3. Hyst is the value set in the hysteresis bits of the configuration register.

Table 24: Hysteresis Applied to Alarm Window Bits in the Temperature Register

Condition	Below Alarm Window Bit		Above Alarm Window Bit	
	Temperature Gradient	Critical Temperature	Temperature Gradient	Critical Temperature
Sets	Falling	T_L - Hyst	Rising	T_H
Clears	Rising	T_L	Falling	T_H - Hyst

Temperature Format

The temperature trip point registers and temperature readout register use a 2's complement format to enable negative numbers. The least significant bit (LSB) is equal to 0.0625°C or 0.25°C, depending on which register is referenced. For example, assuming an LSB of 0.0625°C:

- A value of 0x018C would equal 24.75°C
- A value of 0x06C0 would equal 108°C
- A value of 0x1E74 would equal –24.75°C

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Temperature Trip Point Registers

The upper and lower temperature boundary registers are used to set the maximum and minimum values of the alarm window. LSB for these registers is 0.25°C. All RFU bits in the register will always report zero.

Table 25: Alarm Temperature Lower Boundary Register (Address: 0x02)

Bit														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	MSB										LSB	RFU	RFU
			Alarm window upper boundary temperature												

Table 26: Alarm Temperature Lower Boundary Register (Address: 0x03)

Bit														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	MSB										LSB	RFU	RFU
			Alarm window lower boundary temperature												

Critical Temperature Register

The critical temperature register is used to set the maximum temperature above the alarm window. The LSB for this register is 0.25°C. All RFU bits in the register will always report zero.

Table 27: Critical Temperature Register (Address: 0x04)

Bit														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	MSB										LSB	RFU	RFU
			Critical temperature trip point												

Temperature Register

The temperature register is a read-only register that provides the current temperature detected by the temperature sensor. The LSB for this register is 0.0625°C with a resolution of 0.0625°C. The most significant bit (MSB) is 128°C in the readout section of this register.

The upper three bits of the register are used to monitor the trip points that are set in the previous three registers.

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Table 28: Temperature Register (Address: 0x05)

Bit															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Above critical trip	Above alarm window	Below alarm window	MSB												LSB
			Temperature												

Table 29: Temperature Register Bit Descriptions

Bit	Description
13	Below alarm window 0: Temperature is equal to or above the lower boundary 1: Temperature is below alarm window
14	Above alarm window 0: Temperature is equal to or below the upper boundary 1: Temperature is above alarm window
15	Above critical trip point 0: Temperature is below critical trip point 1: Temperature is above critical trip point

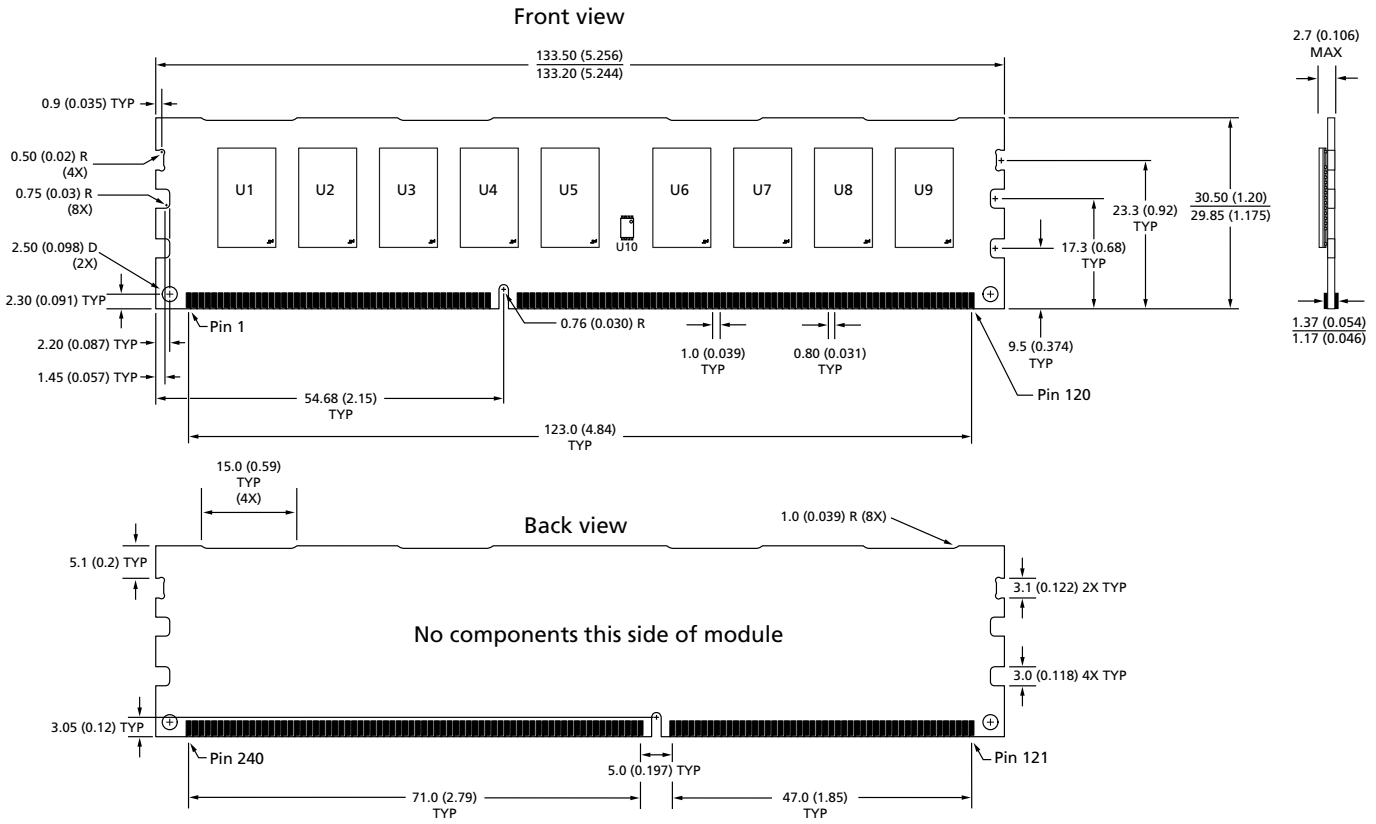
Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.

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Module Dimensions

Figure 5: 240-Pin DDR3 UDIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

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Revision History

Rev C, Production – 09/09

- Updated document format
- Updated parameter formatting throughout document
- Options/Marking, table: Deleted last three lines and note 2
- Part Numbers and Timing Parameters – 1GB Modules, table: Deleted last three lines
- Part Numbers and Timing Parameters – 2GB Modules, table: Deleted last three lines
- Part Numbers and Timing Parameters – 4GB Modules, table: Deleted last three lines
- Pin Descriptions, table: Updated descriptions for DM, ODT, RESET#, SA, SCL, V_{DD}, and V_{DDSPD}
- DDR3 I_{DD} Specifications and Conditions – 1GB, table: Deleted 800 speed grade column; changed I_{DD2P} slow exit to I_{DD2P0}; changed I_{DD2P0} values for 1600, 1333, and 1066 speed grades; changed I_{DD2P} fast exit to I_{DD2P1}; changed I_{DD2P1} values for 1600, 1333, and 1066 speed grades; changed I_{DD4W} value for 1600 speed grade
- DDR3 I_{DD} Specifications and Conditions – 2GB, table: Deleted 800 speed grade column
- DDR3 I_{DD} Specifications and Conditions – 4GB, table: Deleted 800 speed grade column

Rev B, Production – 06/09

- 2GB and 4GB module part numbers and associated functional data added.
- File ID changed to jsf9c128_256_512x72az to show added module densities
- Data sheet source files moved from Frame to Astoria

Rev A, Production – 09/08

- Initial Revision, PCB 0694 referenced

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Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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