1/3-Inch CMOS Digital Image Sensor

MT9M021/MT9M031 Datasheet, Rev. 9

For the latest datasheet revision, please visit www.onsemi.com

Features

- Superior low-light performance
- HD video (720p60)
- Global shutter
- Video/Single Frame mode
- Flexible row-skip modes
- On-chip AE and statistics engine
- Parallel and serial output
- Support for external LED or flash
- Auto black level calibration
- Context switching

Applications

- Scene processing
- Scanning and machine vision
- 720p60 video applications

General Description

The ON Semiconductor MT9M021/MT9M031 is a 1/3-inch CMOS digital image sensor with an active-pixel array of 1280H x 960V. It includes sophisticated camera functions such as auto exposure control, windowing, scaling, row skip mode, and both video and single frame modes. It is designed for low light performance and features a global shutter for accurate capture of moving scenes. It is programmable through a simple two-wire serial interface. The MT9M021/MT9M031 produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of applications, including scanning and HD video.

Table 1: Key Parameters

Parameter		Typical Value
Optical format		1/3-inch (6 mm)
Active pixels		1280 x 960 = 1.2 Mp
Pixel size		3.75µm
Color filter array		RGB Bayer or Monochrome
Shutter type		Global shutter
Input clock range		6 – 50 MHz
Output pixel clock (maximum)		74.25 MHz
Output	Serial	HiSPi (iBGA package only)
	Parallel	12-bit
Frame rate	Full resolution	45 fps
	720p	60 fps
Responsivity (Monochrome)		6.1 V/lux-sec
Responsivity (Color)		5.3 V/lux-sec
SNR_{MAX}		38 dB
Dynamic range		64 dB
Supply voltage	I/O	1.8 or 2.8 V
	Digital	1.8 V
	Analog	2.8 V
	HiSPi	0.4 V
Power consumption		<400 mW
Operating temperature (ambient)		–30°C to +70°C
Package options		9 x 9 mm 64-pin iBGA
		10x10mm 48-pin iLCC

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Ordering Information

Table 2: Available Part Numbers

Part Number	Product Description	Orderable Product Attribute Description
MT9M021IA3XTC-DPBR1	1.2 MP 1/3" GS CIS	Dry Pack with Protective Film, Double Side BBAR Glass
MT9M021IA3XTC-DRBR	1.2 MP 1/3" GS CIS	Dry Pack without Protective Film, Double Side BBAR Glass
MT9M021IA3XTM-DPBR1	1.2 MP 1/3" GS CIS	Dry Pack with Protective Film, Double Side BBAR Glass
MT9M021IA3XTM-DRBR1	1.2 MP 1/3" GS CIS	Dry Pack without Protective Film, Double Side BBAR Glass
MT9M021IA3XTMZ-DPBR	1.2 MP 1/3" GS CIS	Dry Pack with Protective Film, Double Side BBAR Glass
MT9M021IA3XTMZ-DRBR	1.2 MP 1/3" GS CIS	Dry Pack without Protective Film, Double Side BBAR Glass
MT9M021IA3XTMZ-TPBR	1.2 MP 1/3" GS CIS	Tape & Reel with Protective Film, Double Side BBAR Glass
MT9M031D00STMC24BC1-200	1 MP 1/6" SOC	Die Sales, 200 μm Thickness
MT9M031I12STC-DPBR1	1 MP 1/6" SOC	Dry Pack with Protective Film, Double Side BBAR Glass
MT9M031I12STC-DRBR	1.2 MP 1/3" GS CIS	Dry Pack without Protective Film, Double Side BBAR Glass
MT9M031I12STM-DPBR	1.2 MP 1/3" GS CIS	Dry Pack with Protective Film, Double Side BBAR Glass
MT9M031I12STM-DRBR1	1.2 MP 1/3" GS CIS	Dry Pack without Protective Film, Double Side BBAR Glass
MT9M031I12STMZ-DRBR	1.2 MP 1/3" GS CIS	Dry Pack without Protective Film, Double Side BBAR Glass

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General Description

The ON Semiconductor MT9M021/MT9M031 can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a full-resolution image at 45 frames per second (fps). It outputs 12-bit raw data, using either the parallel or serial (HiSPi) output ports. The device may be operated in video (master) mode or in frame trigger mode.

FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a synchronized pixel clock. A dedicated FLASH pin can be programmed to control external LED or flash exposure illumination.

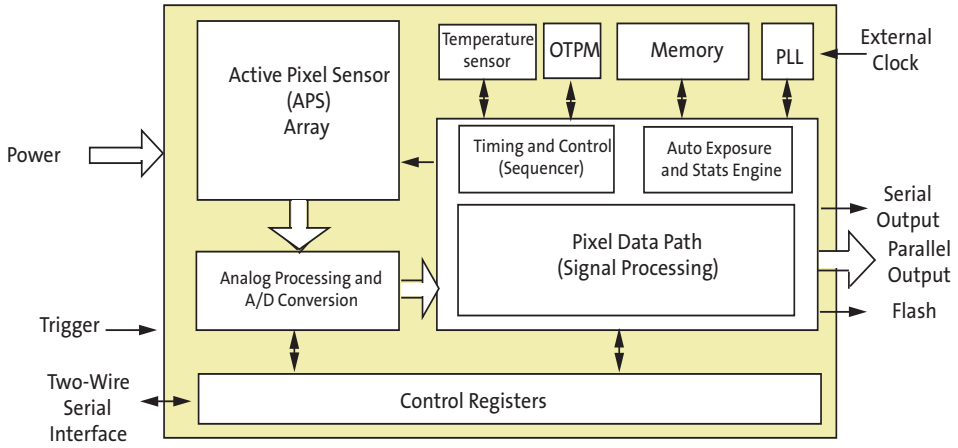
The MT9M021/MT9M031 includes additional features to allow application-specific tuning: windowing, adjustable auto-exposure control, auto black level correction, on-board temperature sensor, and row skip and digital binning modes.

The sensor is designed to operate in a wide temperature range (–30°C to +70°C).

Functional Overview

The MT9M021/MT9M031 is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) that can be optionally enabled to generate all internal clocks from a single master input clock running between 6 and 50 MHz. The maximum output pixel rate is 74.25 Mp/s, corresponding to a clock rate of 74.25 MHz. Figure 1 shows a block diagram of the sensor.

Figure 1: Block Diagram



User interaction with the sensor is through the two-wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 1.2 Mp Active- Pixel Sensor array. The MT9M021/MT9M031 features global shutter technology for accurate capture of moving images. The exposure of the entire array is controlled by programming the integration time by register setting. All rows simultaneously integrate light prior to readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog-to- digital converter (ADC). The output from the ADC is a 12-bit value for each pixel in the array. The ADC output passes through a digital

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processing signal chain (which provides further data path corrections and applies digital gain). The pixel data are output at a rate of up to 74.25 Mp/s, in parallel to frame and line synchronization signals.

Features Overview

The MT9M021/MT9M031 Global Sensor shutter has a wide array of features to enhance functionality and to increase versatility. A summary of features follows. Please refer to the MT9M021/MT9M031 Developer Guide for detailed feature descriptions, register settings, and tuning guidelines and recommendations.

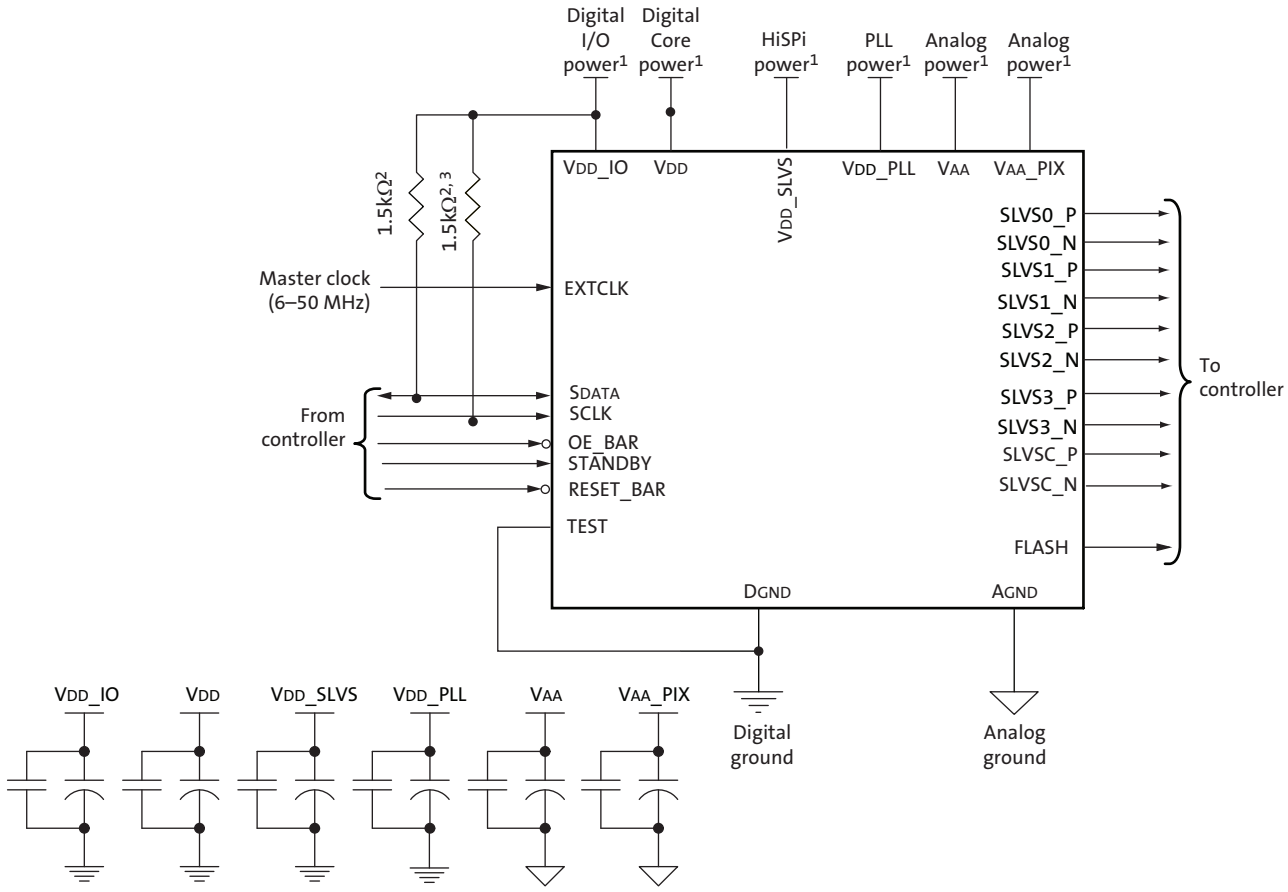
- Operating Modes
  The MT9M021/MT9M031 works in master (video), trigger (single frame), or Auto Trigger modes. In master mode, the sensor generates the integration and readout timing. In trigger mode, it accepts an external trigger to start exposure, then generates the exposure and readout timing. The exposure time is programmed through the two-wire serial interface for both modes.

Note: Trigger mode is not compatible with the HiSPi interface.

- Window Control
  Configurable window size and blanking times allow a wide range of resolutions and frame rates. Digital binning and skipping modes are supported, as are vertical and horizontal mirror operations.
- Context Switching
  Context switching may be used to rapidly switch between two sets of register values. Refer to the MT9M021/MT9M031 Developer Guide for a complete set of context switchable registers.
- Gain
  The MT9M021/MT9M031 Global Shutter sensor can be configured for analog gain of up to 8x, and digital gain of up to 8x.
- Automatic Exposure Control
  The integrated automatic exposure control may be used to ensure optimal settings of exposure and gain are computed and updated every other frame. Refer to the MT9M021/MT9M031 Developer Guide for more details.
- HiSPi
  The MT9M021/MT9M031 Global Shutter image sensor supports two or three lanes of Streaming-SP or Packetized-SP protocols of ON Semiconductor's High-Speed Serial Pixel Interface.
- PLL
  An on chip PLL provides reference clock flexibility and supports spread spectrum sources for improved EMI performance.
- Reset
  The MT9M021/MT9M031 may be reset by a register write, or by a dedicated input pin.
- Output Enable
  The MT9M021/MT9M031 output pins may be tri-stated using a dedicated output enable pin.
- Temperature Sensor
- Black Level Correction
- Row Noise Correction
- Column Correction
- Test Patterns
  Several test patterns may be enabled for debug purposes. These include a solid color, color bar, fade to grey, and a walking 1s test pattern.

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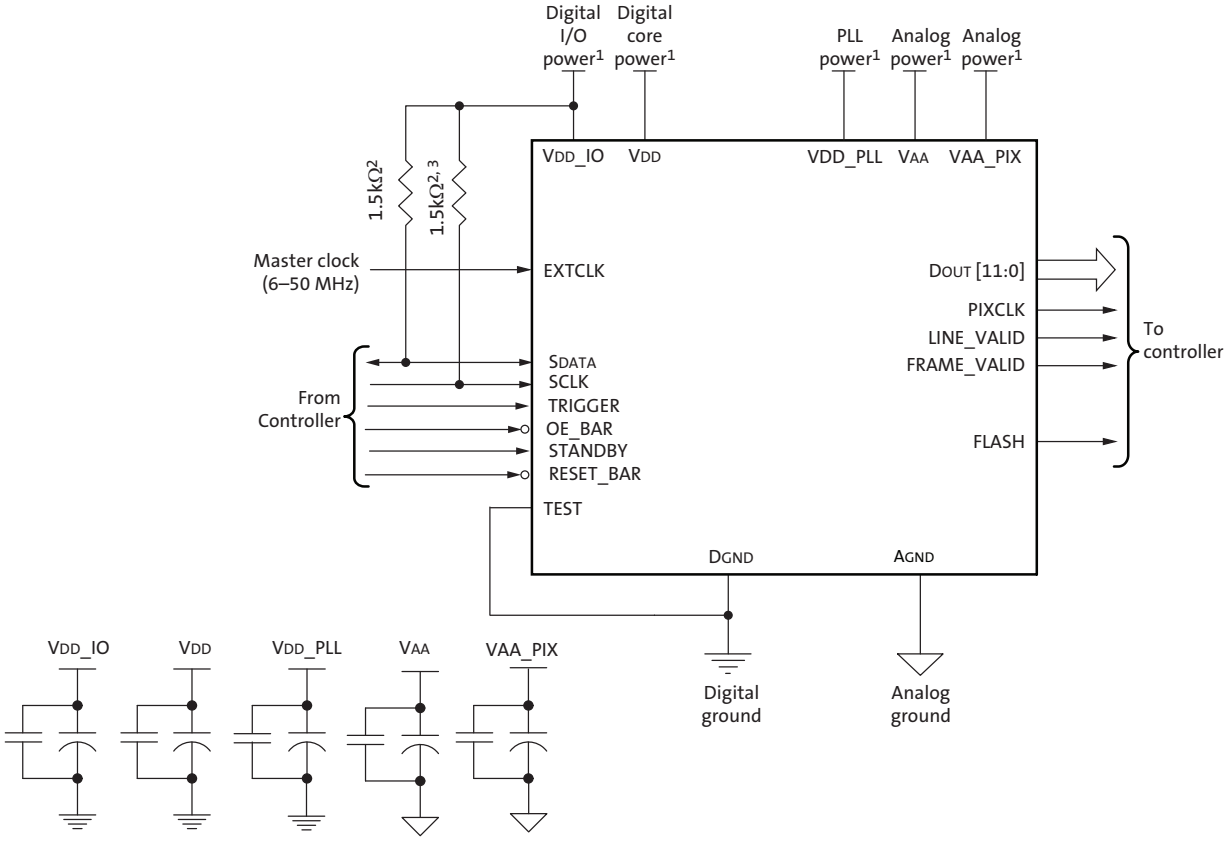
Figure 2: Typical Configuration: Serial Four-Lane HiSPi Interface



Notes:
1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5kΩ, but it may be greater for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. The parallel interface output pads can be left unconnected if the serial output interface is used.
5. ON Semiconductor recommends that 0.1µF and 10µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the MT9M021/MT9M031 demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes be placed in a manner such that coupling with the digital power planes is minimized.
7. Although 4 serial lanes are shown, the MT9M021/MT9M031 supports only 2 or 3 lane HiSPi.

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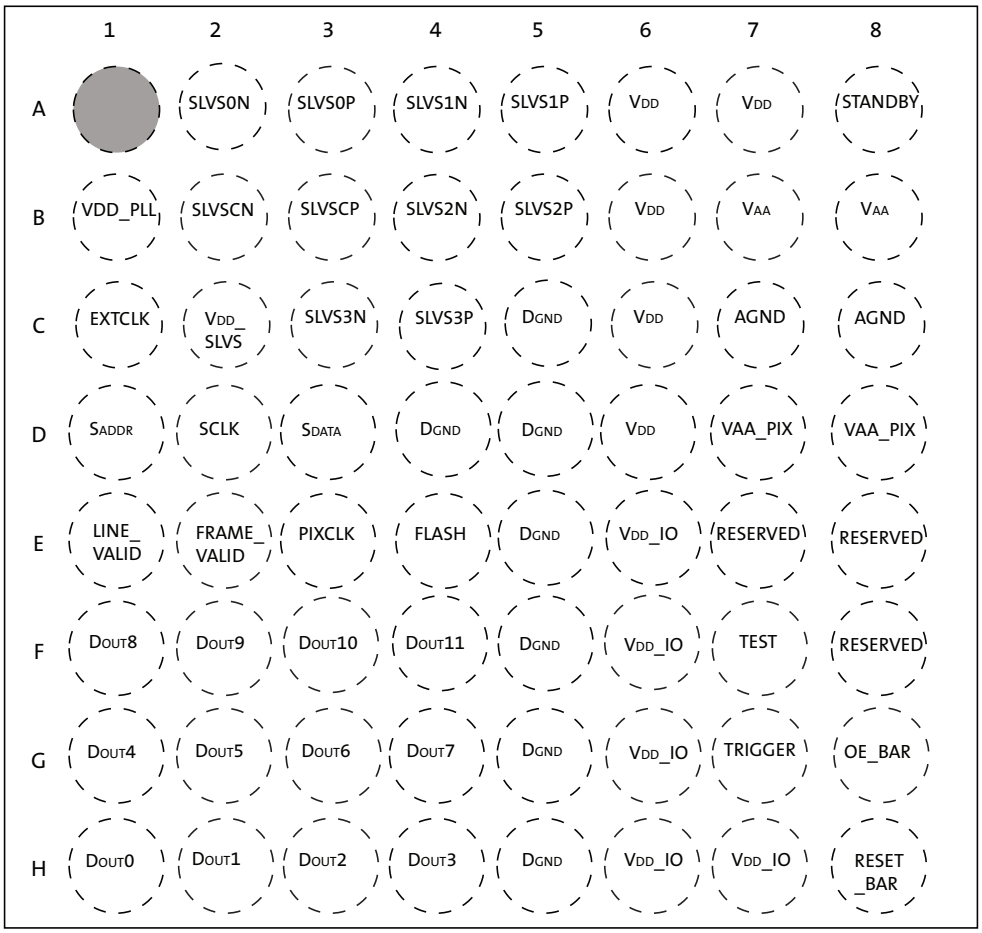
Figure 3: Typical Configuration: Parallel Pixel Data Interface



Notes:
1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5kΩ, but it may be greater for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. The serial interface output pads can be left unconnected if the parallel output interface is used.
5. ON Semiconductor recommends that 0.1µF and 10µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on lay-out and design considerations. Refer to the MT9M021/MT9M031 demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes be placed in a manner such that coupling with the digital power planes is minimized.

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Figure 4: 9x9mm 64-Ball iBGA Package



Top View
(Ball Down)

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Table 3: Pin Descriptions - 64-Ball iBGA Package

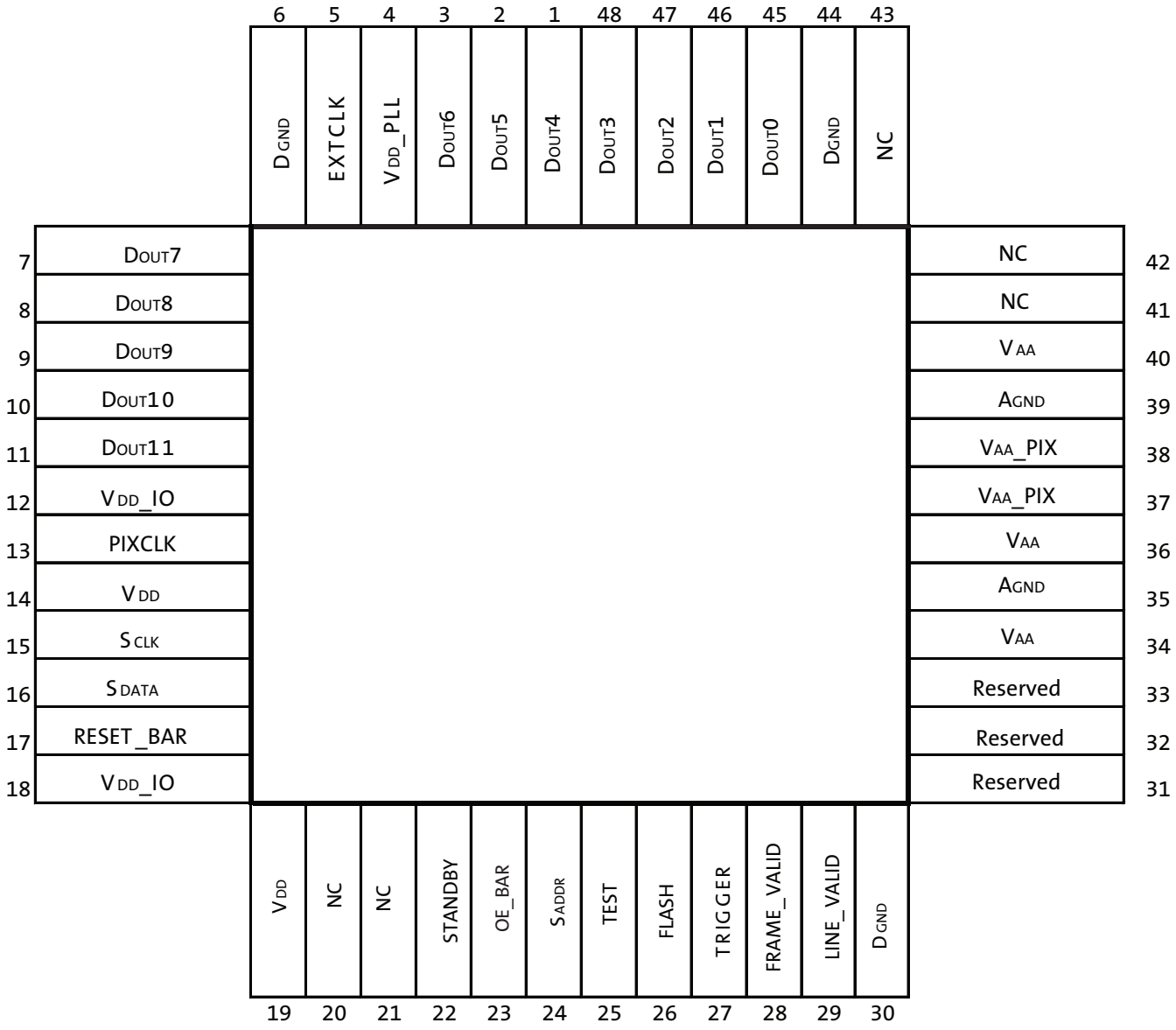
Name	iBGA Pin	Type	Description
SLVS0_N	A2	Output	HiSPi serial data, lane 0, differential N.
SLVS0_P	A3	Output	HiSPi serial data, lane 0, differential P.
SLVS1_N	A4	Output	HiSPi serial data, lane 1, differential N.
SLVS1_P	A5	Output	HiSPi serial data, lane 1, differential P.
STANDBY	A8	Input	Standby-mode enable pin (active HIGH).
VDD_PLL	B1	Power	PLL power.
SLVSC_N	B2	Output	HiSPi serial DDR clock differential N.
SLVSC_P	B3	Output	HiSPi serial DDR clock differential P.
SLVS2_N	B4	Output	HiSPi serial data, lane 2, differential N.
SLVS2_P	B5	Output	HiSPi serial data, lane 2, differential P.
VAA	B7, B8	Power	Analog power.
EXTCLK	C1	Input	External input clock.
VDD_SLVS	C2	Power	HiSPi power.
SLVS3_N	C3	Output	HiSPi serial data, lane 3, differential N.
SLVS3_P	C4	Output	HiSPi serial data, lane 3, differential P.
DGND	C5, D4, D5, E5, F5, G5, H5	Power	Digital GND.
VDD	A6, A7, B6, C6, D6	Power	Digital power.
AGND	C7, C8	Power	Analog GND.
SADDR	D1	Input	Two-Wire Serial address select.
SCLK	D2	Input	Two-Wire Serial clock input.
SDATA	D3	I/O	Two-Wire Serial data I/O.
VAA_PIX	D7, D8	Power	Pixel power.
LINE_VALID	E1	Output	Asserted when DOUT line data is valid.
FRAME_VALID	E2	Output	Asserted when DOUT frame data is valid.
PIXCLK	E3	Output	Pixel clock out. DOUT is valid on rising edge of this clock.
FLASH	E4	Output	Control signal to drive external light sources.
VDD_IO	E6, F6, G6, H6, H7	Power	I/O supply power.
DOUT8	F1	Output	Parallel pixel data output.
DOUT9	F2	Output	Parallel pixel data output.
DOUT10	F3	Output	Parallel pixel data output.
DOUT11	F4	Output	Parallel pixel data output (MSB)
TEST	F7	Input	Manufacturing test enable pin (connect to DGND).
DOUT4	G1	Output	Parallel pixel data output.
DOUT5	G2	Output	Parallel pixel data output.
DOUT6	G3	Output	Parallel pixel data output.
DOUT7	G4	Output	Parallel pixel data output.
TRIGGER	G7	Input	Exposure synchronization input.
OE_BAR	G8	Input	Output enable (active LOW).
DOUT0	H1	Output	Parallel pixel data output (LSB)
DOUT1	H2	Output	Parallel pixel data output.
DOUT2	H3	Output	Parallel pixel data output.
DOUT3	H4	Output	Parallel pixel data output.

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Table 3: Pin Descriptions (continued)- 64-Ball iBGA Package

Name	iBGA Pin	Type	Description
RESET_BAR	H8	Input	Asynchronous reset (active LOW). All settings are restored to factory default.
Reserved	E7, E8, F8	n/a	Reserved (do not connect).

Figure 5: 48 iLCC Package, Parallel Output



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Table 4: Pin Descriptions - 48 iLCC Package, Parallel

Pin Number	Name	Type	Description
1	DOUT4	Output	Parallel pixel data output.
2	DOUT5	Output	Parallel pixel data output.
3	DOUT6	Output	Parallel pixel data output.
4	VDD_PLL	Power	PLL power.
5	EXTCLK	Input	External input clock.
6	DGND	Power	Digital ground.
7	DOUT7	Output	Parallel pixel data output.
8	DOUT8	Output	Parallel pixel data output.
9	DOUT9	Output	Parallel pixel data output.
10	DOUT10	Output	Parallel pixel data output.
11	DOUT11	Output	Parallel pixel data output (MSB).
12	VDD_IO	Power	I/O supply power.
13	PIXCLK	Output	Pixel clock out. DOUT is valid on rising edge of this clock.
14	VDD	Power	Digital power.
15	SCLK	Input	Two-Wire Serial clock input.
16	SDATA	I/O	Two-Wire Serial data I/O.
17	RESET_BAR	Input	Asynchronous reset (active LOW). All settings are restored to factory default.
18	VDD_IO	Power	I/O supply power.
19	VDD	Power	Digital power.
20	NC		No connection.
21	NC		No connection.
22	STANDBY	Input	Standby-mode enable pin (active HIGH).
23	OE_BAR	Input	Output enable (active LOW).
24	SADDR	Input	Two-Wire Serial address select.
25	TEST	Input	Manufacturing test enable pin (connect to DGND).
26	FLASH	Output	Flash output control.
27	TRIGGER	Input	Exposure synchronization input.
28	FRAME_VALID	Output	Asserted when DOUT frame data is valid.
29	LINE_VALID	Output	Asserted when DOUT line data is valid.
30	DGND	Power	Digital ground
31	Reserved	n/a	Reserved (do not connect).
32	Reserved	n/a	Reserved (do not connect).
33	Reserved	n/a	Reserved (do not connect).
34	VAA	Power	Analog power.
35	AGND	Power	Analog ground.
36	VAA	Power	Analog power.
37	VAA_PIX	Power	Pixel power.
38	VAA_PIX	Power	Pixel power.
39	AGND	Power	Analog ground.
40	VAA	Power	Analog power.
41	NC		No connection.
42	NC		No connection.

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Table 4: Pin Descriptions (continued)- 48 iLCC Package, Parallel

Pin Number	Name	Type	Description
43	NC		No connection.
44	DGND	Power	Digital ground.
45	DOUT0	Output	Parallel pixel data output (LSB)
46	DOUT1	Output	Parallel pixel data output.
47	DOUT2	Output	Parallel pixel data output.
48	DOUT3	Output	Parallel pixel data output.

Electrical Specifications

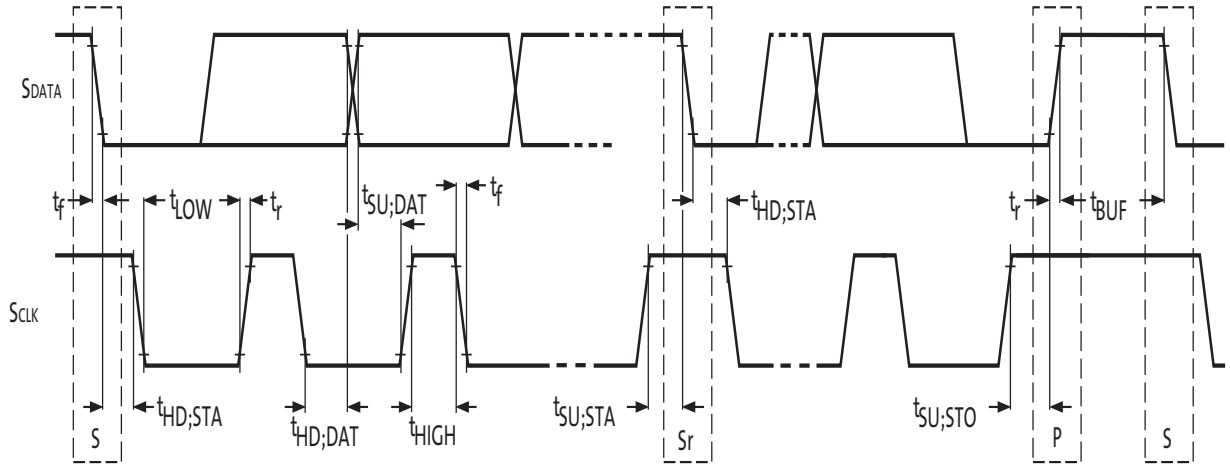
Unless otherwise stated, the following specifications apply to the following conditions:

V_{DD} = 1.8V – 0.10/+0.15; V_{DD_IO} = V_{DD_PLL} = V_{AA} = V_{AA_PIX} = 2.8V ± 0.3V; V_{DD_SLVS} = 0.4V – 0.1/+0.2; T_A = -30°C to +70°C; output load = 10pF; PIXCLK frequency = 74.25 MHz; HiSPi off.

Two-Wire Serial Register Interface

The electrical characteristics of the two-wire serial register interface (SCLK, SDATA) are shown in Figure 6 and Table 5.

Figure 6: Two-Wire Serial Bus Timing Parameters



Note: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

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Table 5: Two-Wire Serial Bus Characteristics

[f]EXTCLK = 27 MHz; V_{DD} = 1.8V; V_{DD}_IO = 2.8V; V_{AA} = 2.8V; V_{AA}_PIX = 2.8V; V_{DD}_PLL = 2.8V; T_A = 25°C

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
SCLK Clock Frequency	[f]SCL	0	100	0	400	KHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	[t]HD;STA	4.0	-	0.6	-	µS
LOW period of the SCLK clock	[t]LOW	4.7	-	1.3	-	µS
HIGH period of the SCLK clock	[t]HIGH	4.0	-	0.6	-	µS
Set-up time for a repeated START condition	[t]SU;STA	4.7	-	0.6	-	µS
Data hold time:	[t]HD;DAT	0[4]	3.45[5]	0[6]	0.9[5]	µS
Data set-up time	[t]SU;DAT	250	-	100[6]	-	nS
Rise time of both SDATA and SCLK signals	[t]r	-	1000	20 + 0.1Cb[7]	300	nS
Fall time of both SDATA and SCLK signals	[t]f	-	300	20 + 0.1Cb[7]	300	nS
Set-up time for STOP condition	[t]SU;STO	4.0	-	0.6	-	µS
Bus free time between a STOP and START condition	[t]BUF	4.7	-	1.3	-	µS
Capacitive load for each bus line	Cb	-	400	-	400	pF
Serial interface input pin capacitance	CIN_SI	-	3.3	-	3.3	pF
SDATA max load capacitance	CLOAD_SD	-	30	-	30	pF
SDATA pull-up resistor	RSD	1.5	4.7	1.5	4.7	KΩ

Notes:
1. This table is based on I^2C standard (v2.1 January 2000). Philips Semiconductor.
2. Two-wire control is I^2C-compatible.
3. All values referred to V_{IHmin} = 0.9 V_{DD} and V_{ILmax} = 0.1V_{DD} levels. Sensor EXCLK = 27 MHz.
4. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.
5. The maximum [t]HD;DAT has only to be met if the device does not stretch the LOW period ([t]LOW) of the SCLK signal.
6. A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system, but the requirement [t]SU;DAT 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA line [t]r max + [t]SU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCLK line is released.
7. Cb = total capacitance of one bus line in pF.

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I/O Timing

By default, the MT9M021/MT9M031 launches pixel data, FV and LV with the falling edge of PIXCLK. The expectation is that the user captures DOUT[11:0], FV and LV using the rising edge of PIXCLK. The launch edge of PIXCLK can be configured in register R0x3028.

See Figure 7 below and Table 6 on page 14 for I/O timing (AC) characteristics.

Figure 7: I/O Timing Diagram

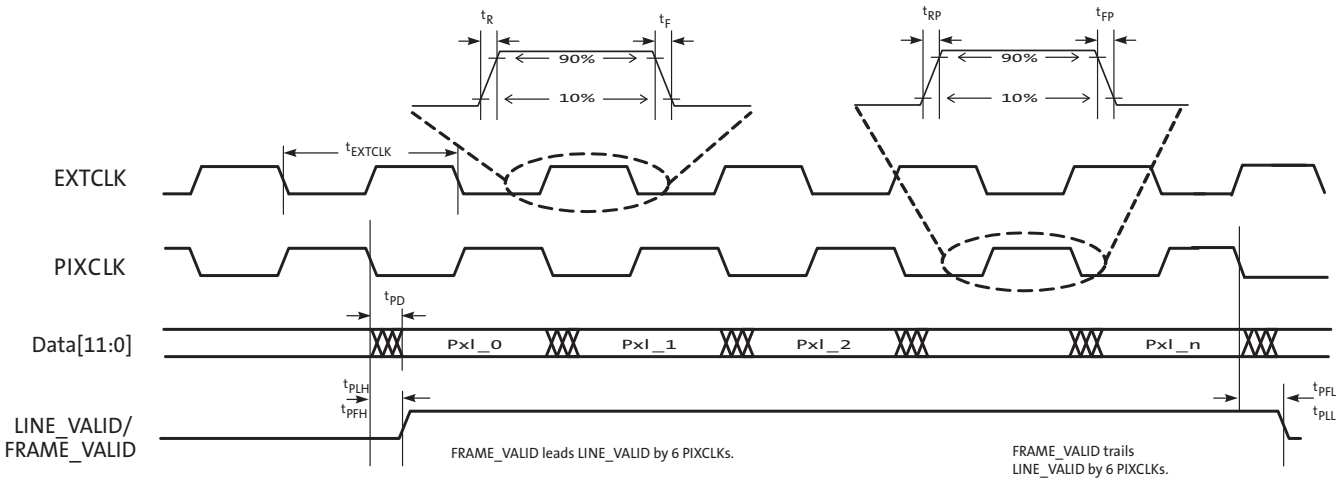


Table 6: I/O Timing Characteristics[1]

Parallel Output									
			VDD_IO=2.8V			VDD_IO=1.8V			
Symbol	Definition	Condition	Min	Typ	Max	Min	Typ	Max	Unit
f_{EXTCLK}	Input clock frequency		6		50	6		50	MHz
t_{EXTCLK}	Input clock period		20		166	20		166	ns
t_R	Input clock rise time	PLL enabled		3	4		3	4	ns
t_F	Input clock fall time	PLL enabled		3	4		3	4	ns
t_{RP}	PIXCLK rise time	Slew setting = 4 (default)	2.3		4.6	2.3		4.6	ns
t_{FP}	PIXCLK fall time	Slew setting = 4 (default)	3		4.4	3		4.4	ns
	PIXCLK duty cycle		40	50	60	40	50	60	%
f_{PIXCLK}	PIXCLK frequency[2]	Nominal voltages, PLL Enabled	6		74.25	6		74.25	MHz
t_{PD}	PIXCLK to data valid	Nominal voltages, PLL Enabled	-3	2.3	4	-3	2.3	4.5	ns

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Table 6: I/O Timing Characteristics[1] (continued)

Parallel Output									
			V_{DD}_IO=2.8V			V_{DD}_IO=1.8V			
Symbol	Definition	Condition	Min	Typ	Max	Min	Typ	Max	Unit
t_{PFH}	PIXCLK to FV HIGH	Nominal voltages, PLL Enabled	-3	1.5	4	-3	1.5	4.5	ns
t_{PLH}	PIXCLK to LV HIGH	Nominal voltages, PLL Enabled	-3	2.3	4	-3	2.3	4.5	ns
t_{PFL}	PIXCLK to FV LOW	Nominal voltages, PLL Enabled	-3	1.5	4	-3	1.5	4.5	ns
t_{PLL}	PIXCLK to LV LOW	Nominal voltages, PLL Enabled	-3	2	4	-3	2	4.5	ns

Notes: 1. Minimum and maximum values are taken at the temperature and voltage limits; for instance, 70°C ambient at 90% of V_{DD}_IO, and -30°C at 110% of VDD_IO. All values are taken at the 50% transition point. The loading used is 20pF.
2. Jitter from PIXCLK is already taken into account as the data of all the output parameters.

Table 7: I/O Rise Slew Rate (2.8V V_{DD}_IO)[1]

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Units
7	Default	1.08	1.77	2.72	V/ns
6	Default	0.77	1.26	1.94	V/ns
5	Default	0.58	0.95	1.46	V/ns
4	Default	0.44	0.70	1.08	V/ns
3	Default	0.32	0.51	0.78	V/ns
2	Default	0.23	0.37	0.56	V/ns
1	Default	0.16	0.25	0.38	V/ns
0	Default	0.10	0.15	0.22	V/ns

Note: 1. Minimum and maximum values are taken at the temperature and voltage limits; for instance, 70°C ambient at 90% of V_{DD}_IO, and -30°C at 110% of V_{DD}_IO. All values are taken at the 50% transition point. The loading used is 20pF.

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Table 8: I/O Fall Slew Rate (2.8V V_{DD}_IO)[1]

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Units
7	Default	1.00	1.62	2.41	V/ns
6	Default	0.76	1.24	1.88	V/ns
5	Default	0.60	0.98	1.50	V/ns
4	Default	0.46	0.75	1.16	V/ns
3	Default	0.35	0.56	0.86	V/ns
2	Default	0.25	0.40	0.61	V/ns
1	Default	0.17	0.27	0.41	V/ns
0	Default	0.11	0.16	0.24	V/ns

Note: 1. Minimum and maximum values are taken at the temperature and voltage limits; for instance, 70°C ambient at 90% of V_{DD}_IO, and -30°C at 110% of V_{DD}_IO. All values are taken at the 50% transition point. The loading used is 20pF.

Table 9: I/O Rise Slew Rate (1.8V V_{DD}_IO)[1]

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Units
7	Default	0.41	0.65	1.10	V/ns
6	Default	0.30	0.47	0.79	V/ns
5	Default	0.24	0.37	0.61	V/ns
4	Default	0.19	0.28	0.46	V/ns
3	Default	0.14	0.21	0.34	V/ns
2	Default	0.10	0.15	0.24	V/ns
1	Default	0.07	0.10	0.16	V/ns
0	Default	0.04	0.06	0.10	V/ns

Note: 1. Minimum and maximum values are taken at the temperature and voltage limits; for instance, 70°C ambient at 90% of V_{DD}_IO, and -30°C at 110% of V_{DD}_IO. All values are taken at the 50% transition point. The loading used is 20pF.

Table 10: I/O Fall Slew Rate (1.8V V_{DD}_IO)[1]

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Units
7	Default	0.42	0.68	1.11	V/ns
6	Default	0.32	0.51	0.84	V/ns
5	Default	0.26	0.41	0.67	V/ns
4	Default	0.20	0.32	0.52	V/ns
3	Default	0.16	0.24	0.39	V/ns
2	Default	0.12	0.18	0.28	V/ns
1	Default	0.08	0.12	0.19	V/ns
0	Default	0.05	0.07	0.11	V/ns

Notes: 1. Minimum and maximum values are taken at the temperature and voltage limits; for instance, 70°C ambient at 90% of V_{DD}_IO, and -30°C at 110% of V_{DD}_IO. All values are taken at the 50% transition point. The loading used is 20pF.

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DC Electrical Characteristics

The DC electrical characteristics are shown in Table 11, Table 12, Table 13, and Table 14.

Table 11: DC Electrical Characteristics

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{DD}	Core digital voltage		1.7	1.8	1.95	V
V_{DD_IO}	I/O digital voltage		1.7/2.5	1.8/2.8	1.9/3.1	V
V_{AA}	Analog voltage		2.5	2.8	3.1	V
V_{AA_PIX}	Pixel supply voltage		2.5	2.8	3.1	V
V_{DD_PLL}	PLL supply voltage		2.5	2.8	3.1	V
V_{DD_SLVS}	HiSPi supply voltage		0.3	0.4	0.6	V
V_{IH}	Input HIGH voltage		V_{DD_IO} * 0.7	–	–	V
V_{IL}	Input LOW voltage		–	–	V_{DD_IO} * 0.3	V
I_{IN}	Input leakage current	No pull-up resistor; V_{IN} = V_{DD_IO} or D_{GND}	20	–	–	µA
V_{OH}	Output HIGH voltage		V_{DD_IO} – 0.3	–	–	V
V_{OL}	Output LOW voltage	V_{DD_IO} = 2.8V	–	–	0.4	V
I_{OH}	Output HIGH current	At specified V_{OH}	–22	–	–	mA
I_{OL}	Output LOW current	At specified V_{OL}	–	–	22	mA

Caution **Stresses greater than those listed in Table 12 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.**

Table 12: Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Symbol
V_{SUPPLY}	Power supply voltage (all supplies)	–0.3	4.5	V	V_{SUPPLY}
I_{SUPPLY}	Total power supply current	–	200	mA	I_{SUPPLY}
I_{GND}	Total ground current	–	200	mA	I_{GND}
V_{IN}	DC input voltage	–0.3	V_{DD_IO} + 0.3	V	V_{IN}
V_{OUT}	DC output voltage	–0.3	V_{DD_IO} + 0.3	V	V_{OUT}
T_{STG}[1]	Storage temperature	–40	+85	°C	T_{STG}[1]

Note: 1. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 13: Operating Current Consumption for Parallel Output

V_{AA} = V_{AA_PIX} = V_{DD_IO} = V_{DD_PLL} = 2.8V; V_{DD}= 1.8V; PLL Enabled and PIXCLK = 74.25 MHz; T_A = 25°C; C_{LOAD} = 10pF

	Condition	Symbol	Min	Typ	Max	Unit
Digital operating current	Parallel, Streaming, Full resolution 45 fps	I_{DD1}		45	55	mA
I/O digital operating current	Parallel, Streaming, Full resolution 45 fps	I_{DD_IO}		50[1]	–	mA
Analog operating current	Parallel, Streaming, Full resolution 45 fps	I_{AA}		45	50	mA
Pixel supply current	Parallel, Streaming, Full resolution 45 fps	I_{AA_PIX}		6	10	mA
PLL supply current	Parallel, Streaming, Full resolution 45 fps	I_{DD_PLL}		6	8	mA

Note: 1. I_{DD_IO} operating current is specified with image at 1/2 saturation level.

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Table 14: Standby Current Consumption
Analog - V_{AA} + V_{AA_PIX} + V_{DD_PLL}; Digital - V_{DD} + V_{DD_IO}; T_A = 25°C

Definition	Condition	Min	Typ	Max	Unit
Hard standby (clock off, driven low)	Analog, 2.8V	–	3	10	µA
	Digital, 1.8V	–	8	75	µA
Hard standby (clock on, EXTCLK = 20 MHz)	Analog, 2.8V	–	12	20	µA
	Digital, 1.8V	–	0.87	1.3	mA
Soft standby (clock off, driven low)	Analog, 2.8V	–	3	10	µA
	Digital, 1.8V	–	8	75	µA
Soft standby (clock on, EXTCLK = 20 MHz)	Analog, 2.8V	–	12	20	µA
	Digital, 1.8V	–	0.87	1.3	mA

HiSPi Electrical Specifications

The ON Semiconductor MT9M021/MT9M031 sensor supports SLVS mode only, and does not have a DLL for timing adjustments. Refer to the High-Speed Serial Pixel (HiSPi) Interface Physical Layer Specification v2.00.00 for electrical definitions, specifications, and timing information. The V_{DD_SLVS} supply in this datasheet corresponds to V_{DD_TX} in the HiSPi Physical Layer Specification. Similarly, V_{DD} is equivalent to V_{DD_HiSPi} as referenced in the specification. The HiSPi transmitter electrical specifications are listed at 700 MHz.

Table 15: Input Voltage and Current (HiSPi Power Supply 0.4 V)
Measurement Conditions: Max Freq 700 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Supply current (PWRHiSPi) (driving 100Ω load)	I_{DD_SLVS}	–	10	15	mA
HiSPi common mode voltage (driving 100Ω load)	V_{CMD}	V_{DD_SLVS} x 0.45	$V_{DD_SLVS}/2$	V_{DD_SLVS} x 0.55	V
HiSPi differential output voltage (driving 100Ω load)	$\|V_{OD}\|$	V_{DD_SLVS} x 0.36	$V_{DD_SLVS}/2$	V_{DD_SLVS} x 0.64	V
Change in V_{CM} between logic 1 and 0	ΔV_{CM}			25	mV
Change in $\|V_{OD}\|$ between logic 1 and 0	$\|V_{OD}\|$			25	mV
Vod noise margin	NM	–		30	%
Difference in V_{CM} between any two channels	$\|\Delta V_{CM}\|$			50	mV
Difference in V_{OD} between any two channels	$\|\Delta V_{OD}\|$			100	mV
Common-mode AC voltage (pk) without V_{CM} cap termination	ΔV_{CM_ac}			50	mV
Common-mode AC voltage (pk) with V_{CM} cap termination	ΔV_{CM_ac}			30	mV
Max overshoot peak $\|V_{OD}\|$	V_{OD_ac}			1.3 x $\|V_{OD}\|$	V
Max overshoot Vdiff pk-pk	V_{diff_pkpk}			2.6 x $\|V_{OD}\|$	V
Eye Height	V_{eye}	1.4 x V_{OD}			
Single-ended output impedance	Ro	35	50	70	Ω
Output impedance mismatch	ΔRo			20	%

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Figure 8: Differential Output Voltage for Clock or Data Pairs

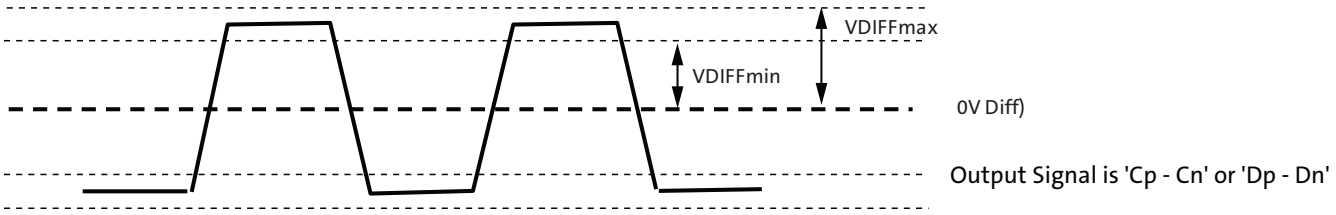


Table 16: Rise and Fall Times
Measurement Conditions: HiSPi Power Supply 0.4V, Max Freq 700 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Data Rate	1/UI	280	–	700	Mb/s
Max setup time from transmitter	TxPRE	0.3	–	–	UI[1]
Max hold time from transmitter	TxPost	0.3	–	–	UI
Rise time (20% - 80%)	RISE	–	0.25UI	–	
Fall time (20% - 80%)	FALL	150ps	0.25 UI	–	
Clock duty	PLL_DUTY	45	50	55	%
Bitrate Period	t_{pw}	1.43		3.57	ns[1]
Eye Width	t_{eye}	0.3			UI[1, 2]
Data Total jitter (pk pk)@1e-9	$t_{totaljit}$			0.2	UI[1, 2]
Clock Period Jitter(RMS)	t_{ckjit}			50	ps[2]
Clock cycle to cycle jitter (RMS)	t_{cyjit}			100	ps[2]
Clock to Data Skew	t_{chskew}	-0.1		0.1	UI[1, 2]
PHY-to-PHY Skew	$t_{\|PHYskew\|}$			2.1	UI[1, 5]
Mean diferential skew	$t_{DIFFSKEW}$	–100		100	ps[6]

Notes:
1. One UI is defined as the normalized mean time between one edge and the following edge of the clock.
2. Taken from 0V crossing point w/ DLL off.
3. Also defined with a maximum loading capacitance of 10pF on any pin. The loading capacitance may also need to be less for higher bitrates so the rise and fall times do not exceed the maximum 0.3UI.
4. The absolute mean skew between the Clock lane and any Data Lane in the same PHY between any edges.
5. The absolute mean skew between any Clock in one PHY and any Data lane in any other PHY between any edges.
6. Differential skew is defined as the skew between complementary outputs. It is measured as the absolute time between the two complementary edges at mean V_{CM} point.

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Figure 9: Eye Diagram for Clock and Data Signals

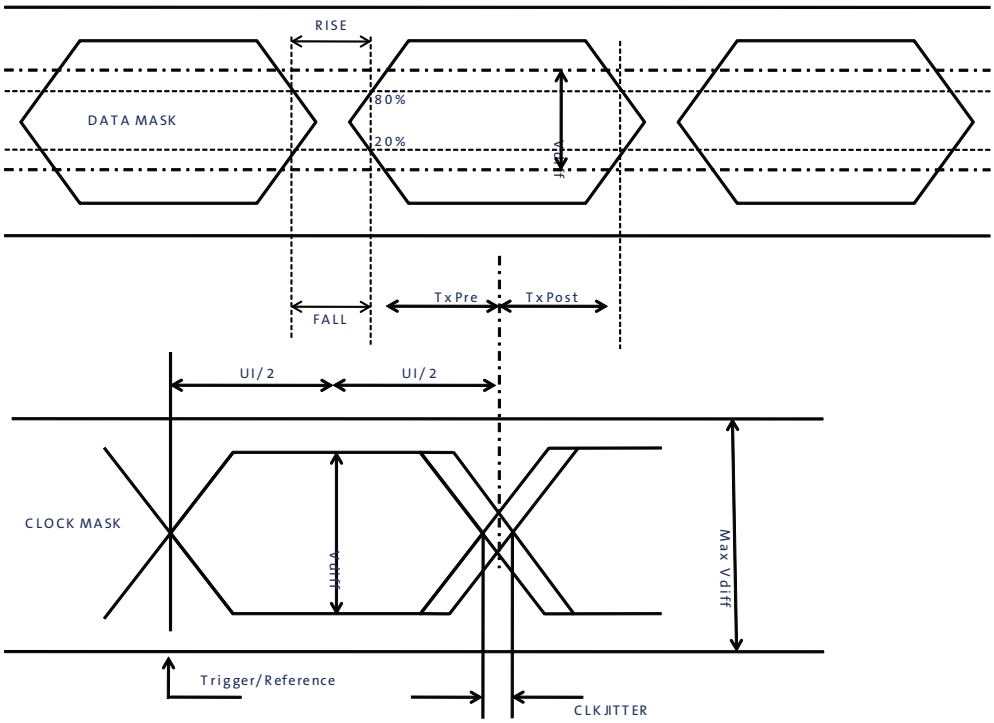
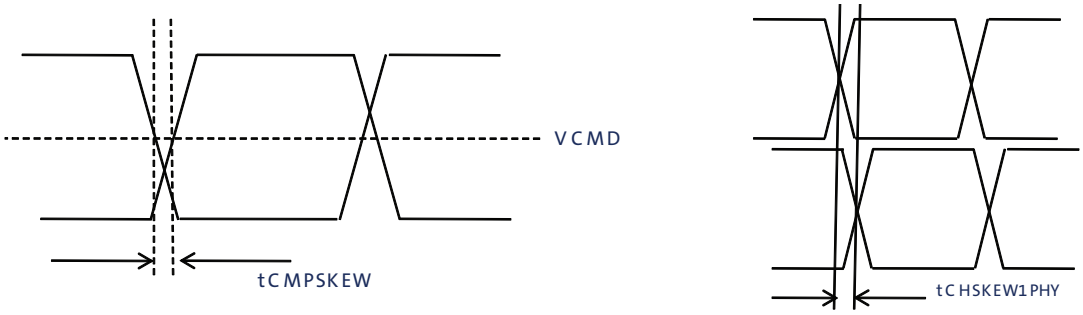


Figure 10: Skew Within the PHY and Output Channels



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Power-On Reset and Standby Timing

Power-Up Sequence

The recommended power-up sequence for the MT9M021/MT9M031 is shown in Figure 11. The available power supplies (VDD_IO, VDD, VDD_SLVS, VDD_PLL, VAA, VAA_PIX) must have the separation specified below.

1. Turn on VDD_PLL power supply.
2. After 0–10µs, turn on VAA and VAA_PIX power supply.
3. After 0–10µs, turn on VDD_IO power supply.
4. After the last power supply is stable, enable EXTCLK.
5. Assert RESET_BAR for at least 1ms.
6. Wait 150000 EXTCLKs (for internal initialization into software standby.
7. Configure PLL, output, and image settings to desired values.
8. Wait 1ms for the PLL to lock.
9. Set streaming mode (R0x301a[2] = 1).

Figure 11: Power Up

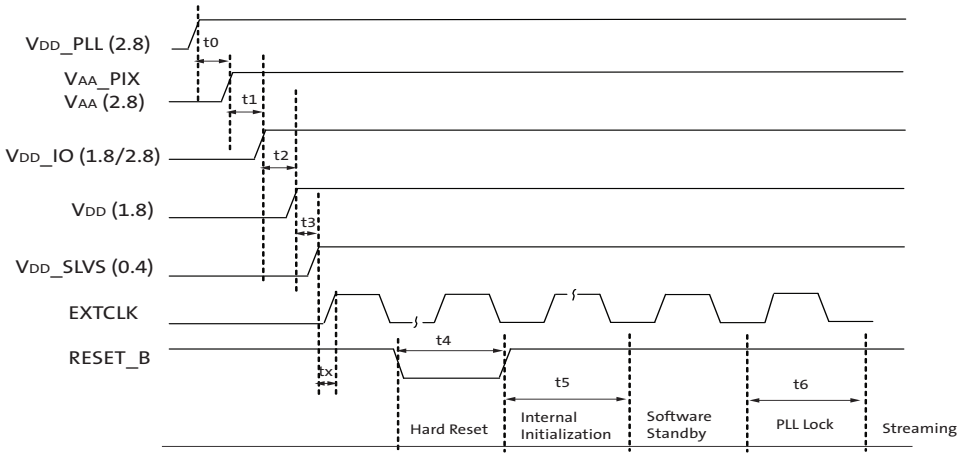


Table 17: Power-Up Sequence

Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD_PLL to VAA/VAA_PIX	t0	0	10	–	µs
VAA/VAA_PIX to VDD_IO	t1	0	10	–	µs
VDD_IO to VDD	t2	0	10	–	µs
VDD to VDD_SLVS	t3	0	10	–	µs
Xtal settle time	tx	–	30[1]	–	ms
Hard Reset	t4	1[2]	–	–	ms
Internal Initialization	t5	150000	–	–	EXTCLKs
PLL Lock Time	t6	1	–	–	ms

Notes:
1. Xtal settling time is component-dependent, usually taking about 10 – 100 ms.
2. Hard reset time is the minimum time required after power rails are settled. In a circuit where hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.
3. It is critical that VDD_PLL is not powered up after the other power supplies. It must be powered before or at least at the same time as the others. If the case happens that VDD_PLL is powered after

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other supplies then the sensor may have functionality issues and will experience high current draw on this supply.

Power-Down Sequence

The recommended power-down sequence for the MT9M021/MT9M031 is shown in Figure 12. The available power supplies (VDD_IO, VDD, VDD_SLVS, VDD_PLL, VAA, VAA_PIX) must have the separation specified below.

1. Disable streaming if output is active by setting standby R0x301a[2] = 0
2. The soft standby state is reached after the current row or frame, depending on configuration, has ended.
3. Turn off VDD_SLVS.
4. Turn off VDD.
5. Turn off VDD_IO
6. Turn off VAA/VAA_PIX.
7. Turn off VDD_PLL.

Figure 12: Power Down

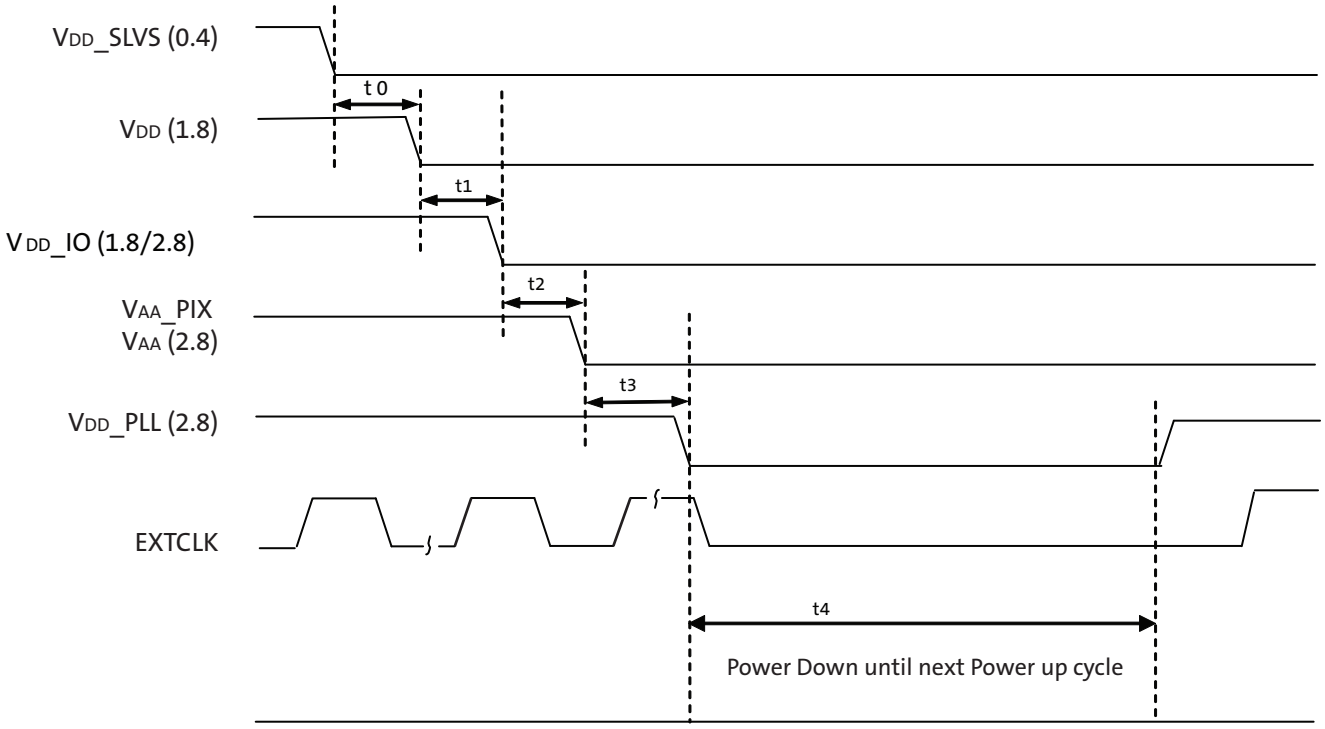


Table 18: Power-Down Sequence

Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD_SLVS to VDD	t0	0	–	–	µS
VDD to VDD_IO	t1	0	–	–	µS
VDD_IO to VAA/VAA_PIX	t2	0	–	–	µS
VAA/VAA_PIX to VDD_PLL	t3	0	–	–	µS

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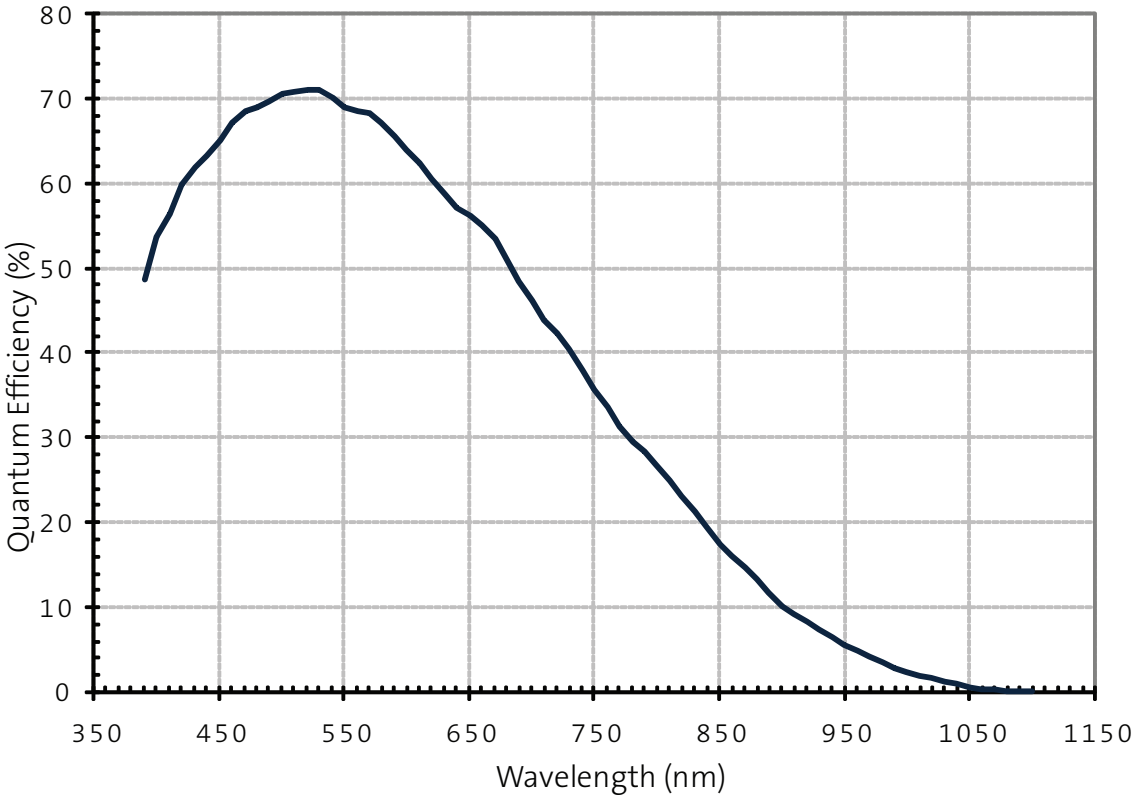
Table 18: Power-Down Sequence

Definition	Symbol	Minimum	Typical	Maximum	Unit
PwrDn until Next PwrUp Time	t4	100	–	–	mS

Note: t4 is required between power down and next power up time; all decoupling caps from regulators must be completely discharged.

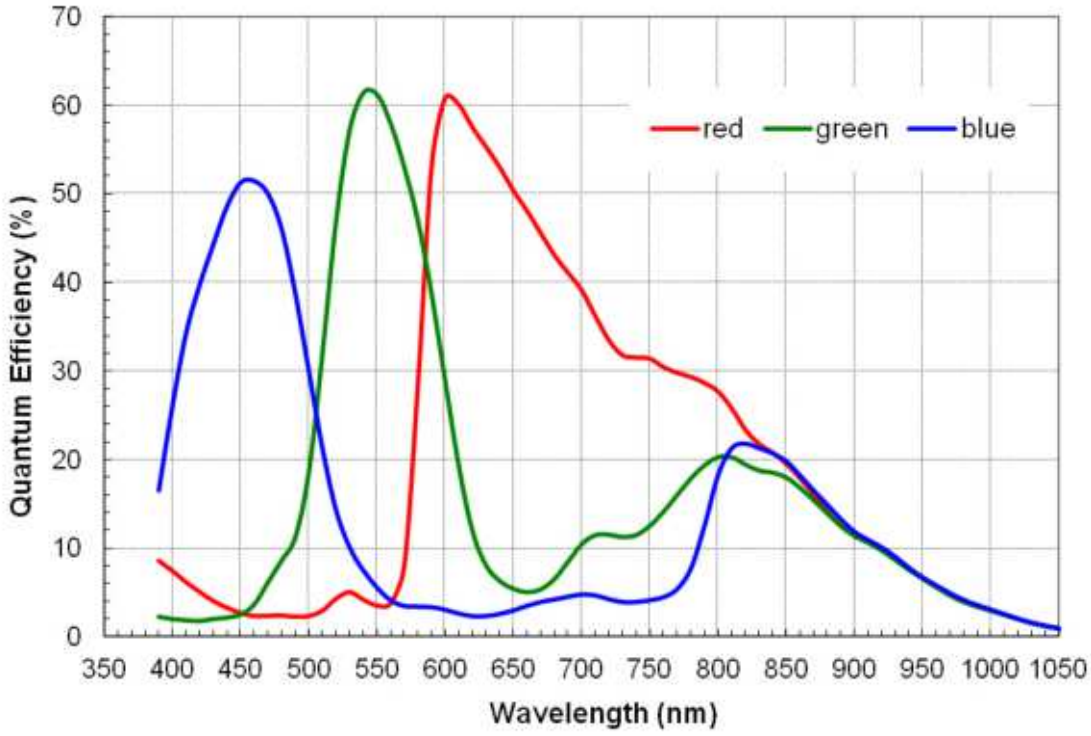
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Figure 13: Quantum Efficiency – Monochrome Sensor



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Figure 14: Quantum Efficiency – Color Sensor

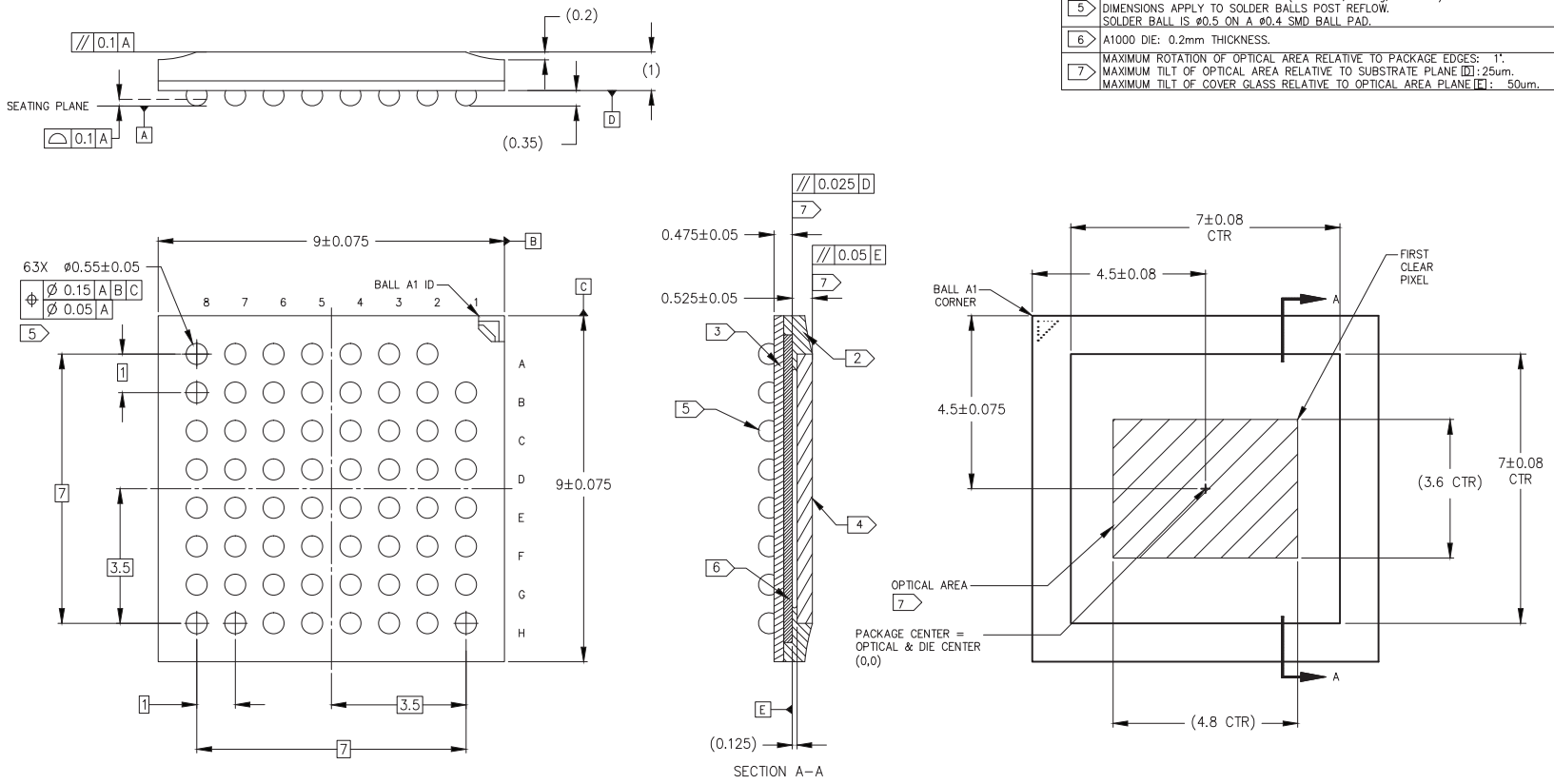


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Package Dimensions

Figure 15: 64-Ball iBGA Package Outline Drawing (Case 503AQ)

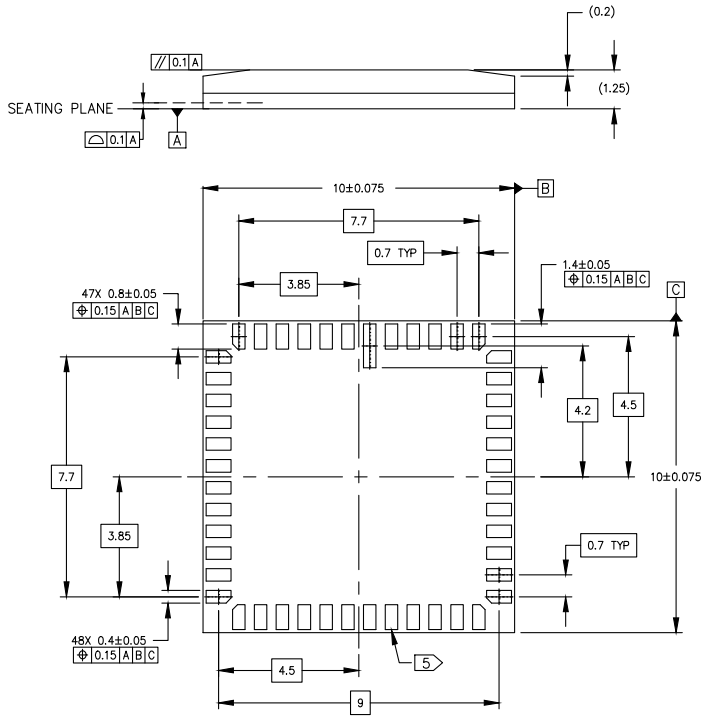
NOTES	
1	DIMENSIONS IN MM. DIMENSIONS IN ( ) ARE FOR REFERENCE ONLY.
2	ENCAPSULANT: EPOXY.
3	SUBSTRATE MATERIAL: PLASTIC LAMINATE 0.25 THICKNESS.
4	LID MATERIAL: BOROSILICATE GLASS 0.4±0.04 THICKNESS. REFRACTIVE INDEX AT 20C° = 1.5255 @ 546nm & 1.5231 @ 588nm.
5	SOLDER BALL MATERIAL: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu). DIMENSIONS APPLY TO SOLDER BALLS POST REFLOW. SOLDER BALL IS ø0.5 ON A ø0.4 SMD BALL PAD.
6	A1000 DIE: 0.2mm THICKNESS.
7	MAXIMUM ROTATION OF OPTICAL AREA RELATIVE TO PACKAGE EDGES: 1°. MAXIMUM TILT OF OPTICAL AREA RELATIVE TO SUBSTRATE PLANE D: 25um. MAXIMUM TILT OF COVER GLASS RELATIVE TO OPTICAL AREA PLANE E: 50um.

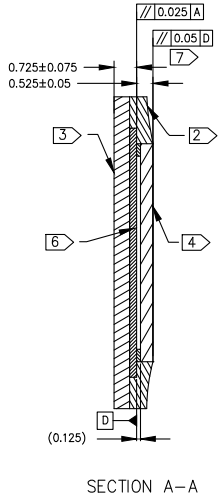


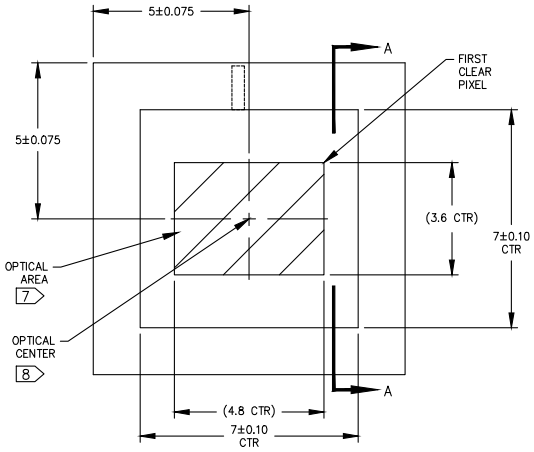
Note: All dimensions in millimeters.

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Figure 16: 48-pin iLCC Package Drawing (Case 847AJ)







NOTES	
1	DIMENSIONS IN MM. DIMENSIONS IN ( ) ARE FOR REFERENCE ONLY
2	ENCAPSULANT: EPOXY
3	SUBSTRATE MATERIAL: EPOXY LAMINATE 0.5 THICKNESS
4	LID MATERIAL: BOROSILICATE GLASS 0.4 THICKNESS. REFRACTIVE INDEX AT 20°C = 1.5255 @ 546nm & 1.5231 @ 588nm
5	LEAD FINISH: GOLD PLATING, 0.5 MICRONS MINIMUM THICKNESS
6	IMAGE SENSOR DIE 0.2 THICKNESS
7	MAXIMUM ROTATION OF OPTICAL AREA RELATIVE TO PACKAGE EDGES: 1°. MAXIMUM TILT OF OPTICAL AREA RELATIVE TO SEATING PLANE [A]: 25 MICRONS MAXIMUM TILT OF OPTICAL AREA RELATIVE TO TOP OF COVER GLASS [D]: 50 MICRONS
8	OPTICAL CENTER = PACKAGE CENTER

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