DDR SDRAM SODIMM

MT9VDDT1672H – 128MB[1]
MT9VDDT3272H – 256MB
MT9VDDT6472H – 512MB

For component data sheets, refer to Micron's Web site: www.micron.com

Features

- 200-pin, small-outline dual in-line memory module (SODIMM)
- Fast data transfer rates: PC2100, PC2700, or PC3200
- 128MB (16 Meg x 72), 256MB (32 Meg x 72), and 512MB (64 Meg x 72)
- Supports ECC error detection and correction
- V_{DD} = $V_{DD}Q$ = +2.5V (-40B: V_{DD} = $V_{DD}Q$ = +2.6V)
- V_{DDSPD} = +2.3V to +3.6V
- 2.5V I/O (SSTL_2-compatible)
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/ received with data—that is, source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Multiple internal device banks for concurrent operation
- Selectable burst lengths (BL) 2, 4, or 8
- Auto precharge option
- Auto refresh and self refresh modes: 15.625µs (128MB) and 7.8125µs (256MB, 512MB) maximum average periodic refresh interval
- Serial presence-detect (SPD) with EEPROM
- Selectable CAS latency (CL) for maximum compatibility
- Single rank
- Gold edge contacts

200-Pin SODIMM (MO-224) Figures

Figure 1: Low-Profile Layout

PCB height: 31.75mm (1.25in)

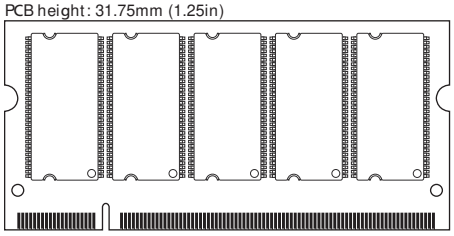
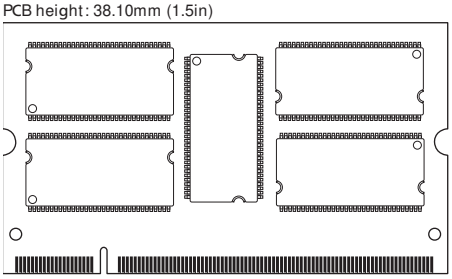


Figure 2: Standard Layout

PCB height: 38.10mm (1.5in)



Options — Marking

- Operating temperature[2]
  - Commercial (0°C ≤ T_A ≤ +70°C) — None
  - Industrial (–40°C ≤ T_A ≤ +85°C) — I
- Package
  - 200-pin DIMM (standard) — G
  - 200-pin DIMM (Pb-free) — Y
- Memory clock, speed, CAS latency
  - 5.0ns (200 MHz), 400 MT/s, CL = 3.0 — -40B
  - 6.0ns (167 MHz), 333 MT/s, CL = 2.5 — -335
  - 7.5ns (133 MHz), 266 MT/s, CL = 2.0[3] — -262
  - 7.5ns (133 MHz), 266 MT/s, CL = 2.0[3] — -26A
  - 7.5ns (133 MHz), 266 MT/s, CL = 2.5[3] — -265

Notes: 1. End of life.
2. Contact Micron for industrial temperature module offerings.
3. Not recommended for new designs.

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Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)			^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)	Notes
		CL = 3	CL = 2.5	CL = 2				
-40B	PC3200	400	333	266	15	15	55	
-335	PC2700	–	333	266	18	18	60	1
-262	PC2100	–	266	266	15	15	60	
-26A	PC2100	–	266	266	20	20	65	
-265	PC2100	–	266	200	20	20	65	

Notes: 1. The values of ^{t}RCD and ^{t}RP for -335 modules show 18ns to align with industry specifications; actual DDR SDRAM device specifications are 15ns.

Table 2: Addressing

Parameter	128MB	256MB	512MB
Refresh count	4K	8K	8K
Row address	8K (A0–A11)	8K (A0–A12)	8K (A0–A12)
Device bank address	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Device configuration	128Mb (16 Meg x 8)	256Mb (32 Meg x 8)	512Mb (64 Meg x 8)
Column address	1K (A0–A9)	1K (A0–A9)	2K (A0–A9, A11)
Module rank address	1 (S0#)	1 (S0#)	1 (S0#)

Table 3: Part Numbers and Timing Parameters – 128MB Modules

Base device: MT46V16M8,[1] 128Mb DDR SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT9VDDT1672HG-335__	128MB	16 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT9VDDT1672HY-335__	128MB	16 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT9VDDT1672HY-262__	128MB	16 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT9VDDT1672HG-26A__	128MB	16 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT9VDDT1672HG-265__	128MB	16 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3

Table 4: Part Numbers and Timing Parameters – 256MB Modules

Base device: MT46V32M8,[1] 256Mb DDR SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT9VDDT3272HG-40B__	256MB	32 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT9VDDT3272HY-40B__	256MB	32 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT9VDDT3272HG-335__	256MB	32 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT9VDDT3272HY-335__	256MB	32 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT9VDDT3272HG-262__	256MB	32 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT9VDDT3272HG-265__	256MB	32 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT9VDDT3272HY-265__	256MB	32 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3

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Table 5: Part Numbers and Timing Parameters – 512MB Modules

Base device: MT46V64M8,[1] 512Mb DDR SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT9VDDT6472HG-40B__	512MB	64 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT9VDDT6472HY-40B__	512MB	64 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT9VDDT6472HG-335__	512MB	64 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT9VDDT6472HY-335__	512MB	64 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT9VDDT6472HG-26A__	512MB	64 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT9VDDT6472HG-265__	512MB	64 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3

Notes:
1. Data sheets for the base devices can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT9VDDT6472HY-335F2.

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Pin Assignments and Descriptions

Table 6: Pin Assignments

200-Pin SODIMM Front								200-Pin SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	51	VSS	101	A9	151	DQ42	2	VREF	52	VSS	102	A8	152	DQ46
3	VSS	53	DQ19	103	VSS	153	DQ43	4	VSS	54	DQ23	104	VSS	154	DQ47
5	DQ0	55	DQ24	105	A7	155	VDD	6	DQ4	56	DQ28	106	A6	156	VDD
7	DQ1	57	VDD	107	A5	157	VDD	8	DQ5	58	VDD	108	A4	158	CK1#
9	VDD	59	DQ25	109	A3	159	VSS	10	VDD	60	DQ29	110	A2	160	CK1
11	DQS0	61	DQS3	111	A1	161	VSS	12	DM0	62	DM3	112	A0	162	VSS
13	DQ2	63	VSS	113	VDD	163	DQ48	14	DQ6	64	VSS	114	VDD	164	DQ52
15	VSS	65	DQ26	115	A10	165	DQ49	16	VSS	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	VDD	18	DQ7	68	DQ31	118	RAS#	168	VDD
19	DQ8	69	VDD	119	WE#	169	DQS6	20	DQ12	70	VDD	120	CAS#	170	DM6
21	VDD	71	CB0	121	S0#	171	DQ50	22	VDD	72	CB4	122	NC	172	DQ54
23	DQ9	73	CB1	123	NC	173	VSS	24	DQ13	74	CB5	124	NC	174	VSS
25	DQS1	75	VSS	125	VSS	175	DQ51	26	DM1	76	VSS	126	VSS	176	DQ55
27	VSS	77	DQS8	127	DQ32	177	DQ56	28	VSS	78	DM8	128	DQ36	178	DQ60
29	DQ10	79	CB2	129	DQ33	179	VDD	30	DQ14	80	CB6	130	DQ37	180	VDD
31	DQ11	81	VDD	131	VDD	181	DQ57	32	DQ15	82	VDD	132	VDD	182	DQ61
33	VDD	83	CB3	133	DQS4	183	DQS7	34	VDD	84	CB7	134	DM4	184	DM7
35	CK0	85	NC	135	DQ34	185	VSS	36	VDD	86	NC	136	DQ38	186	VSS
37	CK0#	87	VSS	137	VSS	187	DQ58	38	VSS	88	VSS	138	VSS	188	DQ62
39	VSS	89	CK2	139	DQ35	189	DQ59	40	VSS	90	VSS	140	DQ39	190	DQ63
41	DQ16	91	CK2#	141	DQ40	191	VDD	42	DQ20	92	VDD	142	DQ44	192	VDD
43	DQ17	93	VDD	143	VDD	193	SDA	44	DQ21	94	VDD	144	VDD	194	SA0
45	VDD	95	NC	145	DQ41	195	SCL	46	VDD	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	VDDSPD	48	DM2	98	NC	148	DM5	198	SA2
49	DQ18	99[1]	NC/A12	149	VSS	199	NC	50	DQ22	100	A11	150	VSS	200	NC

Notes: 1. Pin 99 is NC for 128MB and A12 for 256MB and 512MB.

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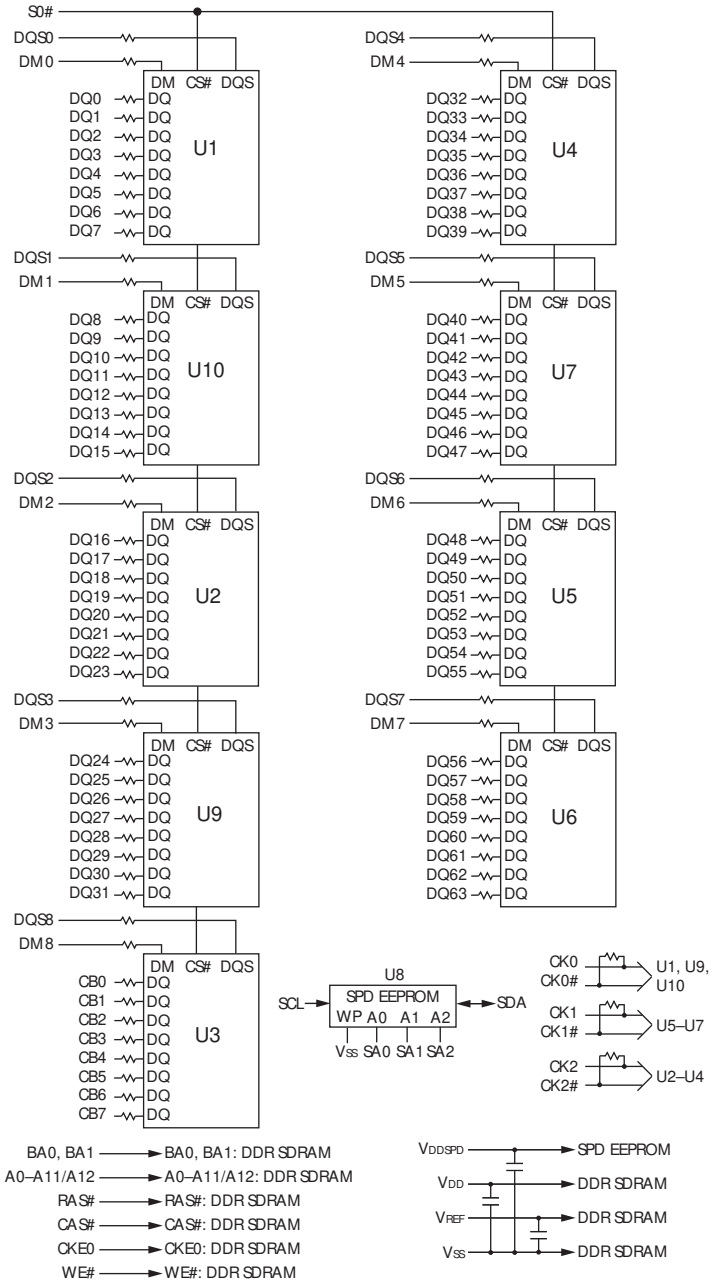
Table 7: Pin Descriptions

Symbol	Type	Description
A0–A12	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command. A0–A11 (128MB) and A0–A12 (256MB, 512MB).
BA0, BA1	Input	**Bank address:** BA0 and BA1 define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
CK0, CK0#, CK1, CK1# CK2, CK2#	Input	**Clock:** CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.
CKE0	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) the internal clock, input buffers, and output drivers.
DM0–DM8	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of the DQ and DQS pins.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
S0#	Input	**Chip selects:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA0–SA2	Input	**Presence-detect address inputs:** These pins are used to configure the presence-detect device.
SCL	Input	**Serial clock for presence-detect:** SCL is used to synchronize the presence-detect data transfer to and from the module.
CB0–CB7	I/O	Check bits.
DQ0–DQ63	I/O	**Data input/output:** Data bus.
DQS0–DQS8	I/O	**Data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data. Used to capture data.
SDA	I/O	**Serial presence-detect data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
V_{DD}	Supply	**Power supply:** +2.5V ±0.2V (-40B: +2.6V ±0.1V).
V_{DDSPD}	Supply	**Serial EEPROM positive power supply:** +2.3V to +3.6V.
V_{REF}	Supply	SSTL_2 reference voltage (V_{DD}/2).
V_{SS}	Supply	Ground.
NC	–	**No connect:** These pins are not connected on the module.

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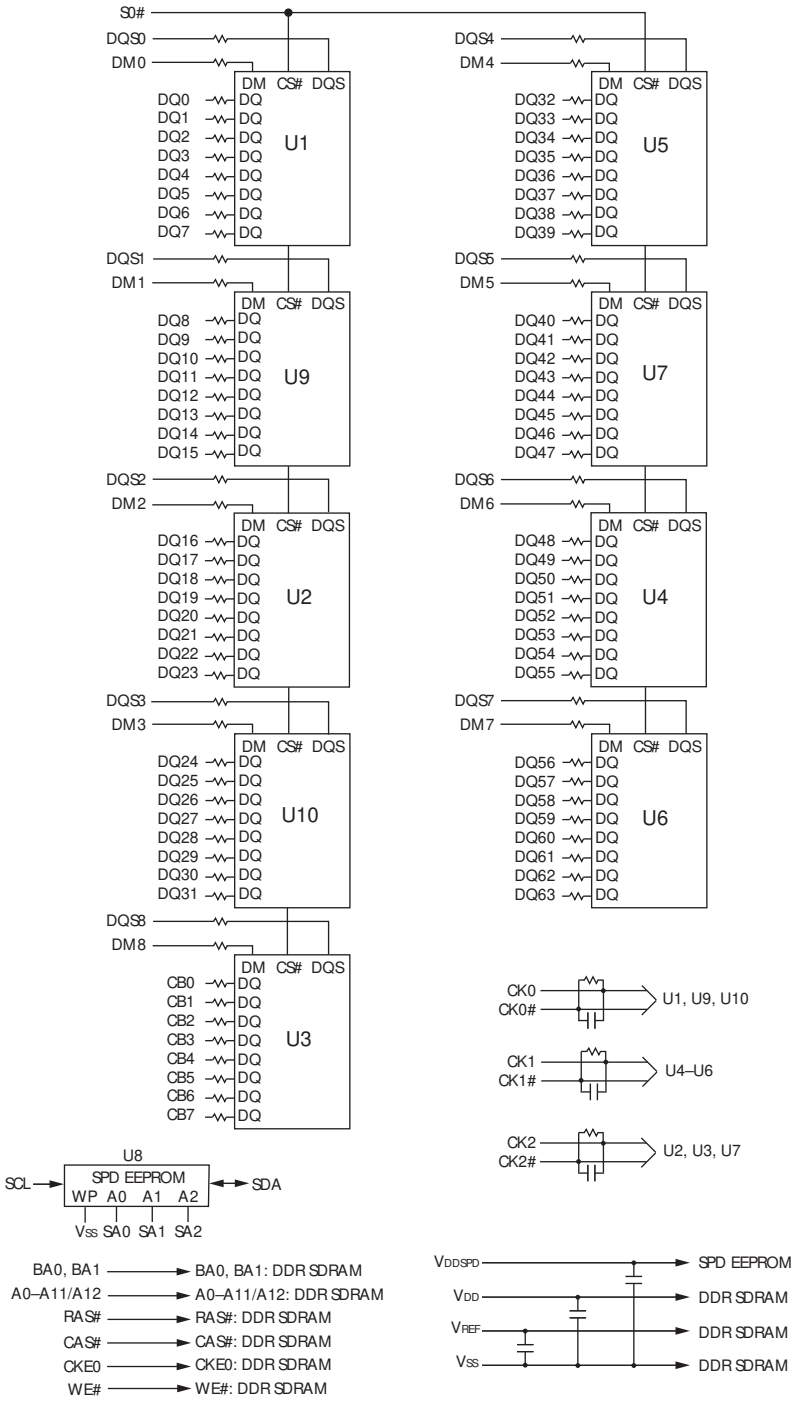
Functional Block Diagrams

Figure 3: Functional Block Diagram – Low-Profile Layout



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Figure 4: Functional Block Diagram – Standard Layout



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General Description

The MT9VDDT1672H, MT9VDDT3272H, and MT9VDDT6472H are high-speed, CMOS dynamic random access, 128MB, 256MB, and 512MB memory modules organized in a x72 configuration. These modules use DDR SDRAM devices with four internal banks.

DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $2n$-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for DDR SDRAM modules effectively consists of a single $2n$-bit-wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR SDRAM modules operate from differential clock inputs (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Serial Presence-Detect Operation

DDR SDRAM modules incorporate serial presence-detect. The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to V_{SS} on the module, permanently disabling hardware write protect.

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Electrical Specifications

Stresses greater than those listed in Table 8 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated on the device data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 8: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}		–1.0	+3.6	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		–0.5	+3.2	V
I_I	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤ 1.35V (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, BA, S#, CKE	–18	+18	µA
		CK, CK#	–6	+6	
		DM	–2	+2	
I_{OZ}	Output leakage current; 0V ≤ V_{OUT} ≤ $V_{DD}Q$; DQ are disabled	DQ, DQS	–5	+5	µA
T_A	DRAM ambient operating temperature[1]	Commercial	0	+70	°C
		Industrial	–40	+85	°C

Notes: 1. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.

Input Capacitance

Micron encourages designers to simulate the performance of the module to achieve optimum values. Simulations are significantly more accurate and realistic than a gross estimation of module capacitance when inductance and delay parameters associated with trace lengths are used in simulations. JEDEC modules are currently designed using simulations to close timing budgets.

Component AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 9.

Table 9: Module and Component Speed Grades
DDR components meet or exceed the listed module speed grades

Module Speed Grade	Component Speed Grade
-40B	-5
-335	-6
-262	-75E
-26A	-75Z
-265	-75

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IDD Specifications

Table 10: IDD Specifications and Conditions – 128MB
Values are shown for the MT46V16M8 DDR SDRAM only and are computed from values specified in the 128Mb (16 Meg x 8) component data sheet

Parameter/Condition		Symbol	-335	-262	-26A/ -265	Units
Operating one bank active-precharge current: $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		IDD0	1,125	990	945	mA
Operating one bank active-read-precharge current: BL = 4; $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle		IDD1	1,215	1,080	1,080	mA
Precharge power-down standby current: All device banks idle; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = LOW		IDD2P	27	27	27	mA
Idle standby current: CS# = HIGH; All device banks idle; $^{t}CK = {}^{t}CK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DM, and DQS		IDD2F	405	405	360	mA
Active power-down standby current: One device bank active; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = LOW		IDD3P	225	225	180	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; $^{t}RC = {}^{t}RAS$ (MAX); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		IDD3N	450	450	405	mA
Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); I_{OUT} = 0mA		IDD4R	1,260	1,170	1,125	mA
Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W	1,260	1,125	1,080	mA
Auto refresh current	$^{t}REFC = {}^{t}RFC$ (MIN)	IDD5	2,385	1,980	1,980	mA
	$^{t}REFC$ = 15.625µs	IDD5A	45	45	45	
Self refresh current: CKE ≤ 0.2V		IDD6	27	27	18	mA
Operating bank interleave read current: Four device bank interleaving reads (BL = 4) with auto precharge; $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); Address and control inputs change only during active READ or WRITE commands		IDD7	3,195	2,970	2,925	mA

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Table 11: IDD Specifications and Conditions – 256MB

Values are shown for the MT46V32M8 DDR SDRAM only and are computed from values specified in the 256Mb (32 Meg x 8) component data sheet

Parameter/Condition		Symbol	-40B	-335	-262	-265	Units
Operating one bank active-precharge current: $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		IDD0	1,215	1,125	1,125	1,080	mA
Operating one bank active-read-precharge current: BL = 4; $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle		IDD1	1,530	1,530	1,440	1,305	mA
Precharge power-down standby current: All device banks idle; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = LOW		IDD2P	36	36	36	36	mA
Idle standby current: CS# = HIGH; All device banks idle; $^{t}CK = {}^{t}CK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DM, and DQS		IDD2F	540	450	405	405	mA
Active power-down standby current: One device bank active; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = LOW		IDD3P	360	270	225	270	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; $^{t}RC = {}^{t}RAS$ (MAX); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		IDD3N	630	540	450	450	mA
Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); I_{OUT} = 0mA		IDD4R	1,800	1,575	1,350	1,350	mA
Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W	1,755	1,575	1,350	1,350	mA
Auto refresh current	$^{t}REFC = {}^{t}RFC$ (MIN)	IDD5	2,340	2,295	2,115	2,205	mA
	$^{t}REFC$ = 7.8125µs	IDD5A	54	54	54	54	
Self refresh current: CKE ≤ 0.2V		IDD6	36	36	36	36	mA
Operating bank interleave read current: Four device bank interleaving reads (BL = 4) with auto precharge; $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); Address and control inputs change only during active READ or WRITE commands		IDD7	4,230	3,690	3,150	3,285	mA

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Table 12: IDD Specifications and Conditions – 512MB

Values are shown for MT46V64M8 DDR SDRAM only and are computed from values specified in the 512Mb (64 Meg x 8) component data sheet

Parameter/Condition		Symbol	-40B	-335	-26A/ -265	Units
Operating one bank active-precharge current: $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		IDD0	1,395	1,170	1,035	mA
Operating one bank active-read-precharge current: BL = 4; $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle		IDD1	1,665	1,440	1,305	mA
Precharge power-down standby current: All device banks idle; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = LOW		IDD2P	45	45	45	mA
Idle standby current: CS# = HIGH; All device banks idle; $^{t}CK = {}^{t}CK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DM, and DQS		IDD2F	495	405	360	mA
Active power-down standby current: One device bank active; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = LOW		IDD3P	405	315	270	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; $^{t}RC = {}^{t}RAS$ (MAX); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		IDD3N	540	450	405	mA
Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); I_{OUT} = 0mA		IDD4R	1,710	1,485	1,305	mA
Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W	1,775	1,575	1,215	mA
Auto refresh current	$^{t}REFC = {}^{t}RFC$ (MIN)	IDD5	3,105	2,610	2,520	mA
	$^{t}REFC$ = 7.8125µs	IDD5A	99	90	90	
Self refresh current: CKE ≤ 0.2V		IDD6	45	45	45	mA
Operating bank interleave read current: Four device bank interleaving reads (BL = 4) with auto precharge; $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); Address and control inputs change only during active READ or WRITE commands		IDD7	4,050	3,645	3,150	mA

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Serial Presence-Detect

Table 13: Serial Presence-Detect EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	2.3	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	–1.0	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
Standby current: SCL = SDA = V_{DD} - 0.3V; All other inputs = V_{SS} or V_{DD}	I_{SB}	–	30	µA
Power supply current: SCL clock frequency = 100 kHz	I_{CC}	–	2.0	mA

Table 14: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^{t}BUF	1.3	–	µs	
Data-out hold time	^{t}DH	200	–	ns	
Clock/data fall time	^{t}F	–	300	ns	2
Clock/data rise time	^{t}R	–	300	ns	2
Data-in hold time	$^{t}HD:DAT$	0	–	µs	
Start condition hold time	$^{t}H:STA$	0.6	–	µs	
Clock HIGH period	$^{t}HIGH$	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I	–	50	ns	
Clock LOW period	^{t}LOW	1.3	–	µs	
SCL clock frequency	^{f}SCL	–	400	kHz	
Data-in setup time	$^{t}SU:DAT$	100	–	ns	
Start condition setup time	$^{t}SU:STA$	0.6	–	µs	3
Stop condition setup time	$^{t}SU:STO$	0.6	–	µs	
WRITE cycle time	^{t}WRC	–	10	ms	4

Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

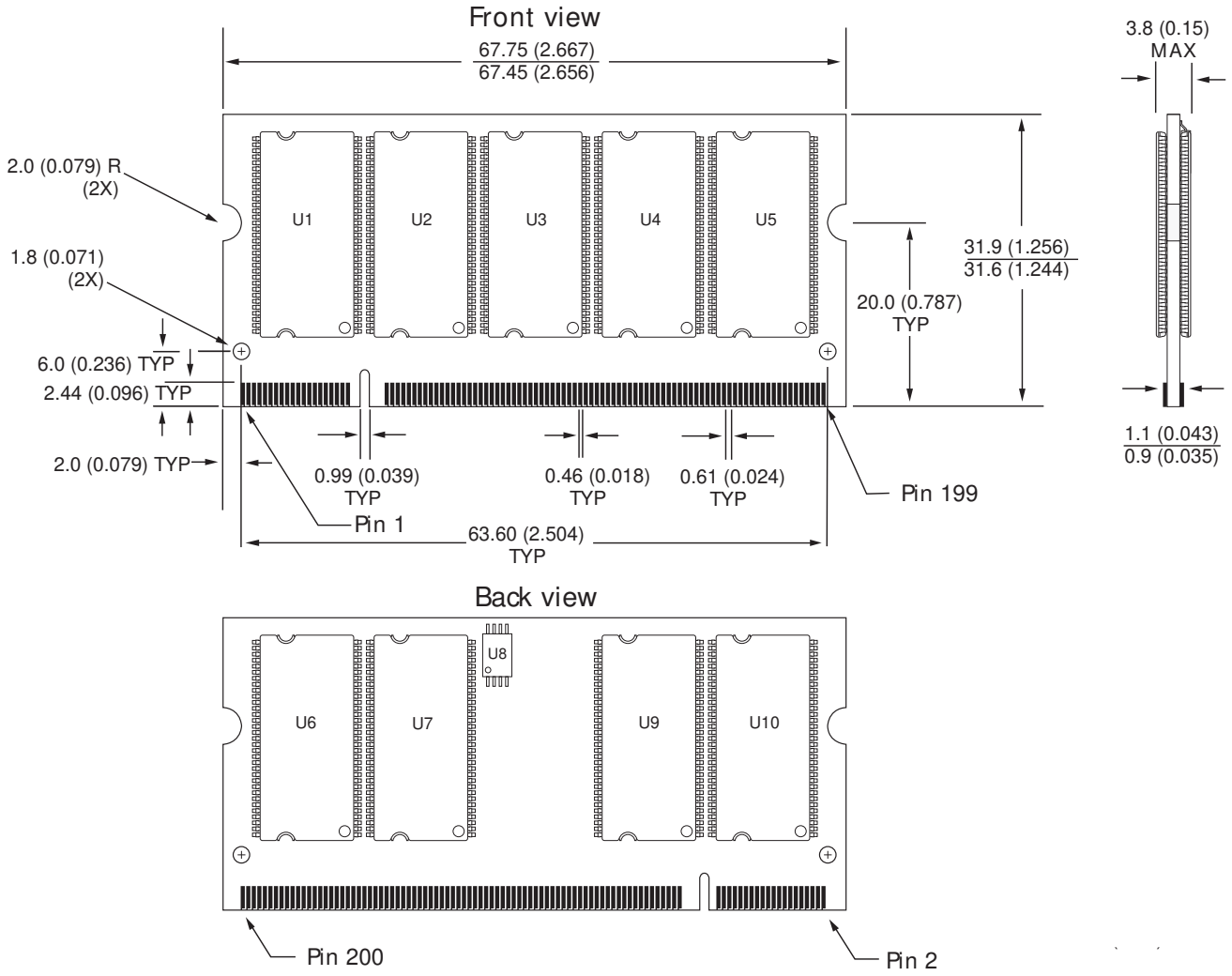
Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.

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Module Dimensions

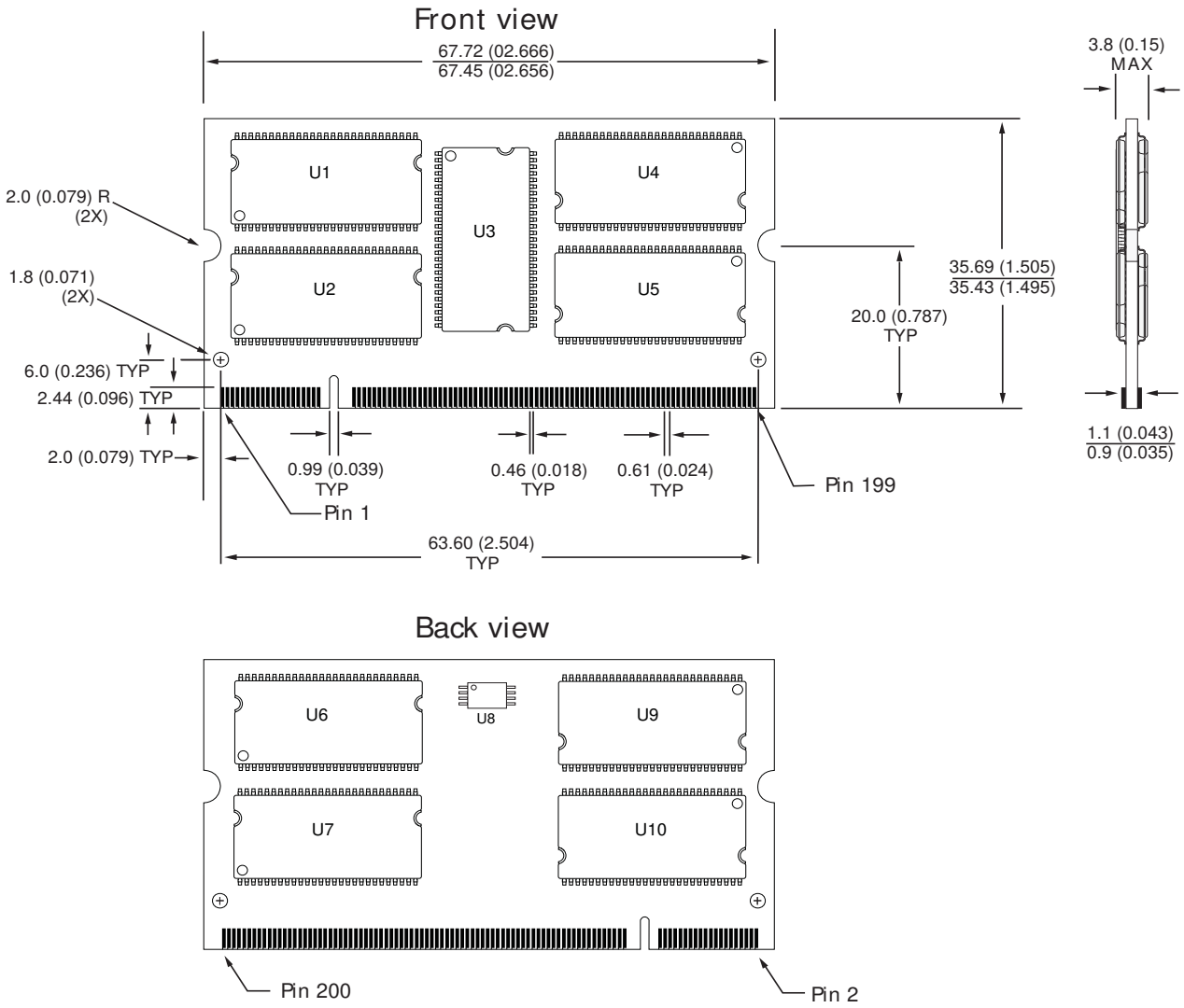
Figure 5: 200-Pin SODIMM – Low-Profile Layout



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.

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Figure 6: 200-Pin SODIMM – Standard Layout



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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