19-0932; Rev 1; 4/93

MAXIM

# CMOS Quad 8-Bit D/A Converters



## General Description

Maxim's MX7225 and MX7226 each contain four 8-bit voltage-output digital-to-analog converters (DACs). They include output buffer amplifiers and input logic for simple microprocessor and TTL/CMOS interfaces. 8-bit performance is achieved over the full operating temperature range without external trimming.

The MX7225 contains double-buffered logic inputs that allow all analog outputs to be simultaneously updated using one control signal. There are also four separate reference inputs so that the range of each DAC can be independently set.

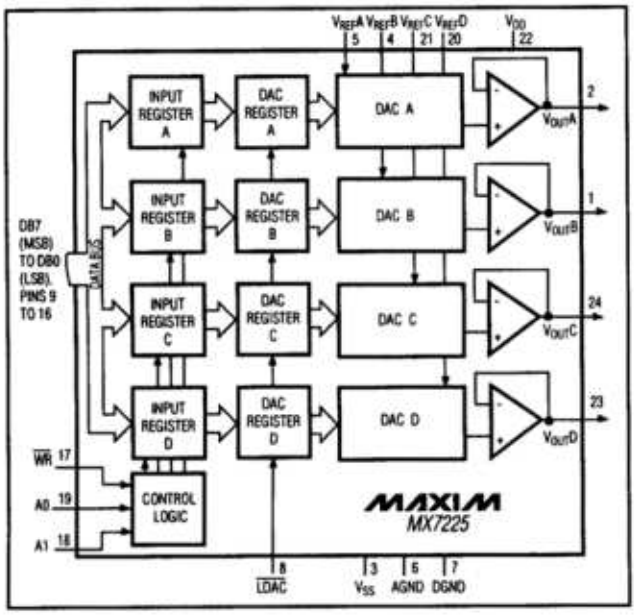
The MX7226 has separate input registers for each of its four DACs. Data is transferred into an input register from a common 8-bit TTL/CMOS-compatible input port. Address inputs A0 and A1 determine which DAC is loaded when WR goes low. All DACs share a common reference input.

For '7225 and '7226 designs utilizing a 5V supply, see the MAX505 and MAX506 data sheet.

## Applications

Minimum Component Count Analog Systems
Digital Offset/Gain Adjustment
Industrial Process Control
Arbitrary Function Generators
Automatic Test Equipment
Microprocessor-Controlled Calibration

## Functional Block Diagram




## Features

- **Buffered Voltage Output**
- **Double-Buffered Inputs (MX7225)**
- **Microprocessor and TTL/CMOS Compatible**
- **Operate from Single or Dual Supplies**
- **Require No External Adjustments**

## Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE | ERROR (LSB) |
|---|---|---|---|
| **MX7225**LN | 0°C to +70°C | 24 Plastic DIP | ±1 |
| MX7225KN | 0°C to +70°C | 24 Plastic DIP | ±2 |
| MX7225LCWG | 0°C to +70°C | 24 Wide SO | ±1 |
| MX7225KCWG | 0°C to +70°C | 24 Wide SO | ±2 |
| MX7225LP | 0°C to +70°C | 28 PLCC | ±1 |
| MX7225KP | 0°C to +70°C | 28 PLCC | ±2 |
| MX7225K/D | 0°C to +70°C | Dice | ±2 |
| MX7225LEWG | -40°C to +85°C | 24 Wide SO | ±1 |
| MX7225KEWG | -40°C to +85°C | 24 Wide SO | ±2 |
| MX7225KERG | -40°C to +85°C | 24 CERDIP* | ±2 |
| MX7225CQ | -40°C to +85°C | 24 CERDIP* | ±1 |
| MX7225BQ | -40°C to +85°C | 24 CERDIP* | ±2 |
| MX7225UQ | -55°C to +125°C | 24 CERDIP* | ±1 |
| MX7225TQ | -55°C to +125°C | 24 CERDIP* | ±2 |
| **MX7226**KN | 0°C to +70°C | 20 Plastic DIP | ±2 |
| MX7226KCWP | 0°C to +70°C | 20 Wide SO | ±2 |
| MX7226KP | 0°C to +70°C | 20 PLCC | ±2 |
| MX7226K/D | 0°C to +70°C | Dice | ±2 |
| MX7226KEWP | -40°C to +85°C | 20 Wide SO | ±2 |
| MX7226BQ | -40°C to +85°C | 20 CERDIP | ±2 |
| MX7226TE | -55°C to +125°C | 20 LCC* | ±2 |
| MX7226TQ | -55°C to +125°C | 20 CERDIP* | ±2 |
| MX7226TD | -55°C to +125°C | 20 Ceramic SB | ±2 |

** Contact factory for availability and processing to MIL-STD-883B.*



***For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.***

# CMOS Quad 8-Bit D/A Converters

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to AGND ..... -0.3V, +17V
$V_{DD}$ to DGND ..... -0.3V, +17V
$V_{SS}$ to AGND ..... -7V, $V_{DD}$
$V_{SS}$ to DGND ..... -7V, $V_{DD}$
$V_{DD}$ to $V_{SS}$ ..... -0.3V, +24V
Digital Input Voltage to DGND ..... -0.3V, $V_{DD}$
$V_{REF}$ to AGND ..... -0.3V, $V_{DD}$
$V_{OUT}$ to AGND (Note 1) ..... $V_{SS}$, $V_{DD}$

Power Dissipation (Any Package) to +75°C ..... 500mW
Derating above +75°C ..... 2mW/°C
Operating Temperature
Commercial (MX722XK/L) ..... 0°C to +70°C
Industrial (MX722XB/C) ..... -25°C to +85°C
Military (MX722XT/U) ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 secs) ..... +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS Dual Supply Specifications

($V_{DD}$ = +11.4V to +16.5V, $V_{SS}$ = -5V ±10%, AGND = DGND = 0V, $V_{REF}$ = +2V to ($V_{DD}$ - 4V), Over Temperature unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| **STATIC PERFORMANCE** | | | | | | |
| Resolution | | | 8 | | | Bits |
| Total Unadjusted Error | | $V_{DD}$ = +15V±5%, $V_{REF}$ = +10V; MX7225LN/CQ/UQ<br>All other devices | | | ±1<br>±2 | LSB |
| Relative Accuracy | | MX7225LN/CQ/UQ<br>All Other Devices | | | ±½<br>±1 | LSB |
| Differential Nonlinearity | | Guaranteed Monotonic | | | ±1 | LSB |
| Full Scale Error | | MX7225LN/CQ/UQ<br>MX7225KN/BQ/TQ<br>All other devices | | | ±½<br>±1<br>±1½ | LSB |
| Full Scale Temperature Coefficient | | $V_{REF}$ = +10V | | ±5 | | ppm/°C |
| Zero Code Error | | MX7225LN/CQ/UQ, $T_A$ = +25°C<br>Over Temp.<br>MX7225KN/BQ/TQ, $T_A$ = +25°C<br>All other devices, Over Temp. | | | ±15<br>±20<br>±20<br>±30 | mV |
| Zero Code Temperature Coefficient | | | | ±30 | | µV/°C |
| **REFERENCE INPUT** | | | | | | |
| Reference Input Voltage Range | $V_{REF}$ | | 2 | | $V_{DD}$ - 4 | V |
| Reference Input Resistance | $R_{REF}$ | MX7225<br>MX7226 | 11<br>2 | | | kΩ |
| Reference Input Capacitance (Code Dependent, Note 3) | $C_{REF}$ | MX7225<br>MX7226 | <br>65 | | 100<br>300 | pF |
| Channel-to-Channel Isolation | | $V_{REF}$ = 10kHz, $10V_{P-P}$ (Note 2) | -60 | | | dB |
| AC Feedthrough | | **$V_{REF}$ = 10kHz, $10V_{P-P}$ (Note 2, 4)** | -70 | | | dB |
| **DIGITAL INPUTS** | | | | | | |
| Digital Input High Voltage | $V_{INH}$ | | 2.4 | | | V |
| Digital Input Low Voltage | $V_{INL}$ | | | | 0.8 | V |
| Digital Input Leakage Current | | **$V_{IN}$ = 0V or $V_{DD}$** | | | ±1 | µA |
| Digital Input Capacitance | | **(Note 2)** | | | 8 | pF |
| **DYNAMIC PERFORMANCE** | | | | | | |
| Voltage Output Slew Rate | | **(Note 2)** | 3 | | | V/µs |
| Voltage Output Settling Time (Pos. or Neg. Full Scale Change) | | to ½LSB, $V_{REF}$ = +10V, 2kΩ and 100pF Load **(Note 2)** | | | 4 | µs |
| Digital Feedthrough and Crosstalk | | All 0's to 1's code change (Note 4) | | 50 | | nV-s |
| Output Load Resistance | | $V_{OUT}$ = +10V | 2 | | | kΩ |

**Note 1:** The outputs may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typical short circuit current to AGND is 25mA.
**Note 2:** Sample tested at +25°C to ensure compliance.
**Note 3:** Guaranteed by design. Not production tested.
**Note 4:** Feedthrough is reduced by connecting the metal lid on the ceramic package (suffix D) to DGND. (**MX7226** only)

## ELECTRICAL CHARACTERISTICS Dual Supply Specifications (continued)

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| **POWER SUPPLIES** | | | | | | |
| $V_{DD}$ Range | | For Specified Performance | +11.4 | | +16.5 | V |
| Positive Supply Current (Outputs Unloaded) | $I_{DD}$ | MX7225KN/BQ/LN/CQ<br>MX7225TQ/UQ<br>MX7226 | | | 10<br>12<br>13 | mA |
| Negative Supply Current (Outputs Unloaded) | $I_{SS}$ | MX7225KN/BQ/LN/CQ<br>MX7225TQ/UQ<br>MX7226 | | | -9<br>-10<br>-11 | mA |
| **SWITCHING CHARACTERISTICS (Note 2)** | | | | | | |
| Address to Write Setup Time | $t_{AS}$ | Over Temp. | 0 | | | ns |
| Address to Write Hold Time | $t_{AH}$ | Over Temp. MX7225<br>MX7226 | 0<br>10 | | | ns |
| Data Valid to Write Setup Time | $t_{DS}$ | MX7225, $T_A$ = +25°C<br>Over Temp.<br>MX7226, $T_A$ = +25°C<br>Over Temp. | 70<br>90<br>90<br>100 | | | ns |
| Data Valid to Write Hold Time | $t_{DH}$ | Over Temp. | 10 | | | ns |
| Write Pulse Width | $t_{WR}$ | MX7225, $T_A$ = +25°C<br>MX7225KN/BQ/LN/CQ, Over Temp.<br>MX7225TQ/UQ, Over Temp.<br>MX7226, $T_A$ = +25°C<br>Over Temp. | 95<br>120<br>150<br>150<br>200 | | | ns |
| Load DAC ($\overline{LDAC}$) Pulse Width (MX7225 Only) | $t_{LC}$ | MX7225, $T_A$ = +25°C<br>MX7225KN/BQ/LN/CQ, Over Temp.<br>MX7225TQ/UQ, Over Temp. | 95<br>120<br>150 | | | ns |

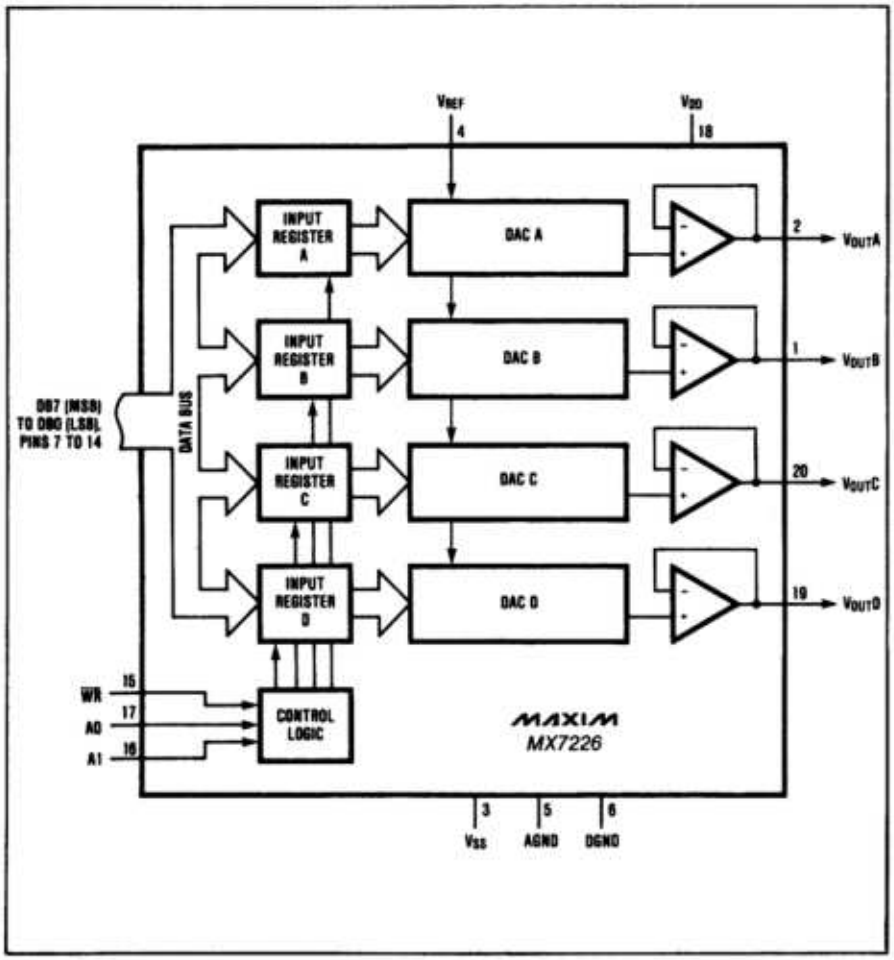
## ELECTRICAL CHARACTERISTICS Single Supply Specifications

($V_{DD}$ = +15V ± 5%, $V_{SS}$ = AGND = DGND = 0V, $V_{REF}$ = +10V, Over Temperature unless otherwise stated.)

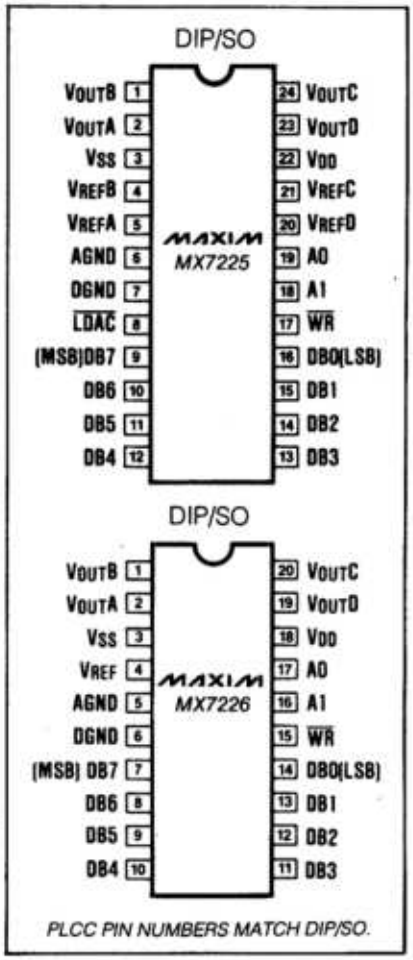
| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| **STATIC PERFORMANCE** | | | | | | |
| Resolution | | | 8 | | | Bits |
| Total Unadjusted Error | | MX7225LN/CQ/UQ<br>All other devices | | | ±1<br>±2 | LSB |
| Differential Nonlinearity | | Guaranteed Monotonic | | | ±1 | LSB |
| **REFERENCE INPUT** | | | | | | |
| Reference Input Voltage Range | $V_{REF}$ | | 2 | | $V_{DD}$-4 | V |
| Reference Input Resistance | $R_{REF}$ | MX7225<br>MX7226 | 11<br>2 | | | kΩ |
| Reference Input Capacitance (Code Dependent, Note 3) | $C_{REF}$ | MX7225<br>MX7226 | <br>65 | | 100<br>300 | pF |
| Channel-to-Channel Isolation | | $V_{REF}$ = 10kHz, $10V_{P-P}$ (Note 2) | -60 | | | dB |
| AC Feedthrough | | $V_{REF}$ = 10kHz, $10V_{P-P}$ **(Note 2, 4)** | -70 | | | dB |
| **DIGITAL INPUTS** — All Specifications Are The Same as For Dual Supply Operation | | | | | | |
| **DYNAMIC PERFORMANCE** — All Specifications Are The Same as For Dual Supply Operation | | | | | | |
| **POWER SUPPLIES** | | | | | | |
| $V_{DD}$ Range | | For Specified Performance | +14.25 | | +15.75 | V |
| Positive Supply Current Output Unloaded | $I_{DD}$ | MX7225KN/BQ/LN/CQ<br>MX7225TQ/UQ<br>MX7226 | | | 10<br>12<br>13 | mA |
| **SWITCHING CHARACTERISTICS** — All Specifications Are The Same as For Dual Supply Operation | | | | | | |

# CMOS Quad 8-Bit D/A Converters

## Functional Block Diagram (MX7226)

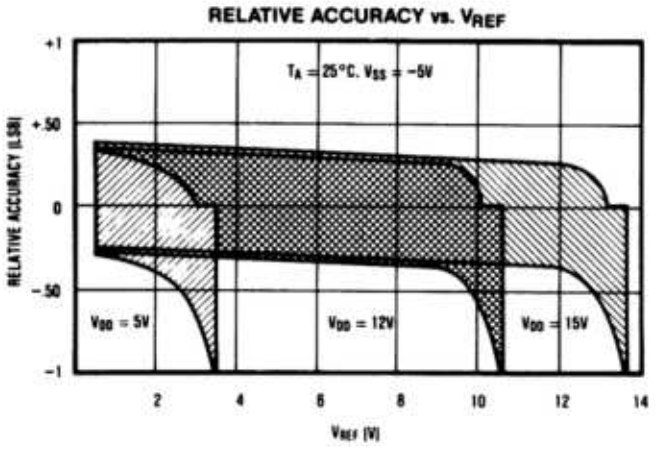


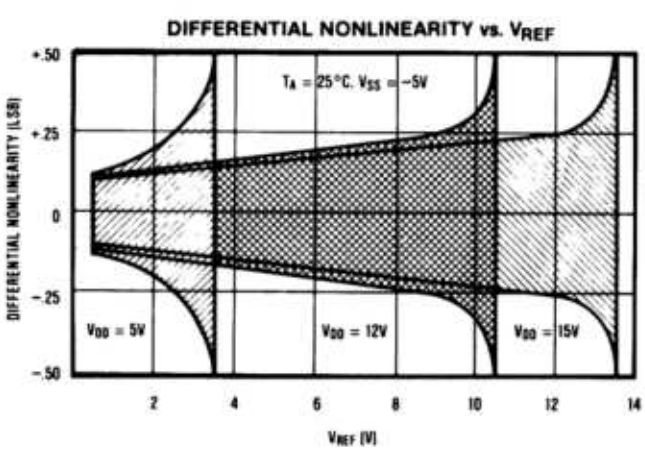

## Pin Configurations

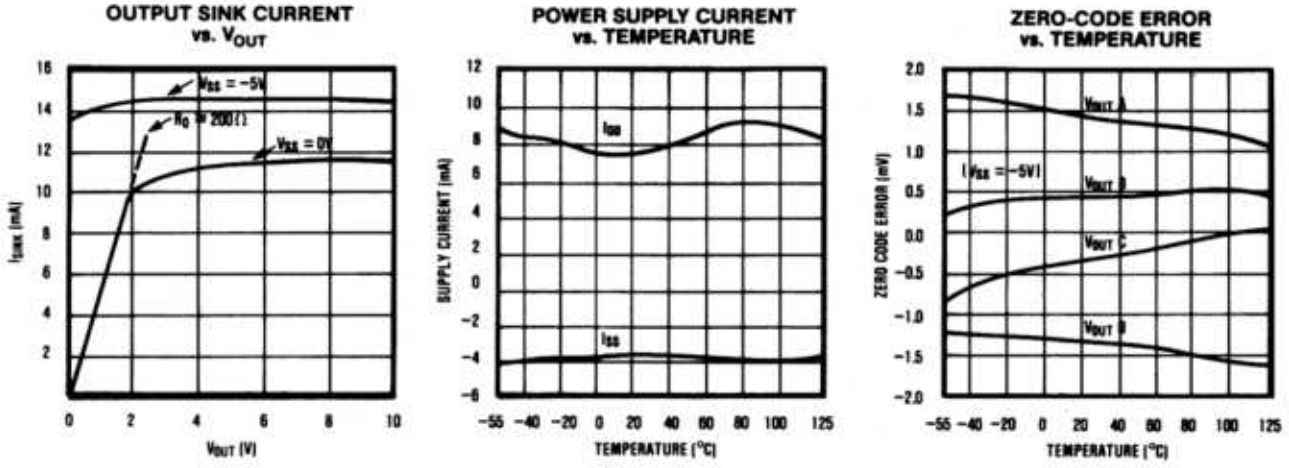



*PLCC PIN NUMBERS MATCH DIP/SO.*

## Typical Operating Characteristics






## Detailed Description

The MX7225 and MX7226 have four matched voltage output digital-to-analog converters (DACs). The DAC's are "inverted" R-2R ladder networks which convert 8 bit digital words into equivalent analog output voltages in proportion to the applied reference voltage(s). Each DAC in the MX7225 has a separate reference input whereas in the MX7226, all reference inputs are tied together. A simplified circuit diagram of one of the four DACs is provided in Figure 1.

### $V_{REF}$ Input

The voltage at $V_{REF}$ sets the full-scale output of the DAC. The input impedance of the $V_{REF}$ input(s) is code dependent. The lowest value, approximately 11kΩ for the MX7225 and 2kΩ for the MX7226, occurs when the input code is 01010101. The maximum value is infinity, which occurs when the input code is 00000000. Because the input resistance at $V_{REF}$ is code dependent, the DAC's reference sources must have an output impedance of no more than 20Ω for the MX7225 and 4Ω for the MX7226, to maintain output linearity. The input capacitance at $V_{REF}$ is also code dependent and typically varies from 15pF to 35pF for the MX7225 and 100pF to 250pF for the MX7226.

$V_{OUT}$A, B, C, or D can be represented by a digitally programmable voltage source as:

$$V_{OUT} = N_B \times V_{REF}/256,$$

where $N_B$ is the numeric value of the DAC's binary input code.

### Output Buffer Amplifiers

All MX7225/26 voltage outputs are internally buffered by precision unity gain followers which slew at greater than 3V/μs. When driving 2kΩ in parallel with 100pF with full scale transitions (0V to +10V or +10V to 0V), the output settles to ±1/2LSB in less than 4μs. Typical dynamic response and settling performance of the MX7225 and MX7226 is shown in Figure 2 and 3.

A simplified circuit diagram of an output buffer is shown in Figure 4. Input common mode range to AGND is provided by a PMOS input structure. The improved

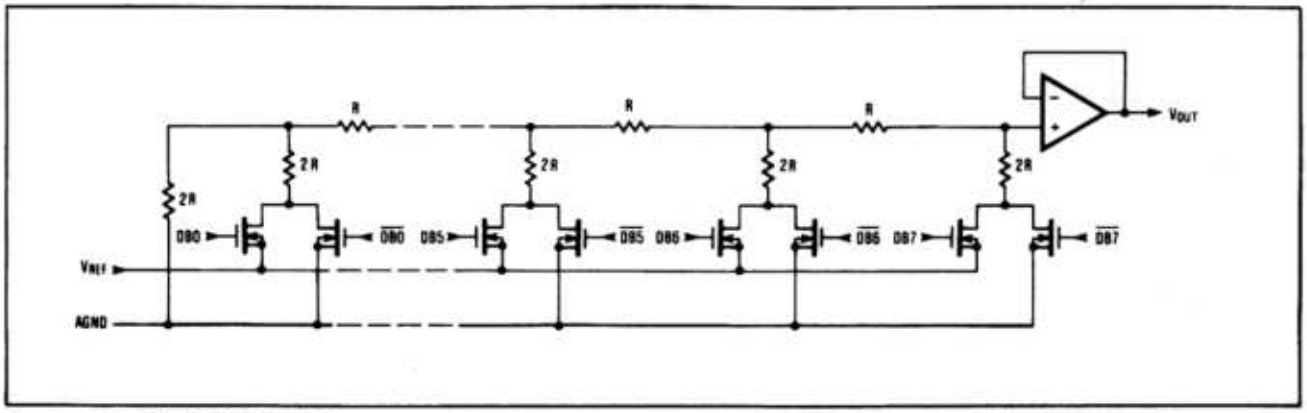



*Figure 1. Simplified DAC Circuit Diagram*

# CMOS Quad 8-Bit D/A Converters

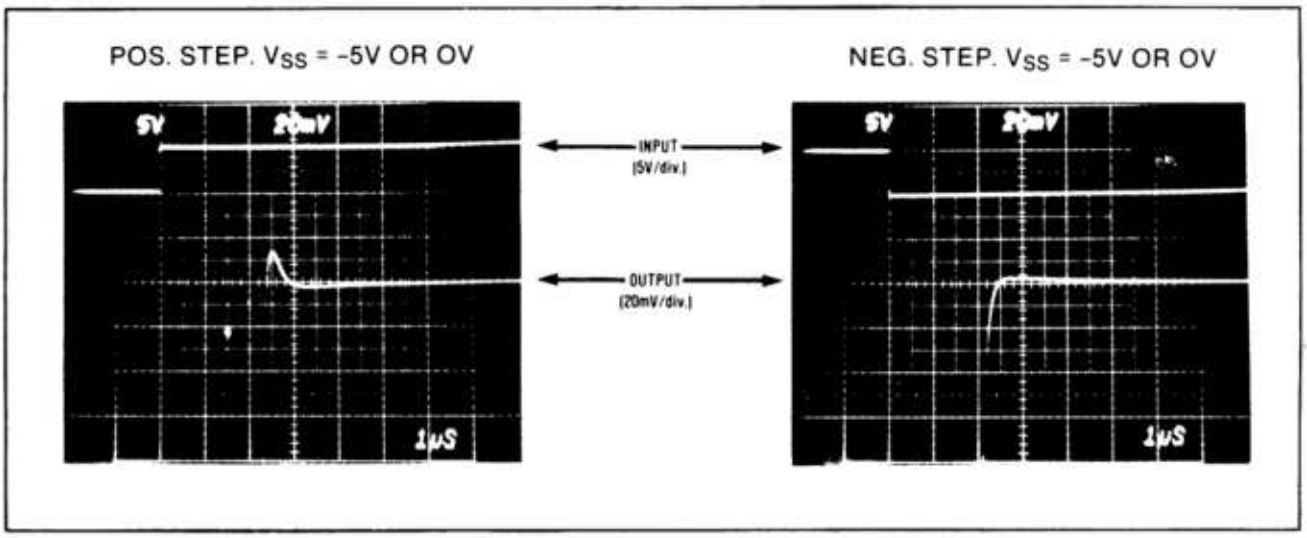



*Figure 2. Positive and Negative Settling Times, $V_{SS}$ = 0V or -5V*

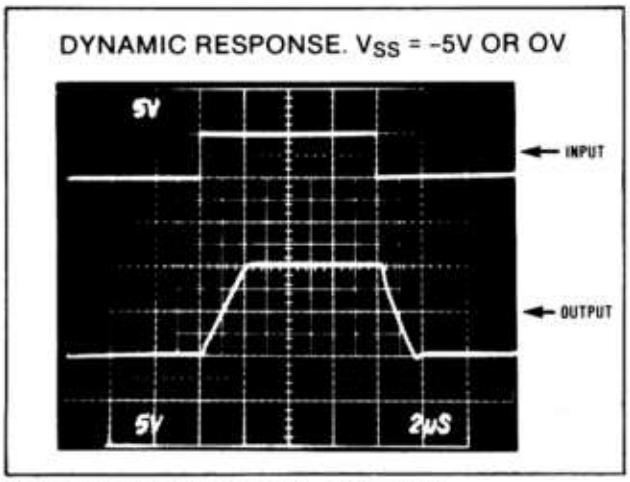



*Figure 3. Dynamic Response, $V_{SS}$ = 0V or -5V*

output circuitry incorporates a Maxim proprietary pull-down circuit to actively drive $V_{OUT}$ to within typically +15mV of the negative supply ($V_{SS}$). The buffer circuitry allows each DAC output to sink, as well as source, up to 5mA. This is especially important in single supply applications, where $V_{SS}$ is connected to GND, so that zero error is kept at or under 1/2LSB ($V_{REF}$ = +10V). A plot of output sink current versus output voltage is shown in the Typical Operating Characteristics section.

## Digital Inputs and Interface Logic

The digital inputs are compatible with both TTL and 5V CMOS logic, however power supply currents, $I_{DD}$ and $I_{SS}$, are somewhat dependent on input logic level. Supply currents are specified for TTL input levels (worst case) but are significantly reduced when the logic inputs are driven as close to DGND as possible, or above 4 volts.

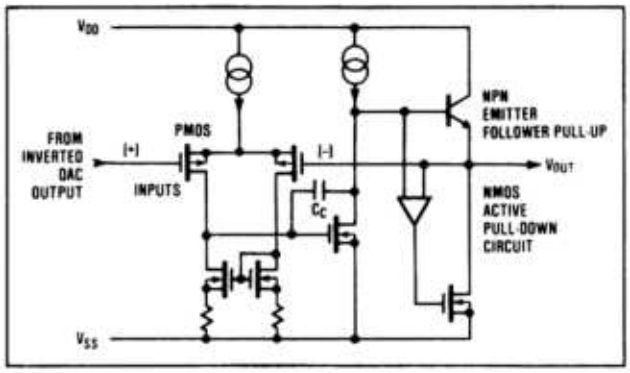



*Figure 4. Simplified Output Buffer Circuit*

Address lines A0 and A1 select which DAC receives data from the input port. When $\overline{WR}$ is low, the input register of the addressed DAC is transparent. The data is then latched when $\overline{WR}$ goes high. Figure 5 shows the input control logic for the MX7225 and MX7226. Table 1 lists the channel addresses.

The MX7226's four DAC outputs represent the data held in four 8 bit input registers. The MX7225 differs from the MX7226 in that in addition to the input registers, there is a separate DAC register for each DAC as well. A DAC's analog output is based only on the contents of its DAC register. Data is transferred from the input registers to the DAC registers by the $\overline{LDAC}$ input. When $\overline{LDAC}$ is LOW, all four DAC registers are transparent to the input registers so that all DACs are updated simultaneously. With $\overline{LDAC}$ held LOW, the MX7225 interface behaves like the MX7226.

Since $\overline{LDAC}$ (MX7225 only) is asynchronous with respect to $\overline{WR}$, care must be taken to assure that incorrect data is not latched through to the output. If $\overline{LDAC}$ is brought LOW before or at the same time that $\overline{WR}$ goes HIGH, then $\overline{LDAC}$ must remain LOW for at least $t_{LD}$ to ensure that the correct data is latched. Data is latched into all four DAC registers on the

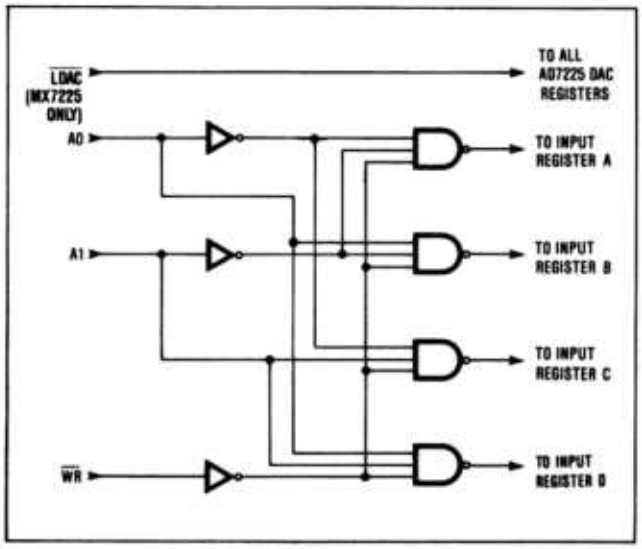



*Figure 5. MX7225, MX7226 Input Control Logic*

**Table 1. DAC Addressing**

| A1 | A0 | SELECTED INPUT REGISTER |
|---|---|---|
| L | L | DAC A Input Register |
| L | H | DAC B Input Register |
| H | L | DAC C Input Register |
| H | H | DAC D Input Register |

**Table 2. MX7225, MX7226 Write Cycle Truth Table**

| $\overline{WR}$ | $\overline{LDAC}$ (MX7225 ONLY) | FUNCTION |
|---|---|---|
| H | H | No operation. Device deselected. |
| L | H | Input register of selected DAC transparent. |
| ⌐¬ | H | Latch the input register of selected DAC. |
| H | L | (MX7225 only) All four DAC registers transparent i.e. DAC outputs reflect the data held in their respective input registers. Input registers are latched. |
| H | ⌐¬ | (MX7225 only) Latch the four DAC registers. Input registers are latched. |
| L | L | (MX7225 only) DAC Registers and the selected input register transparent. DAC output follows input data for selected channel. |

rising edge of $\overline{LDAC}$. Table 2 shows the truth table for $\overline{WR}$ and $\overline{LDAC}$ operation. Figure 6 shows the write cycle timing for both the MX7225 and MX7226.

## Applications Information

### Power Supply and Reference Operating Ranges

The MX7225 and MX7226 are fully specified to operate with $V_{DD}$ between +12V ± 5% and +15V ± 10% (+11.4V to +16.5V), and with $V_{SS}$ from 0V to -5.5V. 8 bit performance is also guaranteed for single supply operation ($V_{SS}$ = 0V), however zero code error is reduced when $V_{SS}$ is -5V (see Output Buffer Amplifier).

For adequate DAC and buffer operating range, the $V_{REF}$ voltage must always be at least 4V below $V_{DD}$. Both the MX7225 and MX7226 are specified to operate with a reference input range of +2V to $V_{DD}$ - 4V.

### Ground Management

Digital or AC transient signals between AGND and DGND will create noise at the analog outputs. It is recommended that AGND and DGND be tied together at the DAC and that this point be tied to the highest quality ground that is available. If separate ground busses are used, then two clamp diodes (IN914 or equivalent) should be connected between AGND and DGND to keep the two ground busses within one diode drop of each other. To avoid parasitic device turn-on, AGND must not be allowed to be more negative than DGND. DGND should be used as supply ground for bypassing purposes.

Careful PCB ground layout techniques should be used to minimize crosstalk between DAC outputs, the reference input(s), and the digital inputs. This is particularly important if the reference is driven from an AC source. Figure 7 and 8 show suggested circuit board layouts for minimizing crosstalk.

### Unipolar Output

In unipolar operation, the output voltages and the reference input(s) are the same polarity. Unipolar circuit configurations are shown in Figure 9 and 10 for the MX7225 and MX7226. Both devices can be operated from a single supply with a slight increase in zero error (see Output Buffer Amplifier section). To avoid parasitic device turn-on, the voltage at $V_{REF}$ must always be positive with respect to DGND. The unipolar code table is given in Table 3.

### Bipolar Output

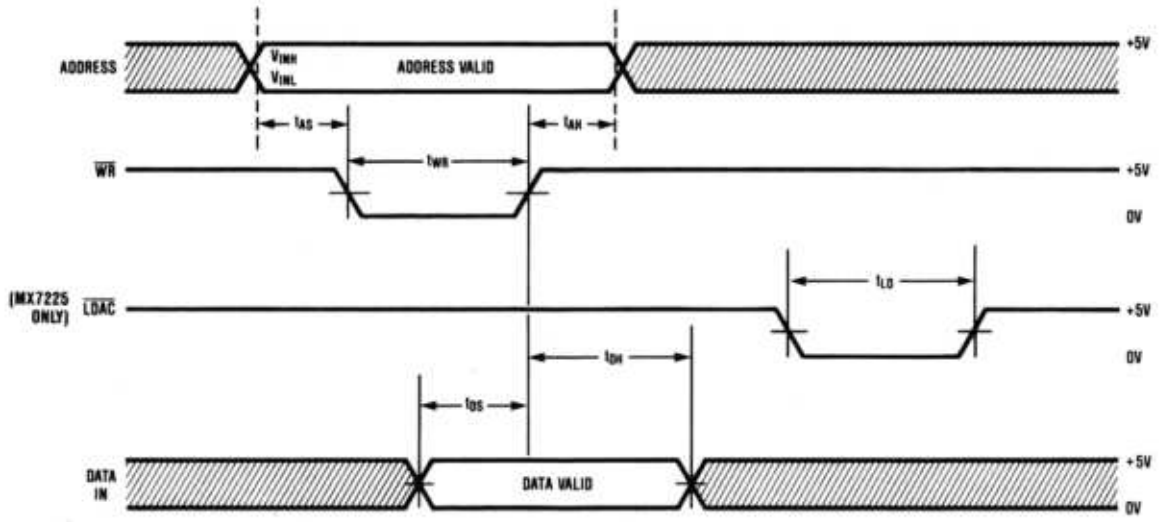
Each DAC output may be configured for bipolar operation using the circuit in Figure 11. One op-amp and two resistors are required per channel. With R1 = R2:

$$V_{OUT} = V_{REF}(2D_A - 1),$$

where $D_A$ is a fractional representation of the digital word in register A.

Table 4 shows the digital code versus output voltage for the circuit in Figure 11.

# CMOS Quad 8-Bit D/A Converters




**Notes:**

1. All input signal rise and fall times measured from 10% to 90% of +5V $t_r = t_f = 20ns$ over $V_{DD}$ range.
2. Timing measurement reference level is,

$$\frac{V_{INH} + V_{INL}}{2}$$

3. If $\overline{LDAC}$ (MX7225 only) is activated prior to the rising edge of $\overline{WR}$, then it must stay low for $t_{LD}$ (or longer) after $\overline{WR}$ goes high.

*Figure 6. Write Cycle Timing Diagram*

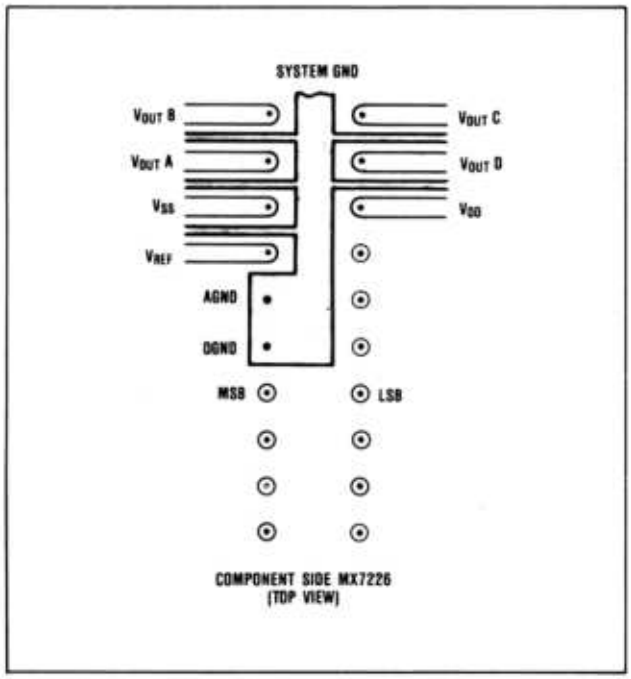



*Figure 7. Suggested MX7226 PCB Layout for Minimizing Crosstalk*

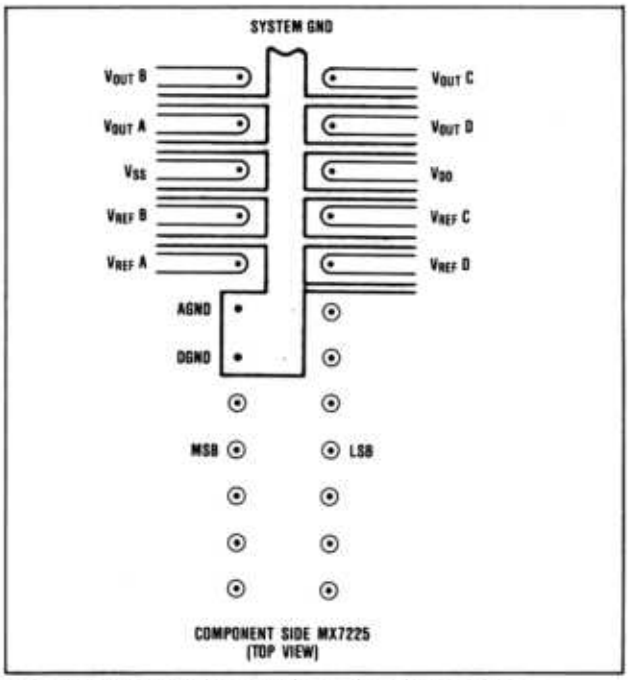



*Figure 8. Suggested MX7225 PCB Layout for Minimizing Crosstalk*

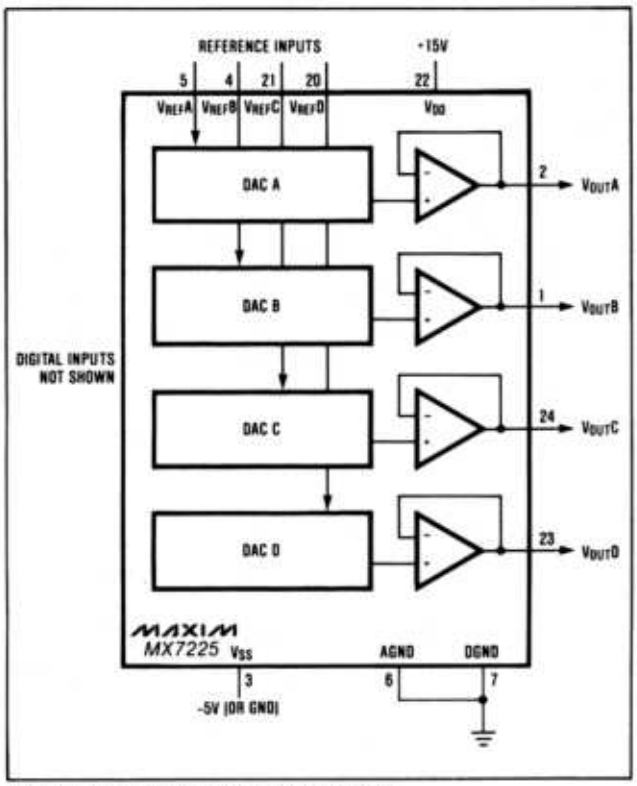



Figure 9. MX7225 Unipolar Output Circuit

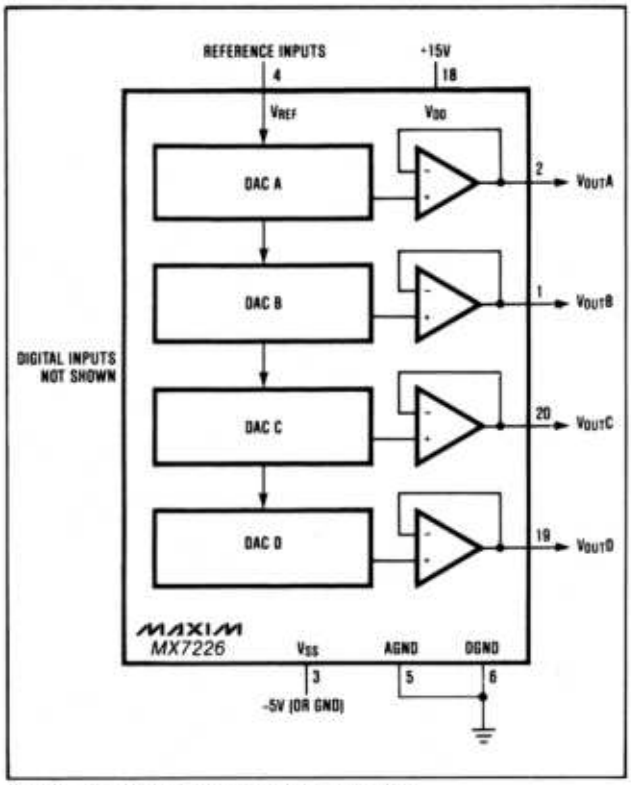



Figure 10. MX7226 Unipolar Output Circuit

**Table 3. Unipolar Code Table**

| DAC CONTENTS MSB | LSB | ANALOG OUTPUT |
|---|---|---|
| 1 1 1 1 | 1 1 1 1 | $+V_{REF}\left(\frac{255}{256}\right)$ |
| 1 0 0 0 | 0 0 0 1 | $+V_{REF}\left(\frac{129}{256}\right)$ |
| 1 0 0 0 | 0 0 0 0 | $+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$ |
| 0 1 1 1 | 1 1 1 1 | $+V_{REF}\left(\frac{127}{256}\right)$ |
| 0 0 0 0 | 0 0 0 1 | $+V_{REF}\left(\frac{1}{256}\right)$ |
| 0 0 0 0 | 0 0 0 0 | 0V |

**Note:** $1LSB = (V_{REF})(2^{-8}) = +V_{REF}\left(\frac{1}{256}\right)$

**Table 4. Bipolar Code Table**

| DAC CONTENTS MSB | LSB | ANALOG OUTPUT |
|---|---|---|
| 1 1 1 1 | 1 1 1 1 | $+V_{REF}\left(\frac{127}{128}\right)$ |
| 1 0 0 0 | 0 0 0 1 | $+V_{REF}\left(\frac{1}{128}\right)$ |
| 1 0 0 0 | 0 0 0 0 | 0V |
| 0 1 1 1 | 1 1 1 1 | $-V_{REF}\left(\frac{1}{128}\right)$ |
| 0 0 0 0 | 0 0 0 1 | $-V_{REF}\left(\frac{127}{128}\right)$ |
| 0 0 0 0 | 0 0 0 0 | $-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$ |

# CMOS Quad 8-Bit D/A Converters

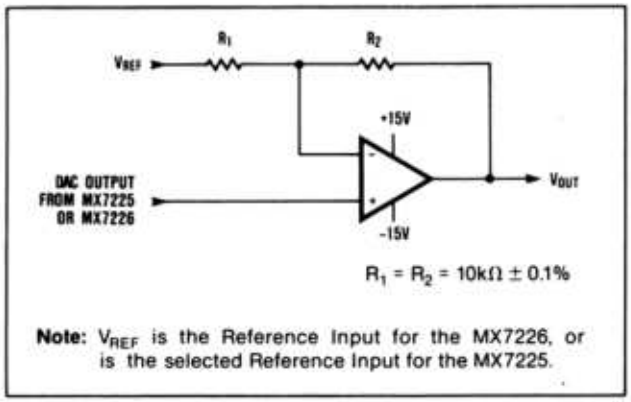



*Figure 11. Bipolar Output Circuit*

### Offsetting AGND

AGND can be biased above DGND to provide an arbitrary nonzero output voltage for a "zero" input code. This is shown in Figure 12. The output voltage at $V_{OUT}A$ is:

$$V_{OUT}A = V_{BIAS} + D_A V_{IN},$$

where $D_A$ is a fractional representation of the digital input word. Since AGND is common to all four DAC's, all outputs will be offset by $V_{BIAS}$ in the same manner.

### Using an AC Reference

In applications where $V_{REF}$ has AC signal components, the MX7225 and MX7226 have multiplying capability within the limits of the $V_{REF}$ input range specifications. Figure 13 shows a technique for applying a sine wave signal to the reference input where the AC signal is biased up before being applied to $V_{REF}$. Output distortion is typically less than 0.1% with input frequencies up to 50kHz, and the typical -3dB frequency is 700kHz. Note that $V_{REF}$ must never be more negative than AGND.

### Generating $V_{SS}$

The performance of the MX7225/7226 is specified for both dual and single supply ($V_{SS}$ = 0V) operation. When the improved performance of dual supply operation is desired, but only a single supply is available, a -5V $V_{SS}$ supply can be generated using an ICL7660 in one of the circuits of figure 14.

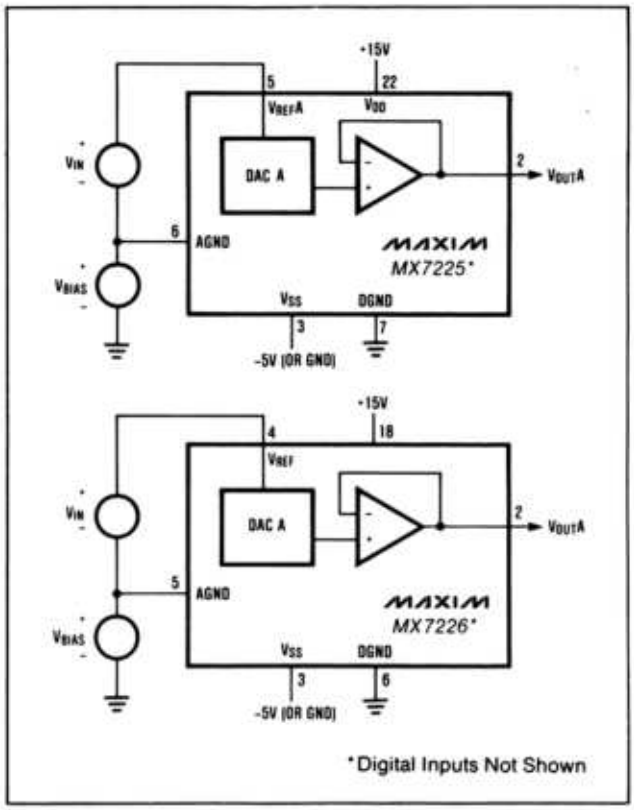



*Figure 12. AGND Bias Circuits*

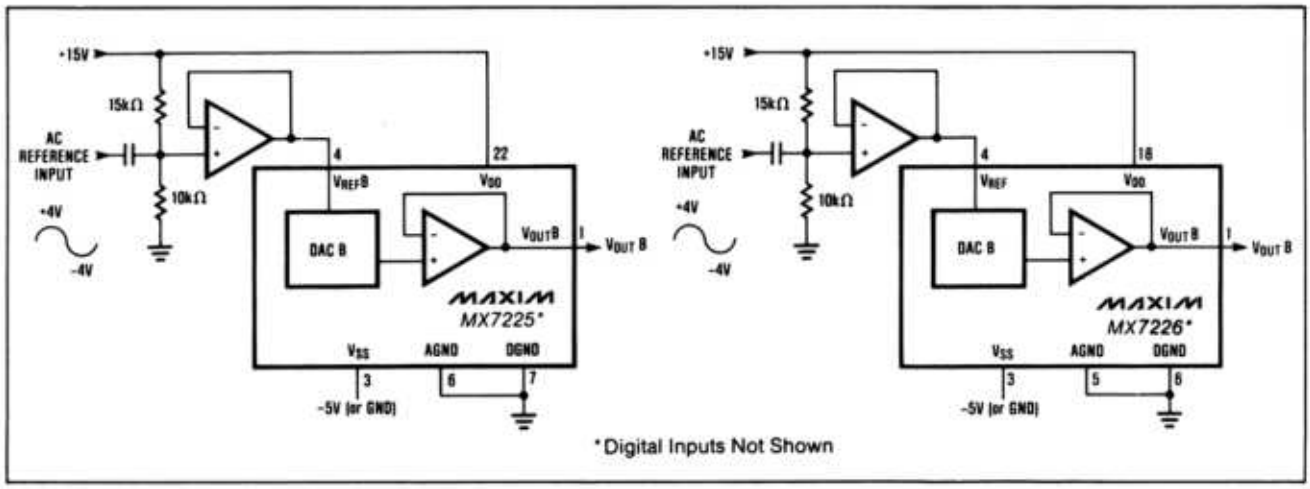



*Figure 13. AC Reference Input Circuit*

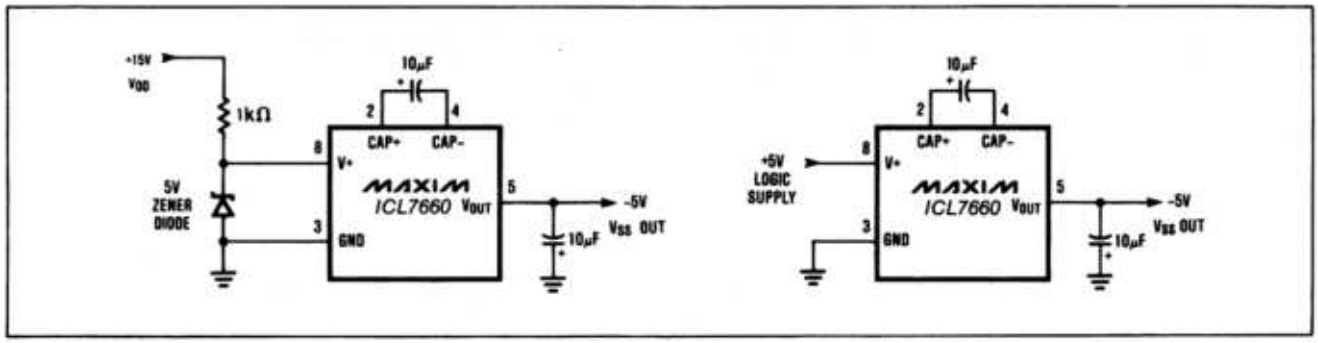



*Figure 14. Generating -5V for $V_{SS}$*

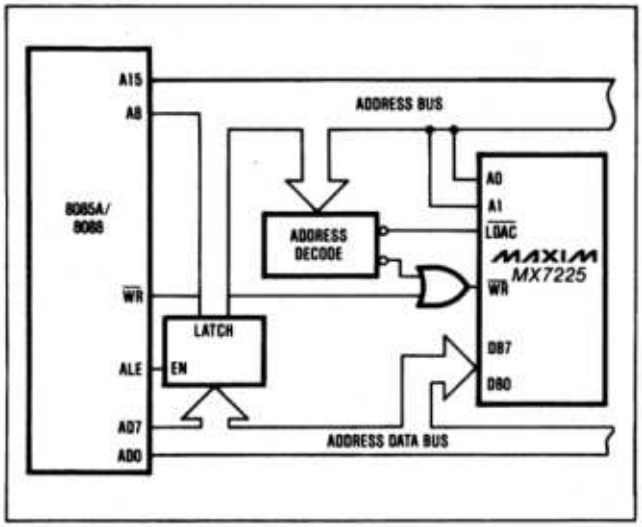



*Figure 15. MX7225 to 8085A/8088 Interface, Double-Buffered Mode*

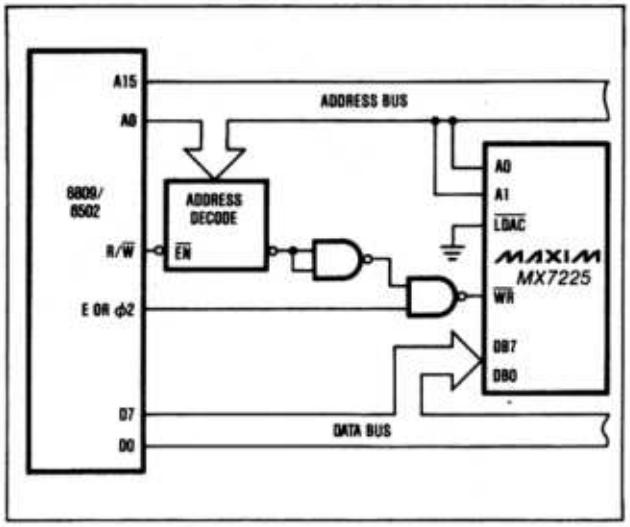



*Figure 16. MX7225 to 6089/6502 Interface, Single-Buffered Mode*

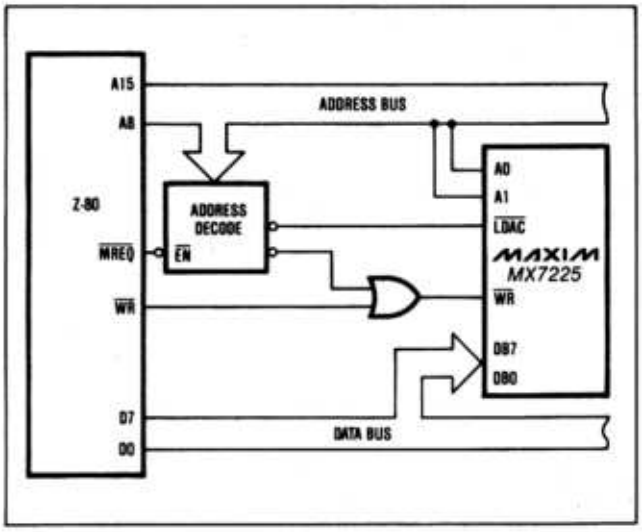



*Figure 17. MX7225 to Z-80 Interface Double-Buffered Mode*

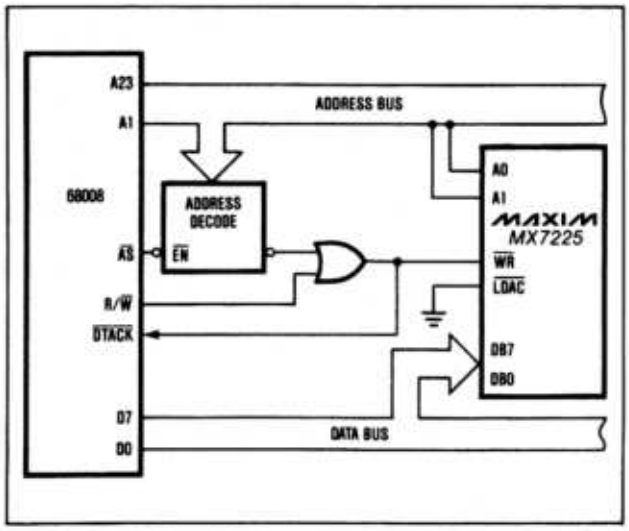



*Figure 18. MX7225 to 68008 Interface, Single-Buffered Mode*

# CMOS Quad 8-Bit D/A Converters

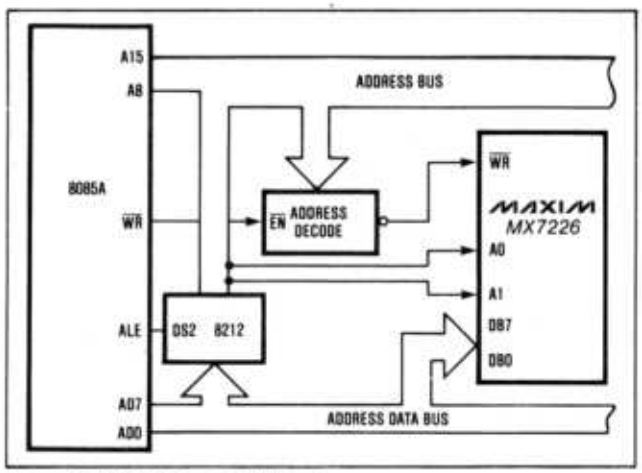



Figure 19. MX7226 to 8085A Interface

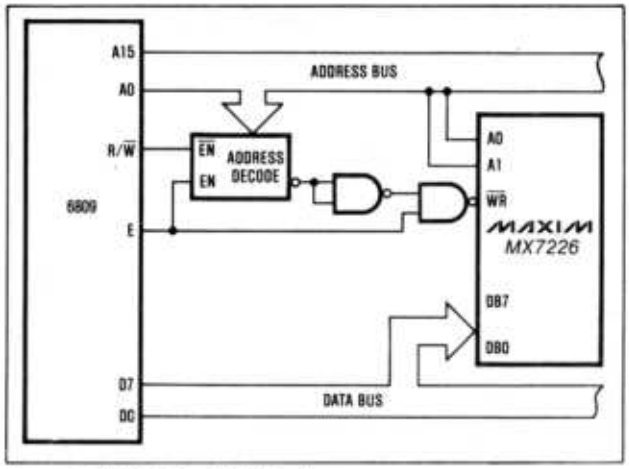



Figure 20. MX7226 to 6809 Interface

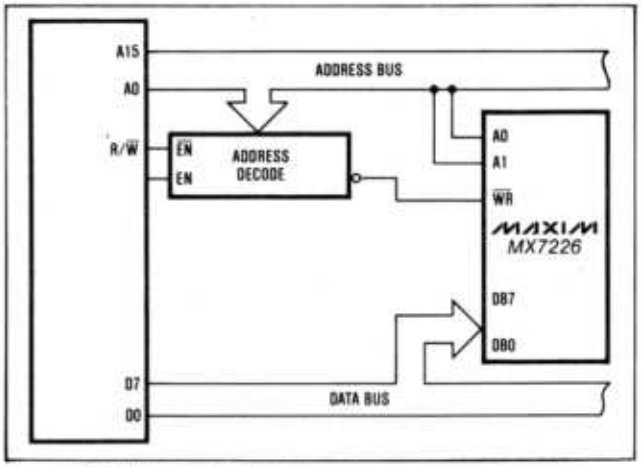



Figure 21. MX7226 to 6502 Interface

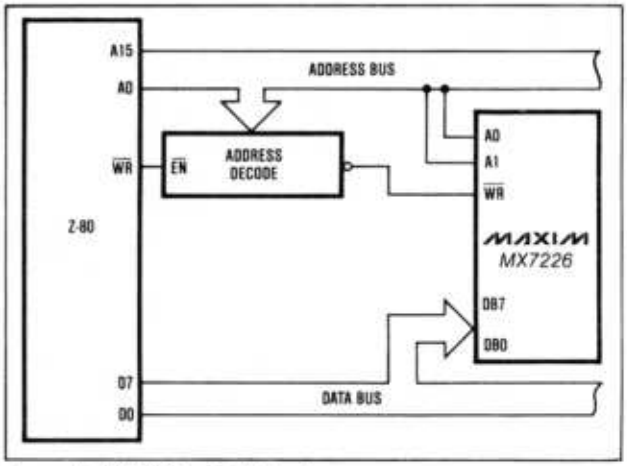
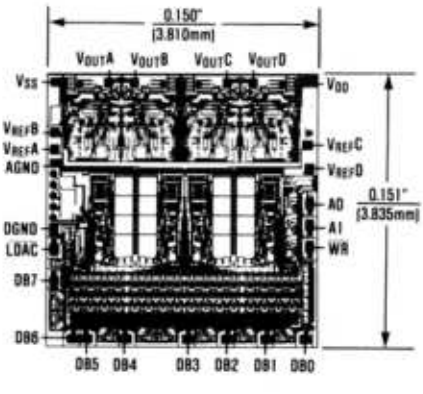
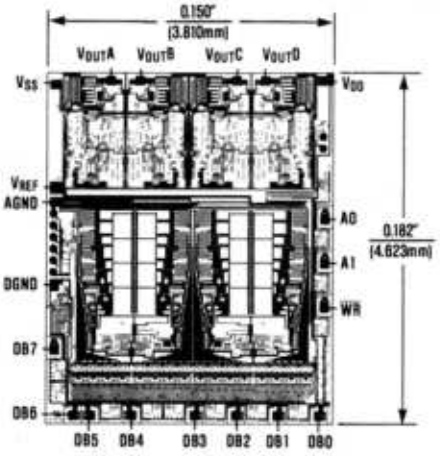



Figure 22. MX7226 to Z-80 Interface

## Chip Topography




MX7225




MX7226

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