FEATURES

- TI TMS320C645x DSP
  - 720 MHz, 1 GHz, & 1.2 GHz options
  - 1 MB cache or 2 MB cache options
  - Integrated 10/100/1000 EMAC
  - 2 Integrated McBSPs
  - JTAG Emulation/Debug
- On-Board Xilinx Spartan3 FPGA
  - XC3S2000 & XC3S4000 options
  - 300 MHz Clock Logic
  - JTAG Interface/Debug
- On-Board 10/100 Ethernet PHY connected to DSP's EMAC
- 128 MB CPU DDR2 SDRAM
- 64 MB FPGA DDR1 SDRAM
- 16 MB NOR FLASH
- SO-DIMM-200 Interface
  - 140 FPGA User I/O Pins
  - 2 McBSP Interfaces
  - I2C Interface
  - 10/100 Ethernet Interface
  - 3.3V Power Interface
- Expansion I/O Connector
  - DSP Rapid IO Interface
  - DSP PCI I/O Interface
  - DSP Gigabit Ethernet Interface (RGMII) to an external PHY

APPLICATIONS

- Embedded Instrumentation
- Rapid Development / Deployment
- Embedded Digital Signal Processing
- Real-time Audio / Video Processing



(3.25" x 2.7" - actual size)

DESCRIPTION

The MityDSP-Pro is a highly configurable, high performance, small form-factor processor card that features a Texas Instruments TMS320C645x Digital Signal Processor (DSP) tightly integrated with a Xilinx Spartan3 Field Programmable Gate Array (FPGA), FLASH and DDR1/DDR2 SDRAM memory subsystems. Both the DSP and the FGPA are capable of loading/executing programs and logic images developed by end users. The MityDSP-Pro provides a complete digital processing infrastructure necessary for embedded applications development.

Users of the MityDSP-Pro are encouraged to develop applications and FPGA firmware using the MityDSP hardware and software development kit provided by Critical Link. The development kit includes API libraries compatible with the TI Code Composer Studio compiler as well as FPGA netlist components compatible with the Xilinx ISE FPGA synthesis/implementation tools. The libraries provide the necessary functions needed to configure the MityDSP-Pro, program standalone MityDSP embedded applications, and interface with the various hardware components on the board. In addition, the libraries include several interface "cores" – FPGA and DSP software

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modules designed to interface with various data converter modules (ADCs, DACs, LCD interfaces, etc) – as well as bootloading and FLASH programming utilities.

Figure 1 provides a top-level block diagram of the MityDSP-Pro processor card. As shown in the figure, the primary interface to the MityDSP-Pro is through a standard SO-DIMM-200 card edge interface. The interface provides 3.3V power, configuration control, Ethernet connectivity, inter-integrated circuit (I2C) connectivity, synchronous serial connectivity, and 140 pins of configurable FPGA I/O for application-defined interfacing. Details of the SO-DIMM connector interface are included in the SO-DIMM-200 Interface Description, below.

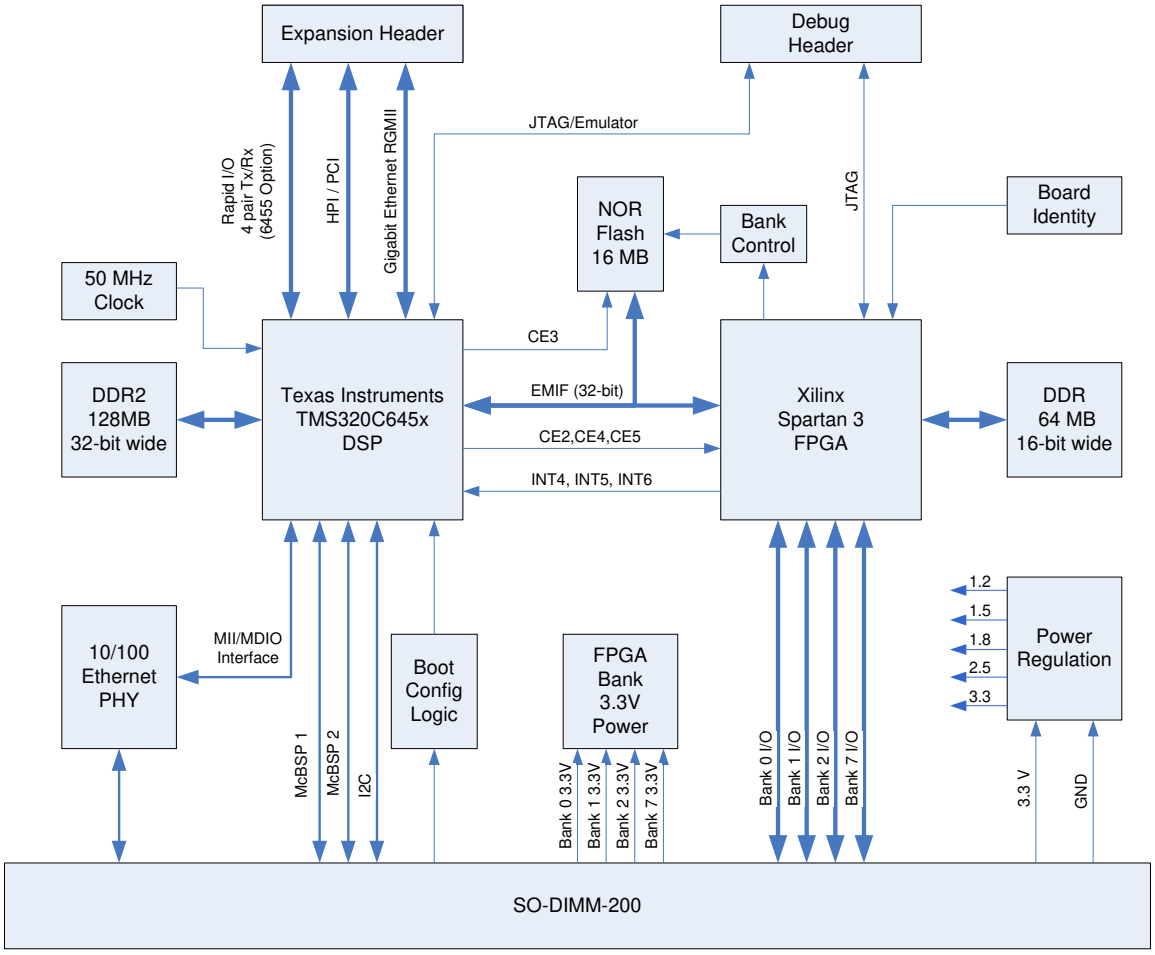


Figure 1: MityDSP-Pro Block Diagram

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FPGA Bank I/O

The MityDSP-Pro provides 140 lines of FPGA I/O directly to the SO-DIMM-200 card edge interface. The 140 lines of FPGA I/O are distributed across 4 banks of the FPGA. These I/O lines and their associated logic are completely configurable within the FPGA.

With the Xilinx Spartan3 family of FPGA, each bank may be configured to operate on a different electrical interface standard based on input voltage and termination configurations. The MityDSP-Pro provides, for each of the four externally accessible FPGA banks, a power supply pin (VCCO_N) to allow the bank to be powered to 2.5V or 3.3V. The following table outlines the various electrical interface standards that are possible on the MityDSP-Pro:

Table 1: MityDSP-Pro FPGA Available I/O Standards

I/O Standard	Bank Voltage	VCCO_N pin
2.5V LVDS with 100 ohm DCI termation	2.5V	Open or 2.5V supply
2.5V LVDS without DCI termination	2.5V	Open or 2.5V supply
2.5V CMOS (pull-up/down options in FPGA)	2.5V	Open or 2.5V supply
3.3V CMOS (pull-up/down options in FPGA)	3.3V	3.3V supply

For complete details regarding hardware bank voltage configuration please refer to the SO-DIMM-200 Interface description and the appropriate Spartan3 manuals from Xilinx.

Integrated DSP Communications Modules

The C6454 processor includes several on-chip communications modules. The MityDSP-Pro design provides access to the several of the modules through the SO-DIMM-200 card edge interface.

The Ethernet MAC MII/MDIO interface on the DSP has been integrated with an on-board Ethernet PHY device. The Tx/Rx line-level signals of the PHY device are brought to the SO-DIMM-200 connector. In order to leverage the Ethernet interface, application boards need only supply appropriate Ethernet magnetics, and the RJ-45 Ethernet connector, which are often available as a single component. The MityDSP software developer's kit includes a software driver and port of the LwIP TCP/IP protocol stack for use with the Ethernet interface.

The DSP's Gigabit Ethernet capability is accessible via the expansion I/O connector on the bottom side of the MityDSP-Pro module. The EMAC's Reduced Gigabit Medium Independent Interface (RGMII) is available on this connector for connection to a PHY device on the end application board. The signals are separate from the MII signals routed to the on-board 10/100 PHY. Although the same EMAC module within the DSP services both sets of signals, only one Ethernet interface can be used at a time.

The inter-integrated circuit (I2C) signals have been routed between the DSP, FPGA, and the SO-DIMM-200 interface. Communication is allowed between any combination of DSP, FPGA, and user board devices. TI provides several I2C interface libraries for

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integration with various data acquisition modules. The MityDSP development kit also contains modules for implementing I2C communication using the FPGA connection. In addition, the I2C interface may be used to boot the DSP processor (see the SO-DIMM-200 interface description for details on MityDSP-Pro boot configuration).

The DSP also includes two multi-channel buffered serial ports (McBSPs) which have been routed directly to the SO-DIMM-200 interface. Both Critical Link (as part of the MityDSP development kit) and TI provide several McBSP interface libraries for integration with various data acquisition modules.

EMIF Interface

The C645x DSP and the Spartan3 FPGA are connected using the DSP External Memory Interface (EMIFA). The EMIFA interface includes 4 chip-select spaces. The EMIFA interface supports multiple data width transfers and bus wait state configurations based on chip select space. 8, 16, 32, and 64 bit data word sizes may be used. Three of the four chip-select lines are reserved for the FPGA interface. The MityDSP-Pro also includes lines between the FPGA and the DSP for the purposes of generating interrupts.

In addition to the FPGA, 16 MB of on-board NOR FLASH memory is also connected to the DSP using the EMIF. The FLASH memory is connected to fourth chip-select line of the EMIF (CE3). The FLASH memory is typically used to store the following types of data:

- secondary bootloader DSP software
- secondary bootloader FPGA image
- application DSP software
- application FPGA images
- application data (non-volatile storage)

The DSP EMIF interface is only capable of addressing 4 MB of data on the EMIF interface. In order to provide access to the remaining 12 MB of FLASH memory, the upper address lines of the FLASH are controlled by Bank Control logic. Upon reset the Bank Control Logic defaults to bank zero for bootloading support. Following bootloading, the bank control logic is controlled by the FPGA. Refer to the MityDSP User's Guide for more information on bank control logic.

System Memory

The C6454 includes a 32 KB level-1 program (L1P) cache/SRAM, a 32 KB level-1 data (L1D) cache/SRAM, and a 1 MB level-2 (L2) cache/SRAM. The C6455 doubles the L2 cache/SRAM to 2MB. All types of cache/SRAM may be split into various amounts of cache and SRAM. Refer to TI's datasheets for specific details on configuring the cache/SRAM memory blocks.

For main DSP software program and runtime data storage, a dedicated 128 MB of DDR2 memory is available via the DDR2 control interface on the DSP. The memory is 32 bits

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wide and is capable of running at 250 MHz providing a burst throughput of 2 GB per second to the processor.

For the FPGA, a separate 64 MB of DDR1 memory is provided. The memory interface is 16 bits wide and is capable of running at 125 MHz providing a burst throughput of 500 MB per second to the FPGA. Common uses for the FPGA memory include custom data collection systems, video frame buffers, and MicroBlaze program storage.

Debug Interface

Both the JTAG interface signals for the FPGA and the JTAG and emulator signals for the C645x processor have been brought out to a connector/header for use with in-circuit debugging. The JTAG chains are separate on the interface. With an appropriate breakout cable, the interface will support the use of standard Xilinx Platform JTAG cable programming and the Spectrum Digital processor emulator (or equivalent). Details of the pin-outs for the debug header are included in the Debug Interface Description below.

Expansion Interface

For system expansion, the MityDSP-Pro also provides a low profile Hirose FX8-100S-SV connector interface that may be used to access the Host-Port-Interface (HPI), Peripheral-Component-Interconnect (PCI), and Gigabit Ethernet MAC ports of the C645x bus. In addition, four lanes of transmit and receive Rapid I/O data lines (and associated clocks) are also provided with the C6455 processor option.

Module Options

The MityDSP-Pro has been designed to support several upgrade options. These include a selection of 3 CPU speeds with a combination of 2 FPGA types. If you do not see a combination in Table 6 that meets your needs please contact a Critical Link sales representative.

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Example Application

The figure below illustrates an example application utilizing the MityDSP-Pro processor card. The example application is a 6-way signal beamformer for use in a radar system. The card is required to capture 6 channels of IF signal data, downconvert the data to baseband, sum the signals together with the input channels and data provided from upstream processors, and send the results to downstream processing.

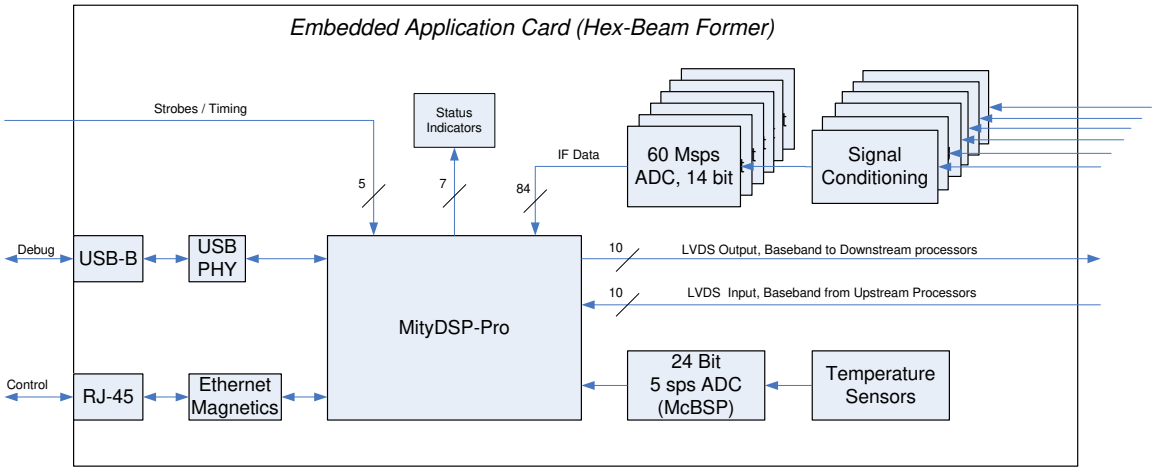


Figure 2: Typical MityDSP-Pro Application

In the example application, a designer leverages three of the four FPGA I/O banks as 3.3V CMOS interface and is able to integrate 6 14-bit ADC circuits directly to the MityDSP-Pro FPGA as well as various strobe signals and status indicators. The fourth bank is reserved for LVDS signaling and is used to receive and transmit data from upstream and downstream processors.

The user is able to utilize the McBSP interface of the MityDSP-Pro to capture on-board temperature data for health monitoring. In addition, an Ethernet interface and a USB interface are added to provide debug and status and control information to external control units.

Within the MityDSP-Pro, the user is able to utilize the FPGA multiply accumulator engines and programmable logic to capture, baseband, and integrate each of the ADC channels on the main board. The TI processor can be used to compute complex coefficients used in the beamforming process and provide the command and control interface for the entire card.

With the application, the user needs only focus on the details of the application specific problems at hand: e.g., developing the appropriate signal conditioning and application software and firmware. The framework for the processing and interconnects is completely designed with the integration of the MityDSP-Pro.

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ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Maximum Supply Voltage, Vcc	3.4 V
Storage Temperature Range	-65 to 80C
Shock, Z-Axis	±10 g
Shock, X/Y-Axis	±10 g

OPERATING CONDITIONS

Commercial Temperature Range	0 to 70C
Industrial Temperature Range	-40 to +85C
Humidity	0 to 95% Non-condensing

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vcc	Voltage supply, 3.3 volt input.			3.3	3.4	Volts
Icc	Quiescent Current draw, 3.3 volt input			1.5	3	Amps
Icc-max	Max current draw, positive 3.3 volt input.			1.7	3.5	Amps
				10	-	KHz
				0	TBD	Volts
						Volts
	Clock Frequency, Digital Inputs			25	25	MHz
	Update period, digital inputs			1280	1280	ns
	Clock Frequency, Digital Output LVDS clk entering deserializer			50	20 / 68	MHz
	Update period, digital outputs			20	14.7 / 50	ns
	1. Power utilization of the MityDSP-Pro is heavily dependant on end-user application. Major factors include: CPU PLL configuration, FPGA utilization, and external SDRAM utilization.					

SO-DIMM-200 Interface Description

The primary interface connector for the MityDSP-Pro is the SO-DIMM-200 card edge interface. Table 2 lists every pin on the SO-DIMM-200 main interface connector. Table 3 describes the function of each group of signals on the main interface connector.

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Table 2: SO-DIMM-200 Pin-Out

Pin	Signal	FPGA Bank	Signal	Pin
1	3.3 V	-	3.3 V	2
3	3.3 V	-	3.3 V	4
5	3.3 V	-	3.3 V	6
7	GND	-	GND	8
9	GND	-	GND	10
11	MRESET#	-	BOOT_MODE	12
13	ETH_TD_P	-	RS232_TXD	14
15	ETH_TD_N	-	RS232_RXD	16
17	ETH_RD_P	-	RS232_RTS	18
19	ETH_RD_N	-	RS232_CTS	20
21	FPGA_RSV1	-	SCL	22
23	FPGA_RSV2	-	SDA	24
25	CLKR0	-	CLKR1	26
27	CLKX0	-	CLKX1	28
29	DR0	-	DR1	30
31	DX0	-	DX1	32
33	FSR0	-	FSR1	34
35	FSX0	-	FSX1	36
37	VCCO_2	-	VCCO_1	38
39	VCCO_0	-	VCCO_7	40
41	GND	-	GND	42
43	ODD1_P.N26	2	EVN1_P.N22	44
45	ODD1_N.N25	2	EVN1_N.N21	46
47	ODD2_P.M26	2	EVN2_P.N24	48
49	ODD2_N.M25	2	EVN2_N.N23	50
51	ODD3_P.M22	2	EVN3_P.M24	52
53	ODD3_N.M21	2	EVN3_N.L23	54
55	ODD4_P.L26	2	EVN4_P.K24	56
57	ODD4_N.L25	2	EVN4_N.K23	58
59	ODD5_P.K26	2	EVN5_P.J25	60
61	ODD5_N.K25	2	EVN5_N.J24	62
63	GND	-	GND	64
65	ODD6_P.K22	2	EVN6_P.H24	66
67	ODD6_N.K21	2	EVN6_N.H23	68
69	ODD7_P.H26	2	EVN7_P.J23	70
71	ODD7_N.H25	2	EVN7_N.J22	72
73	ODD8_P.J21	2	EVN8_P.H21	74
75	ODD8_N.H22	2	EVN8_N.H20	76
77	ODD9_P.D26	2	EVN9_P.E24	78
79	ODD9_N.D25	2	EVN9_N.E23	80
81	ODD10_P.F21	1	EVN10_P.C23	82
83	ODD10_N.E21	1	EVN10_N.B23	84
85	GND	-	GND	86
87	ODD11_P.E20	1	EVN11_P.C22	88
89	ODD11_N.D20	1	EVN11_N.B22	90
91	ODD12_P.B21	1	EVN12_P.D21	92
93	ODD12_N.A21	1	EVN12_N.C21	94
95	ODD13_P.B20	1	EVN13_P.G18	96
97	ODD13_N.A20	1	EVN13_N.F18	98
99	ODD14_P.B19	1	EVN14_P.G17	100

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Pin	Signal	FPGA Bank	Signal	Pin
101	ODD14_N.A19	1	EVN14_N.F17	102
103	ODD15_P.F16	1	EVN15_P.E17	104
105	ODD15_N.E16	1	EVN15_N.D17	106
107	GND	-	GND	108
109	ODD16_P.B15	1	EVN16_P.F15	110
111	ODD16_N.A15	1	EVN16_N.E15	112
113	ODD17_P.C14	1	EVN17_P.E14	114
115	ODD17_N.B14	1	EVN17_N.D14	116
117	ODD18_P.A13	0	EVN18_P.F13	118
119	ODD18_N.B13	0	EVN18_N.G13	120
121	ODD19_P.A12	0	EVN19_P.C13	122
123	ODD19_N.B12	0	EVN19_N.D13	124
125	ODD20_P.H13	0	EVN20_P.E12	126
127	ODD20_N.G12	0	EVN20_N.F12	128
129	GND	-	GND	130
131	ODD21_P.F11	0	EVN21_P.D11	132
133	ODD21_N.G11	0	EVN21_N.E11	134
135	ODD22_P.A8	0	EVN22_P.C10	136
137	ODD22_N.B8	0	EVN22_N.D10	138
139	ODD23_P.A7	0	EVN23_P.E10	140
141	ODD23_N.B7	0	EVN23_N.F10	142
143	ODD24_P.D7	0	EVN24_P.F9	144
145	ODD24_N.E7	0	EVN24_N.G9	146
147	ODD25_P.D6	0	EVN25_P.B6	148
149	ODD25_N.E6	0	EVN25_N.C6	150
151	GND	-	GND	152
153	ODD26_P.A4	0	EVN26_P.B5	154
155	ODD26_N.B4	0	EVN26_N.C5	156
157	ODD27_P.D2	7	EVN27_P.J5	158
159	ODD27_N.D1	7	EVN27_N.J4	160
161	ODD28_P.H5	7	EVN28_P.H4	162
163	ODD28_N.J6	7	EVN28_N.H3	164
165	ODD29_P.K6	7	EVN29_P.J3	166
167	ODD29_N.K5	7	EVN29_N.J2	168
169	ODD30_P.G2	7	EVN30_P.K4	170
171	ODD30_N.G1	7	EVN30_N.K3	172
173	GND	-	GND	174
175	ODD31_P.H2	7	EVN31_P.L6	176
177	ODD31_N.H1	7	EVN31_N.L5	178
179	ODD32_P.K2	7	EVN32_P.M5	180
181	ODD32_N.K1	7	EVN32_N.M6	182
183	ODD33_P.L2	7	EVN33_P.L4	184
185	ODD33_N.L1	7	EVN33_N.M3	186
187	ODD34_P.M2	7	EVN34_P.N4	188
189	ODD34_N.M1	7	EVN34_N.N3	190
191	ODD35_P.N2	7	EVN35_P.N6	192
193	ODD35_N.N1	7	EVN35_N.N5	194
195	GND	-	GND	196
197	3.3V	-	3.3V	198
199	3.3V	-	3.3V	200

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Table 3: Signal Group Description

Signal / Group	I/O	Description
3.3 V	N/A	3.3 volt reference input power referenced to GND.
MRESET#	I	Manual Reset. Pulled-up on the MityDSP-Pro module. When driven to GND for a minimum of 1 us, a module-wide reset is triggered. Can be tied into system system-wide reset and power monitoring circuitry.
ETH_TD_P / N ETH_RD_P / N	O I	Ethernet Transmit Data & Receive Data link lines. These pairs of signals are connected to the onboard 10/100 Ethernet PHY connected to the DSP EMAC. These pairs should be routed through appropriate 1:1 magnetics prior to exposure to an RJ-45 type connector interface.
FPGA_RSV1 / 2	IO	Reserved for Ethernet RJ45 Link & Activity LED signals, driven by the on-board 10/100 PHY. Can also be used as general purpose FPGA I/O.
CLKR0 / 1 CLKX0 / 1 DR0 / 1 DX0 / 1 FSR0 / 1	IO	These pins are direct connects to the corresponding McBSP port-0 / port-1 pins on the C645x DSP. For further interface information, please refer to the TMS645x McBSP Users Guide and Data Sheets.
BOOT_MODE	I	Boot Mode Selection. Reserved for future use. Do not connect.
SCL, SDA	I/O	These pins are connected to the I2C interface on the C645x DSP, and also to FPGA pins. For further interface information, please refer to the TMS320C645x I2C Users Guide and Data Sheets.
GND	N/A	System Digital Ground.
ODDXX_P/N.YYY EVNXX_P/N.YYY	IO	FPGA General Purpose I/O pin. FPGA I/O pins have been routed to the MityDSP connector in pairs denoted ODDXX (odd pin side of connector) or EVNXX (even pin side of connector). When configured for differential termination the pairs should be used according to the _P (positive) or _N (negative) extension. The YYY portion of the name corresponds to the FPGA pin location mapped to the signal.
VCCO_N	N/A	FPGA Banks 0, 1, 2, and 7 Voltage configuration. Leave disconnected for 2.5V bank logic (LVCMOS25 or LVDS25). Connect to 3.3V power supply for 3.3V bank logic (LVCMOS33 or LVTTL). PCB trace must be capable of providing a minimum of 200 mA.

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Debug Interface Description

The debug interface connector pin-out is specified in the table below.

Table 4: Debug Connector Pin-Out

Pin	Signal	Signal	Pin
1	DSP_EMU0	DSP_TMS	2
3	DSP_EMU1	DSP_TDI	4
5	3.3V	DSP_TDO	6
7	GND	DSP_TCK	8
9	GND	DSP_TRST#	10
11	FPGA_TDI	FPGA_TMS	12
13	FPGA_TCK	FPGA_TDO	14
15	GND	2.5V	16

Expansion Interface Description

The Expansion Interface pin-out is described in the table below.

Table 5: Expansion Interface Pin-Out

Pin	Signal	Signal	Pin
1	GND	GND	2
3	RIORX0_N	RIOTX0_P	4
5	RIORX0_P	RIOTX0_N	6
7	RIORX1_P	RIOTX1_P	8
9	RIORX1_N	RIOTX1_N	10
11	RIORX2_N	RIOTX2_N	12
13	RIORX2_P	RIOTX2_P	14
15	RIORX3_P	RIOTX3_N	16
17	RIORX3_N	RIOTX3_P	18
19	RIOCLK_N	GND	20
21	RIOCLK_P	HPI_WIDTH	22
23	GND	PCI_AD27	24
25	PCI_EEAI	PCI_AD1	26
27	PCI66	PCI_AD30	28
29	PCI_EN	PCI_AD0	30
31	PCI_AD11	PCI_AD4	32
33	PCI_AD10	PCI_AD22	34
35	PCI_AD3	PCI_AD25	36
37	PCI_AD5	PCI_AD8	38
39	PCI_AD29	PCI_AD21	40
41	PCI_AD23	PCI_AD13	42
43	PCI_AD7	PCI_AD2	44
45	PCI_AD9	PCI_AD19	46
47	PCI_AD28	PCI_AD15	48
49	PCI_AD31	PCI_ERR#	50
51	PCI_AD16	PCI_AD17	52
53	PCI_AD6	PCI_AD18	54
55	PCI_AD14	PCI_STOP#	56
57	GND	PCI_AD26	58
59	PCI_CLK	PCI_AD20	60
61	GND	PCI_CBE2#	62

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Pin	Signal	Signal	Pin
63	PCI_AD12	PCI_AD24	64
65	PCI_FRAME#	PCI_SERR#	66
67	PCI_DEVSEL#	PCI_RST#	68
69	PCI_PAR	PCI_CBE1#	70
71	PCI_IDSEL	PCI_CBE0#	72
73	PCI_IRDY#	PCI_CBE3#	74
75	PCI_GNT#	PCI_REQ#	76
77	PCI_INTA#	MAC_SEL	78
79	PCI_TRDY#	RGMII_VREF	80
81	GND	GND	82
83	RGMDCLK	RGREFCLK	84
85	RGMDIO	GND	86
87	RGRXD3	RGTXD3	88
89	RGRXD2	RGTXD2	90
91	RGRXD1	RGTXD1	92
93	RGRXD0	RGTXD0	94
95	RGRXCTL	RGTXCTL	96
97	RGRXC	RGTXC	98
99	GND	GND	100

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ORDERING INFORMATION

The following table lists the orderable module configurations. For shipping status, availability, and lead time of these or other configurations please contact your Critical Link representative.

Table 6: Orderable Model Numbers

Model	CPU Speed	FPGA	L2 CPU Cache	NOR Flash	CPU DDR2 RAM	FPGA DDR1 RAM	Operating Temp
6455-JE-3X5-RC	1.2 GHz	XC3S4000	2 MB	16MB	128MB	64MB	0°C to 70° C
6455-IE-3X5-RI	1.0 GHz	XC3S4000	2 MB	16MB	128MB	64MB	-40°C to 85° C
6454-GD-3X5-RC	720 MHz	XC3S2000	1 MB	16MB	128MB	64MB	0°C to 70° C
6454-ID-3X5-RI	1.0 GHz	XC3S2000	1 MB	16MB	128MB	64MB	-40°C to 85° C

MECHANICAL INTERFACE

A mechanical outline of the MityDSP-Pro is illustrated below.

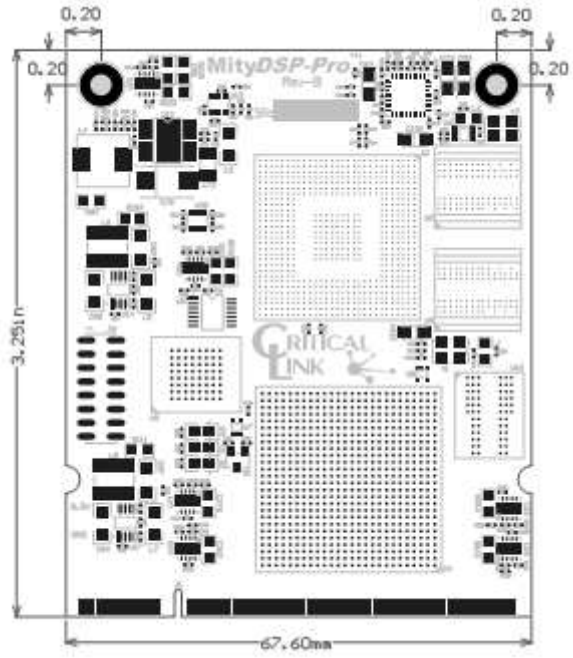


Figure 3: Dimensions 3.25" x 2.7"

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REVISION HISTORY

Date	Change Description
13-MAR-2012	Update available model numbers and add rev history

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