NBSG111BAEVB

Evaluation Board Manual for NBSG111

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EVALUATION BOARD MANUAL

DESCRIPTION

This document describes the NBSG111 evaluation board and the appropriate lab test setups. It should be used in conjunction with the NBSG111 data sheet which contains full technical details on the device specifications and operation.

The evaluation board is designed to facilitate a quick evaluation of the NBSG111 GigaComm™ 1:10 clock data driver. The NBSG111 allows selection between two inputs and fan out 10 identical differential outputs. The Reduced Swing ECL (RSECL) output ensures minimal noise and fast switching edges.

The evaluation board is implemented in two layers for higher performance. For standard lab setup and test, a split (dual) power supply is required enabling the 50 Ω impedance from the scope to be used as termination of the ECL signals ($V_{TT} = V_{CC} - 2.0$ V, in split power supply setup, V_{TT} is the system ground).

What measurements can you expect to make?

With this evaluation board, the following measurements could be performed in single−ended(1) or differential modes of operation:

- Jitter
- Output Skew
- Gain/Return Loss
- Eye Pattern Generation
- Frequency Performance
- Output Rise and Fall Time
- V_{IHCMR} (Input High Common Mode Range)

1. Single−ended measurements can only be made at $V_{CC} - V_{EE} = 3.3$ V using this board setup.

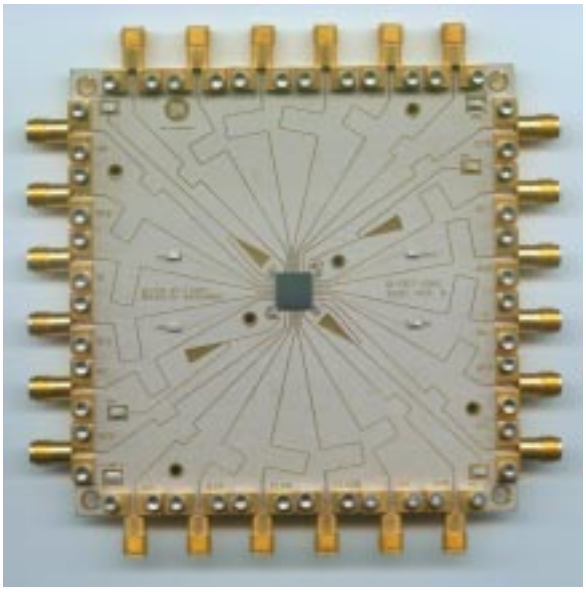


Figure 1. NBSG111 Evaluation Board

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Setup for Time Domain Measurements

Table 1. Basic Equipment

Description	Example Equipment (Note 1)	Qty.
Power Supply with 2 outputs	HP6624A	1
Oscilloscope	TDS8000 with 80E01 Sampling Head (Note 2)	1
Differential Signal Generator	HP 8133A, Advantest D3186	1
Matched high speed cables with SMA connectors	Storm, Semflex	10
Power Supply cables with clips		3

1. Equipment used to generate example measurements within this document.
2. 50 GHz sample module used (for effective rise, fall and jitter performance measurement)

Setup

Step 1:

Connect Power

1a: Three power levels must be provided to the board for V_{CC}, V_{EE}, and GND via the surface mount clips. Using the split power supply mode, GND = V_{TT} = V_{CC} − 2.0 V.

Power Supply Connections	
3.3 V Setup	**2.5 V Setup**
V_{CC} = 2.0 V	V_{CC} = 2.0 V
V_{TT} = GND	V_{TT} = GND
V_{EE} = −1.3 V	V_{EE} = −0.5 V

Step 2:

Connect Inputs

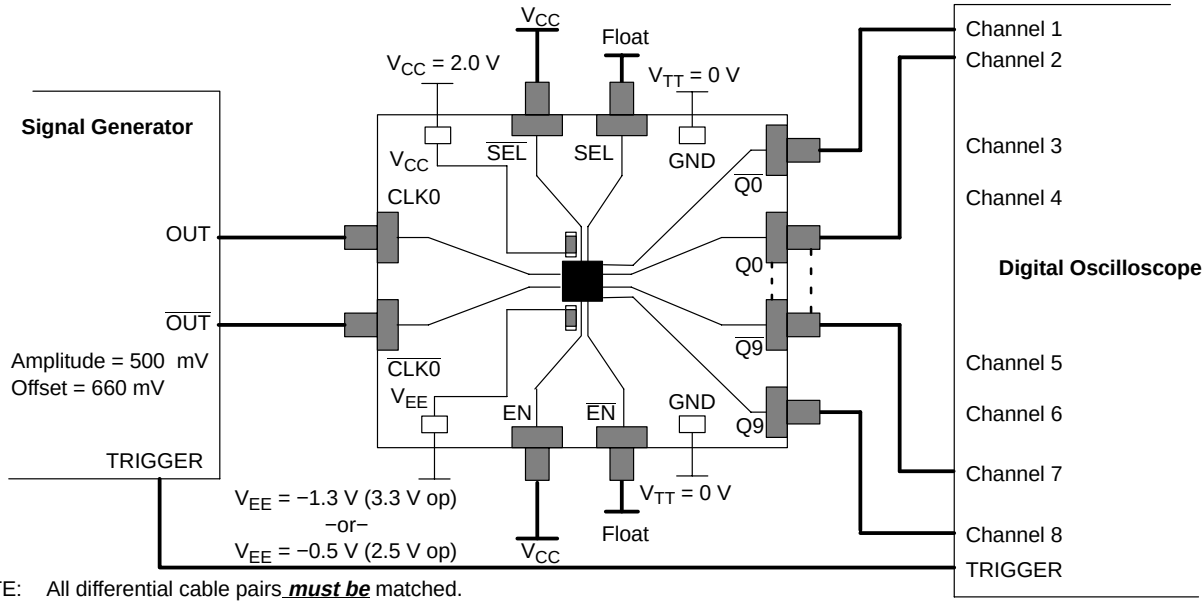
For Differential Mode (3.3 V and 2.5 V operation)

2a: Connect the differential output of the generator to the differential input of the device (CLK0 and $\overline{CLK0}$).

For Single−Ended Mode (3.3 V operation only)

2a: Connect the AC coupled single−ended output generator to input.

NOTE: For best results, unconnected input should be terminated to V_{TT} through 50 Ω resistor



NOTE: All differential cable pairs ***must be*** matched.
Due to simplifcation of the block diagram CLK1/$\overline{CLK1}$ and Q1 − Q8 connections are not shown. * Q0 − Q9 Ouputs

Figure 2. NBSG111 Board Setup − Time Domain (Differential Mode)

Setup (continued)

Setup Input Signals

Step 3: 3a: Set the signal generator amplitude to 500 mV.

NOTE: The signal generator amplitude can vary from 75 mV to 900 mV to produce a 400 mV DUT output.

3b: Set the signal generator offset to 660 mV (the center of a nominal RSECL PECL output).

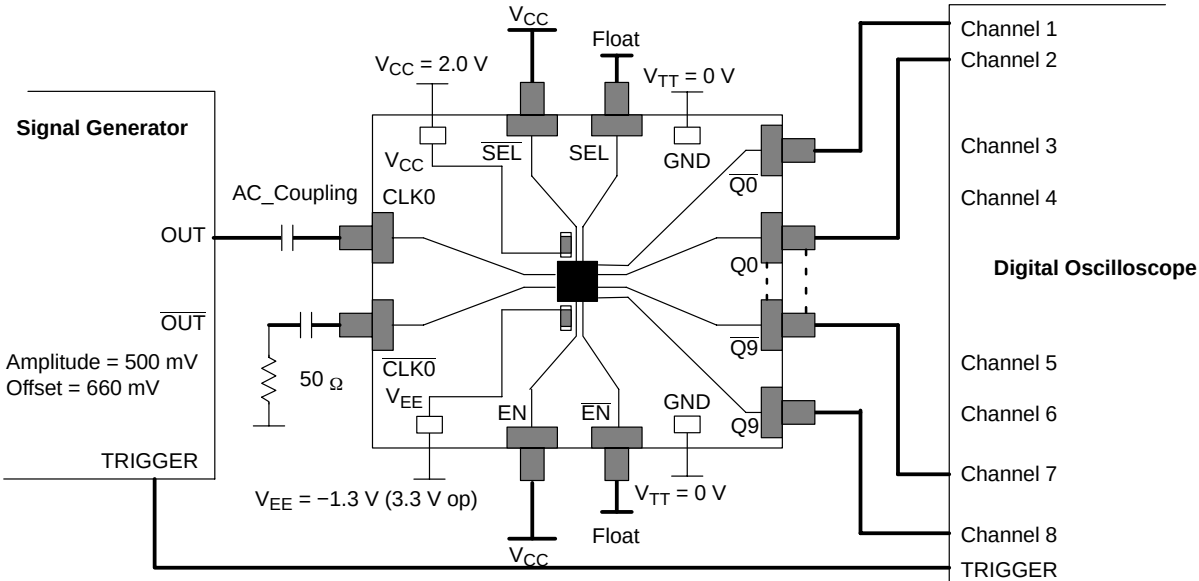
NOTE: The V_{IHCMR} (Input High Voltage Common Mode Range) allows the signal generator offset to vary as long as V_{IH} is within the V_{IHCMR} range. Refer to the device data sheet for further information.

3c: Set the generator output for a PRBS data signal, or for a square wave clock signal with a 50% duty cycle.

Connect Output Signals

Step 4: 4a: Connect the outputs of the device (Q0, Q1, …) to the Oscilloscope. The oscilloscope sampling head must have internal 50 Ω termination to ground.

NOTE: Where a single output is being used, the unconnected output for the pair ***must be*** terminated to V_{TT} through a 50 Ω resistor for best operation. Unused pairs may be left unconnected. Since V_{TT} = 0 V, a standard 50 Ω SMA termination is recommended.



NOTE: All differential cable pairs ***must be*** matched.
Due to simplifcation of the block diagram CLK1/$\overline{CLK1}$ and Q1 − Q8 connections are not shown. * Q0 − Q9 Outputs

Figure 3. NBSG111 Board Setup − Time Domain (Single−Ended Mode)

Setup for Frequency Domain Measurements

Table 2. Basic Equipment

Description	Example Equipment (Note 3)	Qty.
Power Supply with 2 outputs	HP 6624A	1
Vector Network Analyzer (VNA)	R&S ZVK (10 MHz to 40 GHz)	1
180° Hybrid Coupler	Krytar Model #4010180	1
Bias Tee with 50 Ω Resistor Termination	Picosecond Model #5542−219	1
Matched high speed cables with SMA connectors	Storm, Semflex	3
Power Supply cables with clips		3

3. Equipment used to generate example measurements.

Setup

Step 1:

Connect Power

1a: Three power levels must be provided to the board for V_{CC}, V_{EE}, and GND via the surface mount clips. Using the split power supply mode, GND = V_{TT} = V_{CC} − 2.0 V.

Power Supply Connections	
3.3 V Setup	**2.5 V Setup**
V_{CC} = 2.0 V	V_{CC} = 2.0 V
V_{TT} = GND	V_{TT} = GND
V_{EE} = −1.3 V	V_{EE} = −0.5 V

NOTE: For frequency domain measurements, 2.5 V power supply is not recommended because additional equipment (bias tee, etc.) is needed for proper operation. The input signal has to be properly offset to meet V_{IHCMR} range of the device.

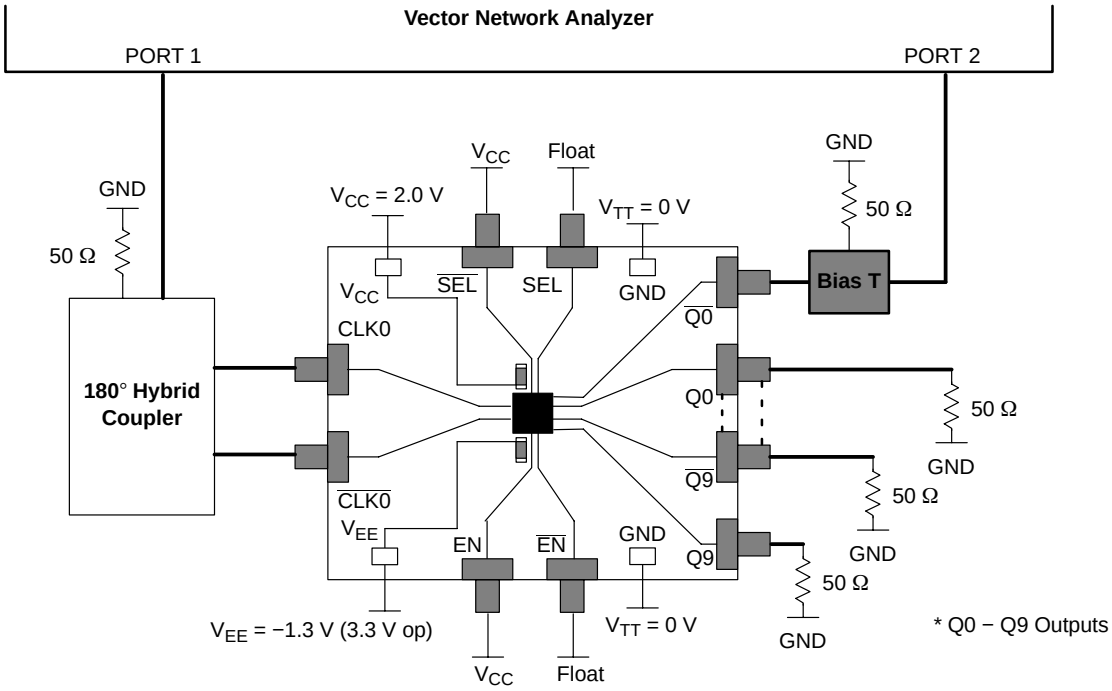
Setup Test Configurations For Differential Operation

Small Signal Setup

Step 2:	**Input Setup** 2a: Calibrate VNA from 1.0 GHz to 12 GHz. 2b: Set input level to –35 dBm at the output of the 180° Hybrid coupler (input of the DUT).
Step 3:	**Output Setup** 3a: Set display to measure S21 and record data.

Large Signal Setup

Step 2:	**Input Setup** 2a: Calibrate VNA from 1.0 GHz to 12 GHz. 2b: Set input levels to −2.0 dBm (500 mV) at the input of DUT.
Step 3:	**Output Setup** 3a: Set display to measure S21 and record data.



NOTE: All differential cable pairs ***must be*** matched.
Due to simplifcation of the block diagram CLK1/$\overline{\text{CLK1}}$ and Q1 − Q8 connections are not shown.

Figure 4. NBSG111 Board Setup – Frequency Domain (Differential Mode)

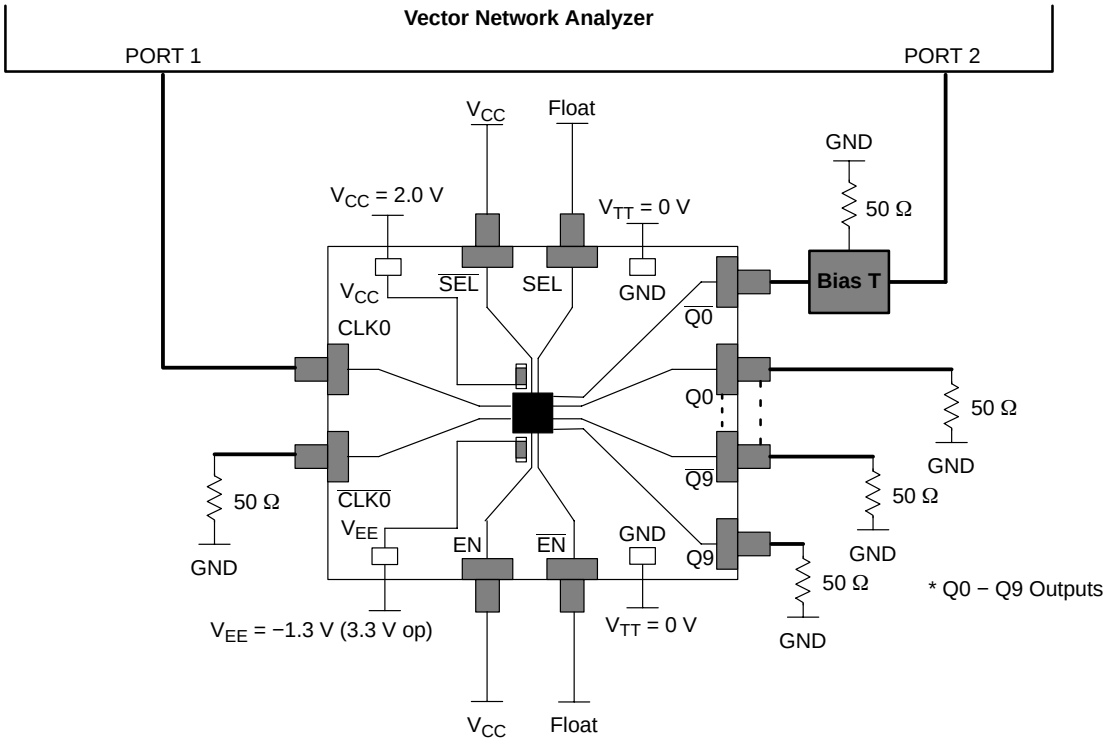
Setup Test Configurations For Single−Ended Operation

Single−Ended Mode – Small Signal

Step 2:	**Input Setup** 2a: Calibrate VNA from 1.0 GHz to 12 GHz. 2b: Set input level to –35 dBm at the input of DUT.
Step 3:	**Output Setup** 3a: Set display to measure S21 and record data.

Single−Ended Mode – Large Signal

Step 2:	**Input Setup** 2a: Calibrate VNA from 1.0 GHz to 12 GHz. 2b: Set input levels to +2 dBm (500 mV) at the input of DUT.
Step 3:	**Output Setup** 3a: Set display to measure S21 and record data.



NOTE: All differential cable pairs ***must be*** matched.
Due to simplifcation of the block diagram CLK1/$\overline{\text{CLK1}}$ and Q1 − Q8 connections are not shown.

Figure 5. NBSG111 Board Setup – Frequency Domain (Single−Ended Mode)

More Information About Evaluation Board

Design Considerations for >10 GHz operation

While the NBSG111 is specified to operate at 12 GHz, this evaluation board is designed to support operating frequencies up to 20 GHz.

The following considerations played a key role to ensure this evaluation board achieves high−end microwave performance:

- Optimal SMA connector launch
- Minimal insertion loss and signal dispersion
- Accurate Transmission line matching (50 ohms)
- Distributed effects while bypassing and noise filtering

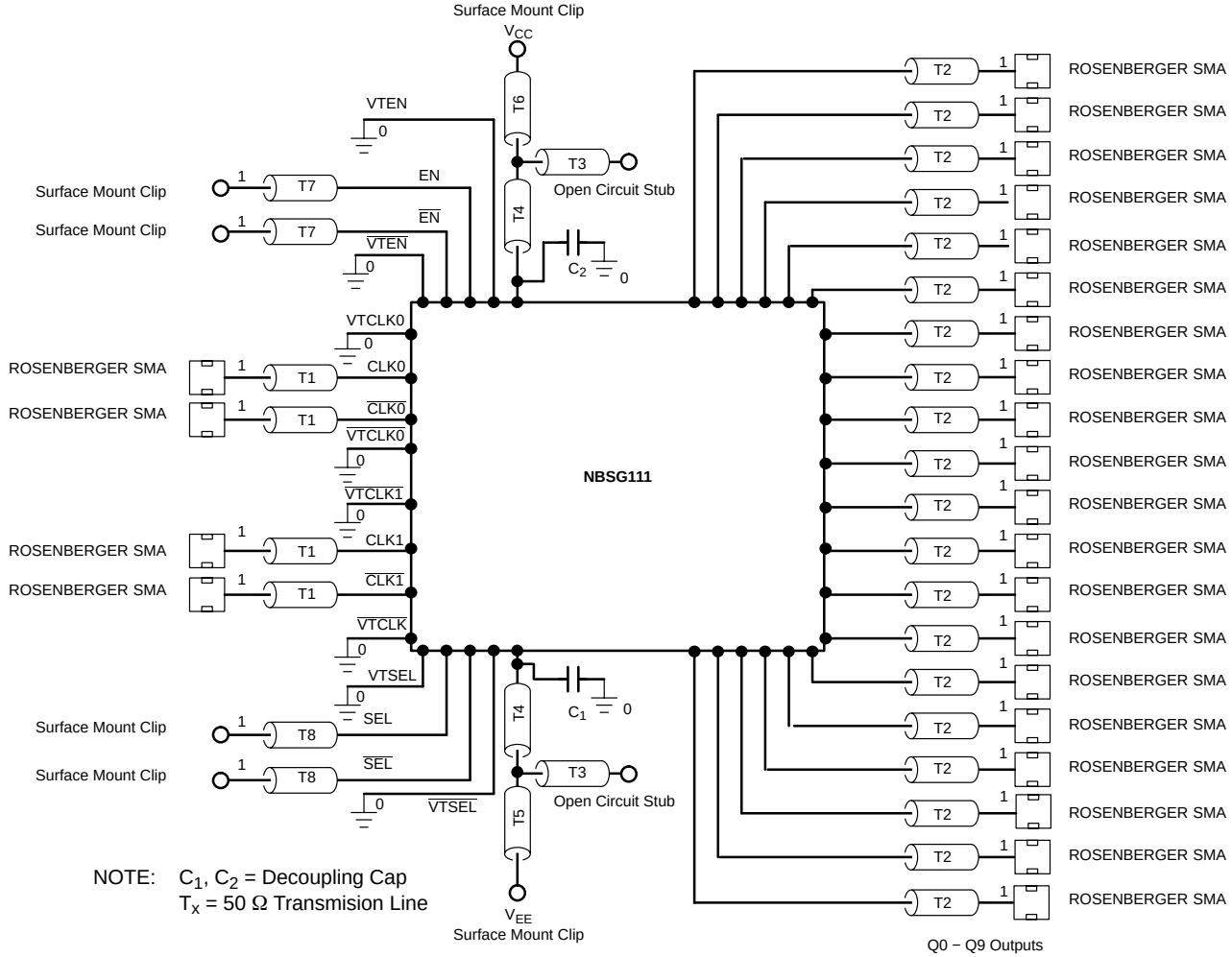


Figure 6. Evaluation Board Schematic

Table 3. Parts List

Part No	Description	Manufacturer	WEB address
NBSG111BA	2.5V/3.3V SiGe Differential 1:10 Clock/Data Driver with RSECL Outputs	ON Semiconductor	http://www.onsemi.com/NBSG111
32K243−40ME3	Gold plated connector	Rosenberger	http://www.rosenberger.de
CO6BLBB2X5UX	2 MHz – 30 GHz capacitor	Dielectric Laboratories	http://www.dilabs.com

Table 4. Board Material

Material	Thickness
Rogers 6002	5.0 mil
Copper Plating	32 mil

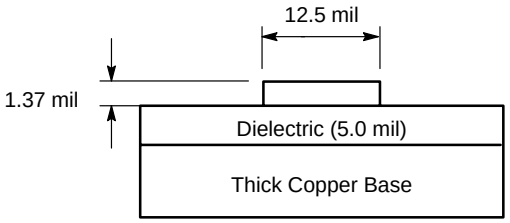


Figure 7. Board Stack−up

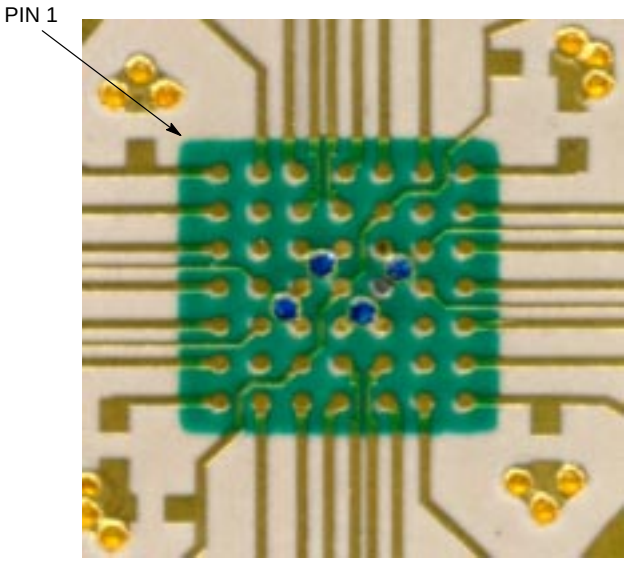


Figure 8. Layout Mask for NBSG111

EXAMPLE MEASUREMENTS IN TIME DOMAIN

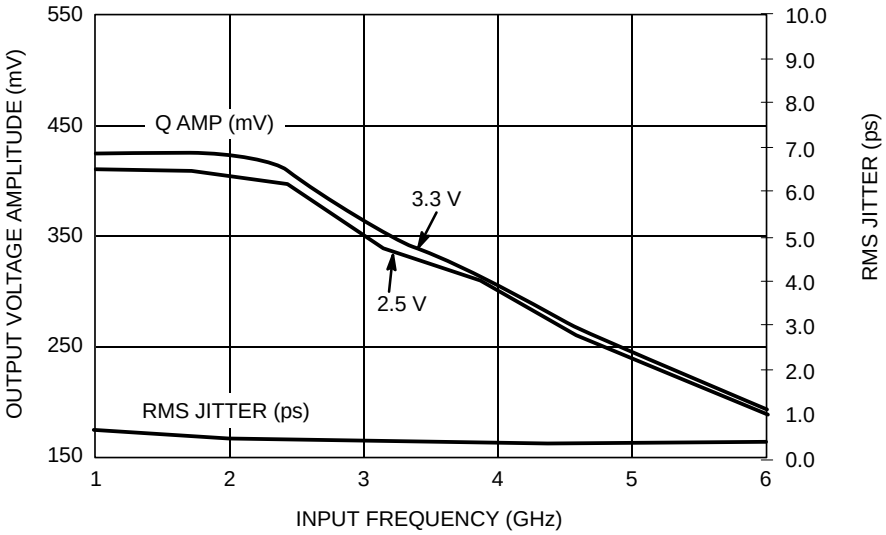


Figure 9. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) at Ambient Temperature (Typical)

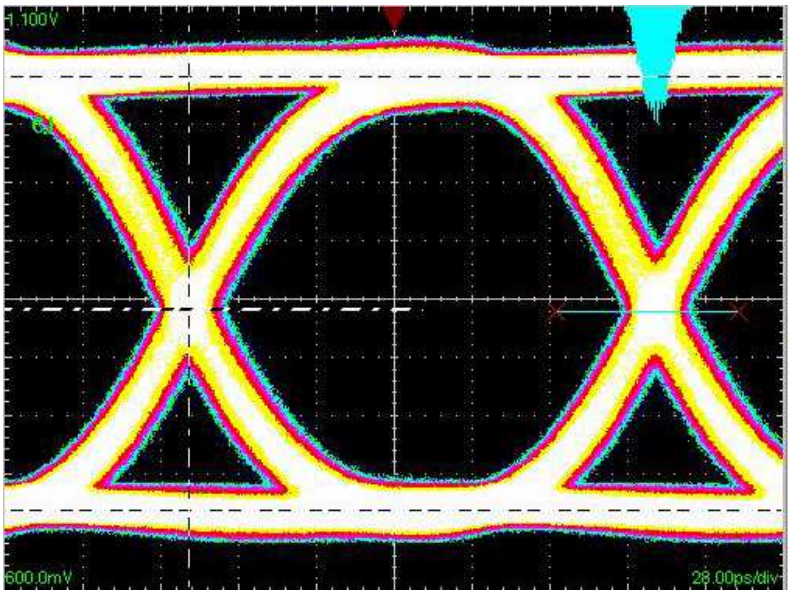


Figure 10. NBSG111: Eye Diagram at 6 Gbps with PRBS 2^31−1 (Total Pk−Pk system jitter including signal generator is 28 ps. Device Pk−Pk jitter is typically 14 ps.)

ADDITIONAL EVALUATION BOARD INFORMATION

www.onsemi.com

In all cases, the most up−to−date information can be found on our website.

- Sample orders for devices and boards
- New Product updates
- Literature download/order
- IBIS and Spice models

References

NBSG111/D, Data Sheet, *NBSG111, 2.5V/3.3V SiGe 1:10 Differential Clock / Data Driver with RSECL Outputs*

AND8077/D, Application Note, *GigaComm™ (SiGe) SPICE Modeling Kit.*

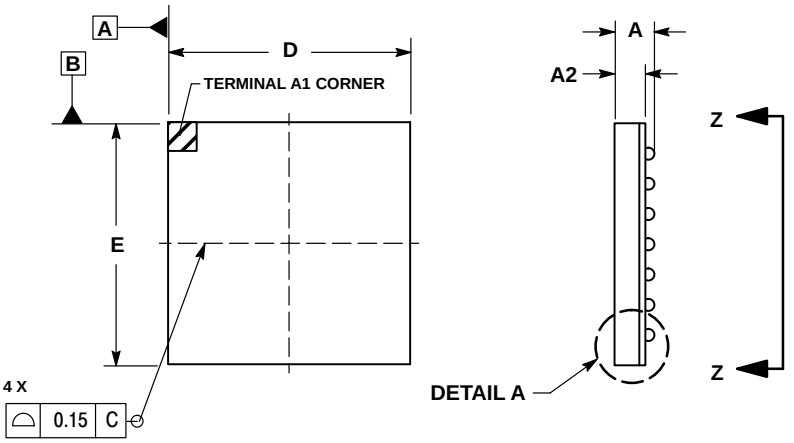
AND8075/D, Application Note, *Board Mounting Considerations for the FCBGA Packages.*

ORDERING INFORMATION

Orderable Part No	Description	Package	Shipping
NBSG111BA	2.5V/3.3V SiGe Differential 1:10 Clock/Data Driver with RSECL Outputs	4X4 mm FCBGA−49	100 Units/Tray
NBSG111BA	2.5V/3.3V SiGe Differential 1:10 Clock/Data Driver with RSECL Outputs	4X4 mm FCBGA−49	500 Units/Reel
NBSG111BAEVB	NBSG111 Evaluation Board		

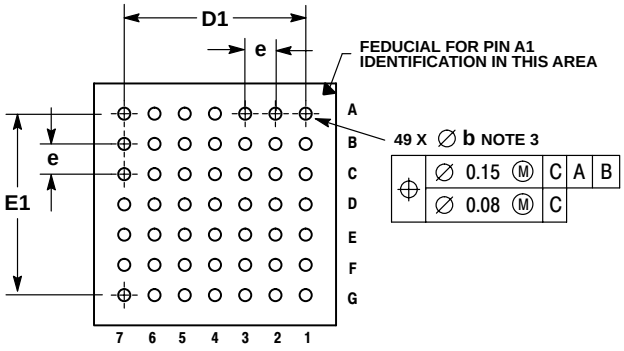
PACKAGE DIMENSIONS

FCBGA−49
BA SUFFIX
PLASTIC 8x8 mm (1.0 mm pitch) BGA FLIP CHIP PACKAGE
CASE 489A−02
ISSUE A

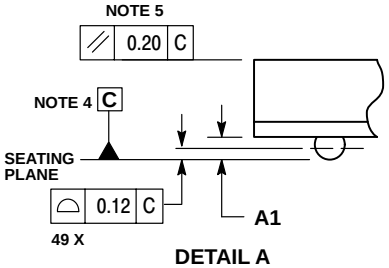


NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
4. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. 489A−01 OBSOLETE, NEW STANDARD 489A−02.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	1.40
A1	0.3	0.5
A2	0.91 REF	
b	0.40	0.60
D	8.00 BSC	
D1	6.00 BSC	
E	8.00 BSC	
E1	6.00 BSC	
e	1.00 BSC	



VIEW Z−Z



DETAIL A
(ROTATED 90° C.W.)

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