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February 1996

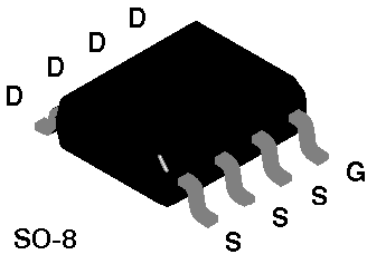
# NDS8410
# Single N-Channel Enhancement Mode Field Effect Transistor

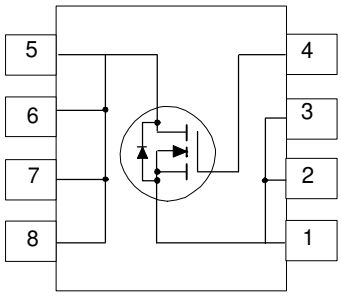
### General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

### Features

- 10A, 30V. $R_{DS(ON)}$ = 0.015Ω @ $V_{GS}$ = 10V
  $R_{DS(ON)}$ = 0.020Ω @ $V_{GS}$ = 4.5V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.




## Absolute Maximum Ratings $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | | NDS8410 | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 30 | V |
| $V_{GSS}$ | Gate-Source Voltage | | 20 | V |
| $I_D$ | Drain Current - Continuous | (Note 1a) | ± 10 | A |
| | - Pulsed | | ± 50 | |
| $P_D$ | Maximum Power Dissipation | (Note 1a) | 2.5 | W |
| | | (Note 1b) | 1.2 | |
| | | (Note 1c) | 1 | |
| $T_J$,$T_{STG}$ | Operating and Storage Temperature Range | | -55 to 150 | °C |
| **THERMAL CHARACTERISTICS** | | | | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 50 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 25 | °C/W |

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 30 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | | | 1 | µA |
| | | $T_J$ = 55°C | | | 10 | µA |
| $I_{GSSF}$ | Gate - Body Leakage, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | | | 100 | nA |
| $I_{GSSR}$ | Gate - Body Leakage, Reverse | $V_{GS}$ = -20 V, $V_{DS}$ = 0 V | | | -100 | nA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 1 | 1.5 | | V |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 10 A | | 0.013 | 0.015 | Ω |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 9 A | | 0.018 | 0.02 | |
| $I_{D(on)}$ | On-State Drain Current | $V_{GS}$ = 10 V, $V_{DS}$ = 5 V | 20 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 10 A | | 22 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 1350 | | pF |
| $C_{oss}$ | Output Capacitance | | | 800 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 300 | | pF |
| **SWITCHING CHARACTERISTICS** (Note 2) | | | | | | |
| $t_{D(on)}$ | Turn - On Delay Time | $V_{DD}$ = 10 V, $I_D$ = 1 A, $V_{GEN}$ = 10 V, $R_{GEN}$ = 6 Ω | | 14 | 30 | ns |
| $t_r$ | Turn - On Rise Time | | | 20 | 25 | ns |
| $t_{D(off)}$ | Turn - Off Delay Time | | | 56 | 100 | ns |
| $t_f$ | Turn - Off Fall Time | | | 31 | 80 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 15 V, $I_D$ = 10 A, $V_{GS}$ = 10 V | | 46 | 60 | nC |
| $Q_{gs}$ | Gate-Source Charge | | | 5.6 | | nC |
| $Q_{gd}$ | Gate-Drain Charge | | | 14 | | nC |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | | | 2.1 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 10 A (Note 2) | | 0.8 | 1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0V, $I_F$ = 2.1 A, $dI_F/dt$ = 100 A/µs | | | 80 | ns |

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

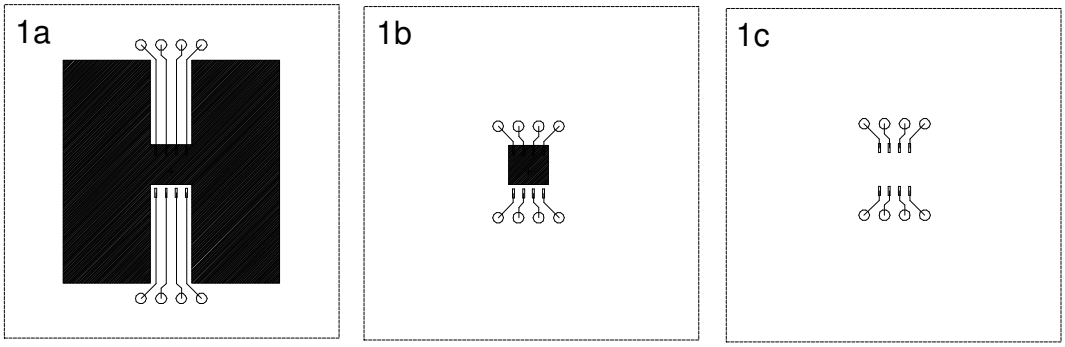
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 50°C/W when mounted on a 1 $in^2$ pad of 2oz copper.

b. 105°C/W when mounted on a 0.04 $in^2$ pad of 2oz copper.

c. 125°C/W when mounted on a 0.006 $in^2$ pad of 2oz copper.




Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

## Typical Electrical Characteristics

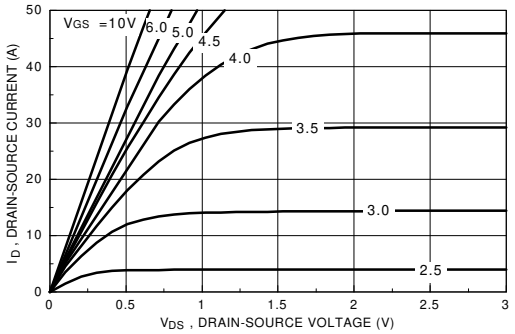



**Figure 1. On-Region Characteristics.**

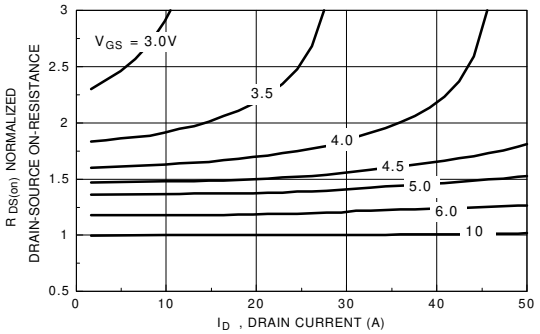



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

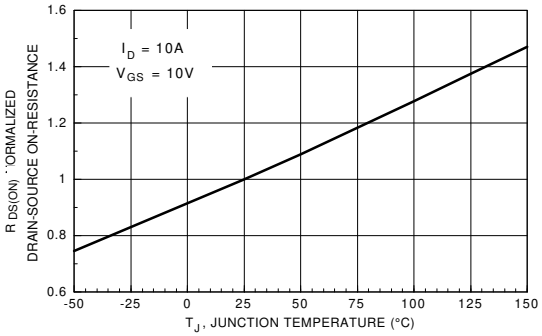



**Figure 3. On-Resistance Variation with Temperature.**

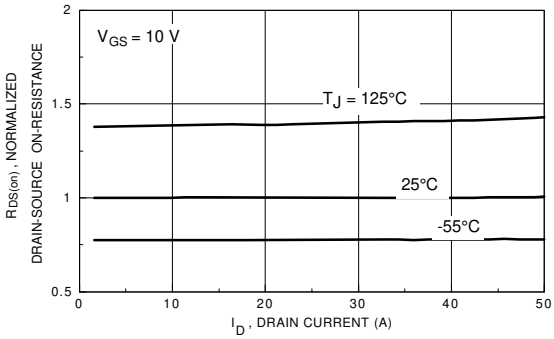



**Figure 4. On-Resistance Variation with Drain Current and Temperature.**

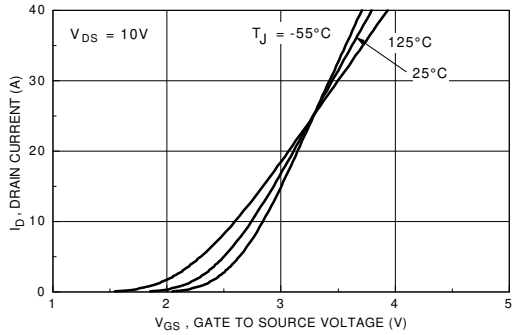



**Figure 5. Transfer Characteristics.**

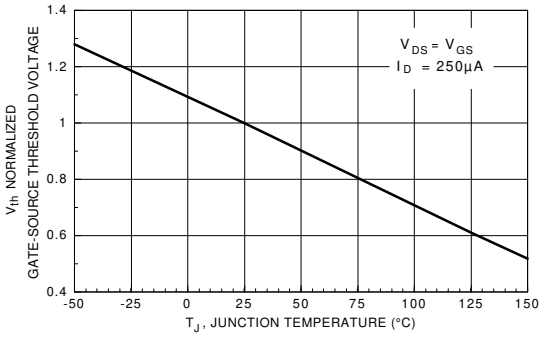



**Figure 6. Gate Threshold Variation with Temperature.**

## Typical Electrical Characteristics (continued)

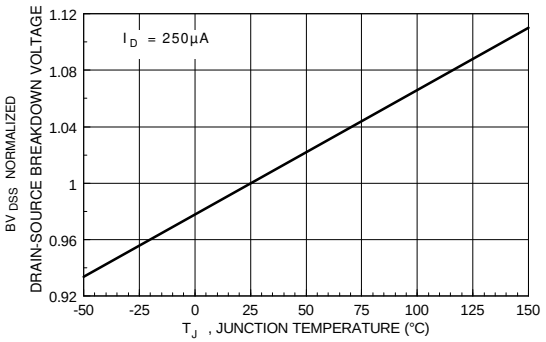



**Figure 7. Breakdown Voltage Variation with Temperature.**

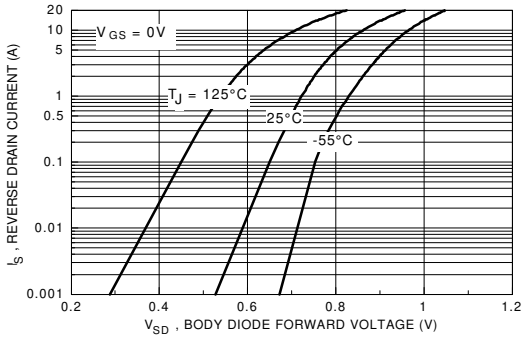



**Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature.**

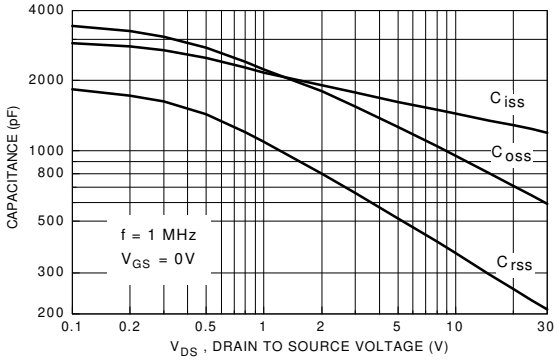



**Figure 9. Capacitance Characteristics.**

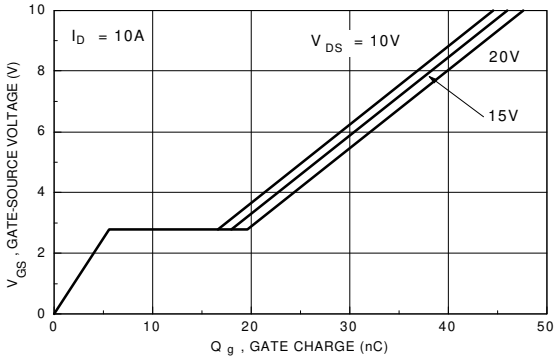



**Figure 10. Gate Charge Characteristics.**

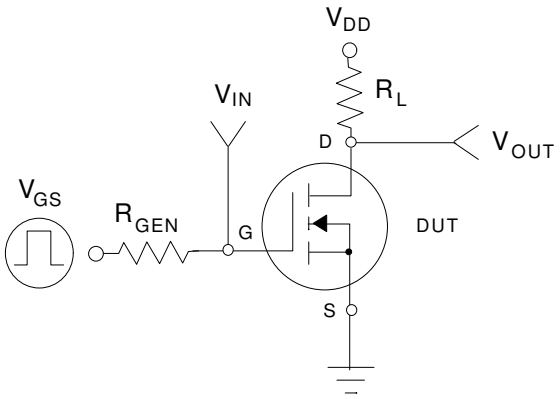



**Figure 11. Switching Test Circuit.**

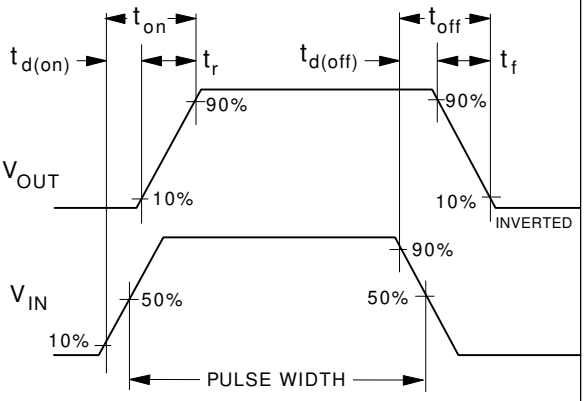



**Figure 12. Switching Waveforms.**

## Typical Electrical and Thermal Characteristics (continued)

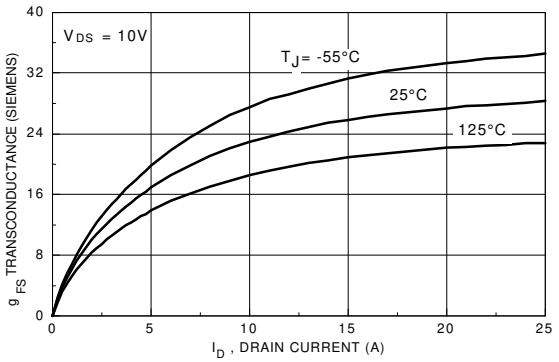



**Figure 13. Transconductance Variation with Drain Current and Temperature.**

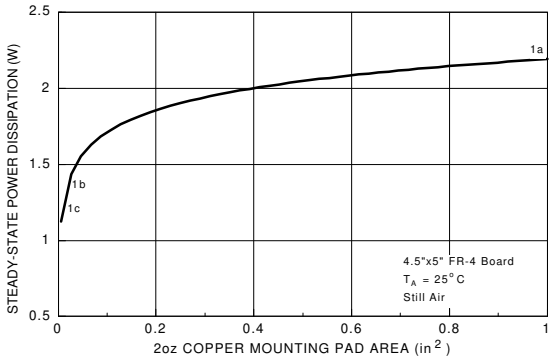



**Figure 14. SO-8 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.**

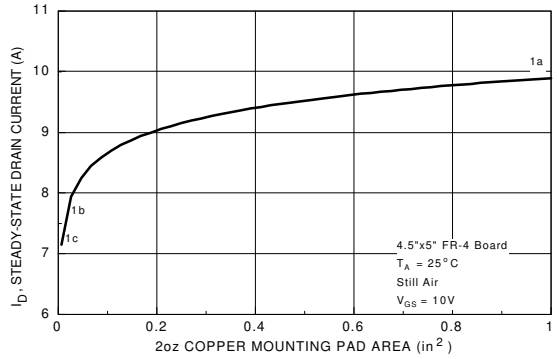



**Figure 15. Maximum Steady- State Drain Current versus Copper Mounting Pad Area.**

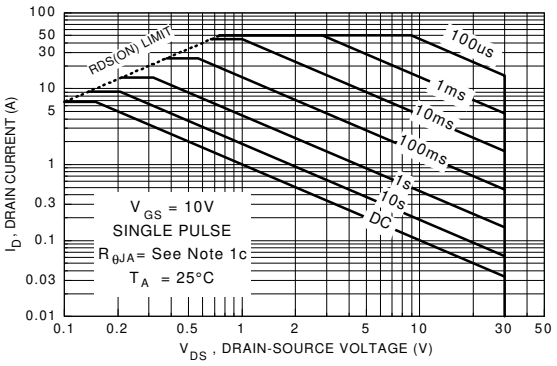



**Figure 16. Maximum Safe Operating Area.**

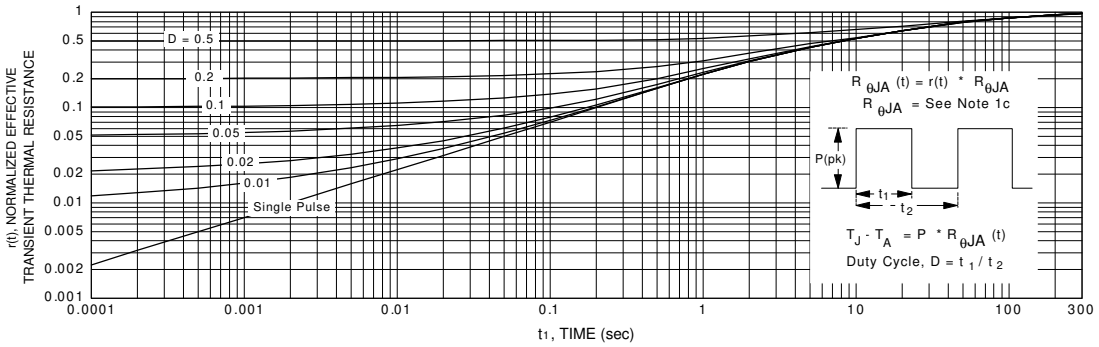



**Figure 17. Transient Thermal Response Curve.**

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

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