NLAS4051

Analog Multiplexer/ Demultiplexer

TTL Compatible, Single−Pole, 8−Position Plus Common Off

The NLAS4051 is an improved version of the MC14051 and MC74HC4051 fabricated in sub−micron Silicon Gate CMOS technology for lower $R_{DS(on)}$ resistance and improved linearity with low current. This device may be operated either with a single supply or dual supply up to ±3.0 V to pass a 6.0 V_{PP} signal without coupling capacitors.

When operating in single supply mode, it is only necessary to tie V_{EE}, pin 7 to ground. For dual supply operation, V_{EE} is tied to a negative voltage, not to exceed maximum ratings.

Features

- Improved $R_{DS(on)}$ Specifications
- Pin for Pin Replacement for MAX4051 and MAX4051A
  - One Half the Resistance Operating at 5.0 V
- Single or Dual Supply Operation
  - Single 2.5−5.0 V Operation, or Dual ±3.0 V Operation
  - With V_{CC} of 3.0 to 3.3 V, Device Can Interface with 1.8 V Logic, No Translators Needed
  - Address and Inhibit Logic are Over−Voltage Tolerant and May Be Driven Up +6.0 V Regardless of V_{CC}
- Improved Linearity Over Standard HC4051 Devices
- Popular SOIC, and Space Saving TSSOP, and QSOP 16 Pin Packages
- Pb−Free Packages are Available*

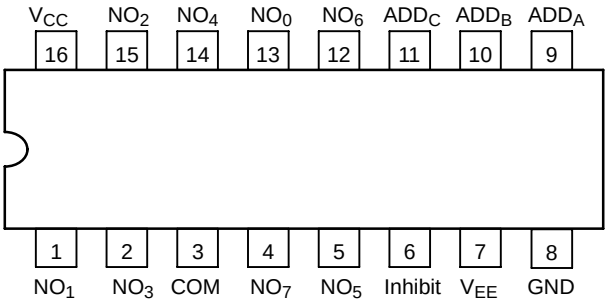


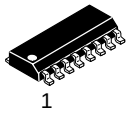
Figure 1. Pin Connection
(Top View)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

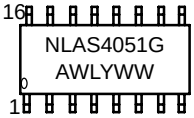
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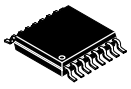
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MARKING DIAGRAMS

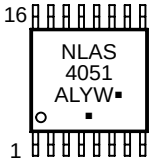


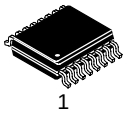
SOIC−16
D SUFFIX
CASE 751B



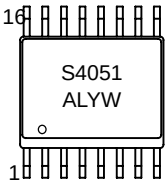


TSSOP−16
DT SUFFIX
CASE 948F





QSOP−16
QS SUFFIX
CASE 492



A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NLAS4051DR2	SOIC−16	2500/Tape & Reel
NLAS4051DR2G	SOIC−16 (Pb−Free)	2500/Tape & Reel
NLAS4051DTR2	TSSOP−16	2500/Tape & Reel
NLAS4051DTR2G	TSSOP−16 (Pb−Free)	2500/Tape & Reel
NLAS4051QSR	QSOP−16	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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TRUTH TABLE

Inhibit	Address C	Address B	Address A	ON SWITCHES*
1	X don't care	X don't care	X don't care	All switches open
0	0	0	0	COM−NO_0
0	0	0	1	COM−NO_1
0	0	1	0	COM−NO_2
0	0	1	1	COM−NO_3
0	1	0	0	COM−NO_4
0	1	0	1	COM−NO_5
0	1	1	0	COM−NO_6
0	1	1	1	COM−NO_7

*NO and COM pins are identical and interchangeable. Either may be considered an input or output; signals pass equally well in either direction.

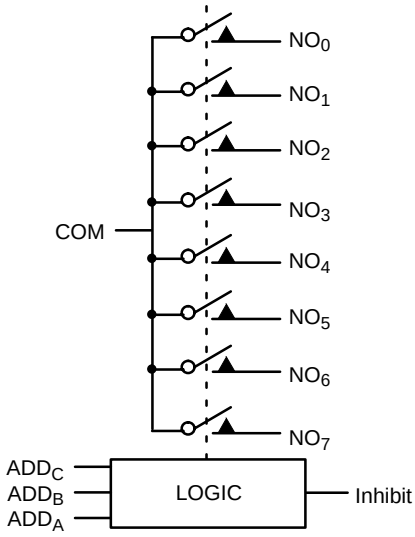


Figure 2. Logic Diagram

MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Negative DC Supply Voltage	(Referenced to GND)	V_{EE}	−7.0 to +0.5	V
Positive DC Supply Voltage (Note 1)	(Referenced to GND) (Referenced to V_{EE})	V_{CC}	−0.5 to +7.0 −0.5 to +7.0	V
Analog Input Voltage		V_{IS}	V_{EE} −0.5 to V_{CC} +0.5	V
Digital Input Voltage	(Referenced to GND)	V_{IN}	−0.5 to 7.0	V
DC Current, Into or Out of Any Pin		I	±50	mA
Storage Temperature Range		T_{STG}	−65 to +150	°C
Lead Temperature, 1 mm from Case for 10 Seconds		T_L	260	°C
Junction Temperature under Bias		T_J	+150	°C
Thermal Resistance	SOIC TSSOP QSOP	θ_{JA}	143 164 164	°C/W
Power Dissipation in Still Air,	SOIC TSSOP QSOP	P_D	500 450 450	mW
Moisture Sensitivity		MSL	Level 1	
Flammability Rating	Oxygen Index: 30% − 35%	F_R	UL 94 V−0 @ 0.125 in	
ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	V_{ESD}	>2000 >200 >1000	V
Latchup Performance	Above V_{CC} and Below GND at 125°C (Note 5)	$I_{LATCHUP}$	±300	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The absolute value of V_{CC} + $|V_{EE}| \le 7.0$.
2. Tested to EIA/JESD22−A114−A.
3. Tested to EIA/JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Max	Unit
Negative DC Supply Voltage	(Referenced to GND)	V_{EE}	−5.5	GND	V
Positive DC Supply Voltage	(Referenced to GND) (Referenced to V_{EE})	V_{CC}	2.5 2.5	5.5 6.6	V
Analog Input Voltage		V_{IS}	V_{EE}	V_{CC}	V
Digital Input Voltage	(Note 6) (Referenced to GND)	V_{IN}	0	5.5	V
Operating Temperature Range, All Package Types		T_A	−55	125	°C
Input Rise/Fall Time (Channel Select or Enable Inputs)	V_{CC} = 3.0 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	t_r, t_f	0 0	100 20	ns/V

6. Unused digital inputs may not be left open. All digital inputs must be tied to a high−logic voltage level or a low−logic input voltage level.

DC CHARACTERISTICS − Digital Section (Voltages Referenced to GND)

Parameter	Condition	Symbol	V_{CC} V	Guaranteed Limit			Unit
				−55 to 25°C	≤ 85°C	≤ 125°C	
Minimum High−Level Input Voltage, Address and Inhibit Inputs		V_{IH}	2.5 3.0 4.5 5.5	1.75 2.1 3.15 3.85	1.75 2.1 3.15 3.85	1.75 2.1 3.15 3.85	V
Maximum Low−Level Input Voltage, Address and Inhibit Inputs		V_{IL}	2.5 3.0 4.5 5.5	.45 0.9 1.35 1.65	.45 0.9 1.35 1.65	.45 0.9 1.35 1.65	V
Maximum Input Leakage Current, Address or Inhibit Inputs	V_{IN} = 6.0 or GND	I_{IN}	0 V to 6.0 V	±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current (per Package)	Address, Inhibit and V_{IS} = V_{CC} or GND	I_{CC}	6.0	4.0	40	80	μA

DC ELECTRICAL CHARACTERISTICS − Analog Section

Parameter	Test Conditions	Symbol	V_{CC} V	V_{EE} V	Guaranteed Limit			Unit
					−55 to 25°C	≤ 85°C	≤ 125°C	
Maximum “ON” Resistance (Note 7)	V_{IN} = V_{IL} or V_{IH} V_{IS} = (V_{EE} to V_{CC}) $\|I_S\|$ = 10 mA (Figures 4 thru 9)	R_{ON}	3.0 4.5 3.0	0 0 −3.0	86 37 26	108 46 33	120 55 37	Ω
Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package	V_{IN} = V_{IL} or V_{IH}, V_{IS}= 2.0 V V_{IS} = ½ (V_{CC} − V_{EE}), V_{IS}= 3.0 V $\|I_S\|$ = 10 mA, V_{IS}= 2.0 V	ΔR_{ON}	3.0 4.5 3.0	0 0 −3.0	15 13 10	20 18 15	20 18 15	Ω
ON Resistance Flatness	$\|I_S\|$ = 10 mA V_{COM} = 1, 2, 3.5 V V_{COM} = 2, 0, 2 V	Rflat(ON)	4.5 3.0	 3.0	4 2	4 2	5 3	Ω
Maximum Off−Channel Leakage Current	Switch Off V_{IN} = V_{IL} or V_{IH} V_{IO} = V_{CC} −1.0 V or V_{EE} +1.0 V (Figure 17)	$I_{NC(OFF)}$ $I_{NO(OFF)}$	6.0 3.0	0 −3.0	0.1 0.1	5.0 5.0	100 100	nA
Maximum On−Channel Leakage Current, Channel− to−Channel	Switch On V_{IO} = V_{CC} −1.0 V or V_{EE} +1.0 V (Figure 17)	$I_{COM(ON)}$	6.0 3.0	0 −3.0	0.1 0.1	5.0 5.0	100 100	nA

7. At supply voltage (V_{CC}) approaching 2.5 V the analog switch on−resistance becomes extremely non−linear. Therefore, for low voltage operation it is recommended that these devices only be used to control digital signals.

AC CHARACTERISTICS (Input $t_r = t_f = 3$ ns)

Parameter	Test Conditions	Symbol	V_{CC} V	V_{EE} V	Guaranteed Limit				Unit
					−55 to 25°C				
					Min	Typ*	≤ 85°C	≤ 125°C	
Minimum Break−Before−Make Time	$V_{IN} = V_{IL}$ or V_{IH} $V_{IS} = V_{CC}$ R_L = 300 Ω, C_L = 35 pF (Figure 19)	t_{BBM}	3.0 4.5 3.0	0.0 0.0 −3.0	1.0 1.0 1.0	6.5 5.0 3.5	− − −	− − −	ns

*Typical Characteristics are at 25°C.

AC CHARACTERISTICS (C_L = 35 pF, Input $t_r = t_f = 3$ ns)

Parameter	Symbol	V_{CC} V	V_{EE} V	Guaranteed Limit							Unit
				−55 to 25°C			≤ 85°C		≤ 125°C		
				Min	Typ	Max	Min	Max	Min	Max	
Transition Time (Address Selection Time) (Figure 18)	t_{TRANS}	2.5 3.0 4.5 3.0	0 0 0 −3.0		22 20 16 16	40 28 23 23		45 30 25 25		50 35 30 28	ns
Turn−on Time (Figures 14, 15, 20, and 21) Inhibit to N_O or N_C	t_{ON}	2.5 3.0 4.5 3.0	0 0 0 −3.0		22 18 16 16	40 28 23 23		45 30 25 25		50 35 30 28	ns
Turn−off Time (Figures 14, 15, 20, and 21) Inhibit to N_O or N_C	t_{OFF}	2.5 3.0 4.5 3.0	0 0 0 −3.0		22 18 16 16	40 28 23 23		45 30 25 25		50 35 30 28	ns
				Typical @ 25°C, V_{CC} = 5.0 V							
Maximum Input Capacitance, Select Inputs	C_{IN}			8							pF
Analog I/O	C_{NO} or C_{NC}			10							
Common I/O	C_{COM}			10							
Feedthrough	$C_{(ON)}$			1.0							

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Parameter	Condition	Symbol	V_{CC} V	V_{EE} V	Typ	Unit
					25°C	
Maximum On−Channel Bandwidth or Minimum Frequency Response	V_{IS} = ½ (V_{CC} − V_{EE}) Source Amplitude = 0 dBm (Figures 10 and 22)	BW	3.0 4.5 6.0 3.0	0.0 0.0 0.0 −3.0	80 90 95 95	MHz
Off−Channel Feedthrough Isolation	f =100 kHz; V_{IS} = ½ (V_{CC} − V_{EE}) Source = 0 dBm (Figures 12 and 22)	V_{ISO}	3.0 4.5 6.0 3.0	0.0 0.0 0.0 −3.0	−93 −93 −93 −93	dB
Maximum Feedthrough On Loss	V_{IS} = ½ (V_{CC} − V_{EE}) Source = 0 dBm (Figures 10 and 22)	V_{ONL}	3.0 4.5 6.0 3.0	0.0 0.0 0.0 −3.0	−2 −2 −2 −2	dB
Charge Injection	V_{IN} = V_{CC} to V_{EE}, f_{IS} = 1 kHz, $t_r = t_f$ = 3 ns R_{IS} = 0 Ω, C_L= 1000 pF, Q = C_L * ΔV_{OUT} (Figures 16 and 23)	Q	5.0 3.0	0.0 −3.0	9.0 12	pC
Total Harmonic Distortion THD + Noise	f_{IS} = 1 MHz, R_L = 10 KΩ, C_L = 50 pF, V_{IS} = 5.0 V_{PP} sine wave V_{IS} = 6.0 V_{PP} sine wave (Figure 13)	THD	6.0 3.0	0.0 −3.0	0.10 0.05	%

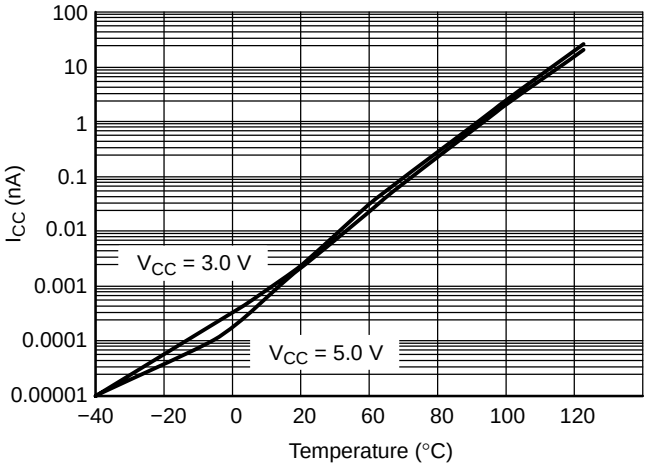


Figure 3. I_{CC} versus Temp, V_{CC} = 3 V and 5 V

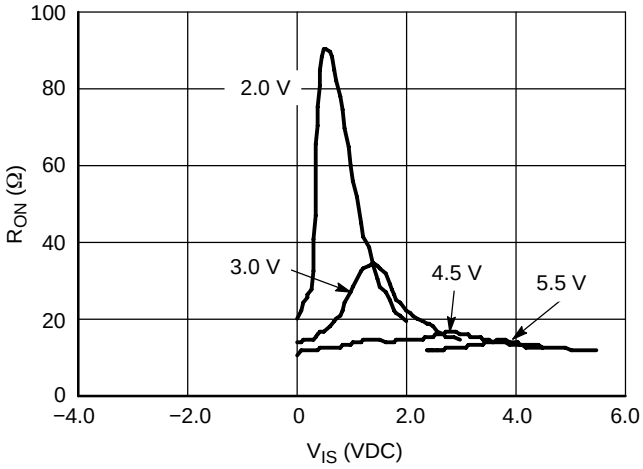


Figure 4. R_{ON} versus V_{CC}, Temp = 25°C

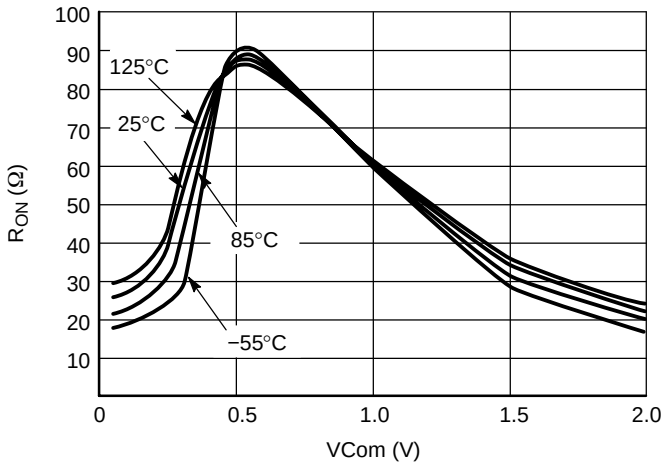


Figure 5. Typical On Resistance
V_{CC} = 2.0 V, V_{EE} = 0 V

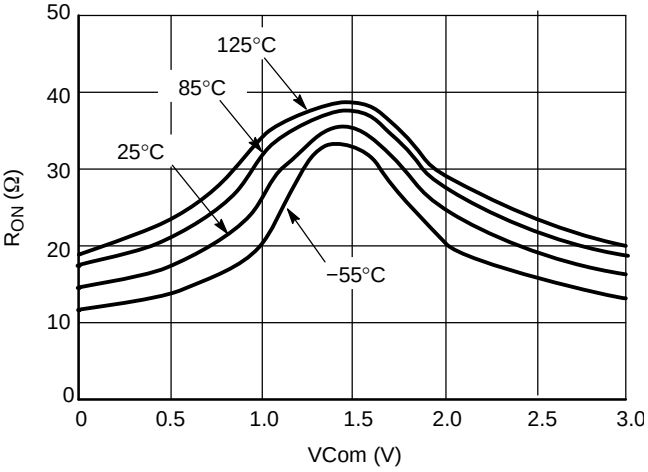


Figure 6. Typical On Resistance
V_{CC} = 3.0 V, V_{EE} = 0 V

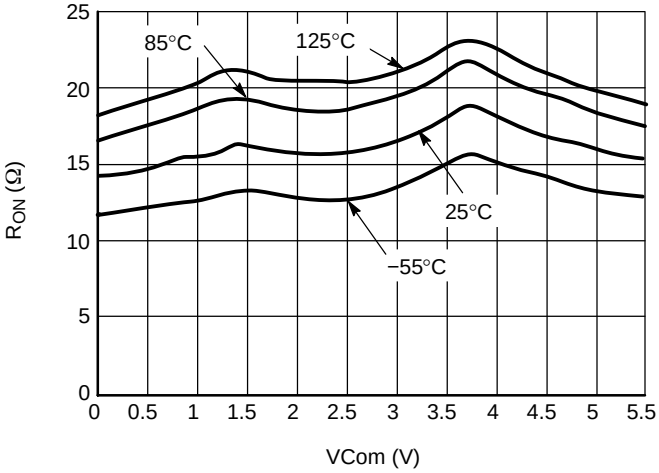


Figure 7. Typical On Resistance
V_{CC} = 4.5 V, V_{EE} = 0 V

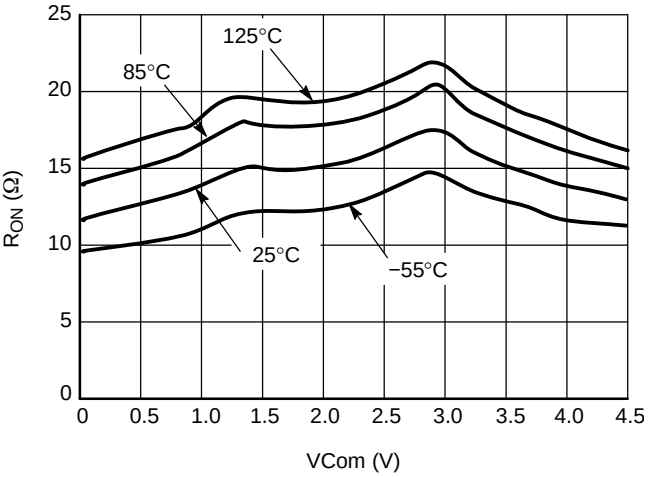


Figure 8. Typical On Resistance
V_{CC} = 5.5 V, V_{EE} = 0 V

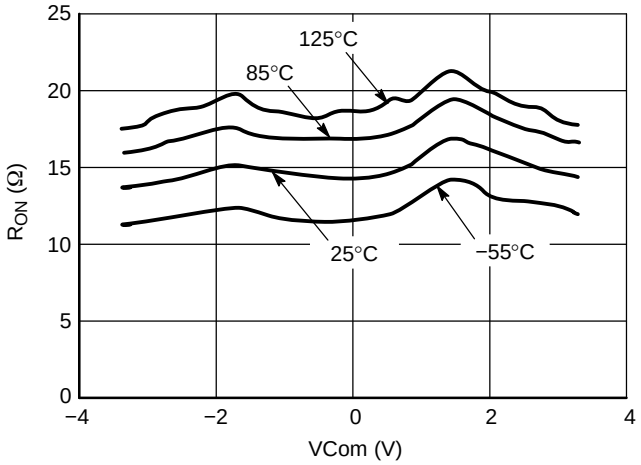


Figure 9. Typical On Resistance
V_{CC} = 3.3 V, V_{EE} = −3.3 V

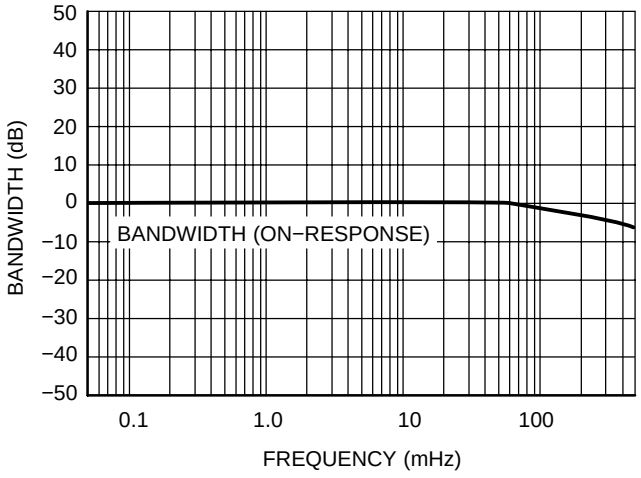


Figure 10. Bandwidth, V_{CC} = 5.0 V

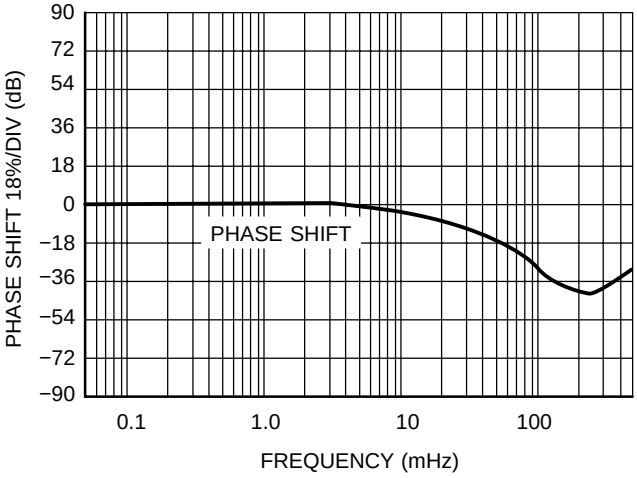


Figure 11. Phase Shift, V_{CC} = 5.0 V

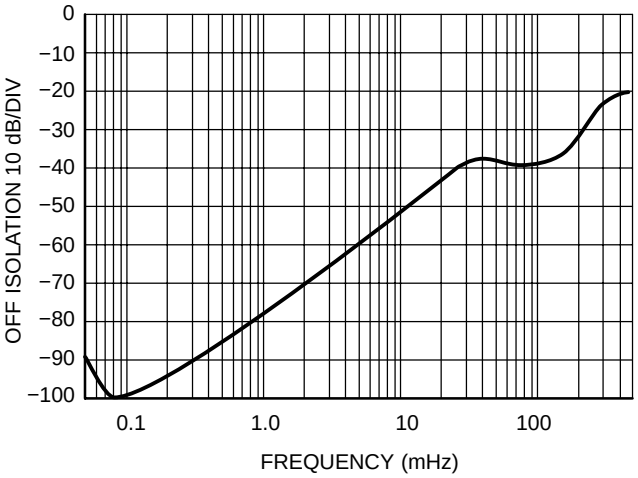


Figure 12. Off Isolation, V_{CC} = 5.0 V

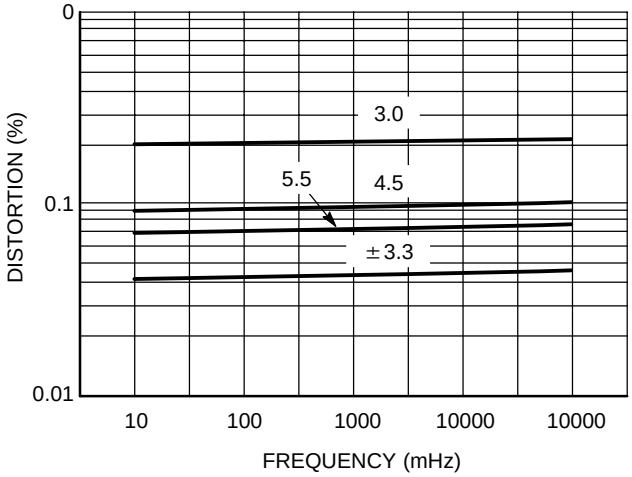


Figure 13. Total Harmonic Distortion

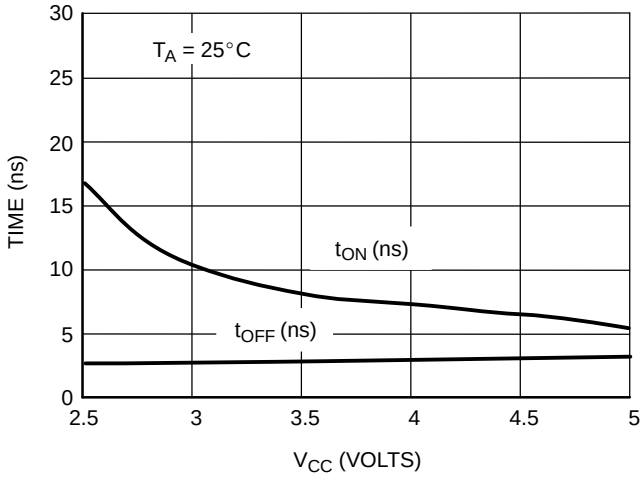


Figure 14. t_{ON} and t_{OFF} versus V_{CC}

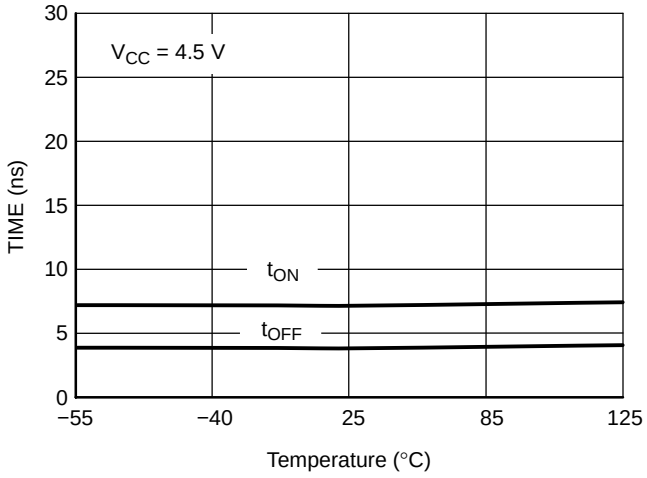


Figure 15. t_{ON} and t_{OFF} versus Temp

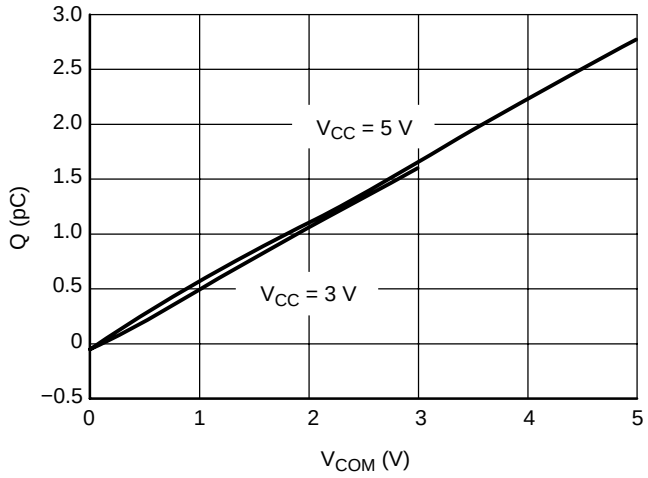


Figure 16. Charge Injection versus COM Voltage

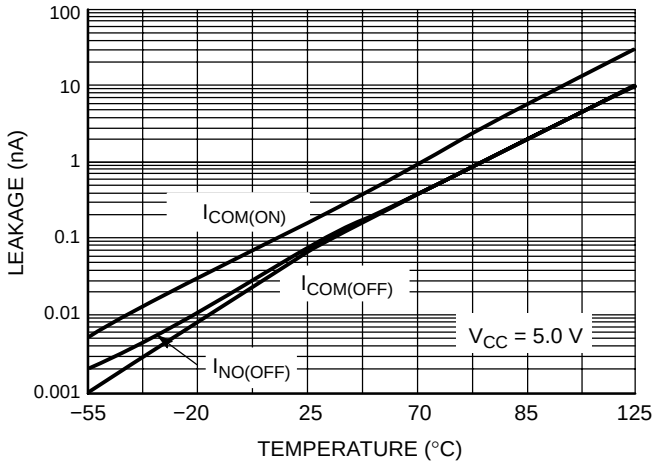
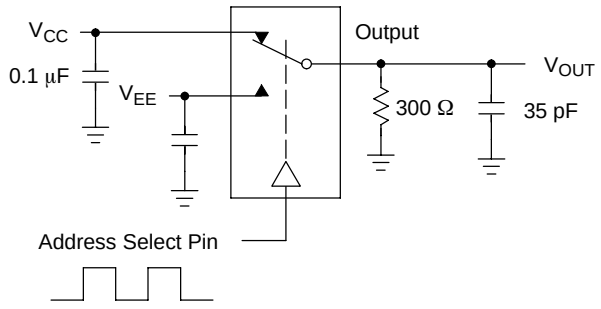


Figure 17. Switch Leakage versus Temperature



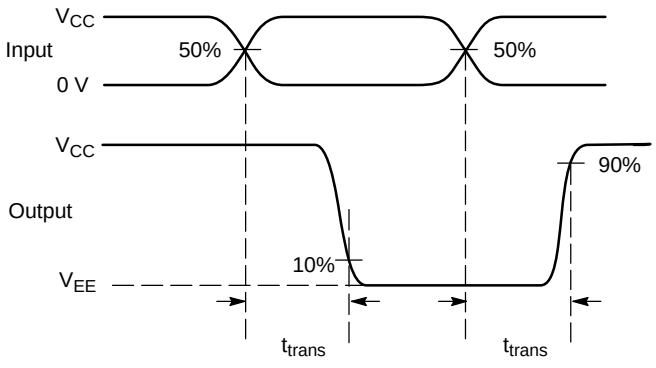


Figure 18. Channel Selection Propagation Delay

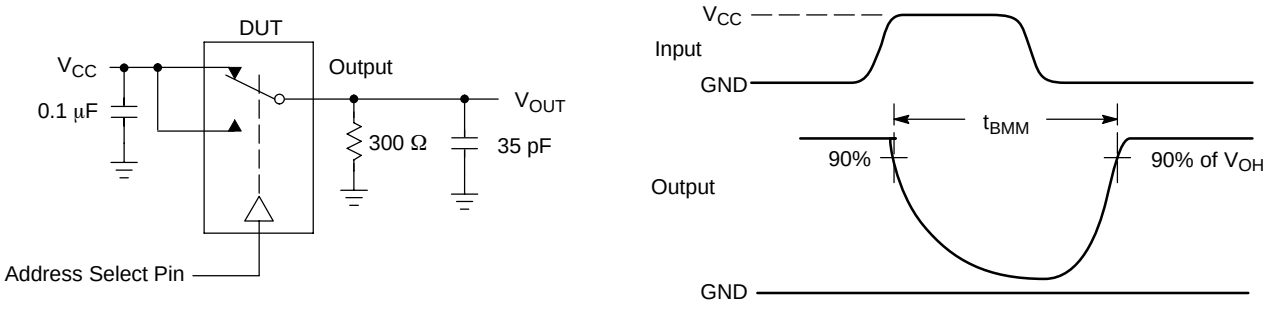


Figure 19. t_{BBM} (Time Break−Before−Make)

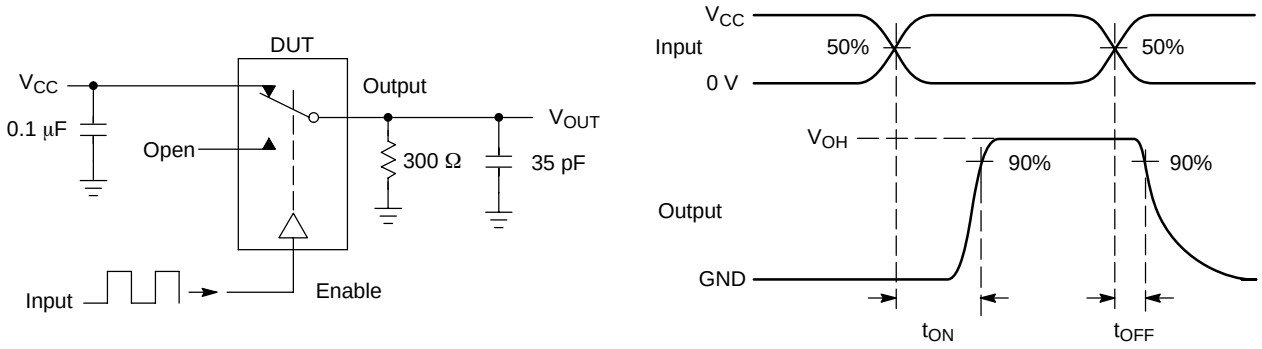


Figure 20. t_{ON}/t_{OFF}

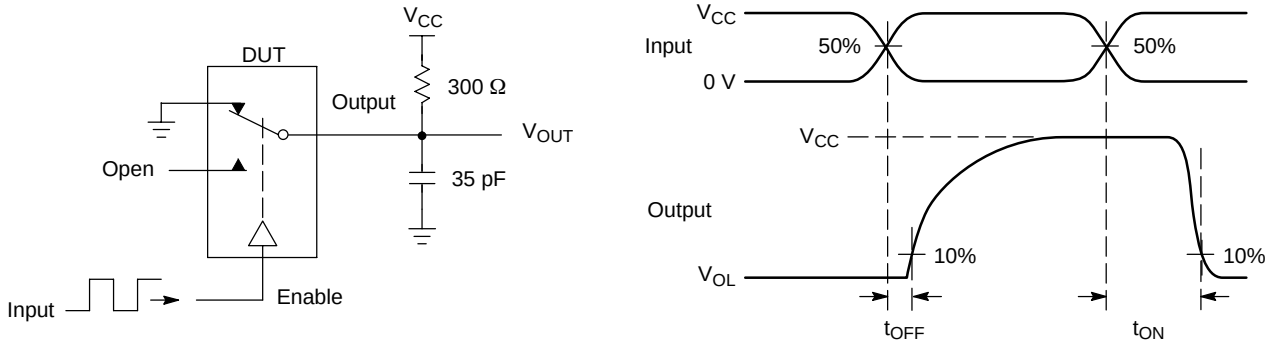
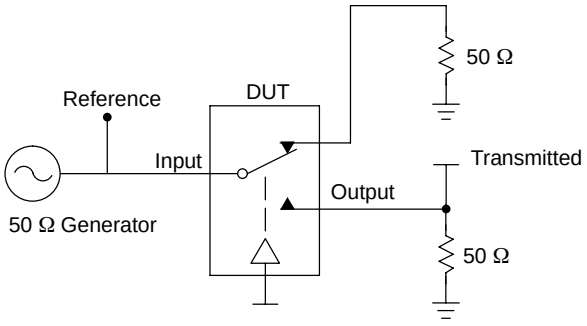


Figure 21. t_{ON}/t_{OFF}



Channel switch Address and Inhibit/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO}, Bandwidth and V_{ONL} are independent of the input signal direction.

V_{ISO} = Off Channel Isolation = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz

V_{ONL} = On Channel Loss = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz to 50 MHz

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

Figure 22. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/V_{ONL}

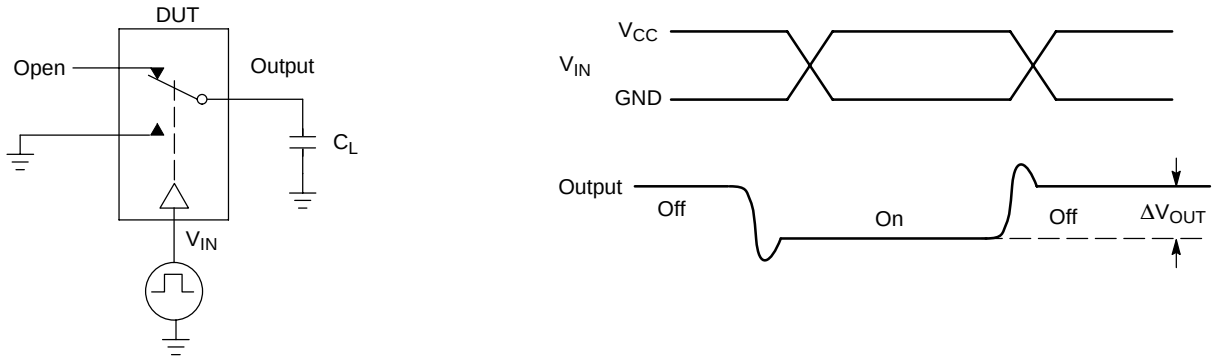


Figure 23. Charge Injection: (Q)

TYPICAL OPERATION

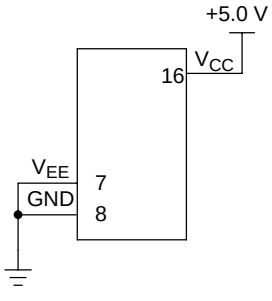


Figure 24. 5.0 Volts Single Supply V_{CC} = 5.0 V, V_{EE} = 0

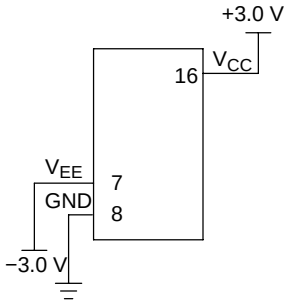
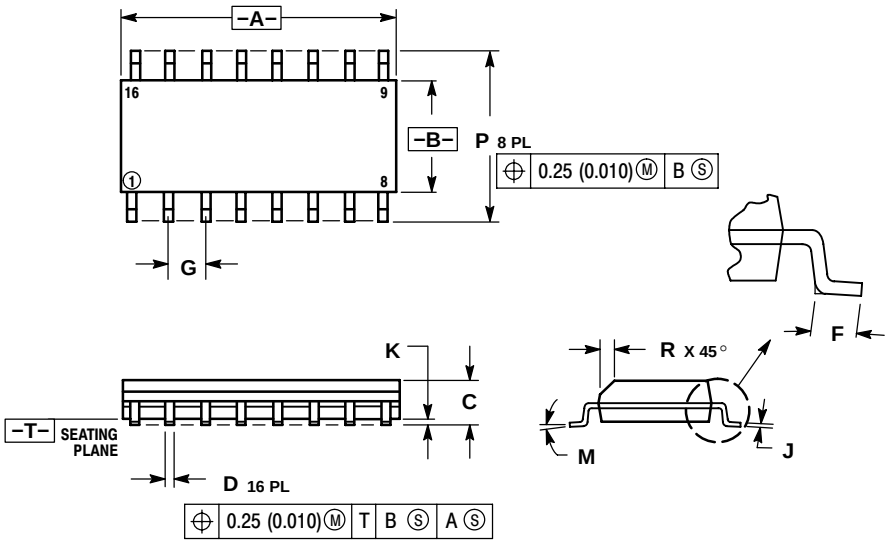


Figure 25. Dual Supply V_{CC} = 3.0 V, V_{EE} = −3.0 V

PACKAGE DIMENSIONS

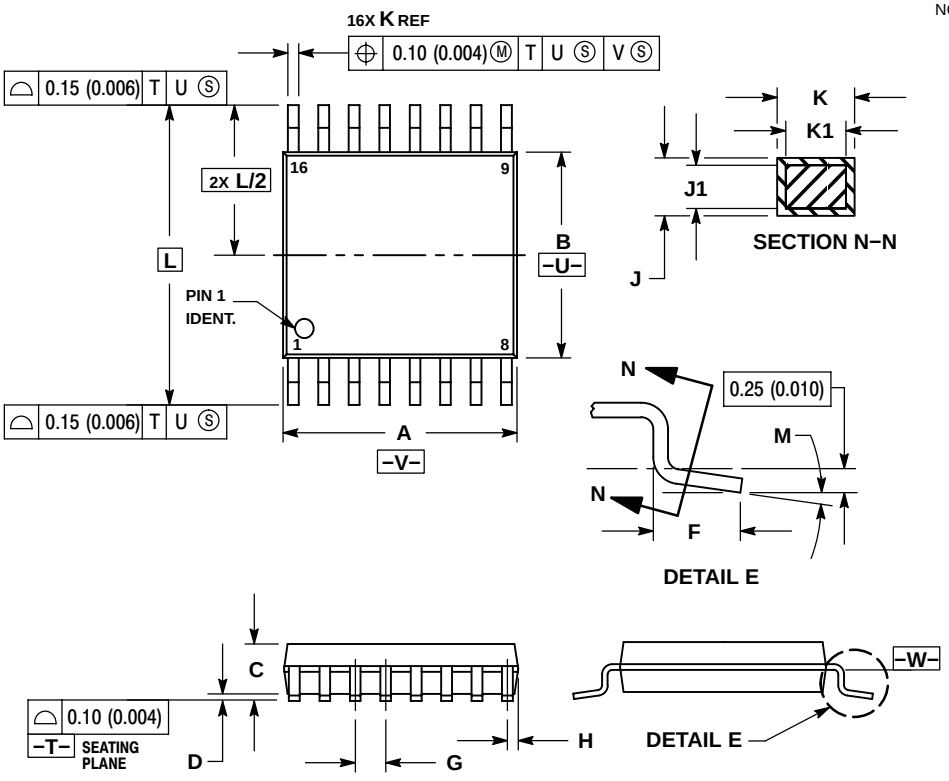
SOIC−16
D SUFFIX
CASE 751B−05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

TSSOP−16
CASE 948F−01
ISSUE A

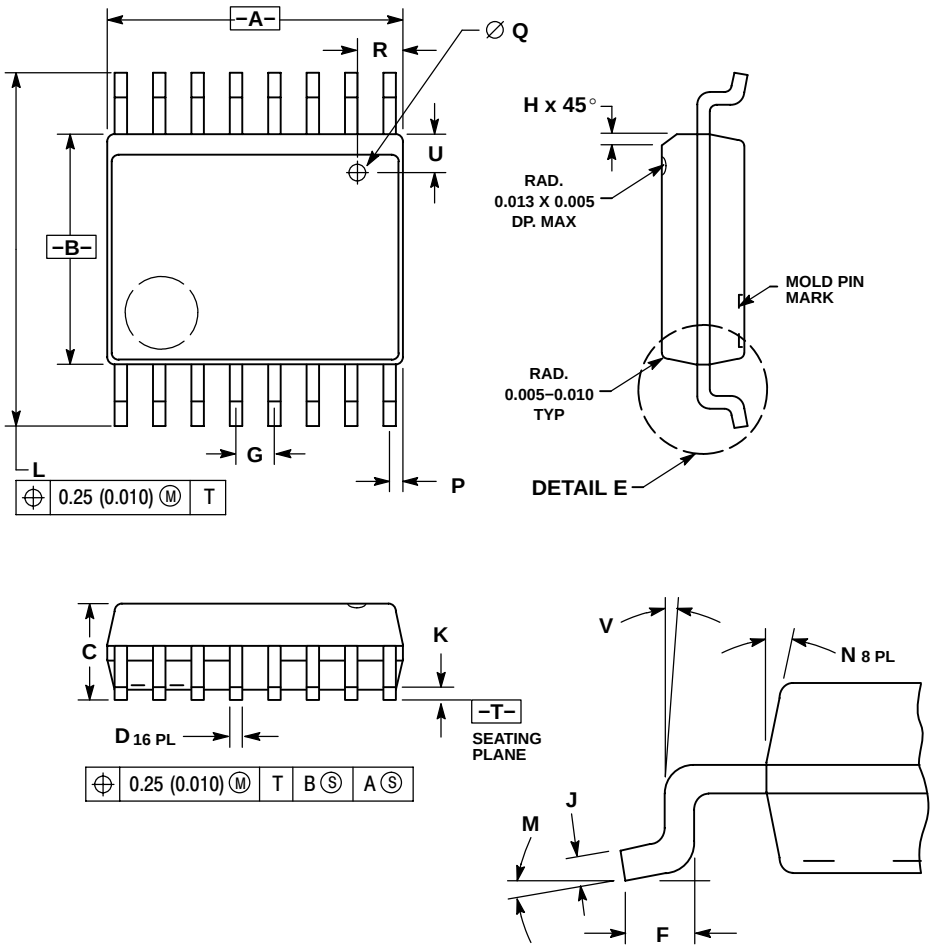


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

PACKAGE DIMENSIONS

QSOP−16
QS SUFFIX
CASE 492−01
ISSUE O



DETAIL E

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. THE BOTTOM PACKAGE SHALL BE BIGGER THAN THE TOP PACKAGE BY 4 MILS (NOTE: LEAD SIDE ONLY). BOTTOM PACKAGE DIMENSION SHALL FOLLOW THE DIMENSION STATED IN THIS DRAWING.
4. PLASTIC DIMENSIONS DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 6 MILS PER SIDE.
5. BOTTOM EJECTOR PIN WILL INCLUDE THE COUNTRY OF ORIGIN (COO) AND MOLD CAVITY I.D.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.189	0.196	4.80	4.98
B	0.150	0.157	3.81	3.99
C	0.061	0.068	1.55	1.73
D	0.008	0.012	0.20	0.31
F	0.016	0.035	0.41	0.89
G	0.025 BSC		0.64 BSC	
H	0.008	0.018	0.20	0.46
J	0.0098	0.0075	0.249	0.191
K	0.004	0.010	0.10	0.25
L	0.230	0.244	5.84	6.20
M	0°	8°	0°	8°
N	0°	7°	0°	7°
P	0.007	0.011	0.18	0.28
Q	0.020 DIA		0.51 DIA	
R	0.025	0.035	0.64	0.89
U	0.025	0.035	0.64	0.89
V	0°	8°	0°	8°

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