NTF3055L175

Preferred Device

Power MOSFET
2.0 A, 60 V, Logic Level
N−Channel SOT−223

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

- Pb−Free Packages are Available

Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	60	Vdc
Drain−to−Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate−to−Source Voltage − Continuous − Non−repetitive ($t_p \le 10$ ms)	V_{GS}	 ± 15 ± 20	 Vdc Vpk
Drain Current − Continuous @ T_A = 25°C − Continuous @ T_A = 100°C − Single Pulse ($t_p \le 10$ μs)	 I_D I_D I_{DM}	 2.0 1.2 6.0	 Adc Apk
Total Power Dissipation @ T_A = 25°C (Note 1) Total Power Dissipation @ T_A = 25°C (Note 2) Derate above 25°C	P_D	2.1 1.3 0.014	W W W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 175	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, $I_{L(pk)}$ = 3.6 A, L = 10 mH, V_{DS} = 60 Vdc)	E_{AS}	65	mJ
Thermal Resistance − Junction−to−Ambient (Note 1) − Junction−to−Ambient (Note 2)	 $R_{\theta JA}$ $R_{\theta JA}$	 72.3 114	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

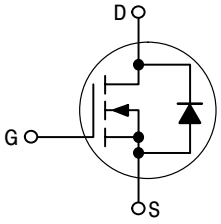
1. When surface mounted to an FR4 board using 1″ pad size, 1 oz. (Cu. Area 0.995 in^2).
2. When surface mounted to an FR4 board using minimum recommended pad size, 2−2.4 oz. (Cu. Area 0.272 in^2).

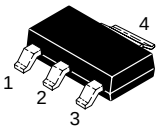
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2.0 A, 60 V
$R_{DS(on)}$ = 175 mΩ

N−Channel

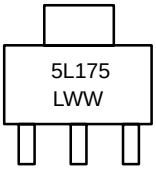




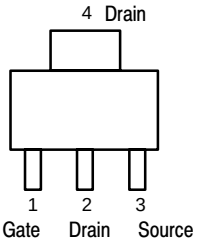
SOT−223
CASE 318E
STYLE 3

MARKING DIAGRAM

5L175 = Device Code
L = Location Code
WW = Work Week



PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (Note 3) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 60 −	 72.8 74.4	 − −	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		I_{DSS}	 − −	 − −	 1.0 10	μAdc
Gate−Body Leakage Current	(V_{GS} = ± 15 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	−	−	± 100	nAdc
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage (Note 3) (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0 −	 1.7 4.2	 2.0 −	Vdc mV/°C
Static Drain−to−Source On−Resistance (Note 3) (V_{GS} = 5.0 Vdc, I_D = 1.0 Adc)		$R_{DS(on)}$	 −	 155	 175	mΩ
Static Drain−to−Source On−Resistance (Note 3) (V_{GS} = 5.0 Vdc, I_D = 2.0 Adc) (V_{GS} = 5.0 Vdc, I_D = 1.0 Adc, T_J = 150°C)		$V_{DS(on)}$	 −	 0.32 0.57	 0.42 −	Vdc
Forward Transconductance (Note 3)	(V_{DS} = 8.0 Vdc, I_D = 1.5 Adc)	g_{fs}	−	3.2	−	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	−	194	270	pF
Output Capacitance		C_{oss}	−	70	100	
Transfer Capacitance		C_{rss}	−	29	40	
SWITCHING CHARACTERISTICS (Note 4)						
Turn−On Delay Time	(V_{DD} = 30 Vdc, I_D = 2.0 Adc, V_{GS} = 5.0 Vdc, R_G = 9.1 Ω) (Note 3)	$t_{d(on)}$	−	10.2	20	ns
Rise Time		t_r	−	21	40	
Turn−Off Delay Time		$t_{d(off)}$	−	14.3	30	
Fall Time		t_f	−	15.3	30	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 2.0 Adc, V_{GS} = 5.0 Vdc) (Note 3)	Q_T	−	5.1	10	nC
		Q_1	−	1.4	−	
		Q_2	−	2.5	−	
SOURCE−DRAIN DIODE CHARACTERISTICS						
Forward On−Voltage	(I_S = 2.0 Adc, V_{GS} = 0 Vdc) (I_S = 2.0 Adc, V_{GS} = 0 Vdc, T_J = 150°C) (Note 3)	V_{SD}	 − −	 0.84 0.68	 1.0 −	Vdc
Reverse Recovery Time	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (Note 3)	t_{rr}	−	28.3	−	ns
		t_a	−	15.6	−	
		t_b	−	12.7	−	
Reverse Recovery Stored Charge		Q_{RR}	−	0.027	−	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
4. Switching characteristics are independent of operating junction temperatures.

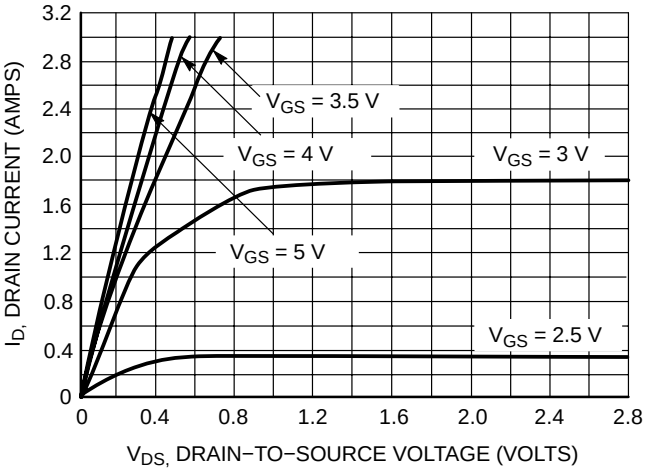


Figure 1. On−Region Characteristics

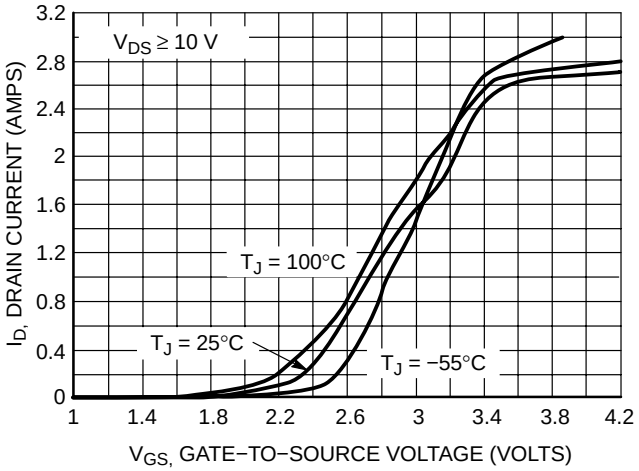


Figure 2. Transfer Characteristics

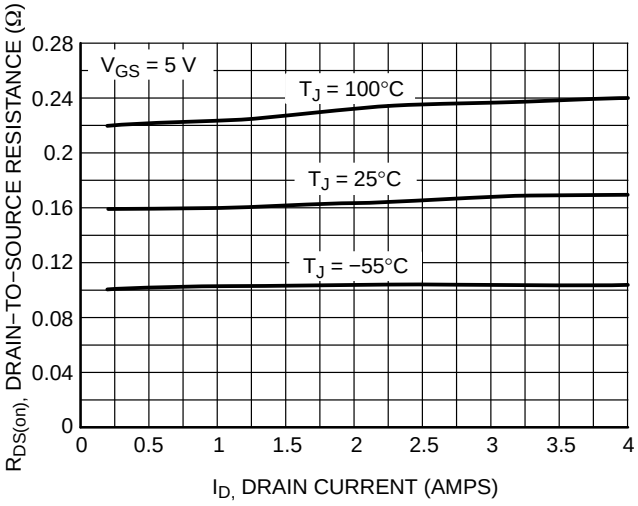


Figure 3. On−Resistance versus Gate−to−Source Voltage

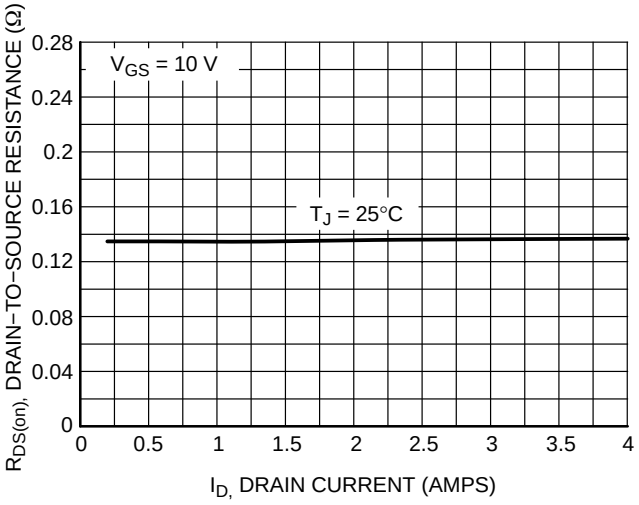


Figure 4. On−Resistance versus Drain Current and Gate Voltage

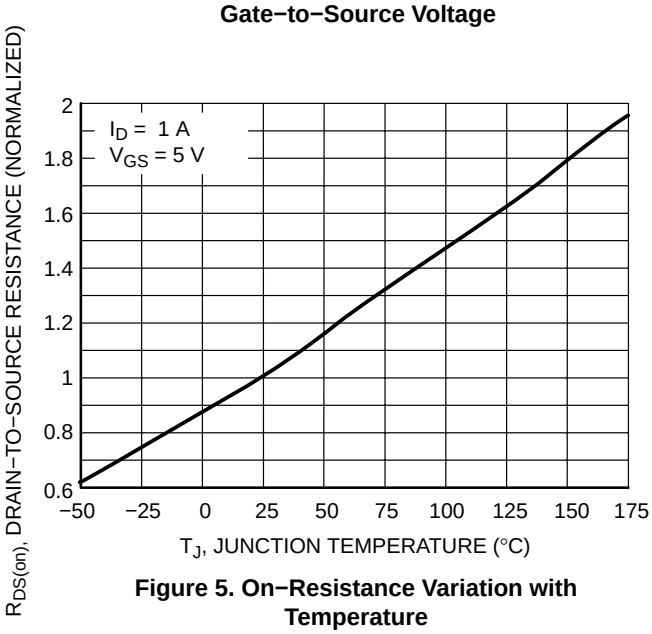


Figure 5. On−Resistance Variation with Temperature

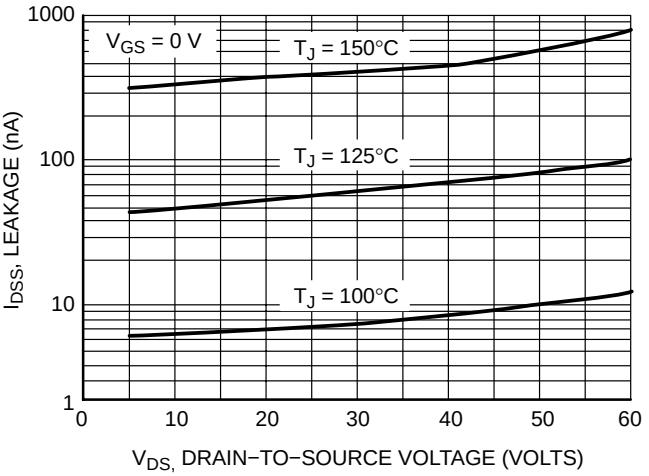


Figure 6. Drain−to−Source Leakage Current versus Voltage

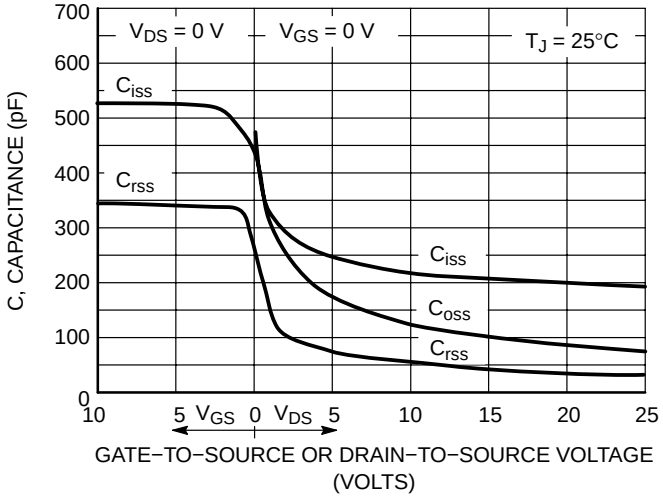


Figure 7. Capacitance Variation

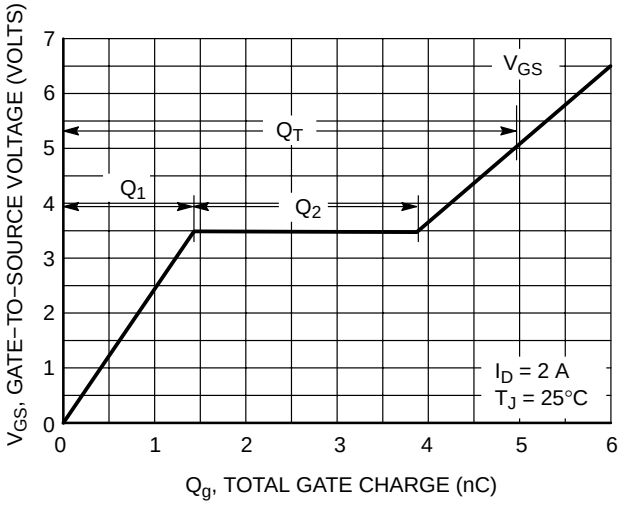


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

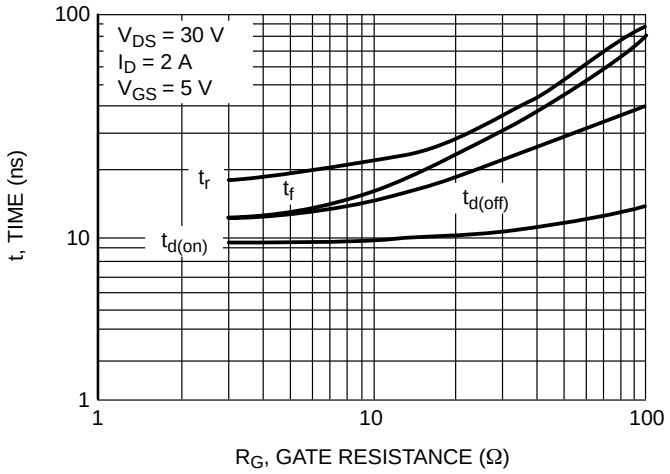


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

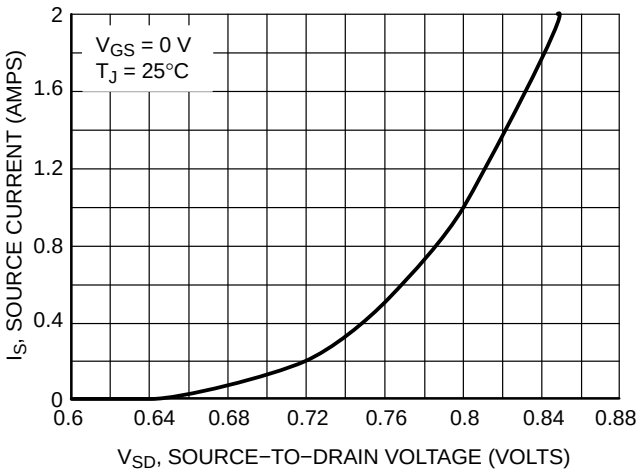


Figure 10. Diode Forward Voltage versus Current

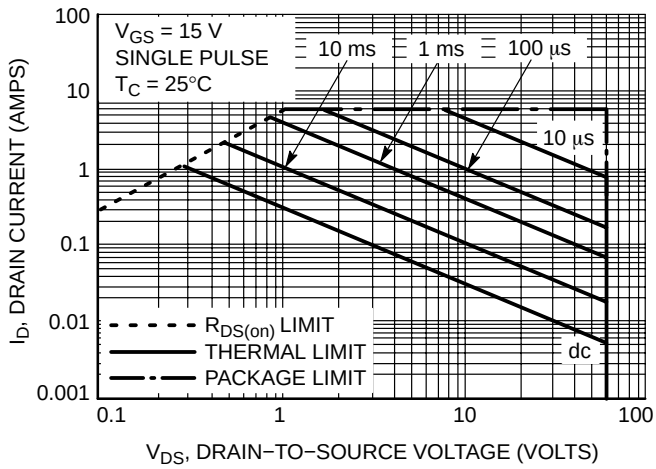


Figure 11. Maximum Rated Forward Biased Safe Operating Area

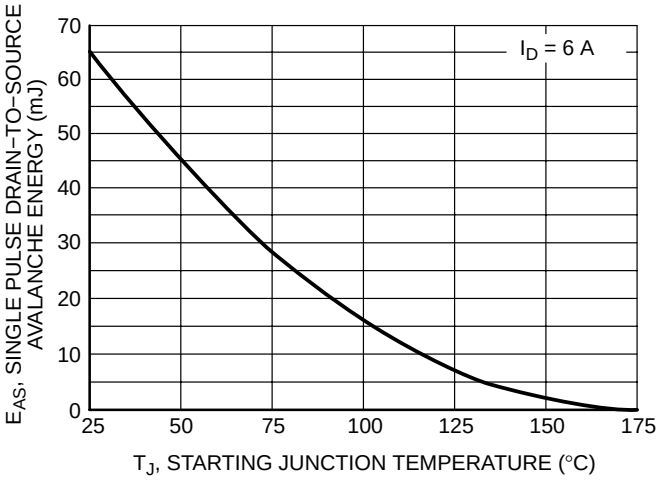


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

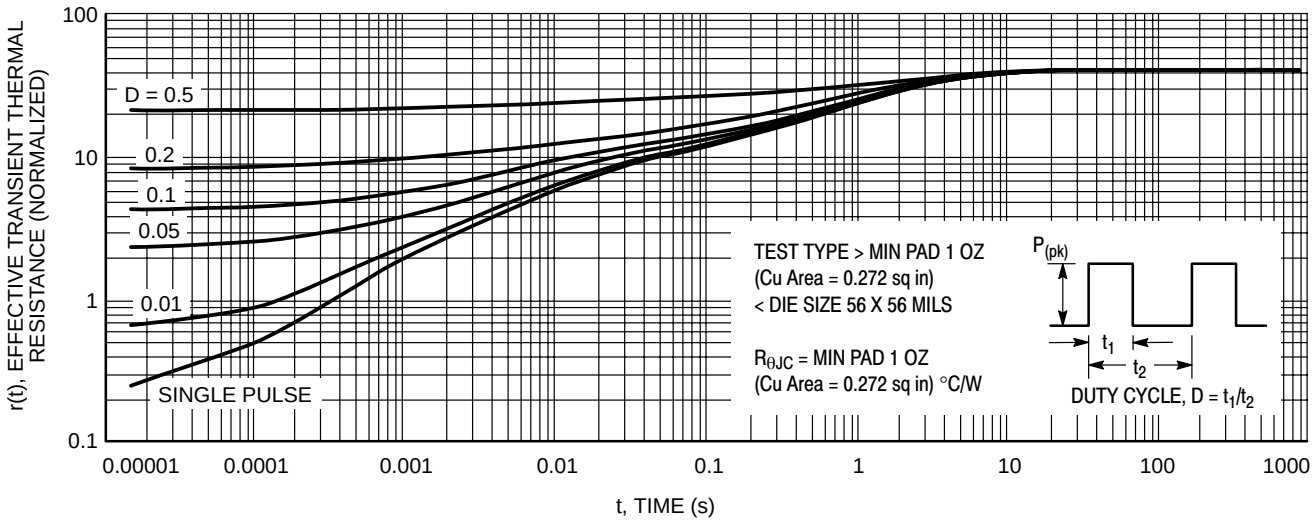


Figure 13. Thermal Response

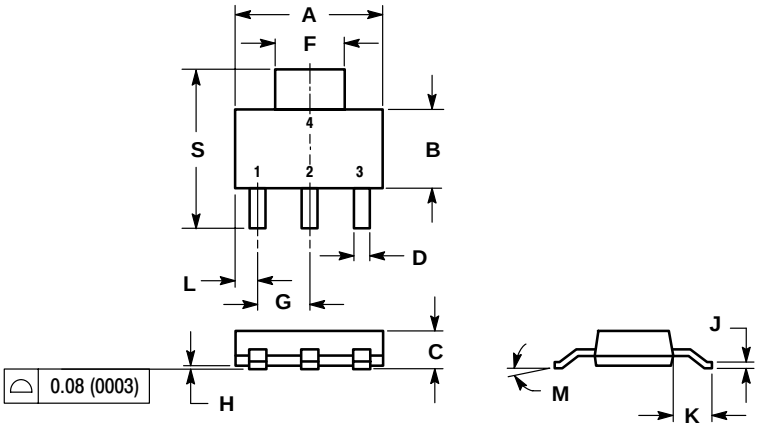
ORDERING INFORMATION

Device	Package	Shipping†
NTF3055L175T1	SOT−223 (TO−261)	1000 / Tape & Reel
NTF3055L175T1G	SOT−223 (TO−261) (Pb−Free)	1000 / Tape & Reel
NTF3055L175T3	SOT−223 (TO−261)	4000 / Tape & Reel
NTF3055L175T3G	SOT−223 (TO−261) (Pb−Free)	4000 / Tape & Reel
NTF3055L175T3LF	SOT−223 (TO−261)	4000 / Tape & Reel
NTF3055L175T3LFG	SOT−223 (TO−261) (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

SOT−223 (TO−261)
CASE 318E−04
ISSUE K

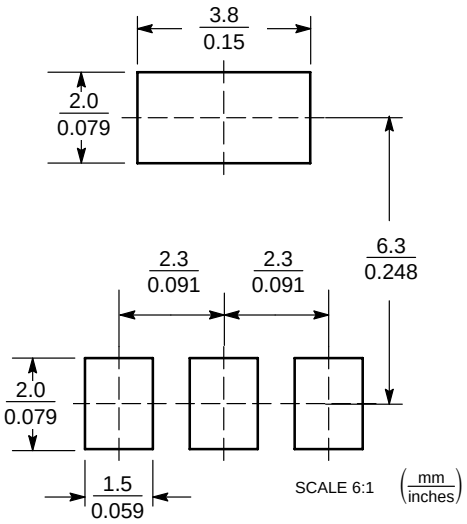


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0 °	10 °	0 °	10 °
S	0.264	0.287	6.70	7.30

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



SOT−223

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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