NVT2008; NVT2010

Bidirectional voltage-level translator for open-drain and push-pull applications

Rev. 3.1 — 20 September 2024 Product data sheet

1 General description

The NVT2008/NVT2010 are bidirectional voltage level translators operational from 1.0 V to 3.6 V ($V_{ref(A)}$) and 1.8 V to 5.5 V ($V_{ref(B)}$), which allow bidirectional voltage translations between 1.0 V and 5 V without the need for a direction pin in open-drain or push-pull applications. Bit widths of 8-bit to 10-bit are offered for level translation application with transmission speeds < 33 MHz for an open-drain system with a 50 pF capacitance and a pull-up of 197 Ω.

When the An or Bn port is LOW, the clamp is in the ON-state and a low resistance connection exists between the An and Bn ports. The low ON-state resistance (R_{on}) of the switch allows connections to be made with minimal propagation delay. Assuming the higher voltage is on the Bn port when the Bn port is HIGH, the voltage on the An port is limited to the voltage set by VREFA. When the An port is HIGH, the Bn port is pulled to the drain pull-up supply voltage ($V_{pu(D)}$) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control.

When EN is HIGH, the translator switch is on, and the An I/O are connected to the Bn I/O, respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports. The EN input circuit is designed to be supplied by $V_{ref(B)}$. To ensure the high-impedance state during power-up or power-down, EN must be LOW.

All channels have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower voltage devices, and at the same time protects less ESD-resistant devices.

2 Features and benefits

- Provides bidirectional voltage translation with no direction pin
- Less than 1.5 ns maximum propagation delay
- Allows voltage level translation between:
  - 1.0 V $V_{ref(A)}$ and 1.8 V, 2.5 V, 3.3 V or 5 V $V_{ref(B)}$
  - 1.2 V $V_{ref(A)}$ and 1.8 V, 2.5 V, 3.3 V or 5 V $V_{ref(B)}$
  - 1.8 V $V_{ref(A)}$ and 3.3 V or 5 V $V_{ref(B)}$
  - 2.5 V $V_{ref(A)}$ and 5 V $V_{ref(B)}$
  - 3.3 V $V_{ref(A)}$ and 5 V $V_{ref(B)}$
- Low 3.5 Ω ON-state connection between input and output ports provides less signal distortion
- 5 V tolerant I/O ports to support mixed-mode signal operation
- High-impedance An and Bn pins for EN = LOW
- Lock-up free operation
- Flow through pinout for ease of printed-circuit board trace routing
- ESD protection exceeds 4 kV HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Packages offered: TSSOP20, DHVQFN20, TSSOP24, DHVQFN24, HVQFN24

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3 Ordering information

Table 1. Ordering information

Type number	Topside mark	Number of bits	Package		
			Name	Description	Version
NVT2008BQ[1]	NVT2008	8	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1
NVT2008PW[1]	NVT2008	8	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
NVT2010BQ[2]	NVT2010	10	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT815-1
NVT2010BS[2]	N010	10	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-1
NVT2010PW[2]	NVT2010	10	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

[1] GTL2003 = NVT2008.
[2] GTL2010 = NVT2010.

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NVT2008BQ	NVT2008BQZ	DHVQFN20	Reel 7" Q1/T1 *Standard mark SMD	3000	T_{amb} = -40 °C to +85 °C
NVT2008PW	NVT2008PW,118	TSSOP20	Reel 13" Q1/T1 *Standard mark SMD	2500	T_{amb} = -40 °C to +85 °C
NVT2010BQ	NVT2010BQ,118	DHVQFN24	Reel 13" Q1/T1 *Standard mark SMD	3000	T_{amb} = -40 °C to +85 °C
NVT2010BS	NVT2010BS,115	HVQFN24	Reel 7" Q1/T1 *Standard mark SMD	1500	T_{amb} = -40 °C to +85 °C
	NVT2010BS,118	HVQFN24	Reel 13" Q1/T1 *Standard mark SMD	6000	T_{amb} = -40 °C to +85 °C
NVT2010PW	NVT2010PW,118	TSSOP24	Reel 13" Q1/T1 *Standard mark SMD	2500	T_{amb} = -40 °C to +85 °C

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4 Functional diagram

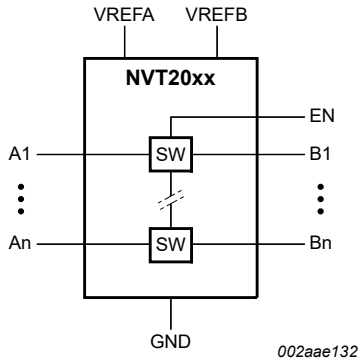


Figure 1. Logic diagram of NVT2008/10 (positive logic)

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5 Pinning information

5.1 Pinning

5.1.1 8-bit in TSSOP20 and DHVQFN20 packages

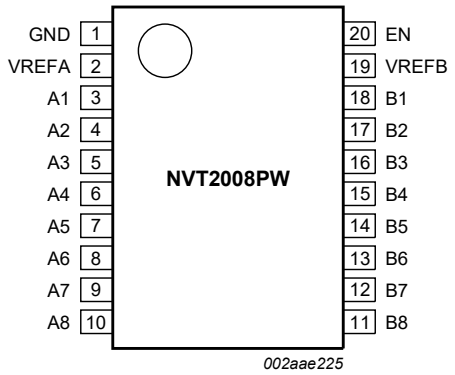


Figure 2. Pin configuration for TSSOP20

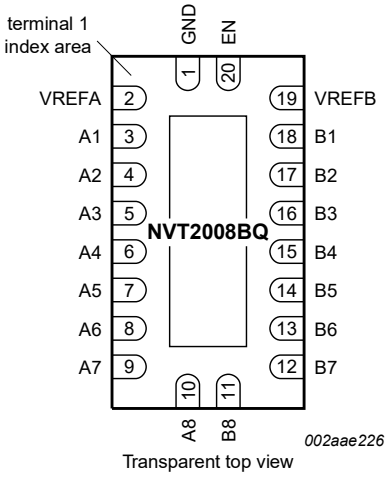


Figure 3. Pin configuration for DHVQFN20

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5.1.2 10-bit in TSSOP24, DHVQFN24 and HVQFN24 packages

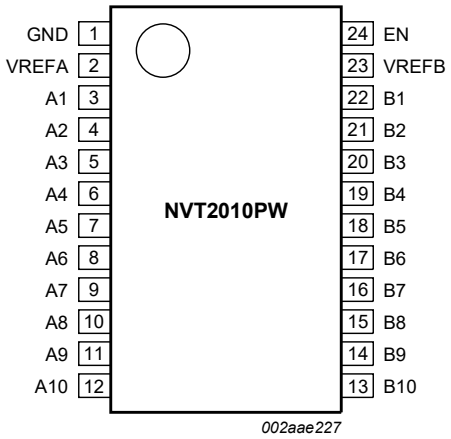
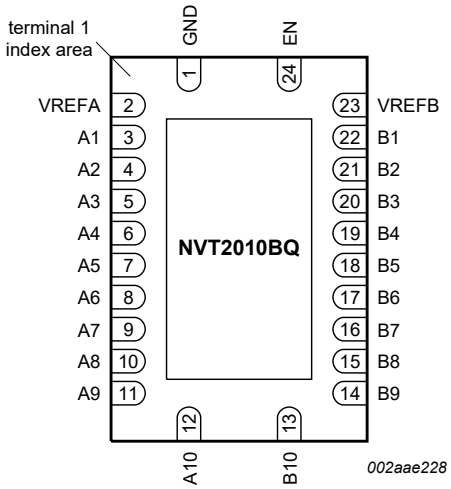
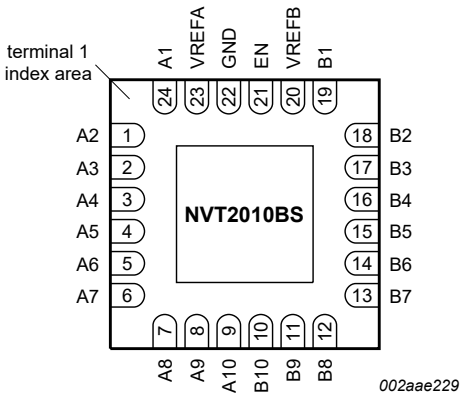


Figure 4. Pin configuration for TSSOP24



Transparent top view

Figure 5. Pin configuration for DHVQFN24



Transparent top view

Figure 6. Pin configuration for HVQFN24

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5.2 Pin description

Table 3. Pin description

Symbol	Pin			Description
	NVT2008BQ, NVT2008PW[1]	NVT2010BQ, NVT2010PW[2]	NVT2010BS[2]	
GND	1	1	22	ground (0 V)
VREFA	2	2	23	low-voltage side reference supply voltage for An
A1	3	3	24	low-voltage side; connect to VREFA through a pull-up resistor
A2	4	4	1	
A3	5	5	2	
A4	6	6	3	
A5	7	7	4	
A6	8	8	5	
A7	9	9	6	
A8	10	10	7	
A9	-	11	8	
A10	-	12	9	
B1	18	22	19	high-voltage side; connect to VREFB through a pull-up resistor
B2	17	21	18	
B3	16	20	17	
B4	15	19	16	
B5	14	18	15	
B6	13	17	14	
B7	12	16	13	
B8	11	15	12	
B9	-	14	11	
B10	-	13	10	
VREFB	19	23	20	high-voltage side reference supply voltage for Bn
EN	20	24	21	switch enable input; connect to VREFB and pull-up through a high resistor

[1] 8-bit NVT2008 available in TSSOP20, DHVQFN20 packages.
[2] 10-bit NVT2010 available in TSSOP24, DHVQFN24, HVQFN24 packages.

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6 Functional description

Refer to Figure 1.

6.1 Function table

Table 4. Function selection (example)

H = HIGH level; L = LOW level.

Input EN[1]	Function
H	An = Bn
L	disconnect

[1] EN is controlled by the $V_{ref(B)}$ logic levels and should be at least 1 V higher than $V_{ref(A)}$ for best translator operation.

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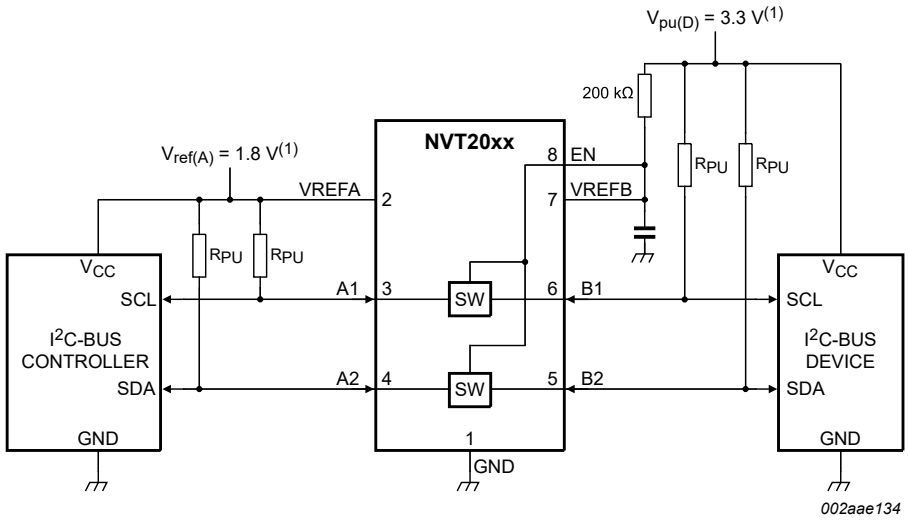
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7 Application design-in information

The NVT2008/10 can be used in level translation applications for interfacing devices or systems operating at different interface voltages with one another. The NVT2008/10 is ideal for use in applications where an open-drain driver is connected to the data I/Os. The NVT2008/10 can also be used in applications where a push-pull driver is connected to the data I/Os.

7.1 Enable and disable

The NVT20xx has an EN input that is used to disable the device by setting EN LOW, which places all I/Os in the high-impedance state.



1. The applied voltages at $V_{ref(A)}$ and $V_{pu(D)}$ should be such that $V_{ref(B)}$ is at least 1 V higher than $V_{ref(A)}$ for best translator operation.

Figure 7. Typical application circuit (switch always enabled)

Table 5. Application operating conditions

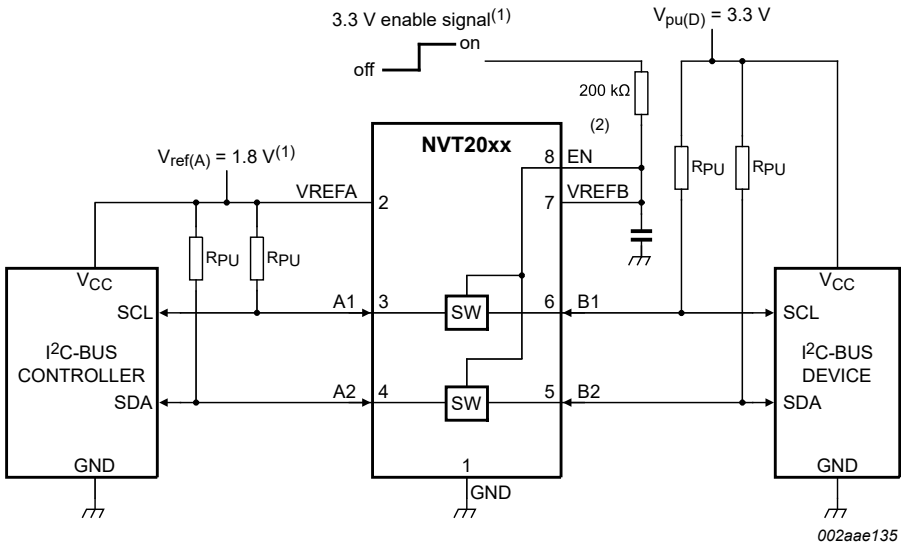
Refer to Figure 7.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{ref(B)}$	reference voltage (B)			$V_{ref(A)}$ + 0.6	2.1	5	V
$V_{I(EN)}$	input voltage on pin EN			$V_{ref(A)}$ + 0.6	2.1	5	V
$V_{ref(A)}$	reference voltage (A)			0	1.5	4.4	V
$I_{sw(pass)}$	pass switch current			-	14	-	mA
I_{ref}	reference current	transistor		-	5	-	µA
T_{amb}	ambient temperature	operating in free-air		-40	-	+85	°C

[1] All typical values are at T_{amb} = 25 °C.

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1. In the Enabled mode, the applied enable voltage $V_{I(EN)}$ and the applied voltage at $V_{ref(A)}$ should be such that $V_{ref(B)}$ is at least 1 V higher than $V_{ref(A)}$ for best translator operation.
2. Note that the enable time and the disable time are essentially controlled by the RC time constant of the capacitor and the 200 kΩ resistor on the EN pin.

Figure 8. Typical application circuit (switch enable control)

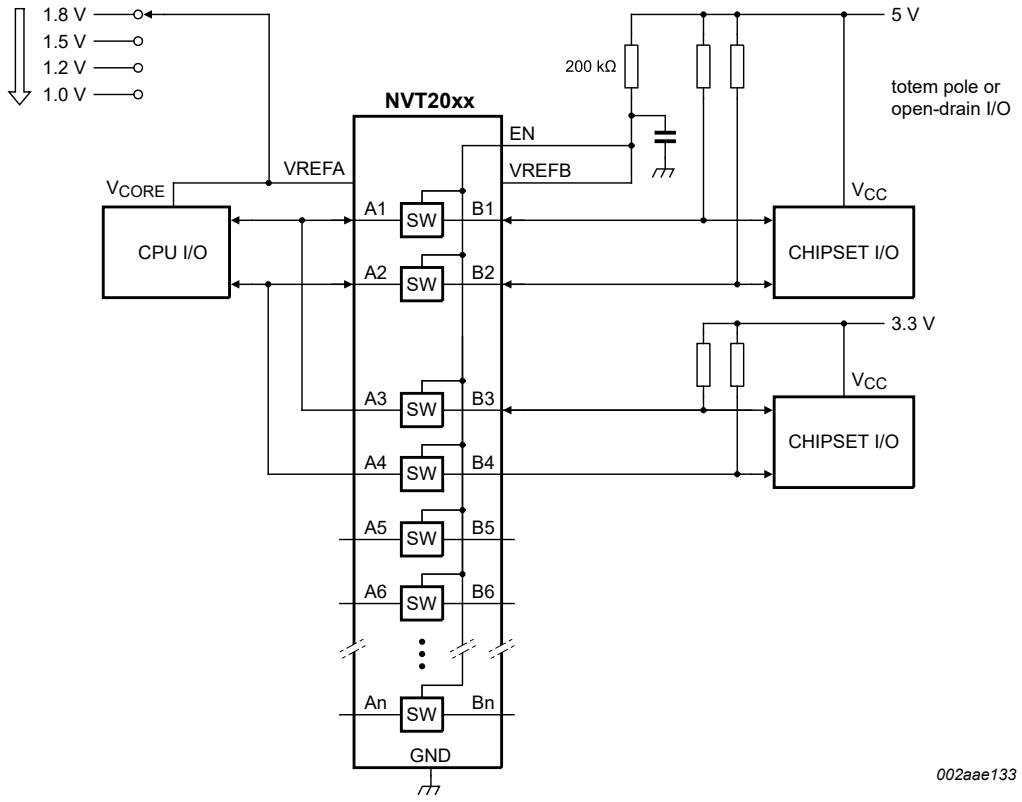


Figure 9. Bidirectional translation to multiple higher voltage levels

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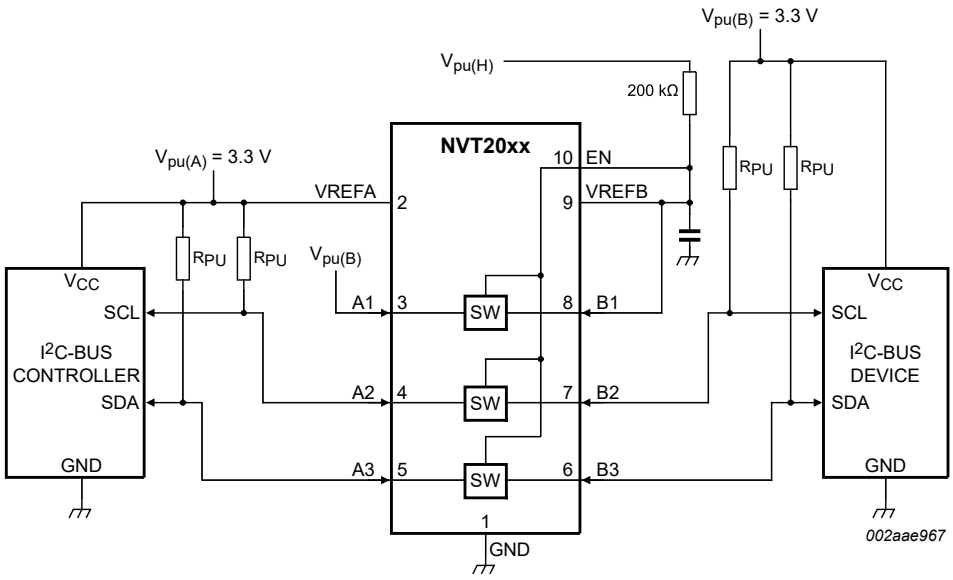
7.2 Bidirectional translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to VREFB and both pins pulled to HIGH side $V_{pu(D)}$ through a pull-up resistor (typically 200 kΩ). This allows VREFB to regulate the EN input. A filter capacitor on VREFB is recommended. The controller output driver can be totem pole or open-drain (pull-up resistors may be required) and the target device output can be totem pole or open-drain (pull-up resistors are required to pull the Bn outputs to $V_{pu(D)}$). However, if either output is totem-pole, data must be unidirectional or the outputs must be 3-stateable and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed.

The reference supply voltage ($V_{ref(A)}$) is connected to the processor core power supply voltage. When VREFB is connected through a 200 kΩ resistor to a 3.3 V to 5.5 V $V_{pu(D)}$ power supply, and $V_{ref(A)}$ is set between 1.0 V and ($V_{pu(D)}$ - 1 V), the output of each An has a maximum output voltage equal to VREFA, and the output of each Bn has a maximum output voltage equal to $V_{pu(D)}$.

7.3 Bidirectional level shifting between two different power domains nominally at the same potential

The less obvious application for the NVT2008/NVT2010 is for level shifting between two different power domains that are nominally at the same potential, such as a 3.3 V system where the line crosses power supply domains that under normal operation would be at 3.3 V, but one could be at 3.0 V and the other at 3.6 V, or one could be experiencing a power failure while the other domain is trying to operate. One of the channel transistors is used as a second reference transistor with its B side connected to a voltage supply that is at least 1 V (and preferably 1.5 V) above the maximum possible for either $V_{pu(A)}$ or $V_{pu(B)}$. Then if either pull-up voltage is at 0 V, the channels are disabled, and otherwise the channels are biased such that they turn OFF at the lower pull-up voltage, and if the two pull-up voltages are equal, the channel is biased such that it just turns OFF at the common pull-up voltage.



The applied enable voltage $V_{pu(H)}$ and the applied voltage at $V_{ref(A)}$ and $V_{ref(B)}$ should be such that $V_{ref(H)}$ is at least 1 V higher than $V_{ref(A)}$ and $V_{ref(B)}$ for best translator operation.

Figure 10. Bidirectional level shifting between two different power domains

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7.4 How to size pull-up resistor value

Sizing the pull-up resistor on an open-drain bus is specific to the individual application and is dependent on the following driver characteristics:

- The driver sink current
- The V_{OL} of driver
- The V_{IL} of the driver
- Frequency of operation

The following tables can be used to estimate the pull-up resistor value in different use cases so that the minimum resistance for the pull-up resistor can be found.

Table 6, Table 7 and Table 8 contain suggested minimum values of pull-up resistors for the PCA9306 and NVT20xx devices with typical voltage translation levels and drive currents. The calculated values assume that both drive currents are the same. $V_{OL} = V_{IL} = 0.1 \times V_{CC}$ and accounts for a ±5 % V_{CC} tolerance of the supplies, ±1 % resistor values. It should be noted that the resistor chosen in the final application should be equal to or larger than the values shown in Table 6, Table 7 and Table 8 to ensure that the pass voltage is less than 10 % of the V_{CC} voltage, and the external driver should be able to sink the total current from both pull-up resistors. When selecting the minimum resistor value in Table 6, Table 7 or Table 8, the drive current strength that should be chosen should be the lowest drive current seen in the application and account for any drive strength current scaling with output voltage. For the GTL devices, the resistance table should be recalculated to account for the difference in ON resistance and bias voltage limitations between $V_{CC(B)}$ and $V_{CC(A)}$.

Table 6. Pull-up resistor minimum values, 3 mA driver sink current for PCA9306 and NVT20xx

A-side	B-side					
	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.0 V	$R_{pu(A)}$ = 750 Ω $R_{pu(B)}$ = 750 Ω	$R_{pu(A)}$ = 845 Ω $R_{pu(B)}$ = 845 Ω	$R_{pu(A)}$ = 976 Ω $R_{pu(B)}$ = 976 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 887 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.18 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.82 kΩ
1.2 V		$R_{pu(A)}$ = 931 Ω $R_{pu(B)}$ = 931 Ω	$R_{pu(A)}$ = 1.02 kΩ $R_{pu(B)}$ = 1.02 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 887 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.18 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.82 kΩ
1.5 V			$R_{pu(A)}$ = 1.1 kΩ $R_{pu(B)}$ = 1.1 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 866 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.18 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.78 kΩ
1.8 V				$R_{pu(A)}$ = 1.47 kΩ $R_{pu(B)}$ = 1.47 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.15 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.78 kΩ
2.5 V					$R_{pu(A)}$ = 1.96 kΩ $R_{pu(B)}$ = 1.96 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.78 kΩ
3.3 V						$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.74 kΩ

Table 7. Pull-up resistor minimum values, 10 mA driver sink current for PCA9306 and NVT20xx

A-side	B-side					
	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.0 V	$R_{pu(A)}$ = 221 Ω $R_{pu(B)}$ = 221 Ω	$R_{pu(A)}$ = 255 Ω $R_{pu(B)}$ = 255 Ω	$R_{pu(A)}$ = 287 Ω $R_{pu(B)}$ = 287 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 267 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 357 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 549 Ω
1.2 V		$R_{pu(A)}$ = 274 Ω $R_{pu(B)}$ = 274 Ω	$R_{pu(A)}$ = 309 Ω $R_{pu(B)}$ = 309 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 267 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 357 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 549 Ω
1.5 V			$R_{pu(A)}$ = 332 Ω	$R_{pu(A)}$ = none	$R_{pu(A)}$ = none	$R_{pu(A)}$ = none

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Table 7. Pull-up resistor minimum values, 10 mA driver sink current for PCA9306 and NVT20xx*...continued*

A-side	B-side					
	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
			$R_{pu(B)}$ = 332 Ω	$R_{pu(B)}$ = 261 Ω	$R_{pu(B)}$ = 348 Ω	$R_{pu(B)}$ = 536 Ω
1.8 V				$R_{pu(A)}$ = 442 Ω $R_{pu(B)}$ = 442 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 348 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 536 Ω
2.5 V					$R_{pu(A)}$ = 590 Ω $R_{pu(B)}$ = 590 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 523 Ω
3.3 V						$R_{pu(A)}$ = none $R_{pu(B)}$ = 523 Ω

Table 8. Pull-up resistor minimum values, 15 mA driver sink current for PCA9306 and NVT20xx

A-side	B-side					
	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.0 V	$R_{pu(A)}$ = 147 Ω $R_{pu(B)}$ = 147 Ω	$R_{pu(A)}$ = 169 Ω $R_{pu(B)}$ = 169 Ω	$R_{pu(A)}$ = 191 Ω $R_{pu(B)}$ = 191 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 178 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 237 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 365 Ω
1.2 V		$R_{pu(A)}$ = 182 Ω $R_{pu(B)}$ = 182 Ω	$R_{pu(A)}$ = 205 Ω $R_{pu(B)}$ = 205 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 178 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 237 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 365 Ω
1.5 V			$R_{pu(A)}$ = 221 Ω $R_{pu(B)}$ = 221 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 174 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 232 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 357 Ω
1.8 V				$R_{pu(A)}$ = 294 Ω $R_{pu(B)}$ = 294 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 232 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 357 Ω
2.5 V					$R_{pu(A)}$ = 392 Ω $R_{pu(B)}$ = 392 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 357 Ω
3.3 V						$R_{pu(A)}$ = none $R_{pu(B)}$ = 348 Ω

7.5 How to design for maximum frequency operation

The maximum frequency is limited by the minimum pulse width LOW and HIGH as well as rise time and fall time. See Equation 1 as an example of the maximum frequency. The rise and fall times are shown in Figure 11.

$$f_{max} = \frac{1}{t_{LOW(min)} + t_{HIGH(min)} + t_{r(actual)} + t_{f(actual)}} \quad (1)$$

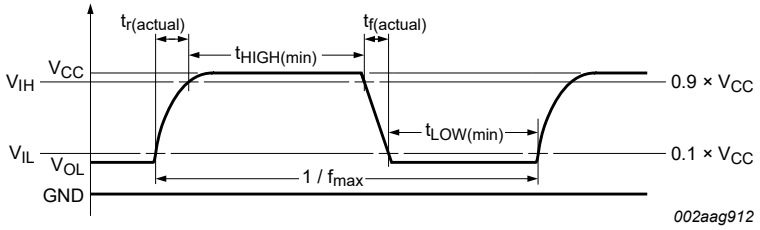


Figure 11. An example waveform for maximum frequency

The rise and fall times are dependent upon translation voltages, the drive strength, the total node capacitance ($C_{L(tot)}$) and the pull-up resistors (R_{PU}) that are present on the bus. The node capacitance is the addition of the PCB trace capacitance and the device capacitance that exists on the bus. Because of the dependency of the

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external components, PCB layout and the different device operating states the calculation of rise and fall times is complex and has several inflection points along the curve.

The main component of the rise and fall times is the RC time constant of the bus line when the device is in its two primary operating states: when device is in the ON state and it is low-impedance, the other is when the device is OFF isolating the A-side from the B-side.

A description of the fall time applied to either An or Bn output going from HIGH to LOW is as follows. Whichever side is asserted first, the B-side down must discharge to the $V_{CC(A)}$ voltage. The time is determined by the pull-up resistor, pull-down driver strength and the capacitance. As the level moves below the $V_{CC(A)}$ voltage, the channel resistance drops so that both A and B sides equal. The capacitance on both sides is connected to form the total capacitance and the pull-up resistors on both sides combine to the parallel equivalent resistance. The R_{on} of the device is small compared to the pull-up resistor values, so its effect on the pull-up resistance can be neglected and the fall is determined by the driver pulling the combined capacitance and pull-up resistor currents. An estimation of the actual fall time seen by the device is equal to the time it takes for the B-side to fall to the $V_{CC(A)}$ voltage and the time it takes for both sides to fall from the $V_{CC(A)}$ voltage to the V_{IL} level.

A description of the rise time applied to either An or Bn output going from LOW to HIGH is as follows. When the signal level is LOW, the R_{on} is at its minimum, so the A and B sides are essentially one node. They will rise together with an RC time constant that is the sum of all the capacitance from both sides and the parallel of the resistance from both sides. As the signal approaches the $V_{CC(A)}$ voltage, the channel resistance goes up and the waveforms separate, with the B side finishing its rise with the RC time constant of the B side. The rise to $V_{CC(A)}$ is essentially the same for both sides.

There are some basic guidelines to follow that will help maximize the performance of the device:

- Keep trace length to a minimum by placing the NVT device close to the processor.
- The signal round trip time on trace should be shorter than the rise or fall time of signal to reduce reflections.
- The faster the edge of the signal, the higher the chance for ringing.
- The higher drive strength controlled by the pull-up resistor (up to 15 mA), the higher the frequency the device can use.

The system designer must design the pull-up resistor value based on external current drive strength and limit the node capacitance (minimize the wire, stub, connector and trace length) to get the desired operation frequency result.

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8 Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Over operating free-air temperature range.

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{ref(A)}$	reference voltage (A)			-0.5	+6	V
$V_{ref(B)}$	reference voltage (B)			-0.5	+6	V
V_I	input voltage			-0.5[1]	+6	V
$V_{I/O}$	voltage on an input/output pin			-0.5[1]	+6	V
I_{ch}	channel current (DC)			-	128	mA
I_{IK}	input clamping current	V_I < 0 V		-50	-	mA
I_{OK}	output clamping current[2]			-50	+50	mA
T_{stg}	storage temperature			-65	+150	°C

[1] The input and input/output negative voltage ratings may be exceeded if the input and input/output clamp current ratings are observed.
[2] Low duty cycle pulses, not DC because of heating.

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9 Recommended operating conditions

Table 10. Operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{I/O}$	voltage on an input/output pin	An, Bn		0	5.5	V
$V_{ref(A)}$[1]	reference voltage (A)	VREFA		0	5.4	V
$V_{ref(B)}$[1]	reference voltage (B)	VREFB		0	5.5	V
$V_{I(EN)}$	input voltage on pin EN			0	5.5	V
$I_{sw(pass)}$	pass switch current			-	64	mA
T_{amb}	ambient temperature	operating in free-air		-40	+85	°C

[1] $V_{ref(A)} \leq V_{ref(B)}$ - 1 V for best results in level shifting applications.

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10 Static characteristics

Table 11. Static characteristics

T_{amb} = -40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IK}	input clamping voltage	I_I = -18 mA; $V_{I(EN)}$ = 0 V		-	-	-1.2	V
I_{IH}	HIGH-level input current	V_I = 5 V; $V_{I(EN)}$ = 0 V		-	-	5	µA
$C_{i(EN)}$	input capacitance on pin EN	V_I = 3 V or 0 V		-	17	-	pF
$C_{io(off)}$	off-state input/output capacitance	An, Bn; V_O = 3 V or 0 V; $V_{I(EN)}$ = 0 V		-	5	6	pF
$C_{io(on)}$	on-state input/output capacitance	An, Bn; V_O = 3 V or 0 V; $V_{I(EN)}$ = 3 V		-	11.5	13[2]	pF
R_{on}	ON-state resistance[3][4]	An, Bn; V_I = 0 V; I_O = 64 mA; $V_{I(EN)}$ = 4.5 V	[5]	1	2.7	5.0	Ω
		V_I = 2.4 V; I_O = 15 mA; $V_{I(EN)}$ = 4.5 V		-	4.8	7.5	Ω

[1] All typical values are at T_{amb} = 25 °C.
[2] Not production tested, maximum value based on characterization data of typical parts.
[3] Measured by the voltage drop between the An and Bn terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two terminals.
[4] See curves in Figure 12 to Figure 15for typical temperature and $V_{I(EN)}$ behavior.
[5] Guaranteed by design.

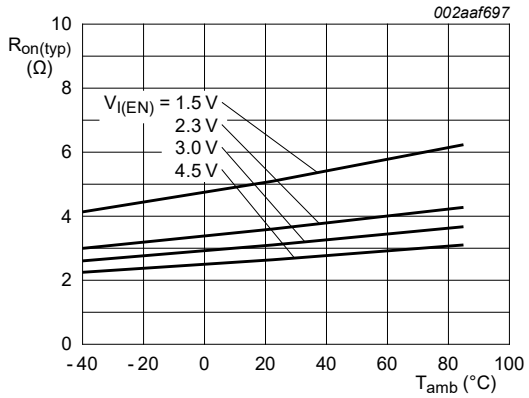


Figure 12. Typical ON-state resistance versus ambient temperature (I_O = 64 mA; V_I = 0 V)

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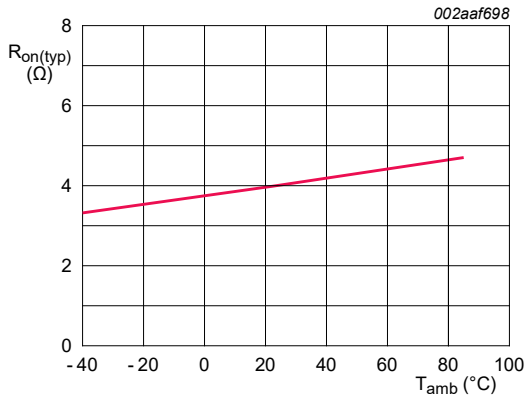


Figure 13. Typical ON-state resistance versus ambient temperature (I_O = 15 mA; V_I = 2.4 V; $V_{I(EN)}$ = 4.5 V)

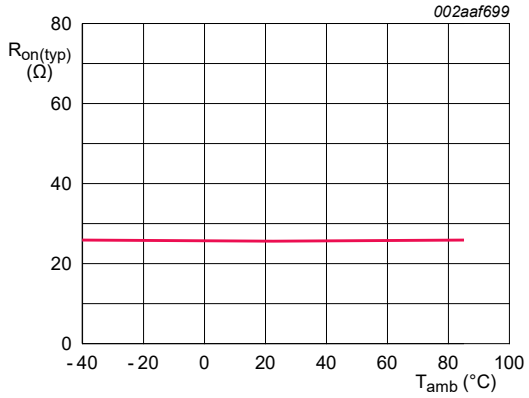


Figure 14. Typical ON-state resistance versus ambient temperature (I_O = 15 mA; V_I = 2.4 V; $V_{I(EN)}$ = 3.0 V)

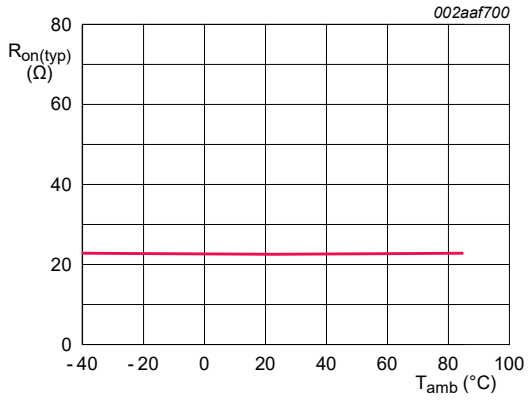


Figure 15. Typical ON-state resistance versus ambient temperature (I_O = 15 mA; V_I = 1.7 V; $V_{I(EN)}$ = 2.3 V)

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11 Dynamic characteristics

11.1 Open-drain drivers

Table 12. Dynamic characteristics for open-drain drivers

T_{amb} = -40 °C to +85 °C; $V_{I(EN)} = V_{ref(B)}$; $R_{bias(ext)}$ = 200 kΩ; C_{VREFB} = 0.1 µF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Refer to Figure 18							
t_{PLH}	LOW to HIGH propagation delay	from (input) Bn to (output) An	[1]		$R_{on} \times (C_L + C_{io(on)})$		ns
t_{PHL}	HIGH to LOW propagation delay	from (input) Bn to (output) An			$R_{on} \times (C_L + C_{io(on)})$		ns

[1] See graphs based on R_{on} typical and $C_{io(on)} + C_L$ = 50 pF.

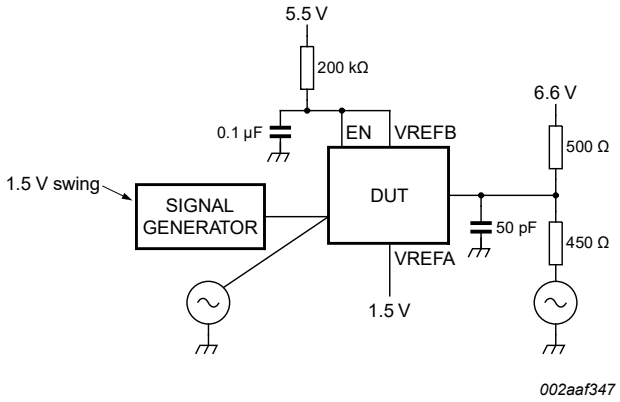


Figure 16. AC test setup

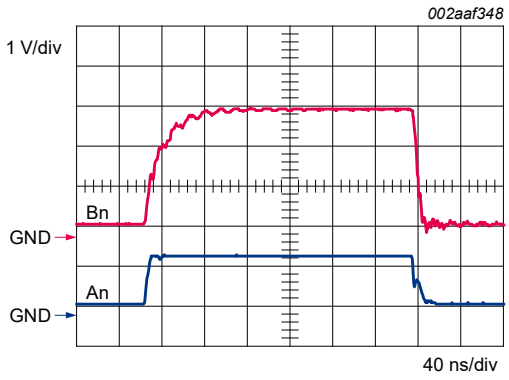
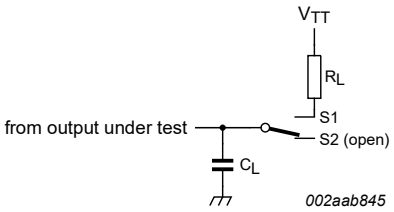


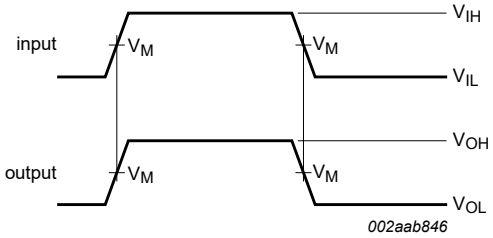
Figure 17. Example of typical AC waveform

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a. Load circuit



b. Timing diagram; high-impedance scope probe used

S2 = translating down, and same voltage.

C_L includes probe and jig capacitance.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r ≤ 2 ns; t_f ≤ 2 ns.

The outputs are measured one at a time, with one transition per measurement.

Figure 18. Load circuit for outputs

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12 Performance curves

t_{PLH} up-translation is typically dominated by the RC time constant, i.e., $C_{L(tot)} \times R_{PU}$ = 50 pF × 197 Ω = 9.85 ns, but the $R_{on} \times C_{L(tot)}$ = 50 pF × 5 Ω = 0.250 ns.

t_{PHL} is typically dominated by the external pull-down driver + R_{on}, which is typically small compared to the t_{PLH} in an up-translation case.

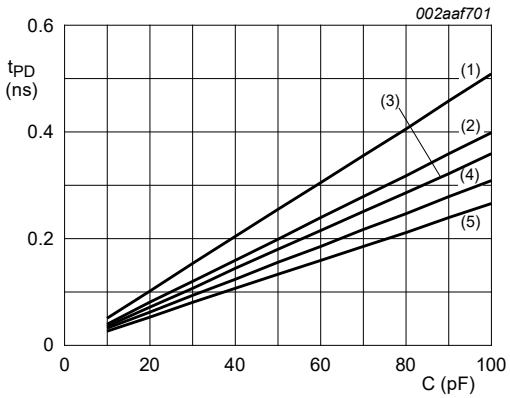
Enable/disable times are dominated by the RC time constant on the EN pin since the transistor turn off is on the order of ns, but the enable RC is on the order of ms.

Fall time is dominated by the external pull-down driver with only a slight R_{on} addition.

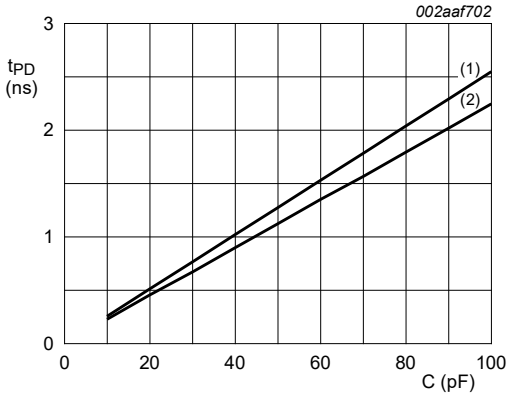
Rise time is dominated by the $R_{PU} \times C_L$.

Skew time within the part is virtually non-existent, dominated by the difference in bond wire lengths, which is typically small compared to the board-level routing differences.

Maximum data rate is dominated by the system capacitance and pull-up resistors.



1. $V_{I(EN)}$ = 1.5 V; I_O = 64 mA; V_I = 0 V.
2. $V_{I(EN)}$ = 4.5 V; I_O = 15 mA; V_I = 2.4 V.
3. $V_{I(EN)}$ = 2.3 V; I_O = 64 mA; V_I = 0 V.
4. $V_{I(EN)}$ = 3.0 V; I_O = 64 mA; V_I = 0 V.
5. $V_{I(EN)}$ = 4.5 V; I_O = 64 mA; V_I = 0 V.



1. $V_{I(EN)}$ = 3.0 V; I_O = 15 mA; V_I = 2.4 V.
2. $V_{I(EN)}$ = 2.3 V; I_O = 15 mA; V_I = 1.7 V.

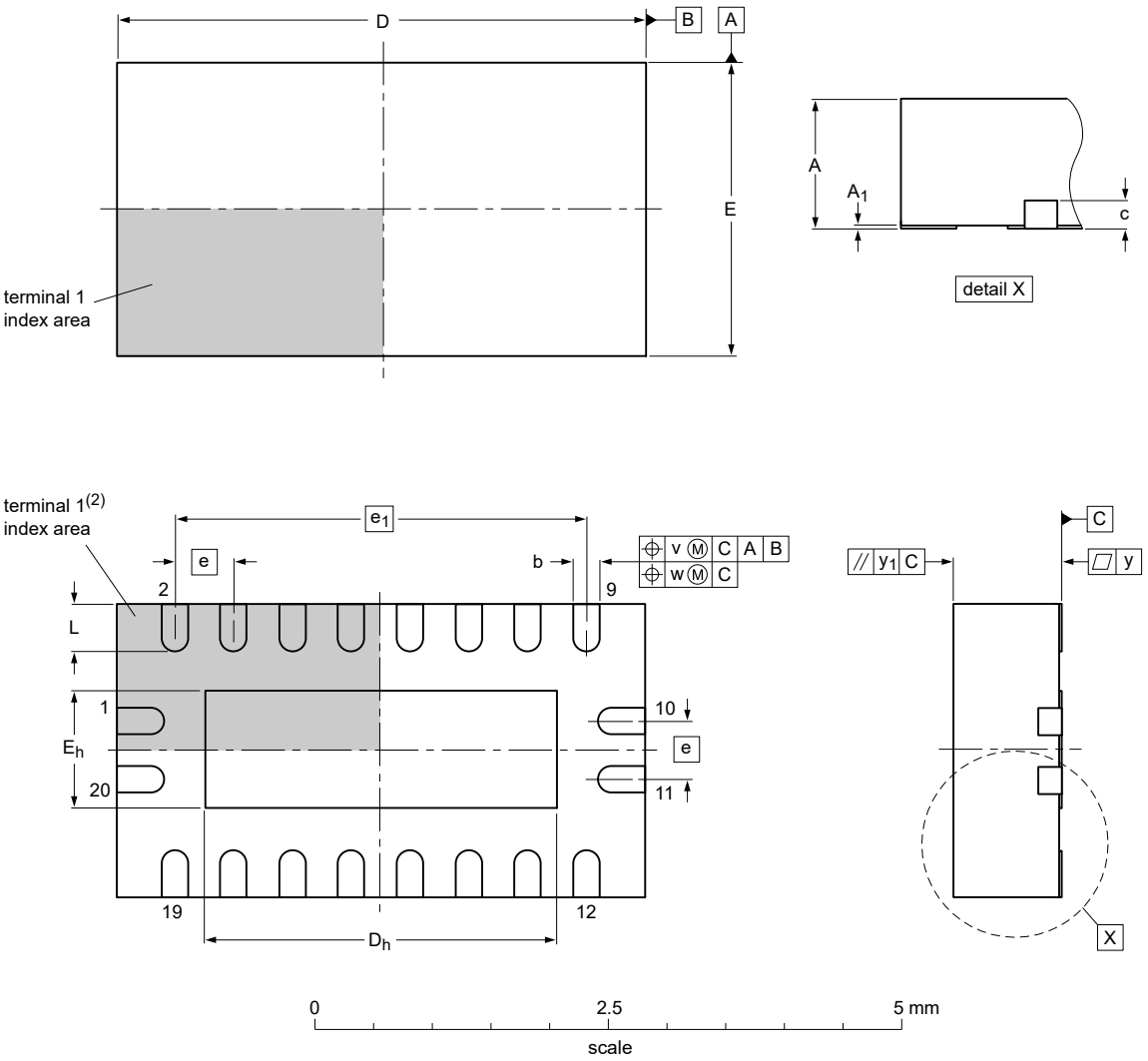
Figure 19. Typical capacitance versus propagation delay

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13 Package outline

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm **SOT764-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
	max	1.00	0.05	0.30		4.6	3.15	2.6	1.15			0.5				
mm	nom	0.90	0.02	0.25	0.2	4.5	3.00	2.5	1.00	0.5	3.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		4.4	2.85	2.4	0.85			0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.
2. Terminal 1 feature shape, size and location may vary.

sot764-1_po

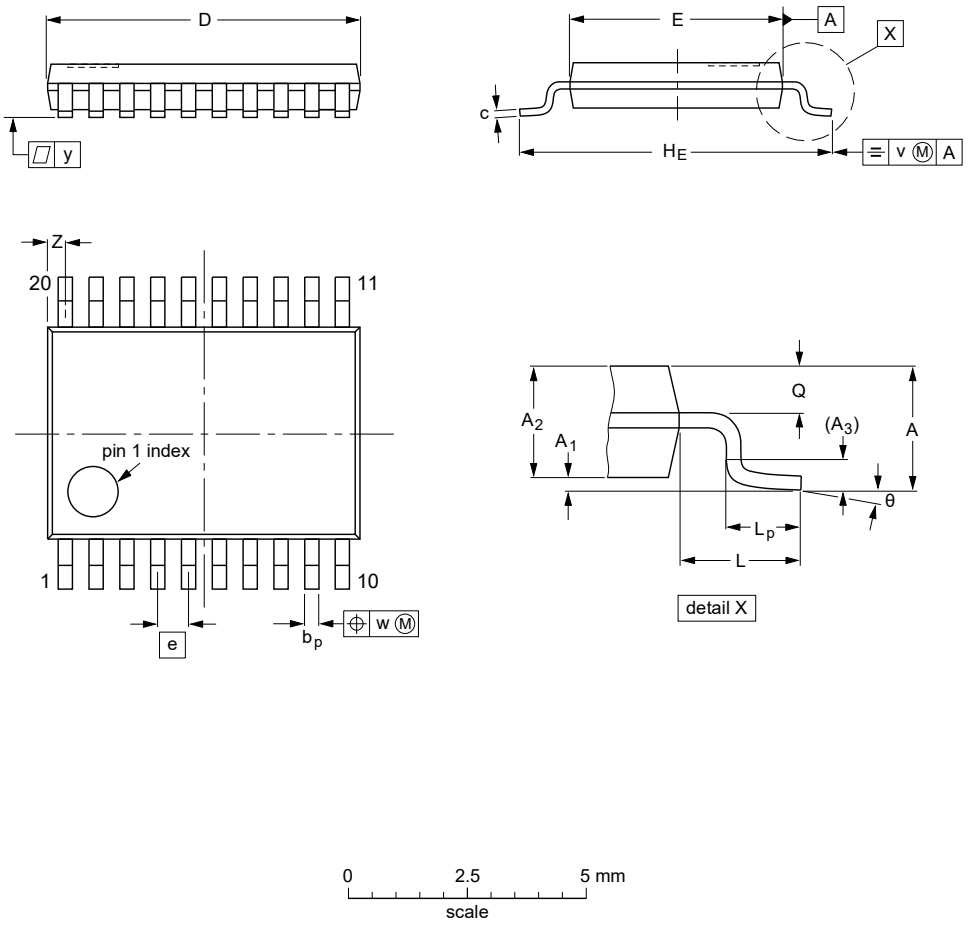
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT764-1	- - -	MO-241	- - -			~~03-01-27~~ 14-12-12

Figure 20. Package outline SOT764-1 (DHVQFN20)

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

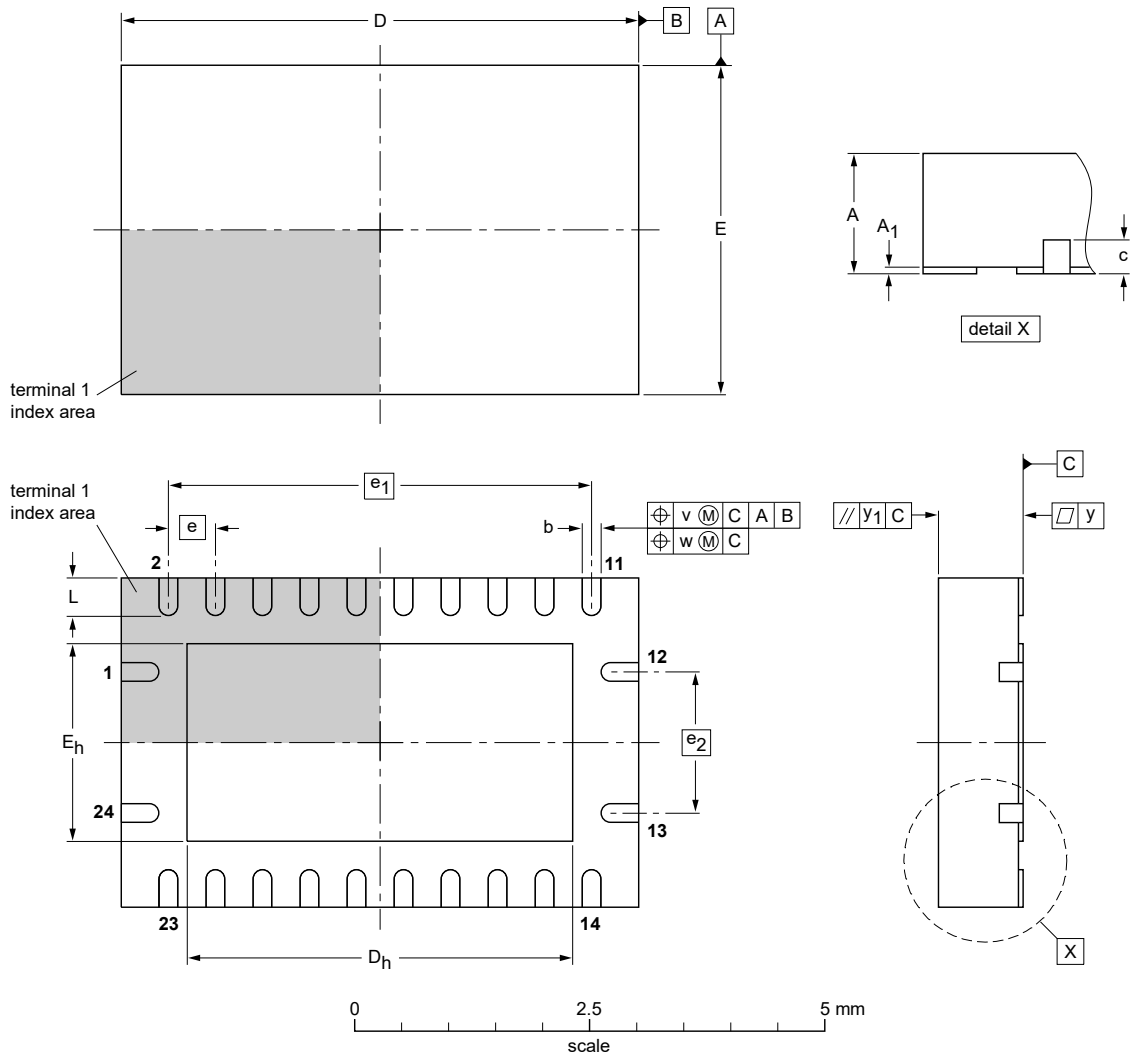
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Figure 21. Package outline SOT360-1 (TSSOP20)

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DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm **SOT815-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.6 5.4	4.25 3.95	3.6 3.4	2.25 1.95	0.5	4.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

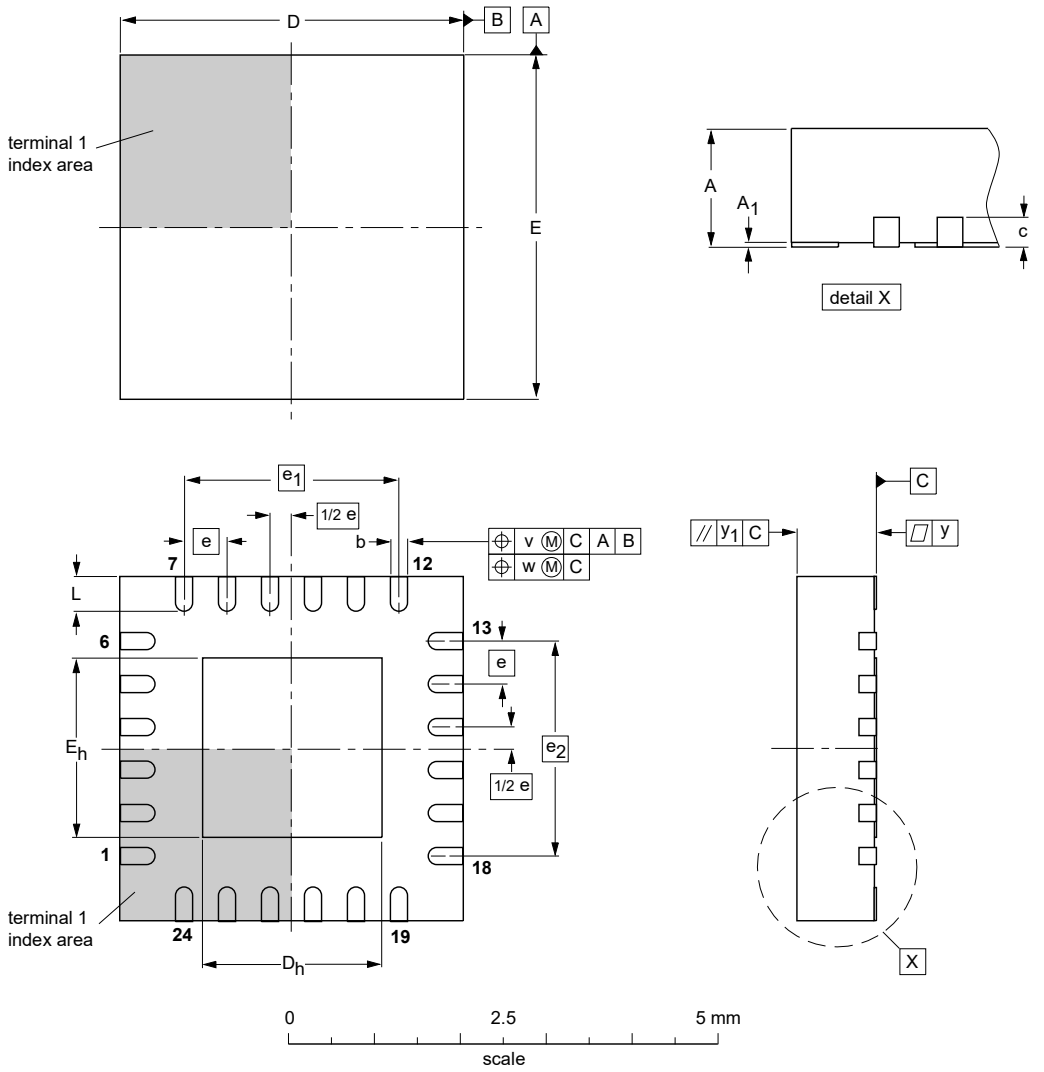
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT815-1	- - -	- - -	- - -			03-04-29

Figure 22. Package outline SOT815-1 (DHVQFN24)

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HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

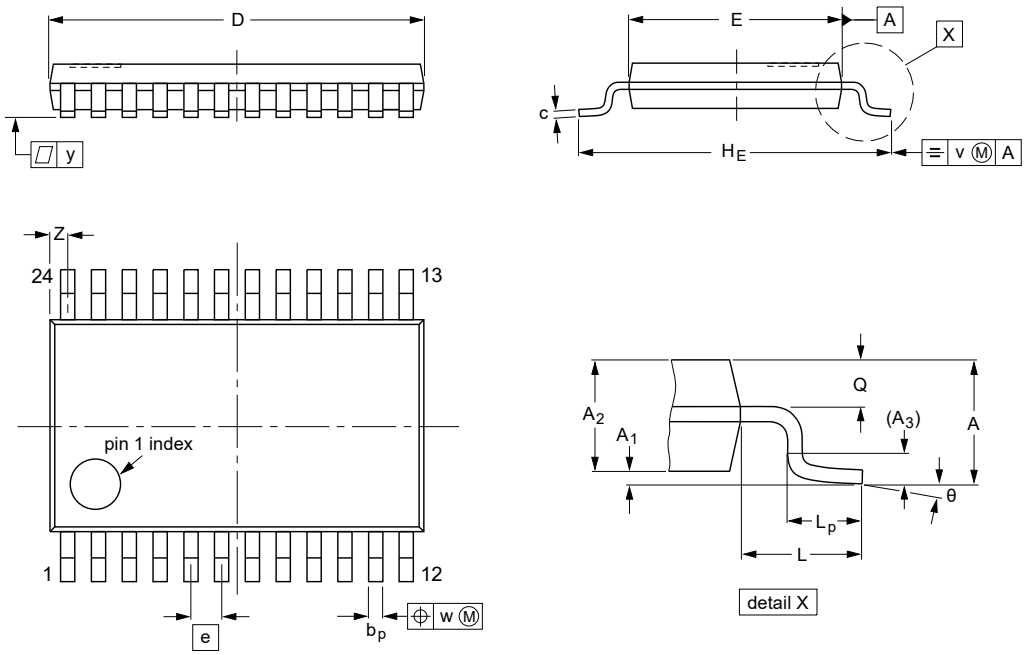
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Figure 23. Package outline SOT616-1 (HVQFN24)

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TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^{o} 0^{o}

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Figure 24. Package outline SOT355-1 (TSSOP24)

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14 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 25) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board

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- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 13 and Table 14

Table 13. SnPb eutectic process (from J-STD-020D)

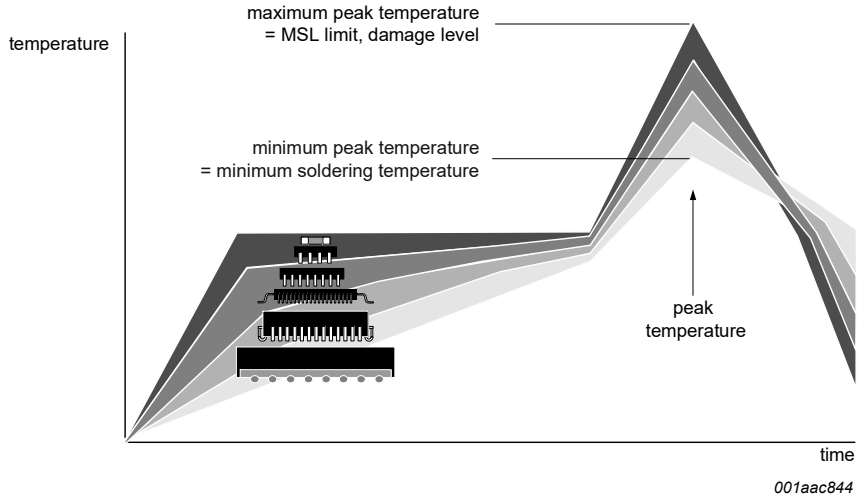
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 14. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 25.



MSL: Moisture Sensitivity Level

Figure 25. Temperature profiles for large and small components

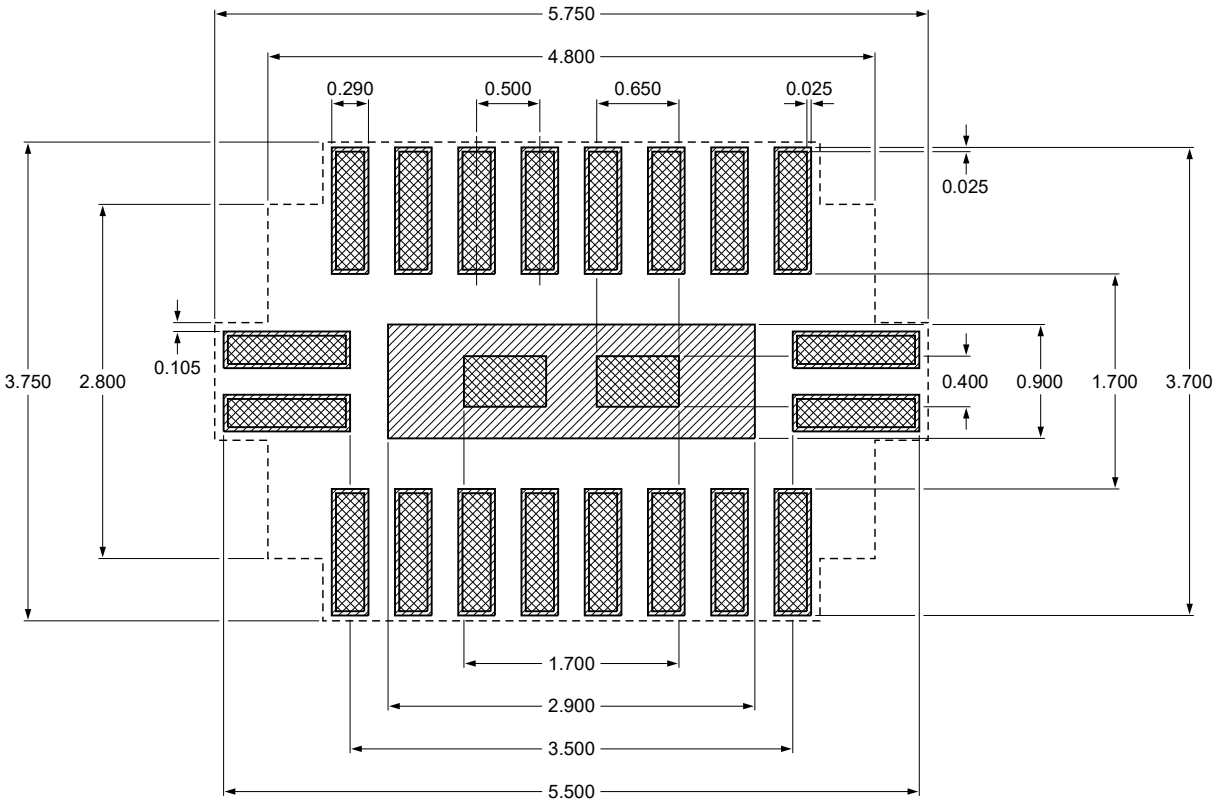
For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

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15 Soldering: PCB footprints

Footprint information for reflow soldering of DHVQFN20 package **SOT764-1**



Refer to the package outline drawing for actual layout

solder land

solder paste deposit

solder land plus solder paste

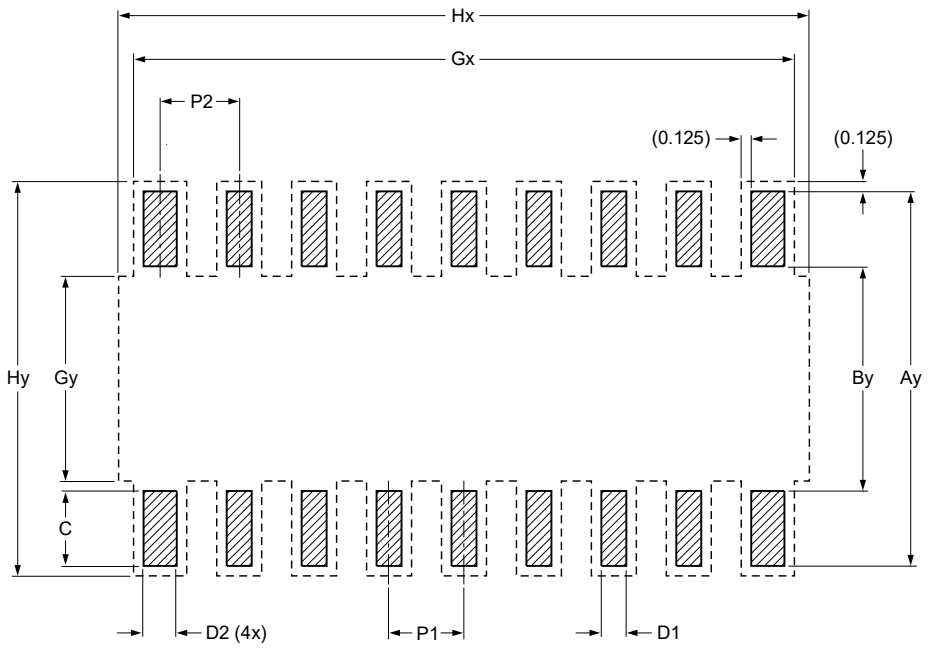
occupied area

Figure 26. PCB footprint for SOT764-1 (DHVQFN20); reflow soldering

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Footprint information for reflow soldering of TSSOP20 package **SOT360-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	6.900	5.300	7.300	7.450

sot360-1_fr

Figure 27. PCB footprint for SOT360-1 (TSSOP20); reflow soldering

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Footprint information for reflow soldering of DHVQFN24 package **SOT815-1**

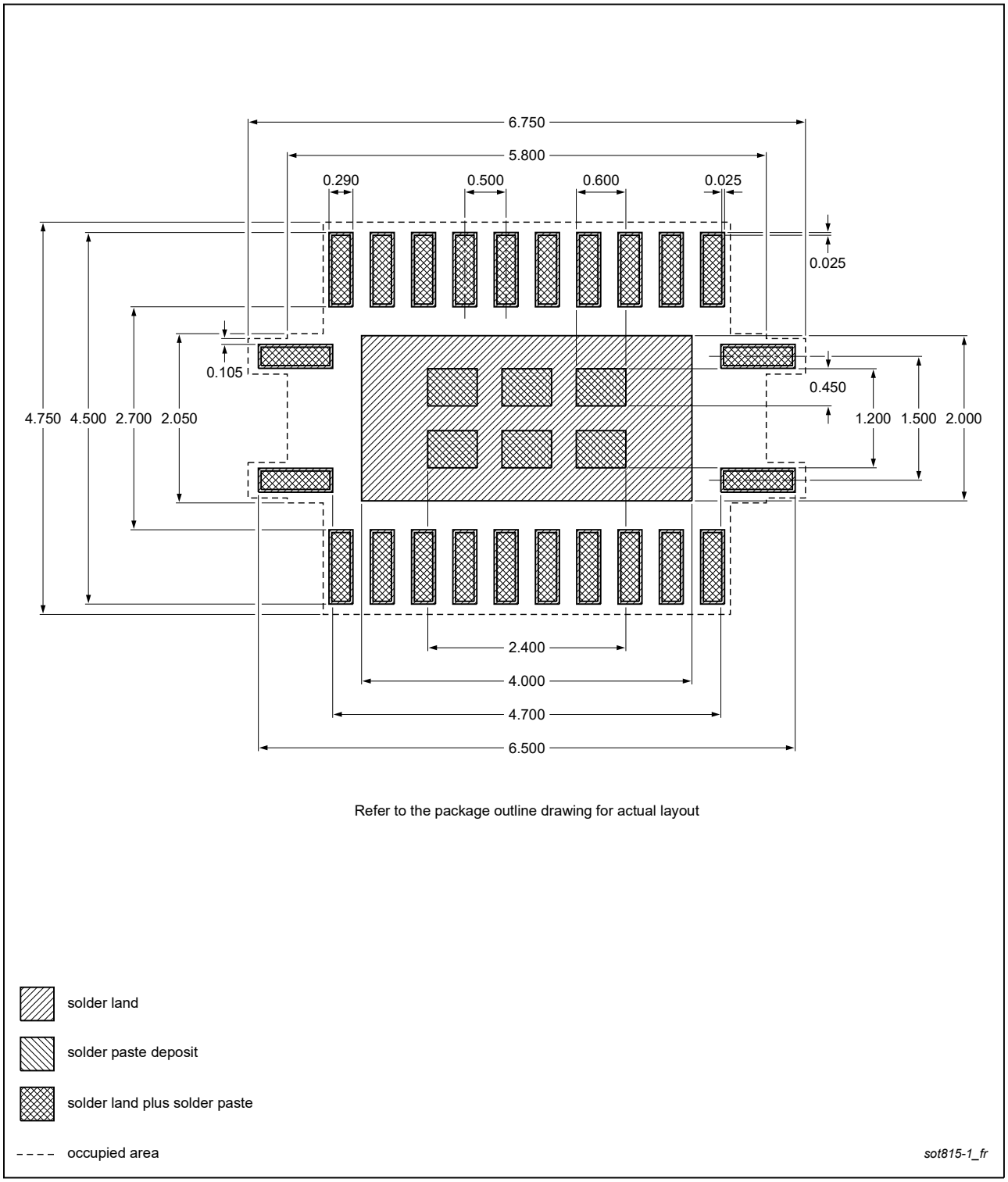
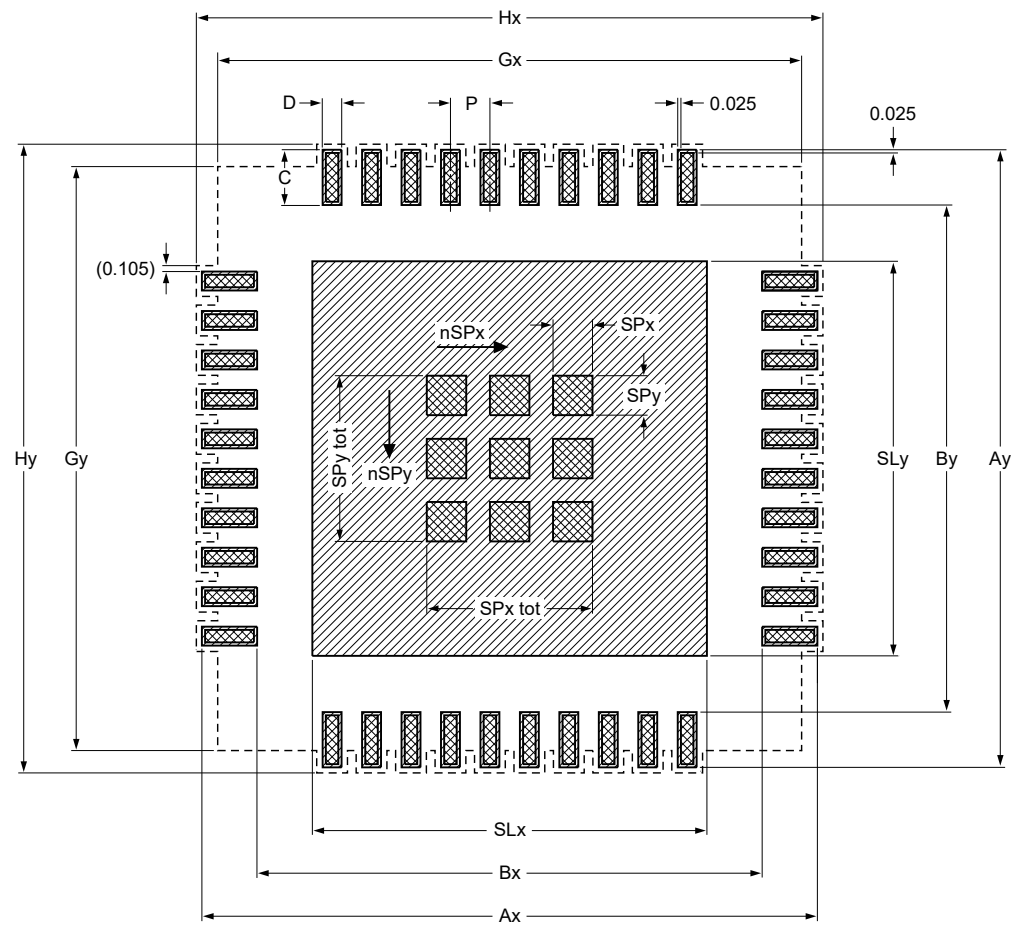


Figure 28. PCB footprint for SOT815-1 (DHVQFN24); reflow soldering

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Footprint information for reflow soldering of HVQFN24 package **SOT616-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

solder paste deposit

solder land plus solder paste

occupied area

nSPx	nSPy
2	2

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.500	5.000	5.000	3.200	3.200	0.900	0.240	2.100	2.100	1.200	1.200	0.450	0.450	4.300	4.300	5.250	5.250

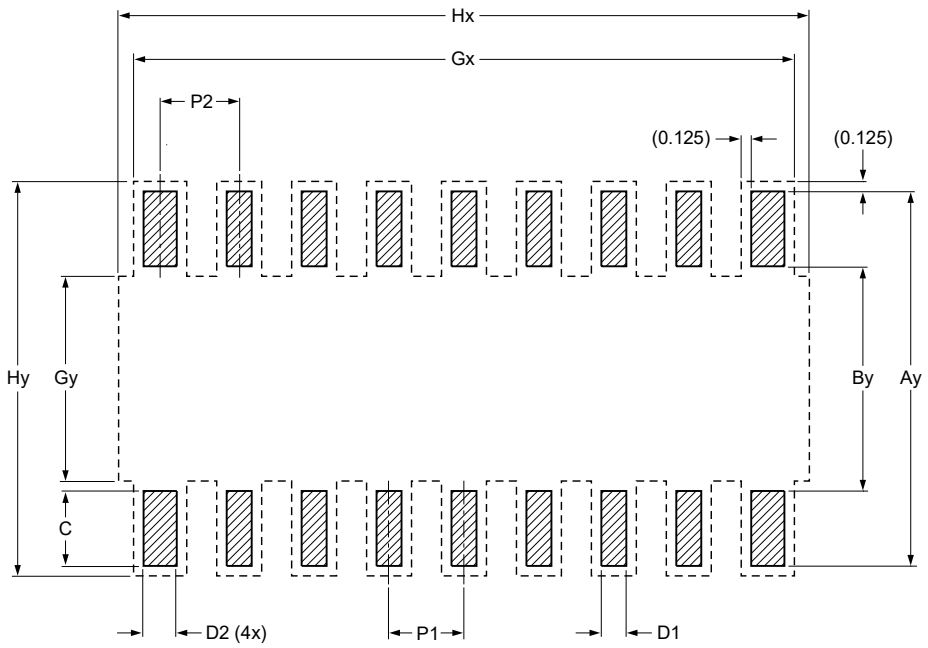
Issue date ~~07-05-07~~ 09-06-15 *sot616-1_fr*

Figure 29. PCB footprint for SOT616-1 (HVQFN24); reflow soldering

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Footprint information for reflow soldering of TSSOP24 package **SOT355-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	8.200	5.300	8.600	7.450

sot355-1_fr

Figure 30. PCB footprint for SOT355-1 (TSSOP24); reflow soldering

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16 Abbreviations

Table 15. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
GTL	Gunning Transceiver Logic
HBM	Human Body Model
I^2C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LVTTL	Low Voltage Transistor-Transistor Logic
PRR	Pulse Repetition Rate
RC	Resistor-Capacitor network

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17 Revision history

Table 16. Revision history

Document ID	Release date	Description
NVT2008_NVT2010 v.3.1	20 September 2024	• Replaced part number NVT2008 BQ,115 with NVT2008BQZ; refer to DN 202405004DN
NVT2008_NVT2010 v.3	27 January 2014	• added (new) Section 3.1 • deleted (old) Section 7.4 "Sizing pull-up resistor" • added (new) Section 7.4 • added (new) Section 7.5 • added (new) Section 15
NVT2008_NVT2010 v.2	3 September 2012	Product data sheet
NVT2008_NVT2010 v.1	8 September 2010	Product data sheet

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Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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