OL2385

Industrial RF transceiver

Rev. 1.0 — 15 June 2016

Product data sheet
COMPANY PUBLIC

1. General information

1.1 General description

The device is a fully integrated single-chip transceiver intended for use in an industrial environment.

The device incorporates several commonly used building blocks including a crystal stabilized oscillator, a fractional-N based Phase Locked Loop (PLL) for accurate frequency selection in both TX and RX, Low Noise Amplifier (LNA), attenuator for Automatic Gain Control (AGC), I/Q down-mixer and two high resolution Analog to Digital Converters (ADC).The conversion into the digital domain is done in an early phase, enabling a software defined radio like approach.

By transforming signals in the digital domain in an early phase, one highly configurable RX channel is available including channel mixer, channel filter, ASK/FSK demodulator, clock-data recovery, bit processor and a micro-controller memory interface (DMA) allowing the micro-controller to complete the data handling and handshaking.

The device has an embedded RISC micro-controller optimized for high performance and low power as well as an EROM for customer applications. The device also includes a medium power UHF transmit system with a high dynamic range of -35dBm to +14dBm which makes it ideal for the use in narrow band communication systems. The TX system allows transmission with data rates up to 400 kbit/s NRZ.

Power ramping and splatter avoidance filters are included to ensure that the transmit spectrum fulfills all the common standards in Europe, USA and Asia. The phase noise of the transmitter supports ARIB operation.

The device includes a series of timers to allow for autonomous polling and wake-up applications. The TX and RX data buffers are located in the RAM with autonomous direct memory access (DMA), reducing the 'real-time' overhead for the accompanying micro-controller. The device can be interfaced via SPI, UART or LIN protocol compatible UART. Simplified programming of the device is facilitated by the HAL (Hardware Abstraction Layer).

The transceiver is configured to operate with low active and standby power consumption, ideal for battery powered applications.

2. Features and benefits

- Single IC for worldwide usage in bands between 160 MHz and 960 MHz
- Wide dynamic range with AGC to achieve excellent blocking performance
- I/Q down conversion with digital IF processing and automatic gain compensation
- Integrated I/Q phase and amplitude mismatch compensation
- Receiver path with 2 multiplexed antenna inputs enables different antenna matching
- Advanced signal monitoring and data management for fast and reliable signal detection and processing
- High dynamic range RSSI measurement
- Programmable PA with digitally controlled power ramping and shaping
- Operation up to 400 kbit/s 4FSK for high data rate applications
- RX and TX data buffer in RAM with independent DMA channels
- Integrated temperature sensor for crystal temperature drift compensation
- Support of high accuracy external temperature sensor for ARIB systems
- Integrated 16-bit extended micro RISC kernel for system on chip solutions with up to 32 kByte EROM
- 10 independent DMA channels for powerful data transfer and configuration
- Integrated copy machine for fast data transfer
- Coprocessor for bit manipulation and code redundancy cycle calculation (CRC)
- Several timers for firmware development including 3 general purpose timers, 3 RX channel timers, low power mode polling timer and watch dog timer
- Clock driver for micro controller crystal sharing
- Controlled via SPI, UART, LIN compatible UART
- 10 bit ADC sensor interface with up to 100 kSps sampling rate
- Tool chain (compiler, assembler, linker, debugger) with in circuit debug capability
- API available to simplify custom firmware development
- IREC evaluation and demonstration kit available for basic RF operation
- Remote control protocol (RCP) to operate RF without custom firmware via SPI/UART

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3. Applications

The IC supports the following system applications:

- Smart Metering (sub-GHz Zigbee, wireless M-bus)
- Home and building security and automation (KNX-RF)
- Remote control devices
- Wireless medical applications
- Wireless sensor network
- Industrial monitoring and control
- Low Power Wide Area networks (SigFox)

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4. Quick reference data

Table 1. Quick reference data

	Parameter	Conditions	Min	Typ	Max	Unit
1	General					
1.1	UHF Carrier Frequency		158		960	MHz
1.2	Power Down Current			700		nA
1.3	Supply Voltage		1.9		5.5	V
1.4	Operating Temperature		-40		+85	°C
2	Transmitter					
2.1	Supply Current	XTAL		0.25		mA
		Tx @ 0 dBm		9		mA
		Tx @ 14dBm		29		mA
2.2	Max Output Power		14			dBm
2.3	Phase Noise @ 100 kHz Offset	169 MHz band		-120		dBc/Hz
		434 MHz band		-117		dBc/Hz
		868 MHz band		-109		dBc/Hz
		925 MHz band		-108		dBc/Hz
3	Receiver					
3.1	Supply Current	@ 45 kHz BW		11		mA
		@ 10 kHz BW		11		mA
3.2	Data Rate				400	kbit/s
3.3	Sensitivity	ASK/OOK @ 10 kHz BW		-123		dBm
3.3.1		FSK @ 50 kHz BW		-112		dBm
3.3.2		FSK @ 10 kHz BW		-124		dBm
3.5	Adjacent channel rejection	868 MHz		>50		dB
3.6	Image channel rejection (calibrated)			60		dB
3.7	Channel Filter Band Width		4		360	kHz
3.8	RSSI	Dynamic Range @ 10kHz BW	120			dB
3.10		Variation	-3		3	dB
4	Micro-controller					
4.1	EROM				32	kByte
4.2	Customer RAM				7	kByte

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5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
OL2385AHN/00100[1]	HVQFN48	Plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 x 7 x 0.85 mm; terminal pitch 0.5 mm; wettable flanks	SOT619-13
OL2385AHN/001A0[2]	HVQFN48	Plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 x 7 x 0.85 mm; terminal pitch 0.5 mm; wettable flanks	SOT619-13
OL2385AHN/001B0[3]	HVQFN48	Plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 x 7 x 0.85 mm; terminal pitch 0.5 mm; wettable flanks	SOT619-13
OL2385AHN/001C0[4]	HVQFN48	Plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 x 7 x 0.85 mm; terminal pitch 0.5 mm; wettable flanks	SOT619-13

[1] Generic version without preflashed software

[2] SigFox software stack preflashed

[3] WMBus 2013 software stack preflashed

[4] sub-GHz ZigBee MAC layer software stack preflashed

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6. Marking

Table 3. Marking information

Line	Example	Description
A	OL2385	2385 = Type number
B	*******	ID: *****xx (* = Diffusion lot number + x = Assembly ID); In case the number of digits exceeds 7, ID is truncated by sequentially removing positions from left to right.
C	ZSDyww*	Z = Manufacturer Code SSMC S = Assembly Centre Kaohsiung D = RoHS2006 yww = Date Code (Y = year, W = calendar week) * = Release Status X = customer engineering sample (CES) Y = customer qualification sample (CQS) _ = released samples (RFS)
D	2385ABrrff	2385 = Type number A = std version B = BOM version rr = Rom Code version ff = SW version

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7. Block diagram

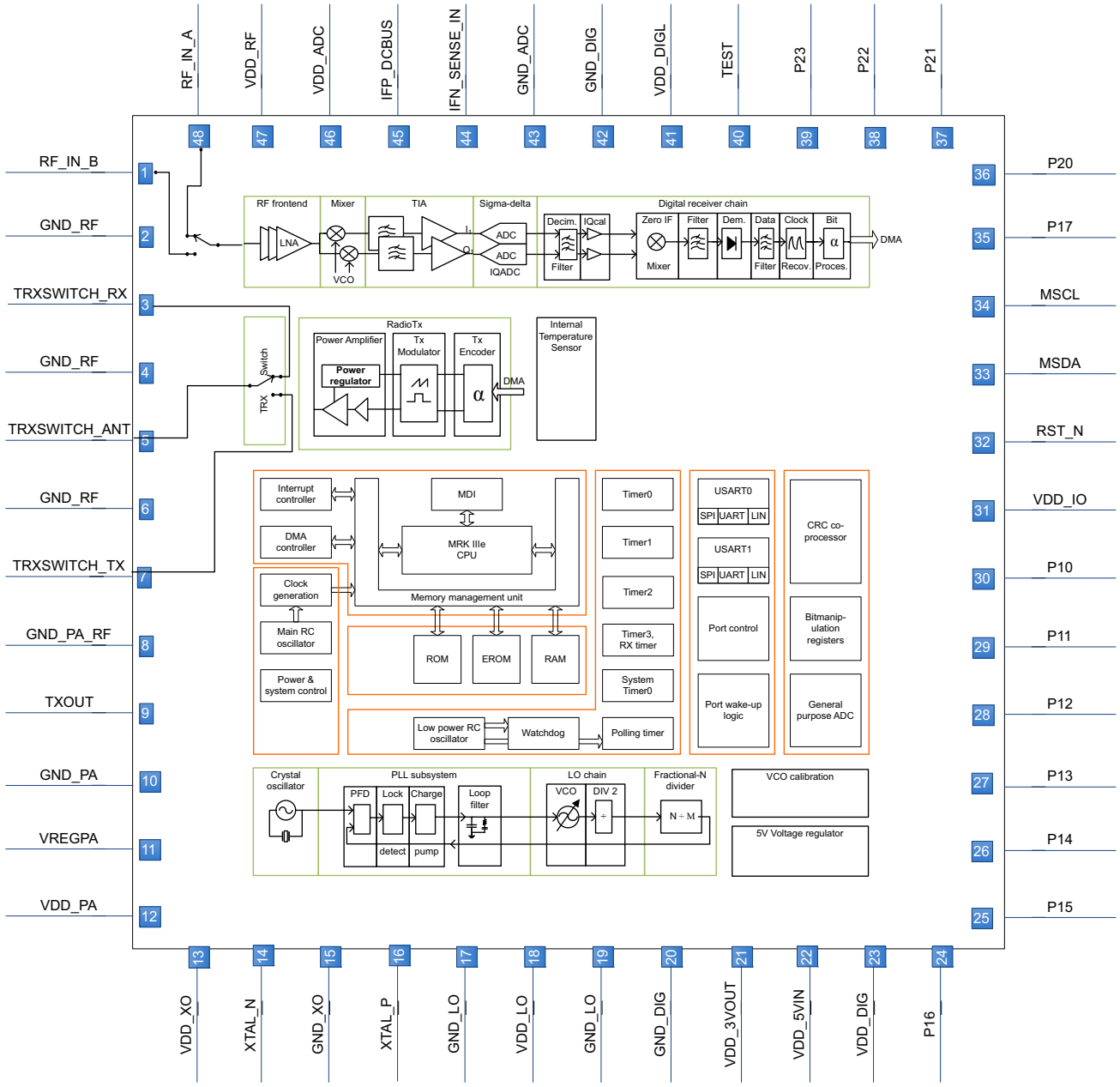


Fig 1. Block diagram

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8. Pinning information

The circuit is packaged in a HVQFN48 with wettable flanks.

8.1 Pinning

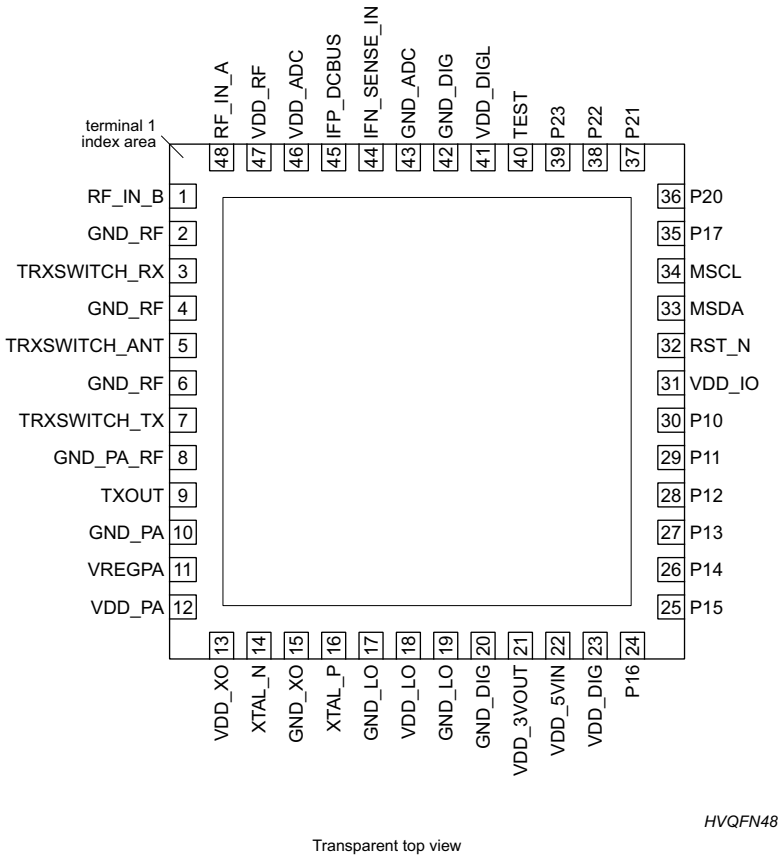


Fig 2. Pinout HVQFN48

8.1.1 Pin 1 keep out area

For the purpose of package orientation, so called "pin 1" identification is included. This can either be as an additional small pin / pad as shown in design 1 (left) of Figure 3, or a notch in the die pad as shown in design 2 (right) of Figure 3.

Note that the pin 1 identifier is electrically connected to the ground plate.

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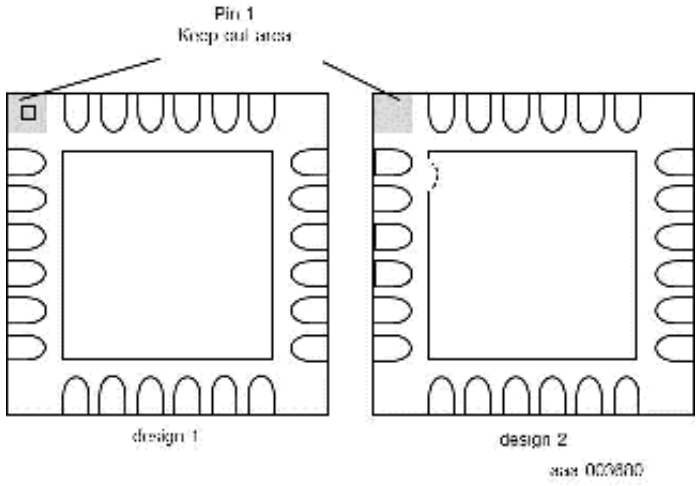


Fig 3. Pin 1 keep out area

8.2 Pin description

Table 4. Pinning description

Symbol	Pin	Description
RF_IN_B	1	RF receiver input B (internally multiplexed with RF receiver input A)
GND_RF [6]	2	Ground
TRXSWITCH_RX	3	TRX switch (interface to RX part)
GND_RF [6]	4	Ground
TRXSWITCH_ANT	5	TRX switch (interface to antenna)
GND_RF [2][6]	6	Ground - connected to exposed die pad area
TRXSWITCH_TX	7	TRX switch (interface to TX part)
GND_PA_RF	8	Ground
TXOUT [7]	9	Power amplifier output
GND_PA	10	Ground
VREGPA	11	Regulated power amplifier supply, requires external choke to TXOUT
VDD_PA	12	Power supply for PA block in transmit path
VDD_XO	13	Power supply for crystal oscillator
XTAL_N	14	Crystal oscillator input
GND_XO	15	Ground
XTAL_P	16	Crystal oscillator output
GND_LO	17	Ground
VDD_LO	18	Power supply for local oscillator
GND_LO	19	Ground
GND_DIG	20	Ground (digital)
VDD_3VOUT	21	3 V output voltage of the 5 V to 3 V LDO
VDD_5VIN	22	5 V input voltage of the 5 V to 3 V LDO
VDD_DIG	23	Power supply for digital part
P16	24	GPIO, wake-up, USART0, USART1

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Table 4. Pinning description

Symbol	Pin	Description
P15	25	GPIO, timer input, timer output, USART0, USART1
P14	26	GPIO, timer output, USART0, USART1
P13	27	GPIO, USART0
P12	28	GPIO, wake-up, timer input, USART0, USART1
P11	29	GPIO, fail safe wake-up, timer input, USART0, USART1
P10	30	GPIO, fail safe wake-up, timer output, RX and TX clock output
VDD_IO	31	Power supply for digital I/Os
RST_N [8]	32	Reset input (active low), internal pull-up resistor
MSDA [9]	33	Monitor and debug interface serial data (input/output; internal pull-up in input mode)
MSCL [10]	34	Monitor and debug interface serial clock (output)
P17	35	GPIO, wake-up, timer input, timer output, RX data output, TX data input, USART0, USART1
P20	36	GPIO, wake-up, timer output, USART1
P21	37	GPIO, GP ADC input NEG
P22	38	GPIO, wake-up, GP ADC input POS, timer output
P23	39	GPIO, wake-up, GP ADC reference voltage, USART1
TEST [1]	40	Test pin (must be connected to ground in the application)
VDD_DIGL [3][4][5]	41	LDO output voltage
GND_DIG	42	Ground (digital)
GND_ADC	43	Ground
IFN_SENSE_IN	44	Selectable ADC negative input / pin used for test purposes
IFP_DCBUS	45	Selectable ADC positive input / pin used for test purposes
VDD_ADC	46	Power supply for ADC in receiver chain
VDD_RF	47	Power supply for receive path
RF_IN_A	48	RF receiver input A (internally multiplexed with RF receiver input B)

[1] Pin TEST must be connected to ground in the application.

[2] The exposed die pad area must be connected to ground.

[3] VDD_DIGL is the internal supply of the digital part and shall only be externally connected to a blocking capacitor 15 nF (nominal).

[4] VDD_DIGL must neither be pulled to high voltages nor to GND

[5] Do not use VDD_DIGL to supply external devices

[6] All GND_RF are connected internally

[7] TXOUT is not to be supplied externally except for an inductor connected to VREGPA

[8] RST_N shall be connected only with a 4.7 kΩ resistor in series.

[9] MSDA features an on-chip pull-up resistor to VDD_IO and may be left open or terminated to VDD_IO, as desired.

[10] MSCL is an output and shall be unconnected in the application.

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9. Design information

9.1 Introduction

The device can be used in many applications where the flexibility of the micro-controller in combination with the dedicated receive and transmit hardware are exploited. The range of applications of such a device span from simple transmitter applications triggered by a key press to complex half duplex RF multi protocol transceivers. In order to describe the wealth of features and possibilities it is necessary to describe more detailed the key functional blocks of the device. Functions, such as power management and wake-up procedures (where the micro-controller is not controlling the process directly), permeate the complete device and are described in the coming sections. The main functions are the micro-controller subsystem, including the frequency generation system (the core of all RF functionality), the transmitter system and the receiver systems.

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9.2 Power management

9.2.1 Modes of operation

The device supports operation in a 3 V, 5 V or a mixed 3 V and 5 V environment supporting the following supply use cases:

1. Device and digital interface supplied with regulated 5 V supply
   - Digital signaling between all devices in the system is done at 5 V level.
2. Device and digital interface supplied with regulated 3 V (3.3 V) supply
   - Digital signaling between all devices in the system is done at 3 V (3.3 V) level.
3. Device supplied with regulated 3 V (3.3 V) supply and digital interface supplied with regulated 5 V supply
   - Digital signaling between all devices in the system is done at 5 V level.
4. Device and digital interface supplied with a single primary lithium battery cell (3.6 V … 1.9 V)
   - Digital signaling between all devices in the system is done at the unregulated battery voltage level.
5. Supply with a single rechargeable battery cell (4.2 V … 3.0 V) and an accompanied voltage regulator (3.6 V … 2.5 V)
   - Device is supplied with the regulated voltage.
   - Digital signaling between all devices in the system is done at the unregulated battery voltage level.

Connection diagrams for these different use cases are depicted in Figure 4.

9.2.2 External power supply domains

Several power supply pins are present to provide the required supply isolation between various RF, analogue and digital blocks (external power supply domains). The power supply pins have to be directly connected to a regulator output or a battery. External supply switches are not required.

Adequate blocking capacitors have to be connected to the external supply pins.

Table 5. External power supply domains

Power supply pin	Voltage range	Description
VDD_IO, GND_IO	3 V, 5 V	Main power supply domain of the device; supplies the I/O port pins, the power-on reset circuit and an internal low-power regulator which supplies the power state logic, the I/O port control latches, the polling timer and the watchdog.
VDD_LO, GND_LO	3 V	Power supply for the local oscillator (fractional-N PLL).
VDD_XO, GND_XO	3 V	Power supply for the crystal oscillator.
VDD_RF, GND_RF	3 V	Power supply for the radio frontend including the LNA, the input attenuators and the mixer for receive mode.
VDD_PA, GND_PA	3 V	Power supply for the power amplifier regulator output and the power amplifier control for transmit mode.
VDD_ADC, GND_ADC	3 V	Power supply for the sigma-delta ADCs in the radio receiver.

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Table 5. External power supply domains

Power supply pin	Voltage range	Description
VDD_DIG, GND_DIG	3 V	Power supply for the digital part.
VDD_5VIN	5 V	Supply voltage input for the internal power regulator. This regulator generates the required supply voltage for the device's VDD supply pins in the 3 V domains.
VDD_3VOUT	3 V	Regulated supply voltage output of the internal power regulator.

[1] Voltage ranges are given here only for information purpose. Please refer to the electrical characteristics for detailed voltage range specification.

The external power supply domains with the associated power supply pins are briefly described in the Table 5.

The package HVQFN has an exposed die pad at the back which is intended as heat sink and additional ground connection.

The device includes an internal power regulator which can be used to generate a voltage less than 3.6 V when such a voltage is not available. This regulator utilizes the two supply pins VDD_5VIN and VDD_3VOUT. The regulator is only on if the device is in power supply state ACTIVE. In all other power supply states the regulator is off. VDD_5VIN can be supplied permanently and the input voltage must be greater than 3.6 V.

The application has to ensure that the current drawn from the internal power regulator does not exceed the maximum limit given in the section electrical characteristics. If this limit is exceeded all supply voltage pins in the 3 V domain must be connected to an external voltage regulator. It is not allowed to supply parts of the device with the internal and other ones with an external 3 V supply.

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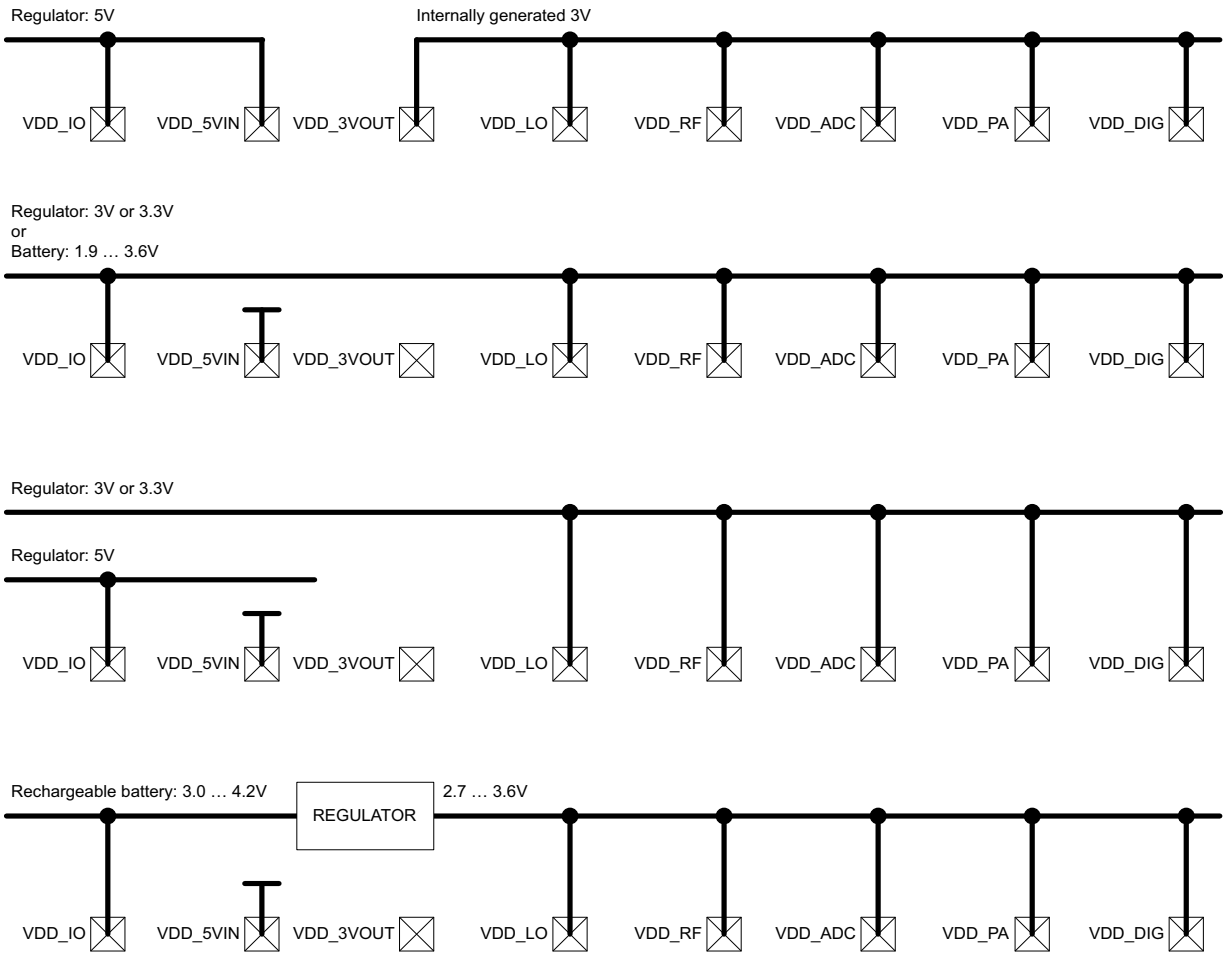


Fig 4. Connection of external power supply domains for different power supply use cases

9.2.3 Recommended external capacitors in the supply domains

- The device is supplied by an external supply with 3 V or 3.3 V:
  - Pin 21 VDD_3VOUT: open, not connected
  - Pin 22 VDD_5VIN: connected to GND
  - Pin 31 VDD_IO: 10 nF (±20 %) capacitor
  - Pin 41 VDD_DIGL: 15 nF (±20 %) capacitor (mandatory)
  - Pin 47 VDD_RF: 10 nF (±20 %) capacitor
  - Pin 12 VDD_PA: 10 nF (±20 %) capacitor
  - Pin 23 VDD_DIG: 10 nF (±20 %) capacitor
  - Pin 18 VDD_LO: 22 nF (±20 %) capacitor
  - Pin 13 VDD_XO: 68 nF (±20 %) capacitor
  - Pin 46 VDD_ADC: 10 nF (±20 %) capacitor

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- The device is supplied by an external supply with 5V and the internal 5V to 3V regulator is used:
  - Pin 21 VDD_3VOUT: 10nF capacitor (±20%)
  - Pin 22 VDD_5VIN: connected to external 5 V supply, 100nF (±20%) capacitor plus optional 2.2µF capacitor
  - Pin 31 VDD_IO: 10nF (±20%) capacitor
  - Pin 41 VDD_DIGL: 15nF (±20%) capacitor (mandatory)
  - Pin 47 VDD_RF: 10nF (±20%) capacitor
  - Pin 12 VDD_PA: 10nF (±20%) capacitor
  - Pin 23 VDD_DIG: 10nF (±20%) capacitor
  - Pin 18 VDD_LO: 22nF (±20%) capacitor
  - Pin 13 VDD_XO: 68nF (±20%) capacitor
  - Pin 46 VDD_ADC: 10nF (±20%) capacitor

9.2.4 Power supply states

The device supports four different power states:

- RESET state
- POWER-OFF state
- ACTIVE state
- STANDBY state

The state diagram for the functional power supply states is given in Figure 5:

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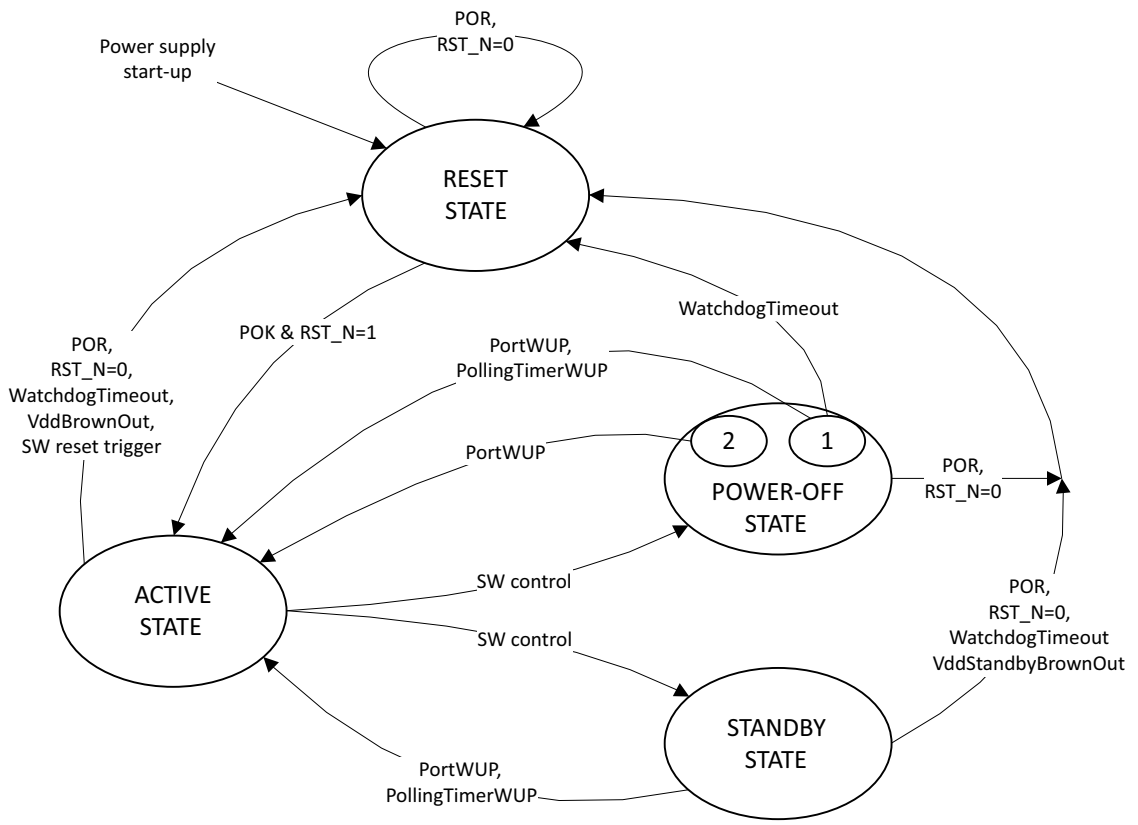


Fig 5. Power supply state diagram

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9.3 Local oscillator

The radio frequencies needed for reception and transmission are created using a local oscillator. The signals for the reference namely crystal oscillator, mixer signals and the mixer phases for both transmission and reception are generated here. The purity, stability and matching of these signals define the maximum performance that can be achieved by the RF system; therefore the blocks are optimized for these performance parameters. The choice of the architecture of the Fractional-N_PLL and that of the voltage controlled oscillator (VCO) guarantees highest performance and flexibility with the minimum of current consumption.

The transmission of FSK is achieved by modulation of the PLL and therefore the loop filter supports a high bandwidth to allow data rates up to 400kbit/s.

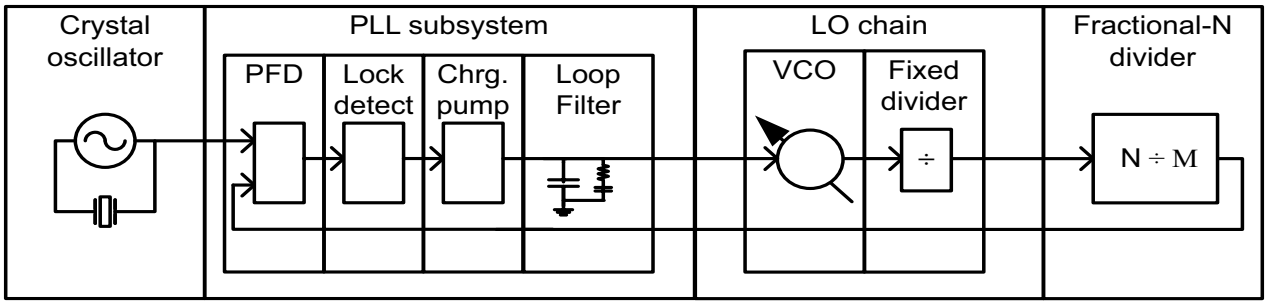


Fig 6. Local Oscillator

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9.4 UHF transmitter subsystem

9.4.1 General description

The UHF transmitter consists of a modulator block for narrow band FSK and ASK, which controls the PLL to generate the RF signal and two power amplifier blocks. A 12 dBm PA block, which is able to deliver +14 dBm output power, and a 0 dBm block to save power.

The modulation is digitally controlled, either directly to the power amplifier regulator for ASK and power ramping, or via the main LO by controlling the fractional divider to generate FSK modulation in the LO.

- TX Modulator for ASK and FSK
- High current regulator with fast response
- Power amplifier delivering 14dBm max.
- Power amplifier switchable to deliver 0dBm max.
- Power can be regulated in 0.25dB steps

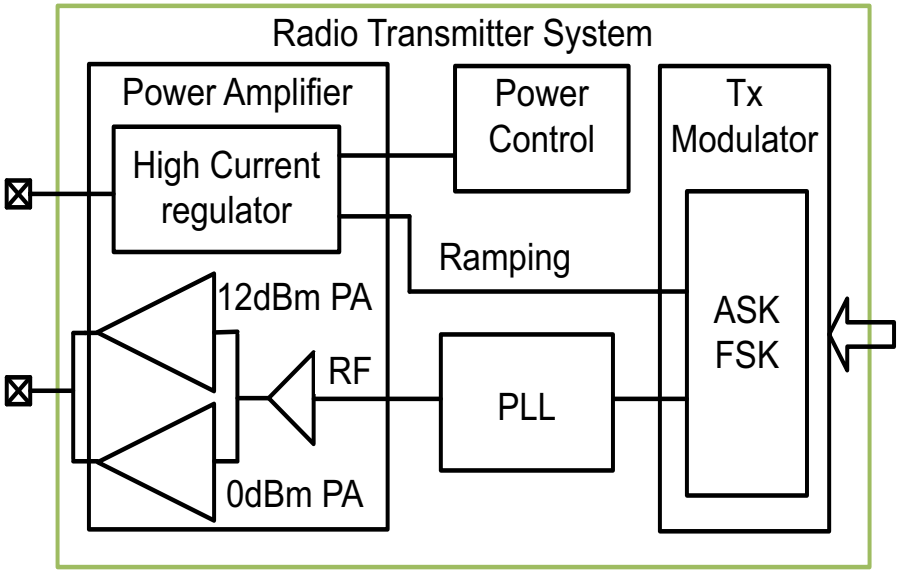


Fig 7. Radio transmitter system

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9.4.2 TRX switch

The TRX switch is a fully featured RF switch used to optimize the component count on the application boards. Many system require a software controlled RF switch function to select between antennas and auxiliary inputs. Although the circuit has two dedicated RF inputs the flexibility in combining the RX and TX paths after the relevant RF matching adds real benefit for the product.

9.4.2.1 Features

- 50 Ohm low loss paths from TX to Antenna
- 50 Ohm low loss path RX to antenna
- High isolation when switch is open
- Save external components

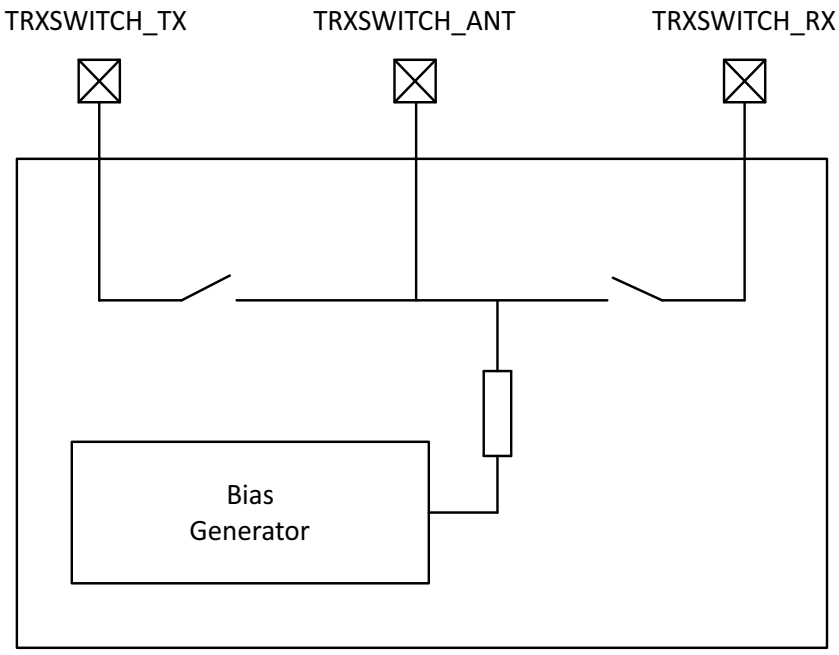


Fig 8. Transmit receive switch

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9.5 UHF receiver subsystem

The UHF receiver subsystem consists of a low IF RF down conversion system. With low gain in the RF and a high resolution ADC used in the baseband to provide the necessary dynamic range. The system includes a low noise figure and high linearity LNA stage, supported by passive attenuator blocks controlled by an AGC loop. Down conversion and high gain baseband amplifiers ensure that the dynamic range of the ADC is exploited fully. The digital receiver front-end includes the preprocessing and I/Q compensation. The digital receive chain performs the channel selection, demodulation and framing. The complete system is shown in Figure 9.

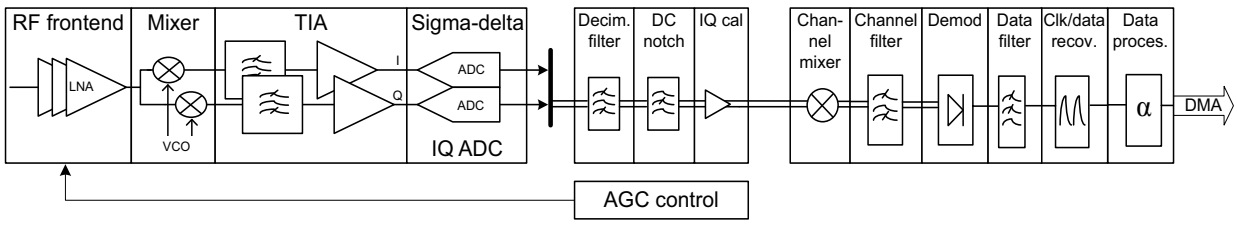


Fig 9. UHF receiver subsystem

9.5.1 Features

- RX Antenna switch with 2 inputs
- Wide band receiver for carrier frequencies in the range of 158 to 960 MHz
- Low noise figure: 5 dB typically @ 434 MHz
- Digitally controlled automatic gain control
  - 18 attenuation steps of 2 dB at RF input
  - 15 attenuation steps of 2 dB at mixer input
- IQ down conversion - high phase accuracy
- IF bandwidth with +/-400 kHz (3dB)
- RF and IF level detectors for AGC loop
- Programmable bias for amplifier stages
- DC offset correction in the baseband
- Digital IF preprocessing
- Narrow band receive chain with DMA

9.5.2 Antenna switch

In order to have the possibility to use the device at more than one frequency band or in an antenna diversity application, an integrated antenna switch is implemented.

9.5.3 LNA

The LNA is a wide-band inductor-free, highly-linear, low-power and low-noise amplifier. The LNA uses internal feedback for obtaining its high linearity and a well defined gain as well as good input matching over temperature and voltage. The LNA has a single-ended

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input with a wide-band input matching optimized for 200 Ohms. A current reuse scheme is employed to maintain maximum performance with minimum current consumption. Power consumption is controllable depending on the demands of the system. The advanced feedback structure in combination with the attenuator set-up results in very low LO radiation.

9.5.4 Attenuators

Passive 2 dB step attenuators are positioned in front of the LNA and in front of the mixer in order to control the gain of the receiver. The RF inputs have integrated ESD protection and integrated AC coupling for easy application. A matching network can be applied off-chip for best performance and adaptation to different source impedances.

9.5.5 Mixer

The mixer multiplies the single-ended RF signal with a balanced quadrature (I and Q) LO signal in order to differentiate between the wanted and image channel. A special algorithm is used to remove the impact of analog mismatch on the image rejection. This usually leads to intrusion (leakage) of the image channel into the wanted channel.

9.5.6 Baseband amplifier (TIA) and DC offset compensation

The baseband amplifier stage (TIA - transimpedance amplifier) amplifies the balanced quadrature (I and Q) mixer output signals to the optimal level for the ADC and performs the anti-aliasing filtering in front of the sigma-delta ADC. Internal DC offset correction loops guarantee maximum image suppression and high linearity and dynamic range.

9.5.7 SD ADC

The SD ADC is a 1-bit higher order oversampled sigma-delta ADC with very low current consumption. The sigma delta switched time core makes use of the most modern feedback techniques to ensure stability and performance over a wide frequency band, process and temperature variation. It features fast auto-calibration for optimum performance. The calibration time is typically below 1 µs. The output is a single bit data-stream which is further processed by the digital baseband.

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9.5.8 Digital receiver block diagram

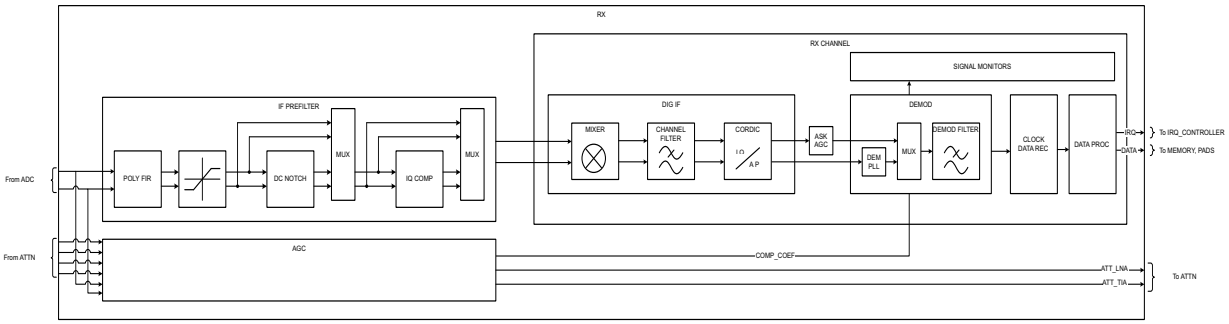


Fig 10. Digital receiver block diagram

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9.5.9 Digital IF preprocessing

9.5.9.1 Features

- Decimation filter
- DC notch filter with optional bypass
- IQ mismatch compensation with optional bypass

The IF prefilter blocks perform sampling rate reduction from the highly oversampled 1-bit sigma delta bit stream into a Nyquist sampling multi bit signal. Furthermore the decimated signal is high pass filtered to remove unwanted DC components which could disturb further processing in the IQ compensation unit. The IQ compensation unit removes the unwanted image frequency components from the complex low IF signal.

9.5.9.2 Block diagram

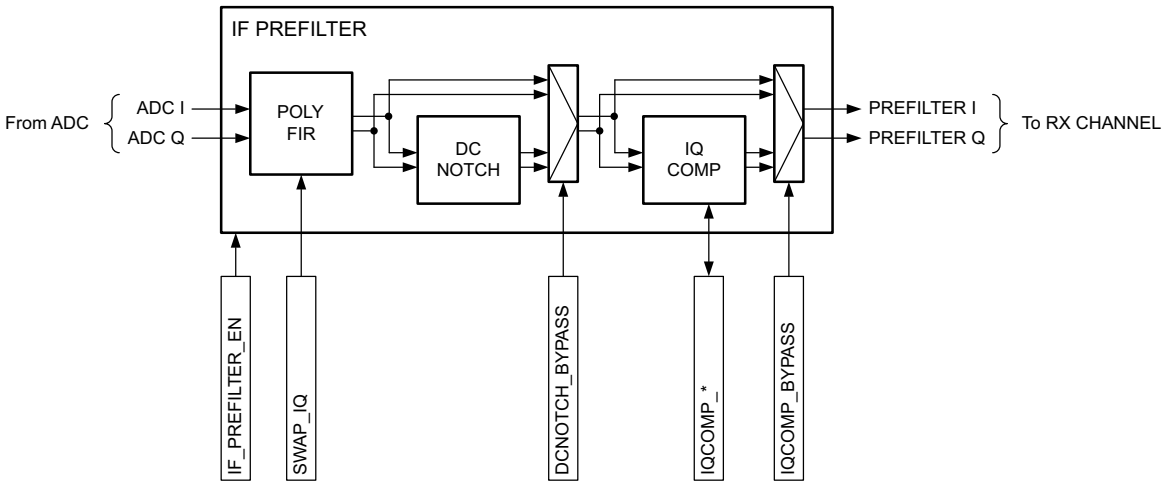


Fig 11. Digital receiver front-end

9.5.9.3 Description

The IF prefilter block has a dedicated enable bit field which allows power saving in case the receiver is not enabled at all.

Due to the tuner design, the resulting spectral view at the intermediate frequency is inverted (higher frequencies are mapped to lower and vice versa). In order to compensate that, it is possible to swap the I and Q components. If the IQ swap is enabled, the frequency order at IF is matching to the RF.

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9.5.10 Automatic gain control

9.5.10.1 Features

- Highly programmable for best flexibility
- 2dB gain steps
- Automatic or manual mode

9.5.10.2 Block diagram

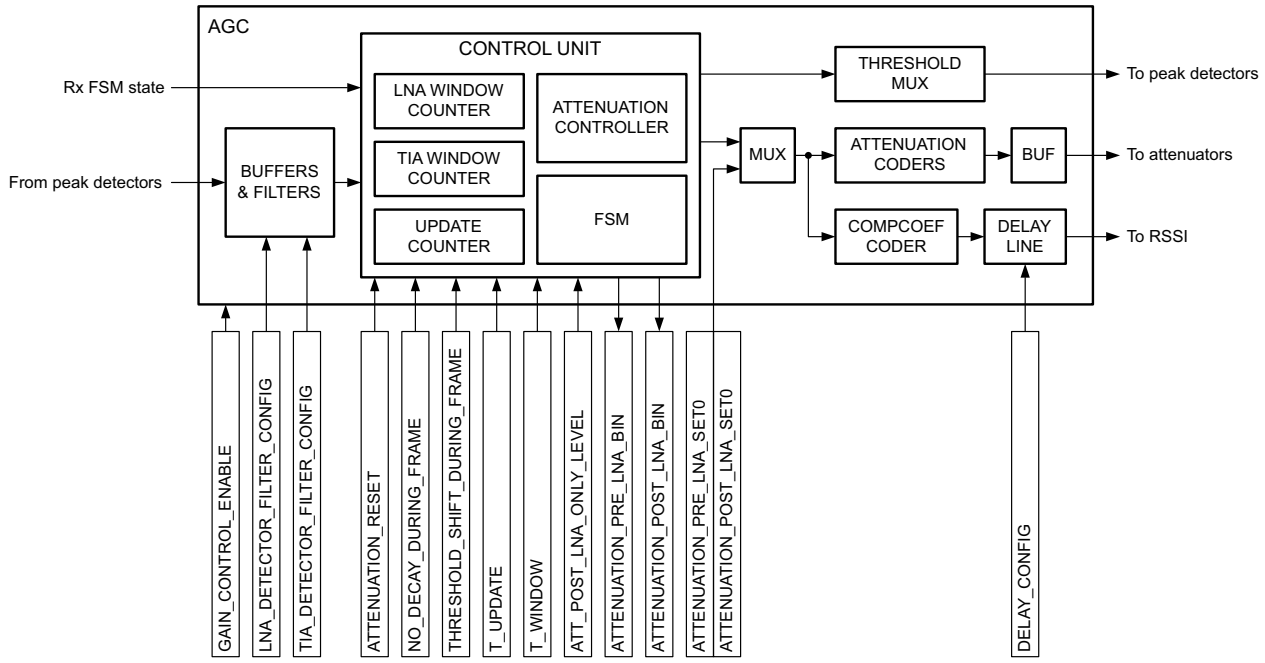


Fig 12. AGC block diagram

9.5.10.3 Description

The automatic gain control (AGC) ensures that the analog front-end is protected from high power signals and therefore ensures high linearity figures throughout the whole dynamic range of the receiver.

The AGC can work in manual or automatic gain control mode. The manual mode is intended for debugging system level use cases and for device test.

In automatic mode the AGC measures signal strength, makes a decision to get the best performance and drives the gain of the analogue front-end.

For measuring signal strength pairs of underload and overload peak detectors are present at the LNA and at the TIA. The detectors are fast-response voltage comparators checking if the signal envelope belong to the range specified by the underload and overload threshold values.

The AGC control strategy has been optimized for providing the best noise figure and maintaining all linearity requirements. Therefore the first steps of the attenuation are always done with the baseband (TIA) attenuator. The next steps are done with the

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front-end (LNA) attenuator until it has reached its maximum attenuation. The remaining attenuation steps are done with the baseband attenuator again. The attenuation level at which attenuation control is given from the baseband to the front-end attenuator (takeover threshold) can be modified by software. The control strategy has been presented on the attenuation distribution figure below. It shows how the attenuation sum A_S is distributed between front-end A_{FE} and baseband A_{BB} attenuations with regards to the requested attenuation A_R.

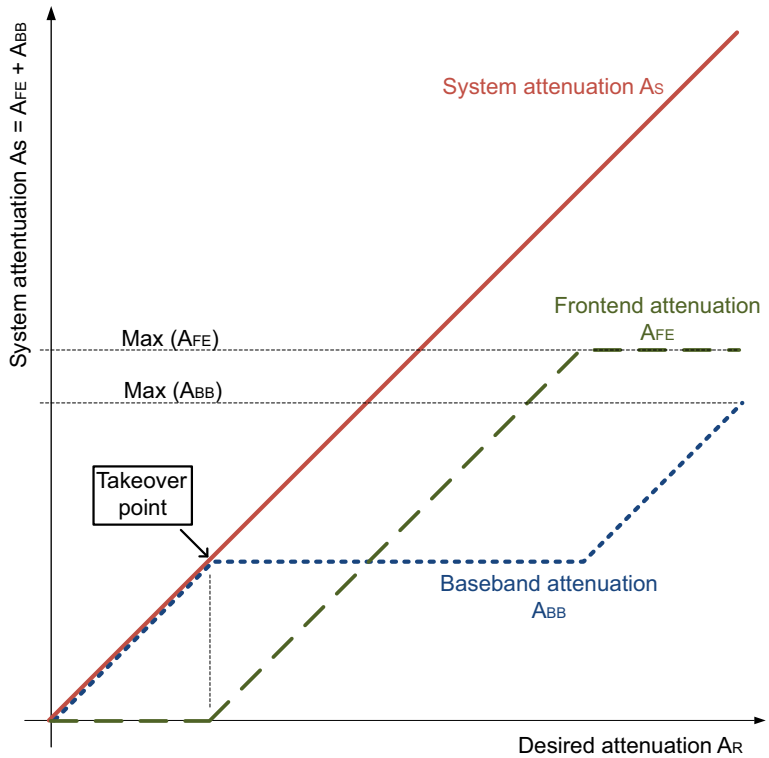


Fig 13. Attenuation Distribution

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9.5.11 Narrow band receive chain

9.5.11.1 Features

- Complex IF channel mixer (-400kHz to +400kHz)
- AGC compensation (for RSSI correction)
- Configurable channel filter (4kHz to 360kHz)
- FSK and ASK demodulator with configurable data filter
- RSSI and offset frequency detector/measurement
- Clock and data recovery for ASK and FSK Manchester encoded data (high data rate offset up to 12%)
- Manchester receiver for ASK and FSK Manchester encoded data (high data rate offset up to 12%)
- NRZ receiver for NRZ data for 2FSK, 4FSK and 8FSK
- Signal monitors (signal property checks)
- Data processing unit with DMA interface

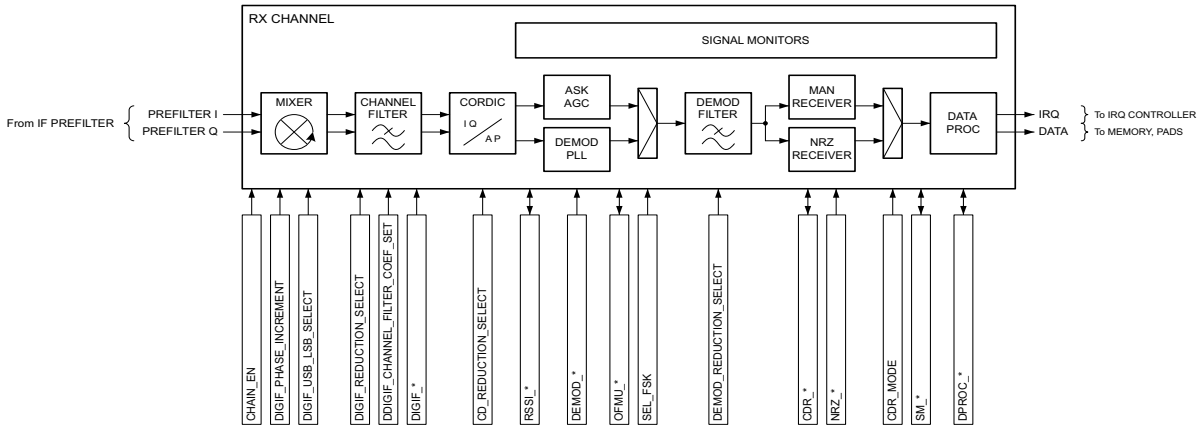


Fig 14. RX chain/channel block diagram

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9.5.12 Data processing

The data processing block combines the functions of data recognition and packet building for valid data sequences and accommodates the transfer to the memory of the device. There are many functional blocks which work together to carry out this function.

9.5.12.1 Features

- Data processing core
  - Line decoder
  - Pattern matching unit
  - Signal monitors (code properties)
- Data counter
- Timer
- Receive state machine
- Interrupt generation and status flags
- Micro-controller interface with direct memory access (DMA) channel

The data processing sub units are enabled by the main state machine automatically on demand.

Two different receive algorithms can be selected. The Manchester receiver is optimized for line coded data (e.g. Manchester, Biphase Mark Code) and supports high data rate offsets. The NRZ receiver is optimized for NRZ data and supports higher-order modulation (2FSK, 4FSK, 8FSK). Signal monitors can be used to minimize the likelihood of a false synchronization in noise (i.e. false alarm rate).

The following signal monitors can be used for the Manchester receiver: modulation present detector, RSSI measurement, data rate checker, FSK deviation checker, CDR PLL lock detector, gap detector

The following signal monitors can be used for the NRZ receiver: modulation present detector, RSSI measurement, FSK deviation checker.

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9.6 Micro-controller subsystem

The digital control of the device is done with a RISC micro controller (uC) designed for low power and high performance applications. The uC has optimized peripherals to facilitate quick and efficient control of the radio frequency blocks as well as having multiple peripherals for interfacing the device to the external application. Timers and mathematical units are also implemented in hardware to allow the uC to concentrate upon the main application level challenges. Such activities as data recognition and data movement are carried out with specific blocks thus increasing the computing power available for the user application.

The core uC is discussed in detail in a separate document but the interaction as concerns this specific device and moreover the peripherals are discussed in depth here.

9.6.1 RISC controller

The device is powered by NXP's 3rd generation low power 16-Bit Extended Micro RISC Kernel (MRK IIIe), which controls device operation in ACTIVE state.

The MRK IIIe utilizes a Harvard architecture featuring a 16 bit ALU. The instruction set supports 8 bit and 16 bit operations and is optimized for C programming. Additionally to all commands supported by the standard MRK III, MRK IIIe supports an extended instruction set with hardware supported multiplication and division as well as efficient bit field modification operations. Details about the MRK III controller including full instruction set description are found in Ref. 1.

Due to the efficient 2-stage pipeline (fetch / execute), most instructions execute in a single machine cycle (four clock cycles), resulting in ultra low power consumption.

The device provides 64 kByte of linear data address range and 128 kByte linear code address range, powerful addressing modes and high code density. Besides, the MRK IIIe supports a power saving mode and code/data protection mechanisms (privilege modes).

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9.6.2 System clock

9.6.2.1 Clock sources

The following clock sources are available:

- Crystal oscillator clock, XOCLK, 27.6 MHz or 55.2 MHz
  - Clock source for system clock, PLL synthesizer, Sigma-Delta ADC
- Main RC oscillator clock, MRCCLK, nominal 25.5 MHz
  - Clock source for system clock
- Sampling clock of the Sigma-Delta ADC, FSCLK, 27.6 MHz
  - Clock source for system clock, RX subsystem
- Low-power RC oscillator, LPRCCLK, nominal 180 kHz
  - Clock source for polling timer and watchdog
- Digitally calibrated divided clock output, PTCLK, nominal 16 kHz

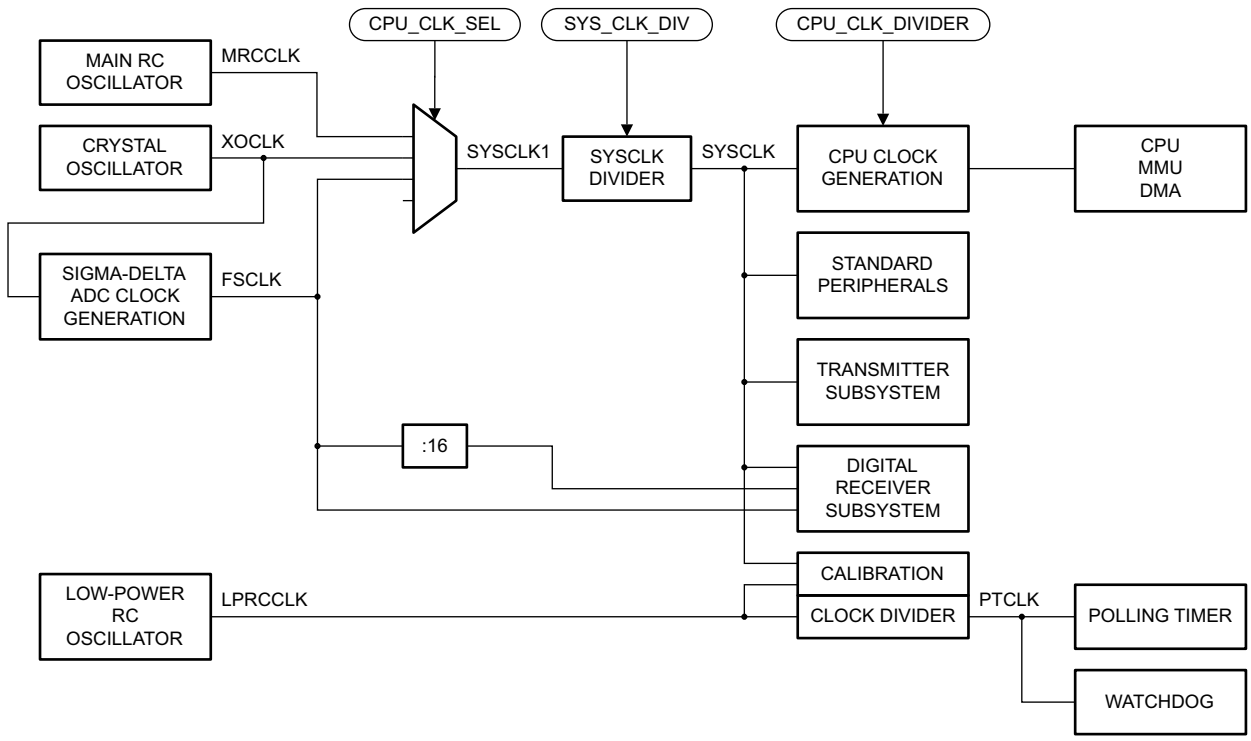


Fig 15. Clock distribution overview

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9.6.3 Direct Memory Access

The device supports direct memory access channels for different peripherals to unload the CPU from simple data copying tasks between the peripherals and the data memory. Besides these DMA channels the device also supports one general purpose DMA channel for block data transfer between any two data memory ranges.

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9.6.4 Interrupt system

The device contains an interrupt controller featuring 10 hardware interrupt priority levels. If more than one hardware interrupt request is pending at the same time the source with the highest request level is selected.

The application can switch dynamically between single or nested interrupt execution and whether a selected event causes an interrupt or a wake-up event. If an interrupt is enabled, it causes the RISC controller to perform a CALL operation to the interrupt vector address, where execution of the Interrupt Service Routine (ISR) starts.

User interrupts are usually disabled during the execution of system code (SYS instructions). In this case any interrupt request is latched and execution is delayed until control is returned to the application code. Please note that the system is basically able to allow user interrupts also during execution of system code. Any system call using this feature will describe this behavior explicitly.

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9.6.5 I/O ports

The device incorporates two quasi-identical I/O port structures—port 1 and port 2—with in total 12 independently configurable bidirectional pins. The I/O pins provide alternative port functions with individual control.

All I/O ports provide wake-up function and all but two have a battery buffered configurable wake-up edge selection (falling/rising) and wake-up disabling function.

Port 1 consists of 8 I/O pins, that serve the function to control external peripherals and that are used as button inputs (wake-up). Port 2 comprises 4 I/O pins, providing additional button inputs as well as various extended functions.

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9.6.6 Timer/Counter 0, 2

Timer/Counter 0 and Timer/Counter 2 are identical. The following description takes Timer/Counter 0 as reference. All descriptions are also valid for Timer/Counter 2 if T0 is replaced by T2 in names and figures.

Timer/Counter 0 is a 16 bit timer/counter with 12 bit prescaler and can be operated as interval and event counter, as digital modulator or as clock divider.

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9.6.7 Timer/Counter 1

Timer 1 is an 8/16 bit timer with 12 bit prescaler and is intended as interval and event counter for general purpose applications, as demodulator or signal generator and modulator. Together with Timer 0 it can be used as versatile clock measurement and/or trimming unit.

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9.6.8 Timer 3 and RX chain timers

Timer 3 is a general purpose timer. The receiver chain has an embedded timer of type Timer 3 which is called RX chain timer.

The RX chain timer is connected with RX state machine and can generate timeout events. It can be used for example to detect that a frame has not been received during an expected time window.

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9.6.9 Polling and wake-up timer

Features:

- Wake-up generation from POWER-OFF or STANDBY state
- Uses crystal calibrated divided low-power RC oscillator as clock source
- Configurable wake-up time generation from 1/16 ms to 65536 ms with 1/16 ms resolution
- Interrupt generation on wake-up time match
- Update of wake-up time from last device wake-up or from current time
- Polling timer register can be used as timestamp
- Interrupt generation on polling timer register overflow

The polling and wake-up timer can be used to terminate the POWER-OFF or STANDBY state after a predefined time but it can be also used in ACTIVE state to generate additional timer intervals.

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9.6.10 Watchdog timer

Features:

- Watchdog timer running in ACTIVE, STANDBY and POWER-OFF state 1
- Generates device reset, if not properly cleared by the application
- Uses crystal calibrated divided low-power RC oscillator as clock source
- Configurable wake-up time generation from 16 to 65536 ms in 13 steps
- Window watchdog operation with 25%, 50%, 75%, 100% clearing window
- Supports watchdog timer reset flag to detect watchdog overflow by the application
- Non-maskable watchdog timer interrupt instead of reset for devices in INIT mode

The device incorporates a watchdog timer to recover the system from application program deadlocks. The watchdog timer runs continuously in ACTIVE state, STANDBY state and POWER-OFF state 1 whereas it is off in RESET state and POWER-OFF state 2.

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9.6.11 USART

The USART is a universal synchronous and asynchronous receiver and transmitter featuring SPI, UART and LIN compatible UART operation. The device contains two identical USARTs denoted as USART0 and USART1. In the register description USART0 or USART1 must be used instead of the prefix USART.

9.6.11.1 Features:

- Integer and fractional baud rate generator
- Large range of selectable baud rates
- Two separate DMA channels for receive and transmit data

SPI

- Synchronous SPI operation
- SPI master and slave mode
- SPI clock polarity and clock phase selection
- SPI full and half duplex operation
- Configurable data length from 1 to 16 bits
- SPI mode fault and slave abort fault detection
- Hardware supported clock absent detection in slave mode to identify stalled SPI slave operation (4 … 255 bits)
- Full synchronous design, oversampling rate = 6, 8, 10 or 16
- SPI Stop bit to stop an ongoing SPI data transfer

UART

- Asynchronous UART operation
- Configurable parity generation (no, odd, even, sticky 0 or 1) and parity check
- 1 or 2 stop bits
- Configurable data length from 1 to 16 bits
- Full duplex and half duplex UART operation
- Half duplex operation with combined TRXD pin or separate RXD and TXD pin
- Half duplex operation with optional bit collision detection
- Optional selection to abort or continue transmission upon collision detection
- LIN compatible break detection mechanism on RXD line with configurable time-out window (4 … 255 bits)
- Frame error detection
- ISO7816 compatible operation mode
- Optional inversion of data bit

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9.6.12 Registers for mathematical- logical operations

9.6.12.1 CRC register

Features:

- Configurable CRC polynomial from CRC1 to CRC16
- Configurable CRC start value
- Parallel CRC calculation for 1 to 8 bit input data
- Support for LSBit/MSBit first and right/left aligned input data

The CRC register is intended for CRC generation and CRC checking tasks. It consists of a 16 bit CRC data register CRC_DAT and a configurable CRC polynomial, which can be set via register CRC_POLY.

9.6.12.2 CRC32 register

Features:

- Configurable CRC polynomial from CRC1 to CRC32
- Configurable CRC start value
- Parallel CRC calculation for 8 bit input data
- Support for LSBit/MSBit first aligned input data

The CRC register is intended for CRC generation and CRC checking tasks. It consists of a 32 bit CRC data register and a configurable CRC polynomial.

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9.6.13 Analog-to-digital converter (ADC)

The ADC is a 10 bit successive approximation analog to digital converter using charge redistribution techniques to achieve very low power consumption but also a high data conversion rate.

Features:

- 10 bit A-D conversion
- Selection between four input channels
- Selection between four reference voltages
- Power efficient and area saving switched capacitor charge tank
- Typical A-D conversion time of 37 µs
- Dynamic range up to the maximal supply level VDD_DIG
- Ratiometric measurement possible
- End-of-conversion and Data overflow flagging
- Interrupt generation for End-of-conversion

The ADC is configured and the resulting data can be read out via bit fields. It does not include multiple data buffering. Thus if previous conversion data was not read when a subsequent conversion is finished previous data will be overwritten which is flagged with an overflow flag.

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9.6.14 Temperature measurement

The temperature can be measured in two ways, either with the internal temperature sensor or using an external temperature sensor, connected to the on-chip 10 bit ADC.

9.6.14.1 External temperature measurement

An external temperature sensor can be used, connected as shown in Figure 16, with connections made to pins P21, P22 and P23.

The temperature measurement uses the calibration value for R2 stored in the variable ADC_R2 in EROM (see Section “Trim data”). The resistance value *RT* of the external temperature sensor is calculated according to Equation 1. The temperature can then be derived from the resistance value.

$$RT = \frac{RP + R2}{\frac{512}{\text{ADCDATA} - 511{,}5} - 1} \quad (1)$$

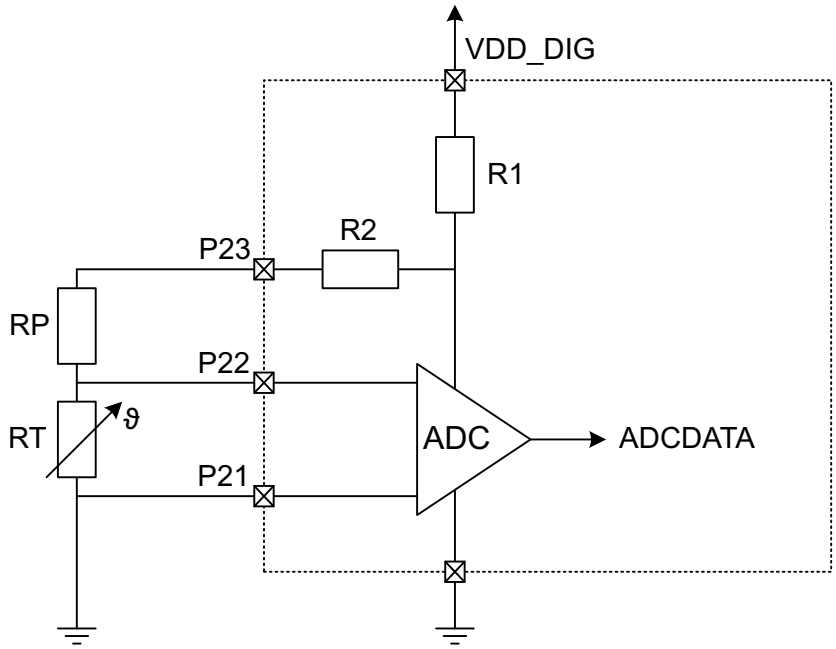


Fig 16. External temperature sensor measurement

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9.7 Device modes

The device features the following Device Modes:

- INIT
- PROTECTED
- TAMPERED
- VIRGIN

The Device Modes affect the overall device behavior, the Monitor and Download Interface operation and the user ability to access the EROM.

A Device Mode is controlled by a set of configuration bytes, which are located in the EROM.

The configuration bytes may not be altered by the user directly, instead, the corresponding Monitor and Download command has to be used.

9.7.1 INIT

When the device is supplied from NXP, it is configured in INIT mode by default.

The INIT mode shall be used during software development only. The Monitor and Download Interface is fully operational, enabling the customer to initialize the EROM as desired for the application.

To protect the EROM from readout and to disable the debug features, the device shall be forced into PROTECTED mode.

Leaving the device in INIT mode may cause the device to execute a software break, in case a corresponding debug command is received at pin MSDA. This would terminate execution of the application program and would call the built-in debug program. In this case, execution of the application program is interrupted until a proper debug command is issued or a device reset is applied.

9.7.2 PROTECTED

In the moment the device is set into PROTECTED mode, the EROM is protected against altering and readout via the Monitor and Download Interface, and the debug features are disabled. The PROTECTED mode has to be used during system testing and in the final application.

The device may be forced into INIT mode again by issuing a corresponding command via the Monitor and Download Interface. This command sets the EROM to a predefined state before the INIT mode is resumed. Hence, the EROM based application program is discarded. In case this sequence does not complete successfully, the device enters TAMPERED mode.

9.7.3 TAMPERED

The TAMPERED mode is entered temporarily during the sequence that forces the device from PROTECTED mode back into INIT mode. If this sequence does not complete successfully, the TAMPERED mode is entered.

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The device may be forced into INIT mode by again issuing a corresponding command via the Monitor and Download Interface. This command sets the EROM to a predefined state first, before the INIT mode is resumed. Hence, the EROM based application program is discarded. In case this sequence does not complete successfully, the device remains in TAMPERED mode until a new attempt is made.

9.7.4 VIRGIN

After manufacturing, the device operates in VIRGIN mode, enabling extended device test and device configuration. Finally, NXP forces the device into INIT mode and the VIRGIN mode is irreversibly locked in order to ensure it cannot be activated again.

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9.8 System routines

9.8.1 Boot routine

The ROM based boot routine is called immediately after a device reset or a wake-up from any POWER-OFF state. This event is referred to as cold boot.

The boot routine executes a sequence of instructions to evaluate the device mode and configures the device, using device protection and configuration flags and passes control to the application code at the warm boot vector in EROM.

The boot routine does not change the information and the bit fields about the wake-up events initiated by pressed buttons, polling timer or reset source.

9.8.2 Monitor and download interface

The in-circuit Monitor and Download Interface is intended for non intrusive debug operation during application program development. The interface allows manipulating the embedded peripherals and provides means to initialize the EROM. It is implemented as two-wire serial interface using the dedicated pins MSDA and MSCL. The EROM has a programming granularity of 64 byte.

The Monitor and Download Interface provides a 16 Bit Real Time Monitor containing Watches. Besides several HW/SW Break Points and single step operation, the interface contains an HW accelerator and allows autonomous operation.

The majority of the features provided by the Monitor and Download Interface are available only, if the device is set into INIT mode, which is the factory default setting. When performing system tests and field trials, the device shall be set to PROTECTED mode. Latter one locks the EROM content, protecting it against alteration and read out, as well as disables the debug features. The device may be forced back into INIT mode by a dedicated monitor command, which will set the EROM to a predefined state.

A detailed description about the operation and the command set of the Monitor and Download interface is given in Ref. 3.

9.8.3 Hardware abstraction layer

The device features functions located in ROM which are accessible using system calls. These are grouped in:

- Retrieving the version number of the device and its related firmware module versions.
- Debug functions which send customer defined data using the MDI interface
- Control of dedicated system debug functionality
- EROM programming function
- Low power functions to enable low power modes

Additionally, an EROM software library is available helping to control all hardware blocks. This can be seen as guidance and can be fully modified. The detailed information is available in a separate document.

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10. Characterization information

10.1 Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134)

Parameter	Condition	Min	Typ	Max	Unit
Storage temperature range		-55		150	°C
Junction temperature				150	°C
VDD_5VIN; VDD_IO; Voltage at any digital I/O pin		-0.3		5.5	V
Voltage at digital I/O pins (5.5 V must not be exceeded)		-0.3		VDD_IO + 0.3	V
VDD_DIG; VDD_RF; VDD_XO; VDD_LO; VDD_ADC; VDD_PA	Must not exceed VDD_IO	-0.3		3.6	V
Voltage difference between any of the following voltages: VDD_DIG; VDD_RF; VDD_XO; VDD_LO; VDD_ADC; VDD_PA				0.1	V
VREGPA		-0.3		2.0	V
TXOUT		-0.3		3.6	V
VDD_DIGL		-0.3		1.95	V
XTAL_N; XTAL_P		-0.3		1.95	V
IFN_SENSE_IN; IFP_DCBUS		-0.3		VDD_ADC	V
RF_IN_A; RF_IN_B; TRXSWITCH_RX; TRXSWITCH_ANT; TRXSWITCH_TX		-0.3		VDD_RF	V
Maximum RX input level without damage				10	dBm
EROM data retention	AEC-Q100-005 measurement method with mission profile as follows: 6 % @ -40 °C 20 % @ 30 °C 65 % @ 85 °C 5 % @ 100 °C 4 % @ 125 °C	15			Years
EROM write endurance[1]	T_{amb} = 25 °C	10k			cycles

[1] The activation energy equals 0.15 eV. According to Arrhennius' Law, the number of useful cycles at 25 °C is about 2.6 times higher than at 85 °C and about 4.3 times higher than at 125 °C.

10.2 Recommended operating conditions

Table 7. Recommended operating conditions

Parameter	Condition	Min	Typ	Max	Unit
Parametric ambient temperature	Unless otherwise specified	-40	25	85	°C

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Table 7. Recommended operating conditions

Parameter	Condition	Min	Typ	Max	Unit
Supply voltage range 1A	All specification parameters fulfilled	2.5	3	3.6	V
Supply voltage range 1B	Device fully functional; deviating RX and TX characteristics	1.9		2.5	V
Supply voltage range 2	Only on VDD_5VIN and VDD_IO. Full performance and IO operation on nominal 5 V supply	4.5	5	5.5	V

10.3 Characteristics

Table 8. RX Characteristics - General

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 870MHz, crystal = 27.6 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Frequency band 169 MHz		165		172	MHz	[1]
2	Frequency band 315 MHz		310		320	MHz	[1]
3	Frequency band 410 MHz		410		424	MHz	[1]
4	Frequency band 426/429/434/447 MHz		425		450	MHz	[1]
5	Frequency band 868 MHz		863		876	MHz	[1]
6	Frequency band 915 MHz		902		928	MHz	[1]
7	Frequency band 950 MHz		928		960	MHz	[1]
8	Frequency Step Size			53		Hz	[4]
9	Data latency Manchester / NRZ	Min. at 2.4 kchip/s and 10 kHz channel filter BW Max. at 225 kchip/s and 300 kHz channel filter BW	1.5		6.5	Chip	[4]
10	Sensitivity variation over baud rate deviation	Baud rate deviation ±1 %. Data rate 50 kbit/s, channel filter BW = 300 kHz		0.1	3	dB	[4]
11	Sensitivity variation over baud rate deviation	Baud rate deviation ±10 %. Data rate 50 kbit/s, channel filter BW = 300 kHz		1.5	3	dB	[4]
12	Maximum input level for reception	FER 10 %	5	10		dBm	[4]
13	Dynamic range of input	FER 10 % Channel filter BW = 10 kHz	125	130		dB	[4]
14	FSK sensitivity variation over temperature	-40 °C to 85 °C		2		dB	[4]
15	FSK sensitivity variation over supply voltage	2.5 V to 3.6 V		0.3		dB	[4]
16	FSK sensitivity variation over supply voltage	1.9 V to 3.6 V		1		dB	[4]

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Table 9. RX Characteristics - manchester receiver

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 870 MHz, crystal = 55.2 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	FSK sensitivity at input (FER 10 %) Manchester data rate = 50 kbit/s, deviation = ±100 kHz, channel filter BW = 300 kHz			-103	-101	dBm	[5]
2	ASK sensitivity at input (FER 10 %) Manchester data rate = 0.6 kbit/s, channel filter BW = 10 kHz. Peak envelope power ASK			-120	-117	dBm	[5]
3	ASK sensitivity at input (FER 10 %) Manchester data rate = 1.2 kbit/s, channel filter BW = 20 kHz. Peak envelope power ASK			-118	-115	dBm	[5]
4	ASK sensitivity at input (FER 10 %) Manchester data rate = 2.4 kbit/s, channel filter BW = 50 kHz. Peak envelope power ASK			-114	-111	dBm	[5]
5	ASK sensitivity at input (FER 10 %) Manchester data rate = 4.8 kbit/s, channel filter BW = 50 kHz. Peak envelope power ASK			-112	-110	dBm	[5]
6	Image frequency suppression without calibration RSSI at wanted frequency minus RSSI at image frequency			45		dB	[5]
7	Image frequency suppression with calibration (internal tone) at desired temperature / frequency RSSI at wanted frequency minus RSSI at image frequency		46	67		dB	[1]
8	Image frequency suppression with calibration (external tone) at desired frequency and 25 °C RSSI at wanted frequency minus RSSI at image frequency			72		dB	[5]
9	Spurious emission in RX mode: 9 kHz to 1 GHz	Conducted measurement at 50 Ohm reference board		-82	-70	dBm	[5]
10	Spurious emission in RX mode: 1 GHz to 4 GHz	Conducted measurement at 50 Ohm reference board		-78	-70	dBm	[5]

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Table 9. RX Characteristics - manchester receiver

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 870 MHz, crystal = 55.2 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
11	Spurious emission in RX mode within signal band in use	Conducted measurement at 50 Ohm reference board		-83	-70	dBm	[1]
12	Leakage LO	Tuned LO frequency. Conducted 50 Ohm		-83	-78	dBm	[1]
13	Leakage VCO	Tuned to VCO frequency. Conducted 50 Ohm		-70	-63	dBm	[1]
14	RSSI tolerance	One point calibration at -60 dBm, -120dBm to 0dBm, channel filter BW = 10 kHz	-3		3	dB	[5]
15	RSSI variance over temperature			0.3		dB	[5]
16	RSSI variance over voltage	1.9 V to 3.6 V		0.1		dB	[5]
17	Current consumption in STANDBY state	-40 °C		3	20	µA	[1]
		25 °C		4	20	µA	[1]
		85 °C		12	25	µA	[1]
18	Current consumption in POWER-OFF 2 state (polling timer and watchdog timer off)	-40 °C		0.6	1.5	µA	[1]
		25 °C		0.6	1.5	µA	[1]
		85 °C		2.5	5	µA	[1]
19	Current consumption in POWER-OFF 1 state (polling timer and watchdog timer on)	-40 °C		2	5	µA	[1]
		25 °C		2	5	µA	[1]
		85 °C		3	6	µA	[1]
20	Current consumption in RESET state	-40 °C		46	60	µA	[1]
		25 °C		52	60	µA	[1]
		85 °C		58	70	µA	[1]
21	Current consumption XTAL oscillator	NDK XTAL NX3225SA		450	600	µA	[2]
22	Current consumption in ACTIVE state	XTAL clock; System clock divided by 2 to be used. EROM execution					
		-40 °C		1.9	2.2	mA	[2]
		25 °C		2.0	2.5	mA	[2]
		85 °C		2.2	2.8	mA	[2]
23	Current consumption in ACTIVE state	RC clock; System clock divided by 2 to be used. EROM execution					
		-40 °C		1.3	1.6	mA	[2]
		25 °C		1.5	1.8	mA	[2]
		85 °C		1.7	2	mA	[2]
24	Delta of current consumption in ACTIVE state using system clock instead of system clock divided by 2.	EROM execution		0.1		mA	[2]

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Table 9. RX Characteristics - manchester receiver

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 870 MHz, crystal = 55.2 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
25	Delta of current consumption in ACTIVE state using system clock divided by 4	EROM execution		-0.1		mA	[2]
26	Current Consumption in idle mode	CPU idle; XTAL clock; System clock divided by 2 to be used. EROM execution					
		-40 °C		2	2.2	mA	[2]
		25 °C		2	2.4	mA	[2]
		85 °C		2.2	2.6	mA	[2]
27	Current Consumption in idle mode	CPU idle; RC clock; System clock divided by 2 to be used. EROM execution					
		-40 °C		1.0	1.3	mA	[2]
		25 °C		1.2	1.5	mA	[2]
		85 °C		1.4	1.7	mA	[2]
28	Delta of current consumption in IDLE mode using system clock instead of the system clock divided by 2.	EROM execution		0.4		mA	[2]
29	Delta of current consumption in IDLE mode using system clock instead of the system clock divided by 4.	EROM execution		0.2		mA	[2]
30	Receiver supply current for single channel Channel filter BW = 10 kHz	ACTIVE state; System clock divided by 2 to be used. EROM execution					
		-40°C		10	10.5	mA	[2]
		25 °C		10.5	11.5	mA	[2]
		85 °C		11.5	12	mA	[2]
31	Receiver supply current for single channel Channel filter BW = 300 kHz	ACTIVE state; System clock divided by 2 to be used. EROM execution					
		-40°C		8.9	11.5	mA	[2]
		25 °C		9.5	11.5	mA	[2]
		85 °C		10.1	12	mA	[2]
32	Analog start-up time from XTAL on to RX ready	From crystal regulator active to RX ready; NDK XTAL NX3225SA		270	450	µs	[2]
33	XTAL start-up time	From crystal regulator active to XTAL ready; NDK XTAL NX3225SA		150	200	µs	[2]

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Table 9. RX Characteristics - manchester receiver

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 870 MHz, crystal = 55.2 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
34	Time from power supply activation to start of EROM execution			1200		µs	[2]
35	Time from ACTIVE state to STANDBY state	System clock to be used.		23		µs	[2]
36	Time from STANDBY state to ACTIVE state	System clock is used.		230		µs	[2]
37	Temperature sensor tolerance	Calibrated at 30 °C.					
		-40 °C to 85 °C	-4		4	°C	[2]
38	Internal 5 V regulator output voltage available at VDD_3VOUT	VDD_5VIN = 5 V, 35 mA load current	2.5	3.1		V	[1]

Table 10. RX Characteristics - Wireless MBUS mode S

Following characteristics are valid for conditions as follows (unless otherwise specified)
2FSK modulation, frequency. deviation= 50kHz, manchester code, datarate = 32.768 kChip/s, Channel filter bandwidth = 360kHz, Frame Error Rate (FER) = 80%, payload length = 20 byte, crystal = 55.2 MHz
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 870MHz
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Sensitivity	-40 °C to 85 °C		-108	-100	dBm	[2]
2	Co-channel rejection	FSK jammer - same modulation as wanted.		2	5	dB	[5]
3	Co-channel rejection	CW jammer		2	5	dB	[5]
4	Adjacent channel rejection	Channel separation = 600 kHz, Channel filter BW = 360 kHz, jammer same modulation as wanted	45	50		dB	[5]
5	Adjacent channel rejection	Channel separation = 600 kHz, Channel filter BW = 360 kHz, jammer modulation CW	50	55		dB	[5]
6	Blocking	2 MHz	55	60		dB	[5]
7	Blocking	2 MHz (LBT)	55	60		dB	[5]
8	Blocking	6 MHz	60	65		dB	[5]
9	Blocking	10 MHz	65	70		dB	[5]
10	Blocking	10 MHz (LBT)	65	70		dB	[5]
11	Blocking	20 MHz	70	75		dB	[5]
12	Current consumption	System clock to be used.		12	13	mA	[2]
13	Current consumption	System clock divided by 2 to be used.		11	13	mA	[2]
14	Current consumption	System clock divided by 4 to be used.		11	12	mA	[2]

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Table 11. RX Characteristics - Wireless MBUS mode T1 (meter to other device)

Following characteristics are valid for conditions as follows (unless otherwise specified)
2FSK modulation, frequency deviation = 50kHz, 3 out of 6 code, data-rate = 100 kChips/s, Channel filter bandwidth = 360kHz, Frame Error Rate (FER) = 80%, payload length = 20 byte, crystal = 55.2 MHz.
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 870MHz
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Sensitivity	-40 °C to 85 °C		-105	-100	dBm	[2]
2	Co-channel rejection	FSK jammer - same modulation as wanted.		2	5	dB	[5]
3	Co-channel rejection	CW jammer		2	5	dB	[5]
4	Adjacent channel rejection	Channel separation = 600 kHz, Channel filter BW = 360 kHz, jammer same modulation as wanted	45	48		dB	[5]
5	Adjacent channel rejection	Channel separation = 600 kHz, Channel filter BW = 360 kHz, jammer modulation CW	50	55		dB	[5]
6	Blocking	2 MHz	55	60		dB	[5]
7	Blocking	2 MHz (LBT)	55	60		dB	[5]
8	Blocking	6 MHz	60	65		dB	[5]
9	Blocking	10 MHz	65	70		dB	[5]
10	Blocking	10 MHz (LBT)	65	70		dB	[5]
11	Blocking	20 MHz	70	75		dB	[5]
12	Current consumption	System clock to be used.		12.5	13.5	mA	[2]
13	Current consumption	System clock divided by 2 to be used.		12	13	mA	[2]
14	Current consumption	System clock divided by 4 to be used.		11.5	12.5	mA	[2]

Table 12. RX Characteristics - Wireless MBUS mode T2 (meter to other device)

Following characteristics are valid for conditions as follows (unless otherwise specified)
2FSK modulation, frequency deviation = 50kHz, manchester code, datarate = 100 kChips/s, Channel filter bandwidth = 360kHz, Frame Error Rate (FER) = 80%, payload length = 20 byte, crystal = 55.2 MHz.
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 870MHz
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Sensitivity	-40 °C to 85 °C		-108	-105	dBm	[2]
2	Co-channel rejection	FSK jammer - same modulation as wanted.		2	5	dB	[5]
3	Co-channel rejection	CW jammer		2	5	dB	[5]
4	Adjacent channel rejection	Channel separation = 600 kHz, Channel filter BW = 360 kHz, jammer same modulation as wanted	50	55		dB	[5]
5	Adjacent channel rejection	Channel separation = 600 kHz, Channel filter BW = 360 kHz, jammer modulation CW	50	55		dB	[5]

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Table 12. RX Characteristics - Wireless MBUS mode T2 (meter to other device)

Following characteristics are valid for conditions as follows (unless otherwise specified)
2FSK modulation, frequency deviation = 50kHz, manchester code, datarate = 100 kChips/s, Channel filter bandwidth = 360kHz, Frame Error Rate (FER) = 80%, payload length = 20 byte, crystal = 55.2 MHz.
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 870MHz
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
6	Blocking	2 MHz	55	60		dB	[5]
7	Blocking	2 MHz (LBT)	55	60		dB	[5]
8	Blocking	6 MHz	60	65		dB	[5]
9	Blocking	10 MHz	65	70		dB	[5]
10	Blocking	10 MHz (LBT)	65	70		dB	[5]
11	Blocking	20 MHz	70	75		dB	[5]
12	Current consumption	System clock to be used.		12.5	13.5	mA	[2]
13	Current consumption	System clock divided by 2 to be used.		12	13	mA	[2]
14	Current consumption	System clock divided by 4 to be used.		11.5	12.5	mA	[2]

Table 13. RX Characteristics - Wireless MBUS mode R2 channelised system (meter to other device)

Following characteristics are valid for conditions as follows (unless otherwise specified)
2FSK modulation, channel spacing 60kHz, frequency deviation = 6kHz, manchester code, datarate = 4.8 kChips/s, Channel filter bandwidth = 51kHz, Frame Error Rate (FER) = 80%, payload length = 20 byte, crystal = 55.2 MHz.
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 870MHz
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Sensitivity	-40 °C to 85 °C		-117	-112	dBm	[2]
2	Co-channel rejection	FSK jammer - same modulation as wanted.		2	2	dB	[5]
3	Co-channel rejection	CW jammer		2	2	dB	[5]
4	Adjacent channel rejection	Channel filter BW = 51 kHz, jammer same modulation as wanted. Channel separation = 60kHz, 120kHz, 300 kHz	48	52		dB	[5]
			50	58		dB	[5]
			58	62		dB	[5]
5	Adjacent channel rejection	Channel filter BW = 51 kHz, jammer modulation CW. Channel separation = 60kHz, 120kHz, 300 kHz	50	55		dB	[5]
			50	58		dB	[5]
			55	62		dB	[5]
6	Blocking	2 MHz	68	72		dB	[5]
7	Blocking	2 MHz (LBT)	68	72		dB	[5]
8	Blocking	6 MHz	75	80		dB	[5]
9	Blocking	10 MHz	75	82		dB	[5]
10	Blocking	10 MHz (LBT)	75	82		dB	[5]
11	Blocking	20 MHz	75	84		dB	[5]
12	Current consumption	System clock to be used.		12	13	mA	[2]
13	Current consumption	System clock divided by 2 to be used.		11	12	mA	[2]
14	Current consumption	System clock divided by 4 to be used.		11	11.5	mA	[2]

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Table 14. RX Characteristics - Wireless MBUS mode C1

Following characteristics are valid for conditions as follows (unless otherwise specified)
2FSK modulation, frequency deviation = 45kHz, NRZ, datarate = 100 kChips/s, Channel filter bandwidth = 240kHz, Frame Error Rate (FER) = 80%, payload length = 20 byte, crystal = 55.2 MHz.
T_{amb} = 25 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 870MHz
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Sensitivity	-40 °C to 85 °C		-105	-100	dBm	[2]
2	Co-channel rejection	FSK jammer - same modulation as wanted.		2	5	dB	[5]
3	Co-channel rejection	CW jammer		2	5	dB	[5]
4	Adjacent channel rejection	Channel filter BW = 240 kHz, jammer same modulation as wanted. Channel separation = 575 kHz	45	50		dB	[5]
5	Adjacent channel rejection	Channel filter BW = 240 kHz, jammer modulation CW. Channel separation = 575 kHz	50	55		dB	[5]
6	Blocking	2 MHz	55	60		dB	[5]
7	Blocking	2 MHz (LBT)	55	60		dB	[5]
8	Blocking	6 MHz	60	65		dB	[5]
9	Blocking	10 MHz	65	70		dB	[5]
10	Blocking	10 MHz (LBT)	65	70		dB	[5]
11	Blocking	20 MHz	70	75		dB	[5]
12	Current consumption	System clock to be used.		13	13.5	mA	[2]
13	Current consumption	System clock divided by 2 to be used.		12	13	mA	[2]
14	Current consumption	System clock divided by 4 to be used.		12	12.5	mA	[2]

Table 15. RX Characteristics - Wireless MBUS mode C2

Following characteristics are valid for conditions as follows (unless otherwise specified)
2GFSK modulation, BT = 0.5, frequency deviation = 25kHz, NRZ, datarate = 50kChips/s, Channel filter bandwidth = 180kHz, Frame Error Rate (FER) = 80%, payload length = 20 byte, crystal = 55.2 MHz.
T_{amb} = 25 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 870MHz
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Sensitivity	-40 °C to 85 °C		-108	-103	dBm	[2]
2	Co-channel rejection	GFSK jammer - same modulation as wanted.		2	5	dB	[5]
3	Co-channel rejection	CW jammer		2	5	dB	[5]
4	Adjacent channel rejection	Channel filter BW = 180 kHz, jammer same modulation as wanted. Channel separation = 575 kHz	50	55		dB	[5]

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Table 15. RX Characteristics - Wireless MBUS mode C2

Following characteristics are valid for conditions as follows (unless otherwise specified)
2GFSK modulation, BT = 0.5, frequency deviation = 25kHz, NRZ, datarate = 50kChips/s, Channel filter bandwidth = 180kHz, Frame Error Rate (FER) = 80%, payload length = 20 byte, crystal = 55.2 MHz.
T_{amb} = 25 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 870MHz
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
5	Adjacent channel rejection	Channel filter BW = 180 kHz, jammer modulation CW. Channel separation = 575 kHz	50	55		dB	[5]
6	Blocking	2 MHz	55	60		dB	[5]
7	Blocking	2 MHz (LBT)	55	60		dB	[5]
8	Blocking	6 MHz	60	65		dB	[5]
9	Blocking	10 MHz	65	70		dB	[5]
10	Blocking	10 MHz (LBT)	65	70		dB	[5]
11	Blocking	20 MHz	70	75		dB	[5]
12	Current consumption	System clock to be used.		12	13	mA	[2]
13	Current consumption	System clock divided by 2 to be used.		11.5	12.5	mA	[2]
14	Current consumption	System clock divided by 4 to be used.		11	12	mA	[2]

Table 16. RX Characteristics - Wireless MBUS mode N

Following characteristics are valid for conditions as follows (unless otherwise specified)
2GFSK modulation, h = 2.0, BT = 0.5, frequency deviation = 2.4 kHz, NRZ, data-rate = 2.4 kChips/s, Channel spacing = 12.5kHz, Channel filter bandwidth = 12kHz, Frame Error Rate (FER) = 80%, payload length = 20 byte, crystal = 55.2 MHz.
T_{amb} = 25 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 169.5MHz
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Sensitivity	-40 °C to 85 °C		-123	-117	dBm	[2]
2	Co-channel rejection	GFSK jammer - same modulation as wanted.		2	5	dB	[5]
3	Co-channel rejection	CW jammer		2	5	dB	[5]
4	Adjacent channel rejection	Channel filter BW = 12 kHz, jammer same modulation as wanted. Channel separation: 12.5 kHz, 25 kHz, 62.5 kHz.	16	18		dB	[5]
			60	67		dB	[5]
			60	65		dB	[5]
4	Adjacent channel rejection	Channel filter BW = 12 kHz, jammer modulation CW. Channel separation: 12.5 kHz, 25 kHz, 62.5 kHz..	45	50		dB	[5]
			60	65		dB	[5]
			60	65		dB	[5]
6	Blocking	2 MHz	75	78		dB	[5]
7	Blocking	2 MHz (LBT)	75	78		dB	[5]
8	Blocking	6 MHz	80	85		dB	[5]
9	Blocking	10 MHz	80	85		dB	[5]
10	Blocking	10 MHz (LBT)	80	85		dB	[5]
11	Blocking	20 MHz	80	85		dB	[5]

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Table 16. RX Characteristics - Wireless MBUS mode N

Following characteristics are valid for conditions as follows (unless otherwise specified)
2GFSK modulation, h = 2.0, BT = 0.5, frequency deviation = 2.4 kHz, NRZ, data-rate = 2.4 kChips/s, Channel spacing = 12.5kHz, Channel filter bandwidth = 12kHz, Frame Error Rate (FER) = 80%, payload length = 20 byte, crystal = 55.2 MHz.
T_{amb} = 25 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 169.5MHz
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
12	Current consumption	System clock to be used.		11	11.5	mA	[2]
13	Current consumption	System clock divided by 2 to be used.		10	11	mA	[2]
14	Current consumption	System clock divided by 4 to be used.		9.5	10.5	mA	[2]

Table 17. RX Characteristics - Wireless MBUS mode F

Following characteristics are valid for conditions as follows (unless otherwise specified)
2FSK modulation, frequency deviation = 5.5 kHz, NRZ, data-rate = 2.4 kChips/s, Channel spacing = 50kHz, Channel filter bandwidth = 24 kHz, Frame Error Rate (FER) = 80%, payload length = 20 byte, crystal = 55.2 MHz.
T_{amb} = 25 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 434 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Sensitivity	-40 °C to 85 °C		-117	-114	dBm	[2]
2	Co-channel rejection	GFSK jammer - same modulation as wanted.		2	5	dB	[5]
3	Co-channel rejection	CW jammer		2	5	dB	[5]
4	Adjacent channel rejection	Channel filter BW = 24 kHz, jammer same modulation as wanted. Channel separation: 870 kHz	65	70		dB	[5]
5	Adjacent channel rejection	Channel filter BW = 24 kHz, jammer modulation CW. Channel separation: 870 kHz	65	70		dB	[5]
6	Blocking	2 MHz	70	75		dB	[5]
7	Blocking	2 MHz (LBT)	70	75		dB	[5]
8	Blocking	6 MHz	75	80		dB	[5]
9	Blocking	10 MHz	75	80		dB	[5]
10	Blocking	10 MHz (LBT)	80	85		dB	[5]
11	Blocking	20 MHz	80	85		dB	[5]
12	Current consumption	System clock to be used.		11	12	mA	[2]
13	Current consumption	System clock divided by 2 to be used.		10.5	11.5	mA	[2]
14	Current consumption	System clock divided by 4 to be used.		10	11	mA	[2]

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Table 18. RX Characteristics - Zigbee 868

Following characteristics are valid for conditions as follows (unless otherwise specified)
2GFSK modulation, h = 0.7, BT = 0.5, frequency deviation = 35 kHz, NRZ, data-rate = 100 kChips/s, Channel spacing = 200 kHz, Channel filter bandwidth = 200 kHz, Frame Error Rate (FER) = 80%, payload length = 20 byte crystal = 55.2 MHz.
T_{amb} = 25 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 434 MHz,
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Sensitivity	-40 °C to 85 °C		-104	-100	dBm	[2]
2	Co-channel rejection	2GFSK jammer - same modulation as wanted.		8	12	dB	[5]
3	Co-channel rejection	CW jammer		6	10	dB	[5]
4	Adjacent channel rejection	Channel filter BW = 200 kHz, jammer same modulation as wanted. Channel separation: 200 kHz, 400 kHz, 1000 kHz	25	28		dB	[5]
			45	50		dB	[5]
			50	55		dB	[5]
4	Adjacent channel rejection	Channel filter BW = 200 kHz, jammer modulation CW. Channel separation: 200 kHz, 400 kHz, 1000 kHz	40	45		dB	[5]
			45	50		dB	[5]
			50	55		dB	[5]
6	Blocking	2 MHz	55	60		dB	[5]
7	Blocking	2 MHz (LBT)	55	60		dB	[5]
8	Blocking	6 MHz	60	65		dB	[5]
9	Blocking	10 MHz	60	65		dB	[5]
10	Blocking	10 MHz (LBT)	65	70		dB	[5]
11	Blocking	20 MHz	65	70		dB	[5]
12	Current consumption	System clock to be used.		14	15	mA	[2]
13	Current consumption	System clock divided by 2 to be used.		13.5	14.5	mA	[2]
14	Current consumption	System clock divided by 4 to be used.		13	13.5	mA	[2]

Table 19. RX Characteristics - SigFox

Following characteristics are valid for conditions as follows (unless otherwise specified)
2GFSK modulation, h = 2.67, BT = 1.0, NRZ, data-rate = 0.6 kChips/s, Channel spacing = 10 kHz, Channel filter bandwidth = 10 kHz, Frame Error Rate (FER) = 20%, payload length = 228 byte, crystal = 55.2 MHz.
T_{amb} = 25 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 870 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Sensitivity	-40 °C to 85 °C		-124	-119	dBm	[2]
2	Co-channel rejection	2GFSK jammer - same modulation as wanted.		2	5	dB	[5)
3	Co-channel rejection	CW jammer		2	5	dB	[5]
4	Adjacent channel rejection	Channel filter BW = 10 kHz, jammer same modulation as wanted. Channel separation: 10 kHz, 20 kHz, 150 kHz.	50	55		dB	[5]
			55	60		dB	[5]
			60	65		dB	[5]

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Table 19. RX Characteristics - SigFox

Following characteristics are valid for conditions as follows (unless otherwise specified)
2GFSK modulation, h = 2.67, BT = 1.0, NRZ, data-rate = 0.6 kChips/s, Channel spacing = 10 kHz, Channel filter bandwidth = 10 kHz, Frame Error Rate (FER) = 20%, payload length = 228 byte, crystal = 55.2 MHz.
T_{amb} = 25 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 870 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
5	Adjacent channel rejection	Channel filter BW = 10 kHz, jammer modulation CW. Channel separation: 10 kHz, 20 kHz, 150 kHz.	50	55		dB	[5]
			55	60		dB	[5]
			60	65		dB	[5]
6	Blocking	2 MHz	70	75		dB	[5]
7	Blocking	2 MHz (LBT)	75	80		dB	[5]
8	Blocking	6 MHz	80	85		dB	[5]
9	Blocking	10 MHz	85	90		dB	[5]
10	Blocking	10 MHz (LBT)	85	90		dB	[5]
11	Blocking	20 MHz	85	90		dB	[5]
12	Current consumption	System clock to be used.		13.5	14.5	mA	[2]
13	Current consumption	System clock divided by 2 to be used.		13	13.5	mA	[2]
14	Current consumption	System clock divided by 4 to be used.		12.5	13	mA	[2]

Table 20. RX Characteristics - Narrowband 400MHz application

Following characteristics are valid for conditions as follows (unless otherwise specified)
2GFSK modulation, h = 0.5, BT = 0.5, NRZ, data-rate = 5 kChips/s, Channel spacing = 25kHz, Channel filter bandwidth = 25kHz, Frame Error Rate (FER) = 20%, payload length = 28 byte, crystal = 55.2 MHz.
T_{amb} = 25 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 423MHz
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Sensitivity	-40 °C to 85 °C		-116	-110	dBm	[2]
2	Co-channel rejection	2GFSK jammer - same modulation as wanted.		7	10	dB	[5]
3	Co-channel rejection	CW jammer		2	8	dB	[5]
4	Adjacent channel rejection	Channel filter BW = 25 kHz, jammer same modulation as wanted. Channel separation: 25 kHz, 50 kHz, 125 kHz	50	55		dB	[5]
			55	60		dB	[5]
			60	65		dB	[5]
5	Adjacent channel rejection	Channel filter BW = 25 kHz, jammer modulation CW. Channel separation: 25 kHz, 50 kHz, 125 kHz	50	55		dB	[5]
			55	60		dB	[5]
			60	65		dB	[5]
6	Blocking	2 MHz	70	75		dB	[5]
7	Blocking	2 MHz (LBT)	70	75		dB	[5]
8	Blocking	6 MHz	75	80		dB	[5]
9	Blocking	10 MHz	80	85		dB	[5]
10	Blocking	10 MHz (LBT)	80	85		dB	[5]

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Table 20. RX Characteristics - Narrowband 400MHz application

Following characteristics are valid for conditions as follows (unless otherwise specified)
2GFSK modulation, h = 0.5, BT = 0.5, NRZ, data-rate = 5 kChips/s, Channel spacing = 25kHz, Channel filter bandwidth = 25kHz, Frame Error Rate (FER) = 20%, payload length = 28 byte, crystal = 55.2 MHz.
T_{amb} = 25 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 423MHz
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
11	Blocking	20 MHz	80	85		dB	[5]
12	Current consumption	System clock to be used.		14.5	15.5	mA	[2]
13	Current consumption	System clock divided by 2 to be used.		13.5	14.5	mA	[2]
14	Current consumption	System clock divided by 4 to be used.		13	14	mA	[2]

Table 21. RX Characteristics - Narrowband 400MHz application

Following characteristics are valid for conditions as follows (unless otherwise specified)
4GFSK modulation, h = 0.5, BT = 0.5, NRZ, data-rate = 10 kChips/s, Channel spacing = 25kHz, Channel filter bandwidth = 25kHz, Frame Error Rate (FER) = 20%, payload length = 28 byte, crystal = 55.2 MHz.
T_{amb} = 25 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 423MHz
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Sensitivity	-40 °C to 85 °C		-115	-110	dBm	[2]
2	Co-channel rejection	2GFSK jammer - same modulation as wanted.		6	10	dB	[5]
3	Co-channel rejection	CW jammer		8	12	dB	[5]
4	Adjacent channel rejection	Channel filter BW = 25 kHz, jammer same modulation as wanted. Channel separation: 25 kHz, 50 kHz, 125 kHz	50	55		dB	[5]
			55	60		dB	[5]
			60	65		dB	[5]
5	Adjacent channel rejection	Channel filter BW = 25 kHz, jammer modulation CW. Channel separation: 25 kHz, 50 kHz, 125 kHz	50	55		dB	[5]
			55	60		dB	[5]
			60	65		dB	[5]
6	Blocking	2 MHz	70	75		dB	[5]
7	Blocking	2 MHz (LBT)	70	75		dB	[5]
8	Blocking	6 MHz	75	80		dB	[5]
9	Blocking	10 MHz	80	85		dB	[5]
10	Blocking	10 MHz (LBT)	80	85		dB	[5]
11	Blocking	20 MHz	80	85		dB	[5]
12	Current consumption	System clock to be used.		14.5	15.5	mA	[2]
13	Current consumption	System clock divided by 2 to be used.		13.5	14.5	mA	[2]
14	Current consumption	System clock divided by 4 to be used.		13	14	mA	[2]

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Table 22. RX Characteristics - Narrowband 400MHz application

Following characteristics are valid for conditions as follows (unless otherwise specified)
8GFSK modulation, h = 0.5, BT = 0.5, NRZ, data-rate = 15 kChips/s, Channel spacing = 50kHz, Channel filter bandwidth = 50kHz, Frame Error Rate (FER) = 20%, payload length = 28 byte, crystal = 55.2 MHz.
T_{amb} = 25 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 423MHz
VDD = VDD_IO, VDD_DIG, VDD_XO, VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Sensitivity	-40 °C to 85 °C		-113	-108	dBm	[2]
2	Co-channel rejection	2GFSK jammer - same modulation as wanted.		6	10	dB	[5]
3	Co-channel rejection	CW jammer		8	12	dB	[5]
4	Adjacent channel rejection	Channel filter BW = 50 kHz, jammer same modulation as wanted. Channel separation: 50 kHz, 100 kHz, 250 kHz	50	55		dB	[5]
			55	60		dB	[5]
			60	65		dB	[5]
5	Adjacent channel rejection	Channel filter BW = 50 kHz, jammer modulation CW. Channel separation: 50 kHz, 100 kHz, 250 kHz	50	55		dB	[5]
			55	60		dB	[5]
			60	65		dB	[5]
6	Blocking	2 MHz	65	70		dB	[5]
7	Blocking	2 MHz (LBT)	65	70		dB	[5]
8	Blocking	6 MHz	70	75		dB	[5]
9	Blocking	10 MHz	75	80		dB	[5]
10	Blocking	10 MHz (LBT)	75	80		dB	[5]
11	Blocking	20 MHz	75	80		dB	[5]
12	Current consumption	System clock to be used.		13.5	15	mA	[2]
13	Current consumption	System clock divided by 2 to be used.		13.5	14.5	mA	[2]
14	Current consumption	System clock divided by 4 to be used.		13	14	mA	[2]

Table 23. TX Characteristics

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 870 MHz, crystal = 55.2 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO_VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Analog start-up time from XTAL on to TX ready	From crystal LDO regulator active to TX ready; NDK XTAL NX3225SA		250		us	[2]
2	Maximum output power, CW mode, L-front matching		13	14.		dBm	[2]
3	Minimum output power, CW mode, L-front matching			-28	-22	dBm	[2]
4	Variation of maximum output power over temperature, CW mode, L-front matching	3.0 V				dB	
		-40 °C to 25 °C		0.3	1.0	dB	[2]
		25 °C to 85 °C		0.3	1.0	dB	[2]

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Table 23. TX Characteristics

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 870 MHz, crystal = 55.2 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO_VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
5	Variation of maximum output power over supply voltage, CW mode, L-front matching	25 °C 2.5V to 3.6V		0.1	0.5		
		25 °C 1.9 V to 3.6 V		0.8	3.0	dB	[2]
6	PA output power steps,			0.25	0.5	dB	[2]
7	2nd harmonic, at maximum output power	Conducted measurement at 50 Ohm		-40	-36	dBm	[2]
8	3rd harmonic, at maximum output power	Conducted measurement at 50 Ohm		-60	-50	dBm	[2]
9	Spurious emission, at maximum output power	Conducted measurement at 50 Ohm reference, 47 MHz to 230 MHz and 470 MHz to 862 MHz		-80	-70	dBm	[2]
10	Spurious emission, at maximum output power	Conducted measurement at 50 Ohm Other frequencies below 1 GHz		-73	-65	dBm	[2]
11	Spurious emission, at maximum output power	Conducted measurement at 50 Ohm 1 GHz to 12.5 GHz		-73	-53	dBm	[2]
12	Out of band TX noise at 12.5 kHz offsets, CW mode	868 MHz band		-100	-90	dBc/Hz	[2]
13	Out of band TX noise at 25 kHz offsets, CW mode	868 MHz band		-102	-95	dBc/Hz	[2]
14	Out of band TX noise at 100 kHz offset, CW mode	868 MHz band		-105	-100	dBc/Hz	[2]
15	Out of band TX noise at 1 MHz offset, CW mode	868 MHz band		-125	-120	dBc/Hz	[2]
16	Adjacent channel power	GFSK, BT = 0.5, h = 1, channel spacing = 12.5 kHz, symbol rate = 3 kBaud, modulation with PN9 sequence		-58		dBc	[2]
17	Adjacent channel power	GFSK, BT = 0.5, h = 1, channel spacing = 25 kHz, symbol rate = 6 kBaud, modulation with PN9 sequence		-56		dBc	[2]
18	Adjacent channel power	GFSK, BT = 0.5, h = 1, channel spacing = 50 kHz, symbol rate = 6 kBaud, modulation with PN9 sequence		-56		dBc	[2]
19	Adjacent channel power	GFSK, BT = 0.5, h = 1, channel spacing = 300 kHz, symbol rate = 6 kBaud, modulation with PN9 sequence		-60		dBc	[2]

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Table 23. TX Characteristics

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 870 MHz, crystal = 55.2 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO_VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
20	99.5 % occupied bandwidth	GFSK, BT = 0.5, Manchester data rate = 1.2 kbit/s, frequency deviation = ±2.0 kHz		5	6	kHz	[2]
21	99.5 % occupied bandwidth	GFSK, BT = 0.5, Manchester data rate = 2.4 kbit/s, frequency deviation = ±2.4 kHz		8	12	kHz	[2]
22	99.5 % occupied bandwidth	GFSK, BT = 0.5, Manchester data rate = 4.8 kbit/s, frequency deviation = ±4.8 kHz		15	20	kHz	[2]
23	99.5 % occupied bandwidth	GFSK, BT = 0.5, Manchester data rate = 50 kbit/s, frequency deviation = ±50 kHz		155	170	kHz	[2]
24	TX supply current at maximum output power	System clock divided by 2 to be used. EROM execution		30	33	mA	[2]
25	Variation over Temperature of TX Supply Current at maximum Output Power 14 dBm	System clock divided by 2 to be used. EROM execution;		0.5		mA	[2]
26	Variation over Voltage of TX Supply Current at maximum Output Power 14 dBm (1.9 V - 3.6 V)	System clock divided by 2 to be used. EROM execution;		3.0		mA	[2]
27	Out of band tx noise @ 200kHz	Application: zigbee Band: 870MHz using channel filter = 10kHz		-112	-108	dBc/Hz	[2]
28	Out of band tx noise @ 400kHz	Application: zigbee Band: 870MHz using channel filter = 10kHz		-118	-113	dBc/Hz	[2]
29	Out of band tx noise @ 100kHz	Application: zigbee Band: 870MHz using channel filter = 10kHz		-127	-125	dBc/Hz	[2]
30	Out of band tx noise @ 10000kHz	Application: zigbee Band: 870MHz using channel filter = 10kHz		-138	-135	dBc/Hz	[2]
31	Out of band tx noise @ 60kHz	Application: wmbus Band: 870 using channel filter = 10kHz		-104	-99	dBc/Hz	[2]
32	Out of band tx noise @ 360kHz	Application: wmbus Band: 870 using channel filter = 10kHz		-115	-112	dBc/Hz	[2]

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Table 23. TX Characteristics

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 870 MHz, crystal = 55.2 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO_VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
33	Out of band tx noise @ 6000kHz	Application: wmbus Band: 870 using channel filter = 10kHz		-130	-125	dBc/Hz	[2]
34	Out of band tx noise @ 10000kHz	Application: wmbus Band: 870 using channel filter = 10kHz		-135	-130	dBc/Hz	[2]
35	ADJACENT CHANNEL POWER, 870 MHz band, SigFox :	2GFSK, h=2.67, BT=1.0, Channel spacing 10kHz, 0.6kChip/s		-60		dBc	[2]
36	Occupied bandwidth, 870 MHz band, SigFox	2GFSK, h=2.67, BT=1.0, Channel spacing 10kHz, 0.6kChip/s		4	5	kHz	[2]

Table 24. TX Characteristics

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 169MHz, crystal = 55.2 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO_VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Analog start-up time from XTAL on to TX ready	From crystal LDO regulator active to TX ready; NDK XTAL NX3225SA		250		us	[2]
2	Maximum output power, CW mode, L-front matching		13	14.		dBm	[2]
3	Minimum output power, CW mode, L-front matching			-31	-22	dBm	[2]
4	Variation of maximum output power over temperature, CW mode, L-front matching	3.0 V				dB	
		-40 °C to 25 °C		0.3	1.0	dB	[2]
		25 °C to 85 °C		0.3	1.0	dB	[2]
5	Variation of maximum output power over supply voltage, CW mode, L-front matching	25 °C 2.5V to 3.6V		0.1	0.5		
		25 °C 1.9 V to 3.6 V		0.8	3.0	dB	[2]
6	PA output power steps,			0.25	0.5	dB	[2]
7	2nd harmonic, at maximum output power	Conducted measurement at 50 Ohm		-51	-36	dBm	[2]
8	3rd harmonic, at maximum output power	Conducted measurement at 50 Ohm		-65	-30	dBm	[2]
9	Spurious emission, at maximum output power	Conducted measurement at 50 Ohm reference, 47 MHz to 230 MHz and 470 MHz to 862 MHz		-80	-74	dBm	[2]
10	Spurious emission, at maximum output power	Conducted measurement at 50 Ohm Other frequencies below 1 GHz		-78	-70	dBm	[2]

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Table 24. TX Characteristics

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 169MHz, crystal = 55.2 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO_VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
11	Spurious emission, at maximum output power	Conducted measurement at 50 Ohm 1 GHz to 12.5 GHz		-78	-70	dBm	[2]
12	Out of band TX noise at 12.5 kHz offsets, CW mode	169 MHz band		-114	-105	dBc/Hz	[2]
13	Out of band TX noise at 25 kHz offsets, CW mode	169 MHz band		-114	-105	dBc/Hz	[2]
14	Out of band TX noise at 100 kHz offset, CW mode	169 MHz band		-118	-110	dBc/Hz	[2]
15	Out of band TX noise at 1 MHz offset, CW mode	169 MHz band		-135	-125	dBc/Hz	[2]
16	Adjacent channel power	GFSK, BT = 0.5, h = 1, channel spacing = 12.5 kHz, symbol rate = 3 kBaud, modulation with PN9 sequence		-70		dBc	[2]
17	Adjacent channel power	GFSK, BT = 0.5, h = 1, channel spacing = 25 kHz, symbol rate = 6 kBaud, modulation with PN9 sequence		-65		dBc	[2]
18	Adjacent channel power	GFSK, BT = 0.5, h = 1, channel spacing = 50 kHz, symbol rate = 6 kBaud, modulation with PN9 sequence		-70		dBc	[2]
19	Adjacent channel power	GFSK, BT = 0.5, h = 1, channel spacing = 300 kHz, symbol rate = 6 kBaud, modulation with PN9 sequence		-68		dBc	[2]
20	99.5 % occupied bandwidth	GFSK, BT = 0.5, Manchester data rate = 1.2 kbit/s, frequency deviation = ±2.0 kHz		3.8	5	kHz	[2]
21	99.5 % occupied bandwidth	GFSK, BT = 0.5, Manchester data rate = 2.4 kbit/s, frequency deviation = ±2.4 kHz		5.3	8	kHz	[2]
22	99.5 % occupied bandwidth	GFSK, BT = 0.5, Manchester data rate = 4.8 kbit/s, frequency deviation = ±4.8 kHz		10	15	kHz	[2]
23	99.5 % occupied bandwidth	GFSK, BT = 0.5, Manchester data rate = 50 kbit/s, frequency deviation = ±50 kHz		100	120	kHz	[2]

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Table 24. TX Characteristics

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 169MHz, crystal = 55.2 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO_VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
24	TX supply current at maximum output power	System clock divided by 2 to be used. EROM execution		32	40	mA	[2]
25	Variation over Temperature of TX Supply Current at maximum Output Power 14 dBm	System clock divided by 2 to be used. EROM execution;		0.5		mA	[2]
26	Variation over Voltage of TX Supply Current at maximum Output Power 14 dBm (1.9 V - 3.6 V)	System clock divided by 2 to be used. EROM execution;		3.0		mA	[2]
27	Out of band tx noise @ 12.5kHz	Application: wmbus Band: 170MHz using channel filter = 10kHz		-115	-103	dBc/Hz	[2]
28	Out of band tx noise @ 37.5kHz	Application: wmbus Band: 170MHz using channel filter = 10kHz		-115	-110	dBc/Hz	[2]
29	Out of band tx noise @ 50kHz	Application: wmbus Band: 170MHz using channel filter = 10kHz		-115	-110	dBc/Hz	[2]
30	Out of band tx noise @ 4500kHz	Application: wmbus Band: 170MHz using channel filter = 10kHz		-136	-131	dBc/Hz	[2]
31	ADJACENT CHANNEL POWER, 169 MHz band, Wireless MBus - Mode N, 15.4g	2GFSK, h=2.0, BT=0.5, Channel spacing 12.5kHz, freq. dev. 2.4kHz, NRZ, 2.4kChip/s		-64		dBc	[2]
32	Occupied bandwidth, 169 MHz band, Wireless MBus - Mode N, 15.4g	2GFSK, h=2.0, BT=0.5, Channel spacing 12.5kHz, freq. dev. 2.4kHz, NRZ, 2.4kChip/s		7.7	9	kHz	[2]

Table 25. TX Characteristics

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 413MHz, crystal = 55.2 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO_VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Analog start-up time from XTAL on to TX ready	From crystal LDO regulator active to TX ready; NDK XTAL NX3225SA		250		us	[2]
2	Maximum output power, CW mode, L-front matching		13	14.		dBm	[2]
3	Minimum output power, CW mode, L-front matching			-30	-22	dBm	[2]

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Table 25. TX Characteristics

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 413MHz, crystal = 55.2 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO_VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
4	Variation of maximum output power over temperature, CW mode, L-front matching	3.0 V				dB	
		-40 °C to 25 °C		0.3	1.0	dB	[2]
		25 °C to 85 °C		0.3	1.0	dB	[2]
5	Variation of maximum output power over supply voltage, CW mode, L-front matching	25 °C 2.5V to 3.6V		0.1	0.5		
		25 °C 1.9 V to 3.6 V		0.8	3.0	dB	[2]
6	PA output power steps,			0.25	0.5	dB	[2]
7	2nd harmonic, at maximum output power	Conducted measurement at 50 Ohm		-55	-50	dBm	[2]
8	3rd harmonic, at maximum output power	Conducted measurement at 50 Ohm		-45	-40	dBm	[2]
9	Spurious emission, at maximum output power	Conducted measurement at 50 Ohm reference, 47 MHz to 230 MHz and 470 MHz to 862 MHz		-80	-70	dBm	[2]
10	Spurious emission, at maximum output power	Conducted measurement at 50 Ohm Other frequencies below 1 GHz		-70	-60	dBm	[2]
11	Spurious emission, at maximum output power	Conducted measurement at 50 Ohm 1 GHz to 12.5 GHz		-78	-60	dBm	[2]
12	Out of band TX noise at 12.5 kHz offsets, CW mode	169 MHz band		-110	-100	dBc/Hz	[2]
13	Out of band TX noise at 25 kHz offsets, CW mode	169 MHz band		-110	-100	dBc/Hz	[2]
14	Out of band TX noise at 100 kHz offset, CW mode	169 MHz band		-113	-105	dBc/Hz	[2]
15	Out of band TX noise at 1 MHz offset, CW mode	169 MHz band		-130	-125	dBc/Hz	[2]
16	Adjacent channel power	GFSK, BT = 0.5, h = 1, channel spacing = 12.5 kHz, symbol rate = 3 kBaud, modulation with PN9 sequence		-66		dBc	[2]
17	Adjacent channel power	GFSK, BT = 0.5, h = 1, channel spacing = 25 kHz, symbol rate = 6 kBaud, modulation with PN9 sequence		-65		dBc	[2]
18	Adjacent channel power	GFSK, BT = 0.5, h = 1, channel spacing = 50 kHz, symbol rate = 6 kBaud, modulation with PN9 sequence		-63		dBc	[2]

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Table 25. TX Characteristics

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 413MHz, crystal = 55.2 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO_VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
19	Adjacent channel power	GFSK, BT = 0.5, h = 1, channel spacing = 300 kHz, symbol rate = 6 kBaud, modulation with PN9 sequence		-60		dBc	[2]
20	99.5 % occupied bandwidth	GFSK, BT = 0.5, Manchester data rate = 1.2 kbit/s, frequency deviation = ±2.0 kHz		5.3	8	kHz	[2]
21	99.5 % occupied bandwidth	GFSK, BT = 0.5, Manchester data rate = 2.4 kbit/s, frequency deviation = ±2.4 kHz		7.8	9	kHz	[2]
22	99.5 % occupied bandwidth	GFSK, BT = 0.5, Manchester data rate = 4.8 kbit/s, frequency deviation = ±4.8 kHz		15	18	kHz	[2]
23	99.5 % occupied bandwidth	GFSK, BT = 0.5, Manchester data rate = 50 kbit/s, frequency deviation = ±50 kHz		154	180	kHz	[2]
24	TX supply current at maximum output power	System clock divided by 2 to be used. EROM execution		33	38	mA	[2]
25	Variation over Temperature of TX Supply Current at maximum Output Power 14 dBm	System clock divided by 2 to be used. EROM execution;		0.5		mA	[2]
26	Variation over Voltage of TX Supply Current at maximum Output Power 14 dBm (1.9 V - 3.6 V)	System clock divided by 2 to be used. EROM execution;		3.0		mA	[2]
27	Out of band tx noise @ 12.5kHz	Application: sensus Band: 413MHz using channel filter = 10kHz		-110	-100	dBc/Hz	[2]
28	Out of band tx noise @ 25kHz	Application: sensus Band: 413MHz using channel filter = 10kHz		-110	-100	dBc/Hz	[2]
29	Out of band tx noise @ 100kHz	Application: sensus Band: 413MHz using channel filter = 10kHz		-116	-110	dBc/Hz	[2]
29	Out of band tx noise @ 2000kHz	Application: sensus Band: 413MHz using channel filter = 10kHz		-135	-128	dBc/Hz	[2]

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Table 25. TX Characteristics

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 413MHz, crystal = 55.2 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO_VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
30	Out of band tx noise @ 10000kHz	Application: sensus Band: 413MHz using channel filter = 10kHz		-140	-132	dBc/Hz	[2]
31	ADJACENT CHANNEL POWER, 412 MHz band, Sensus	4GFSK, h=0.5, BT=0.5, Channel spacing 25kHz, 5kChip/s		-65		dBc	[2]
32	Occupied bandwidth, 412 MHz band, Sensus	4GFSK, h=0.5, BT=0.5, Channel spacing 25kHz, 5kChip/s		11.3	13	kHz	[2]

Table 26. TX Characteristics

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 434MHz, crystal = 55.2 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO_VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Analog start-up time from XTAL on to TX ready	From crystal LDO regulator active to TX ready; NDK XTAL NX3225SA		250		us	[2]
2	Maximum output power, CW mode, L-front matching		12.5	14		dBm	[2]
3	Minimum output power, CW mode, L-front matching			-31	-25	dBm	[2]
4	Variation of maximum output power over temperature, CW mode, L-front matching	3.0 V				dB	
		-40 °C to 25 °C		0.3	1.5	dB	[2]
		25 °C to 85 °C		0.3	1.2	dB	[2]
5	Variation of maximum output power over supply voltage, CW mode, L-front matching	25 °C 2.5V to 3.6V		0.1	0.5		
		25 °C 1.9 V to 3.6 V		0.8	3.0	dB	[2]
6	PA output power steps,			0.25	0.5	dB	[2]
7	2nd harmonic, at maximum output power	Conducted measurement at 50 Ohm		-51	-36	dBm	[2]
8	3rd harmonic, at maximum output power	Conducted measurement at 50 Ohm		-47	-30	dBm	[2]
9	Spurious emission, at maximum output power	Conducted measurement at 50 Ohm reference, 47 MHz to 230 MHz and 470 MHz to 862 MHz		-75	-65	dBm	[2]
10	Spurious emission, at maximum output power	Conducted measurement at 50 Ohm Other frequencies below 1 GHz		-75	-55	dBm	[2]
11	Spurious emission, at maximum output power	Conducted measurement at 50 Ohm 1 GHz to 12.5 GHz		-75	-53	dBm	[2]

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Table 26. TX Characteristics

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 434MHz, crystal = 55.2 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO_VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
12	Out of band TX noise at 12.5 kHz offsets, CW mode	434 MHz band		-110	-98	dBc/Hz	[2]
13	Out of band TX noise at 25 kHz offsets, CW mode	434 MHz band		-110	-98	dBc/Hz	[2]
14	Out of band TX noise at 100 kHz offset, CW mode	434 MHz band		-114	-100	dBc/Hz	[2]
15	Out of band TX noise at 1 MHz offset, CW mode	434 MHz band		-130	-125	dBc/Hz	[2]
16	Adjacent channel power	GFSK, BT = 0.5, h = 1, channel spacing = 12.5 kHz, symbol rate = 3 kBaud, modulation with PN9 sequence		-66		dBc	[2]
17	Adjacent channel power	GFSK, BT = 0.5, h = 1, channel spacing = 25 kHz, symbol rate = 6 kBaud, modulation with PN9 sequence		-54		dBc	[2]
18	Adjacent channel power	GFSK, BT = 0.5, h = 1, channel spacing = 50 kHz, symbol rate = 6 kBaud, modulation with PN9 sequence		-64		dBc	[2]
19	Adjacent channel power	GFSK, BT = 0.5, h = 1, channel spacing = 300 kHz, symbol rate = 6 kBaud, modulation with PN9 sequence		-60		dBc	[2]
20	99.5 % occupied bandwidth	GFSK, BT = 0.5, Manchester data rate = 1.2 kbit/s, frequency deviation = ±2.0 kHz		5.3	7	kHz	[2]
21	99.5 % occupied bandwidth	GFSK, BT = 0.5, Manchester data rate = 2.4 kbit/s, frequency deviation = ±2.4 kHz		7.8	9	kHz	[2]
22	99.5 % occupied bandwidth	GFSK, BT = 0.5, Manchester data rate = 4.8 kbit/s, frequency deviation = ±4.8 kHz		12.5	18	kHz	[2]
23	99.5 % occupied bandwidth	GFSK, BT = 0.5, Manchester data rate = 50 kbit/s, frequency deviation = ±50 kHz		154	180	kHz	[2]
24	TX supply current at maximum output power	System clock divided by 2 to be used. EROM execution		30	36	mA	[2]

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Table 26. TX Characteristics

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 434MHz, crystal = 55.2 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO_VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
25	Variation over Temperature of TX Supply Current at maximum Output Power 14 dBm	System clock divided by 2 to be used. EROM execution;		0.5		mA	[2]
26	Variation over Voltage of TX Supply Current at maximum Output Power 14 dBm (1.9 V - 3.6 V)	System clock divided by 2 to be used. EROM execution;		3.0		mA	[2]
27	Out of band tx noise @ 12.5kHz	Application: wmbus Band: 434MHz using channel filter = 10kHz		-110	-100	dBc/Hz	[2]
28	Out of band tx noise @ 37.5kHz	Application: wmbus Band: 434MHz using channel filter = 10kHz		-112	-102	dBc/Hz	[2]
29	Out of band tx noise @ 50kHz	Application: wmbus Band: 434MHz using channel filter = 10kHz		-112	-102	dBc/Hz	[2]
29	Out of band tx noise @ 4500kHz	Application: wmbus Band: 434MHz using channel filter = 10kHz		-135	-130	dBc/Hz	[2]
31	ADJACENT CHANNEL POWER, 434 MHz band, Wireless MBus - Mode F	4GFSK, h=0.5, BT=0.5, Channel spacing 25kHz, 5kChip/s		-50		dBc	[2]
32	Occupied bandwidth, 434 MHz band, Wireless MBus - Mode F	4GFSK, h=0.5, BT=0.5, Channel spacing 25kHz, 5kChip/s		20	22	kHz	[2]

Table 27. Characteristics for TRX switch

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 434 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO_VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	TRX switch isolation from TRXSWITCH_TX to TRXSWITCH_ANT	169 MHz band		27		dB	[5]
		315 MHz band		23		dB	[5]
		434 MHz band		20		dB	[5]
		868 MHz band		16		dB	[5]
		925 MHz band		16		dB	[5]
2	TRX switch loss from TRXSWITCH_TX to TRXSWITCH_ANT	169 MHz band		0.3		dB	[5]
		315 MHz band		0.3		dB	[5]
		434 MHz band		0.3		dB	[5]
		868 MHz band		0.5		dB	[5]
		925 MHz band		0.5		dB	[5]

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Table 27. Characteristics for TRX switch

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD = 2.5 V to 3.6 V, f_C = 434 MHz
VDD = VDD_IO, VDD_DIG, VDD_XO_VDD_RF, VDD_ADC, VDD_PA

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
3	TRX switch isolation from TRXSWITCH_RX to TRXSWITCH_ANT	169 MHz band		27		dB	[5]
		315 MHz band		24		dB	[5]
		434 MHz band		22		dB	[5]
		868 MHz band		18		dB	[5]
		925 MHz band		18		dB	[5]
4	TRX switch loss from TRXSWITCH_RX to TRXSWITCH_ANT	169 MHz band		0.4		dB	[5]
		315 MHz band		0.4		dB	[5]
		434 MHz band		0.4		dB	[5]
		868 MHz band		0.6		dB	[5]
		925 MHz band		0.6		dB	[5]

Table 28. Characteristics for ESD

Nr.	Description	Conditions	Min	Typ	Max	Unit
1	ESD HBM - RF pins[1] Electrostatic Discharge (Human Body Model)	1500 Ω, 100 pF	2			kV
2	ESD HBM - non RF pins[1] Electrostatic Discharge (Human Body Model)	1500 Ω, 100 pF	2			kV
3	ESD CDM[2] Electrostatic Discharge (Charged Device Model)	All pins	500			V

[1] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

[2] JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Table 29. Static Characteristics I/O Ports

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD_IO = 1.9 V to 3.6 V and 4.5 V to 5.5 V

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	High level input voltage		0.7 × VDD_IO		VDD_IO + 0.3	V	[1]
2	Low Level input voltage		–0.3		0.3 × VDD_IO	V	[1]
3	Input hysteresis voltage		0.1 × VDD_IO			V	[4]
4	Output high current	At VOH = VDD_IO - 0.4 V	1			mA	[1]
5	Output low current	At VOL = 0.4 V	1			mA	[1]
6	Output high current	VDD_IO > 2.7 V; At VOH = 0.8 × VDD_IO	2			mA	[2]

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Table 29. Static Characteristics I/O Ports

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD_IO = 1.9 V to 3.6 V and 4.5 V to 5.5 V

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
7	Output low current	VDD_IO > 2.7 V; At VOL = 0.2 × VDD_IO	2			mA	[2]
8	Pull-up resistor	Voltage at port pin = 0 V	50	70	110	kOhm	[1]
9	Pull-down resistor	Voltage at port pin = VDD_IO	50	70	110	kOhm	[1]

Table 30. Dynamic Characteristics I/O Ports

Following characteristics are valid for conditions as follows (unless otherwise specified)
T_{amb} = -40 °C to 85 °C, VSS = 0 V, VDD_IO = VDD_IO = 2.5 V to 3.6 V and 4.5 V to 5.5 V

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Output rise time	50 pF load	6		35	ns	[4]
2	Output fall time	50 pF load	6		35	ns	[4]
3	Bandwidth 50	50 pF load			5	MHz	[4]
4	Bandwidth 20	20 pF load			10	MHz	[4]
5	Bandwidth 20	20 pF load, VDD_IO = 1.9 V to 2.5 V			5	MHz	[4]

Table 31. SPI / UART

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	SPI operation speed Master Mode	CPU_CLK_SEL = 1 or 2; System clock to be used.	50		1.0M	baud	[4]
2	SPI operation speed Slave Mode	CPU_CLK_SEL = 1 or 2; System clock to be used.	50		1.0M	baud	[4]
3	UART operation speed	CPU_CLK_SEL = 1 or 2; System clock to be used.	50		1.7M	baud	[4]

Table 32. Application relevant limits

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
1	Power-on reset level		1.5			V	[1]
2	Maximum current in pin TXOUT using 12 dBm PA	Maximum 10 % PA activation over 10 years			40	mA	[4]
3	Maximum current in pin TXOUT using 0 dBm PA	Maximum 10 % PA activation over 10 years			3.5	mA	[4]
4	Maximum current that can be provided by the internal 5 V regulator; available at VDD_3VOUT				50	mA	[1]
5	Maximum external load capacitance[1] connected at VDD_3VOUT				168	nF	[4]
6	Frequency of external reference crystal connected to XTAL_N and XTAL_P			27.6		MHz	[4]

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Table 32. Application relevant limits

Nr.	Description	Conditions	Min	Typ	Max	Unit	Note
7	Frequency of external reference clock connected to XTAL_N			27.6		MHz	[4]
8	Frequency of external reference crystal connected to XTAL_N and XTAL_P	Second Crystal frequency selected.		55.2		MHz	[4]
9	Frequency of external reference clock connected to XTAL_N	Second Crystal frequency selected.		55.2		MHz	[4]
10	External clock input voltage level at XTAL_N	LDO_XO_OK = 1	0		1.5	V	[4]
11	External clock input signal amplitude at XTAL_N	LDO_XO_OK = 1	0.6			Vpp	[4]
12	Input voltage level at XTAL_N when XO LDO is disabled or not ready	LDO_XO_OK = 0	-0.1		0.1	V	[4]
13	Duty cycle of external clock input signal XTAL_N[2]		45		55	%	[4]

[1] All tolerances of the external capacitors must be taken into account when calculating the maximum allowed external load capacitance.

[2] As the external clock input signal requires a DC offset the average value of the external clock signal shall be used as reference level to determine the duty cycle.

Notes:

[1] Tested in production test

[2] Characterized at 1.9V, 2.5 V, 3 V, 3.6 V; -40 °C, 25 °C, 85 °C

[3] Characterized at 3 V; -40 °C, 25 °C, 85 °C

[4] Guaranteed by design

[5] Characterized at 3 V; -40 °C, 25 °C, 85 °C, limited sample size

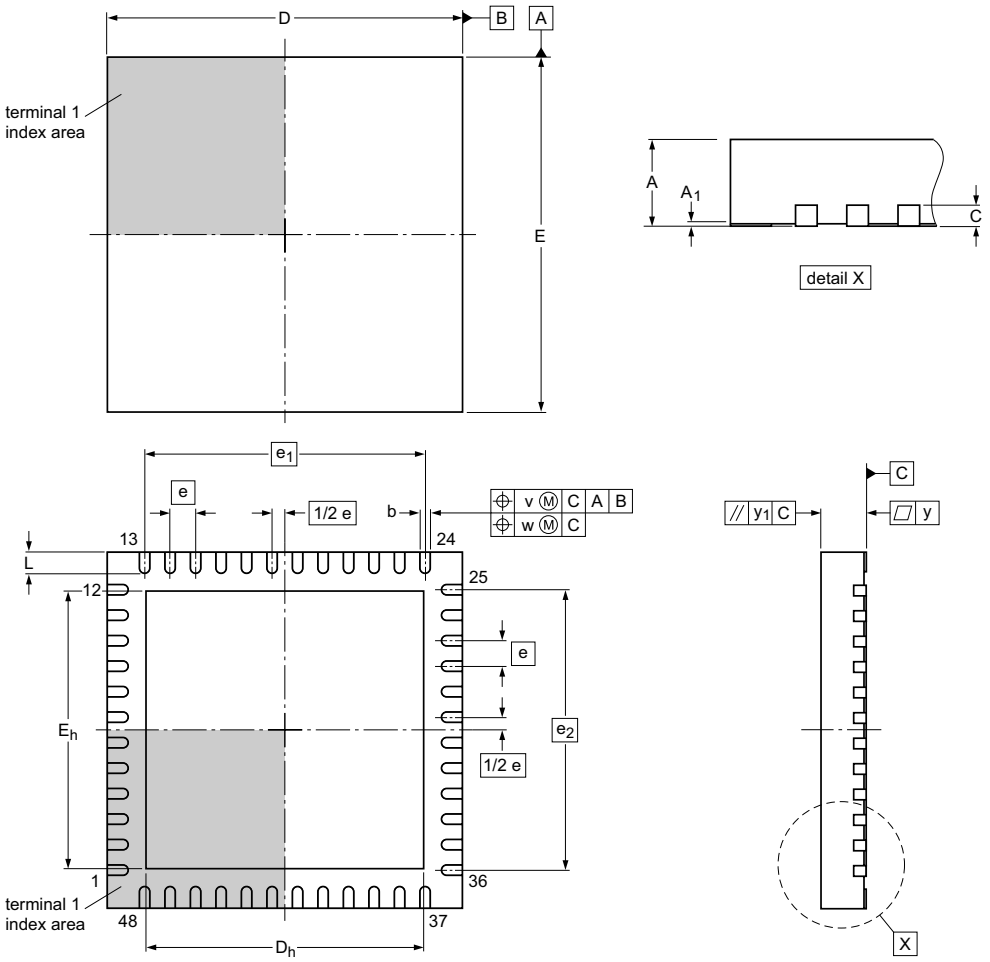
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11. Mechanical information

11.1 Package outline

HVQFN48: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 x 7 x 0.85 mm **SOT619-13**



Dimensions (mm are the original dimensions)

Unit(1)		A(1)	A1	b	C	D	Dh	E	Eh	e	e1	e2	L	v	w	y	y1
mm	max	1.00	0.05	0.30		7.1	5.65	7.1	5.65				0.5				
	nom	0.85	0.02	0.21	0.2	7.0	5.50	7.0	5.50	0.5	5.5	5.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		6.9	5.35	6.9	5.35				0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included

sot619-13_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT619-13	- - -	MO-220	- - -			~~09-08-24~~ 13-03-27

Fig 17. Package outline HVQFN48

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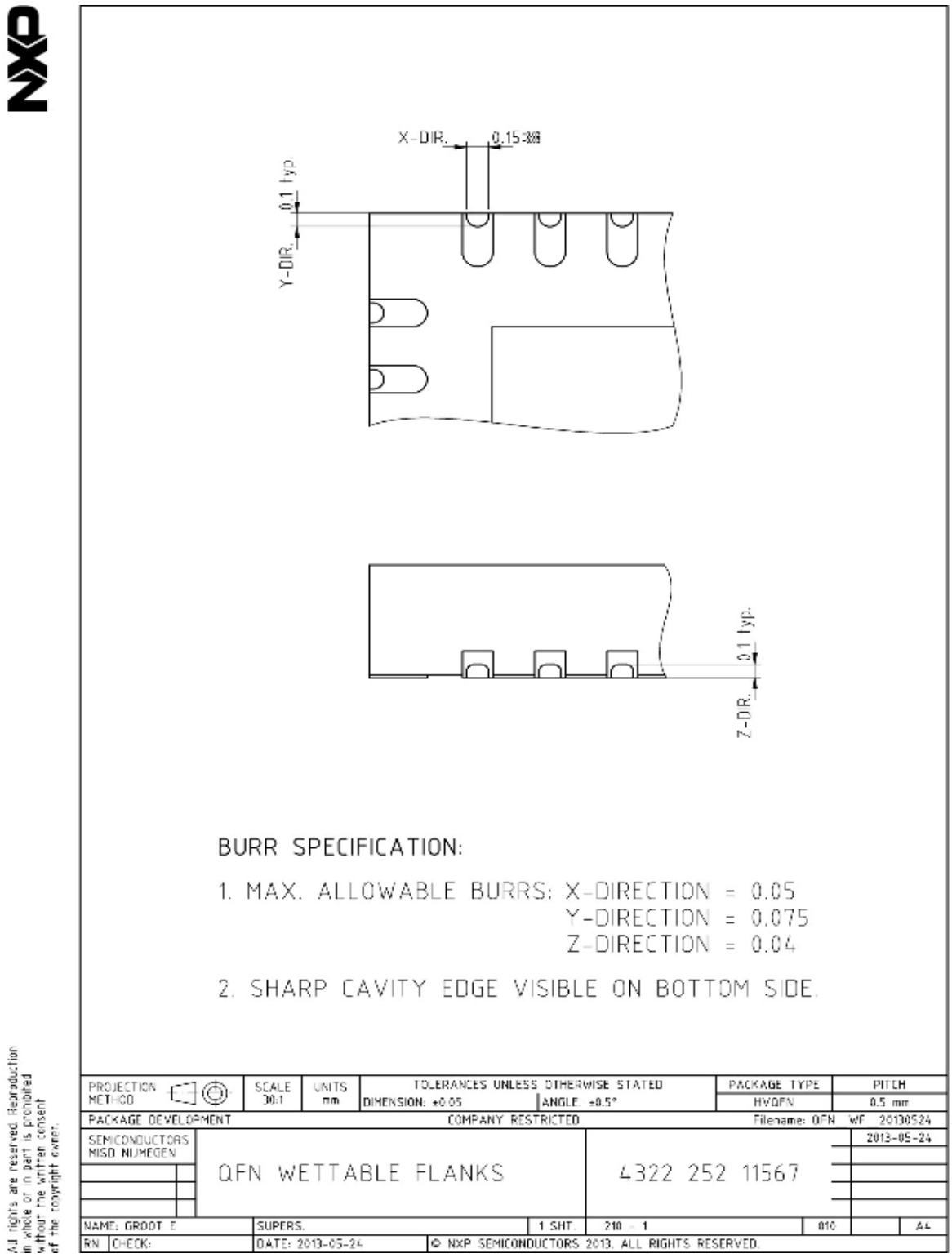


Fig 18. Package detail wettable flanks

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12. Glossary

AAC — Automatic Amplitude Calibration

AAFC — Automatic Amplitude and Frequency Calibration

AC — Alternating Current

ADC — Analogue to Digital Converter

AFC — Automatic Frequency Calibration

AGC — Automatic Gain Control

API — Application Programming Interface

ASK — Amplitude Shift Keying

BF — Bit Field

BW — BandWidth

BWC — BandWidth Control

CDR — Clock and Data Recovery

CP — Charge Pump

CW — Continuous Wave

DAC — Digital to Analogue Converter

DC — Direct Current

DMA — Direct Memory Access

ESD — ElectroStatic Discharge

FER — Frame Error Rate

FSK — Frequency Shift Keying

FSM — Finite State Machine

FSYNC — Frame SYNChronisation

HAL — Hardware Abstraction Layer

HBM — Human Body Model

IF — Intermediate Frequency

IREC — Intelligent Radio Evaluation and Configuration

ISM — Industrial, Scientific and Medical

ISR — Interrupt Service Routine

LDO — Low Drop-Out regulator

LIN — Local Interconnect Network

LNA — Low Noise Amplifier

LO — Local Oscillator

LPF — Low-Pass Filter

MMR — Missed Message Rate

MMU — Memory Management Unit

NC — Not Connected

NRZ — Non Return to Zero

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OFMU — Offset Frequency Measurement Unit

OOK — On-Off Keying

PA — Power Amplifier

PFD — Phase-Frequency Detector

PLL — Phase Locked Loop

POR — Power-On-Reset

POK — Power OK

PRN — Pseudo-Random Number

PRNG — Pseudo-Random Number Generator

RF — Radio Frequency

RFU — Reserved for Future Use

RSSI — Received Signal Strength Indicator

RX — Receiver

SD — Sigma-Delta

SFR — Special Function Register

SPI — Serial Peripheral Interface

TIA — Trans-Impedance Amplifier

TX — Transmitter

UART — Universal Asynchronous Receiver and Transmitter

UHF — Ultra High Frequency

PLL — Phase Locked Loop

VCO — Voltage Controlled Oscillator

WUP — Wake-UP

ZIF — Zero Intermediate Frequency

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13. References

[1] **MRK III Programmers Reference —** MRK III and MRK IIIe instruction set, Rev. 04 — 04 Jul 2012

[2] **Application note AN10365 —** Surface mount reflow soldering, Rev. 7 — 18 April 2013

[3] **MRK III MDI —** Monitor and Download Interface, Rev. 09 — 23 June 2014

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14. Revision history

Table 33. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
OL2385_1.0	15 June 2016	Product data sheet	—	—
Modifications:	• Initial product data sheet - COMPANY PUBLIC			

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15. Legal information

15. Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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