P19800B Spectrometer ASIC

Keywords: Spectrometer ASIC, Earth observation, polyphase filter, FFT, ADC

Technical Summary

The P19800B spectrometer ASIC processes up to 5.5GHz bandwidth input signals provided by microwave front ends. The ASIC (Fig.1) includes a VGA, a 6-bit ADC, an FFT based on polyphase filtering and an accumulator capable of accumulating up to 34 seconds of frequency-domain data. The chip also includes an output data interface, a PLL based frequency synthesizer and a SPI interface for the ASIC's programming and data interchange at low speed. The chip (Fig.2) is offered in a BGA package and as an IP block for integration into SoCs. The P19800B ASIC is also offered on an evaluation board (Fig.3). Fig. 4 shows measured ASIC performance results.

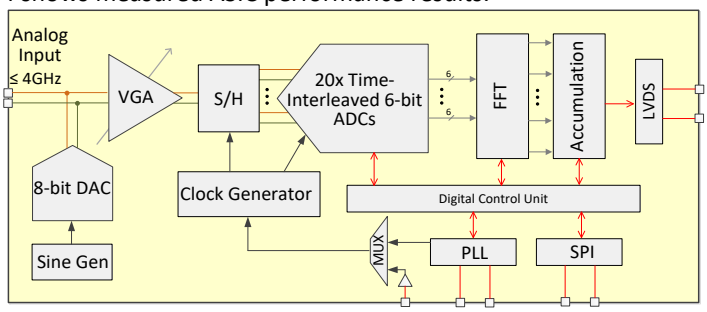


Figure 1. A block diagram of the ASIC.



Figure 2. The ASIC chip and the BGA package.



Figure 3. Evaluation board.

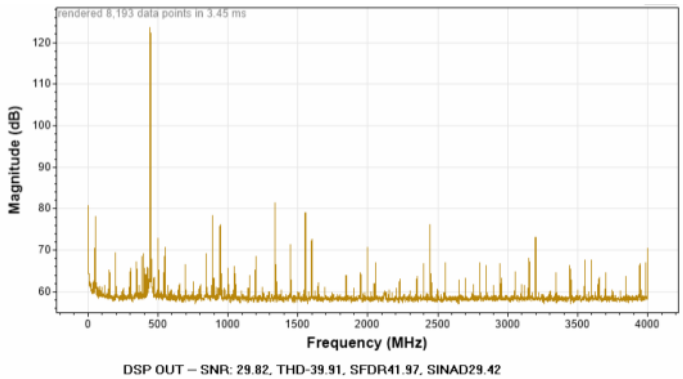


Figure 4. An Example - ASIC readout with Fin = 447MHz.

Operational Capabilities

The ASIC digitizes the RF signal and splits the spectrum into 8192 frequency bins. The power or magnitude is computed for each bin and the result accumulated.

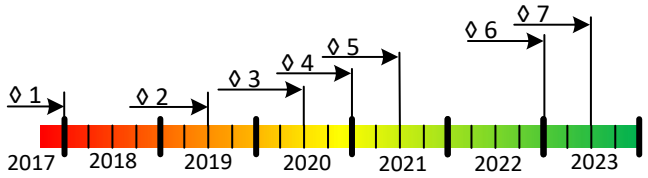
- Input signal bandwidth up to 5.5GHz
- Sampling rate up to 8GS/s
- Input signal FSR programmable from 66mV to 400mV pp differential
- Digitizer ENOB > 4.5-bit to 4GHz
- Power consumption < 1.6W (full functionality)
- Power consumption < 1.2W (4MHz bin resolution)
- Up to 8192 Frequency bins within 0 to 4GHz
- Accumulation time programmable from 2us to 34s
- An integrated 16GHz PLL with selectable Fref
- An SPI interface for control, diagnostics and readout
- Temperature range -40°C to 110°C
- 15 x 15 BGA package (12.8mm x 12.8 mm)
- Fabrication technology 28nm CMOS

Development Objectives & Milestones

P19800B (Rev 2) spectrometer ASIC is designed, fabricated, packaged and tested. The part and an eval PCB are available for purchasing. In case if any further improvements are required, the Rev 3 ASIC will be designed, fabricated, tested and made available to the customers.

The project includes the following milestones:

◊ 1. Feasibility is proven based on simulations
◊ 2. Rev 1 prototype ASIC chip is designed and taped out
◊ 3. Rev 1 ASIC is fabricated/tested, being sampled
◊ 4. Rev 2 ASIC is fabricated/tested, sales started
◊ 5. Rev 2 ASIC has SEE tested
◊ 6. If required, Rev 3 ASIC is designed/fabricated
◊ 7. Flight qualified chip is tested, sales started



Current TRL: 5, Estimated final TRL: 6

Applications

- Remote sensing instruments
- Radio astronomy
- Planet and Sun exploration missions
- Synthetic aperture radiometers
- Spectrum analyzers

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