PCMFxUSB30 series

Common-mode EMI filter for differential channels with integrated ESD protection

Rev. 1 — 01 April 2016 Product data sheet

1. Product profile

1.1 General description

Common-mode ElectroMagnetic Interference (EMI) filters with integrated ElectroStatic Discharge (ESD) protection for one, two and three differential channels. The devices are designed to provide low insertion loss for differential high-speed signals on each channel while unwanted common-mode signals are attenuated.

Each differential channel incorporates two signal lines that are coupled by integrated coils. Diodes provide protection to downstream components from ESD voltages up to ±15 kV on each signal line.

Table 1. Product overview

Type number	Number of channels	Package Name
PCMF1USB30	1	WLCSP5
PCMF2USB30	2	WLCSP10
PCMF3USB30	3	WLCSP15

1.2 Features and benefits

- One, two and three differential channels common-mode EMI filters with integrated ESD protection
- ESD protection up to ±15 kV contact discharge according to IEC 61000-4-2
- Superior common-mode suppression over a wide frequency range
- Superior RF performance compared to other integrated filters or discrete filters with external ESD protection
- Extremely high symmetry between line pairs
- Industry-standard Wafer Level Chip Scale Packages: WLCSP5, 10 and 15 for smaller footprint

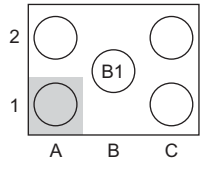
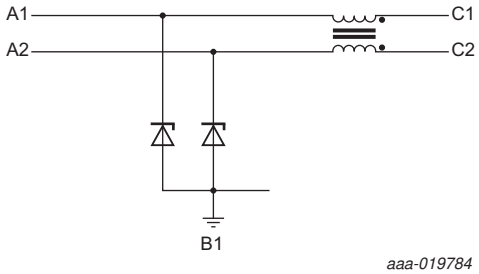
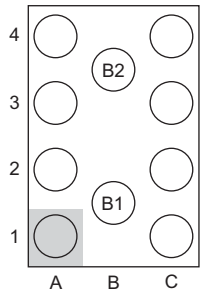
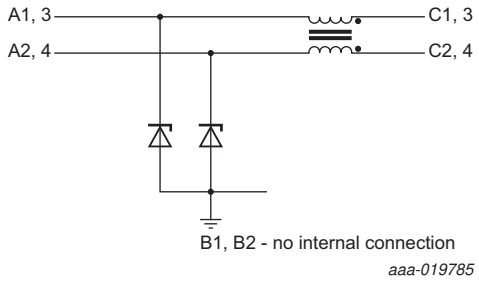
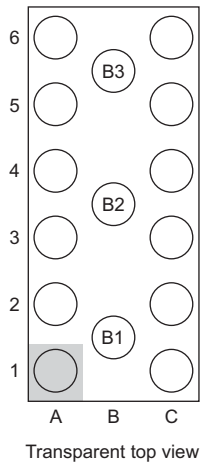
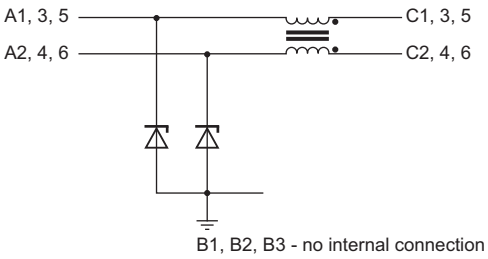
1.3 Applications

- Smartphone, cellular and cordless phone
- Tablet PC and Mobile Internet Device (MID)
- USB 3.1, USB 2.0, HDMI 2.0, HDMI 1.4
- MIPI M-PHY and D-PHY as used in Camera Serial Interface (CSI) and Display Serial Interface (DSI)
- General-purpose EMI and Radio-Frequency Interference (RFI) filter and downstream ESD protection

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2. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
PCMF1USB30 (WLCSP5_2-1-2)				
A1	CH1_IN+	channel 1+, external	 Transparent top view **WLCSP5_2-1-2**	 *aaa-019784*
A2	CH1_IN–	channel 1–, external		
B1	GND_CH1	ground channel 1		
C1	CH1_OUT+	channel 1+, internal		
C2	CH1_OUT–	channel 1–, internal		
PCMF2USB30 (WLCSP10_4-2-4)				
A1	CH1_IN+	channel 1+, external	 Transparent top view **WLCSP10_4-2-4**	 *aaa-019785*
A2	CH1_IN–	channel 1–, external		
A3	CH2_IN+	channel 2+, external		
A4	CH2_IN–	channel 2–, external		
B1	GND_CH1	ground channel 1		
B2	GND_CH2	ground channel 2		
C1	CH1_OUT+	channel 1+, internal		
C2	CH1_OUT–	channel 1–, internal		
C3	CH2_OUT+	channel 2+, internal		
C4	CH2_OUT–	channel 2–, internal		
PCMF3USB30 (WLCSP15_6-3-6)				
A1	CH1_IN+	channel 1+, external	 Transparent top view **WLCSP15_6-3-6**	 *aaa-019786*
A2	CH1_IN–	channel 1–, external		
A3	CH2_IN+	channel 2+, external		
A4	CH2_IN–	channel 2–, external		
A5	CH3_IN+	channel 3+, external		
A6	CH3_IN–	channel 3–, external		
B1	GND_CH1	ground channel 1		
B2	GND_CH2	ground channel 2		
B3	GND_CH3	ground channel 3		
C1	CH1_OUT+	channel 1+, internal		
C2	CH1_OUT–	channel 1–, internal		
C3	CH2_OUT+	channel 2+, internal		
C4	CH2_OUT–	channel 2–, internal		
C5	CH3_OUT+	channel 3+, internal		
C6	CH3_OUT–	channel 3–, internal		

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3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PCMF1USB30	WLCSP5	wafer level chip-size package; 5 bumps (2-1-2)	PCMF1USB30
PCMF2USB30	WLCSP10	wafer level chip-size package; 10 bumps (4-2-4)	PCMF2USB30
PCMF3USB30	WLCSP15	wafer level chip-size package; 15 bumps (6-3-6)	PCMF3USB30

4. Marking

Table 4. Marking codes

Type number	Marking code
PCMF1USB30	PF1S
PCMF2USB30	PF2S
PCMF3USB30	PF3S

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage		−0.5	5	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4; all input pins to ground			
		contact discharge	−15	15	kV
		air discharge	−15	15	kV
		IEC 61000-4-2, level 4; all output pins to ground			
		contact discharge	−2	2	kV
		air discharge	−2	2	kV
I_{PPM}	rated peak pulse current	t_p = 8/20 μs	−7	7	A
T_{stg}	storage temperature		−40	+125	°C
T_{amb}	ambient temperature		−40	+85	°C

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6. Characteristics

6.1 Channel characteristics

Table 6. Channel characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{s(ch)}$	channel series resistance	single line; input to output	-	3	-	Ω
C_d	diode capacitance	f = 1 MHz; V_I = 2.5 V [1]	-	0.25	-	pF
I_{RM}	reverse leakage current	per line; V_I = 5 V	-	-	100	nA
V_{BR}	breakdown voltage	I_R = 1 mA	6	9	-	V
V_F	forward voltage	I_F = 10 mA	-	0.8	-	V
R_{dyn}	dynamic resistance	TLP [2]				
		positive transient	-	0.14	-	Ω
		negative transient	-	0.14	-	Ω
		surge [3]				
		positive transient	-	0.22	-	Ω
		negative transient	-	0.22	-	Ω

[1] This parameter is guaranteed by design.

[2] 100 ns Transmission Line Pulse (TLP); 50 W; pulser at 70 ns to 90 ns.

[3] According to IEC 61000-4-5 (8/20 ms).

6.2 Frequency characteristics

Table 7. Frequency characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Common mode: S_{21cc}						
α_{il}	insertion loss	[1]				
		f = 800 MHz	-	–12	-	dB
		f = 2.6 GHz	-	–38	-	dB
		f = 5 GHz	-	–18	-	dB
Differential mode: S_{21dd}						
α_{il}	insertion loss	f = 1 MHz [1]	-	0.3	-	dB
f_{-3dB}	cut-off frequency	[1]	-	6	-	GHz

[1] Normalized to attenuation at 1 MHz.

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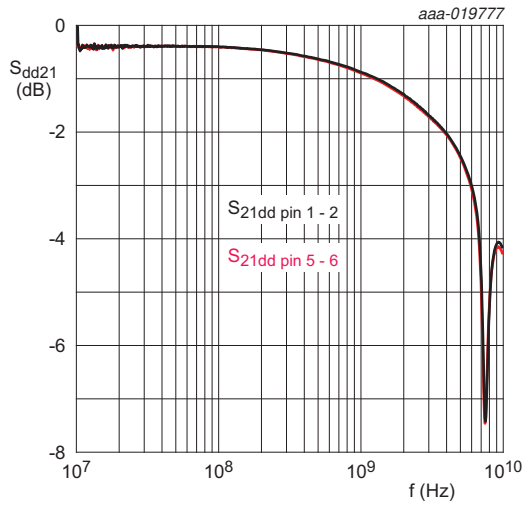


Fig 1. Differential-mode insertion loss; typical values

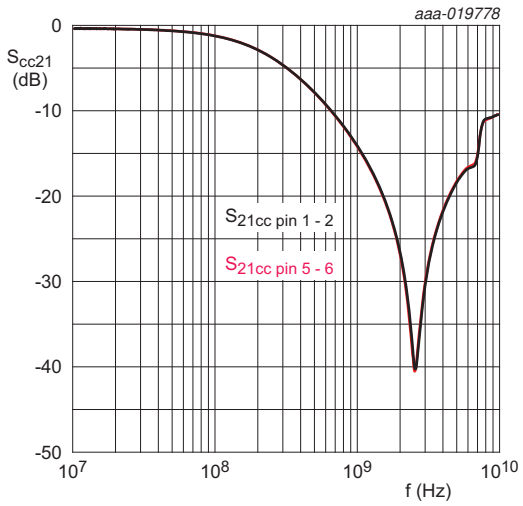


Fig 2. Common-mode insertion loss; typical values

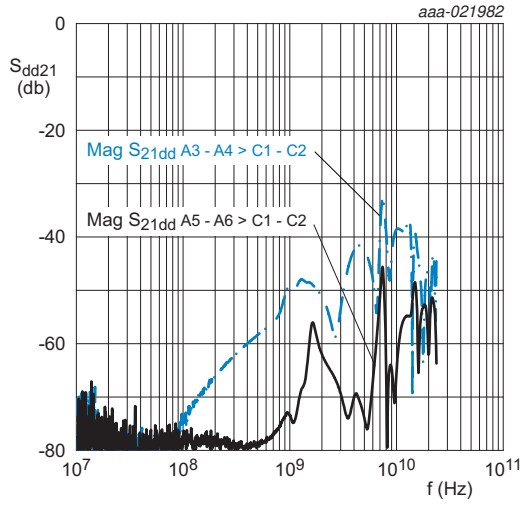
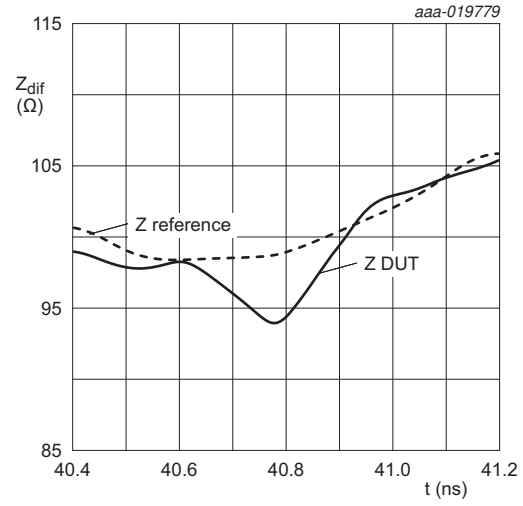


Fig 3. Differential crosstalk; typical values

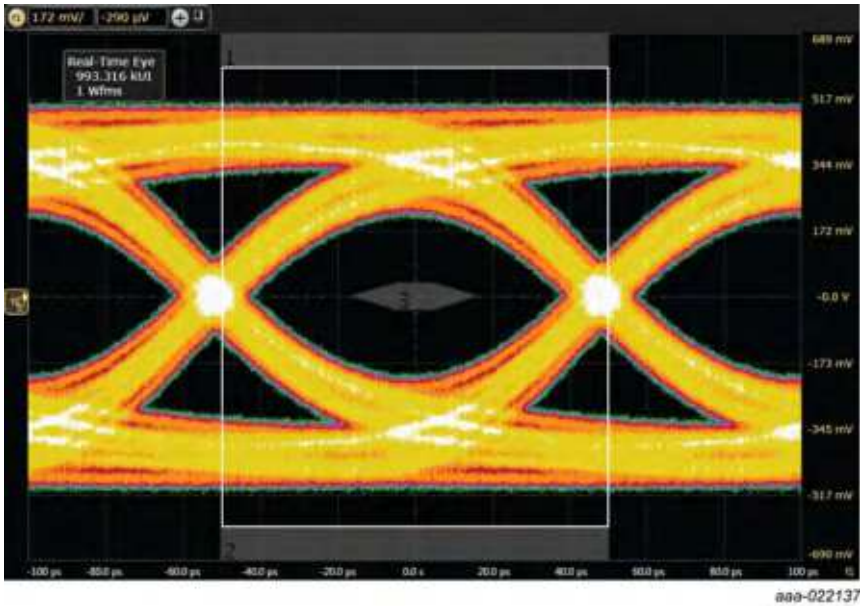


t_r = 200 ps

Fig 4. Differential Time Domain Reflectometer (TDR) plot; typical values

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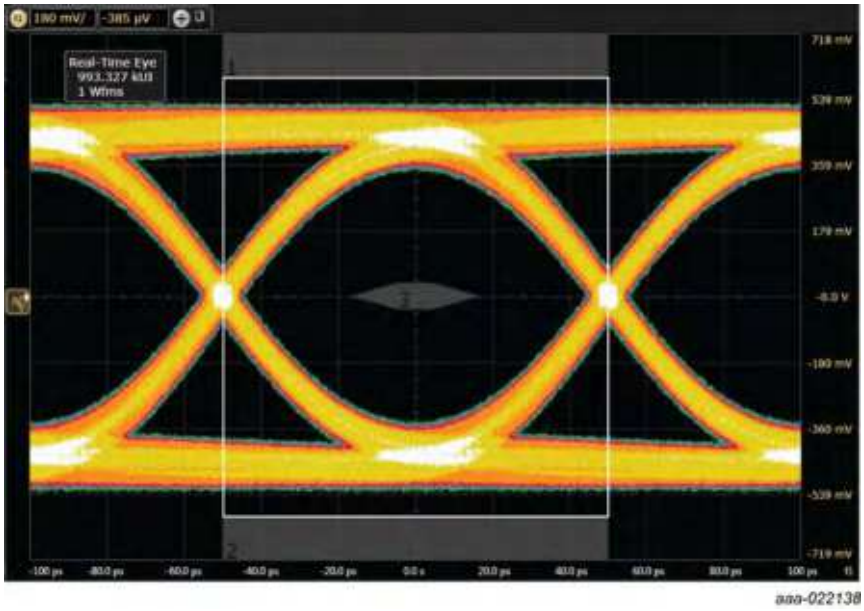


Data rate: 10 Gbit/s

Vertical scale: 173 mV/div

Horizontal scale: 20 ps/div

Fig 5. USB 3.1 eye diagram, test board with PCMF2USB30; typical values



Data rate: 10 Gbit/s

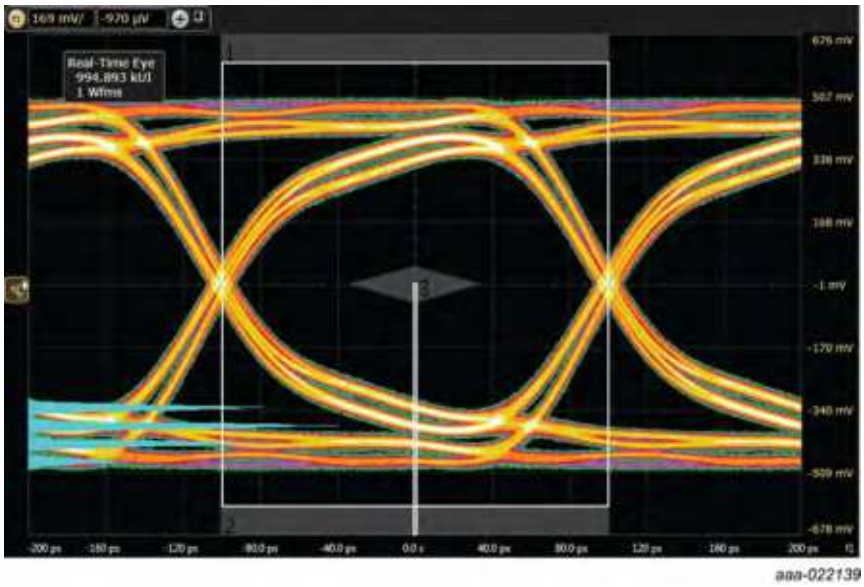
Vertical scale: 180 mV/div

Horizontal scale: 20 ps/div

Fig 6. USB 3.1 eye diagram, test board without device; typical values

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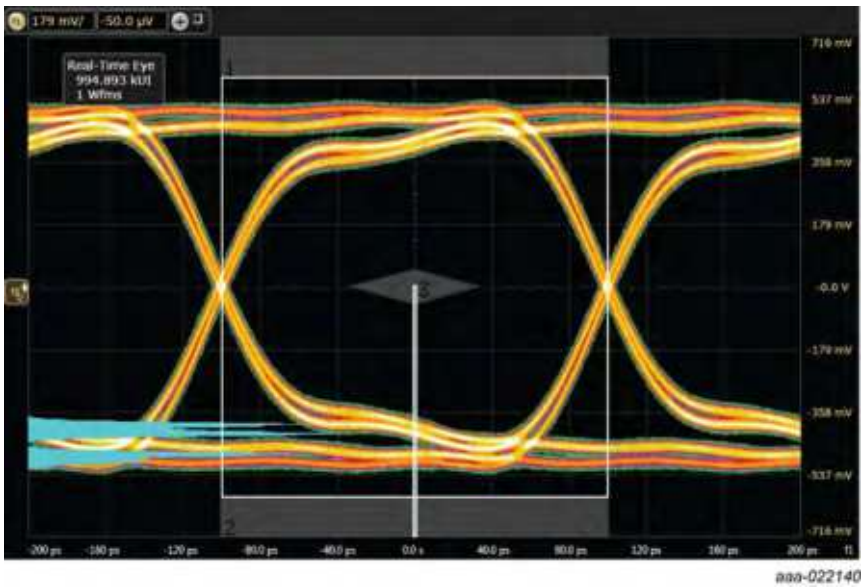


Data rate: 5 Gbit/s

Vertical scale: 169 mV/div

Horizontal scale: 40 ps/div

Fig 7. USB 3.1 eye diagram, test board with PCMF2USB30; typical values



Data rate: 5 Gbit/s

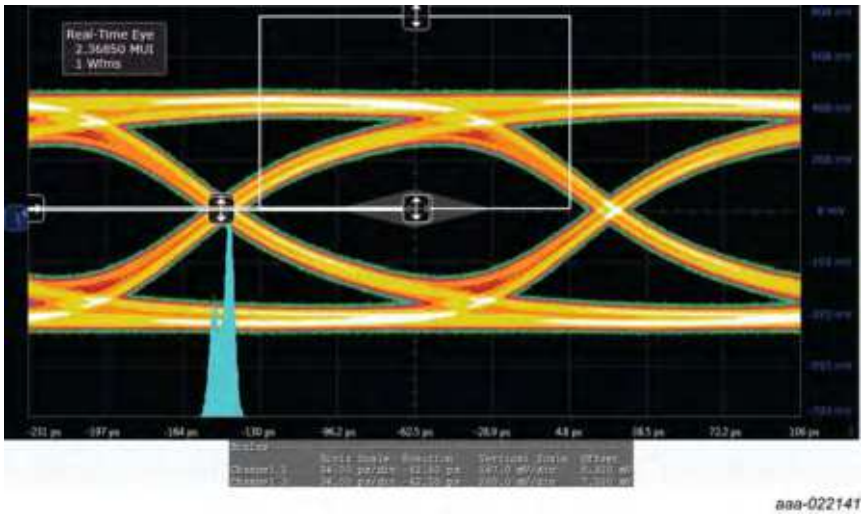
Vertical scale: 179 mV/div

Horizontal scale: 40 ps/div

Fig 8. USB 3.1 eye diagram, test board without device; typical values

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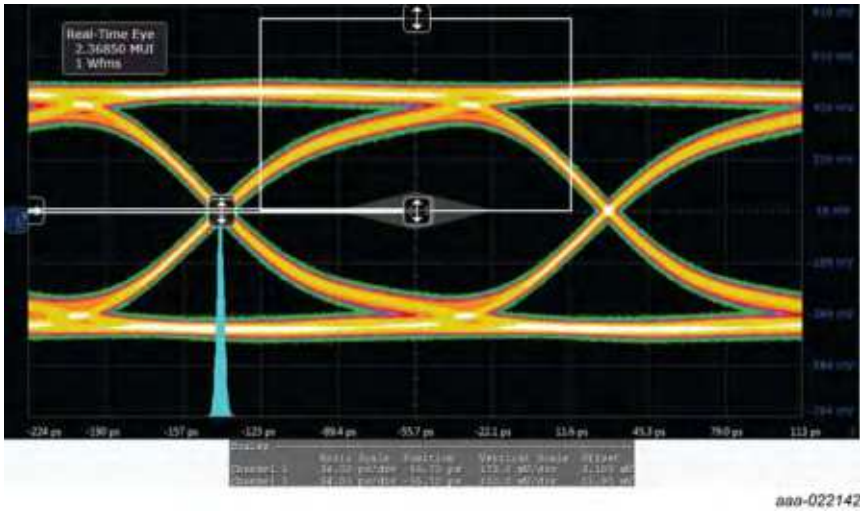


Test frequency: 148.5 MHz

Differential swing voltage: 861 mV

Horizontal scale: 34 ps/div

Fig 9. HDMI 2.0 eye diagram TP1, test board with PCMF2USB30; typical values



Test frequency: 148.5 MHz

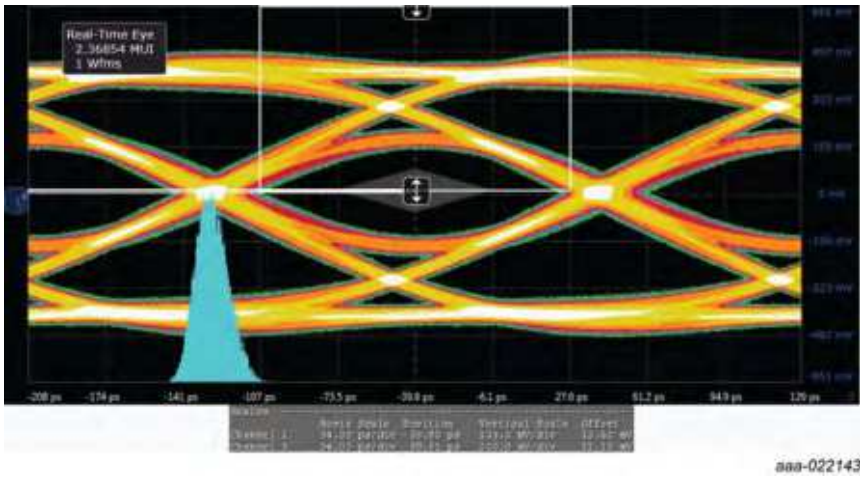
Differential swing voltage: 917 mV

Horizontal scale: 34 ps/div

Fig 10. HDMI 2.0 eye diagram TP1, test board without device; typical values

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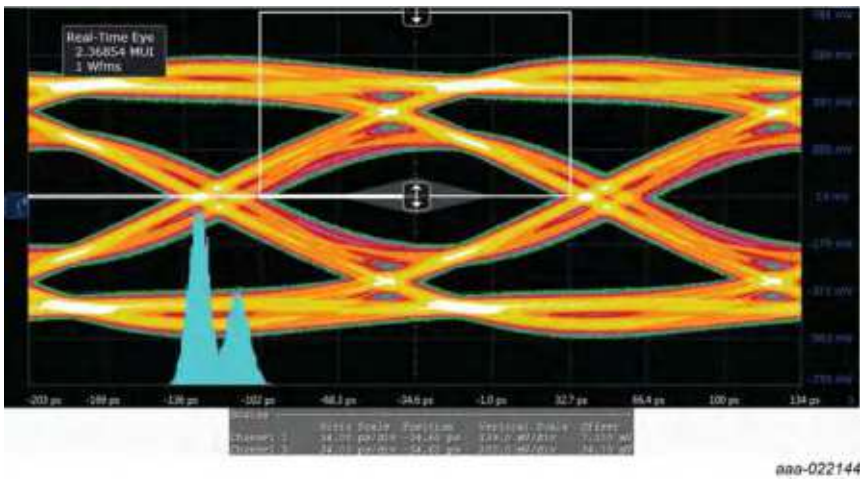
Test frequency: 148.5 MHz

Differential swing voltage: 849 mV

Horizontal scale: 34 ps/div

Remark: Measured at Test Point 2 (TP2) worst cable emulator, reference cable equalizer and worst case positive skew.

Fig 11. HDMI 2.0 eye diagram TP2, test board with PCMF2USB30; typical values



Test frequency: 148.5 MHz

Differential swing voltage: 909 mV

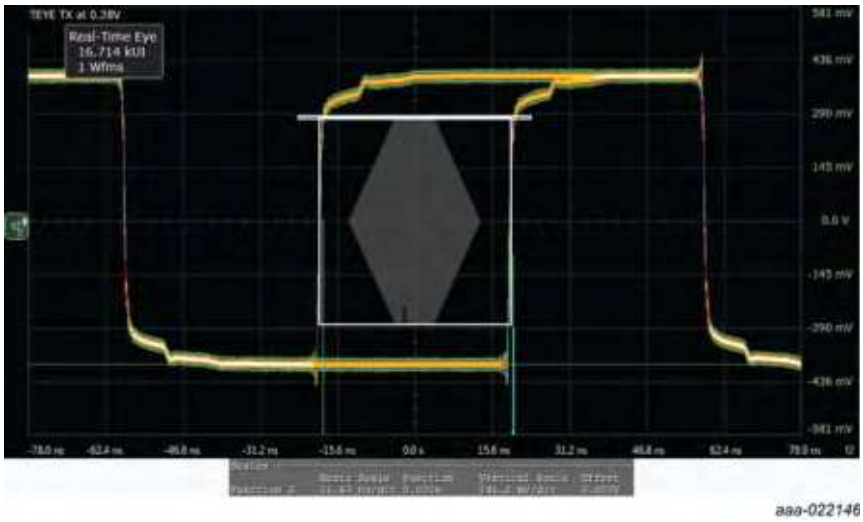
Horizontal scale: 34 ps/div

Remark: Measured at Test Point 2 (TP2) worst cable emulator, reference cable equalizer and worst case positive skew.

Fig 12. HDMI 2.0 eye diagram TP2, test board without device; typical values

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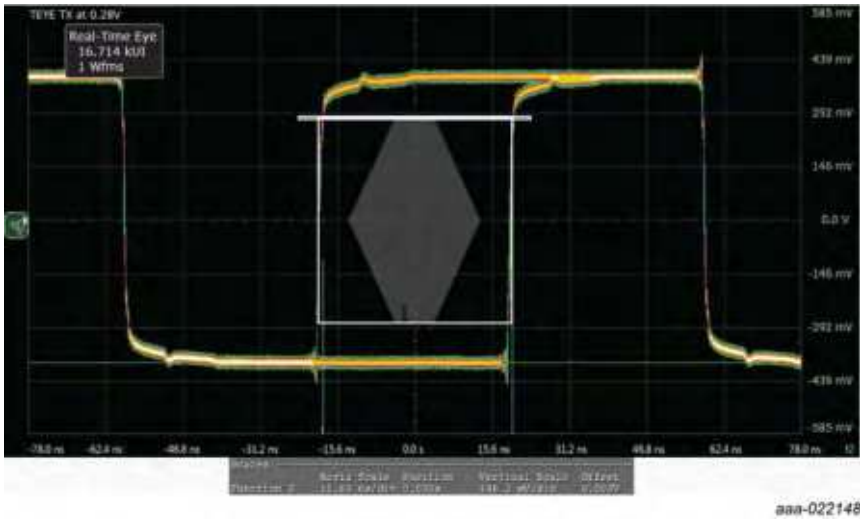
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Vertical scale: 145 mV/div

Horizontal scale: 15.6 ns/div

Fig 13. MIPI M-PHY PWM-TX transmitter eye opening at 140 mV, test board with PCMF2USB30; typical values



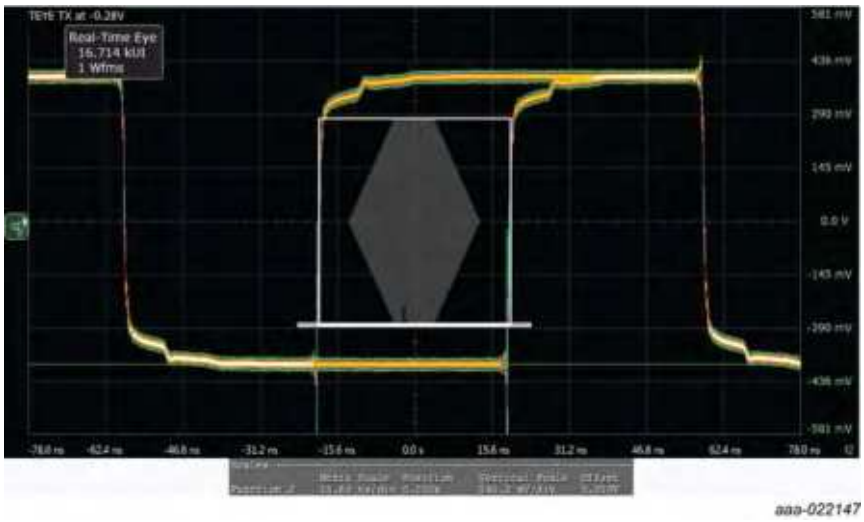
Vertical scale: 146 mV/div

Horizontal scale: 15.6 ns/div

Fig 14. MIPI M-PHY PWM-TX transmitter eye opening at 140 mV, test board without device; typical values

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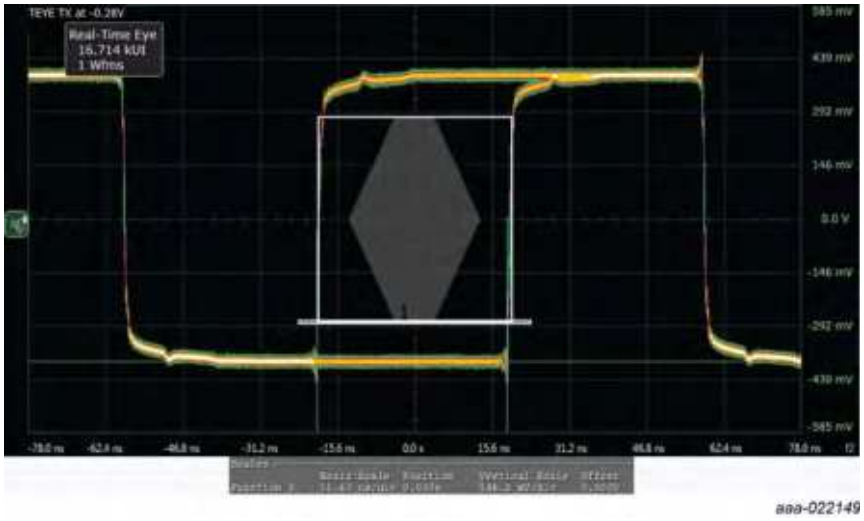
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Vertical scale: 145 mV/div

Horizontal scale: 15.6 ns/div

Fig 15. MIPI M-PHY PWM-TX transmitter eye opening at –140 mV, test board with PCMF2USB30; typical values



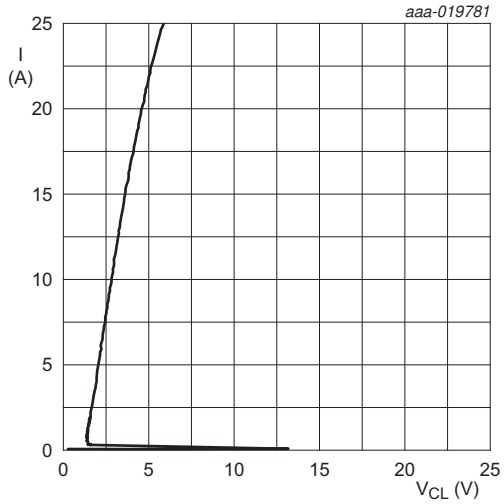
Vertical scale: 146 mV/div

Horizontal scale: 15.6 ns/div

Fig 16. MIPI M-PHY PWM-TX transmitter eye opening at –140 mV, test board without device; typical values

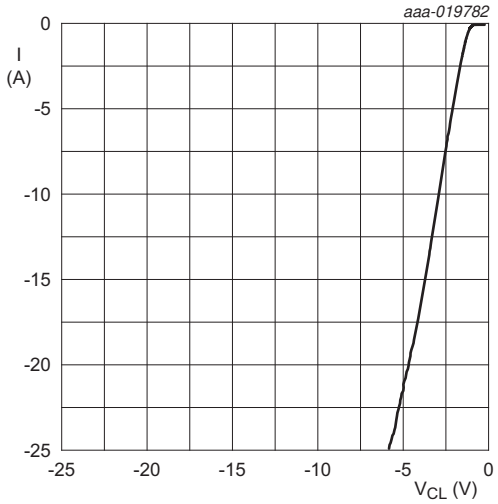
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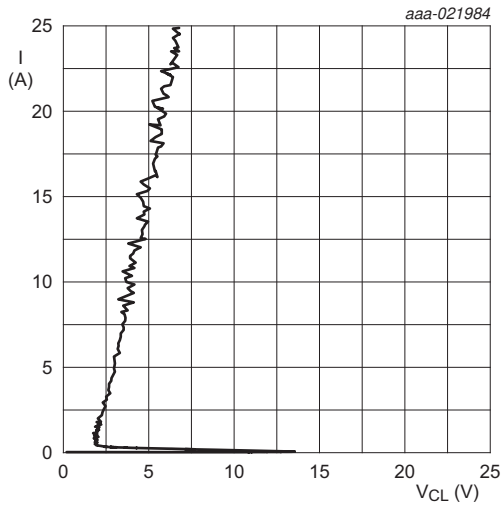
Transmission Line Pulse (TLP) = 100 ns;
t_r = 1 ns

Fig 17. Dynamic resistance with positive clamping; typical values



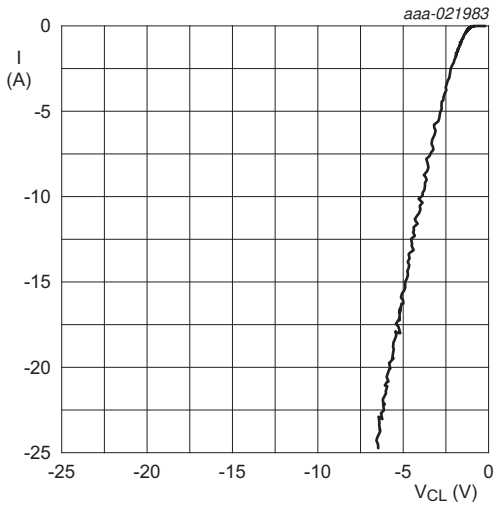
Transmission Line Pulse (TLP) = 100 ns;
t_r = 1 ns

Fig 18. Dynamic resistance with negative clamping; typical values



Very-Fast Transmission Line Pulse (VF-TLP) = 5 ns;
t_r = 600 ps

Fig 19. Dynamic resistance with positive clamping; typical values



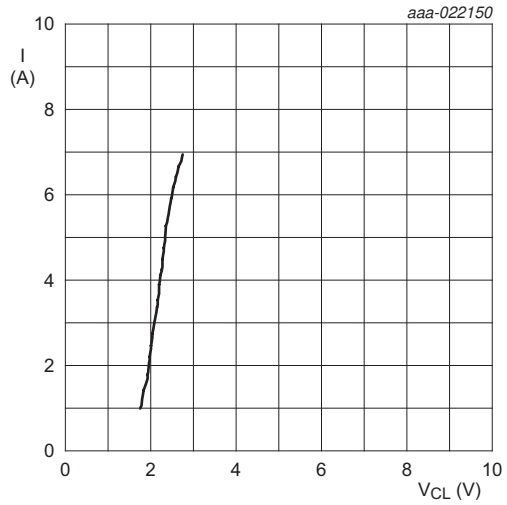
Very-Fast Transmission Line Pulse (VF-TLP) = 5 ns;
t_r = 600 ps

Fig 20. Dynamic resistance with negative clamping; typical values

The device uses an advanced clamping structure showing a negative dynamic resistance. This snapback behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snapback state after exceeding breakdown voltage (due to an ESD pulse for instance).

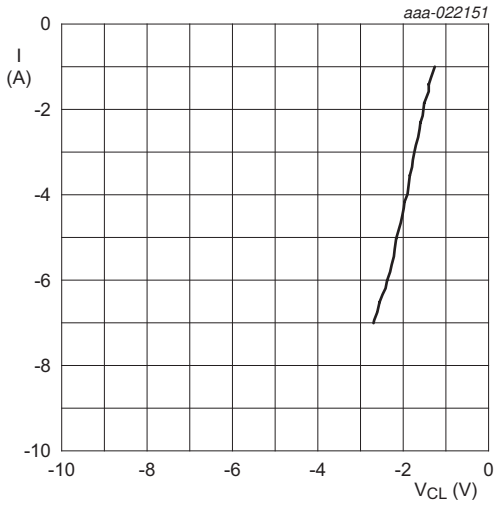
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According to IEC 61000-4-5 (8/20 μs)

Fig 21. Dynamic resistance with positive clamping; typical values



According to IEC 61000-4-5 (8/20 μs)

Fig 22. Dynamic resistance with negative clamping; typical values

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7. Application information

The device is designed to provide high-level ESD protection and common-mode filtering for differential high-speed data line pairs such as:

- USB 3.1
- HDMI 2.0
- Transition-Minimized Differential Signaling (TMDS)
- DisplayPort
- external Serial Advanced Technology Attachment (eSATA)
- Low Voltage Differential Signaling (LVDS)

When designing the PCB, give careful consideration to impedance matching and signal coupling. Do not connect the protected signal lines to unlimited current sources like, for example, a battery.

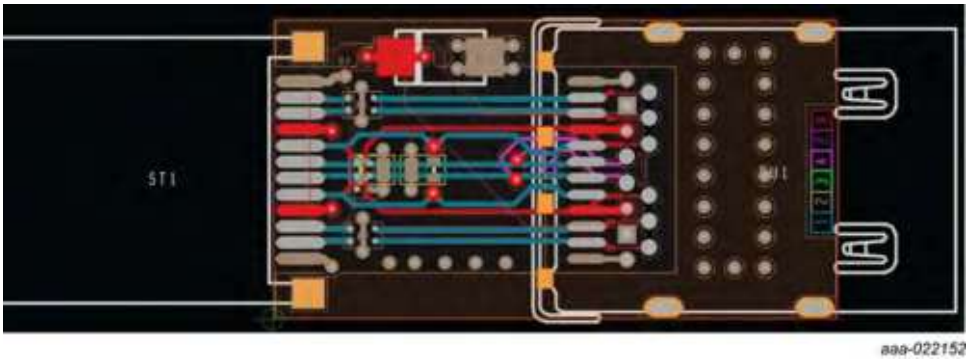


Fig 23. Application diagram: protecting and filtering the differential data lines of a USB Type-C connector evaluation dongle with PCMF1USB30

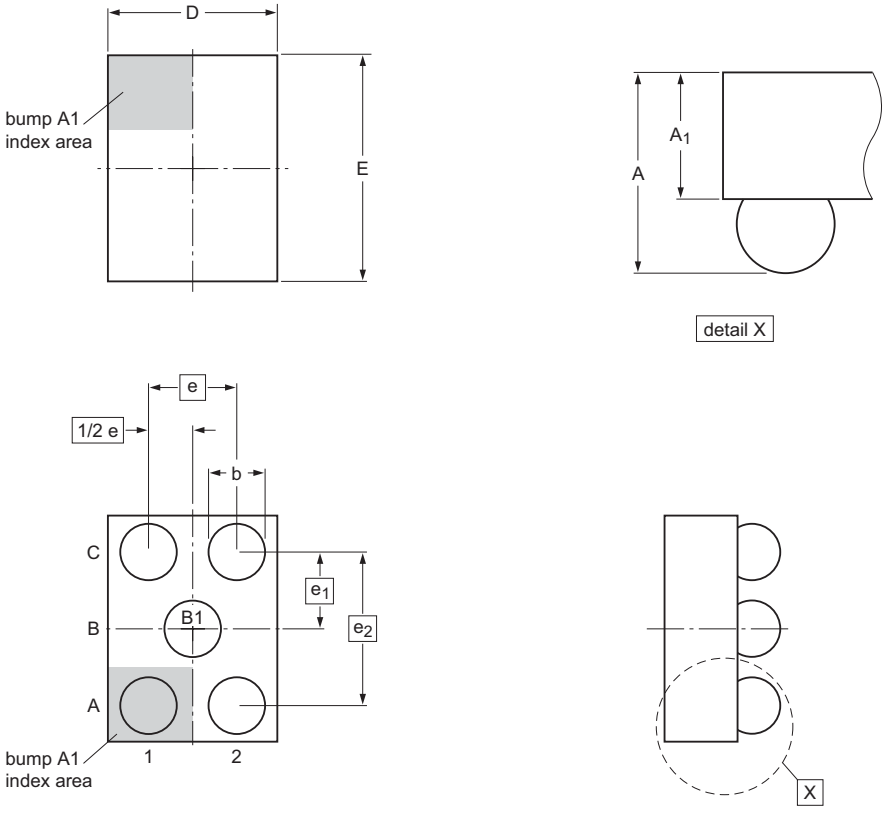
Since the SuperSpeed TX/RX lines are separated by GND or VBUS from the Hi-Speed lines, PCMF1USB30 makes it easy to achieve same signal lengths, straight routing, and optimal positioning for ESD protection directly at the connector.

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8. Package outline

WLCSP5: wafer level chip-size package; 5 bumps (2-1-2) **PCMF1USB30**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	D	E	e	e_1	e_2
mm	max	0.60	0.38	0.31	0.82	1.22			
	nom	0.57	0.37	0.26	0.77	1.17	0.40	0.40	0.80
	min	0.54	0.36	0.21	0.72	1.12			

pcmf1usb30_po

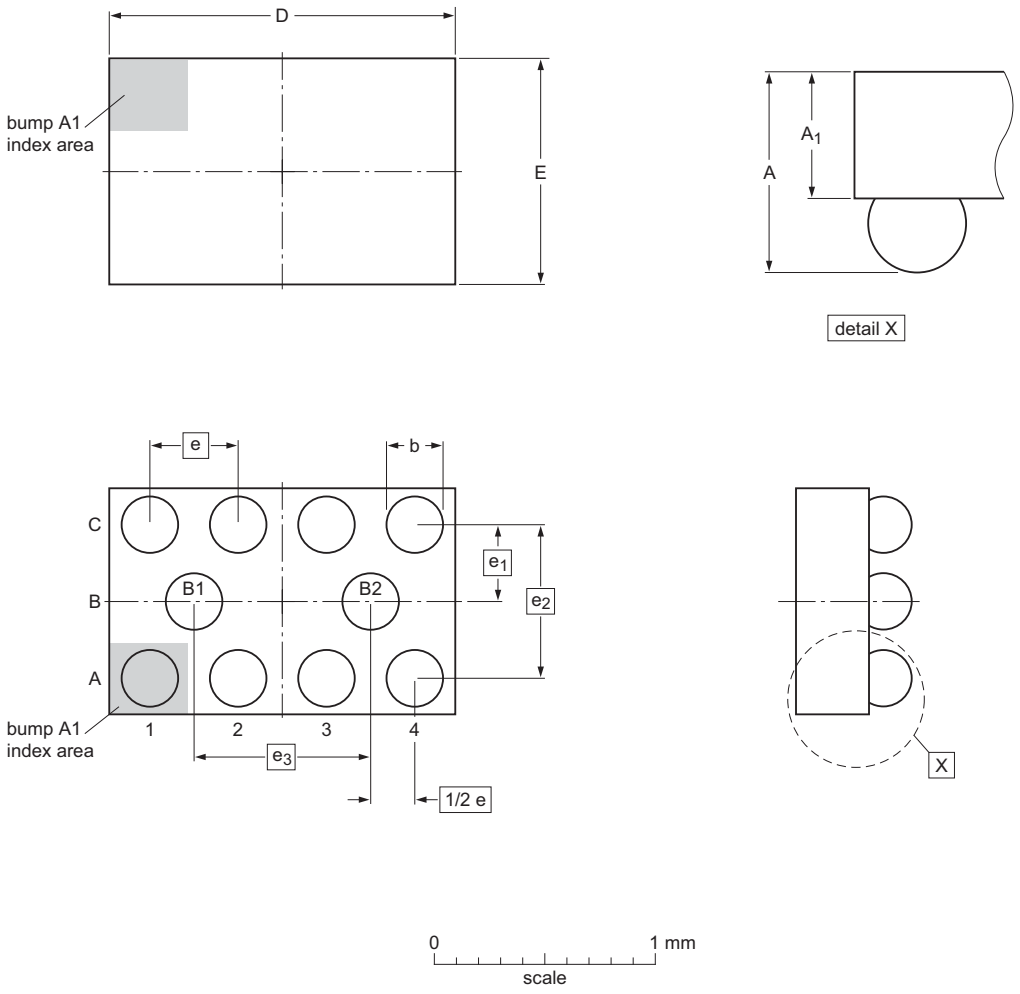
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCMF1USB30						16-03-22

Fig 24. Package outline WLCSP5

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WLCSP10: wafer level chip-size package; 10 bumps (4-2-4) **PCMF2USB30**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	D	E	e	e_1	e_2	e_3
mm	max	0.60	0.38	0.31	1.62	1.22				
	nom	0.57	0.37	0.26	1.57	1.17	0.40	0.40	0.80	0.80
	min	0.54	0.36	0.21	1.52	1.12				

pcmf2usb30_po

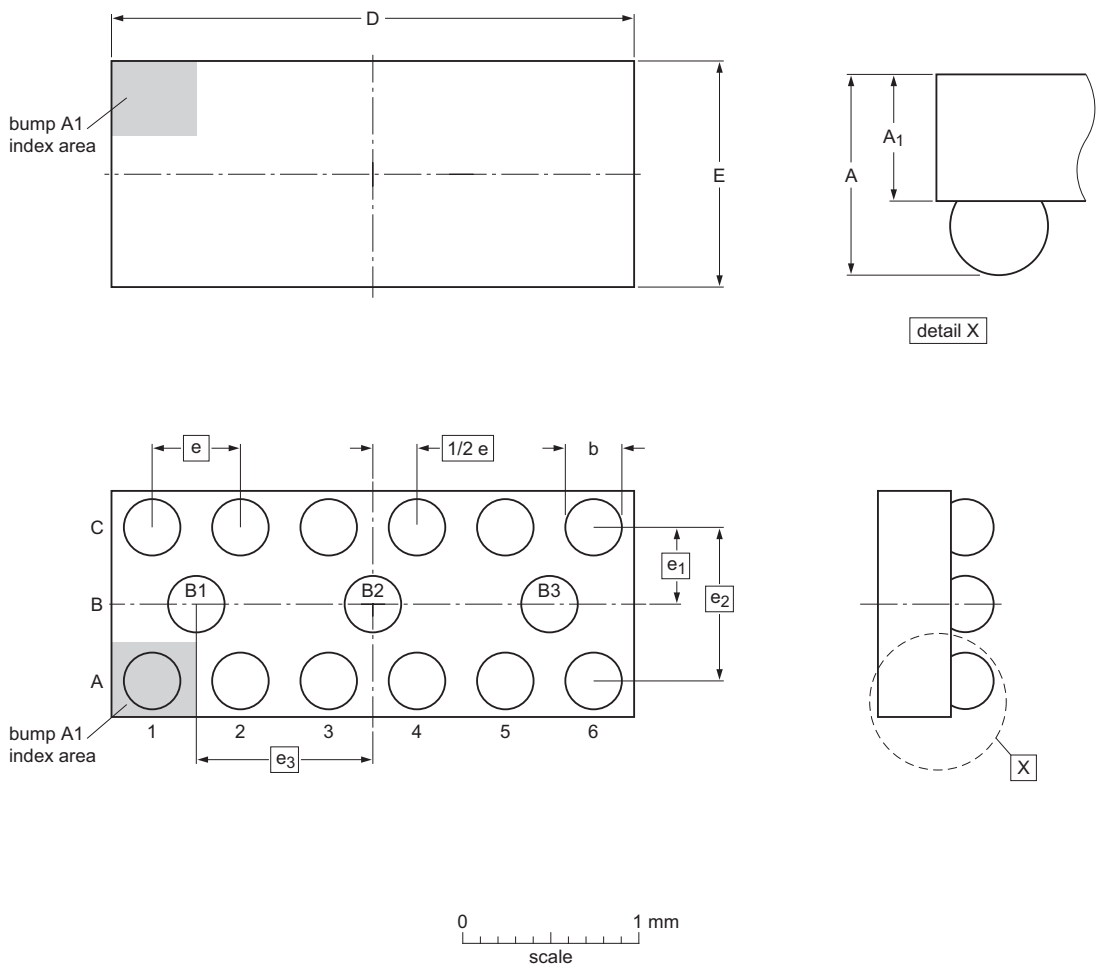
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCMF2USB30						16-03-22

Fig 25. Package outline WLCSP10

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WLCSP15: wafer level chip-size package; 15 bumps (6-3-6) **PCMF3USB30**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	D	E	e	e_1	e_2	e_3
mm	max	0.60	0.38	0.31	2.42	1.22				
	nom	0.57	0.37	0.26	2.37	1.17	0.40	0.40	0.80	0.80
	min	0.54	0.36	0.21	2.32	1.12				

pcmf3usb30_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCMF3USB30						16-03-22

Fig 26. Package outline WLCSP15

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9. Soldering

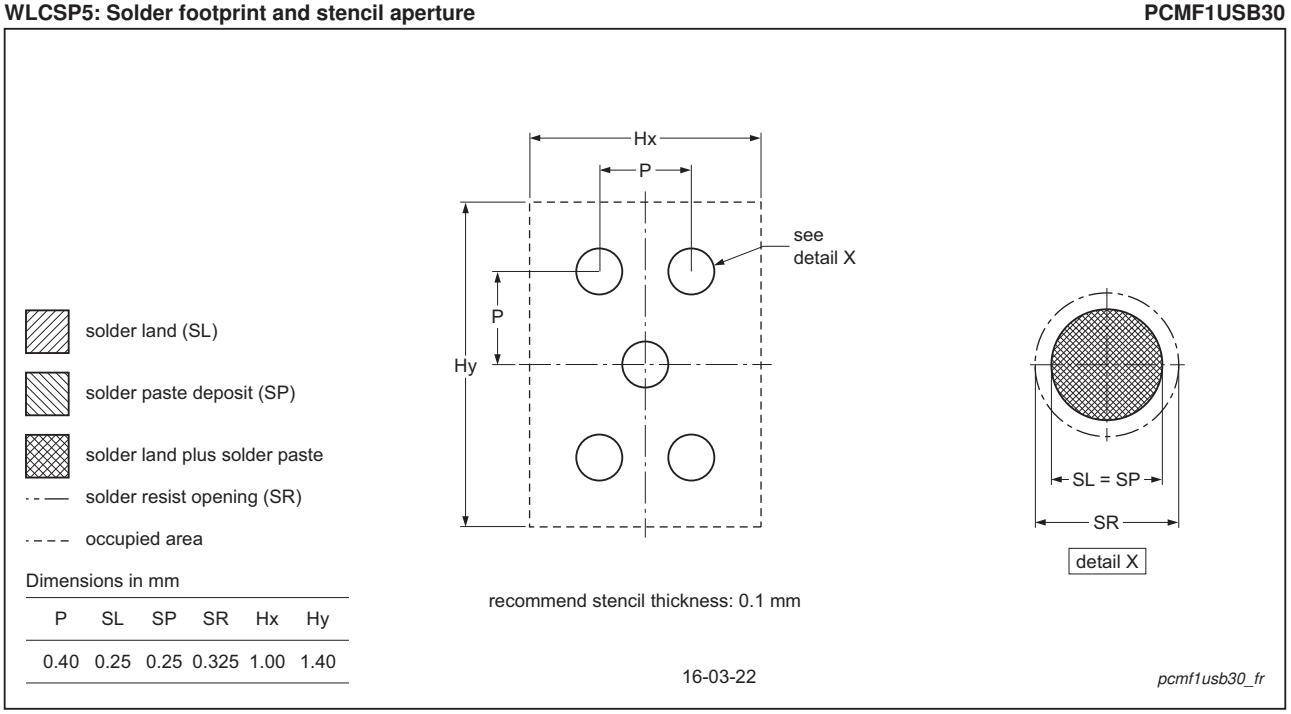
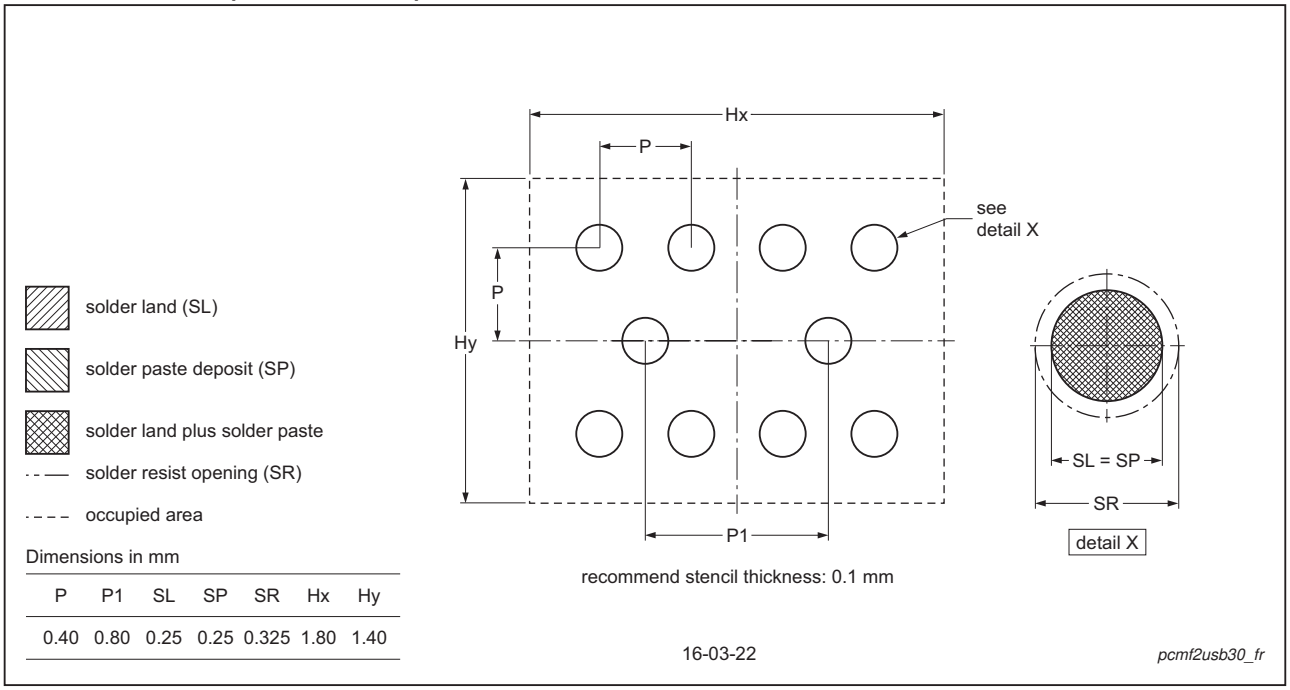


Fig 27. Soldering footprint WLCSP5 (PCMF1USB30)

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WLCSP10: Solder footprint and stencil aperture **PCMF2USB30**

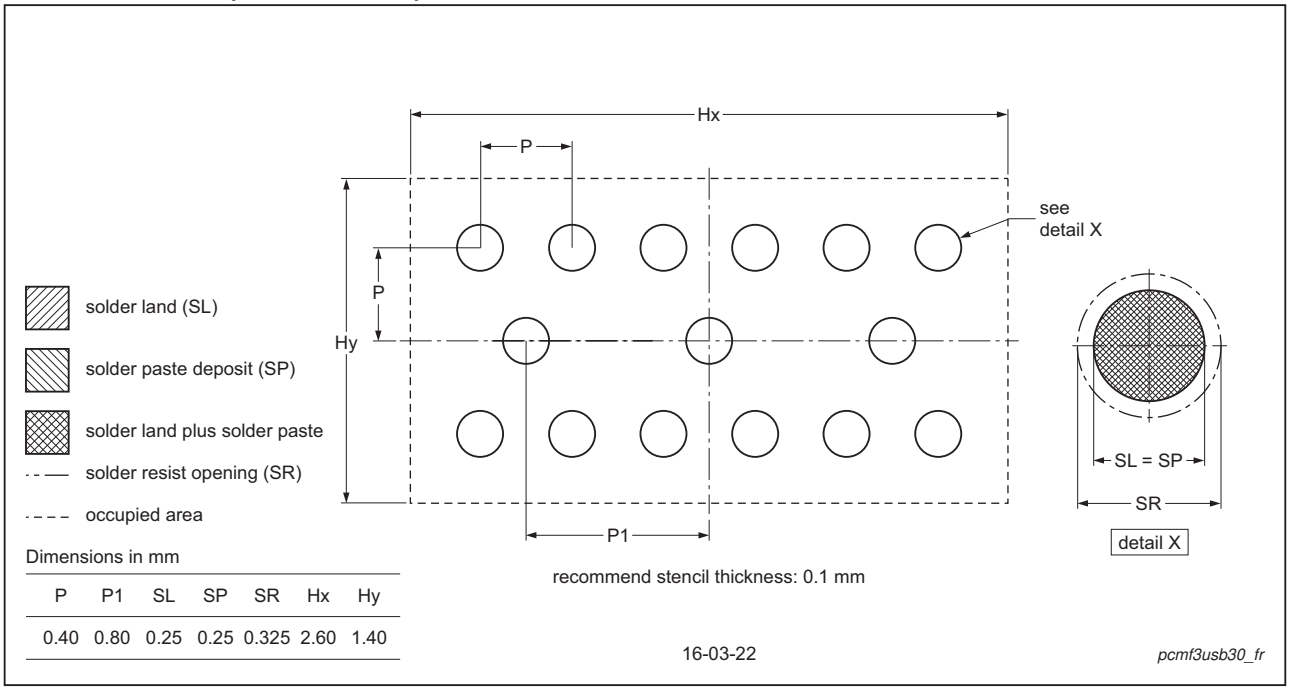


Dimensions in mm

P	P1	SL	SP	SR	Hx	Hy
0.40	0.80	0.25	0.25	0.325	1.80	1.40

Fig 28. Soldering footprint WLCSP10 (PCMF2USB30)

WLCSP15: Solder footprint and stencil aperture **PCMF3USB30**



Dimensions in mm

P	P1	SL	SP	SR	Hx	Hy
0.40	0.80	0.25	0.25	0.325	2.60	1.40

Fig 29. Soldering footprint WLCSP15 (PCMF3USB30)

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10. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCMFXUSB30_SER v.1	20160401	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 01 April 2016