PD69201

1-Port PSE PoE Manager

Introduction

Microchip's PD69201 device is an IEEE® 802.3af and IEEE 802.3at compliant single-port Power over Ethernet (PoE) Manager, used in Ethernet switches to allow network devices to share power and data over the same cable. With minimal external components, the PD69201 supports both IEEE 802.3af/at and Legacy Powered Devices (PDs). Integrating power, analog, and state-of-the-art logic, the PD69201 is available in a 10-pin, 3 mm × 4 mm DFN package.

Features

- Fully IEEE 802.3af and at compliant
- Includes two-event classification
- Supports pre-standard PD detection
- Single DC voltage input (32V–57V)
- Wide temperature range: –40°C to 85°C
- Low thermal dissipation (internal 100 mΩ sense resistor)
- I^2C communication
- Continuous port and system data monitoring
- Power soft-start mechanism
- On-chip thermal protection
- Voltage monitoring and protection
- Internal power-on reset
- RoHS compliant
- MSL1

Application Block Diagrams

The PD69201 may be used in either an unmanaged standalone or a managed configuration.

Figure 1. Unmanaged Application

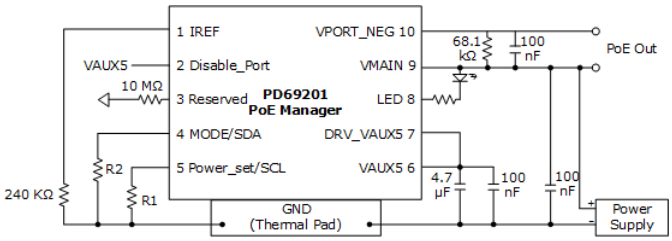


Figure 2. Managed Application

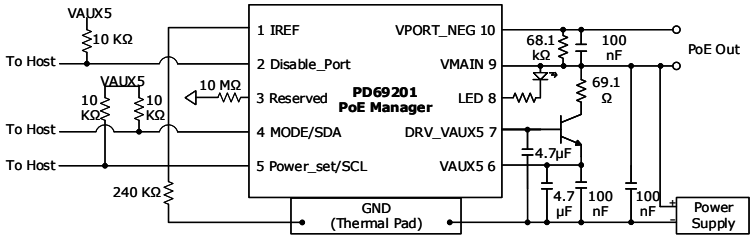


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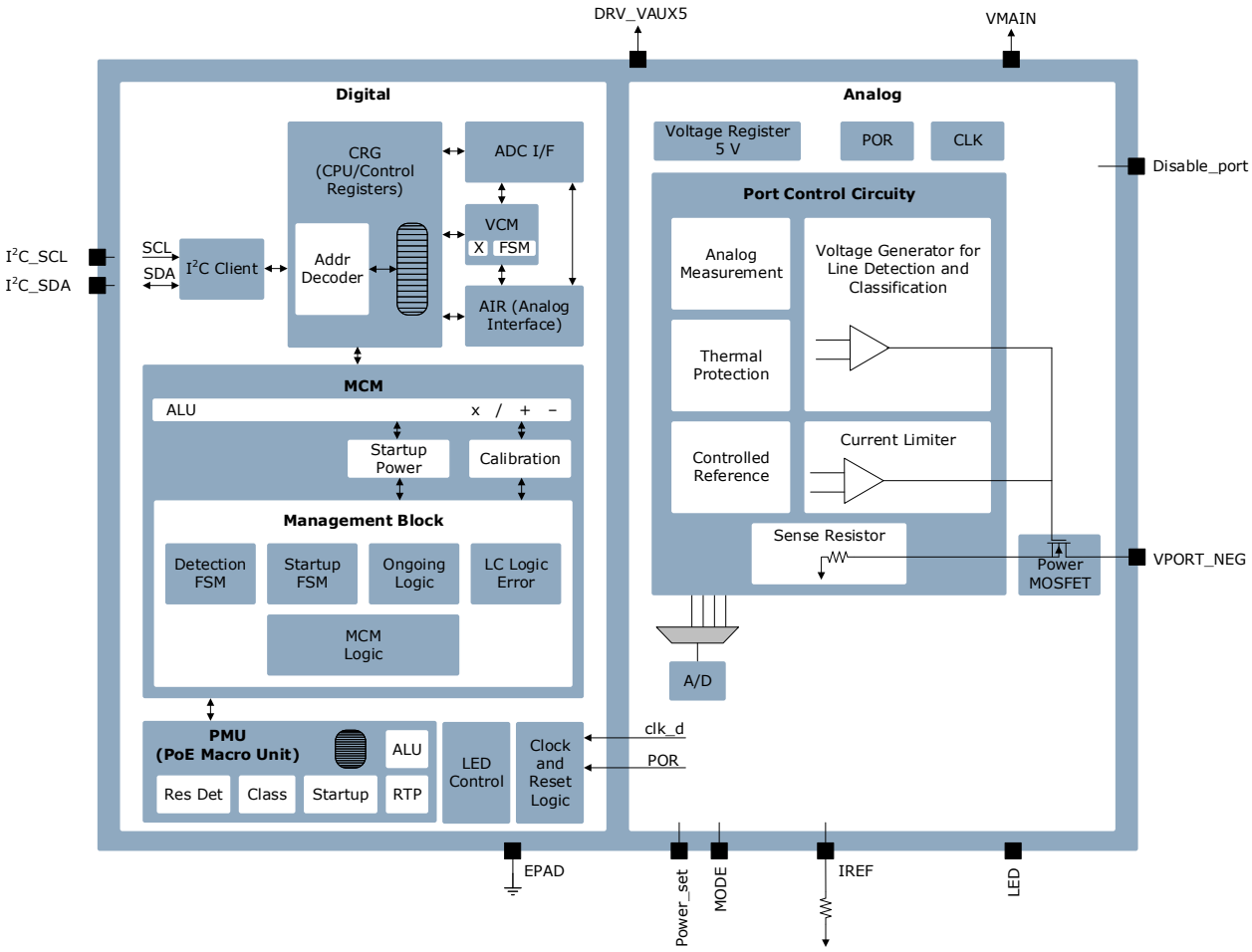
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1. Functional Descriptions

The PD69201 device has two major sections: a digital section that controls and monitors the logical PoE functions (state machines, timings, and so on) and an analog section that performs the front-end analog PoE functionality.

The following illustration shows the internal functional blocks of the PD69201 device.

Figure 1-1. PD69201 Internal Block Diagram



1.1 I²C Communication

The PD69201 can be controlled via I²C bus, based on registers access. There are two I²C addresses that can be set (0x20 or 0x21). I²C address is set by pin 8.

1.1.1 Features

- I²C Client mode only.
- Data rate: 0 kbps–100 kbps
- Broadcast address: 0x00
- Watchdog reset. Resets the block if I²C input clock halts for 0.5s during a transaction.
- Host does not need to support I²C clock stretching.

1.1.2 Setting Capability

- Port enable/disable
- Operating modes
  - Power delivered over Alt A/B
  - Current limit setting (I_{LIM})
  - Legacy detection enable/disable

1.1.3 Reading Capability

- Port voltage
- IEEE 802.3at detection result
- Classification result
- Port status

The following illustration shows the I^2C sequence for both write and read transactions.

Figure 1-2. I^2C Sequence

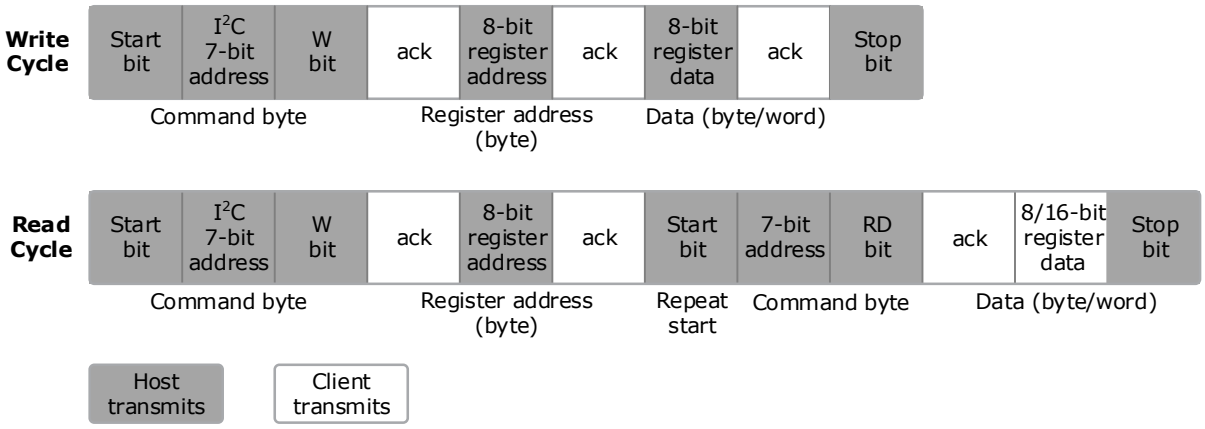


Table 1-1. I²C Commands

Name	Address	Width	Field	Bits	Type	Reset Value	Description
PORT_TYPE	0x00	7	AF_AT	2:0	R/W	7	Mode, ICUT, and ILIM are listed as follows. 0: AF, 375 mA, 425 mA (No Class) 1: AF1, Disabled, 110 mA (No Class) 2: AF2, Disabled, 195 mA (No Class) 3: AF3, Disabled, 280 mA (No Class) 4: AT1, Disabled, 485 mA (No Class) 5: AT2, Disabled, 607 mA (No Class) 6: AT3, Disabled, 970 mA (Class) 7: AT, 642 mA, 720 mA (Class)
			Reserved	3	R/W	—	—
			ALT	6:4	R/W	7	Value equals 3 MSB of ADC R_{MODE} measurement. 0: AltB Res 1, 6, 7: AltB Res+Cap 2: AltA Res 3: AltA Res+Cap
VPORT_L	0x02	8	DATA	[7:0]	RO	—	Port voltage. Updated every 1 ms. Host must first read VPORT_L, then VPORT_ H. Resolution: 58.6 mV per bit.

.....continued

Name	Address	Width	Field	Bits	Type	Reset Value	Description
VPORT_H	0x03	8	DATA	1:0	RO	—	The 2 ms bits of port voltage reading (total 10 bits includes reg 0x02). Updated every 1 ms. Host must first read VPORT_L, then VPORT_H. Resolution: 58. 6 mV per bit.
			VALID	2	Clear on read (COR)	0	V_{PORT} measurement is valid. 1: Data was not read by the host. 0: Data was already read by the host.
			UDL_EVENT	3	R/W	0	Under-load indication 0: No event. 1: Event occurred. This bit is not COR, and should be cleared by the host.
			OVT_EVENT	4	R/W	0	Over-temperature indication (155°C +/- 15°C) 0: No event. 1: Event occurred. This bit is a real-time indication (no latch).
			OVL_EVENT	5	R/W	0	Over-load indication 0: No event. 1: Event occurred. In AF modes, can also be set in T_{LIM} events. This bit is not COR, and should be cleared by the host.
			SC_EVENT	6	R/W	0	Short circuit indication 0: No event. 1: Event occurred. This bit is not COR, and should be cleared by the host.

.....continued

Name	Address	Width	Field	Bits	Type	Reset Value	Description
TLIM	0x04	8	TLIM	0	R/W	0	T_{LIM} event indication 0: No event. 1: Event occurred. In AF, OVT_EVENT can be set in case of T_{LIM} events. This bit is not COR, and should be cleared by the host.
			LD_ERR	1	R/W	0	Repetitive over load indication 0: No event. 1: Event occurred. This bit is not COR, and should be cleared by the host.
			DIS_PRT	2	R/W	0	Disable_port external pin high-to-low event. 0: No event. 1: Event occurred. This bit is not COR, and should be cleared by the host.
			SU_DVDT_FAIL	3	R/W	0	Port turned off due to high inrush current (dV/dt). 0: No event. 1: Event occurred. This bit is not COR, and should be cleared by the host.
			SU_SC_FAIL	4	R/W	0	Port turned off due to short during start-up. 0: No event. 1: Event occurred. This bit is not COR, and should be cleared by the host.
			OVT_EVENT	6	R/W	0	Over-temperature indication (155°C +/- 15°C) 0: No event. 1: Event occurred. This bit is not COR, and should be cleared by the host.

.....continued

Name	Address	Width	Field	Bits	Type	Reset Value	Description
			RPR_EVENT	7	R/W	0	Port external voltage feed indication 0: No event. 1: Event occurred. This bit is not COR, and should be cleared by the host.
STATUS	0x0B	7	RES_DET	1:0	RO	0	0: Open 1: Fail 2: Pass 3: Pass_res_cap
			CLASS	4:2	RO	0	0: reset_value 1: class_ovl_err (above 50 mA) 2: class_diff_err (1st class event is different then 2nd class event) 3: class_0123 4: class_4
			PDP	5	R/W	0	Port delivering power indication If host writes 0, port shutdown momentary (push-button). 1: Port is delivering power. Startup succeeded. RTP is working. 0: Port is not delivering power. Host shall not write 1, only 0.
			SU_FAIL	6	RO	0	1: Startup fail indication.
SW_USE	0x0D	5	User bits	[3:0]	R/W	0	Software read/write register (general use). Detects a reset by setting register to non-zero value and reading it periodically.
			SPARE_IN	[4]	RO	—	—
SW_RST	0x0E	8	GEN	[7:0]	WO	—	Reset can be generated by the host writing 0xAB (push-button functionality).

.....continued

Name	Address	Width	Field	Bits	Type	Reset Value	Description
RST_SRC	0x0F	3	POR	[0]	R/W	1	Power-on-reset has occurred. This bit is not COR, and should be cleared by the host.
			SW_RST	[1]	R/W	0	Software reset has occurred. This bit is not COR, and should be cleared by the host.
			I2C_WD_RST	[2]	R/W	0	I^2C module watchdog reset has occurred (reset does not influence PoE functionality).
CHIP_REV_L	0x10	6	DATA	[5:0]	RO	—	Chip digital version [2:0] = digital_ver_d[2:0] V1R1='001'b , V3R1='001'b Chip analog version[5:3] = analog_ver_d[5:3] V1R1='001'b , V3R1='010'b
PORT_LED	0xB5	2	OFF	[0]	R/W	0	Set the control of the LED 0: LED operated by the PD69201. 1: LED operated by external host (using bit 1).
			EN	[1]	R/W	1	Open-drain output control. Need to set only after bit 0 was set to 1 (not in the same command). 0: LED pin on. 1: LED pin off.
DISABL_PORT	0xD9	2	SEL	[0]	R/W	0	Disable port pin control 0: External pin enabled. 1: External pin disabled, external host controls the port through bit 1. When setting bit to 0, port immediately starts detection cycle (can be used for sync).
			VAL	[1]	R/W	0	Disable port (when bit 0= 1) 0: Port disable. 1: Port enable.

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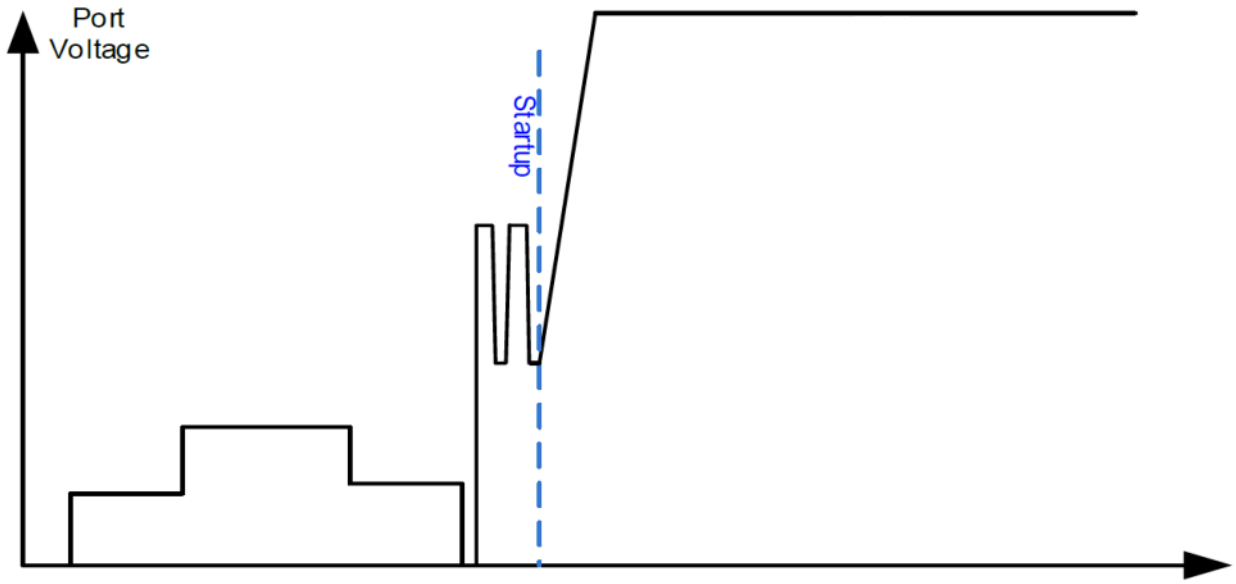
1.2 Detection and Classification

The PD69201 signature detection is IEEE 802.3at-compliant. Pre-standard or legacy detection may also be enabled.

Detection is executed in three levels to guarantee power delivering to a valid PD.

Following a successful detection, the PD69201 generates two classification events per the IEEE 802.3at standard.

Figure 1-3. Detection and Classification



1.3 Port Start-Up

Upon successful detection and classification, power is applied via a controlled start-up mechanism.

As defined by IEEE 802.3at, during the startup period, the current is limited to 425 mA for a duration of 65 ms, allowing the PD's capacitors to charge to the steady state power condition.

1.4 Over-Load and Short-Circuit Protection

After successful power-up, the PD69201 initializes its internal protection mechanism that monitors and disconnects power from the port in cases of over-current or short circuit, as specified by IEEE 802.3af/at.

1.5 Maintain Power Signature (MPS)

The no-load function detects if a PD is still connected to the port by measuring the port current over time and comparing it to current and time thresholds.

The MPS parmeters are fixed: TMPDO= 324 ms, TMPS= 48 ms, I_{MPS}= 7.5 mA.

1.6 Over-Temperature Protection

A thermal sensor is located inside the PD69201.

In the case of an over-temperature event, the port will be turned off.

1.7 LED

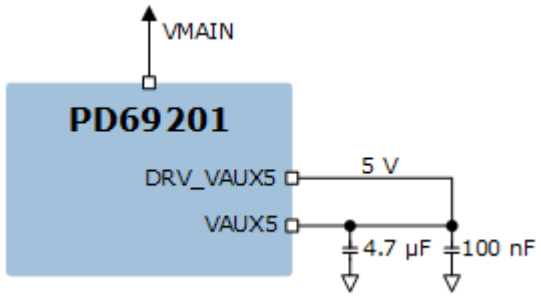
Table 1-2. LED

State	LED
Port on	ON
Port OVL/short/dvdt error/res fail/class error	Blink 1 Hz
V_{MAIN} voltage out of range or IC over temperature	Blink 4 Hz
Port off, UDL	OFF
Idle	Pulse of 30 ms every 2s

1.8 Auxiliary 5 V_{DC} Power Options

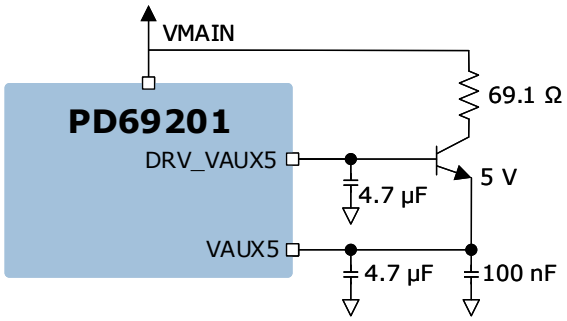
The PD69201 has an internal 5 V_{DC} regulator, which eliminates the need for an external DC/DC converter. This is option 1, as shown in the following figure. To use the internal regulator, connect DRV-VAUX5 (internal regulator output) to VAUX5.

Figure 1-4. Option 1



In case it is required to use the 5 V for external periphery, the 5 V_{DC} regulator can be boosted by an external transistor, which enables powering peripheral circuitry up to 20 mA. This is option 2, as shown in the following figure.

Figure 1-5. Option 2



1.9 Power_set Pin (Unmanaged Mode)

In the Unmanaged mode of operation, pin 5 sets the power limit of the port, based on a resistor connected from the pin to GND.

The following table describes the power levels.

Table 1-3. Power_set Pin

Level	Resistor Value	I_{LIM} (typ)	I_{CUT} (OVL)	Class Events
0	0 Ω	430 mA[1]	Enabled (375 mA)	No
1	15 kΩ	111 mA	Disabled	No
2	34.8 kΩ	197 mA	Disabled	No
3	59 kΩ	283 mA	Disabled	No
4	86.6 kΩ	490 mA	Disabled	No
5	118 kΩ	614 mA	Disabled	No
6	154 kΩ	981 mA	Disabled	2 Events
7	200 kΩ	759 mA[2]	Enabled (637 mA)	2 Events

1. IEEE 802.3af Class 3
2. IEEE 802.3at Class 4

1.10 MODE Pin (Unmanaged Mode)

In the Unmanaged mode of operation, pin 4 sets the the operation mode of the PD69201, based on a resistor connected from the pin to GND.

The following table describes the power levels.

Table 1-4. MODE Pin

Level	Resistor Value	Alt A/B	Detection
0	0 Ω	Alt B	IEEE
1	15 kΩ	Alt B	IEEE+ Pre-Standard
2	34.8 kΩ	Alt A	IEEE
3	59 kΩ	Alt A	IEEE+ Pre-Standard

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2. Electrical Specifications

The following sections describe the electrical specifications of the PD69201 device.

2.1 Absolute Maximum Ratings

The following table lists the absolute maximum ratings for the PD69201. Exceeding these ratings can cause damage to the device. All voltages are with respect to ground. Currents are marked positive when flowing into a specified terminal and marked negative when flowing out of a specified terminal. Drv_vaux5 pin should not be forced to any voltage from external source.

Table 2-1. Absolute Maximum Ratings

Parameter	Rating
Supply input voltage (V_{MAIN})	–0.3V to 72V
LED	–0.3V to V_{MAIN} + 0.5
Port_Neg pin	–0.3V to V_{MAIN} + 0.5
VAUX5	–0.3V to 5.5V
GND (thermal pad)	–0.3V to 5.5V
All other pins	–0.3V to 5.5V
Operating ambient temperature range	–40°C to 85°C
Maximum junction temperature	150°C
Storage temperature range	–65°C to 150°C
ESD protection at all I/O pins	±2KV (HBM)

2.2 Recommended Operating Conditions

The following table lists the recommended operating conditions for the PD69201.

Table 2-2. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Input voltage	V_{MAIN}	32	57	V
Recommended operating junction temperature	T_J Operating	—	125	°C

2.3 Test Specifications

Unless otherwise specified, the minimum and maximum ratings apply to the operating ambient temperature (T_{AMB}): –40°C to 85°C and tested at 55V. Typical values stated are either by design or by production testing at 25°C ambient.

Table 2-3. Power Supply

Parameter	Symbol	Test Conditions/ Comment	Min.	Typ.	Max.	Unit
Power supply current at operating mode	—	V_{MAIN} = 57V Port is on.	—	—	5	mA

Table 2-4. Digital I/O (SDA, SCL)

Parameter	Symbol	Test Conditions/ Comment	Min.	Typ.	Max.	Unit
Input logic, high threshold	V_{IH}	—	0.6* V_{AUX5}	—	—	V
Input logic, low threshold	V_{IL}	—	—	—	0.8	V
Input high current	I_{IH}	—	–10	—	10	µA
Input low current	I_{IL}	—	–10	—	10	µA
Output low voltage	V_{OL}	I_{OH} = 1 mA	—	—	0.4	V

Table 2-5. Current Limit

Parameter	Symbol	Test Conditions/ Comment	Min.	Typ.	Max.	Unit
Current Limit	I_{LIM}	Custom setting for 4 W	105	111	117	mA
		Custom setting for 7 W	186	197	208	mA
		Custom setting 10 W	268	283	298	mA
		IEEE 802.3af Class 3 setting for 15.4 W	400	430	450	mA
		Custom setting for 20 W	464	490	516	mA
		Custom setting for 25 W	581	614	647	mA
		IEEE 802.3at Class 4 setting for 30 W	684	759	800	mA
		Custom setting for 40 W	928	981	1034	mA

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Table 2-6. Current Limit Timing

Parameter	Symbol	Test Conditions/ Comment	Typ.	Unit
Current Limit Timing	T_{LIM}	4W	64	ms
		7W	64	ms
		10W	64	ms
		IEEE 802.3af Class 3 (15.4W)	64	ms
		20W	12	ms
		25W	12	ms
		IEEE 802.3at Class 4 (30W)	7	ms
		40W	12	ms

Table 2-7. Over-Current Indication

Parameter	Symbol	Test Conditions/ Comment	Min.	Typ.	Max.	Unit
ICUT_AT	I_{CUT}	—	600	637	684	mA
ICUT_AF	I_{CUT}	—	350	375	400	mA

Table 2-8. Main Power Switching FET

Parameter	Symbol	Test Conditions/ Comment	Min.	Typ.	Max.	Unit
Output leakage	$I_{LEAKAGE}$	At port off state. V_{PORT}= 57 V	—	—	12	µA
Total channel resistance	Ron = Rdson+sense Res + bonding resistance	At port on state, at I_{PORT}= 0.1 A	—	0.44	0.7	Ω

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Table 2-9. Classification Voltage Generation

Parameter	Symbol	Test Conditions/ Comment	Min.	Typ.	Max.	Unit
Class event output voltage	—	Measured between VMAIN and VPORT_NEG pins (for both class blocks on port). Load Current= 1 mA, 30 mA, and 60 mA	15.5	18	20.5	V
Mark event output voltage	—	Measured between VMAIN and VPORT_NEG pins (for both class blocks on single port). Load current= 1 mA and 10 mA	7	8.5	10	V
Class event current limitation	I_CLASS_LIM	—	51	71	100	mA

Table 2-10. POR Cell

Parameter	Symbol	Test Conditions/ Comment	Min.	Typ.	Max.	Unit
POR high threshold	—	—	4.1	—	4.35	V

Table 2-11. Disable Port Pin/I²C_address Pins

Parameter	Symbol	Test Conditions/ Comment	Min.	Typ.	Max.	Unit
Disable_port/ I²C_address logic high threshold	V_{IH}	—	—	2.2	—	V
Disable_port/ I²C_address logic low threshold	V_{IL}	—	—	—	0.4	V

Table 2-12. LED

Parameter	Symbol	Test Conditions/ Comment	Min.	Typ.	Max.	Unit
Low level voltage	V_{LOW}	Sink current from V_{MAIN} I_{SINK}= 5 mA	—	—	1	V

3. Pin Descriptions

The following figure and table describe the pins of the PD69201 device.

Figure 3-1. PD69201 Pinout

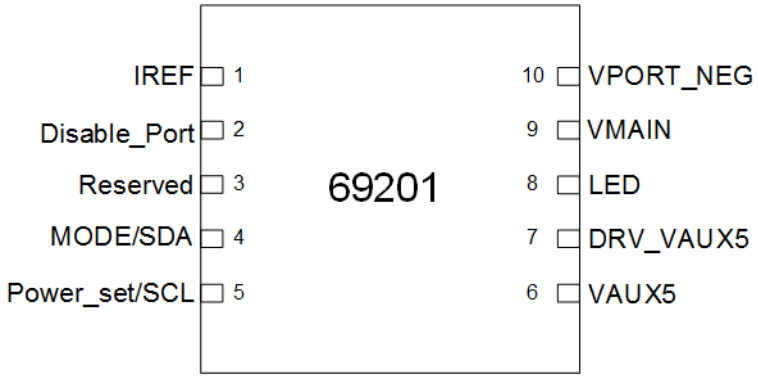


Table 3-1. Pin Descriptions

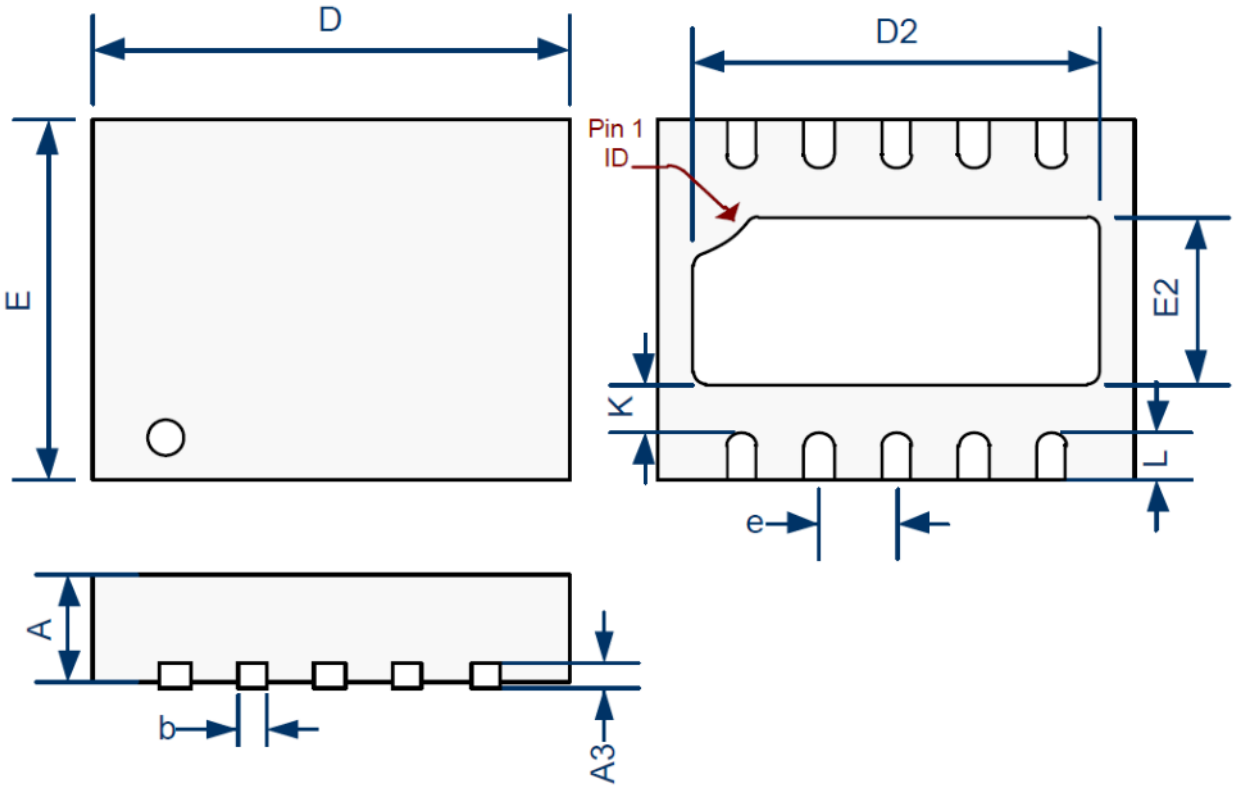
Number	Name	Type	Description
0	PAD	GND-power	Exposed PAD: Connect to analog ground. Maximum the Ground plane (especially on the bottom layer) for optimal thermal performance. Use recommended footprint. (See *PD69201 Layout Design Guidelines*).
1	IREF	Analog input	Reference resistor pin. Connect a 240 kΩ 1% resistor to AGND.
2	Disable_Port	Analog I/O	Enable/disable port pin: When applying 5 V—port enable, 0 V—port disable.
3	Reserved	N/A	Reserved pin. Do not connect externally.
4	MODE/SDA	Analog Input/DIO	Dual purpose: Mode select pin (by connecting external resistor to ground). I^2C SDA signal for PD69201.
5	Power_set/SCL	Analog Input/DI	Dual purpose: Mode select pin (by connecting external resistor to ground). I^2C SDA signal for PD69201.
6	VAUX5	Power	Regulated 5 V output voltage source; Connect to filtering capacitors (4.7 uF + 100 nF).
7	DRV_VAUX5		See section Auxiliary 5 V_{DC} Power Options.
8	LED	Analog I/O	Dual purpose: Current sink for controlling external LED. I^2C address setting for PD69201 (low sets to address 0x20; high sets to address 0x21). **Note:** When an LED is connected to the pin, it sets to address 0x21.
9	VMAIN	Power	Main high-voltage supply voltage. A low ESR 100 nF (or higher) bypass capacitor, connected to AGND, should be placed as close as possible to this pin through low-resistance traces.
10	VPORT_NEG	Analog I/O	Negative port output.

4. Package Specifications

This section provides the package drawing, RoHS and solder reflow information, and thermal specifications for the PD69201 device.

The PD69201 package is a 3 mm × 4 mm, 10-pin DFN, as shown in the following figure.

Figure 4-1. DFN Package



Dimensions do not include protrusions; these shall not exceed 0.155 mm (0.006”) on any side. Lead dimension shall not include solder coverage.

Table 4-1. Package Dimensions

Dimension	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.80	1.00	0.031	0.039
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	4.00 BSC		0.236 BSC	
E	3.00 BSC		0.315 BSC	
D2	3.30	3.5	0.130	0.138
E2	1.30	1.5	0.051	0.059
e	0.65 BSC		0.026 BSC	
K	0.30	—	0.012	—
L	0.30	0.45	0.012	0.018

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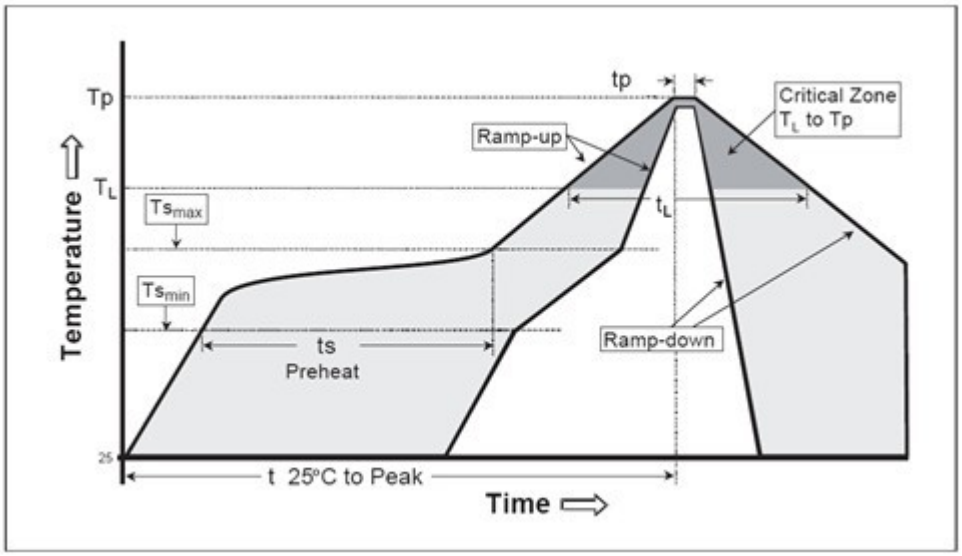
4.1 RoHS and Solder Reflow Information

- RoHS 6/6
- Pb-free NiPdAu pin finish
- Package peak temperature for solder reflow (40s maximum exposure)—260°C (0°C, –5°C)

Table 4-2. Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-up Rate (TSmax to Tp)	3°C/second max	3°C/second max
Preheat		
Temperature Min (TS_{min})	100°C	150°C
Temperature Max (TS_{max})	150°C	200°C
Time (ts_{min} to ts_{max})	60s to 120s	60s to 180s
Time Maintained		
Temperature (T_L)	183°C	217°C
Time (t_L)	60s to 150s	60s to 150s
Peak Classification Temperature (TP)	210°C to 235°C	240°C to 255°C
Time within 5 °C of Actual Peak Temperature (tp)	10s to 30s	20s to 40s
Ramp-Down Rate	6°C/second max	6°C/second max
Time 25 °C to Peak Temperature	6 minutes max	8 minutes max

Figure 4-2. Classification Reflow Profiles



4.2 Thermal Specifications

The following table lists the thermal specifications for the PD69201 device.

Table 4-3. Thermal Specifications

Typical Thermal Resistance	Value
Junction to ambient (T_A)	36.4°C/W
Junction to case (T_C) (bottom)	0.94°C/W
Junction to board (T_B)	9.05°C/W

The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All specifications assume no ambient airflow.

4.3 Recommended PCB Footprint

The following figures illustrate the PCB footprint pattern for PD69201. Units are in mm [mils].

Figure 4-3. Top Solder Mask

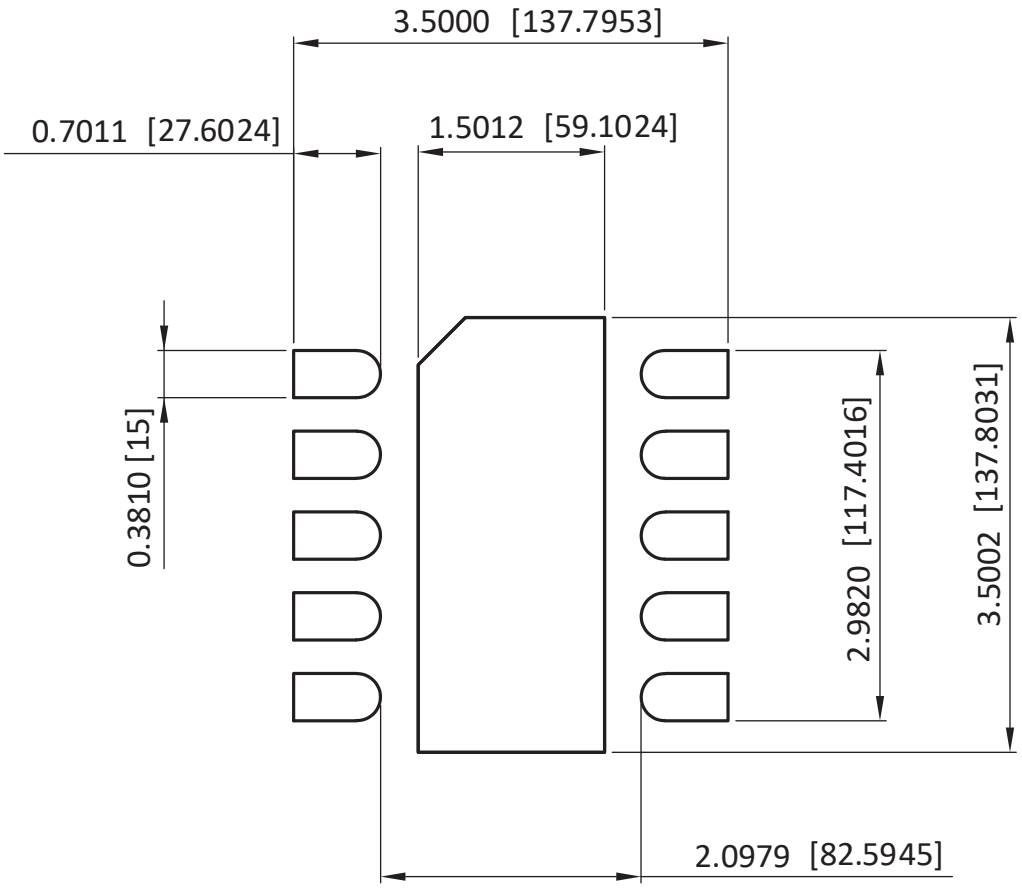


Figure 4-4. Top Copper

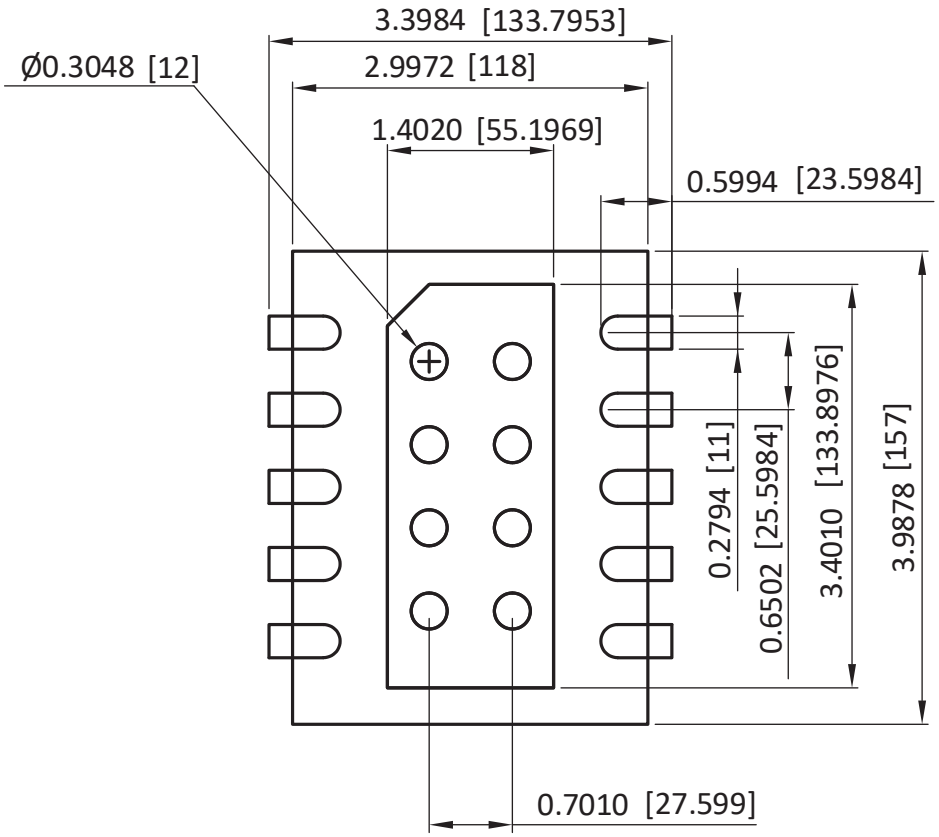


Figure 4-5. Bottom and Internal Layer Copper

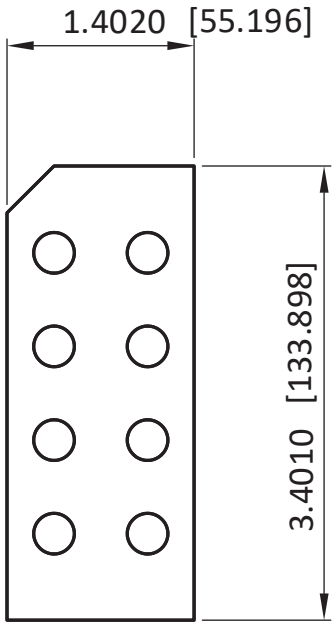


Figure 4-6. Top Paste Mask

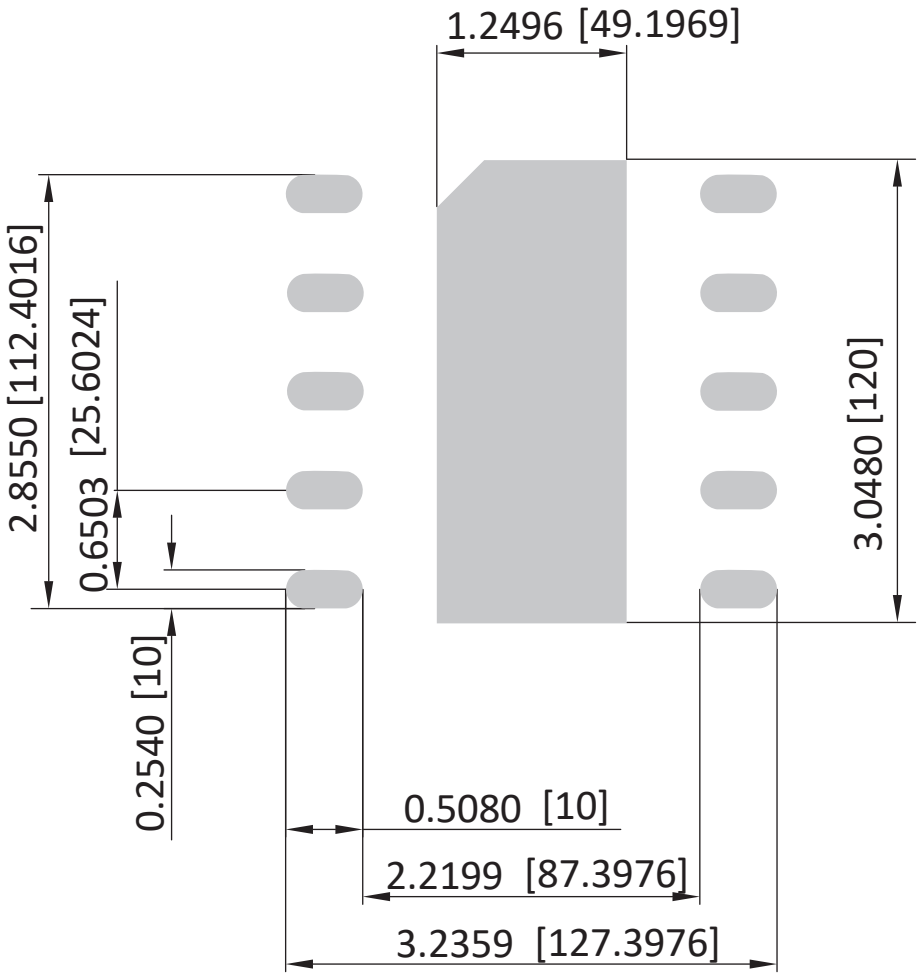
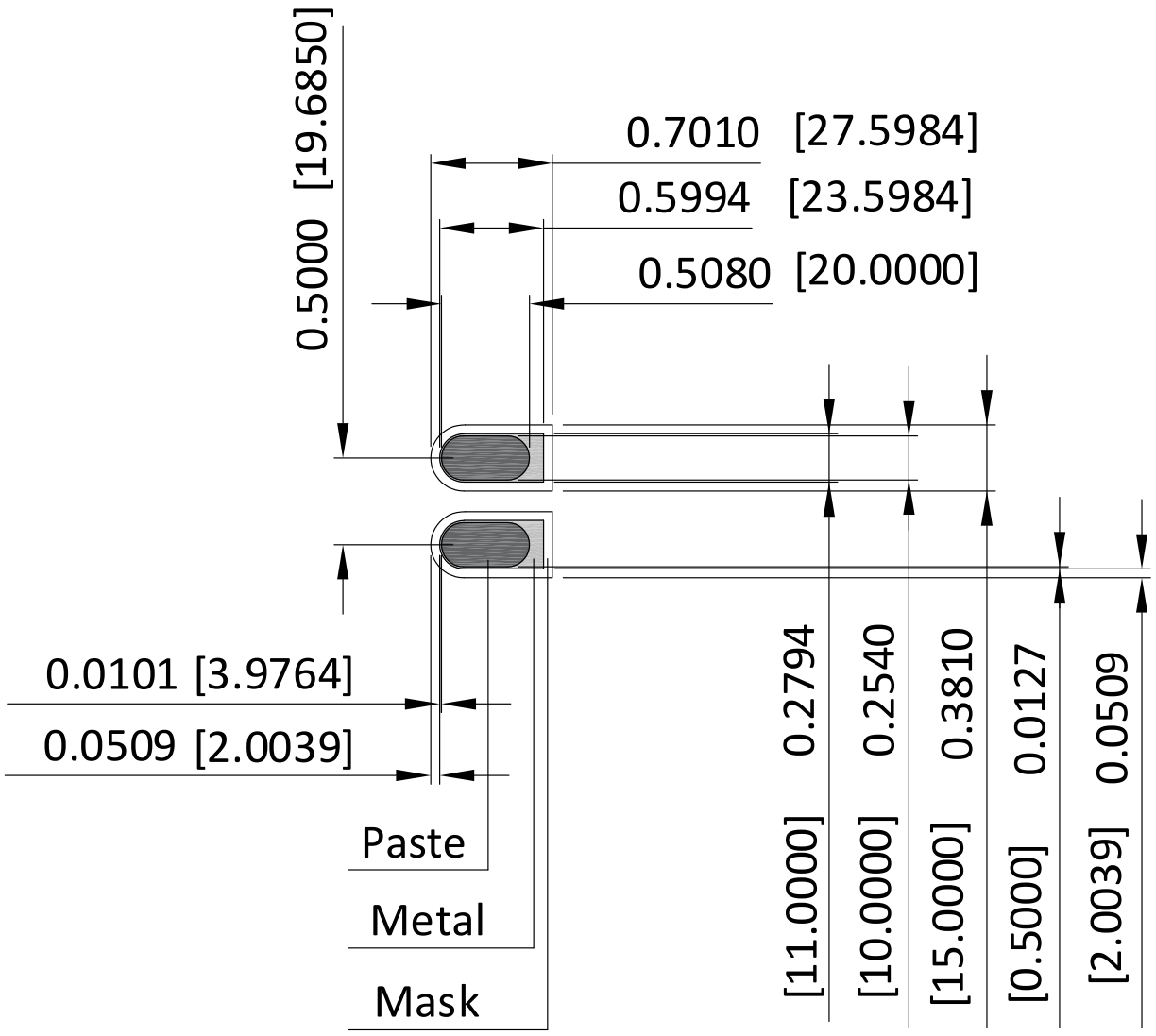


Figure 4-7. Top Layer Pin Geometry



5. Ordering Information

The following table lists the ordering information for the PD69201 device.

Table 5-1. Ordering Information

Part Number	Package	Packaging Type	Temperature	Part Marking
PD69201ILD-TR	Plastic 10-pin DFN: 3 mm × 4 mm	Tape and Reel	–40°C to 85°C	69201 ZZ[1] YYWWNNN[2]

1. ZZ= Random character
2. YY= Year; WW= Week; NNN= Trace code

6. Revision History

Revision	Date	Description
E	January 2022	The following is a summary of changes in revision E of this document: • Updated Reset Values, ALT values, and OVT_EVENT description in I^2C Commands table. • Updated I_{CUT} (OVL) value for Level 7 in Power_set Pin table.
D	January 2021	The following is a summary of changes in revision D of this document. • Added NPN transistor, 69.1 Ω resistor, and 4.7 µF capacitor to pin 7 in Managed Application figure. • Updated "DNIE_LD_ERR" to "LD_ERR" in I^2C Commands table. • Added "V_{MAIN} voltage out of range or IC over temperature"/ "Blink 4 Hz" and "Idle" / "Pulse of 30 ms every 2 s" rows to LED table. • Added resistor 69.1 Ω to NPN transistor in Option 2 figure. • Changed "Power" column to "I_{LIM} (typ)" column and updated values in Power_set Pin table. • Added MHz values for I_{CUT} Enabled mode in Power_set Pin table. • Updated "af/at" information in Current Limit Timing table. • Added Recommended PCB Footprint section.
C	September 2020	The following is a summary of changes in revision C of this document. • Updated the PD69201 Internal Block Diagram figure. For more information, see Figure 1-1. • Updated the figure and the table in the Reading Capability section. For more inofrmation, see 1.1.3. Reading Capability. • Updated the MODE Pin table. For more inofrmation, see Table 1-4.
B	September 2020	Updated LED details in Table 3-1.
A	May 2020	Initial Revision

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ISBN: 978-1-5224-9618-2

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