DATA SHEET

PDTA144E series

PNP resistor-equipped transistors;
R1 = 47 kΩ, R2 = 47 kΩ

Product data sheet
Supersedes data of 2003 Apr 10

2004 Aug 05

NXP founded by Philips

PNP resistor-equipped transistors; R1 = 47 kΩ, R2 = 47 kΩ

PDTA144E series

FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{CEO}	collector-emitter voltage	–	−50	V
I_O	output current (DC)	–	−100	mA
R1	bias resistor	47	–	kΩ
R2	bias resistor	47	–	kΩ

DESCRIPTION

PNP resistor-equipped transistor (see “Simplified outline, symbol and pinning” for package details).

PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	NPN COMPLEMENT
	PHILIPS	EIAJ		
PDTA144EE	SOT416	SC-75	07	PDTC144EE
PDTA144EEF	SOT490	SC-89	07	PDTC144EEF
PDTA144EK	SOT346	SC-59	07	PDTC144EK
PDTA144EM	SOT883	SC-101	DR	PDTC144EM
PDTA144ES	SOT54 (TO-92)	SC-43	TA144E	PDTC144ES
PDTA144ET	SOT23	–	*07[1]	PDTC144ET
PDTA144EU	SOT323	SC-70	*07[1]	PDTC144EU

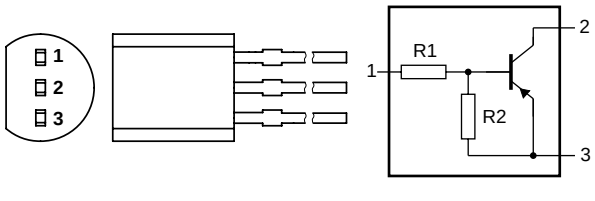
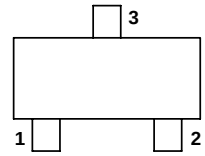
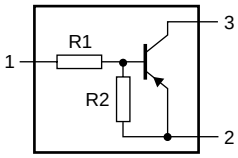
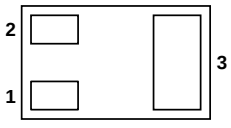
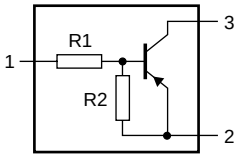
Note

1. * = p: Made in Hong Kong.
   * = t: Made in Malaysia.
   * = W: Made in China.

PNP resistor-equipped transistors; R1 = 47 kΩ, R2 = 47 kΩ

PDTA144E series

SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PDTA144ES	 MAM338	1 2 3	base collector emitter
PDTA144EE PDTA144EEF PDTA144EK PDTA144ET PDTA144EU	 Top view  MDB271	1 2 3	base emitter collector
PDTA144EM	 Bottom view  MDB267	1 2 3	base emitter collector

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	−	−50	V
V_{CEO}	collector-emitter voltage	open base	−	−50	V
V_{EBO}	emitter-base voltage	open collector	−	−10	V
V_I	input voltage				
	positive		−	+10	V
	negative		−	−40	V
I_O	output current (DC)		−	−100	mA
I_{CM}	peak collector current		−	−100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C			
	SOT54	note 1	−	500	mW
	SOT23	note 1	−	250	mW
	SOT346	note 1	−	250	mW
	SOT323	note 1	−	200	mW
	SOT416	note 1	−	150	mW
	SOT490	notes 1 and 2	−	250	mW
	SOT883	notes 2 and 3	−	250	mW
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		−	150	°C
T_{amb}	operating ambient temperature		−65	+150	°C

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μm copper strip line.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air		
	SOT54	note 1	250	K/W
	SOT23	note 1	500	K/W
	SOT346	note 1	500	K/W
	SOT323	note 1	625	K/W
	SOT416	note 1	833	K/W
	SOT490	notes 1 and 2	500	K/W
	SOT883	notes 2 and 3	500	K/W

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μm copper strip line.

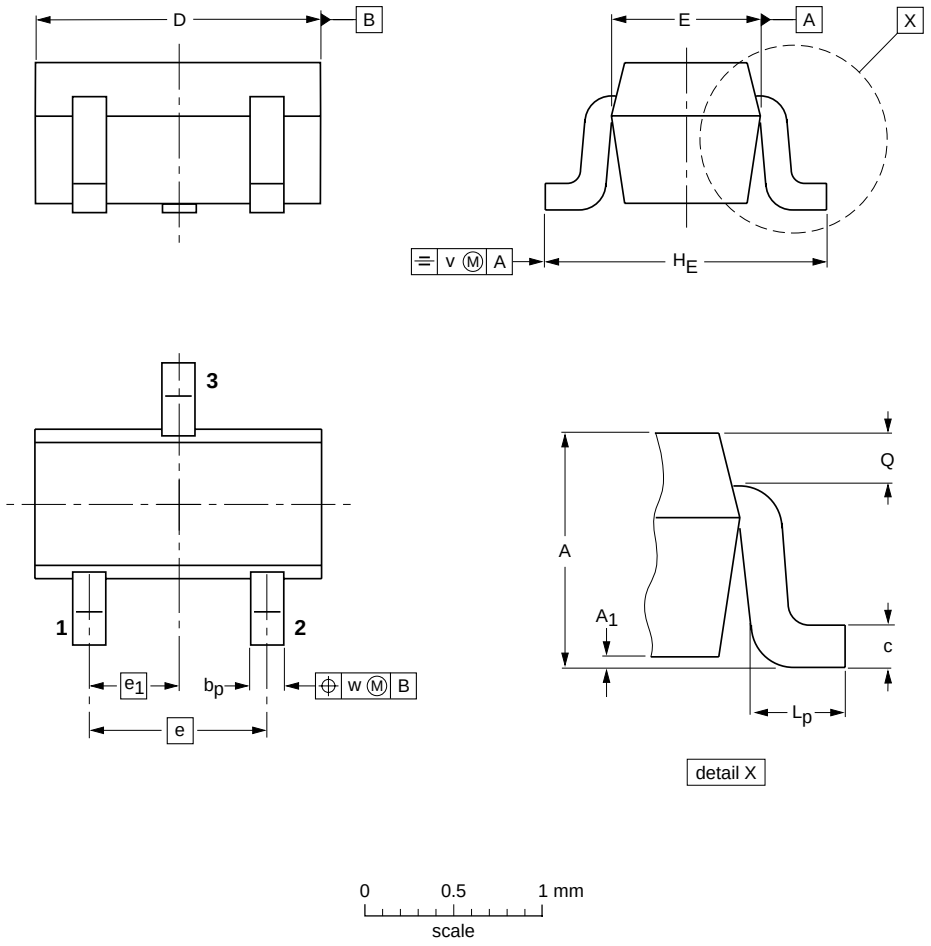
CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	V_{CB} = −50 V; I_E = 0	−	−	−100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = −30 V; I_B = 0	−	−	−1	μA
		V_{CE} = −30 V; I_B = 0; T_j = 150 °C	−	−	−50	μA
I_{EBO}	emitter-base cut-off current	V_{EB} = −5 V; I_C = 0	−	−	−90	μA
h_{FE}	DC current gain	V_{CE} = −5 V; I_C = −5 mA	80	−	−	
V_{CEsat}	collector-emitter saturation voltage	I_C = −10 mA; I_B = −0.5 mA	−	−	−150	mV
$V_{i(off)}$	input-off voltage	I_C = −100 μA; V_{CE} = −5 V	−	−1.2	−0.8	V
$V_{i(on)}$	input-on voltage	I_C = −2 mA; V_{CE} = −0.3 V	−3	−1.6	−	V
R1	input resistor		33	47	61	kΩ
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	
C_c	collector capacitance	$I_E = i_e$ = 0; V_{CB} = −10 V; f = 1 MHz	−	−	3	pF

PACKAGE OUTLINES

Plastic surface-mounted package; 3 leads **SOT416**

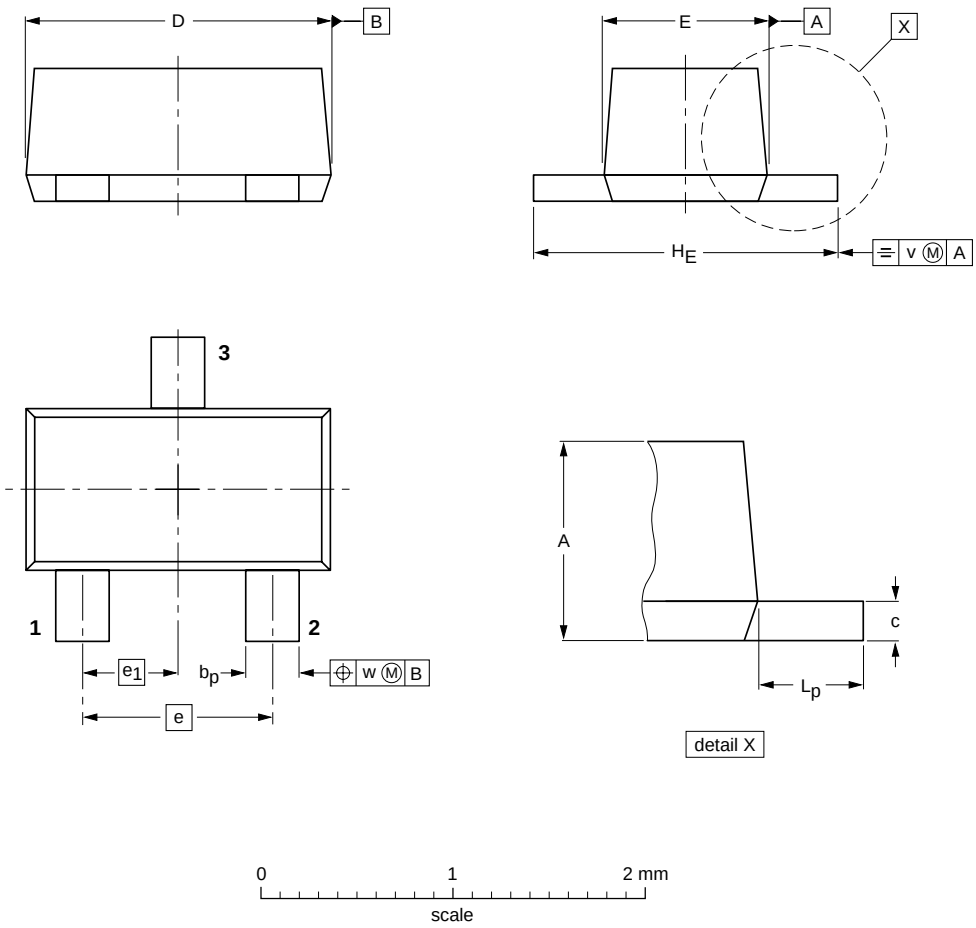


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	0.95 0.60	0.1	0.30 0.15	0.25 0.10	1.8 1.4	0.9 0.7	1	0.5	1.75 1.45	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT416			SC-75			~~04-11-04~~ 06-03-16

Plastic surface-mounted package; 3 leads **SOT490**

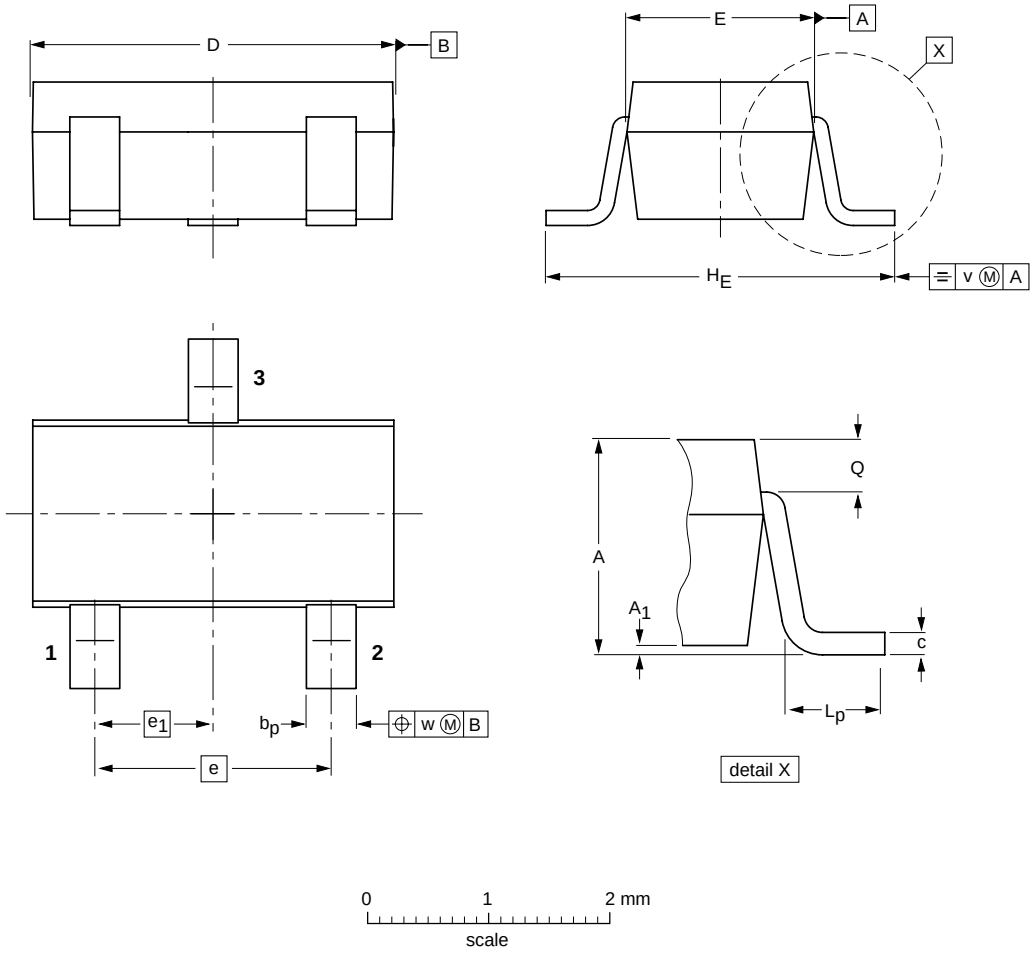


DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	H_E	L_p	v	w
mm	0.8 0.6	0.33 0.23	0.2 0.1	1.7 1.5	0.95 0.75	1.0	0.5	1.7 1.5	0.5 0.3	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT490			SC-89			~~05-07-28~~ 06-03-16

Plastic surface-mounted package; 3 leads **SOT346**

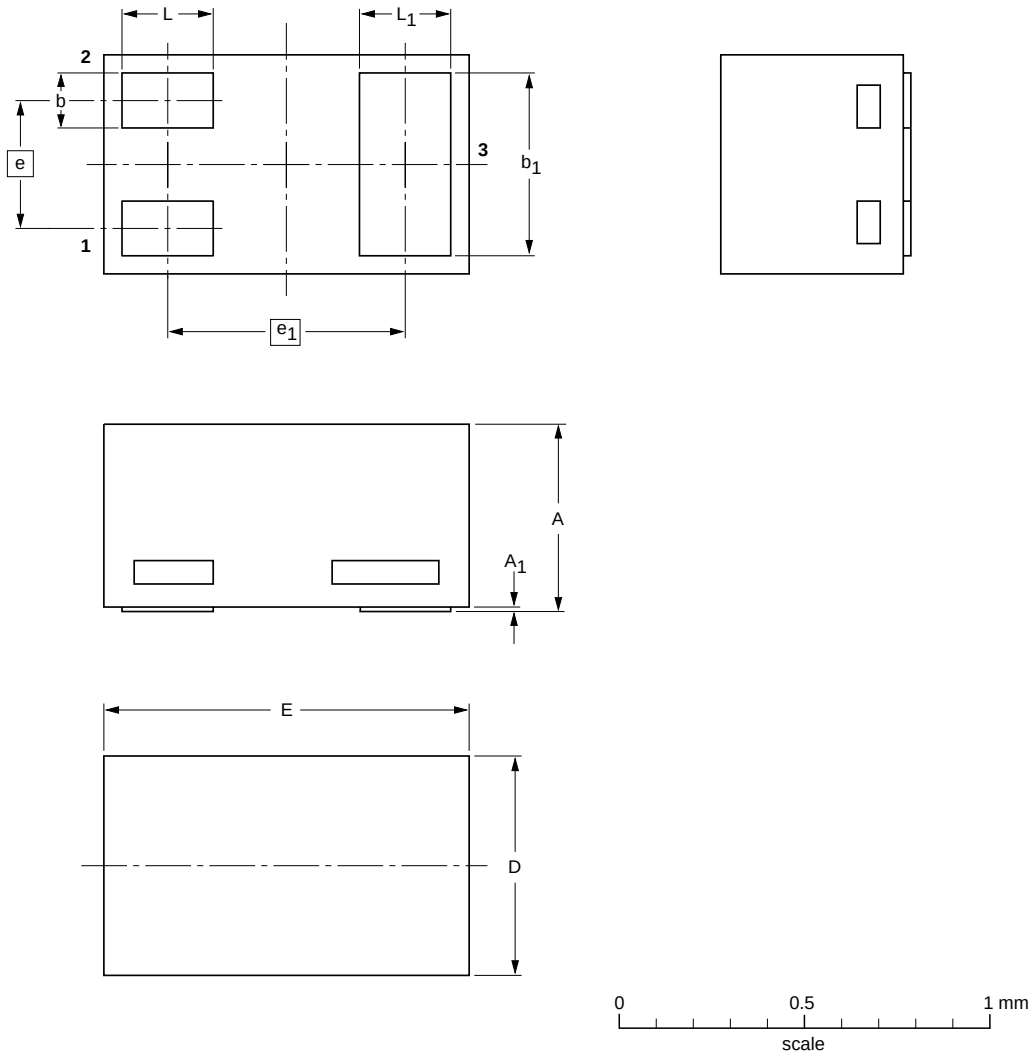


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.3 1.0	0.1 0.013	0.50 0.35	0.26 0.10	3.1 2.7	1.7 1.3	1.9	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT346		TO-236	SC-59A			~~04-11-11~~ 06-03-16

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm **SOT883**



DIMENSIONS (mm are the original dimensions)

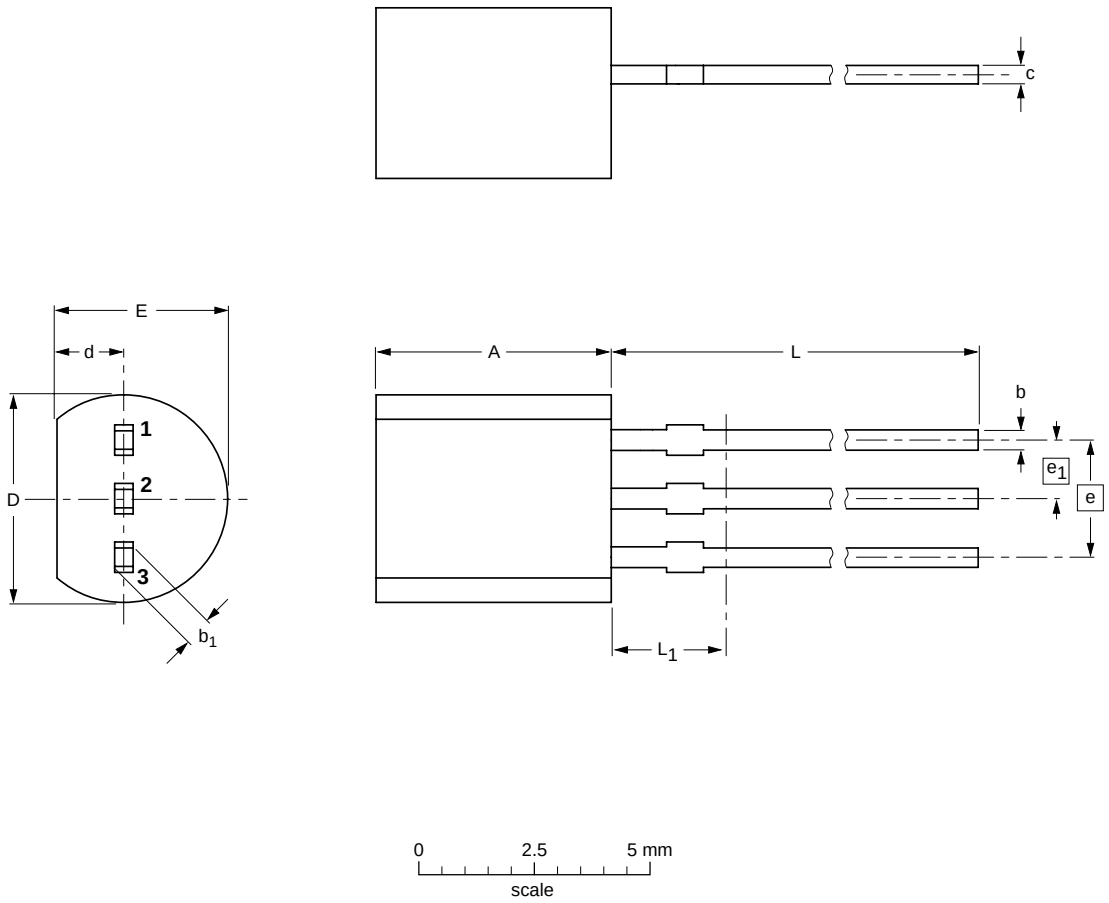
UNIT	A(1)	A_1 max.	b	b_1	D	E	e	e_1	L	L_1
mm	0.50 0.46	0.03	0.20 0.12	0.55 0.47	0.62 0.55	1.02 0.95	0.35	0.65	0.30 0.22	0.30 0.22

Note

1. Including plating thickness

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT883			SC-101			~~03-02-05~~ 03-04-03

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**



DIMENSIONS (mm are the original dimensions)

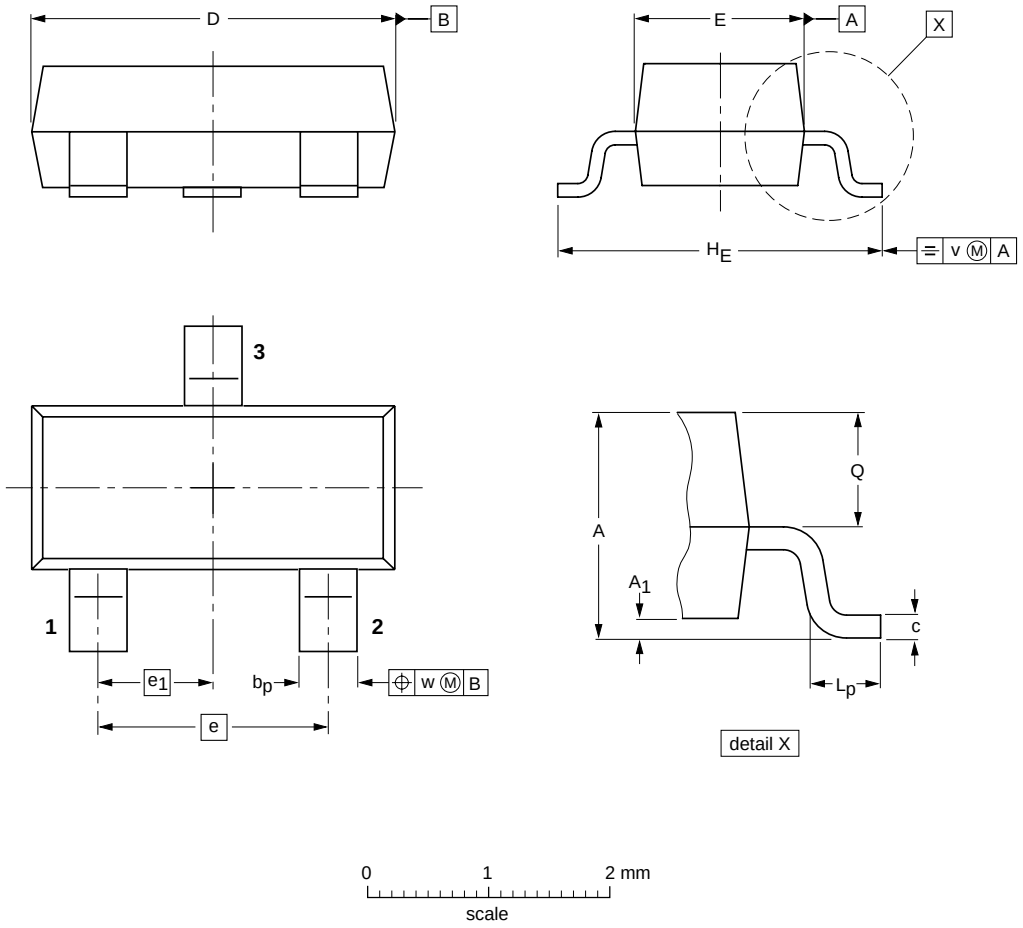
UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1 (1) max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			~~04-06-28~~ 04-11-16

Plastic surface-mounted package; 3 leads **SOT23**

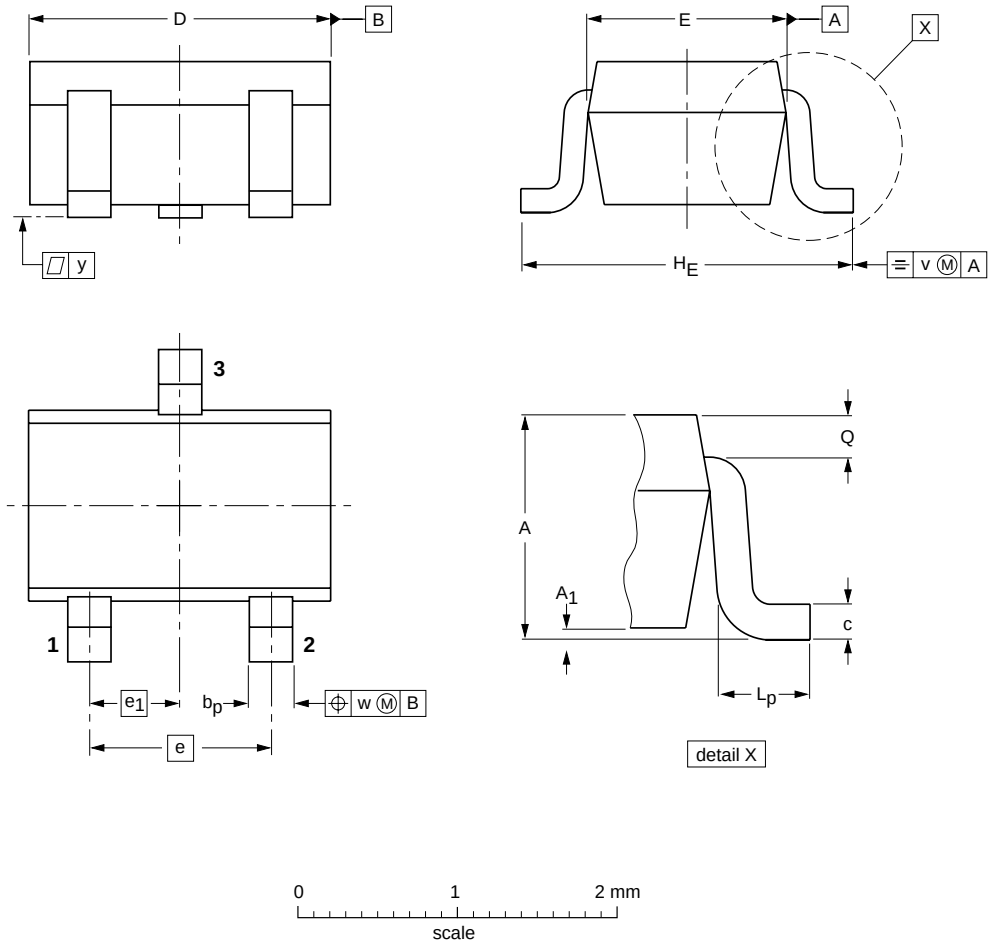


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT23		TO-236AB				~~04-11-04~~ 06-03-16

Plastic surface-mounted package; 3 leads **SOT323**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT323			SC-70			~~04-11-04~~ 06-03-16

DATA SHEET STATUS

DOCUMENT STATUS[1]	PRODUCT STATUS[2]	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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2. The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Contact information

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