

PESD2V5Y1BSF

Extremely low capacitance bidirectional ESD protection diode

8 April 2021 Product data sheet

1. General description

Extremely low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode, part of the TrEOS protection family. This device is housed in a DSN0603-2 (SOD962-2) leadless ultra small Surface-Mounted Device (SMD) package designed to protect one signal line from the damage caused by ESD and other transients.

2. Features and benefits

- Bidirectional ESD protection of one line
- Extremely low trigger-voltage V_{t1} < 5 V
- Extremely low diode capacitance C_d = 0.25 pF
- Extremely low clamping voltage to protect sensitive I/Os
- Extremely low-inductance protection path to ground
- ESD protection up to ±15 kV according to IEC 61000-4-2
- Ultra small SMD package

3. Applications

- Thunderbolt and USB 3.2 data lines
- Cellular handsets and accessories
- Portable electronics
- Communication systems
- Computers and peripherals

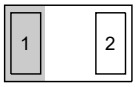
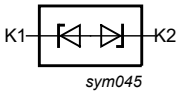
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage			-2.5	-	2.5	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V		-	0.25	0.3	pF

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 Transparent top view **DSN0603-2 (SOD962-2)**	
2	K2	cathode (diode 2)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD2V5Y1BSF	DSN0603-2	silicon, leadless ultra small package; 2 terminals; 0.4 mm pitch; 0.6 mm x 0.3 mm x 0.3 mm body	SOD962-2

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD2V5Y1BSF	C8

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{RWM}	reverse standoff voltage			-2.5	2.5	V
T_{amb}	ambient temperature			-40	125	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[1]	-15	15	kV
		IEC 61000-4-2; air discharge	[1]	-15	15	kV

[1] Device stressed with ten non-repetitive ESD pulses.

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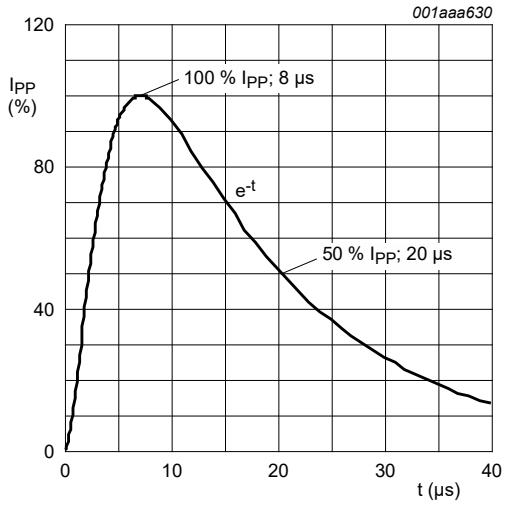


Fig. 1. 8/20 µs pulse waveform according to IEC 61000-4-5 and IEC 61643-321

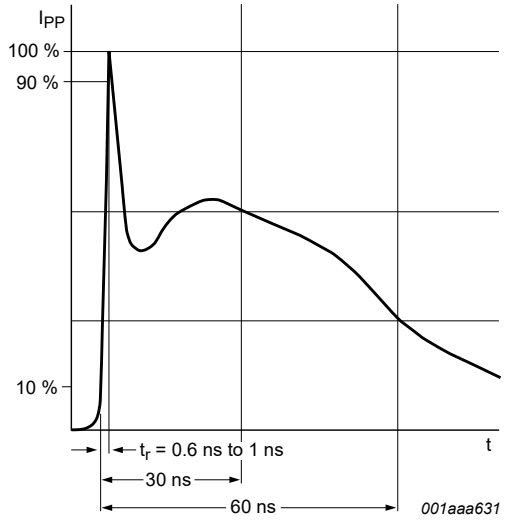


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BR}	breakdown voltage	I_R = 1 mA		-	4.1	-	V
I_{RM}	reverse leakage current	V_{RWM} = 2.5 V		-	1	50	nA
C_d	diode capacitance	f = 1 MHz; V_R = 0 V		-	0.25	0.3	pF
		f = 1 MHz; V_R = 1 V		-	0.24	-	pF
V_{CL}	clamping voltage	I_{PPM} = 4 A	[1]	-	3.9	-	V
R_{dyn}	dynamic resistance	I_R = 10 A	[2]	-	0.23	-	Ω
		I_R = -10 A	[2]	-	0.23	-	Ω
f_{-3dB}	-3 dB cut-off frequency	normalized to attenuation at 1 MHz		-	18	-	GHz

[1] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
[2] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.

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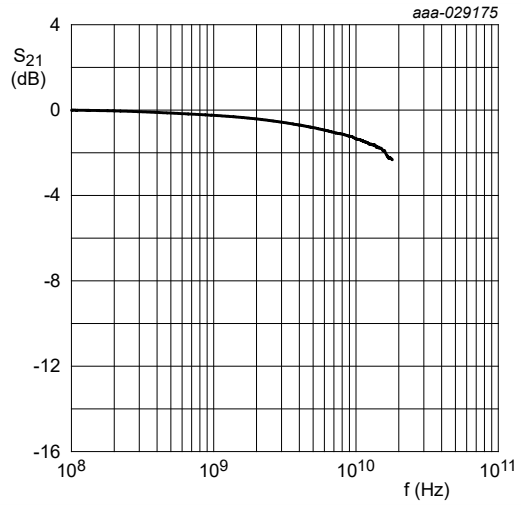
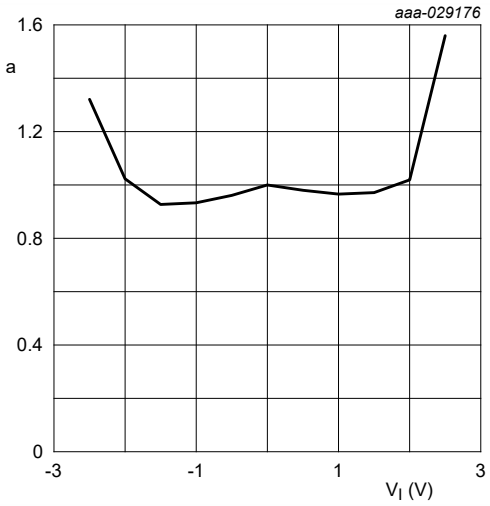
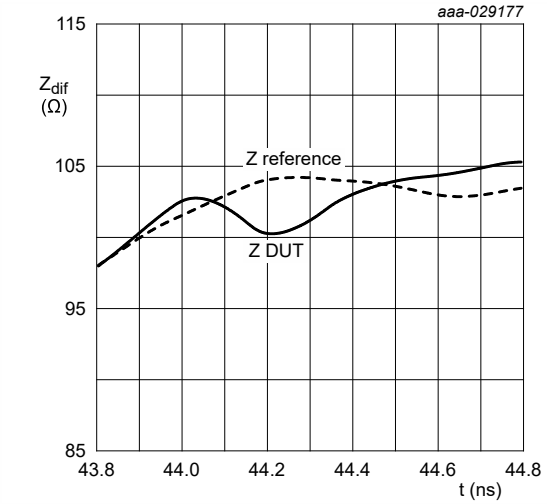


Fig. 3. Insertion loss; typical values



$$a = \frac{C_d}{C_d(V_I = 0\ V)}$$

Fig. 4. Relative capacitance as a function of input voltage; typical values

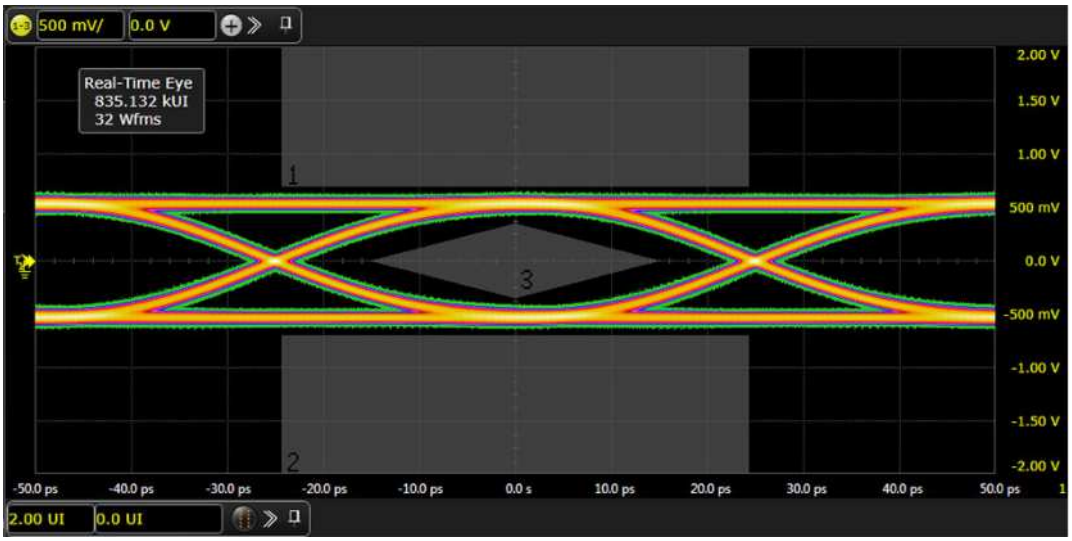


rise time = 200 ps

Fig. 5. Differential Time Domain Reflectometer (TDR) plot; typical values

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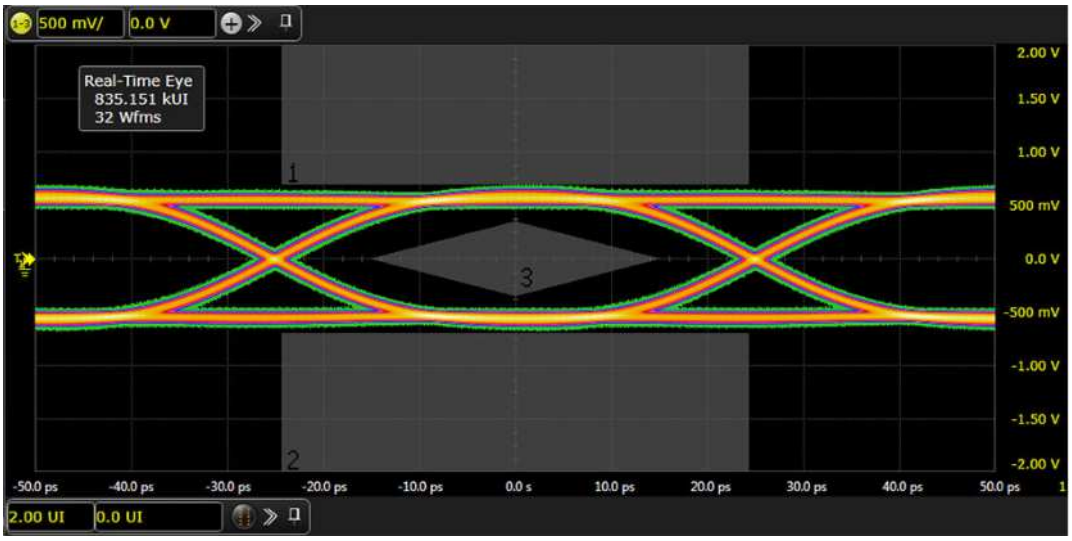
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aaa-030227

Data rate: 20 Gbit/s

Fig. 6. Thunderbolt eye diagram with device; typical values



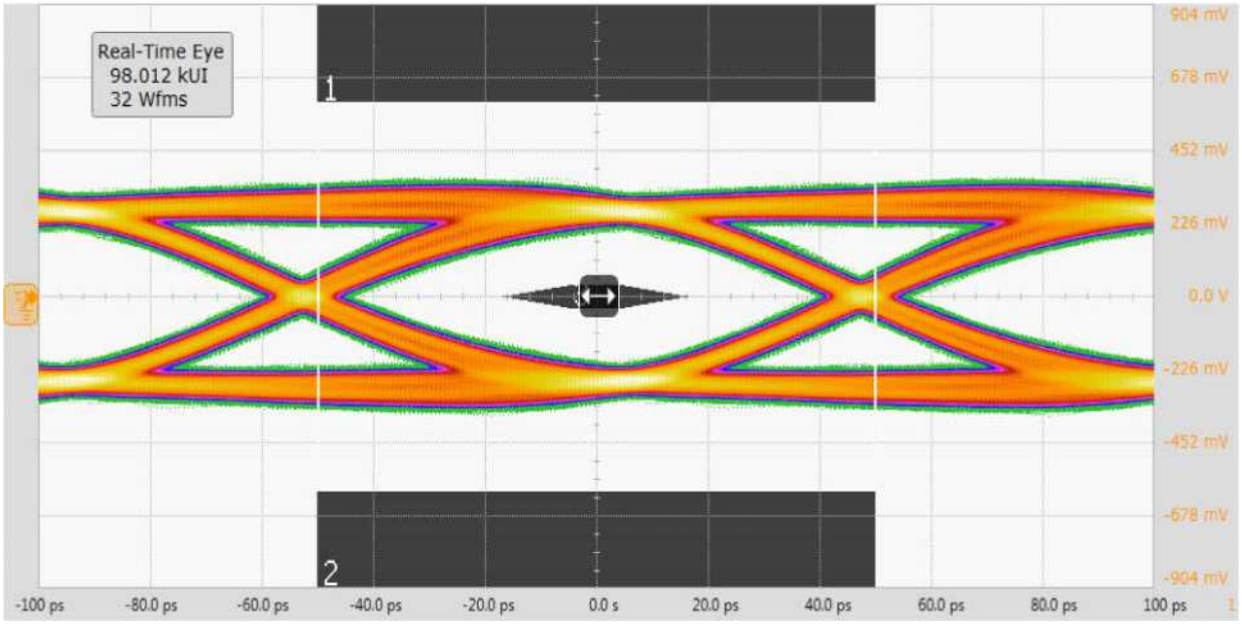
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Data rate: 20 Gbit/s

Fig. 7. Thunderbolt eye diagram without device; typical values

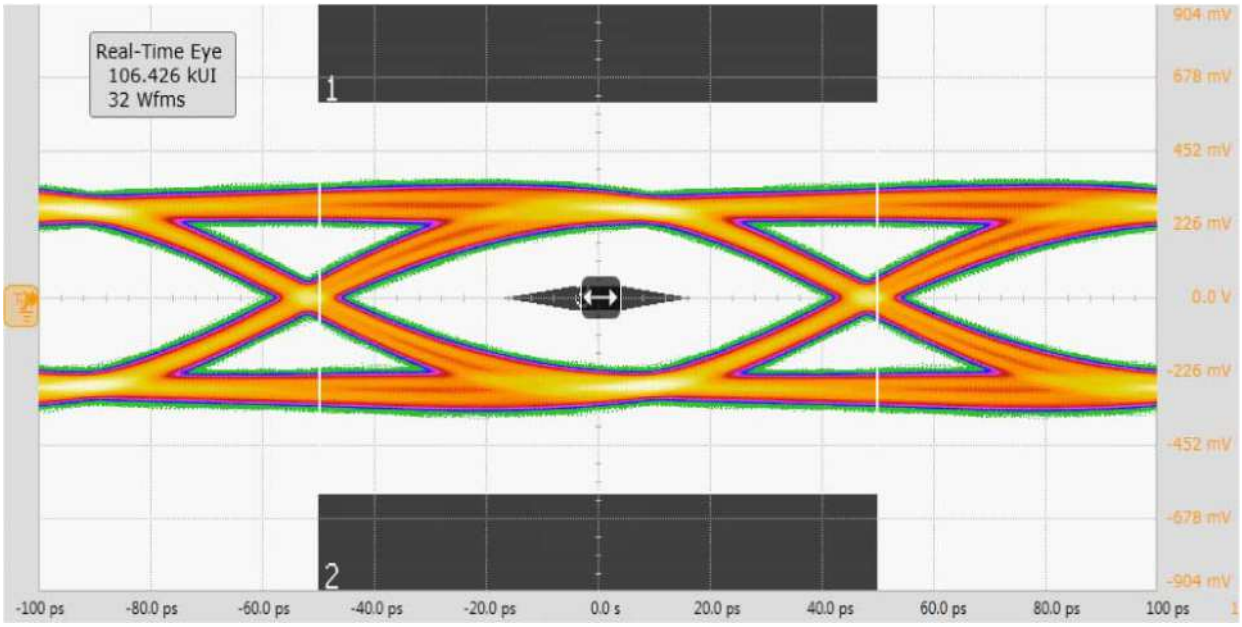
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Data rate: 10 Gbit/s

Fig. 8. USB 3.2 eye diagram, test board with device; typical values

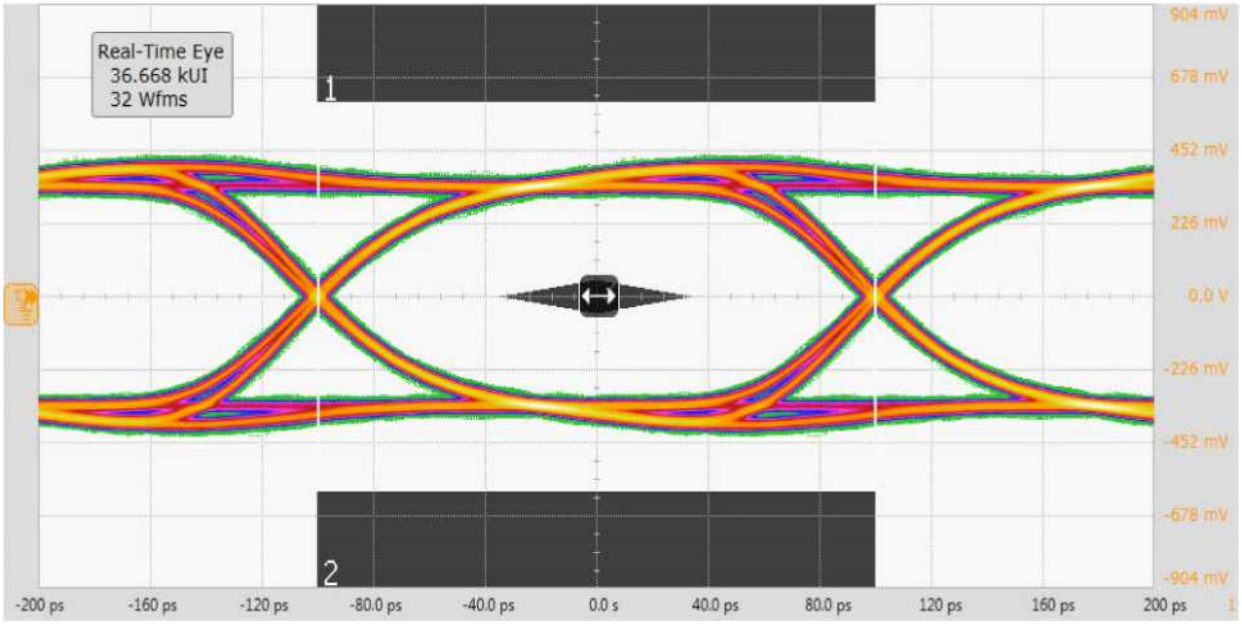


Data rate: 10 Gbit/s

Fig. 9. USB 3.2 eye diagram, test board without device; typical values

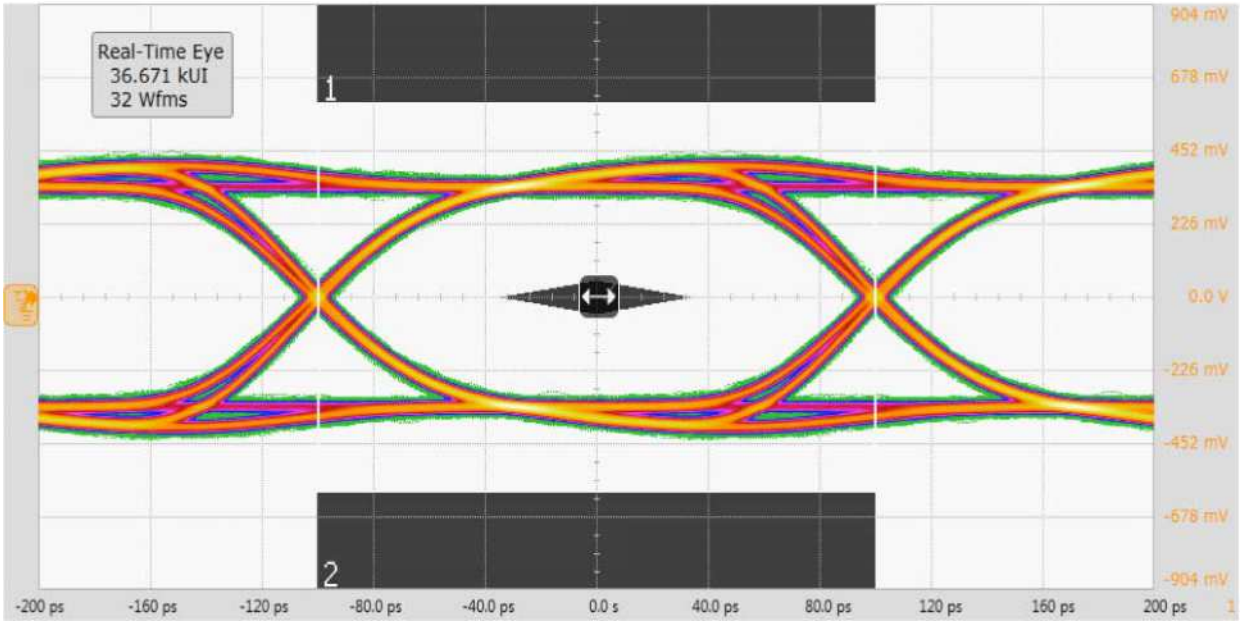
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Data rate: 5 Gbit/s

Fig. 10. USB 3.2 eye diagram, test board with device; typical values

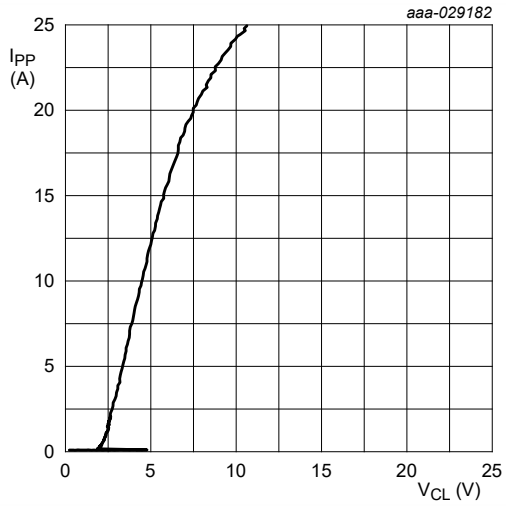


Data rate: 5 Gbit/s

Fig. 11. USB 3.2 eye diagram, test board without device; typical values

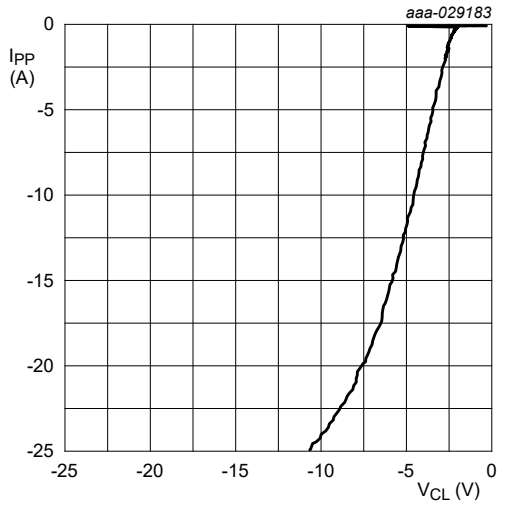
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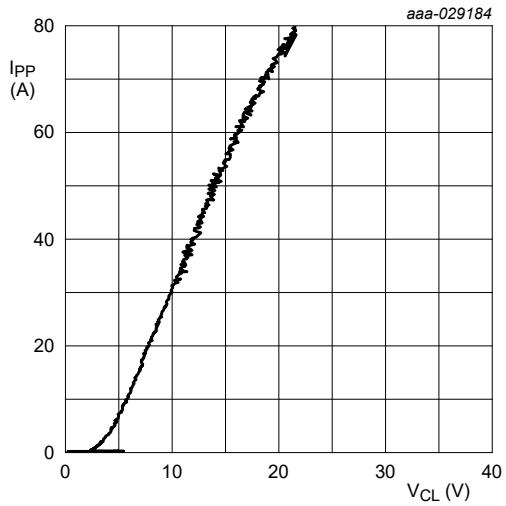
t_r = 600 ps
t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 12. Dynamic resistance with positive clamping; typical values



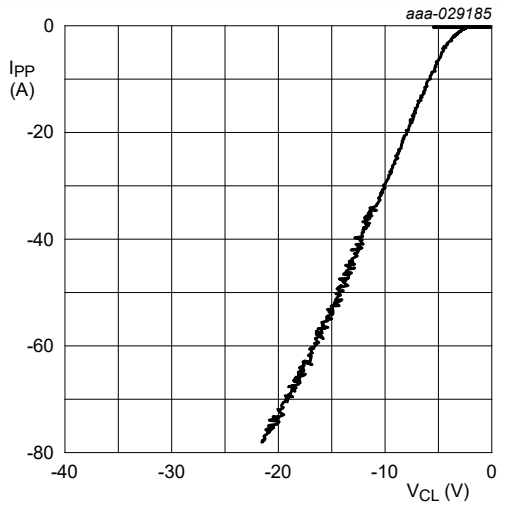
t_r = 600 ps
t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 13. Dynamic resistance with negative clamping; typical values



t_r = 600 ps
t_p = 5 ns; Very-Fast Transmission Line Pulse (VF-TLP)

Fig. 14. Dynamic resistance with positive clamping; typical values



t_r = 600 ps
t_p = 5 ns; Very-Fast Transmission Line Pulse (VF-TLP)

Fig. 15. Dynamic resistance with negative clamping; typical values

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10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

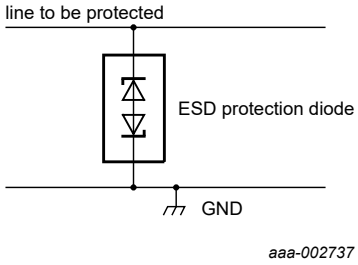


Fig. 16. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

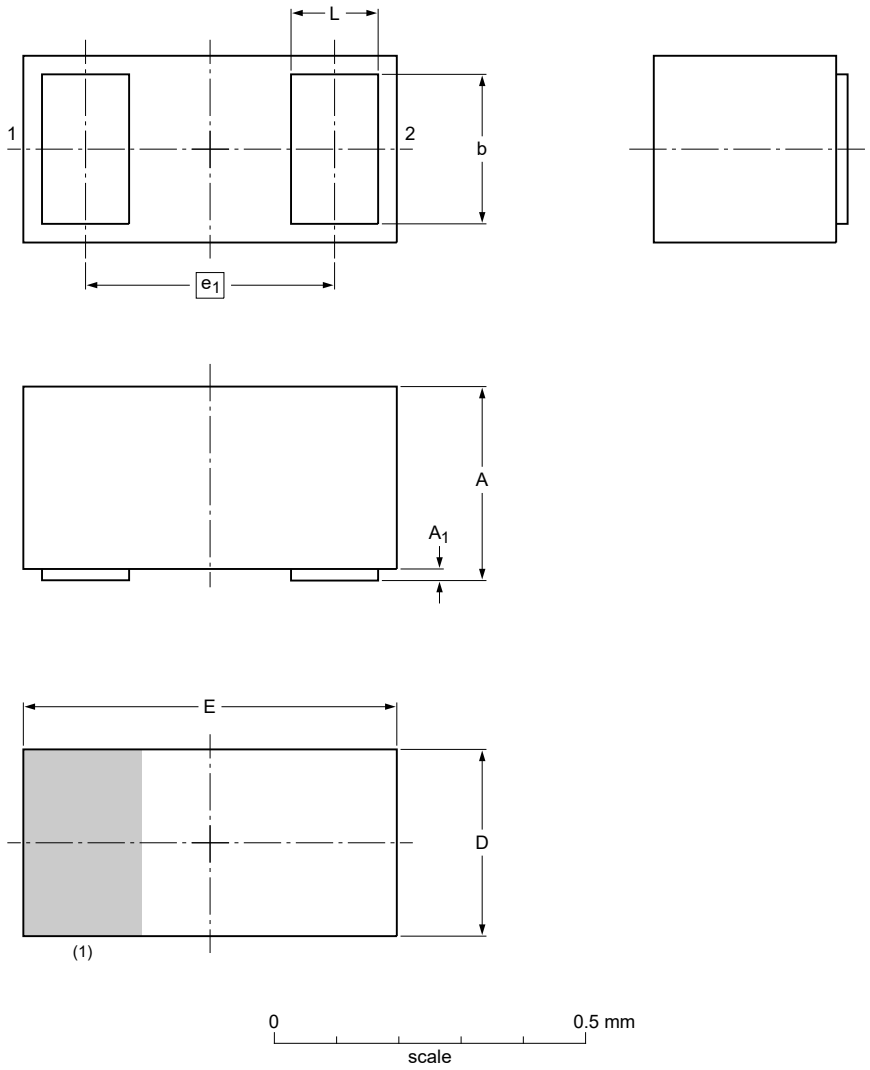
1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

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11. Package outline

Leadless ultra small package; 2 terminals; body 0.6 x 0.3 x 0.3 mm **SOD962-2**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	D	E	e_1	L
mm	max	0.32	0.03	0.25	0.325	0.625		0.15
	nom						0.4	
	min	0.28		0.23	0.275	0.575		0.13

Note
1. The marking bar indicates the cathode.

sod962-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOD962-2						~~13-07-12~~ 13-07-17

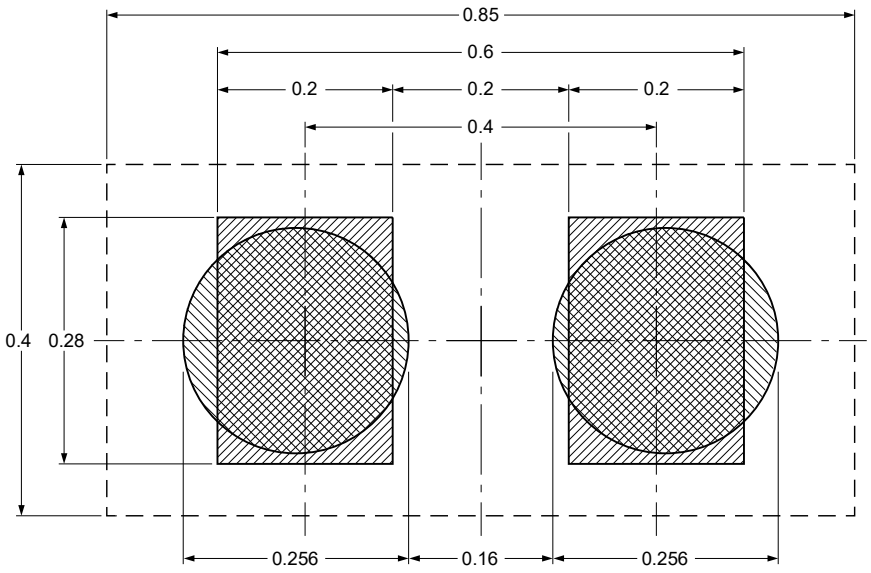
Fig. 17. Package outline DSN0603-2 (SOD962-2)

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12. Soldering

Footprint information for reflow soldering of leadless ultra small package; 2 terminals **SOD962-2**



recommended stencil thickness: 0.1 mm

occupied area

solder paste

solder lands

Dimensions in mm

Issue date ~~16-02-01~~ 20-09-15

sod962-2_fr

Fig. 18. Reflow soldering footprint for DSN0603-2 (SOD962-2)

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13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD2V5Y1BSF v.4	20210408	Product data sheet	-	PESD2V5Y1BSF v.3
Modifications:	• Figure "Reflow soldering footprint" updated			
PESD2V5Y1BSF v.3	20190816	Product data sheet	-	PESD2V5Y1BSF v.2
PESD2V5Y1BSF v.2	20190131	Product data sheet	-	PESD2V5Y1BSF v.1
PESD2V5Y1BSF v.1	20181017	Preliminary data sheet	-	-

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14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
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